MOSFET Silicon N-Channel MOS

1. Applications

For Soft Switching Boost PFC switch, HB or AHB or LLC half bridge and full bridge topologies.
Such as phase-shift-bridge(ZVS),LLC Application-Server Power, Telecom Power,EV Charging, Solar inverter.

2. Features

Low drain-source on-resistance: RDS(ON) = 0.035Ω (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 3 to 5 V

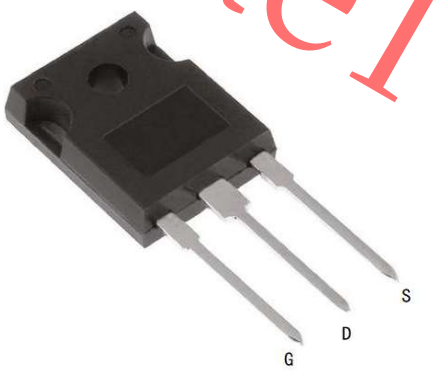
Table 1 Key Performance Parameters

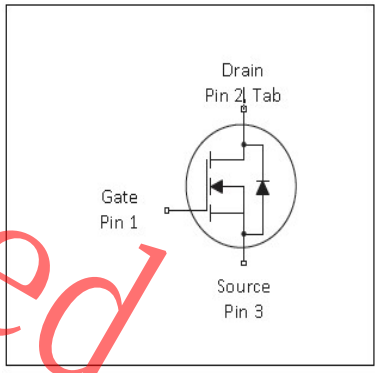
Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$R_{DS(on),max}$	41	mΩ
$Q_{g,typ}$	290.6	nC
$I_{D,pulse}$	240	A
Body diode dv/dt	50	V/ns

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASW65R041EFDA	TO247	ASW65R041EFDA

TO247





1 Maximumratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximumratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D		-	80	A	T_C=25°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	240	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	16000	mJ	Tc=25°C,VDD=50V,L = 20mH, RG=25Ω
Avalanche current, single pulse	I_{AR}	-	-	10	A	Tc=25°C,VDD=50V,L = 20mH, RG=25Ω
MOSFET dv/dt ruggedness	dv/dt	-	-	26	V/ns	V_{DS}=0...150V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	500	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	
Operating junction temperature	T_j	-55	-	150	°C	
Reverse diode dv/dt[3]	dv/dt	-	-	50	V/ns	V_{DS}=0...400V, I_{SD}<=48A, T_j=25°C see table 8

[1] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Thermal resistance, junction	- case	R_{thJC}	-	-	0.205	°C/W	-
Thermal resistance, junction	- ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	655	-	-	V	V_{GS}=0V, I_D=10mA
Gate threshold voltage	$V_{(GS)th}$	3		5	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	5	uA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=30V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.035	0.041	Ω	V_{GS}=10V, I_D=28A, T_j=25°C
Gate resistance (Intrinsic)	R_G	-	13	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	7356	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Output capacitance	C_{oss}	-	436	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Reverse transfer capacitance	C_{rss}	-	12.1	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Turn-on delay time	$t_{d(on)}$	-	63.7	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=49.6A R_G=1.7Ω; see table 9
Rise time	t_r	-	28.4	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=49.6A R_G=1.7Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	270	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=49.6A R_G=1.7Ω; see table 9
Fall time	t_f	-	24.1	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=49.6A R_G=1.7Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	46.1	-	nC	V_{DD} =480V, I_D =49.6A, V_{GS} =10V
Gate to drain charge	Q_{gd}	-	151.3	-	nC	V_{DD} =480V, I_D =49.6A, V_{GS} =10V
Gate charge total	Q_g	-	290.6	-	nC	V_{DD} =480V, I_D =49.6A, V_{GS} =10V
Gate plateau voltage	$V_{plateau}$	-	7.8	-	V	V_{DD} =480V, I_D =49.6A, V_{GS} =10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.61	-	V	V_{GS}=0V, I_F=1A, T_j=25°C
Reverse recovery time	t_{rr}	-	193.5	-	ns	Vr=400v,IF=49.6A,di/dt=100A/us see table 8
Reverse recovery charge	Q_{rr}	-	1.67	-	uC	Vr=400v,IF=49.6A,di/dt=100A/us see table 8
Peak reverse recovery current	I_{rrm}	-	14.5	-	A	Vr=400v,IF=49.6A,di/dt=100A/us see table 8

4 Electrical characteristics diagram

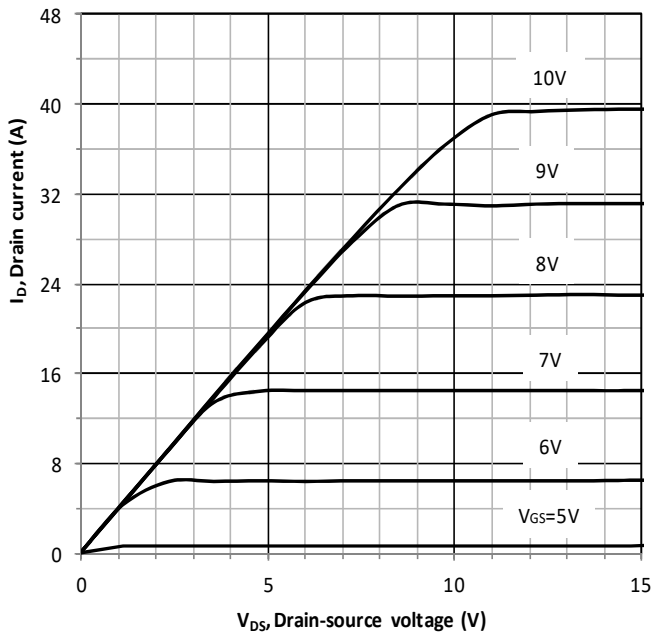
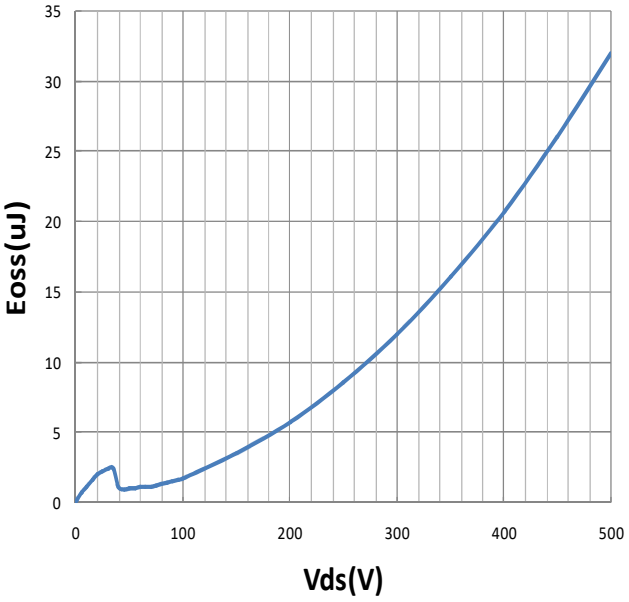
Diagram 1: Typ. output characteristics	Diagram 2: Typ. Coss stored energy
	
I_D=f(V_{DS});T_j=25 °C; parameter: V_{GS}	*Eoss=f(VDS)*

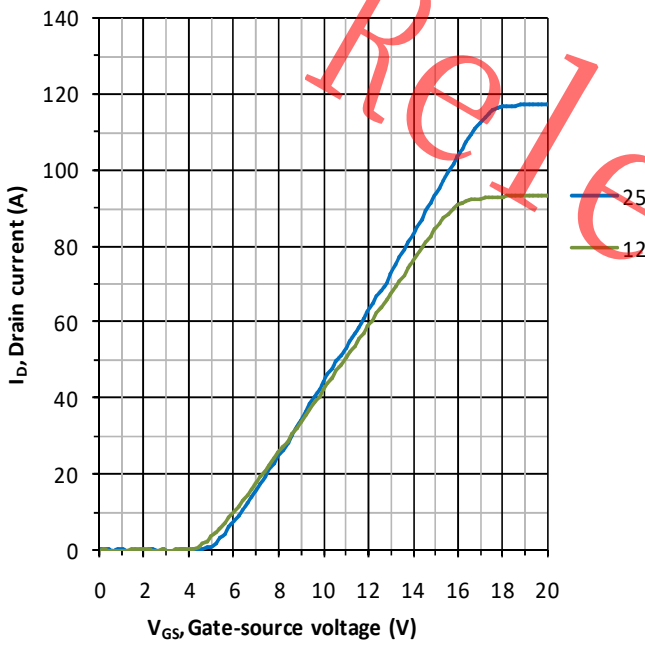
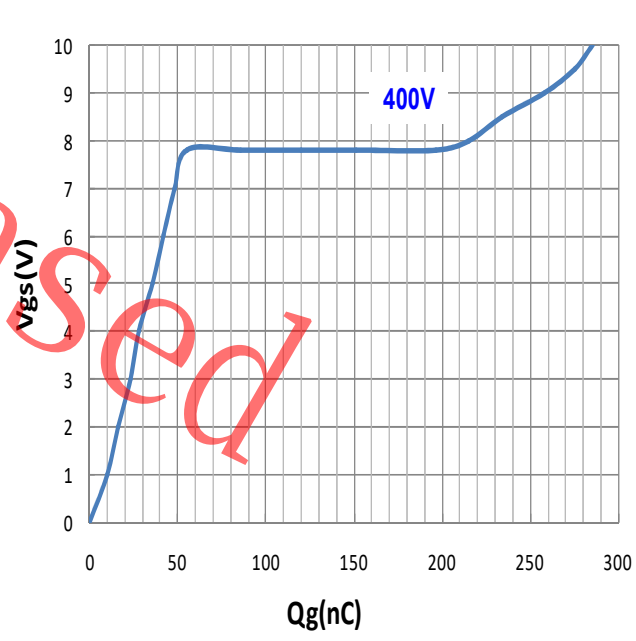
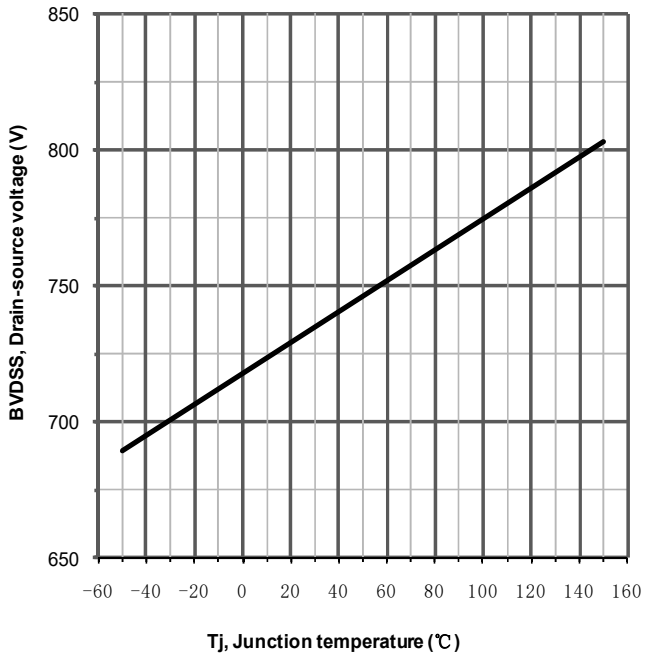
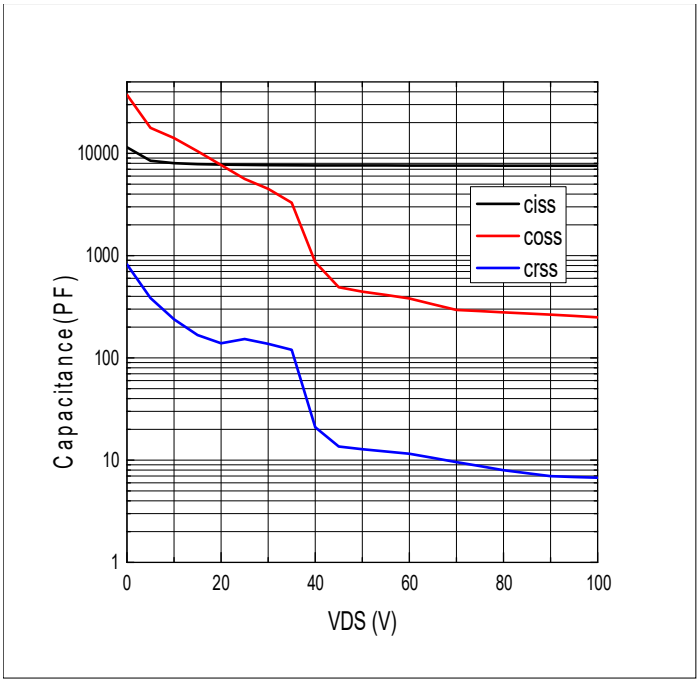
Diagram 3: Typ. transfer characteristics	Diagram 4: Typ. gate charge
	
I_D=f(V_{GS});parameter: T_j	V_{GS}=f(Q_{gate});I_D=49.6A pulsed; parameter: V_{DD}

Diagram 5: Drain-source breakdown voltage



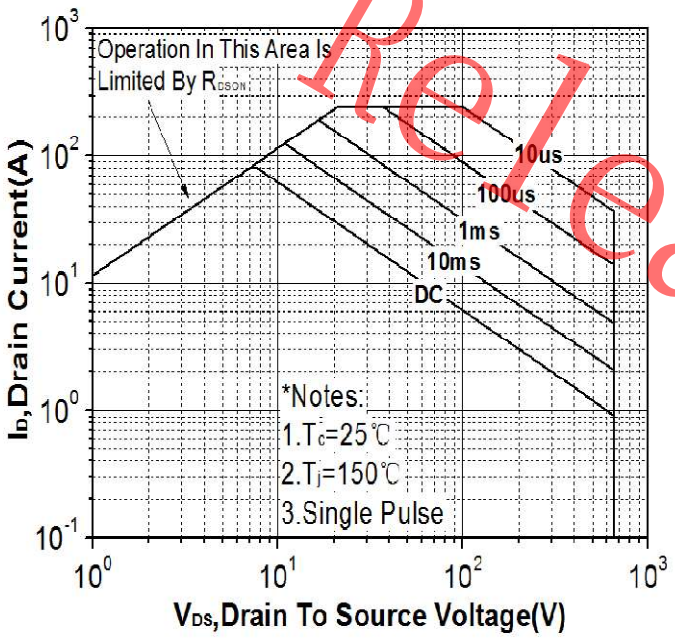
$V_{BR(DSS)}$=f(T_j);I_D=10mA

Diagram 6: Typ. capacitances



C=f(V_{DS});V_{GS}=0V; f=10 kHz

Diagram 7: Safe operating area T_C=25 °C， TO247



I_D=f(V_{DS}); T_C=25 °C; V_{GS}> 7V; D=0; parameter tp

5 Test Circuits

Table 8 Diode characteristics

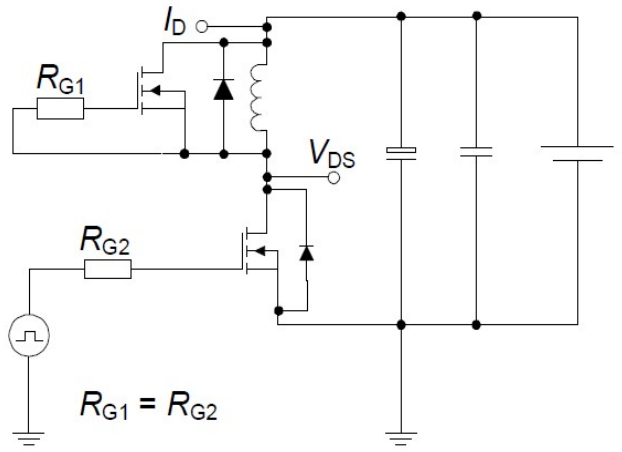
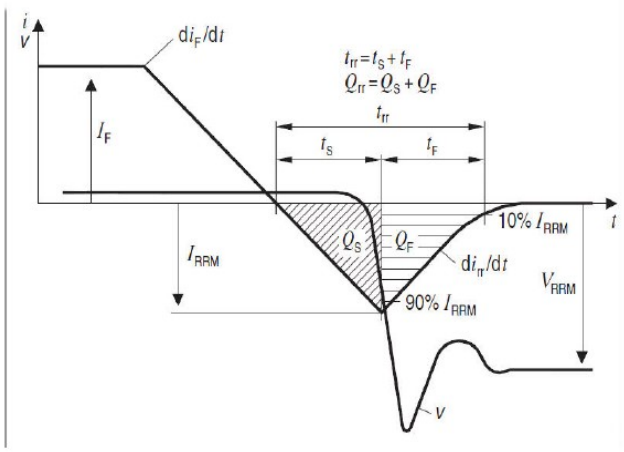
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

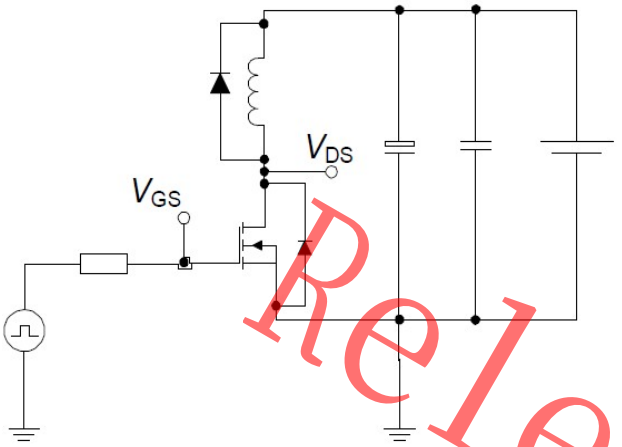
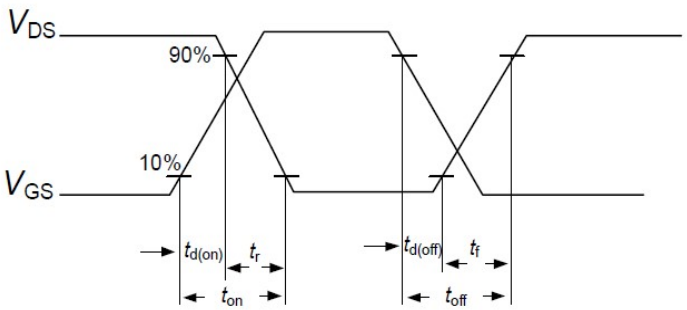
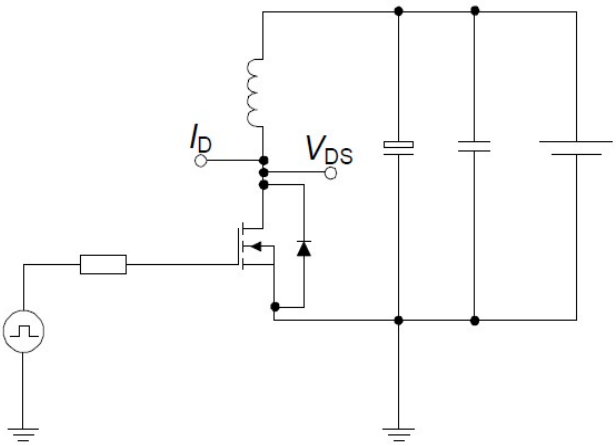
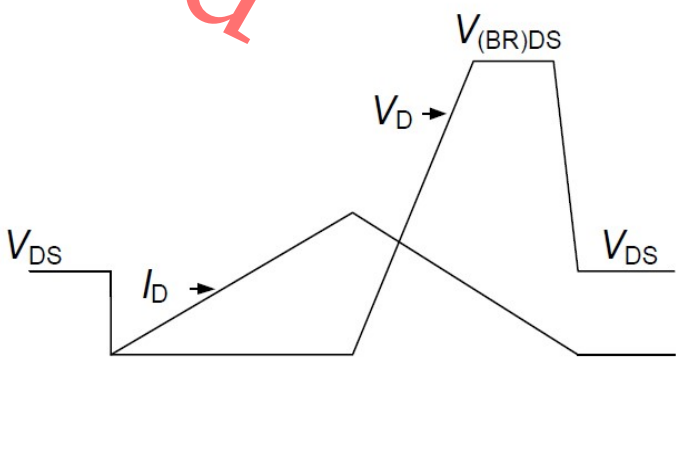
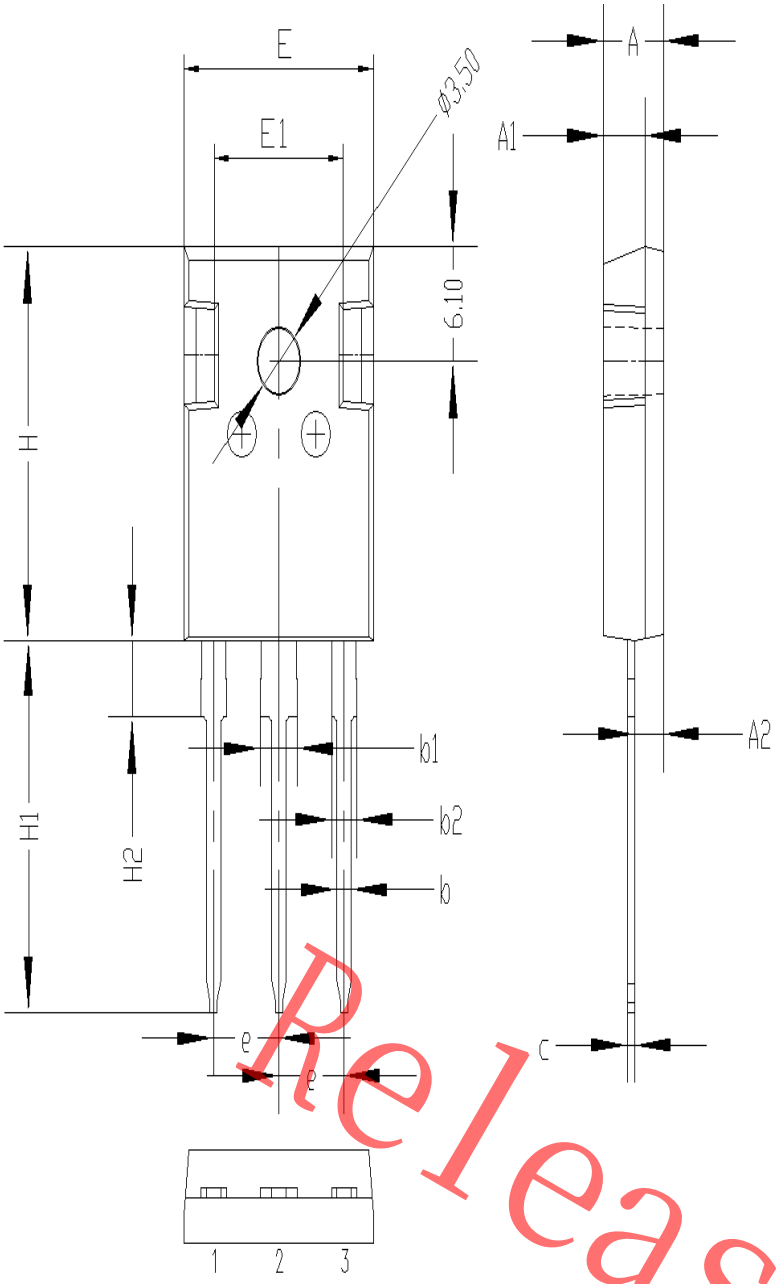
Switching times test circuit for inductive load	Switching times waveform
	

Table10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



	单位: mm		
	MIN	NOM	MAX
A	4.8	5	5.2
A1	3.3	3.5	3.7
A2	2.1	2.3	2.5
b	1	1.2	1.4
b1	2.9	3.1	3.3
b2	1.9	2.1	2.3
c	0.4	0.6	0.8
e	5.25	5.45	5.65
E	15.6	15.8	16
E1	10.6	10.8	11
H	20.8	21	21.2
H1	19.4	19.9	20.4
H2	3.9	4.1	4.3
G	5.9	6.1	6.3
ØP	3.3	3.5	3.7

Figure1：Outline PG-TO247

Revision History

Revision	Date	Subjects (major changes since last revision)
0.1	2019-05-21	Preliminary version
1.0	2019-11-07	Fine tune outline and add Crss test data.etc
1.1	2020-04-05	Add Electrical characteristics Curve
1.2	2020-04-18	Add avalanche energy test condition, avalanche current data and test condition