ASA60R330E, ASD60R330E, ASM60R330E

MOSFET Silicon N-Channel MOS

1. Applications

Boost PFC switch,single-ended flyback or two-transistor forward,
Half bridge or Asymmetric half bridge or Series resonance half bridge topologies. .
PC power, PD Adaptor,LCD & PDP TV, LED Lighting,Server power,UPS application.

2. Features

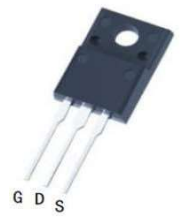
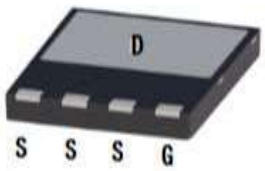
Low drain-source on-resistance: RDS(ON) = 0.305Ω (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 2.8 to 4.2 V

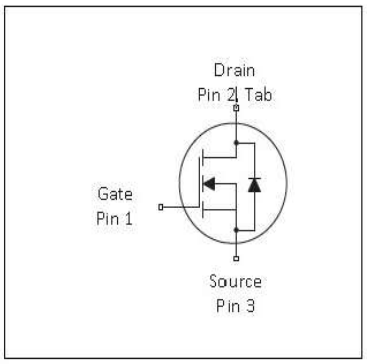
Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	330	mΩ
$Q_{g,typ}$	22	nC
$I_{D,pulse}$	33	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASA60R330E	TO220F	ASA60R330E
ASD60R330E	TO252	ASD60R330E
ASM60R330E	DFN8x8	ASM60R330E

TO220F	TO252	DFN8x8
		



1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D		-	11	A	T_C=25°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	33	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	400	mJ	Tc=25°C,VDD=50V,L= 10mH, RG=25Ω
Avalanche current, single pulse	I_{AR}	-	-	7	A	Tc=25°C,VDD=50V,L = 10mH, RG=25Ω
MOSFET dv/dt ruggedness	dv/dt	-	-	70	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation (TO220F)	P_{tot}	-	-	32	W	T_C=25°C
Power dissipation (TO252)	P_{tot}	-	-	83	W	T_C=25°C
Power dissipation (DFN8x8)	P_{tot}	-	-	176	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	
Operating junction temperature	T_j	-55	-	150	°C	
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS}=0...400V, I_{SD}<=48A, T_j=25°C see table 8

[1] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics（TO220 FullPAK）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.9	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	device on PCB, minimal footprint

Thermal characteristics（TO252）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

Thermal characteristics（DFN8x8）

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.71	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	605	-	-	V	V_{GS}=0V, I_D=10mA
Gate threshold voltage	$V_{(GS)th}$	2.8		4.2	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	1	uA	V_{DS}=600V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=30V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.305	0.33	Ω	V_{GS}=10V, I_D=5.5A, T_j=25°C
Gate resistance (Intrinsic)	R_G	2	4.8	9.6		f=1MHz

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	720	901	1082	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Output capacitance	C_{oss}	47	59	71	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Reverse transfer capacitance	C_{rss}	4.2	5.3	6.4	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Turn-on delay time	$t_{d(on)}$	5.7	7.2	8.6	ns	V_{DD}=400V,V_{GS}=13V,I_D=4.8A, R_G=3.4Ω;see table 9
Rise time	t_r	16.6	20.8	24.9	ns	V_{DD}=400V,V_{GS}=13V,I_D=4.8A, R_G=3.4Ω;see table 9
Turn-off delay time	$t_{d(off)}$	23.3	29.2	35.1	ns	V_{DD}=400V,V_{GS}=13V,I_D=4.8A, R_G=3.4Ω;see table 9
Fall time	t_f	15.3	19.2	23.1	ns	V_{DD}=400V,V_{GS}=13V,I_D=4.8A, R_G=3.4Ω;see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	4.6	5.8	7.1	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	13.6	17	20.4	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate charge total	Q_g	17.5	22	26.5	nC	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	4.2	5.3	6.4	V	V_{DD}=400V, I_D=4.8A, V_{GS}=0 to 10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	0.5	0.74	1.2	V	V_{GS}=0V, I_F=1A, T_j=25°C
Reverse recovery time	t_{rr}	200	250	300	ns	V_R=400V, I_F=4.8 A, di_F/dt=100A/μs; see table 8
Reverse recovery charge	Q_{rr}	2.057	2.572	3.086	uC	V_R=400V, I_F=4.8 A, di_F/dt=100A/μs; see table 8
Peak reverse recovery current	I_{rrm}	15.7	19.6	23.5	A	V_R=400V, I_F=4.8 A, di_F/dt=100A/μs; see table 8

4 Electrical characteristics diagram

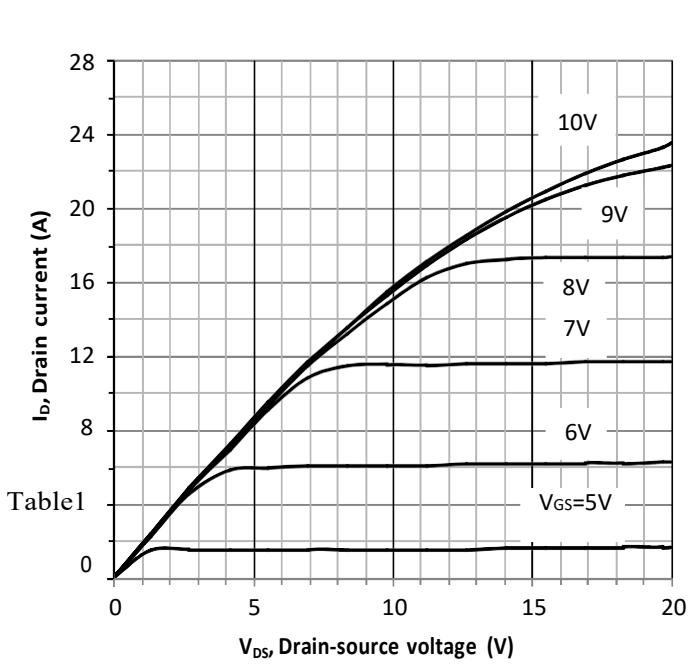
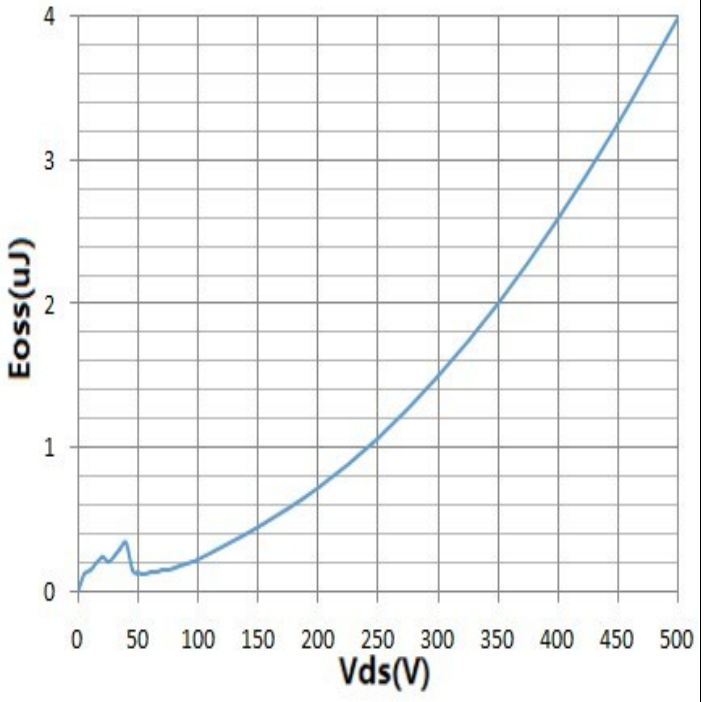
Diagram 1: Typ. Output characteristics	Diagram 2: Typ. Coss stored energy
	
I_D=f(V_{DS});T_j=25 °C; parameter: V_{GS}	*Eoss=f(VDS)*

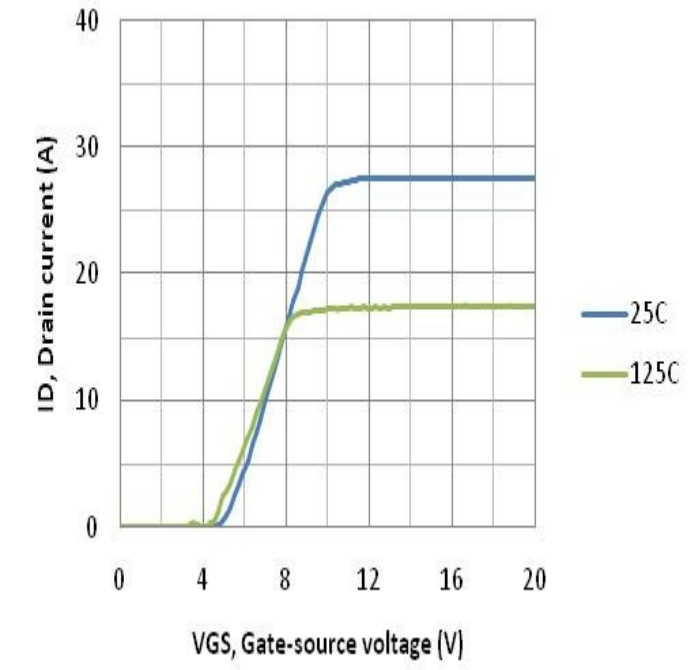
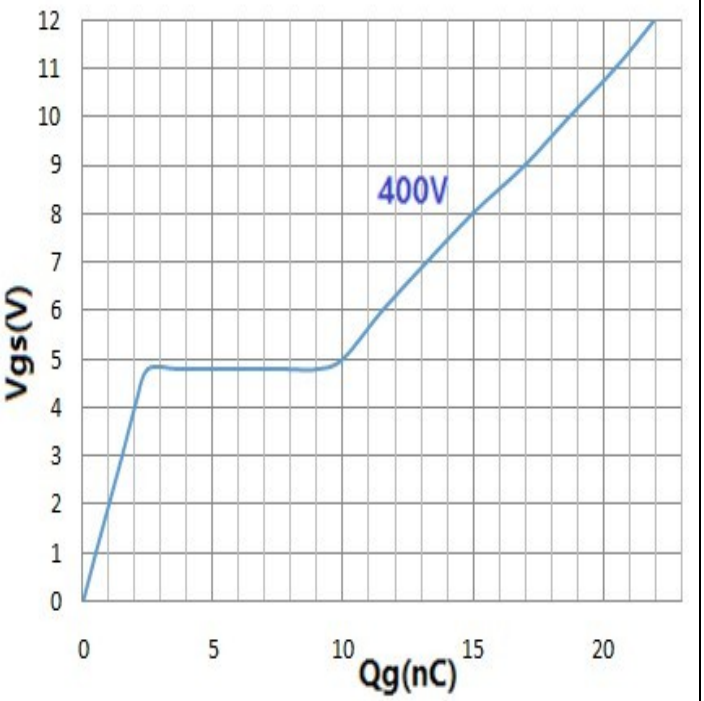
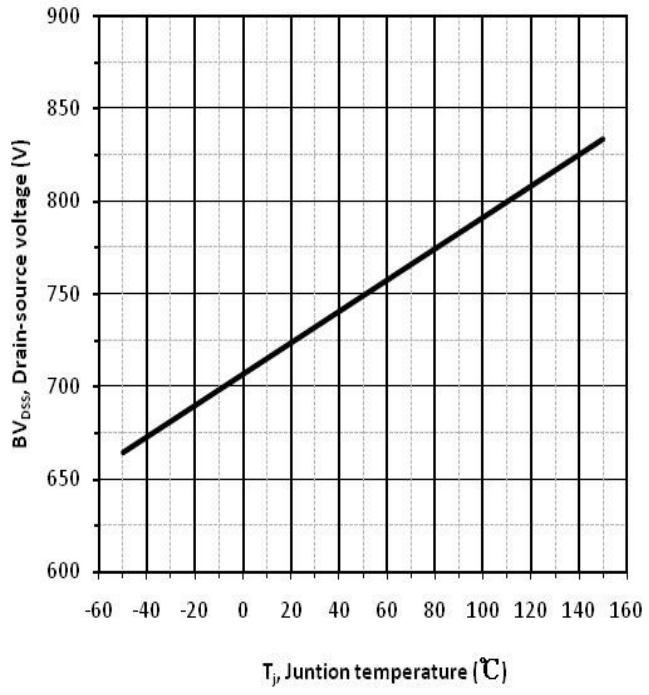
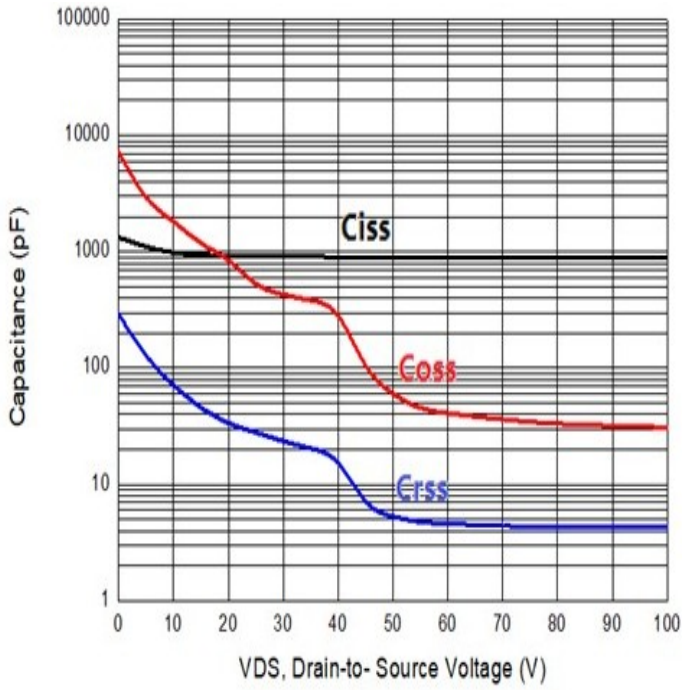
Diagram 3: Typ. Transfer characteristics	Diagram 4: Typ. Gate charge
	
I_D=f(V_{GS});parameter: T_j	V_{GS}=f(Q_{gate});I_D=4.8A pulsed; parameter: V_{DD}

Diagram 5: Drain-source breakdown voltage	Diagram 6: Typ. capacitances	
		
$V_{BR(DSS)}$=f(T_j);I_D=10mA	C=f(V_{DS});V_{GS}=0V; f=10 kHz	

5 Test Circuits

Table 8 Diode characteristics

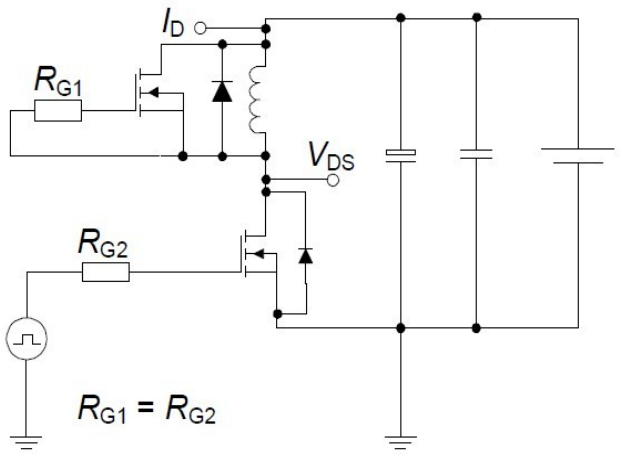
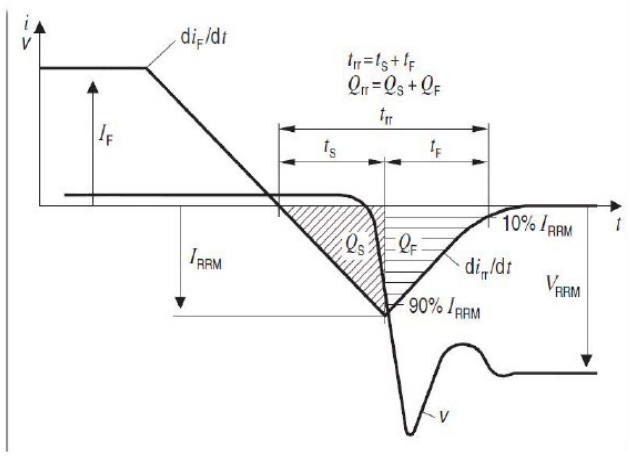
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

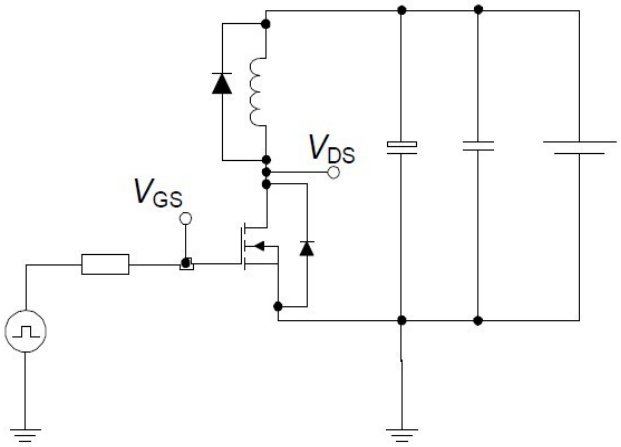
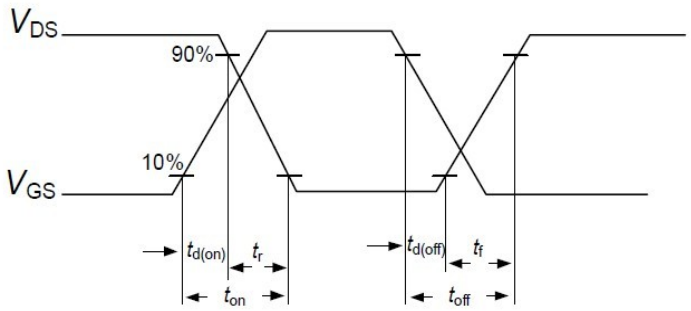
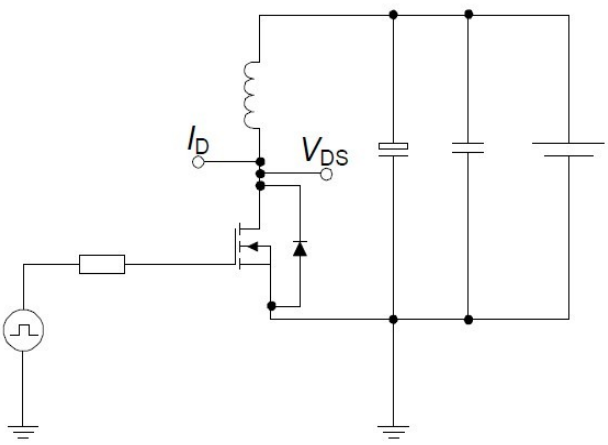
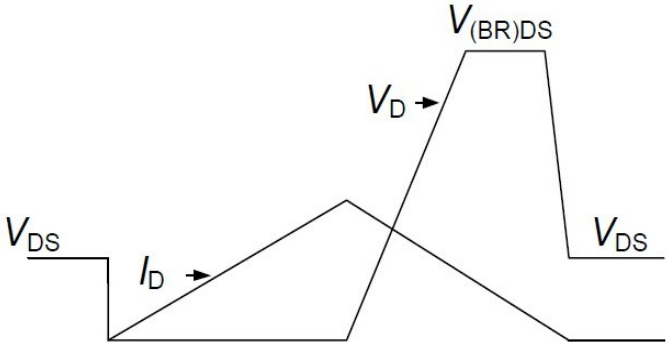
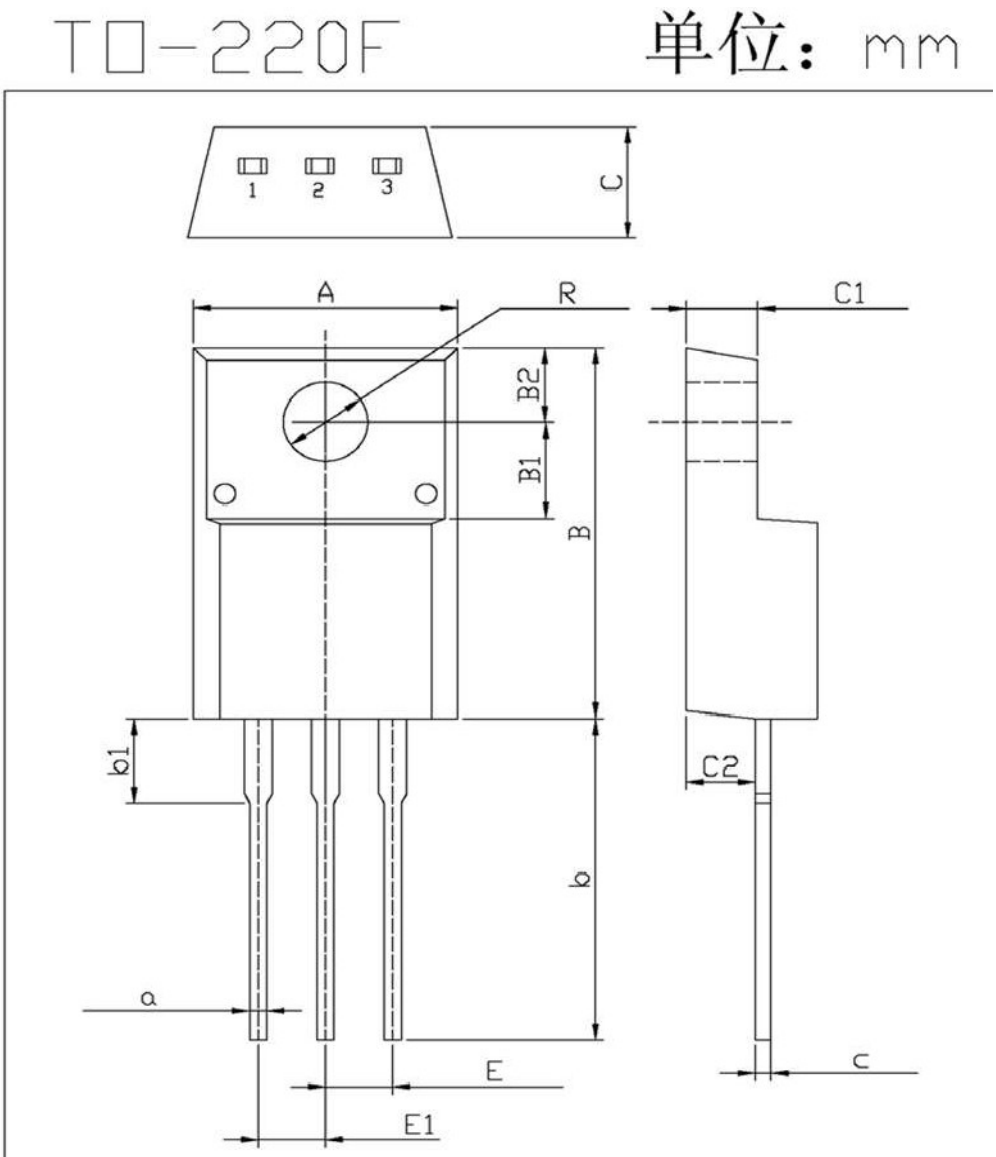
Switching times test circuit for inductive load	Switching times waveform
	

Table10 Unclamped inductive load

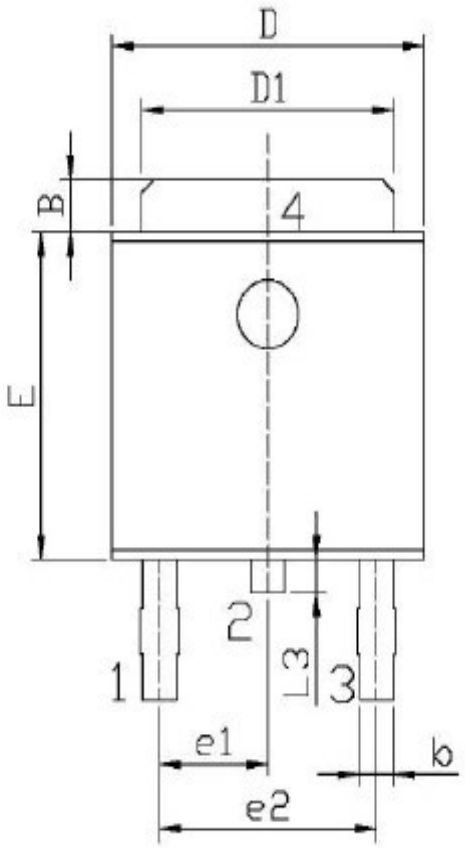
Unclamped inductive load test circuit	Unclamped inductive waveform
	

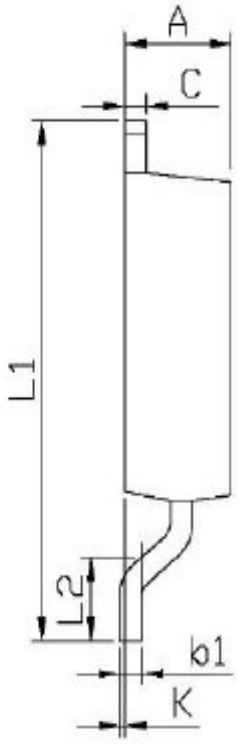
6 Package Outlines



Symbol	Dimensions In Millmeters		Symbol	Dimensions In Millmeters	
	Min	Max		Min	Max
C	4.3	4.8	b1	2.9	3.9
A	9.7	10.3	a	0.55	0.9
B	14.7	16.1	E	2.29	2.79
B1	3.8	4	E1	2.29	2.79
B2	2.9	3.55	C1	2.5	2.9
R	3	3.4	C2	2.15	2.7
b	12.5	13.6	c	0.4	0.7

Figure1：Outline PG-TO220F

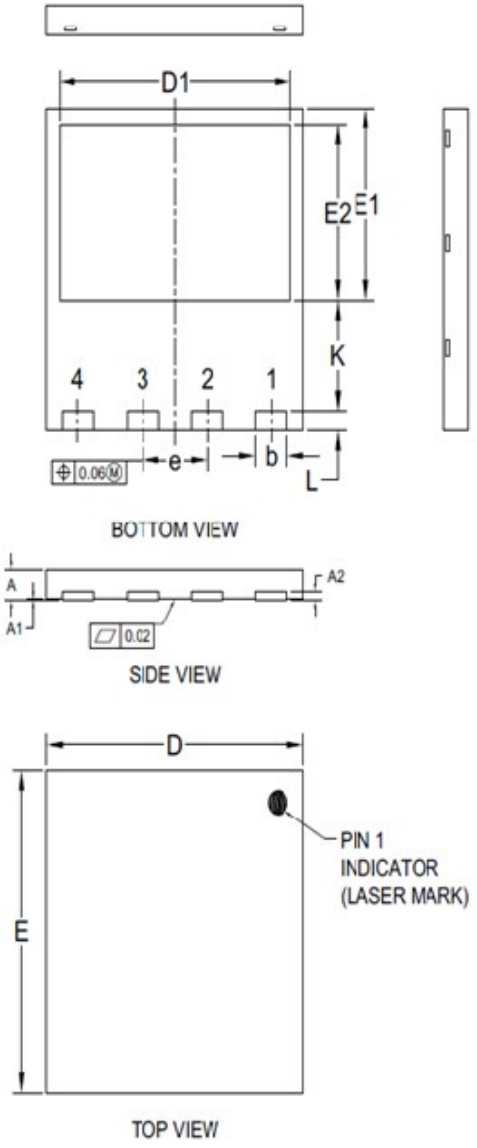




单位：mm

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	2.20	2.40	E	5.95	6.25
B	0.95	1.25	e1	2.24	2.34
b	0.50	0.70	e2	4.43	4.73
b1	0.45	0.55	L1	9.45	9.95
C	0.45	0.55	L2	1.25	1.75
D	6.45	6.75	L3	0.60	0.90
D1	5.10	5.50	K	0.00	0.10

Figure2：OutlinePG-TO252



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

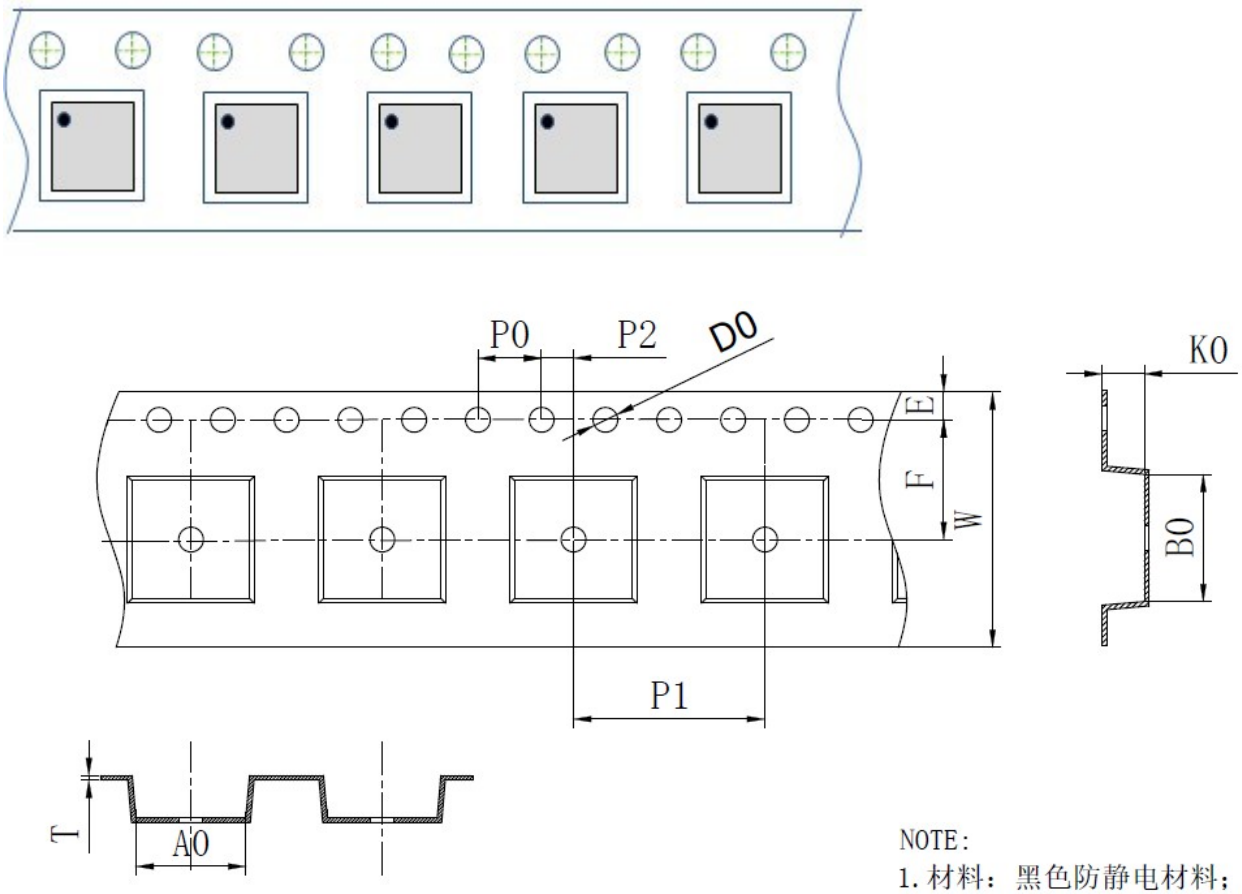
SYMBOL	MIN	TYP	MAX
A	0.70	0. 8	0. 9
A1	0.00	——	0.05
A2		0.20REF	
b	0.90	1.00	1.10
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.65	4.75	4.85
E2	4.25	4.35	4.45
e		2.00BSC	
L	0.40	0.50	0.60
K	2.65	——	——

NOTES:
1.CONTROLLING DIMENSIONS ARE IN MILLIMETERS(ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS THE TERMINALS.

Figure3：OutlinePG-DFN8x8

7. DFN8*8 Packing and Carry Tape Size:

3000pcs/reel



NOTE:
1. 材料：黑色防静电材料；
2. 10个链孔的累积公差不能超过 ±0.2

SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	8.40±0.10	8.50±0.10	1.30±0.10	4.00±0.10	12.0±0.10	2.00±0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.25±0.05	1.75±0.10	7.50±0.10	1.55±0.05	Min1.50	16.0±0.3

Unit: mm

Revision History

Revision	Date	Subjects (major changes since last revision)
0.1	2019-05-08	Preliminary version
1.0	2019-11-07	Fine tune outline and add Crss test data.etc
1.1	2019-03-13	Modify Marking Name
1.2	2020-03-30	Add Electrical characteristics Curve
1.3	2020-04-18	Add avalanche energy test condition, avalanche current data and test condition
1.4	2021-01-18	Add package for DFN8x8
1.5	2021-10-20	Keep VDSS
1.6	2021-12-08	Updated DFN8X8 PG outlines size and added carry tape size