MOSFET Silicon N-Channel MOS

1. Applications

Boost PFC switch,single-ended flyback ortwo-transistor forward,
Half bridge or Asymmetric half bridge or Series resonance half bridge topologies.
PC power, Adaptor,LCD & PDP TV,LED Lighting,Server power,
Telecom power and UPS application.

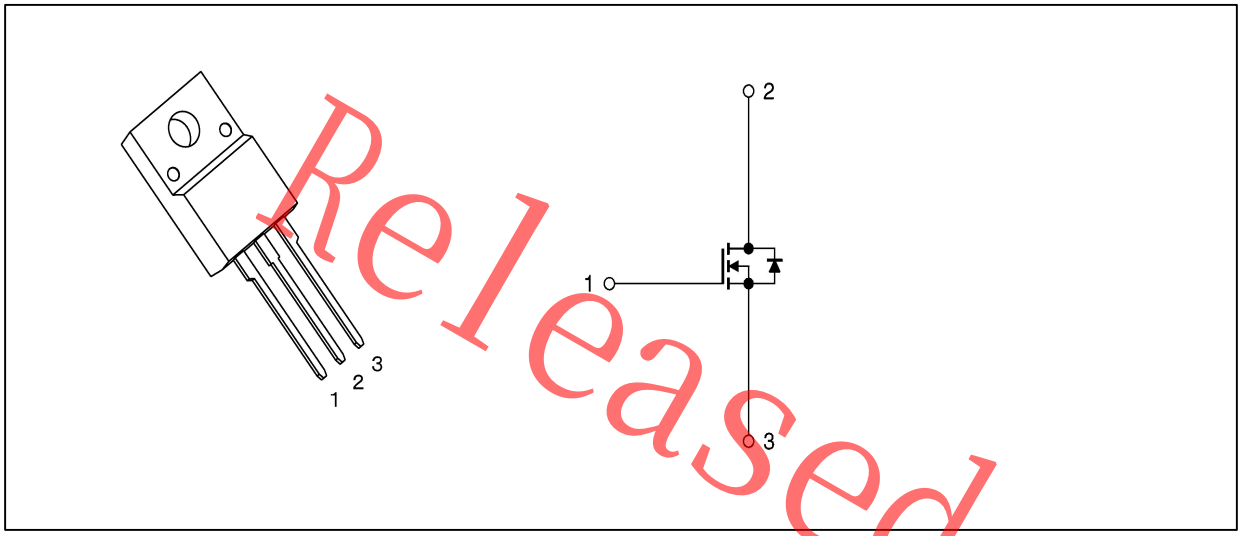
2. Features

Low drain-source on-resistance: RDS(ON) = 0.18Ω (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 2.8 to 4.2 V

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	210	mΩ
$Q_{g,typ}$	32.23	nC
$I_{D,pulse}$	60	A

3. Packaging and Internal Circuit



1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D		-	20	A	T_C=25°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	60	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	898	mJ	
MOSFET dv/dt ruggedness	dv/dt	-	-	135	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	33	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	
Operating junction temperature	T_j	-55	-	150	°C	
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS}=0...400V, I_{SD}<=48A, T_j=25°C see table 8

[1] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.8	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	605	-	-	V	V_{GS}=0V, I_D=10mA
Gate threshold voltage	$V_{(GS)th}$	2.8		4.2	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	100	nA	V_{DS}=600V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=30V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.18	0.21	Ω	V_{GS}=10V, I_D=7.5A, T_j=25°C
Gate resistance (Intrinsic)	R_G	-	5.6	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1547	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Output capacitance	C_{oss}	-	134	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Reverse transfer capacitance	C_{rss}	-	5.28	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Turn-on delay time	$t_{d(on)}$	-	12.4	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4Ω; see table 9
Rise time	t_r	-	21.6	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	52	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4Ω; see table 9
Fall time	t_f	-	18.8	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=8A, R_G=3.4Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8.242	-	nC	V_{DD}=400V, I_D=8A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	10.85	-	nC	V_{DD}=400V, I_D=8A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	32.23	-	nC	V_{DD}=400V, I_D=8A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	V_{DD}=400V, I_D=8A, V_{GS}=0 to 10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.72	-	V	V_{GS}=0V, I_F=1A, T_j=25°C
Reverse recovery time	t_{rr}	-	275	-	ns	V_R=400V, I_F=8 A, di_F/dt=100A/μs; see table 8
Reverse recovery charge	Q_{rr}	-	3.809	-	uC	V_R=400V, I_F=8 A, di_F/dt=100A/μs; see table 8
Peak reverse recovery current	I_{rrm}	-	25.6	-	A	V_R=400V, I_F=8 A, di_F/dt=100A/μs; see table 8

4 Test Circuits

Table 8 Diode characteristics

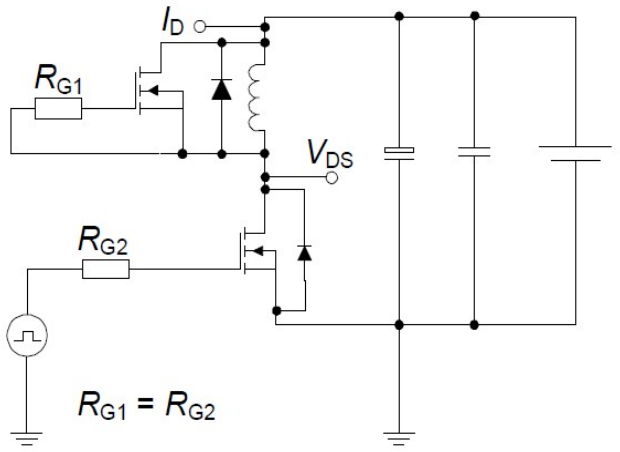
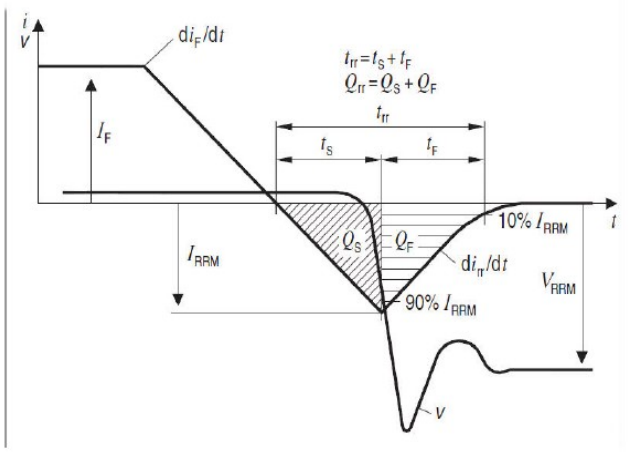
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

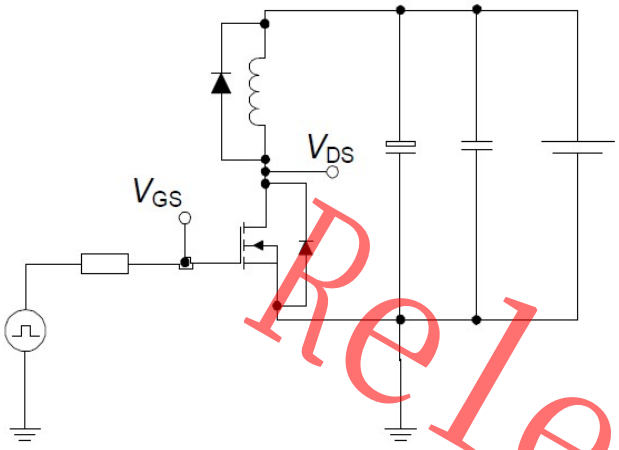
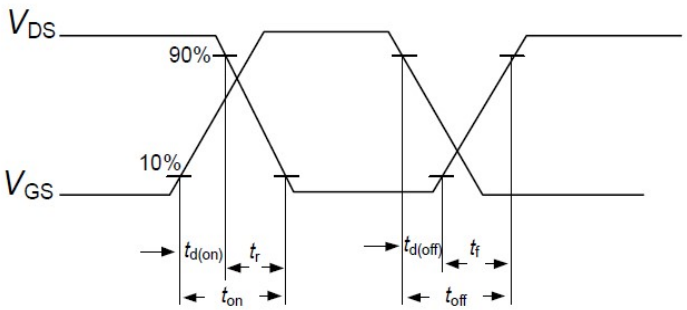
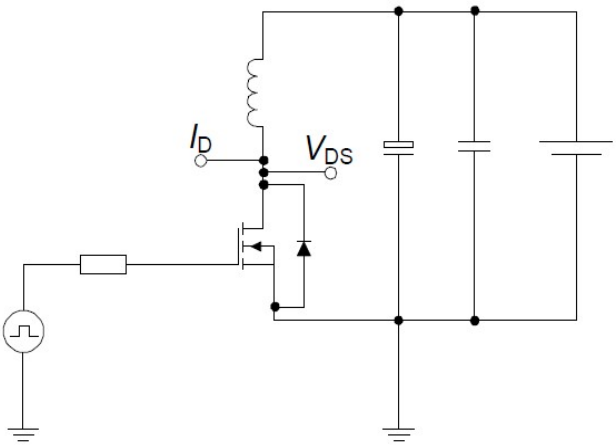
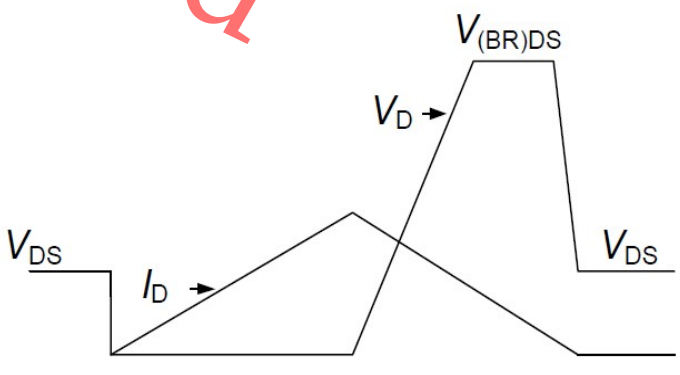
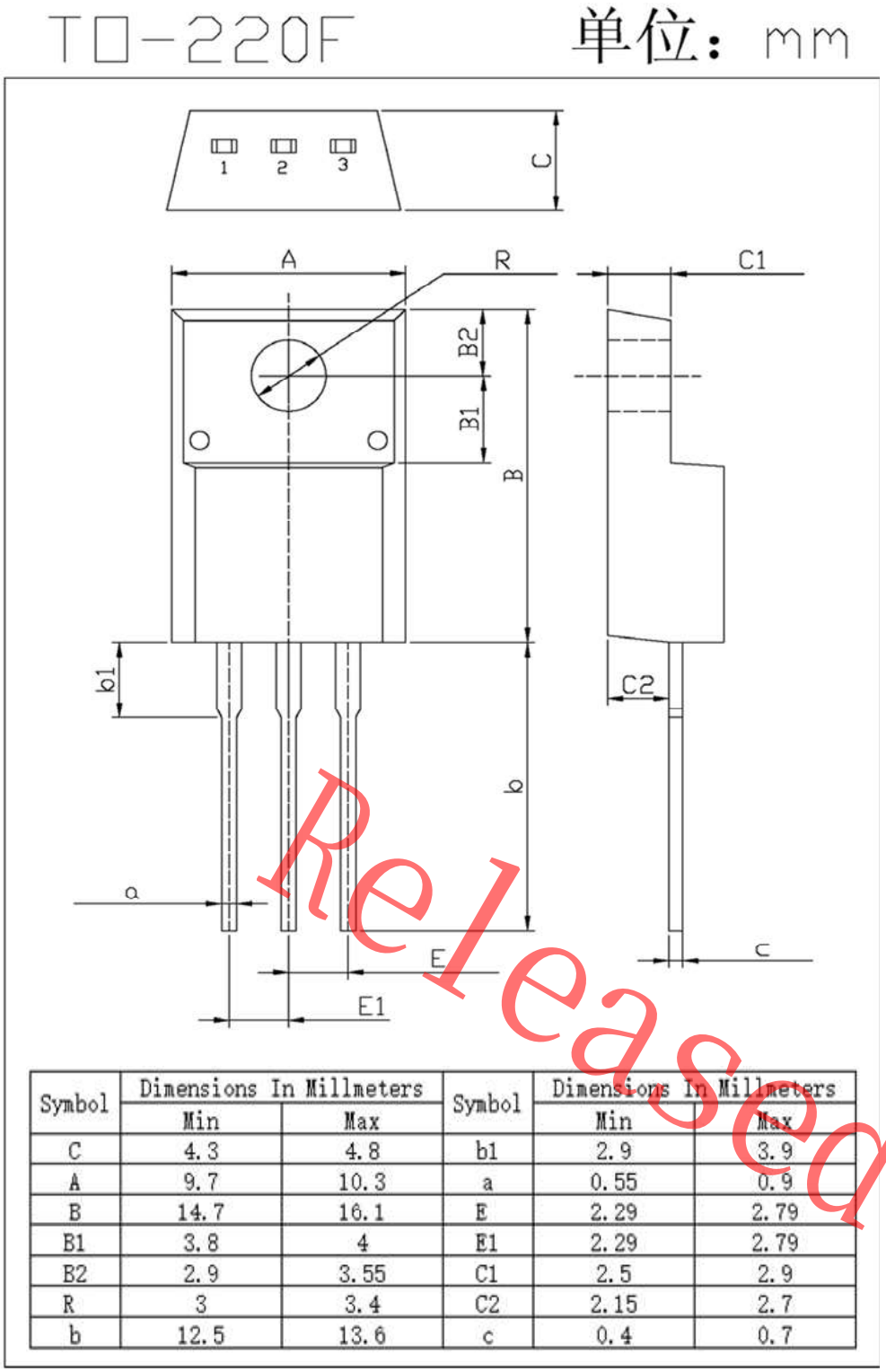
Switching times test circuit for inductive load	Switching times waveform
	

Table10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

5 Package Outlines



Symbol	Dimensions In Millmeters		Symbol	Dimensions In Millmeters	
	Min	Max		Min	Max
C	4.3	4.8	b1	2.9	3.9
A	9.7	10.3	a	0.55	0.9
B	14.7	16.1	E	2.29	2.79
B1	3.8	4	E1	2.29	2.79
B2	2.9	3.55	C1	2.5	2.9
R	3	3.4	C2	2.15	2.7
b	12.5	13.6	c	0.4	0.7

Figure1：Outline PG-TO220F

Revision History

ASA60R210E

Revision	Date	Subjects (major changes since last revision)
0.1	2019-05-08	Preliminary version
1.0	2019-11-07	Fine tune outline and add Crss test data.etc