

## MOSFET Silicon N-Channel MOS



### 1. Applications

Boost PFC switch, single-ended flyback or two-transistor forward, HB or AHB or LLC topologies.  
PC power, Adaptor, LCD & PDP TV, LED Lighting, Server power, Telecom power and UPS application.

### 2. Features

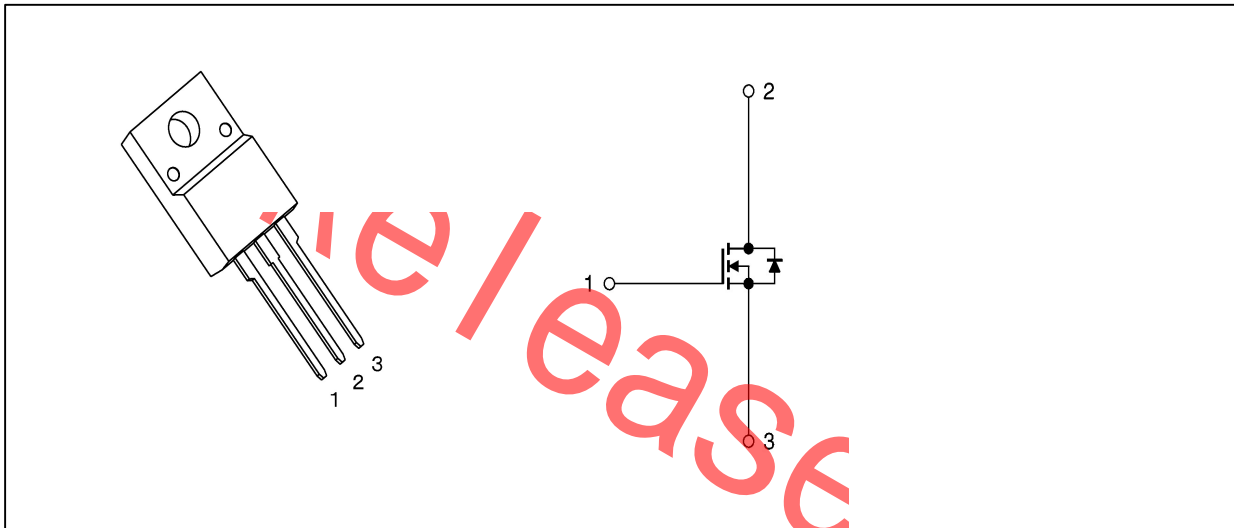
Low drain-source on-resistance:  $R_{DS(ON)} = 0.139\Omega$  (typ.)  
Easy to control Gate switching  
Enhancement mode:  $V_{th} = 2.8$  to  $4.2$  V



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	170	m $\Omega$
$Q_{g,typ}$	37.84	nC
$I_{D,pulse}$	75	A

### 3. Packaging and Internal Circuit



## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$		-	25	A	$T_C = 25^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	75	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	845	mJ	
MOSFET dv/dt ruggedness	dv/dt	-	-	135	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f > 1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	34	W	$T_C = 25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq 48\text{A}$ , $T_j = 25^\circ\text{C}$ see table 8

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.50$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_G$

Not for release

## 2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	3.67	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	80	°C/W	device on PCB, minimal footprint

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### 3 Electrical characteristics

at  $T_j=25^{\circ}\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	605	-	-	V	$V_{GS}=0\text{V}, I_D=10\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	2.8		4.2	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=25^{\circ}\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=30\text{V}, V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.139	0.17	$\Omega$	$V_{GS}=10\text{V}, I_D=12.5\text{A}, T_j=25^{\circ}\text{C}$
Gate resistance (Intrinsic)	$R_G$	-	5.5	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1760	-	pF	$V_{GS}=0\text{V}, V_{DS}=50\text{V}, f=10\text{kHz}$
Output capacitance	$C_{oss}$	-	176	-	pF	$V_{GS}=0\text{V}, V_{DS}=50\text{V}, f=10\text{kHz}$
Reverse transfer capacitance	$C_{rss}$	-	3.79	-	pF	$V_{GS}=0\text{V}, V_{DS}=50\text{V}, f=10\text{kHz}$
Turn-on delay time	$t_{d(on)}$	-	11.4	-	ns	$V_{DD}=400\text{V}, V_{GS}=13\text{V}, I_D=11.3\text{A}, R_G=1.7\Omega$ ; see table 9
Rise time	$t_r$	-	21.8	-	ns	$V_{DD}=400\text{V}, V_{GS}=13\text{V}, I_D=11.3\text{A}, R_G=1.7\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	43	-	ns	$V_{DD}=400\text{V}, V_{GS}=13\text{V}, I_D=11.3\text{A}, R_G=1.7\Omega$ ; see table 9
Fall time	$t_f$	-	18.8	-	ns	$V_{DD}=400\text{V}, V_{GS}=13\text{V}, I_D=8\text{A}, R_G=3.4\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	8.039	-	nC	$V_{DD}=400\text{V}, I_D=11.3\text{A}, V_{GS}=10\text{V}$
Gate to drain charge	$Q_{gd}$	-	29.28	-	nC	$V_{DD}=400\text{V}, I_D=11.3\text{A}, V_{GS}=10\text{V}$
Gate charge total	$Q_g$	-	37.84	-	nC	$V_{DD}=400\text{V}, I_D=11.3\text{A}, V_{GS}=10\text{V}$
Gate plateau voltage	$V_{plateau}$	-	7.5	-	V	$V_{DD}=400\text{V}, I_D=11.3\text{A}, V_{GS}=10\text{V}$

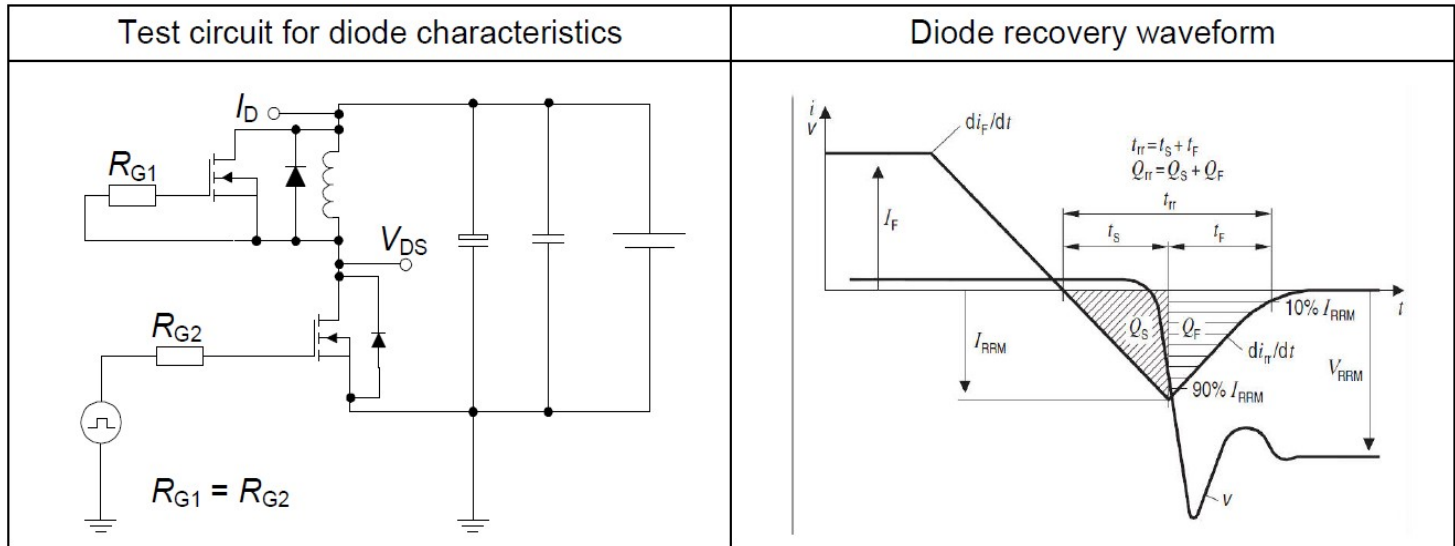
Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.71	-	V	$V_{GS}=0V, I_F=1A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	320	-	ns	$V_R=400V, I_F=11.3A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	4.770	-	uC	$V_R=400V, I_F=11.3A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	29.1	-	A	$V_R=400V, I_F=11.3A, di_F/dt=100A/\mu s$ ; see table 8

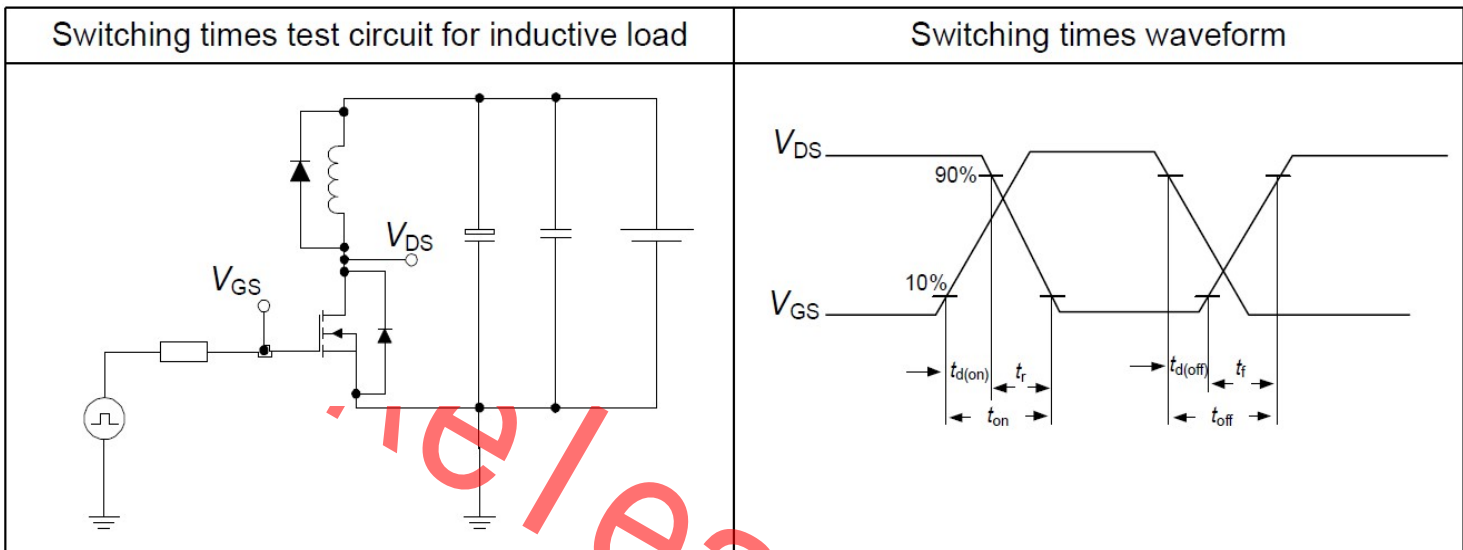
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## 4 Test Circuits

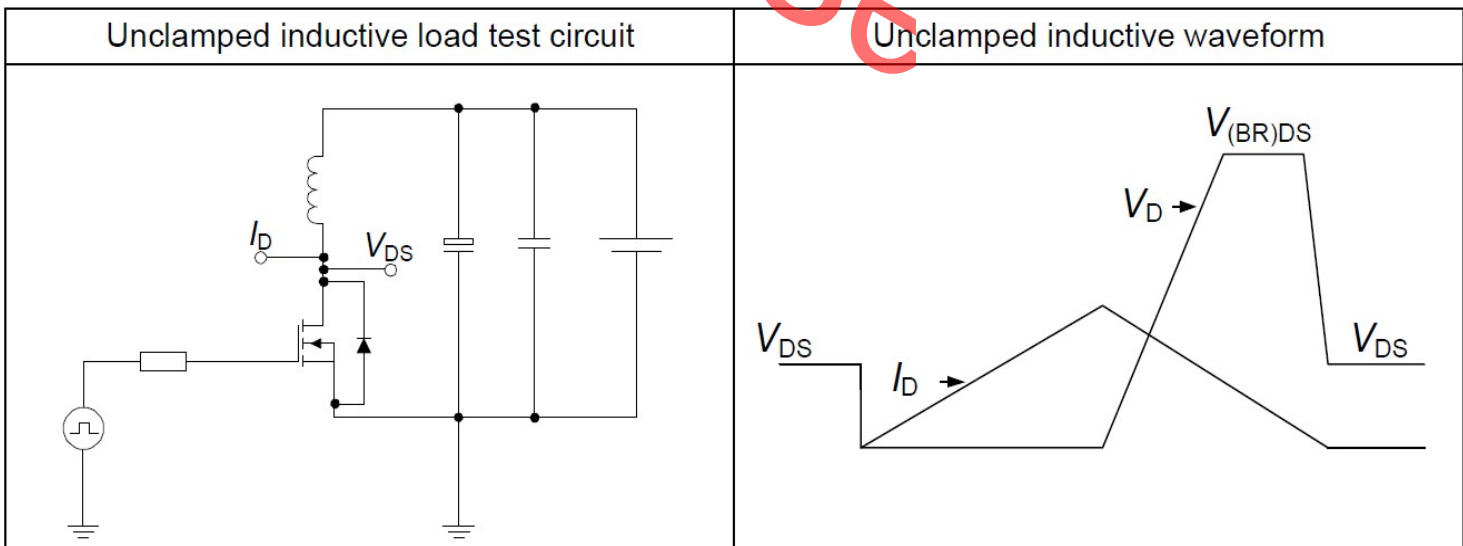
**Table 8 Diode characteristics**



**Table 9 Switching times**



**Table 10 Unclamped inductive load**



5 Package Outlines

TO-220F

单位: mm

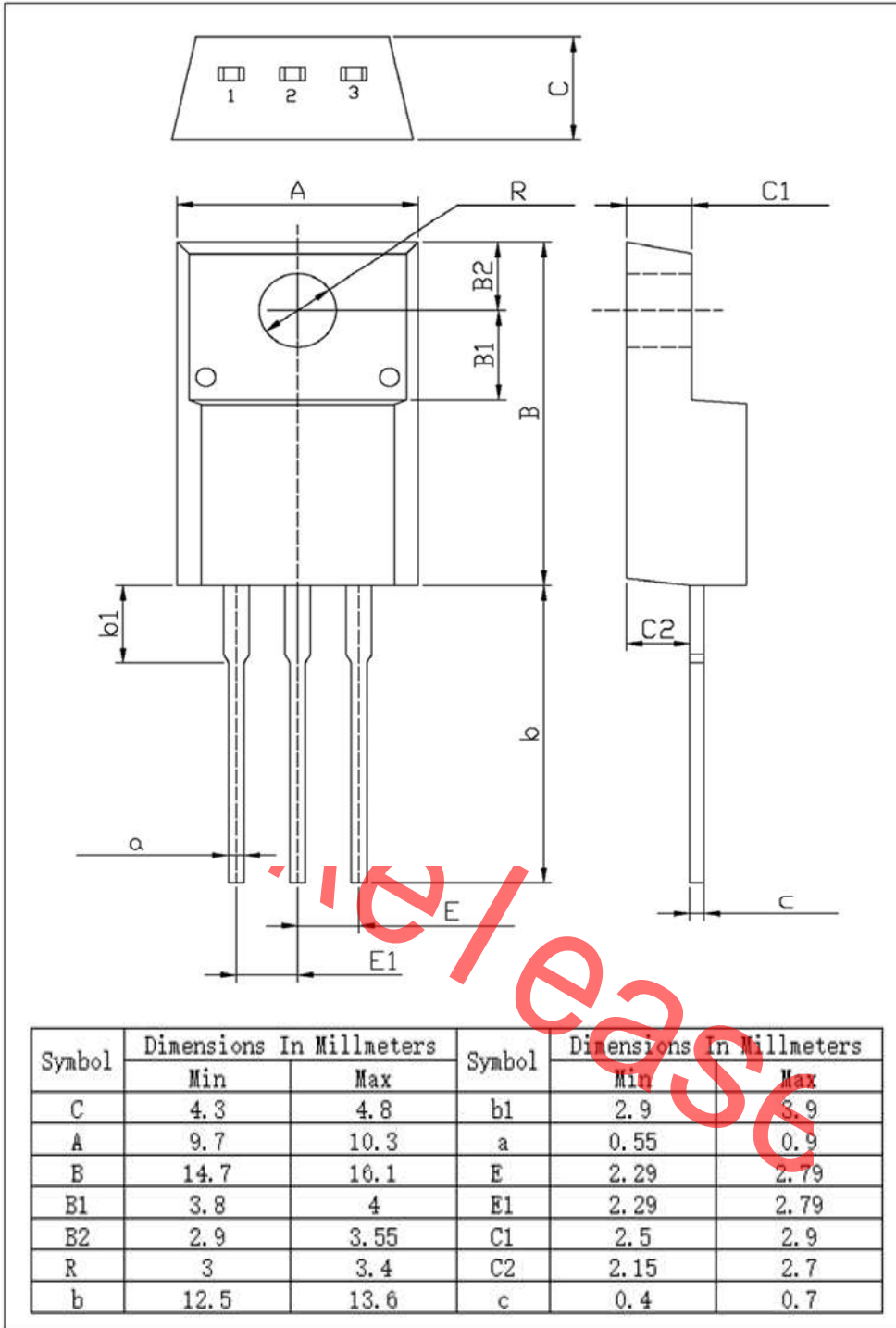


Figure3: Outline PG-TO220F

## Revision History

### ASA60R170E

Revision	Date	Subjects (major changes since last revision)
1.0	2020-03-18	Preliminary version

Pre-release