

High-Performance AI Vision Processor

Overview

V853 is a new generation of high-performance and low-power processor SoC targeted for the field of intelligent vision. It can be widely used in intellectually upgraded industries such as intelligent door lock, intelligent attendance and access control, webcam, tachograph, and intelligent desk lamp.

V853 integrates the single Cortex-A7 core and RISC-V MCU. It is also designed with a new generation of high-performance ISP image processor and Allwinner Smart video engine with maximum 5M@25fps H.265/H.264 encoding and 5M@25fps H.264 decoding to achieve professional picture effect. It has built-in NPU with maximum 1T computing power and supports INT8/INT16 hybrid operation and typical network models such as TensorFlow/MXNet/PyTorch/Caffe. V853 has advanced 22nm technics to support product miniaturization design. It also supports various special video input and output interfaces such as 1*4-lane MIPI-CSI/DVP/MIPI-DSI/RGB to meet the needs of all AI visual products. V853 supports 16-bit DDR3/LDDR3L to meet the requirements of various products on high bandwidth. In addition, Allwinner provides the stable and easy-to-use matching reference design for Linux SDK and software and hardware to assist clients in the rapid mass production of products.

Highlight

- High Performance: V853 integrates ARM Cortex-A7@1GHz, RISC-V@600MHz, 1Tops NPU and 16-bit DDR3/DDR3L at maximum frequency of 933MHz to meet the variable requirements of computing power and bandwidth.
- Video Multimedia: Supports 5M@25fps H.264/H.265 video online real-time encoder and Allwinner new-generation display engine ISP600 and reach the mainstream level in 2/3DNR, HDR, edge enhancement and so on.
- Video Input: Parallel CSI and 4-lane MIPI CSI support maximum 4-ch AHD camera or 3-ch RAW data camera interleaved-input.
- Rich Peripheral Interfaces: 5xTWI, 4xUART, 4xSPI, 4xGPADC, USB2.0 DRD, WIEGAND and other interfaces greatly facilitate product expansion.

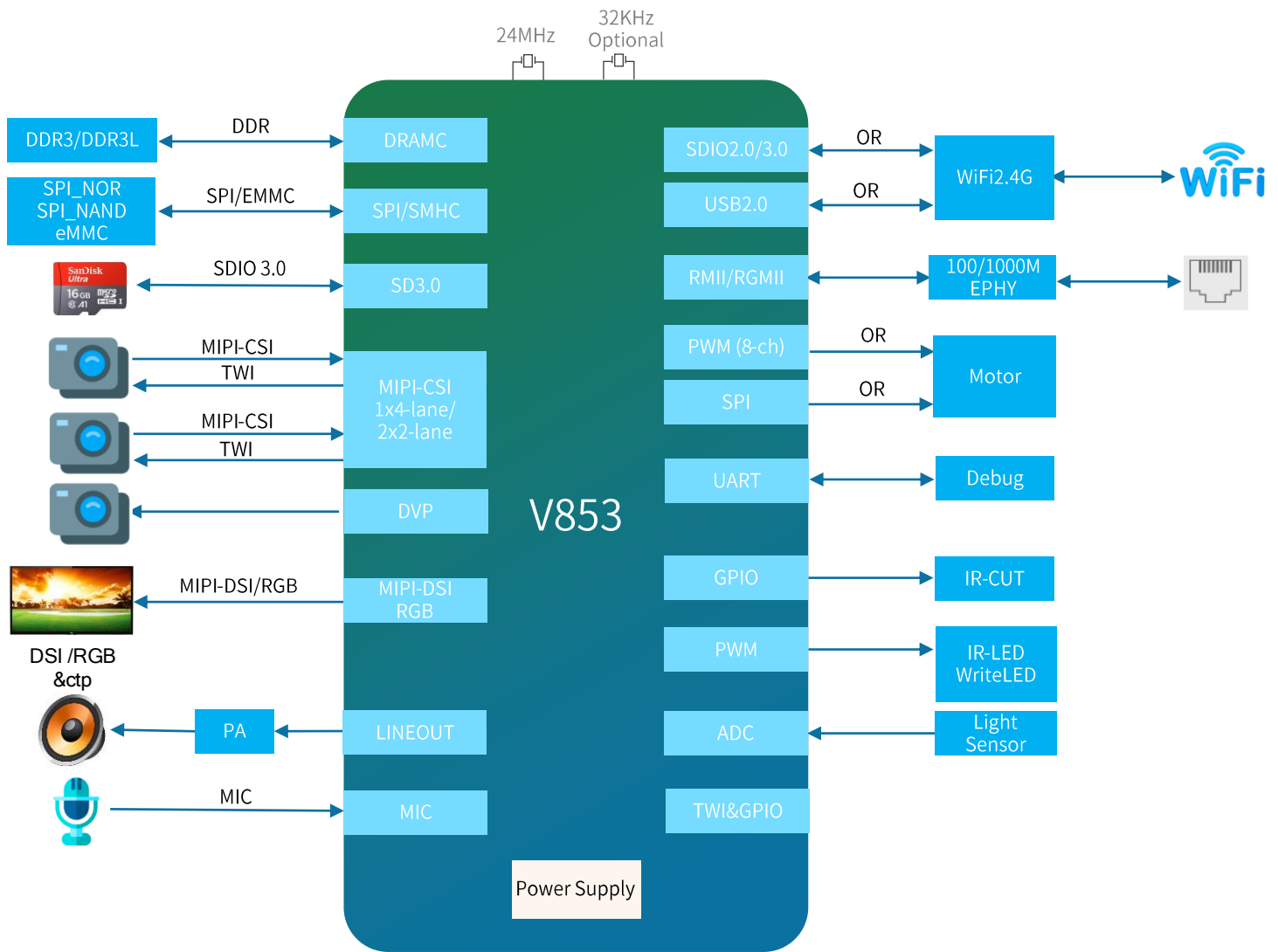
Features

CPU	<ul style="list-style-type: none"> Cortex-A7@1 GHz CPU core, supporting 32 KB I-cache, 32 KB D-cache, and 128 KB L2 cache RISC-V@600 MHz core, supporting 16 KB I-cache and 16 KB D-cache
NPU	<ul style="list-style-type: none"> Maximum performance up to 1 Tops Embedded 128KB internal buffer Supports deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, and so on
Memory	<ul style="list-style-type: none"> 16-bit DDR3/DDR3L interface, supporting maximum capacity of 1GB SD3.0/eMMC 5.1 interface SPI Nor/SPI Nand Flash
Video Engine	<p>Video encoder</p> <ul style="list-style-type: none"> H.264/H.265 up to 4K@15fps or 5M@25fps JPEG up to 1080p@60fps <p>Video decoder</p> <ul style="list-style-type: none"> Supports H.264 BP/MP/HP, JPEG Real-time multiple streams H.264 encoding capability: 5M@25fps JPEG snapshot performance of 1080p@60fps independently
Display Engine	<ul style="list-style-type: none"> Allwinner SmartColor post processing for an excellent display experience Supports 2 video channels and 1 UI channel Supports G2D hardware accelerator including rotate, mixer, scaler functions
Video Input	<p>ISP</p> <ul style="list-style-type: none"> Maximum performance of 5M@30fps and maximum resolution of 3072 x 1772 Adjustable 3A functions (AE, AWB, and AF), and 3A parameters are adjustable Provides ISP tuning tools for the PC <p>VIPP</p> <ul style="list-style-type: none"> Four VIPP YUV422 or YUV420 outputs Maximum performance of 5M@30fps and maximum resolution of 3072 x 1772 <p>8-/10-/12-/16-bit parallel CSI interface</p> <ul style="list-style-type: none"> Supports digital camera (DC), BT.601, BT.656, BT.1120 protocol Maximum video capture resolution up to 5M@30fps <p>1*4-lane MIPI CSI interface</p> <ul style="list-style-type: none"> Supports DOL WDR mode and splitting into 2*2-lane MIPI CSI Supports 4-ch VC de-interleaver function Maximum video capture resolution up to 5M@30fps
Video OUT	<ul style="list-style-type: none"> RGB LCD output interface up to 1920 x 1080@60fps 1*4-lane MIPI DSI interface up to 1920 x 1200@60fps
Audio	<ul style="list-style-type: none"> 1 DAC and 2 ADCs Analog audio interfaces: MICIN1P/N, MICIN2P/N, LINEOUTP/N Digital audio interfaces: I2S/PCM x 2, DMIC
Security System	<ul style="list-style-type: none"> AES, DES, 3DES encryption and decryption algorithms RSA/ECC signature verification algorithm MD5/SHA and HMAC tamper proofing PRNG/TRNG hardware random number generator Integrated 2 Kbits OTP storage space
Connectivity	<ul style="list-style-type: none"> USB2.0 DRD, SDIO 3.0, SPI x 4, UART x 4, TWI x 5, WIEGAND PWM (12-ch), GPADC (4-ch) 10/100/1000M EMAC with RMI2 and RGMII interfaces
Package	<ul style="list-style-type: none"> LFBGA318, 12 mm x 12 mm body size, 0.5 mm ball pitch

Block Diagram



Application Diagram



ABOUT ALLWINNER

Allwinner Technology, founded in 2007, is an outstanding designer dedicated to intelligent application SoC, high performance analog component and wireless connectivity IC. It is headquartered in Zhuhai China, with other R&D centers and offices in Shenzhen, HongKong, Xi'an, Beijing and Shanghai. Listed on the GEM of the Shenzhen Stock Exchange in 2015, with the stock code 300458.

Motivated by customer-oriented strategy, Allwinner aligns remarkable R&D teams with long-term core-technology investment in UHD video processing, high-performance multi-core CPU/GPU integration with AI and advanced manufacturing process in terms of high integration, ultra-low power consumption and full-stack integration platform, providing competitive turnkey solutions with considerate services. The products powered by Allwinner spread across from smart hardware, smart home, consumer electronics, HD media, smart video, connected car, industry control, wireless communication to analog products.

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