General Description

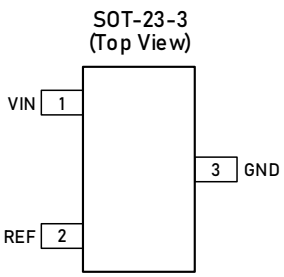
The LTR33 series devices are low temperature drift (20 ppm/℃ maximum), low-power, high-precision CMOS voltage reference, featuring ±0.1% initial accuracy, low operating current with power consumption less than 500 µA. This device also offers very low output noise of 15 $\mu V_{PP}/V$, which enables its ability to maintain high signal integrity with high-resolution data converters in noise critical systems.

Packaged in the same SOT-23-3 package, LTR33xx offers enhanced specifications and pin-to-pin replacement for REF33xx and LM4132. Stability and system reliability are further improved by the low output-voltage hysteresis of the device and low long-term output voltage drift. LTR33xx is specified for the wide temperature range of −40 to +125°C

Features and Benefits

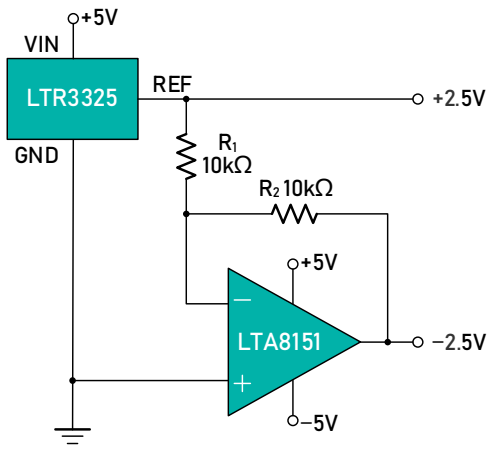
- Voltage options: 1.25 V, 2.048 V, 2.5 V, 3.0 V, 3.3 V, 4.096 V
- Initial accuracy: ±0.1% (maximum)
- Low temperature coefficient: 20 ppm/°C (maximum)
- Output 1/f noise at 0.1 to 10 Hz: 15 $\mu V_{PP}/V$
- Supply voltage: 2.7 to 5.5 V
- Power consumption: < 500 µA
- Start-up time: < 400 µs
- Operating temperature: −40 to 125°C
- Output Current: ±5 mA

Pin Configuration



Applications

- Data acquisition (DAQ)
- PLC analog I/O modules
- Field transmitters
- Motor drive control module
- Battery test equipment
- LCR meters



Pin Description

Pin. Name	Pin Description
VIN	Power supply voltage
GND	Ground.
REF	Reference voltage outputs , an external capacitor is required.

Ordering Information (1)

Type Number	Output Voltage	Quantity	Operating Temperature	Package Name	Marking Code
LTR3312T20YT3	1.25 V	3000	−40 to 125°C	SOT-23-3	3AXXX
LTR3320T20YT3	2.048 V	3000	−40 to 125°C	SOT-23-3	3BXXX
LTR3325T20YT3	2.5 V	3000	−40 to 125°C	SOT-23-3	3CXXX
LTR3330T20YT3	3.0 V	3000	−40 to 125°C	SOT-23-3	3DXXX
LTR3333T20YT3	3.3 V	3000	−40 to 125°C	SOT-23-3	3EXXX
LTR3340T20YT3	4.096 V	3000	−40 to 125°C	SOT-23-3	3FXXX

(1) Please contact to your Linearin representative for the latest availability information and product details.

Limiting Value – In accordance with the Absolute Maximum Rating System (IEC 60134).

Operating Ambient Temperature Range	−40 to 125°C
Storage Temperature Range	−50 to 125°C
Input Voltage Range	−0.3 V to 5.5 V
ESD protection	> 3000 V

Note: Stresses exceeding those listed in the Maximum Rating table may damage the device. Operation beyond the maximum Rating conditions or under harsh conditions may affect product reliability and function.

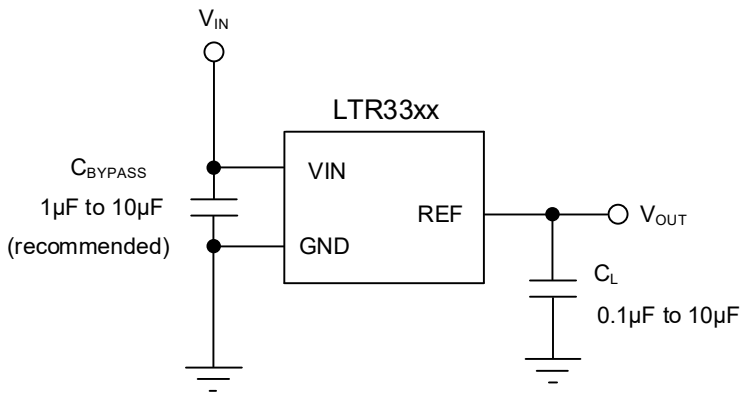
Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply input voltage	V_{IN}	V_{OUT}+0.2		5.5	V
Output current range	I_{CC}	-5		5	mA

Electrical Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Power supply voltage	V_{IN}		2.7	5	5.5	V
Power consumption	I_{CC}	V_{CC} = 5.0 V, no load.		300	500	µA
Output voltage	V_{OUT}	LTR3312		1.25		V
		LTR3320		2.048		V
		LTR3325		2.5		V
		LTR3330		3.0		V
		LTR3333		3.3		V
		LTR3340		4.096		V
Output voltage accuracy	ΔV_{OUT}		−0.1		0.1	%
Output Noise	Vnoise	0.1 to 10 Hz		15		µVpp/V
Temperature coefficient	T_C	-40 to 125°C			20	ppm/°C
Dropout Voltage	V_{IN}–V_{OUT}			200		mV
Line Regulation	ΔV_{OUT} /ΔV_{IN}				100	ppm/V
Load Regulation	ΔV_{OUT}/ ΔI_L				50	ppm/mA
Thermal hysteresis	dT			80		ppm
Long-term stability		0h to 1000h at 25°C		200		ppm
Short-circuit current	I_{SC}	Souring and sinking		50		mA
Capacitive load			0.1		10	µF
Turn-on setting time					400	µs

Typical Application



Layout

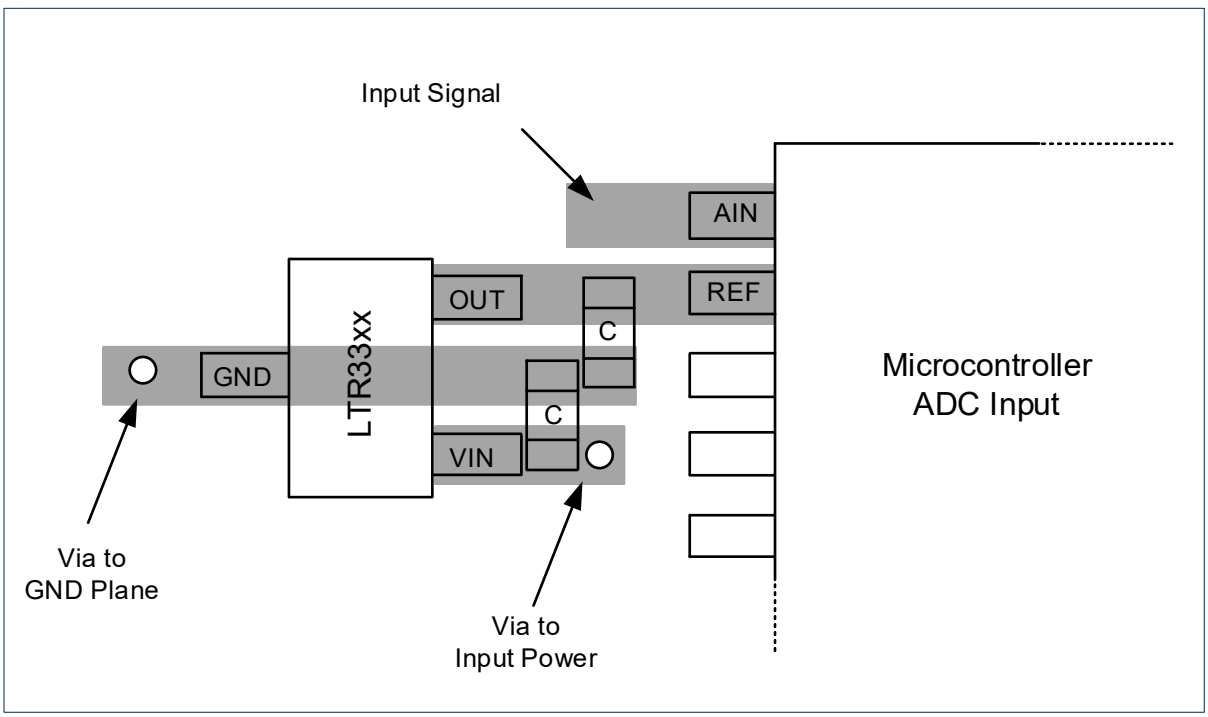
Layout Guidelines

For optimal performance of this design，please follow standard printed circuit board (PCB) layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours.
As shown below an example of a PCB layout for a data acquisition system using the LTR33xx.

Some key considerations are:

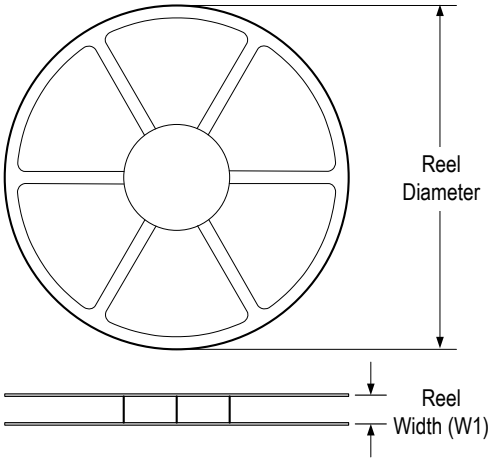
- Connect a low-ESR, 1 µF ceramic capacitor at the IN pin for bypass, and a 0.1 uF to 10 uF ceramic capacitor at the OUT pin for stability of the LTR33xx.
- Decouple other active devices in the system per the device specifications.
- Use a solid ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the ADC to reduce noise pickup·
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

Layout Example

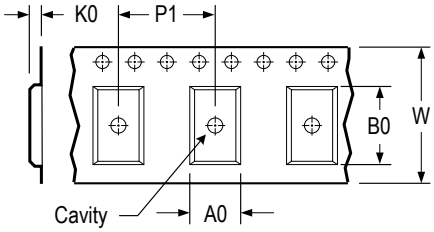


Tape and Reel Information

REEL DIMENSIONS

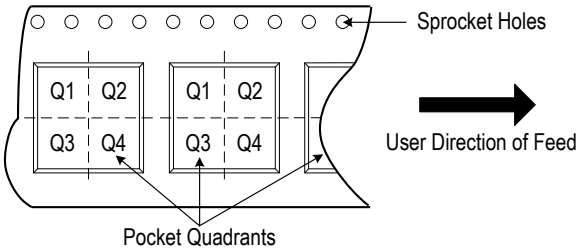


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIETATION IN TAPE

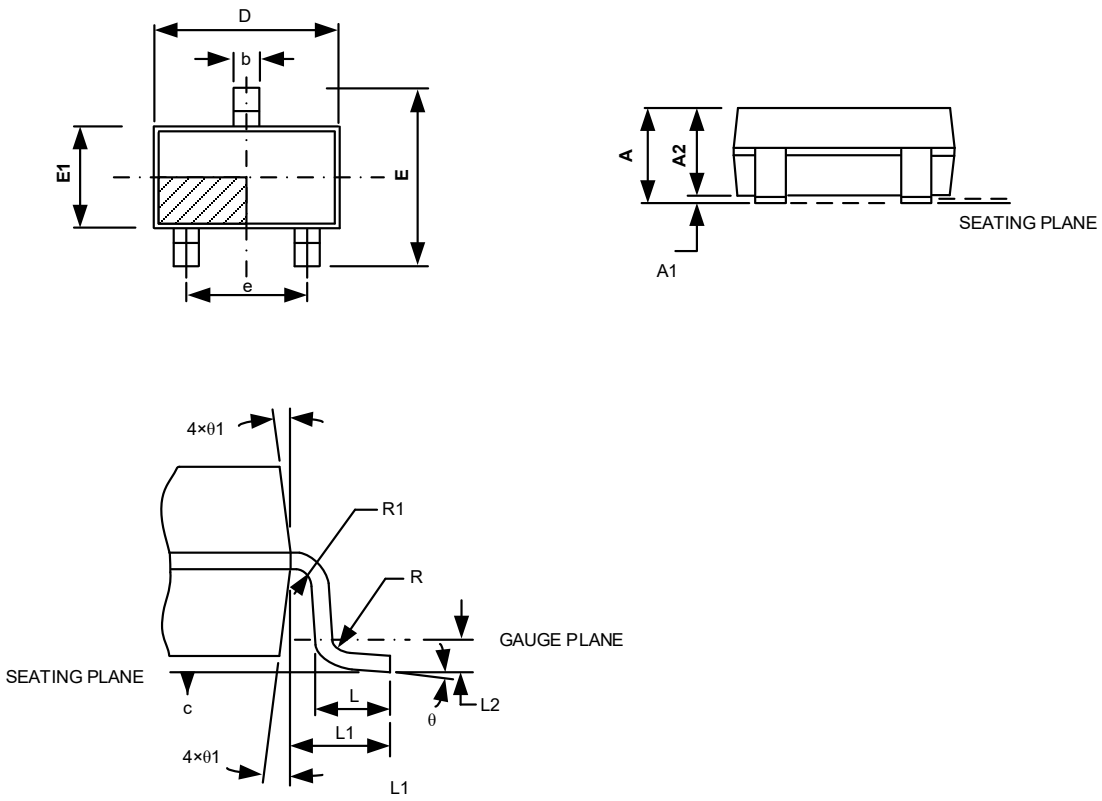


* All dimensions are nominal

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTR3312T20YT3	SOT23	3	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3

Package Outlines

DIMENSIONS, SOT-23-3



Symbol	Min.	Typ.	Max.
A	–	–	1.35
A1	0	–	0.15
A2	1.0	1.1	1.2
b	0.35	–	0.45
b1	0.32	–	0.38
C	0.14	–	0.20
C1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	1.8	1.9	2.0
L	0.35	0.45	0.6
L1	0.6REF		
L2	0.25REF		
R	0.1	–	–
R1	0.1	–	0.25
θ	0°	4°	8°
θ1	5°	10°	15°

(Unit: mm)