# T3 Datasheet

*Smart Automotive Processor*

**Revision 1.9**

**Nov.23, 2022**

# Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | Apr.19,2016 | Initial Release Version. |
| 1.1 | Jun.02,2016 | Update pin characteristics. |
| 1.2 | Jul.20,2016 | Update ambient operating temperature range. |
| 1.3 | Sep.11,2018 | 1. Add carrier, storage and baking information in chapter 8.<br>2. Add reflow profile in chapter 9.<br>3. Add part marking in chapter 10. |
| 1.4 | Nov.26,2018 | 1. Change RTC-VIO to GND in chapter 4 and chapter 7.<br>2. Update reflow profile parameters in chapter 9. |
| 1.5 | May.27,2019 | 1. Add GPIO multiplex function table in section 4.2.<br>2. Add SDRAM I/O DC electrical characteristics in section 5.4.<br>3. Add SDIO electrical parameters in section 5.5.<br>4. Update 24MHz and 32.768kHz crystal requirement tables in section 5.9.<br>5. Add SDRAM AC electrical characteristics in section 5.11.1.<br>6. Add RMII related descriptions in section 2.9, section 4.2, section 4.3. |
| 1.6 | Oct.25,2019 | **Chapter 4 Pin Description**<br>Update pin characteristics in section 4.1. |
| 1.7 | Oct.21,2020 | **Chapter 4 Pin Description**<br>Update GMAC pin names in section 4.2. |
| 1.8 | Jun.02,2021 | 1. Refresh the specification.<br>2. Modify RGMII, RMII and MII timing in section 5.12.3 |
| 1.9 | Nov.23, 2022 | **Chapter 5 Electrical Characteristics**<br>Updated TWI AC Electrical Characteristics |

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# About This Documentation

**Purpose**

The documentation describes features of each module, pin/signal characteristics, current consumption, PLL electrical characteristics, the interface timing, thermal and package of T3 processor. The documentation is intended to provide guidance to the hardware designers for electronics or sales personnel for electronic components. This documentation assumes that the reader has a background in electronic components. For details about register descriptions of each module, see the ***T3 User Manual***.

**Conventions**

The symbols that may be found in this document are defined as follows.

| Symbol | Description |
|---|---|
| **WARNING** | A warning means that injury or death is possible if the instructions are not obeyed. |
| **CAUTION** | A caution means that damage to equipment is possible. |
| **NOTE** | Provides additional information to emphasize or supplement important points of the main text. |

# 1. Overview

The T3 processor represents Allwinner's latest achievement in smart automotive processors. The processor is ideal for applications that require 3D graphics, advanced video processing, rich user interfaces, lower power consumption and higher system integration. It will bring the advanced consumer electronics experiences into the vehicles of the future, and achieve a good balance of high performance, drive safety, greener mobility, drive video record and device connectivity.

The T3 processor has some very exciting features:

- **CPU**: T3 is based on quad-core Cortex™-A7 CPU architecture, the most power efficient CPU core ARM's ever developed.
- **GPU**: T3 adopts the extensively implemented and technically mature Mali400 MP2 to provide mobile users with superior experience in web browsing, video playback and games.
- **Video Encoding**: High-definition (HD) H.264 video encoder is up to 1080p@45fps.
- **Camera**: Supports dual CMOS sensor parallel interfaces and 4-channel TVIN, which can easily finish multi-channel video recording.
- **Display**: Content can be displayed on 4-lane MIPI DSI displays, or RGB panel, or LVDS panel.
- **Audio**: Integrated audio codec with 24bit/192kHz DAC playback, and supports I2S/PCM interface for connecting to an external audio codec.I2S/PCM interface includes eight channels of TDM with sampling precision up to 32bit/192kHz.
- **Memory**: Supports external memory interfaces to NAND Flash, SD/eMMC, Nor Flash and SDRAM port. SDRAM port can be configured to support LPDDR2, LPDDR3, DDR2, DDR3, DDR3L.
- **Peripherals**: To reduce total system cost, T3 has a broad range of hardware peripherals to meet the flexible peripheral configuration requirements such as UART, RTP, SPI, CIR, USB2.0 OTG, TWI, and so on.

# 2. Features

## 2.1. CPU Architecture

- Quad-core ARM Cortex™-A7 Processor
- ARMv7 ISA standard ARM instruction set
- Thumb-2 Technology
- Jazeller RCT
- NEON Advanced SIMD
- VFPv4 floating point
- Large Physical Address Extensions(LPAE)
- 32KB L1 Instruction cache and 32KB L1 Data cache for per CPU
- 512KB L2 cache shared

## 2.2. GPU Architecture

- Mali400 MP2
- Supports OpenGL ES 2.0, OpenGL ES 1.1, Open VG 1.1 standard

## 2.3. Memory Subsystem

### Boot ROM

- On-chip 36KB ROM boot loader
- Supports fast boot from NAND Flash, eMMC, SD/TF card and SPI Nor Flash
- Supports system code download through USB OTG
- Boot select pin(FEL) is used to select system boot method: boot from USB when FEL is low level, or else enter into fast boot process

### SDRAM

- Compatible with JEDEC standard DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
- Up to 2GB address space
- 32-bit data bus width
- Supports clock frequency up to 576MHz(DDR3/DDR3L)

### NAND Flash

- Compliant with ONFI 2.3 and Toggle 1.0
- Up to 64-bit ECC per 512 bytes or 1024 bytes
- Supports 1K/2K/4K/8K/16KB page size
- Up to 8-bit data bus width

- Supports 8 chip selects, and 2 ready_busy signals
- Supports SLC/MLC NAND and EF-NAND
- Supports SDR/Toggle DDR/ONFI DDR NAND interface

### SMHC

- Up to four SMHC controllers
- Compatible with eMMC standard specification V5.0, SD physical layer specification V3.0, SDIO card specification V2.0
- 1/4/8-bit bus width
- Embedded special DMA to do data transfer
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

## 2.4. System Peripheral

### Timer

- 6 Timers
- Two 33-bit AVS counters to synchronize video and audio in the player
- One watchdog to generate reset signal or interrupt
- External 24MHz or 32.768kHz crystal oscillator input

### High Speed Timer

- 4 High Speed Timers
- Clock source is fixed to AHBCLK, and the pre-scale ranges from 1 to 16
- 56-bit counter that can be separated to 24-bit high register and 32-bit low register

### RTC

- Timer, Calendar, Alarm
- Supports full clock features: second/minute/hour/day/month/year(with leap year)

### GIC

- Supports 16 SGIs(Software Generated Interrupt), 16 PPIs(Private Peripheral Interrupt) and 101 SPIs(Shared Peripheral Interrupts)
- Supports ARM architecture security extensions
- Supports ARM architecture virtualization extensions

### DMA

- 16 channels
- Interrupt generated for each DMA channel
- Transfers data width of 8/16/32/64-bit
- Supports linear and IO address modes

- Programs the DMA burst size
- Flexible data source and destination address generation
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

### CCU

- 13 PLLs, one external 24MHz oscillator, one external 32768Hz oscillator, an on-chip RC oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

### PWM

- 8 PWM channels outputs(4 PWM pairs)
- Supports capture input
- Supports three kinds of output waveforms: continuous waveform, pulse waveform and complementarity pair
- Programmable deadzone generator and controllable dead-time
- 0% to 100% adjustable duty cycle
- Up to 24/100MHz output frequency
- Minimum resolution is 1/65536
- Supports interrupt for PWM output and capture input

### Thermal Sensor

- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Supports 2 sensors: sensor0 for CPU,sensor1 for GPU

### Crypto Engine

- Supports symmetrical algorithm: AES, DES, 3DES
- Supports hash algorithm: MD5,SHA1,SHA224,SHA256,SHA384,SHA512,HMAC
- Supports asymmetrical algorithm: RSA512,RSA1024,RSA2048
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- AES mode: ECB,CBC,CTR,CTS,OFB,CFB
- DES/3DES mode: ECB,CBC,CTR

### Security ID

- One on-chip efuse
- Size up to 2Kbit for security chip ID
- Supports on-line LDO programming

## 2.5. Video Engine

### Video Decoder

- Supports video decoding up to 1080p@45fps
- Supports multi-formats:
  - MPEG1 MP/HL: 1080p@45fps
  - MPEG2 MP/HL: 1080p@45fps
  - MPEG4 SP/ASP L5: 1080p@45fps
  - H.263 BP: 1080p@45fps
  - H.264 BP/MP/HP Level4.2: 1080p@45fps
  - xvid: 1080p@45fps
  - Sorenson Spark: 1080p@45fps
  - VP6 6.0/6.1/6.2: 1080P@45fps
  - VP8: 1080p@45fps
  - AVS/AVS+ JiZhun: 1080p@45fps
  - WMV7/WMV8: 1080p@45fps
  - WMV9/VC-1 SP/MP/AP: 1080p@30fps
  - JPEG: 16384 x 16384@45MPPS

### Video Encoder

- H.264 HP encoding up to 1080p@45fps
- JPEG baseline: picture size up to 4096x4096
- Supports H.264 encoding input formats:NV12/NV21/YUV420SP,YUV422SP/NV16,NU12/NV21/YVU420SP, YVU422SP/NV61, 32 x 32 tile-based,128 x 32 tile-based,ARGB8888,RGBA8888,ABGR8888,BGRA8888, YU12/YUV420P,YV12/YVU420P,YU16/YUV422P,YV16/YVU422P,raw YUYV422,raw UYVY422,raw YVYU422,raw VYUY422
- Supports JPEG encoding input formats:YUV420/YUV422/YUV444
- Alpha blending
- Thumb generation
- 4x2 scaling ratio from 1/16 to 64 arbitrary non-integer ratio

## 2.6. Display Subsystem

### DE2.0

- Supports output size up to 2048 x 2048
- Supports four alpha blending channels for main display, two channels for aux display
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports motion-adaptive de-interlace for 480i, 576i and 1080i inputs
- Supports input format YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive edge sharping
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports SmartColor2.0 for excellent display experience

### Video Output

- Supports 4 lanes MIPI DSI up to 1080p@60fps
- Supports LVDS interface up to 1920 x 1080@60fps
- Supports RGB interface up to 1920 x 1080@60fps
- Supports TV output, including 4-ch CVBS, 1-ch YPbPr and 1-ch VGA

## 2.7. Image In

- Supports TV decoder: 4-ch analog CVBS or 1-ch YPbPr(480i/576i/480p/576p) signal input
- Dual CMOS sensor parallel interfaces :CSI0 and CSI1
  - Supports 8-bit YUV422 CMOS sensor interface and 8bit BT656 interface for each CSI
  - Supports CCIR656 protocol for each CSI
  - Supports 16-bit BT1120 interface for CSI0
  - Supports 24-bit RGB/YUV444 input for CSI1
  - Supports multi-channel ITU-R BT.656 time-multiplexed format for CSI0
  - CSI0 supports still capture resolution up to 5M,and video capture resolution up to 1080p@30fps
  - CSI1 supports still capture resolution up to 5M,and video capture resolution up to 720p@30fps

## 2.8. Audio Subsystem

### Audio Codec

- Two audio digital-to-analog(DAC) channels
  - Up to 100±3dB SNR during DAC playback
  - Supports DAC sample rate from 8kHz to 192kHz
- Two audio analog-to-digital(ADC) channels
  - Up to 93±3dB SNR during ADC capture
  - Supports ADC sample rate from 8kHz to 48kHz
- Four audio inputs:
  - Two mono microphone inputs
  - One stereo Line-in input
  - One stereo FM-in input
- Two audio outputs:
  - One differential PHONEOUT output
  - One stereo headphone output
- Supports analog/digital volume control
- Supports dynamic range controller adjusting the DAC playback and ADC capture

### I2S/PCM

- Up to two I2S/PCM interfaces
- Compliant with standard Philips Inter-IC sound(I2S) bus specification
- Compliant with left-justified, right-justified, PCM mode, and TDM(Time Division Multiplexing) format
- Full-duplex synchronous work mode
- Master and slave mode configured
- Adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8kHz to 192kHz
- Supports 8-bit u-law and 8-bit A-law companded sample
- Supports programmable PCM frame width:1 BCLK width(short frame) and 2 BCLKs width(long frame)

### One Wire Audio(OWA)

- IEC-60958 transmitter functionality
- Compatible with S/PDIF protocol
- Supports channel status insertion for the transmitter
- Hardware Parity generation on the transmitter
- One 32x24 bits TX FIFO for audio data transfer
- Programmable FIFO thresholds

### AC97

- Compliant with AC97 2.3 component specification
- Full-duplex synchronous serial interface
- Up to 48kHz sampling rate
- Channels support mono or stereo samples of 16(standard),18(optional) and 20(optional) bit wide
- Supports DRA mode

## 2.9. External Peripherals

### USB

- USB 2.0 OTG, with integrated one USB 2.0 analog PHY
  - Compatible with USB2.0 Specification
  - Support High-Speed(HS,480Mbps),Full-Speed(FS,12Mbps),and Low-Speed(LS,1.5Mbps) in host mode
  - Supports High-Speed (HS, 480Mbps), Full-Speed (FS, 12Mbps) in Device mode
  - Up to 8 user-configurable endpoints for Bulk , Isochronous, Control and Interrupt transfer
- Two USB Hosts, with integrated two USB 2.0 analog PHY
  - Compatible with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

### EMAC

- Compliant with IEEE 802.3 standard
- Supports 10/100Mbps data transfer rate
- Supports MII PHY interface
- Supports full and half duplex operations

### GMAC

- Compliant with the IEEE 802.3-2002 standard
- Programmable frame length to support Standard or Jumbo Ethernet frames with size up to 16KB
- Supports 10/100/1000Mbps data transfer rates
- Supports MII/RGMII/RMII PHY interface
- Supports a variety of flexible address filtering modes
- Supports full and half duplex operations

## Transport Stream Controller

- Up to 2 Transport Stream Controllers
- One external Synchronous Parallel Interface(SPI) and one external Synchronous Serial Interface(SSI)
- SPI and SSI timing parameters are configurable
- Multiple transport stream packet(188,192,204) format support
- Supports 32-channel PID filter
- Supports hardware PCR packet detecting
- Supports DVB-CSA V1.1 Descrambler

## TWI

- Up to 5 TWIs(Two Wire Interface)
- Supports Standard mode(up to 100kbit/s) and Fast mode(up to 400kbit/s)
- Master/Slave configurable
- Allows 10-bit addressing transactions

## Smart Card Reader

- Supports ISO/IEC 7816-3 and EMV2000(4.0) specifications
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Supports configurable timing functions:
  - Smart Card activation time
  - Smart Card reset time
  - Guard time
  - Timeout timers

## SPI

- Up to 4 independent SPI controllers,each SPI controller with two CS signals
- Full-duplex synchronous serial interface
- Master/Slave configurable
- 1-,or 2-wire mode
- Polarity and phase are configurable
- SPI clock is configurable

## UART

- Up to 8 UART controllers
  - UART0 with 2 wires for debug tools
  - UART1 with 8 wires
  - UART2/3 each with 4 wires

- Others with 2 wires
- Compatible with industry-standard 16550 UARTs
- Supports for word length from 5 to 8 bits, an optional parity bit, and 1,1.5 or 2 stop bits
- Programmable parity(even, odd and no parity)

## PS2

- Two PS2 controllers
- Compliant with IBM PS2 and AT-compatible keyboard and mouse interface
- Dual-role controller: PS2 host or PS2 device
- Odd parity generation and checking

## CIR

- Two CIR controllers
- Flexible receiver for consumer IR remote control
- Programmable FIFO thresholds

## SATA

- One SATA Host controller
- Supports SATA 1.5Gb/s and SATA 3.0Gb/s
- Compliant with SATA spec 2.6 and AHCI Revision 1.3 specifications
- Supports external SATA(eSATA)
- Supports power management features including automatic Partial to Slumber transition

## Keypad

- One keypad matrix interface up to 8 rows and 8 columns
- Interrupt for key press or key release
- Internal debouncing filter to prevent switching noises

## KEYADC

- Up to two ADC channels for key application
- 6-bit resolution
- Voltage input range between 0V to 2V
- Supports hold key,already hold key and continuous key
- Supports single,normal and continuous mode

## RTP

- 4-wire I/F
- 12-bit SAR type A/D converter
- Dual touch detection
- Sampling frequency up to 2MHz
- Supports X,Y change function

## 2.10. Package

- LFBGA 468 balls, 0.65 mm ball pitch, 16 mm x 16 mm

# 3. Block Diagram

Figure 3-1 shows the block diagram of the T3 processor.

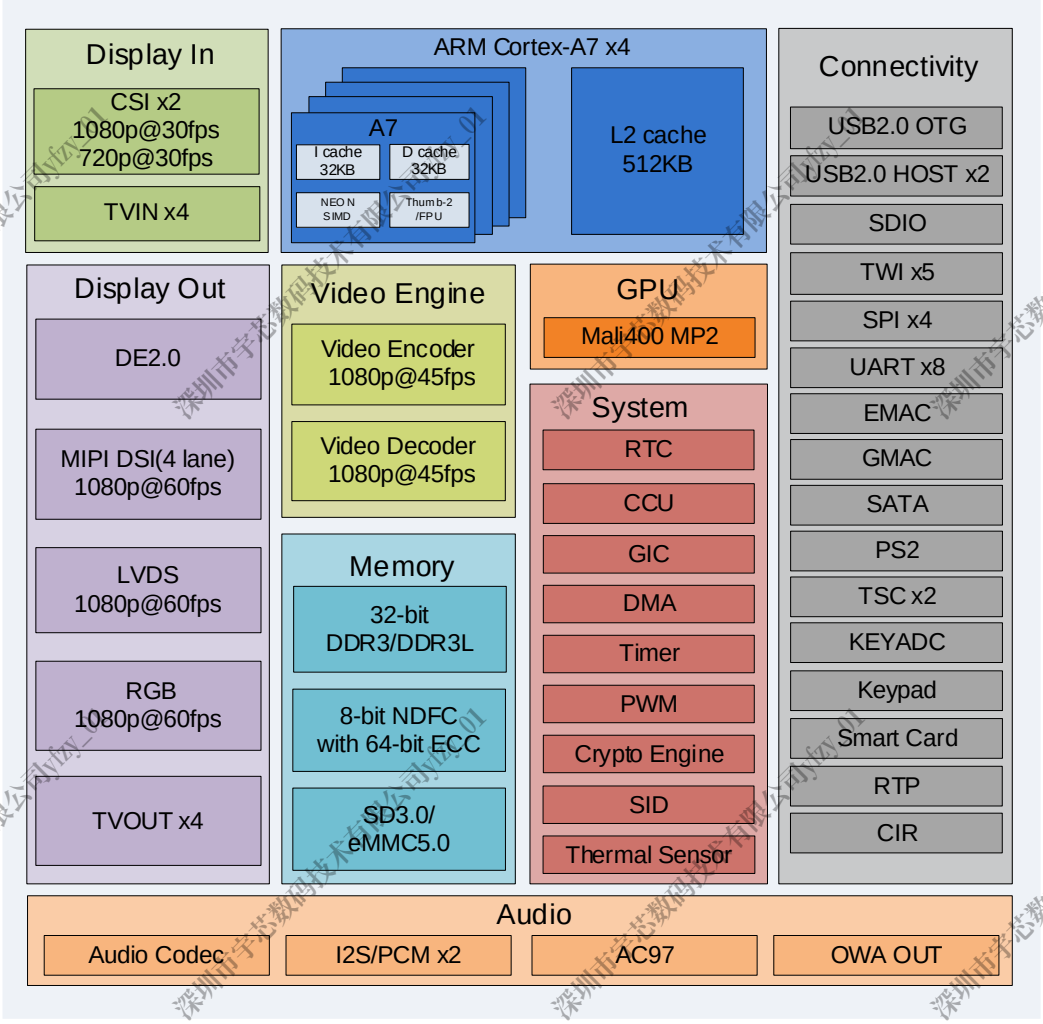



**Figure 3-1. T3 Block Diagram**

The typical application diagram is shown in Figure 3-2.

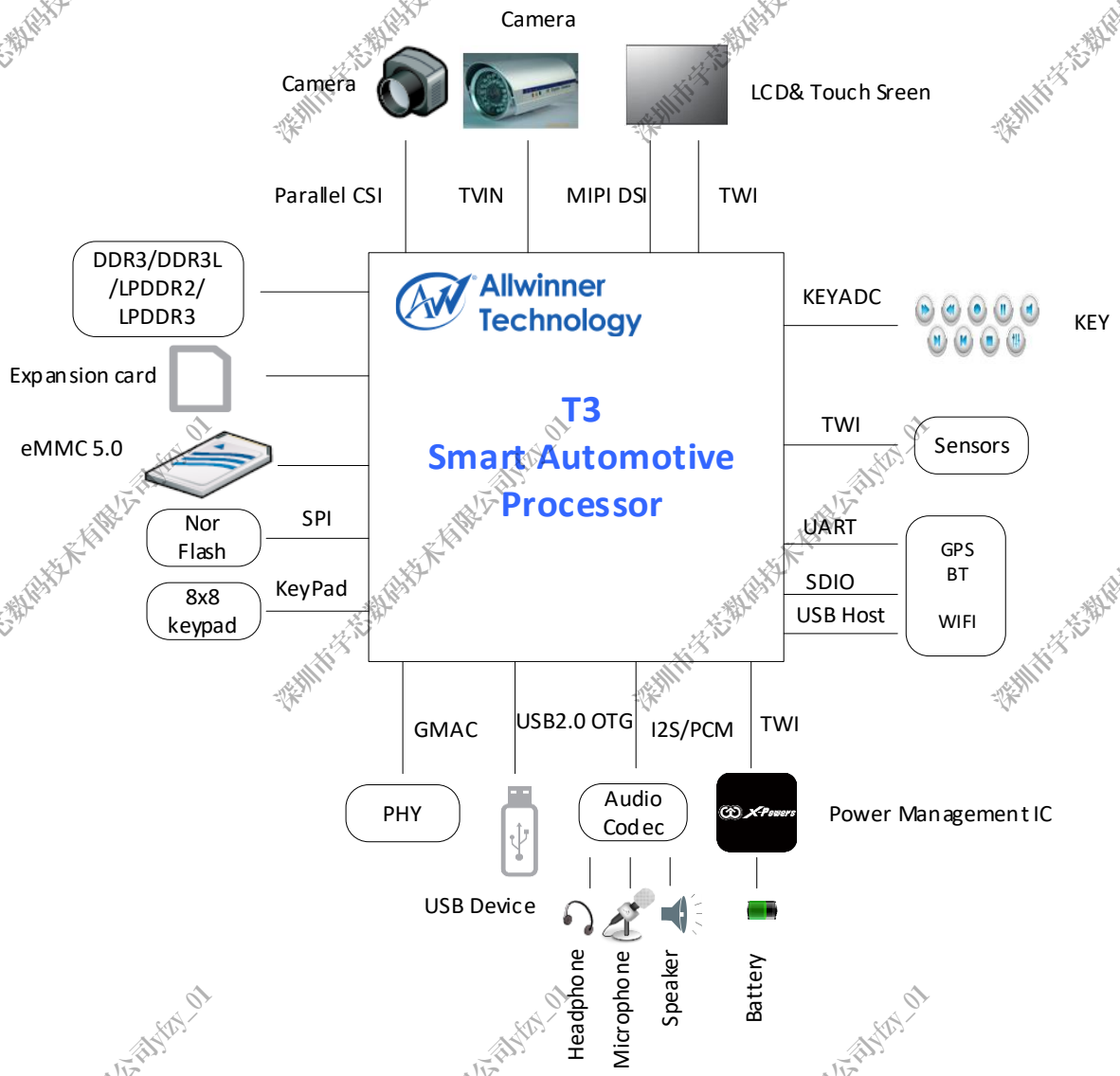



**Figure 3-2. T3 Application Diagram**

# 4. Pin Description

## 4.1. Pin Characteristics

Table 4-1 lists the characteristics of T3 pins from the following ten aspects.

(1).**Ball#**: Package ball numbers associated with each signals.

(2).**Pin Name**: The name of the package pin.

(3).**Signal Name**: The signal name for that pin in the mode being used.

(4).**Function**: Multiplexing function number.

(5).**Ball Reset Rel. Function**: The function is automatically configured after RESET from low to high.

(6).**Type**: Denotes the signal direction

I (Input),
O (Output),
I/O (Input/Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),
AO (Analog Output)
P (Power),
G (Ground)

(7).**Ball Reset State**: The state of the terminal at reset.

(8).**Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

(9).**Buffer Strength**: Defines maximum drive strength of the associated output buffer.

(10).**Power Supply**: The voltage supply for the terminal's IO buffers.

**Table 4-1. Pin Characteristics**

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| **DRAM** | | | | | | | | | |
| F6 | SA0/SCAS | SA0/SCAS | NA | NA | O | Z | NA | NA | VCC-DRAM |
| H5 | SA1 | SA1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| G5 | SA2 | SA2 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| F4 | SA3 | SA3 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| E6 | SA4/SA11 | SA4/SA11 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| E12 | SA5 | SA5 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| C14 | SA6 | SA6 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| F13 | SA7/SBA0 | SA7/SBA0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| D16 | SA8 | SA8 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| E17 | SA9 | SA9 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| E11 | SA10 | SA10 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| E7 | SA11/SA4 | SA11/SA4 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| C13 | SA12 | SA12 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| H3 | SA13 | SA13 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| E9 | SA14 | SA14 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| E4 | SA15/SCS1 | SA15/SCS1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| C16 | SBA0/SA7 | SBA0/SA7 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| E14 | SBA1 | SBA1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| D17 | SBA2 | SBA2 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| C5 | SCAS/SA0 | SCAS/SA0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| C8 | SCKN | SCKN | NA | NA | O | Z | NA | NA | VCC-DRAM |
| C7 | SCKP | SCKP | NA | NA | O | Z | NA | NA | VCC-DRAM |
| C6 | SCKE0 | SCKE0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| D3 | SCKE1 | SCKE1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| F3 | SCS0 | SCS0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| D6 | SODT0 | SODT0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| C3 | SODT1 | SODT1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| F2 | SDQ0 | SDQ0 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| D2 | SDQ1 | SDQ1 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| G1 | SDQ2 | SDQ2 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| D1 | SDQ3 | SDQ3 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| G2 | SDQ4 | SDQ4 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| F1 | SDQ5 | SDQ5 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| C1 | SDQ6 | SDQ6 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| C2 | SDQ7 | SDQ7 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A5 | SDQ8 | SDQ8 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A3 | SDQ9 | SDQ9 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A6 | SDQ10 | SDQ10 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A2 | SDQ11 | SDQ11 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B3 | SDQ12 | SDQ12 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B6 | SDQ13 | SDQ13 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B2 | SDQ14 | SDQ14 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B5 | SDQ15 | SDQ15 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B7 | SDQ16 | SDQ16 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| C11 | SDQ17 | SDQ17 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A8 | SDQ18 | SDQ18 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| C9 | SDQ19 | SDQ19 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B11 | SDQ20 | SDQ20 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B9 | SDQ21 | SDQ21 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| C12 | SDQ22 | SDQ22 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A9 | SDQ23 | SDQ23 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A16 | SDQ24 | SDQ24 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A13 | SDQ25 | SDQ25 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A17 | SDQ26 | SDQ26 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A14 | SDQ27 | SDQ27 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B13 | SDQ28 | SDQ28 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B17 | SDQ29 | SDQ29 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B14 | SDQ30 | SDQ30 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B16 | SDQ31 | SDQ31 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| G3 | SDQM0 | SDQM0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| B1 | SDQM1 | SDQM1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| A7 | SDQM2 | SDQM2 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| A12 | SDQM3 | SDQM3 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| E2 | SDQS0N | SDQS0N | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| E1 | SDQS0P | SDQS0P | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B4 | SDQS1N | SDQS1N | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A4 | SDQS1P | SDQS1P | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B10 | SDQS2N | SDQS2N | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A10 | SDQS2P | SDQS2P | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| B15 | SDQS3N | SDQS3N | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| A15 | SDQS3P | SDQS3P | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| E15 | SRAS | SRAS | NA | NA | O | Z | NA | NA | VCC-DRAM |
| E8 | SRST | SRST | NA | NA | O | Z | NA | NA | VCC-DRAM |
| D9 | SVREF | SVREF | NA | NA | P | Z | NA | NA | VCC-DRAM |
| G6 | SWE | SWE | NA | NA | O | Z | NA | NA | VCC-DRAM |
| H1 | SZQ | SZQ | NA | NA | AI | Z | NA | NA | VCC-DRAM |
| G11,G12,G14, G15,G16,H7,H10, H12,H13,J8 | VCC-DRAM | VCC-DRAM | NA | NA | P | NA | NA | NA | NA |
| **GPIOA** | | | | | | | | | |
| L23 | PA0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ERXD3 | 2 | | I | | | | |
| | | SPI1_CS0 | 3 | | I/O | | | | |
| | | UART2_RTS | 4 | | O | | | | |
| | | GRXD3 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M19 | PA1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ERXD2 | 2 | | I | | | | |
| | | SPI1_CLK | 3 | | I/O | | | | |
| | | UART2_CTS | 4 | | I | | | | |
| | | GRXD2 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M23 | PA2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ERXD1 | 2 | | I | | | | |
| | | SPI1_MOSI | 3 | | I/O | | | | |
| | | UART2_TX | 4 | | O | | | | |
| | | GRXD1 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M22 | PA3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ERXD0 | 2 | | I | | | | |
| | | SPI1_MISO | 3 | | I/O | | | | |
| | | UART2_RX | 4 | | I | | | | |
| | | GRXD0 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M21 | PA4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ETXD3 | 2 | | O | | | | |
| | | SPI1_CS1 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | GTXD3 | 5 | | O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M20 | PA5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ETXD2 | 2 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI3_CS0 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | GTXD2 | 5 | | O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M24 | PA6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ETXD1 | 2 | | O | | | | |
| | | SPI3_CLK | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | GTXD1 | 5 | | O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N24 | PA7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ETXD0 | 2 | | O | | | | |
| | | SPI3_MOSI | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | GTXD0 | 5 | | O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N23 | PA8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ERXCK | 2 | | I | | | | |
| | | SPI3_MISO | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | GRXCK | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N22 | PA9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ERXERR | 2 | | I | | | | |
| | | SPI3_CS1 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | GNULL/ERXERR | 5 | | I | | | | |
| | | I2S1_MCLK | 6 | | O | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N21 | PA10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ERXDV | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | UART1_TX | 4 | | O | | | | |
| | | GRXCTL/ERXDV | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N20 | PA11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | EMDC | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | UART1_RX | 4 | | I | | | | |
| | | GMDC | 5 | | O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N19 | PA12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | EMDIO | 2 | | I/O | | | | |
| | | UART6_TX | 3 | | O | | | | |
| | | UART1_RTS | 4 | | O | | | | |
| | | GMDIO | 5 | | I/O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| P23 | PA13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | ETXEN | 2 | | O | | | | |
| | | UART6_RX | 3 | | I | | | | |
| | | UART1_CTS | 4 | | I | | | | |
| | | GTXCTL/ETXEN | 5 | | O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| P22 | PA14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ETXCK | 2 | | I | | | | |
| | | UART7_TX | 3 | | O | | | | |
| | | UART1_DTR | 4 | | O | | | | |
| | | GNULL/ETXCK | 5 | | I | | | | |
| | | I2S1_BCLK | 6 | | I/O | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R22 | PA15 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ECRS | 2 | | I | | | | |
| | | UART7_RX | 3 | | I | | | | |
| | | UART1_DSR | 4 | | I | | | | |
| | | GTXCK/ECRS | 5 | | O,I | | | | |
| | | I2S1_LRCK | 6 | | I/O | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R21 | PA16 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ECOL | 2 | | I | | | | |
| | | Reserved | 3 | | O | | | | |
| | | UART1_DCD | 4 | | I | | | | |
| | | GCLKIN/ECOL | 5 | | I | | | | |
| | | I2S1_DO | 6 | | O | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R20 | PA17 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PA |
| | | Output | 1 | | O | | | | |
| | | ETXERR | 2 | | O | | | | |
| | | Reserved | 3 | | I | | | | |
| | | UART1_RING | 4 | | I | | | | |
| | | GNULL/ETXERR | 5 | | O | | | | |
| | | I2S1_DI | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| L17 | VCC-PA | VCC-PA | NA | NA | P | NA | NA | NA | NA |
| **GPIOB** | | | | | | | | | |
| L22 | PB0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI0_SCK | 2 | | I/O | | | | |
| | | PLL_LOCK_DBG | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K22 | PB1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI0_SDA | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K23 | PB2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | PWM0 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | IO Disable | 7 | | OFF | | | | |
| K24 | PB3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | PWM1 | 3 | | I/O | | | | |
| | | OWA_MCLK | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J24 | PB4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | CIR0_RX | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K20 | PB5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | I2S_MCLK | 2 | | O | | | | |
| | | AC97_MCLK | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K21 | PB6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | I2S_BCLK | 2 | | I/O | | | | |
| | | AC97_BCLK | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J20 | PB7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | I2S_LRCK | 2 | | I/O | | | | |
| | | AC97_SYNC | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J21 | PB8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | I2S_DO0 | 2 | | O | | | | |
| | | AC97_DO | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J22 | PB9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | I2S_DO1 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | PWM6 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J23 | PB10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | I2S_DO2 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | PWM7 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J19 | PB11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | I2S_DO3 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G19 | PB12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | I2S_DI | 2 | | I | | | | |
| | | AC97_DI | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G20 | PB13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI2_CS1 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | OWA_DO | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G21 | PB14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI2_CS0 | 2 | | I/O | | | | |
| | | JTAG_MS0 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| H22 | PB15 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI2_CLK | 2 | | I/O | | | | |
| | | JTAG_CK0 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| H23 | PB16 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI2_MOSI | 2 | | I/O | | | | |
| | | JTAG_DO0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G22 | PB17 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI2_MISO | 2 | | I/O | | | | |
| | | JTAG_DI0 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G23 | PB18 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI1_SCK | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G24 | PB19 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI1_SDA | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F24 | PB20 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI2_SCK | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | PWM4 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F21 | PB21 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI2_SDA | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | PWM5 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F22 | PB22 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART0_TX | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F23 | PB23 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART0_RX | 2 | | I | | | | |
| | | CIR1_RX | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| **GPIOC** | | | | | | | | | |
| AB11 | PC0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NWE | 2 | | O | | | | |
| | | SPI0_MOSI | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC10 | PC1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NALE | 2 | | O | | | | |
| | | SPI0_MISO | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD10 | PC2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NCLE | 2 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI0_CLK | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB12 | PC3 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NCE1 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W16 | PC4 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NCE0 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC18 | PC5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NRE | 2 | | O | | | | |
| | | SDC2_DS | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC12 | PC6 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NRB0 | 2 | | I | | | | |
| | | SDC2_CMD | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB13 | PC7 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NRB1 | 2 | | I | | | | |
| | | SDC2_CLK | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC14 | PC8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NDQ0 | 2 | | I/O | | | | |
| | | SDC2_D0 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB15 | PC9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NDQ1 | 2 | | I/O | | | | |
| | | SDC2_D1 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC17 | PC10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | NDQ2 | 2 | | I/O | | | | |
| | | SDC2_D2 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC13 | PC11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NDQ3 | 2 | | I/O | | | | |
| | | SDC2_D3 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD14 | PC12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NDQ4 | 2 | | I/O | | | | |
| | | SDC2_D4 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC15 | PC13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NDQ5 | 2 | | I/O | | | | |
| | | SDC2_D5 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD16 | PC14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NDQ6 | 2 | | I/O | | | | |
| | | SDC2_D6 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD17 | PC15 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NDQ7 | 2 | | I/O | | | | |
| | | SDC2_D7 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| Y14 | PC16 | Input | 0 | Function7 | I | PD | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NWP | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC16 | PC17 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NCE2 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB16 | PC18 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Output | 1 | | O | | | | |
| | | NCE3 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AA16 | PC19 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NCE4 | 2 | | O | | | | |
| | | SPI2_CS0 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB18 | PC20 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NCE5 | 2 | | O | | | | |
| | | SPI2_CLK | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AA14 | PC21 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NCE6 | 2 | | O | | | | |
| | | SPI2_MOSI | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| Y16 | PC22 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NCE7 | 2 | | O | | | | |
| | | SPI2_MISO | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB17 | PC23 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | SPI0_CS0 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD13 | PC24 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NDQS | 2 | | I/O | | | | |
| | | SDC2_RST | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T15,U15 | VCC-PC | VCC-PC | NA | NA | P | NA | NA | NA | NA |
| **GPIOD** | | | | | | | | | |
| M2 | PD0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D0 | 2 | | O | | | | |
| | | LVDS0_VP0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M1 | PD1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D1 | 2 | | O | | | | |
| | | LVDS0_VN0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N2 | PD2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D2 | 2 | | O | | | | |
| | | LVDS0_VP1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M3 | PD3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D3 | 2 | | O | | | | |
| | | LVDS0_VN1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| P1 | PD4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D4 | 2 | | O | | | | |
| | | LVDS0_VP2 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| P2 | PD5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D5 | 2 | | O | | | | |
| | | LVDS0_VN2 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R1 | PD6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D6 | 2 | | O | | | | |
| | | LVDS0_VPC | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| P3 | PD7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D7 | 2 | | O | | | | |
| | | LVDS0_VNC | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R2 | PD8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D8 | 2 | | O | | | | |
| | | LVDS0_VP3 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R3 | PD9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D9 | 2 | | O | | | | |
| | | LVDS0_VN3 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| L5 | PD10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D10 | 2 | | O | | | | |
| | | LVDS1_VP0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| L4 | PD11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D11 | 2 | | O | | | | |
| | | LVDS1_VN0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| L3 | PD12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D12 | 2 | | O | | | | |
| | | LVDS1_VP1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M4 | PD13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D13 | 2 | | O | | | | |
| | | LVDS1_VN1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N3 | PD14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D14 | 2 | | O | | | | |
| | | LVDS1_VP2 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N4 | PD15 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D15 | 2 | | O | | | | |
| | | LVDS1_VN2 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| P5 | PD16 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D16 | 2 | | O | | | | |
| | | LVDS1_VPC | 3 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| P4 | PD17 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D17 | 2 | | O | | | | |
| | | LVDS1_VNC | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R5 | PD18 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D18 | 2 | | O | | | | |
| | | LVDS1_VP3 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R4 | PD19 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D19 | 2 | | O | | | | |
| | | LVDS1_VN3 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T2 | PD20 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D20 | 2 | | O | | | | |
| | | CSI1_MCLK | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U1 | PD21 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D21 | 2 | | O | | | | |
| | | SMC_VPPEN | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U2 | PD22 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D22 | 2 | | O | | | | |
| | | SMC_VPPPP | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T3 | PD23 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_D23 | 2 | | O | | | | |
| | | SMC_DET | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T4 | PD24 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_CLK | 2 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | SMC_VCCEN | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T5 | PD25 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_DE | 2 | | O | | | | |
| | | SMC_RST | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U5 | PD26 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_HSYNC | 2 | | O | | | | |
| | | SMC_SLK | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U6 | PD27 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD0_VSYNC | 2 | | O | | | | |
| | | SMC_SDA | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N7,N8 | VCC-PD | VCC-PD | NA | NA | P | NA | NA | NA | NA |
| **GPIOE** | | | | | | | | | |
| AA17 | PE0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_CLK | 2 | | I | | | | |
| | | CSI0_PCLK | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| Y17 | PE1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_ERR | 2 | | I | | | | |
| | | CSI0_MCLK | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W17 | PE2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_SYNC | 2 | | I | | | | |
| | | CSI0_HSYNC | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W19 | PE3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_DVLD | 2 | | I | | | | |
| | | CSI0_VSYNC | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| Y19 | PE4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_D0 | 2 | | I | | | | |
| | | CSI0_D0 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AA19 | PE5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_D1 | 2 | | I | | | | |
| | | CSI0_D1 | 3 | | I | | | | |
| | | SMC_VPPEN | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB19 | PE6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_D2 | 2 | | I | | | | |
| | | CSI0_D2 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC19 | PE7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_D3 | 2 | | I | | | | |
| | | CSI0_D3 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD19 | PE8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_D4 | 2 | | I | | | | |
| | | CSI0_D4 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD20 | PE9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_D5 | 2 | | I | | | | |
| | | CSI0_D5 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB20 | PE10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_D6 | 2 | | I | | | | |
| | | CSI0_D6 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC20 | PE11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | TS0_D7 | 2 | | I | | | | |
| | | CSI0_D7 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | IO Disable | 7 | | OFF | | | | |
| U17 | VCC-PE | VCC-PE | NA | NA | P | NA | NA | NA | NA |
| **GPIOF** | | | | | | | | | |
| AA11 | PF0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PF |
| | | Output | 1 | | O | | | | |
| | | SDC0_D1 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | JTAG_MS1 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| Y11 | PF1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PF |
| | | Output | 1 | | O | | | | |
| | | SDC0_D0 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | JTAG_DI1 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W11 | PF2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PF |
| | | Output | 1 | | O | | | | |
| | | SDC0_CLK | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | UART0_TX | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AA13 | PF3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PF |
| | | Output | 1 | | O | | | | |
| | | SDC0_CMD | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | JTAG_DO1 | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| Y13 | PF4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PF |
| | | Output | 1 | | O | | | | |
| | | SDC0_D3 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | UART0_RX | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W13 | PF5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PF |
| | | Output | 1 | | O | | | | |
| | | SDC0_D2 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | JTAG_CK1 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T12 | VCC-PF | VCC-PF | NA | NA | P | NA | NA | NA | NA |
| **GPIOG** | | | | | | | | | |
| AA20 | PG0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | TS1_CLK | 2 | | I | | | | |
| | | CSI1_PCLK | 3 | | I | | | | |
| | | SDC1_CMD | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| Y20 | PG1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | TS1_ERR | 2 | | I | | | | |
| | | CSI1_MCLK | 3 | | O | | | | |
| | | SDC1_CLK | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB21 | PG2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | TS1_SYNC | 2 | | I | | | | |
| | | CSI1_HSYNC | 3 | | I | | | | |
| | | SDC1_D0 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC21 | PG3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | TS1_DVLD | 2 | | I | | | | |
| | | CSI1_VSYNC | 3 | | I | | | | |
| | | SDC1_D1 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB22 | PG4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | TS1_D0 | 2 | | I | | | | |
| | | CSI1_D0 | 3 | | I | | | | |
| | | SDC1_D2 | 4 | | I/O | | | | |
| | | CSI0_D8 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC22 | PG5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | TS1_D1 | 2 | | I | | | | |
| | | CSI1_D1 | 3 | | I | | | | |
| | | SDC1_D3 | 4 | | I/O | | | | |
| | | CSI0_D9 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD22 | PG6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | TS1_D2 | 2 | | I | | | | |
| | | CSI1_D2 | 3 | | I | | | | |
| | | UART3_TX | 4 | | O | | | | |
| | | CSI0_D10 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD23 | PG7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | TS1_D3 | 2 | | I | | | | |
| | | CSI1_D3 | 3 | | I | | | | |
| | | UART3_RX | 4 | | I | | | | |
| | | CSI0_D11 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC23 | PG8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | TS1_D4 | 2 | | I | | | | |
| | | CSI1_D4 | 3 | | I | | | | |
| | | UART3_RTS | 4 | | O | | | | |
| | | CSI0_D12 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC24 | PG9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Output | 1 | | O | | | | |
| | | TS1_D5 | 2 | | I | | | | |
| | | CSI1_D5 | 3 | | I | | | | |
| | | UART3_CTS | 4 | | I | | | | |
| | | CSI0_D13 | 5 | | I | | | | |
| | | BIST_RESULT0 | 6 | | I/O | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB23 | PG10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | TS1_D6 | 2 | | I | | | | |
| | | CSI1_D6 | 3 | | I | | | | |
| | | UART4_TX | 4 | | O | | | | |
| | | CSI0_D14 | 5 | | I | | | | |
| | | BIST_RESULT1 | 6 | | I/O | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| | | Input | 0 | | I | | | | |
| | | Output | 1 | | O | | | | |
| | | TS1_D7 | 2 | | I | | | | |
| AB24 | PG11 | CSI1_D7 | 3 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | UART4_RX | 4 | | I | | | | |
| | | CSI0_D15 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T17 | VCC-PG | VCC-PG | NA | NA | P | NA | NA | NA | NA |
| **GPIOH** | | | | | | | | | |
| | | Input | 0 | | I | | | | |
| | | Output | 1 | | O | | | | |
| | | LCD1_D0 | 2 | | O | | | | |
| | | IO Disable | 3 | | OFF | | | | |
| | | UART3_TX | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT0 | 6 | | I | | | | |
| D23 | PH0 | CSI1_D0 | 7 | Function3 | I | Z | PU/PD | 6 | VCC-IO |
| | | Input | 0 | | I | | | | |
| | | Output | 1 | | O | | | | |
| | | LCD1_D1 | 2 | | O | | | | |
| | | IO Disable | 3 | | OFF | | | | |
| | | UART3_RX | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT1 | 6 | | I | | | | |
| E23 | PH1 | CSI1_D1 | 7 | Function3 | I | Z | PU/PD | 6 | VCC-IO |
| | | Input | 0 | | I | | | | |
| | | Output | 1 | | O | | | | |
| | | LCD1_D2 | 2 | | O | | | | |
| | | IO Disable | 3 | | OFF | | | | |
| | | UART3_RTS | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT2 | 6 | | I | | | | |
| D24 | PH2 | CSI1_D2 | 7 | Function3 | I | Z | PU/PD | 6 | VCC-IO |
| | | Input | 0 | | I | | | | |
| | | Output | 1 | | O | | | | |
| | | LCD1_D3 | 2 | | O | | | | |
| | | IO Disable | 3 | | OFF | | | | |
| | | UART3_CTS | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT3 | 6 | | I | | | | |
| E22 | PH3 | CSI1_D3 | 7 | Function3 | I | Z | PU/PD | 6 | VCC-IO |
| | | Input | 0 | | I | | | | |
| | | Output | 1 | | O | | | | |
| | | LCD1_D4 | 2 | | O | | | | |
| | | IO Disable | 3 | | OFF | | | | |
| | | UART4_TX | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| C23 | PH4 | | | Function3 | | Z | PU/PD | 6 | VCC-IO |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | EINT4 | 6 | | I | | | | |
| | | CSI1_D4 | 7 | | I | | | | |
| C24 | PH5 | Input | 0 | Function3 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D5 | 2 | | O | | | | |
| | | IO Disable | 3 | | OFF | | | | |
| | | UART4_RX | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT5 | 6 | | I | | | | |
| | | CSI1_D5 | 7 | | I | | | | |
| B24 | PH6 | Input | 0 | Function3 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D6 | 2 | | O | | | | |
| | | IO Disable | 3 | | OFF | | | | |
| | | UART5_TX | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT6 | 6 | | I | | | | |
| | | CSI1_D6 | 7 | | I | | | | |
| B22 | PH7 | Input | 0 | Function3 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D7 | 2 | | O | | | | |
| | | IO Disable | 3 | | OFF | | | | |
| | | UART5_RX | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT7 | 6 | | I | | | | |
| | | CSI1_D7 | 7 | | I | | | | |
| B23 | PH8 | Input | 0 | Function0 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D8 | 2 | | O | | | | |
| | | ERXD3 | 3 | | I | | | | |
| | | KP_IN0 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT8 | 6 | | I | | | | |
| | | CSI1_D8 | 7 | | I | | | | |
| A23 | PH9 | Input | 0 | Function0 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D9 | 2 | | O | | | | |
| | | ERXD2 | 3 | | I | | | | |
| | | KP_IN1 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT9 | 6 | | I | | | | |
| | | CSI1_D9 | 7 | | I | | | | |
| A22 | PH10 | Input | 0 | Function0 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D10 | 2 | | O | | | | |
| | | ERXD1 | 3 | | I | | | | |
| | | KP_IN2 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT10 | 6 | | I | | | | |
| | | CSI1_D10 | 7 | | I | | | | |
| C21 | PH11 | Input | 0 | Function0 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D11 | 2 | | O | | | | |
| | | ERXD0 | 3 | | I | | | | |
| | | KP_IN3 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT11 | 6 | | I | | | | |
| | | CSI1_D11 | 7 | | I | | | | |
| D22 | PH12 | Input | 0 | Function3 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D12 | 2 | | O | | | | |
| | | IO Disable | 3 | | OFF | | | | |
| | | PS2_SCK1 | 4 | | I/O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 5 | | NA | | | | |
| | | EINT12 | 6 | | I | | | | |
| | | CSI1_D12 | 7 | | I | | | | |
| C22 | PH13 | Input | 0 | Function3 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D13 | 2 | | O | | | | |
| | | IO Disable | 3 | | OFF | | | | |
| | | PS2_SDA1 | 4 | | I/O | | | | |
| | | SMC_RST | 5 | | O | | | | |
| | | EINT13 | 6 | | I | | | | |
| | | CSI1_D13 | 7 | | I | | | | |
| B21 | PH14 | Input | 0 | Function0 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D14 | 2 | | O | | | | |
| | | ETXD3 | 3 | | O | | | | |
| | | KP_IN4 | 4 | | I | | | | |
| | | SMC_VPPEN | 5 | | O | | | | |
| | | EINT14 | 6 | | I | | | | |
| | | CSI1_D14 | 7 | | I | | | | |
| A21 | PH15 | Input | 0 | Function0 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D15 | 2 | | O | | | | |
| | | ETXD2 | 3 | | O | | | | |
| | | KP_IN5 | 4 | | I | | | | |
| | | SMC_VPPPP | 5 | | O | | | | |
| | | EINT15 | 6 | | I | | | | |
| | | CSI1_D15 | 7 | | I | | | | |
| D21 | PH16 | Input | 0 | Function5 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D16 | 2 | | O | | | | |
| | | ETXD1 | 3 | | O | | | | |
| | | KP_IN6 | 4 | | I | | | | |
| | | SMC_DET | 5 | | I | | | | |
| | | EINT16 | 6 | | I | | | | |
| | | CSI1_D16 | 7 | | I | | | | |
| D18 | PH17 | Input | 0 | Function0 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D17 | 2 | | O | | | | |
| | | ETXD0 | 3 | | O | | | | |
| | | KP_IN7 | 4 | | I | | | | |
| | | SMC_VCCEN | 5 | | O | | | | |
| | | EINT17 | 6 | | I | | | | |
| | | CSI1_D17 | 7 | | I | | | | |
| C18 | PH18 | Input | 0 | Function0 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D18 | 2 | | O | | | | |
| | | ERXCK | 3 | | I | | | | |
| | | KP_OUT0 | 4 | | O | | | | |
| | | SMC_SLK | 5 | | O | | | | |
| | | EINT18 | 6 | | I | | | | |
| | | CSI1_D18 | 7 | | I | | | | |
| E19 | PH19 | Input | 0 | Function0 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D19 | 2 | | O | | | | |
| | | ERXERR | 3 | | I | | | | |
| | | KP_OUT1 | 4 | | O | | | | |
| | | SMC_SDA | 5 | | I/O | | | | |
| | | EINT19 | 6 | | I | | | | |
| | | CSI1_D19 | 7 | | I | | | | |
| F18 | PH20 | Input | 0 | Function5 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D20 | 2 | | O | | | | |
| | | ERXDV | 3 | | I | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 4 | | O | | | | |
| | | IO Disable | 5 | | OFF | | | | |
| | | EINT20 | 6 | | I | | | | |
| | | CSI1_D20 | 7 | | I | | | | |
| D19 | PH21 | Input | 0 | Function5 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D21 | 2 | | O | | | | |
| | | EMDC | 3 | | O | | | | |
| | | Reserved | 4 | | I | | | | |
| | | IO Disable | 5 | | OFF | | | | |
| | | EINT21 | 6 | | I | | | | |
| | | CSI1_D21 | 7 | | I | | | | |
| G17 | PH22 | Input | 0 | Function6 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D22 | 2 | | O | | | | |
| | | EMDIO | 3 | | I/O | | | | |
| | | KP_OUT2 | 4 | | O | | | | |
| | | SDC1_CMD | 5 | | I/O | | | | |
| | | IO Disable | 6 | | OFF | | | | |
| | | CSI1_D22 | 7 | | I | | | | |
| C19 | PH23 | Input | 0 | Function6 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_D23 | 2 | | O | | | | |
| | | ETXEN | 3 | | O | | | | |
| | | KP_OUT3 | 4 | | O | | | | |
| | | SDC1_CLK | 5 | | O | | | | |
| | | IO Disable | 6 | | OFF | | | | |
| | | CSI1_D23 | 7 | | I | | | | |
| B18 | PH24 | Input | 0 | Function6 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_CLK | 2 | | O | | | | |
| | | ETXCK | 3 | | I | | | | |
| | | KP_OUT4 | 4 | | O | | | | |
| | | SDC1_D0 | 5 | | I/O | | | | |
| | | IO Disable | 6 | | OFF | | | | |
| | | CSI1_PCLK | 7 | | I | | | | |
| E18 | PH25 | Input | 0 | Function6 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_DE | 2 | | O | | | | |
| | | ECRS | 3 | | I | | | | |
| | | KP_OUT5 | 4 | | O | | | | |
| | | SDC1_D1 | 5 | | I/O | | | | |
| | | IO Disable | 6 | | OFF | | | | |
| | | CSI1_FIELD | 7 | | I/O | | | | |
| A18 | PH26 | Input | 0 | Function6 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_HSYNC | 2 | | O | | | | |
| | | ECOL | 3 | | I | | | | |
| | | KP_OUT6 | 4 | | O | | | | |
| | | SDC1_D2 | 5 | | I/O | | | | |
| | | IO Disable | 6 | | OFF | | | | |
| | | CSI1_HSYNC | 7 | | I | | | | |
| B19 | PH27 | Input | 0 | Function6 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD1_VSYNC | 2 | | O | | | | |
| | | ETXERR | 3 | | O | | | | |
| | | KP_OUT7 | 4 | | O | | | | |
| | | SDC1_D3 | 5 | | I/O | | | | |
| | | IO Disable | 6 | | OFF | | | | |
| | | CSI1_VSYNC | 7 | | I | | | | |
| **GPIO I** | | | | | | | | | |
| AA22 | PI0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 2 | | NA | | | | |
| | | TWI3_SCK | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AA23 | PI1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | TWI3_SDA | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AA24 | PI2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | TWI4_SCK | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| Y22 | PI3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | PWM1 | 2 | | I/O | | | | |
| | | TWI4_SDA | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| Y23 | PI4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC3_CMD | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W22 | PI5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC3_CLK | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W23 | PI6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC3_D0 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W24 | PI7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC3_D1 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W20 | PI8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Output | 1 | | O | | | | |
| | | SDC3_D2 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V22 | PI9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC3_D3 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V23 | PI10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI0_CS0 | 2 | | I/O | | | | |
| | | UART5_TX | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT22 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V24 | PI11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI0_CLK | 2 | | I/O | | | | |
| | | UART5_RX | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT23 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U18 | PI12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI0_MOSI | 2 | | I/O | | | | |
| | | UART6_TX | 3 | | O | | | | |
| | | CLK_OUT_A | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT24 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V21 | PI13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI0_MISO | 2 | | I/O | | | | |
| | | UART6_RX | 3 | | I | | | | |
| | | CLK_OUT_B | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT25 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U23 | PI14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI0_CS1 | 2 | | I/O | | | | |
| | | PS2_SCK1 | 3 | | I/O | | | | |
| | | TCLKIN0 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT26 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U22 | PI15 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI1_CS1 | 2 | | I/O | | | | |
| | | PS2_SDA1 | 3 | | I/O | | | | |
| | | TCLKIN1 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT27 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| T19 | PI16 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI1_CS0 | 2 | | I/O | | | | |
| | | UART2_RTS | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT28 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T23 | PI17 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI1_CLK | 2 | | I/O | | | | |
| | | UART2_CTS | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT29 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T24 | PI18 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI1_MOSI | 2 | | I/O | | | | |
| | | UART2_TX | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT30 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T22 | PI19 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI1_MISO | 2 | | I/O | | | | |
| | | UART2_RX | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | EINT31 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T21 | PI20 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | PS2_SCK0 | 2 | | I/O | | | | |
| | | UART7_TX | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PWM2 | 6 | | I/O | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R23 | PI21 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | PS2_SDA0 | 2 | | I/O | | | | |
| | | UART7_RX | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PWM3 | 6 | | I/O | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| **System** | | | | | | | | | |
| C20 | NMI | NMI | NA | NA | I | Z | PU/PD | NA | VCC-RTC |
| R24 | RESET | RESET | NA | NA | I | Z | PU/PD | NA | VCC-IO |
| U12 | TEST | TEST | NA | NA | I | PD | PU/PD | NA | VCC-PF |
| L7 | FEL | FEL | NA | NA | I | PU | PU/PD | NA | VCC-PD |
| K7 | JTAG-SEL | JTAG-SEL | NA | NA | I | PU | PU/PD | NA | VCC-PD |
| **ADC** | | | | | | | | | |
| AD3 | KEYADC0 | KEYADC0 | NA | NA | AI | NA | NA | NA | AVCC |
| AA4 | KEYADC1 | KEYADC1 | NA | NA | AI | NA | NA | NA | AVCC |
| **TV-OUT** | | | | | | | | | |
| V1 | TVOUT0 | TVOUT0 | NA | NA | AO | NA | NA | NA | VCC-TVOUT |
| V2 | TVOUT1 | TVOUT1 | NA | NA | AO | NA | NA | NA | VCC-TVOUT |
| V3 | TVOUT2 | TVOUT2 | NA | NA | AO | NA | NA | NA | VCC-TVOUT |
| V4 | TVOUT3 | TVOUT3 | NA | NA | AO | NA | NA | NA | VCC-TVOUT |
| P8 | VCC-TVOUT | VCC-TVOUT | NA | NA | P | NA | NA | NA | NA |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| N9 | GND-TVOUT | GND-TVOUT | NA | NA | G | NA | NA | NA | NA |
| **TV-IN** | | | | | | | | | |
| W2 | TVIN0 | TVIN0 | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| Y1 | TVIN1 | TVIN1 | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| Y2 | TVIN2 | TVIN2 | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| W3 | TVIN3 | TVIN3 | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| P7 | VCC-TVIN | VCC-TVIN | NA | NA | P | NA | NA | NA | NA |
| T10 | VRP-TVIN | VRP-TVIN | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| U10 | VRN-TVIN | VRN-TVIN | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| **SATA** | | | | | | | | | |
| AA9 | SATA-TXP | SATA-TXP | NA | NA | AO | NA | NA | NA | VDD25-SATA |
| AB9 | SATA-TXM | SATA-TXM | NA | NA | AO | NA | NA | NA | VDD25-SATA |
| AA8 | SATA-RXP | SATA-RXP | NA | NA | AI | NA | NA | NA | VDD25-SATA |
| AB8 | SATA-RXM | SATA-RXM | NA | NA | AI | NA | NA | NA | VDD25-SATA |
| W10 | REXT-SATA | REXT-SATA | NA | NA | AO | NA | NA | NA | VDD25-SATA |
| AB7 | SATA-CLKP | SATA-CLKP | NA | NA | AI | NA | NA | NA | VDD25-SATA |
| AA7 | SATA-CLKM | SATA-CLKM | NA | NA | AI | NA | NA | NA | VDD25-SATA |
| T9 | VDD-SATA | VDD-SATA | NA | NA | P | NA | NA | NA | NA |
| U9 | VDD25-SATA | VDD25-SATA | NA | NA | P | NA | NA | NA | NA |
| **MIPI DSI** | | | | | | | | | |
| L2 | MDSI-CKN | MDSI-CKN | NA | NA | AO | NA | NA | NA | VCC-DSI |
| L1 | MDSI-CKP | MDSI-CKP | NA | NA | AO | NA | NA | NA | VCC-DSI |
| J2 | MDSI-D0N | MDSI-D0N | NA | NA | A I/O | NA | NA | NA | VCC-DSI |
| J1 | MDSI-D0P | MDSI-D0P | NA | NA | A I/O | NA | NA | NA | VCC-DSI |
| K2 | MDSI-D1N | MDSI-D1N | NA | NA | AO | NA | NA | NA | VCC-DSI |
| K1 | MDSI-D1P | MDSI-D1P | NA | NA | AO | NA | NA | NA | VCC-DSI |
| J4 | MDSI-D2N | MDSI-D2N | NA | NA | AO | NA | NA | NA | VCC-DSI |
| J3 | MDSI-D2P | MDSI-D2P | NA | NA | AO | NA | NA | NA | VCC-DSI |
| K4 | MDSI-D3N | MDSI-D3N | NA | NA | AO | NA | NA | NA | VCC-DSI |
| K3 | MDSI-D3P | MDSI-D3P | NA | NA | AO | NA | NA | NA | VCC-DSI |
| L8 | VCC-DSI | VCC-DSI | NA | NA | P | NA | NA | NA | NA |
| **TP** | | | | | | | | | |
| AA6 | TPX1 | TPX1 | NA | NA | AI | NA | NA | NA | AVCC |
| AB6 | TPX2 | TPX2 | NA | NA | AI | NA | NA | NA | AVCC |
| AB5 | TPY1 | TPY1 | NA | NA | AI | NA | NA | NA | AVCC |
| AB4 | TPY2 | TPY2 | NA | NA | AI | NA | NA | NA | AVCC |
| **USB** | | | | | | | | | |
| AC8 | USB0-DM | USB0-DM | NA | NA | A I/O | NA | NA | NA | VCC-USB |
| AD8 | USB0-DP | USB0-DP | NA | NA | A I/O | NA | NA | NA | VCC-USB |
| AC9 | USB1-DM | USB1-DM | NA | NA | A I/O | NA | NA | NA | VCC-USB |
| AD9 | USB1-DP | USB1-DP | NA | NA | A I/O | NA | NA | NA | VCC-USB |
| AA10 | USB2-DM | USB2-DM | NA | NA | A I/O | NA | NA | NA | VCC-USB |
| AB10 | USB2-DP | USB2-DP | NA | NA | A I/O | NA | NA | NA | VCC-USB |
| T11 | VCC-USB | VCC-USB | NA | NA | P | NA | NA | NA | NA |
| **Audio Codec** | | | | | | | | | |
| V5 | PHONEOUTN | PHONEOUTN | NA | NA | AO | NA | NA | NA | AVCC |
| V6 | PHONEOUTP | PHONEOUTP | NA | NA | AO | NA | NA | NA | AVCC |
| AC2 | FMINR | FMINR | NA | NA | AI | NA | NA | NA | AVCC |
| AC1 | FMINL | FMINL | NA | NA | AI | NA | NA | NA | AVCC |
| AC3 | VMIC | VMIC | NA | NA | AO | NA | NA | NA | AVCC |
| AB3 | MICIN1 | MICIN1 | NA | NA | AI | NA | NA | NA | AVCC |
| AD2 | MICIN2 | MICIN2 | NA | NA | AI | NA | NA | NA | AVCC |
| R8 | VRA1 | VRA1 | NA | NA | AO | NA | NA | NA | AVCC |
| T7 | VRA2 | VRA2 | NA | NA | AO | NA | NA | NA | AVCC |
| T8 | VRP | VRP | NA | NA | AO | NA | NA | NA | AVCC |
| R7 | AVCC | AVCC | NA | NA | P | NA | NA | NA | NA |
| AB2 | LINEINR | LINEINR | NA | NA | AI | NA | NA | NA | AVCC |
| AA3 | LINEINL | LINEINL | NA | NA | AI | NA | NA | NA | AVCC |
| V7 | AGND | AGND | NA | NA | G | NA | NA | NA | NA |
| AA1 | HPOUTR | HPOUTR | NA | NA | AO | NA | NA | NA | VCC-HP |
| AA2 | HPOUTL | HPOUTL | NA | NA | AO | NA | NA | NA | VCC-HP |
| V8 | GND-HP | GND-HP | NA | NA | G | NA | NA | NA | NA |
| Y3 | HPCOM | HPCOM | NA | NA | AO | NA | NA | NA | AVCC |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| W4 | HPCOMFB | HPCOMFB | NA | NA | AI | NA | NA | NA | AVCC |
| W8 | HPBP | HPBP | NA | NA | AO | NA | NA | NA | VCC-HP |
| R9 | VCC-HP | VCC-HP | NA | NA | P | NA | NA | NA | NA |
| **Clock** | | | | | | | | | |
| A20 | X32KIN | X32KIN | NA | NA | AI | NA | NA | NA | VCC-RTC |
| B20 | X32KOUT | X32KOUT | NA | NA | AO | NA | NA | NA | VCC-RTC |
| H17 | VCC-RTC | VCC-RTC | NA | NA | P | NA | NA | NA | NA |
| AD11 | X24MIN | X24MIN | NA | NA | AI | NA | NA | NA | VCC-PLL |
| AC11 | X24MOUT | X24MOUT | NA | NA | AO | NA | NA | NA | VCC-PLL |
| T13 | VCC-PLL | VCC-PLL | NA | NA | P | NA | NA | NA | NA |
| **Efuse** | | | | | | | | | |
| M8 | VDD-EFUSE | VDD-EFUSE | NA | NA | P | NA | NA | NA | NA |
| M7 | VDD-EFUSEBP | VDD-EFUSEBP | NA | NA | O | NA | NA | NA | NA |
| **NC** | | | | | | | | | |
| AD5 | NC0 | NC0 | NA | NA | NA | NA | NA | NA | NA |
| AC5 | NC1 | NC1 | NA | NA | NA | NA | NA | NA | NA |
| AD6 | NC2 | NC2 | NA | NA | NA | NA | NA | NA | NA |
| AC6 | NC3 | NC3 | NA | NA | NA | NA | NA | NA | NA |
| AD7 | NC4 | NC4 | NA | NA | NA | NA | NA | NA | NA |
| AC7 | NC5 | NC5 | NA | NA | NA | NA | NA | NA | NA |
| AD4 | NC6 | NC6 | NA | NA | NA | NA | NA | NA | NA |
| AC4 | NC7 | NC7 | NA | NA | NA | NA | NA | NA | NA |
| V9 | NC8 | NC8 | NA | NA | NA | NA | NA | NA | NA |
| W9 | NC9 | NC9 | NA | NA | NA | NA | NA | NA | NA |
| V10 | NC10 | NC10 | NA | NA | NA | NA | NA | NA | NA |
| U11 | NC11 | NC11 | NA | NA | NA | NA | NA | NA | NA |
| **Power** | | | | | | | | | |
| N17 | VDD-CPUFB | VDD-CPUFB | NA | NA | O | NA | NA | NA | NA |
| J15,J16,J17,K16,K17,L16 | VCC-IO | VCC-IO | NA | NA | P | NA | NA | NA | NA |
| N14,N15,N16,P15,P16,P17,R15,R16 | VDD-CPU | VDD-CPU | NA | NA | P | NA | NA | NA | NA |
| M11,M12,N11,N12,P12,R13 | VDD-SYS | VDD-SYS | NA | NA | P | NA | NA | NA | NA |
| U8 | VCC33 | VCC33 | NA | NA | P | NA | NA | NA | NA |
| **Ground** | | | | | | | | | |
| A1,A24,AB14,AD1,AD24,B12,B8,C10,C15,C17,C4,D7,E10,E13,E16,E3,F10,F11,F12,F14,F17,F5,F7,F8,F9,G10,G13,G7,G8,G9,H11,H14,H15,H16,H2,H4,H6,H8,H9,J10,J11,J12,J13,J14,J7,J9,K10,K11,K12,K13,K14,K15,K8,K9,L10,L11,L12,L13,L14,L15,L9,M10,M13,M14,M15,M16,M17,M9,N10,N13,P9,P10,P11,P13,P14,P18,R10,R11,R12,R14,R17,T16,U13,U14,U16 | GND | GND | NA | NA | G | NA | NA | NA | NA |

(1).NA: No Application.

(2).OFF: Disable IO function of GPIO.

## 4.2. GPIO Multiplex Function

The following table provides a description of the T3 GPIO multiplex function.

**NOTE**

**For each GPIO, Function0 is input function; Function1 is output function.**

**Table 4-2. GPIO Multiplex Function**

| Pin Name | GPIO Group | IO Type | Default Pull-up/ down | Function2 | Function3 | Function4 | Function 5 | Function 6 | Function7 |
|---|---|---|---|---|---|---|---|---|---|
| PA0 | GPIOA | I/O | No Pull | ERXD3 | SPI1_CS0 | UART2_RTS | RGMII_RXD3/ RMII_NULL/ MII_RXD3 | - | - |
| PA1 | | I/O | No Pull | ERXD2 | SPI1_CLK | UART2_CTS | RGMII_RXD2/ RMII_NULL/ MII_RXD2 | - | - |
| PA2 | | I/O | No Pull | ERXD1 | SPI1_MOSI | UART2_TX | RGMII_RXD1/ RMII_RXD1/ MII_RXD1 | - | - |
| PA3 | | I/O | No Pull | ERXD0 | SPI1_MISO | UART2_RX | RGMII_RXD0/ RMII_RXD0/ MII_RXD0 | - | - |
| PA4 | | I/O | No Pull | ETXD3 | SPI1_CS1 | - | RGMII_TXD3/ RMII_NULL/ MII_TXD3 | - | - |
| PA5 | | I/O | No Pull | ETXD2 | SPI3_CS0 | - | RGMII_TXD2/ RMII_NULL/ MII_TXD2 | - | - |
| PA6 | | I/O | No Pull | ETXD1 | SPI3_CLK | - | RGMII_TXD1/ RMII_TXD1/ MII_TXD1 | - | - |
| PA7 | | I/O | No Pull | ETXD0 | SPI3_MOSI | - | RGMII_TXD0/ RMII_TXD0/ MII_TXD0 | - | - |
| PA8 | | I/O | No Pull | ERXCK | SPI3_MISO | - | RGMII_RXCK/ RMII_RXER/ MII_RXCK | - | - |
| PA9 | | I/O | No Pull | ERXERR | SPI3_CS1 | - | RGMII_NULL/ RMII_NULL/ MII_RXER | I2S1_MCLK | - |
| PA10 | | I/O | No Pull | ERXDV | - | UART1_TX | RGMII_RXCTL/ RMII_CRS_DV/ MII_RXDV | - | - |
| PA11 | | I/O | No Pull | EMDC | - | UART1_RX | MDC | - | - |
| PA12 | | I/O | No Pull | EMDIO | UART6_TX | UART1_RTS | MDIO | - | - |
| PA13 | | I/O | No Pull | ETXEN | UART6_RX | UART1_CTS | RGMII_TXCTL/ RMII_TXEN/ MII_TXEN | - | - |
| PA14 | | I/O | No Pull | ETXCK | UART7_TX | UART1_DTR | RGMII_NULL/ RMII_TXCK/ MII_TXCK | I2S1_BCLK | - |
| PA15 | | I/O | No Pull | ECRS | UART7_RX | UART1_DSR | RGMII_TXCK/ RMII_NULL/ MII_CRS | I2S1_LRCK | - |
| PA16 | | I/O | No Pull | ECOL | - | UART1_DCD | RGMII_CLKIN/ RMII_NULL/ MII_COL | I2S1_DO | - |
| PA17 | | I/O | No Pull | ETXERR | - | UART1_RING | RGMII_NULL/ RMII_NULL/ | I2S1_DI | - |

| Pin Name | GPIO Group | IO Type | Default Pull-up/ down | Function2 | Function3 | Function4 | Function 5 | Function 6 | Function7 |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | MII_TXER | | |
| PB0 | GPIOB | I/O | No Pull | TWI0_SCK | PLL_LOCK_DBG | - | - | - | - |
| PB1 | | I/O | No Pull | TWI0_SDA | - | - | - | - | - |
| PB2 | | I/O | No Pull | - | PWM0 | - | - | - | - |
| PB3 | | I/O | No Pull | - | PWM1 | OWA_MCLK | - | - | - |
| PB4 | | I/O | No Pull | CIR0_RX | - | - | - | - | - |
| PB5 | | I/O | No Pull | I2S_MCLK | AC97_MCLK | - | - | - | - |
| PB6 | | I/O | No Pull | I2S_BCLK | AC97_BCLK | - | - | - | - |
| PB7 | | I/O | No Pull | I2S_LRCK | AC97_SYNC | - | - | - | - |
| PB8 | | I/O | No Pull | I2S_DO0 | AC97_DO | - | - | - | - |
| PB9 | | I/O | No Pull | I2S_DO1 | - | PWM6 | - | - | - |
| PB10 | | I/O | No Pull | I2S_DO2 | - | PWM7 | - | - | - |
| PB11 | | I/O | No Pull | I2S_DO3 | - | - | - | - | - |
| PB12 | | I/O | No Pull | I2S_DI | AC97_DI | - | - | - | - |
| PB13 | | I/O | No Pull | SPI2_CS1 | - | OWA_DO | - | - | - |
| PB14 | | I/O | No Pull | SPI2_CS0 | JTAG_MS0 | - | - | - | - |
| PB15 | | I/O | No Pull | SPI2_CLK | JTAG_CK0 | - | - | - | - |
| PB16 | | I/O | No Pull | SPI2_MOSI | JTAG_DO0 | - | - | - | - |
| PB17 | | I/O | No Pull | SPI2_MISO | JTAG_DI0 | - | - | - | - |
| PB18 | | I/O | No Pull | TWI1_SCK | - | - | - | - | - |
| PB19 | | I/O | No Pull | TWI1_SDA | - | - | - | - | - |
| PB20 | | I/O | No Pull | TWI2_SCK | - | PWM4 | - | - | - |
| PB21 | | I/O | No Pull | TWI2_SDA | - | PWM5 | - | - | - |
| PB22 | | I/O | No Pull | UART0_TX | - | - | - | - | - |
| PB23 | | I/O | No Pull | UART0_RX | CIR1_RX | - | - | - | - |
| PC0 | GPIOC | I/O | No Pull | NWE | SPI0_MOSI | - | - | - | - |
| PC1 | | I/O | No Pull | NALE | SPI0_MISO | - | - | - | - |
| PC2 | | I/O | No Pull | NCLE | SPI0_CLK | - | - | - | - |
| PC3 | | I/O | PU | NCE1 | - | - | - | - | - |
| PC4 | | I/O | PU | NCE0 | - | - | - | - | - |
| PC5 | | I/O | No Pull | NRE | SDC2_DS | - | - | - | - |
| PC6 | | I/O | PU | NRB0 | SDC2_CMD | - | - | - | - |
| PC7 | | I/O | PU | NRB1 | SDC2_CLK | - | - | - | - |
| PC8 | | I/O | No Pull | NDQ0 | SDC2_D0 | - | - | - | - |
| PC9 | | I/O | No Pull | NDQ1 | SDC2_D1 | - | - | - | - |
| PC10 | | I/O | No Pull | NDQ2 | SDC2_D2 | - | - | - | - |
| PC11 | | I/O | No Pull | NDQ3 | SDC2_D3 | - | - | - | - |
| PC12 | | I/O | No Pull | NDQ4 | SDC2_D4 | - | - | - | - |
| PC13 | | I/O | No Pull | NDQ5 | SDC2_D5 | - | - | - | - |
| PC14 | | I/O | No Pull | NDQ6 | SDC2_D6 | - | - | - | - |
| PC15 | | I/O | No Pull | NDQ7 | SDC2_D7 | - | - | - | - |
| PC16 | | I/O | PD | NWP | - | - | - | - | - |

| Pin Name | GPIO Group | IO Type | Default Pull-up/ down | Function2 | Function3 | Function4 | Function 5 | Function 6 | Function7 |
|---|---|---|---|---|---|---|---|---|---|
| PC17 | | I/O | PU | NCE2 | - | - | - | - | - |
| PC18 | | I/O | PU | NCE3 | - | - | - | - | - |
| PC19 | | I/O | No Pull | NCE4 | SPI2_CS0 | - | - | - | - |
| PC20 | | I/O | No Pull | NCE5 | SPI2_CLK | - | - | - | - |
| PC21 | | I/O | No Pull | NCE6 | SPI2_MOSI | - | - | - | - |
| PC22 | | I/O | No Pull | NCE7 | SPI2_MISO | - | - | - | - |
| PC23 | | I/O | PU | - | SPI0_CS0 | - | - | - | - |
| PC24 | | I/O | No Pull | NDQS | SDC2_RST | - | - | - | - |
| PD0 | GPIOD | I/O | No Pull | LCD0_D0 | LVDS0_VP0 | - | - | - | - |
| PD1 | | I/O | No Pull | LCD0_D1 | LVDS0_VN0 | - | - | - | - |
| PD2 | | I/O | No Pull | LCD0_D2 | LVDS0_VP1 | - | - | - | - |
| PD3 | | I/O | No Pull | LCD0_D3 | LVDS0_VN1 | - | - | - | - |
| PD4 | | I/O | No Pull | LCD0_D4 | LVDS0_VP2 | - | - | - | - |
| PD5 | | I/O | No Pull | LCD0_D5 | LVDS0_VN2 | - | - | - | - |
| PD6 | | I/O | No Pull | LCD0_D6 | LVDS0_VPC | - | - | - | - |
| PD7 | | I/O | No Pull | LCD0_D7 | LVDS0_VNC | - | - | - | - |
| PD8 | | I/O | No Pull | LCD0_D8 | LVDS0_VP3 | - | - | - | - |
| PD9 | | I/O | No Pull | LCD0_D9 | LVDS0_VN3 | - | - | - | - |
| PD10 | | I/O | No Pull | LCD0_D10 | LVDS1_VP0 | - | - | - | - |
| PD11 | | I/O | No Pull | LCD0_D11 | LVDS1_VN0 | - | - | - | - |
| PD12 | | I/O | No Pull | LCD0_D12 | LVDS1_VP1 | - | - | - | - |
| PD13 | | I/O | No Pull | LCD0_D13 | LVDS1_VN1 | - | - | - | - |
| PD14 | | I/O | No Pull | LCD0_D14 | LVDS1_VP2 | - | - | - | - |
| PD15 | | I/O | No Pull | LCD0_D15 | LVDS1_VN2 | - | - | - | - |
| PD16 | | I/O | No Pull | LCD0_D16 | LVDS1_VPC | - | - | - | - |
| PD17 | | I/O | No Pull | LCD0_D17 | LVDS1_VNC | - | - | - | - |
| PD18 | | I/O | No Pull | LCD0_D18 | LVDS1_VP3 | - | - | - | - |
| PD19 | | I/O | No Pull | LCD0_D19 | LVDS1_VN3 | - | - | - | - |
| PD20 | | I/O | No Pull | LCD0_D20 | CSI1_MCLK | - | - | - | - |
| PD21 | | I/O | No Pull | LCD0_D21 | SMC_VPPEN | - | - | - | - |
| PD22 | | I/O | No Pull | LCD0_D22 | SMC_VPPPP | - | - | - | - |
| PD23 | | I/O | No Pull | LCD0_D23 | SMC_DET | - | - | - | - |
| PD24 | | I/O | No Pull | LCD0_CLK | SMC_VCCEN | - | - | - | - |
| PD25 | | I/O | No Pull | LCD0_DE | SMC_RST | - | - | - | - |
| PD26 | | I/O | No Pull | LCD0_HSYNC | SMC_SLK | - | - | - | - |
| PD27 | | I/O | No Pull | LCD0_VSYNC | SMC_SDA | - | - | - | - |
| PE0 | GPIOE | I/O | No Pull | TS0_CLK | CSI0_PCLK | - | - | - | - |
| PE1 | | I/O | No Pull | TS0_ERR | CSI0_MCLK | - | - | - | - |
| PE2 | | I/O | No Pull | TS0_SYNC | CSI0_HSYNC | - | - | - | - |
| PE3 | | I/O | No Pull | TS0_DVLD | CSI0_VSYNC | - | - | - | - |
| PE4 | | I/O | No Pull | TS0_D0 | CSI0_D0 | - | - | - | - |
| PE5 | | I/O | No Pull | TS0_D1 | CSI0_D1 | - | - | - | - |

| Pin Name | GPIO Group | IO Type | Default Pull-up/ down | Function2 | Function3 | Function4 | Function 5 | Function 6 | Function7 |
|---|---|---|---|---|---|---|---|---|---|
| PE6 | | I/O | No Pull | TS0_D2 | CSI0_D2 | - | - | - | - |
| PE7 | | I/O | No Pull | TS0_D3 | CSI0_D3 | - | - | - | - |
| PE8 | | I/O | No Pull | TS0_D4 | CSI0_D4 | - | - | - | - |
| PE9 | | I/O | No Pull | TS0_D5 | CSI0_D5 | - | - | - | - |
| PE10 | | I/O | No Pull | TS0_D6 | CSI0_D6 | - | - | - | - |
| PE11 | | I/O | No Pull | TS0_D7 | CSI0_D7 | - | - | - | - |
| PF0 | GPIOF | I/O | No Pull | SDC0_D1 | | JTAG_MS1 | - | - | - |
| PF1 | | I/O | No Pull | SDC0_D0 | | JTAG_DI1 | - | - | - |
| PF2 | | I/O | No Pull | SDC0_CLK | | UART0_TX | - | - | - |
| PF3 | | I/O | No Pull | SDC0_CMD | | JTAG_DO1 | - | - | - |
| PF4 | | I/O | No Pull | SDC0_D3 | | UART0_RX | - | - | - |
| PF5 | | I/O | No Pull | SDC0_D2 | | JTAG_CK1 | - | - | - |
| PG0 | GPIOG | I/O | No Pull | TS1_CLK | CSI1_PCLK | SDC1_CMD | - | - | - |
| PG1 | | I/O | No Pull | TS1_ERR | CSI1_MCLK | SDC1_CLK | - | - | - |
| PG2 | | I/O | No Pull | TS1_SYNC | CSI1_HSYNC | SDC1_D0 | - | - | - |
| PG3 | | I/O | No Pull | TS1_DVLD | CSI1_VSYNC | SDC1_D1 | - | - | - |
| PG4 | | I/O | No Pull | TS1_D0 | CSI1_D0 | SDC1_D2 | CSI0_D8 | - | - |
| PG5 | | I/O | No Pull | TS1_D1 | CSI1_D1 | SDC1_D3 | CSI0_D9 | - | - |
| PG6 | | I/O | No Pull | TS1_D2 | CSI1_D2 | UART3_TX | CSI0_D10 | - | - |
| PG7 | | I/O | No Pull | TS1_D3 | CSI1_D3 | UART3_RX | CSI0_D11 | - | - |
| PG8 | | I/O | No Pull | TS1_D4 | CSI1_D4 | UART3_RTS | CSI0_D12 | - | - |
| PG9 | | I/O | No Pull | TS1_D5 | CSI1_D5 | UART3_CTS | CSI0_D13 | BIST_RESULT0 | - |
| PG10 | | I/O | No Pull | TS1_D6 | CSI1_D6 | UART4_TX | CSI0_D14 | BIST_RESULT1 | - |
| PG11 | | I/O | No Pull | TS1_D7 | CSI1_D7 | UART4_RX | CSI0_D15 | - | - |
| PH0 | GPIOH | I/O | No Pull | LCD1_D0 | - | UART3_TX | - | EINT0 | CSI1_D0 |
| PH1 | | I/O | No Pull | LCD1_D1 | - | UART3_RX | - | EINT1 | CSI1_D1 |
| PH2 | | I/O | No Pull | LCD1_D2 | - | UART3_RTS | - | EINT2 | CSI1_D2 |
| PH3 | | I/O | No Pull | LCD1_D3 | - | UART3_CTS | - | EINT3 | CSI1_D3 |
| PH4 | | I/O | No Pull | LCD1_D4 | - | UART4_TX | - | EINT4 | CSI1_D4 |
| PH5 | | I/O | No Pull | LCD1_D5 | - | UART4_RX | - | EINT5 | CSI1_D5 |
| PH6 | | I/O | No Pull | LCD1_D6 | - | UART5_TX | - | EINT6 | CSI1_D6 |
| PH7 | | I/O | No Pull | LCD1_D7 | - | UART5_RX | - | EINT7 | CSI1_D7 |
| PH8 | | I/O | No Pull | LCD1_D8 | ERXD3 | KP_IN0 | - | EINT8 | CSI1_D8 |
| PH9 | | I/O | No Pull | LCD1_D9 | ERXD2 | KP_IN1 | - | EINT9 | CSI1_D9 |
| PH10 | | I/O | No Pull | LCD1_D10 | ERXD1 | KP_IN2 | - | EINT10 | CSI1_D10 |
| PH11 | | I/O | No Pull | LCD1_D11 | ERXD0 | KP_IN3 | - | EINT11 | CSI1_D11 |
| PH12 | | I/O | No Pull | LCD1_D12 | - | PS2_SCK1 | - | EINT12 | CSI1_D12 |
| PH13 | | I/O | No Pull | LCD1_D13 | - | PS2_SDA1 | SMC_RST | EINT13 | CSI1_D13 |
| PH14 | | I/O | No Pull | LCD1_D14 | ETXD3 | KP_IN4 | SMC_VPPEN | EINT14 | CSI1_D14 |
| PH15 | | I/O | No Pull | LCD1_D15 | ETXD2 | KP_IN5 | SMC_VPPPP | EINT15 | CSI1_D15 |
| PH16 | | I/O | No Pull | LCD1_D16 | ETXD1 | KP_IN6 | SMC_DET | EINT16 | CSI1_D16 |
| PH17 | | I/O | No Pull | LCD1_D17 | ETXD0 | KP_IN7 | SMC_VCCEN | EINT17 | CSI1_D17 |

| Pin Name | GPIO Group | IO Type | Default Pull-up/ down | Function2 | Function3 | Function4 | Function 5 | Function 6 | Function7 |
|---|---|---|---|---|---|---|---|---|---|
| PH18 | | I/O | No Pull | LCD1_D18 | ERXCK | KP_OUT0 | SMC_SLK | EINT18 | CSI1_D18 |
| PH19 | | I/O | No Pull | LCD1_D19 | ERXERR | KP_OUT1 | SMC_SDA | EINT19 | CSI1_D19 |
| PH20 | | I/O | No Pull | LCD1_D20 | ERXDV | - | - | EINT20 | CSI1_D20 |
| PH21 | | I/O | No Pull | LCD1_D21 | EMDC | - | - | EINT21 | CSI1_D21 |
| PH22 | | I/O | No Pull | LCD1_D22 | EMDIO | KP_OUT2 | SDC1_CMD | - | CSI1_D22 |
| PH23 | | I/O | No Pull | LCD1_D23 | ETXEN | KP_OUT3 | SDC1_CLK | - | CSI1_D23 |
| PH24 | | I/O | No Pull | LCD1_CLK | ETXCK | KP_OUT4 | SDC1_D0 | - | CSI1_PCLK |
| PH25 | | I/O | No Pull | LCD1_DE | ECRS | KP_OUT5 | SDC1_D1 | - | CSI1_FIELD |
| PH26 | | I/O | No Pull | LCD1_HSYNC | ECOL | KP_OUT6 | SDC1_D2 | - | CSI1_HSYNC |
| PH27 | | I/O | No Pull | LCD1_VSYNC | ETXERR | KP_OUT7 | SDC1_D3 | - | CSI1_VSYNC |
| PI0 | GPIOI | I/O | No Pull | - | TWI3_SCK | - | - | - | - |
| PI1 | | I/O | No Pull | - | TWI3_SDA | - | - | - | - |
| PI2 | | I/O | No Pull | - | TWI4_SCK | - | - | - | - |
| PI3 | | I/O | No Pull | PWM1 | TWI4_SDA | - | - | - | - |
| PI4 | | I/O | No Pull | SDC3_CMD | - | - | - | - | - |
| PI5 | | I/O | No Pull | SDC3_CLK | - | - | - | - | - |
| PI6 | | I/O | No Pull | SDC3_D0 | - | - | - | - | - |
| PI7 | | I/O | No Pull | SDC3_D1 | - | - | - | - | - |
| PI8 | | I/O | No Pull | SDC3_D2 | - | - | - | - | - |
| PI9 | | I/O | No Pull | SDC3_D3 | - | - | - | - | - |
| PI10 | | I/O | No Pull | SPI0_CS0 | UART5_TX | - | - | EINT22 | - |
| PI11 | | I/O | No Pull | SPI0_CLK | UART5_RX | - | - | EINT23 | - |
| PI12 | | I/O | No Pull | SPI0_MOSI | UART6_TX | CLK_OUT_A | - | EINT24 | - |
| PI13 | | I/O | No Pull | SPI0_MISO | UART6_RX | CLK_OUT_B | - | EINT25 | - |
| PI14 | | I/O | No Pull | SPI0_CS1 | PS2_SCK1 | TCLKIN0 | - | EINT26 | - |
| PI15 | | I/O | No Pull | SPI1_CS1 | PS2_SDA1 | TCLKIN1 | - | EINT27 | - |
| PI16 | | I/O | No Pull | SPI1_CS0 | UART2_RTS | - | - | EINT28 | - |
| PI17 | | I/O | No Pull | SPI1_CLK | UART2_CTS | - | - | EINT29 | - |
| PI18 | | I/O | No Pull | SPI1_MOSI | UART2_TX | - | - | EINT30 | - |
| PI19 | | I/O | No Pull | SPI1_MISO | UART2_RX | - | - | EINT31 | - |
| PI20 | | I/O | No Pull | PS2_SCK0 | UART7_TX | - | - | PWM2 | - |
| PI21 | | I/O | No Pull | PS2_SDA0 | UART7_RX | - | - | PWM3 | - |

The RGB output can be multiplexed to BT656 output, so the pin correspondence between LCD0 and BT656 is as follows.

| Pin Name | LCD Pin | BT656 Pin |
|---|---|---|
| PD3 | LCD0_D3 | VD0 |
| PD4 | LCD0_D4 | VD1 |
| PD5 | LCD0_D5 | VD2 |
| PD6 | LCD0_D6 | VD3 |
| PD7 | LCD0_D7 | VD4 |
| PD10 | LCD0_D10 | VD5 |
| PD11 | LCD0_D11 | VD6 |
| PD12 | LCD0_D12 | VD7 |

## 4.3. Signal Descriptions

T3 contains many peripheral interfaces. Many of the interfaces can multiplex up to eight functions. Pin-multiplexing configuration can refer to Table 4-1 and Table 4-2. Table 4-3 shows the detailed function description of every signal based on the different interface.

(1).**Signal Name**: The name of every signal.

(2).**Description**: The detailed function description of every signal.

(3).**Type**: Denotes the signal direction.

I (Input),
O (Output),
I/O (Input / Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),
AO (Analog Output),
A I/O (Analog Input/Output),
P (Power),
G (Ground)

**Table 4-3. Signal Descriptions**

| Pin/Signal Name(1) | Description(2) | Type(3) |
|---|---|---|
| **DRAM** | | |
| SDQ[31:0] | DRAM Bidirectional Data Line to the Memory Device | I/O |
| SDQS[3:0]P | DRAM Active-High Bidirectional Data Strobes to the Memory Device | I/O |
| SDQS[3:0]N | DRAM Active-Low Bidirectional Data Strobes to the Memory Device | I/O |
| SDQM[3:0] | DRAM Data Mask Signal to the Memory Device | O |
| SCKP | DRAM Active-High Clock Signal to the Memory Device | O |
| SCKN | DRAM Active-Low Clock Signal to the Memory Device | O |
| SCKE[1:0] | DRAM Clock Enable Signal to the Memory Device | O |
| SA[15:0] | DRAM Address Signal to the Memory Device | O |
| SBA[2:0] | DRAM Bank Address Signal to the Memory Device | O |
| SWE | DRAM Write Enable Strobe to the Memory Device | O |
| SCAS | DRAM Column Address Strobe to the Memory Device | O |
| SRAS | DRAM Row Address Strobe to the Memory Device | O |
| SCS0 | DRAM Chip Select Signal to the Memory Device | O |
| SODT[1:0] | DRAM On-Die Termination Output Signal | O |
| SZQ | DRAM ZQ Calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer) | AI |
| SRST | DRAM Reset Signal to the Memory Device | O |
| SVREF | DRAM Reference Power | P |
| VCC-DRAM | DRAM Power Supply | P |
| **System Control** | | |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| FEL | Boot Mode Select | I |
| JTAG-SEL | JTAG Mode Select | I |
| TEST | Test Signal | I |
| NMI | Non-Maskable Interrupt | I |
| RESET | Reset Signal | I |
| **Interrupt** | | |
| EINT[31:0] | External Interrupt Input | I |
| **JTAG** | | |
| JTAG_DO[1:0] | JTAG Data Output | O |
| JTAG_DI[1:0] | JTAG Data Input | I |
| JTAG_MS[1:0] | JTAG Mode Select Input | I |
| JTAG_CK[1:0] | JTAG Clock Input | I |
| **PWM** | | |
| PWM[7:0] | Pulse Width Modulation Channel | I/O |
| **CLOCK** | | |
| X32KIN | Clock Input of 32768Hz Crystal | AI |
| X32KOUT | Clock Output of 32768Hz Crystal | AO |
| VCC-RTC | RTC Power Supply | P |
| X24MIN | Clock Input of 24MHz Crystal | AI |
| X24MOUT | Clock Output of 24MHz Crystal | AO |
| VCC-PLL | PLL Power | P |
| **NAND FLASH** | | |
| NDQ[7:0] | Nand Flash Data Bit | I/O |
| NCE[7:0] | Nand Flash Chip Select | O |
| NWE | Nand Flash Write Enable | O |
| NALE | Nand Flash Address Latch Enable | O |
| NCLE | Nand Flash Command Latch Enable | O |
| NRE | Nand Flash Read Enable | O |
| NRB[1:0] | Nand Flash Ready/Busy Status Indicator Signal | I |
| NWP | Nand Flash Write Protection | O |
| NDQS | Nand Flash Data Strobe | I/O |
| **LCD(x=[1:0])** | | |
| LCDx_D[23:0] | LCD Data Bit | O |
| LCDx_CLK | LCD Clock Signal | O |
| LCDx_DE | LCD Data Enable | O |
| LCDx_HSYNC | LCD Horizontal Sync | O |
| LCDx_VSYNC | LCD Vertical Sync | O |
| **LVDSx(x=1:0)** | | |
| LVDSx_VP[3:0] | LVDSx Data Positive Signal Output | O |
| LVDSx_VN[3:0] | LVDSx Data Negative Signal Output | O |
| LVDSx_VPC | LVDSx Clock Positive Output | O |
| LVDSx_VNC | LVDSx Clock Negative Output | O |
| **MIPI DSI** | | |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| MDSI-CKN | MIPI DSI Differential Clock Negative | AO |
| MDSI-CKP | MIPI DSI Differential Clock Positive | AO |
| MDSI-D0N | MIPI DSI Differential Data0 Negative | A I/O |
| MDSI-D0P | MIPI DSI Differential Data0 Positive | A I/O |
| MDSI-D1N | MIPI DSI Differential Data1 Negative | AO |
| MDSI-D1P | MIPI DSI Differential Data1 Positive | AO |
| MDSI-D2N | MIPI DSI Differential Data2 Negative | AO |
| MDSI-D2P | MIPI DSI Differential Data2 Positive | AO |
| MDSI-D3N | MIPI DSI Differential Data3 Negative | AO |
| MDSI-D3P | MIPI DSI Differential Data3 Positive | AO |
| VCC-DSI | MIPI DSI Power Supply | P |
| **TV-OUT** | | |
| TVOUT[3:0] | TV-out Output | AO |
| VCC-TVOUT | TV-out Power Supply | P |
| GND-TVOUT | TV-out Ground | G |
| **CSI(x=[1:0])** | | |
| CSI0_D[15:0] | CSI0 Data Bit | I |
| CSI1_D[23:0] | CSI1 Data Bit | I |
| CSIx_PCLK | CSI Pixel Clock | I |
| CSIx_MCLK | CSI Master Clock | O |
| CSIx_HSYNC | CSI Horizontal Sync | I |
| CSIx_VSYNC | CSI Vertical Sync | I |
| CSI1_FIELD | CSI Field Indicator | I/O |
| **TV-IN** | | |
| TVIN[3:0] | TV-in Input | AI |
| VCC-TVIN | TV-in Power Supply | P |
| VRP-TVIN | TV-in Reference Voltage Positive | AI |
| VRN-TVIN | TV-in Reference Voltage Negative | AI |
| **USB** | | |
| USB0-DM | USB0 D- Signal | A I/O |
| USB0-DP | USB0 D+ Signal | A I/O |
| USB1-DM | USB1 D- Signal | A I/O |
| USB1-DP | USB1 D+ Signal | A I/O |
| USB2-DM | USB2 D- Signal | A I/O |
| USB2-DP | USB2 D+ Signal | A I/O |
| VCC-USB | USB Power Supply | P |
| **RTP** | | |
| TPX[2:1] | Touch Panel X[2:1] Input | AI |
| TPY[2:1] | Touch Panel Y[2:1] Input | AI |
| **Audio Codec** | | |
| PHONEOUTN | Phone Negative Output | AO |
| PHONEOUTP | Phone Positive Output | AO |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| FMINR | FM Right Channel Input | AI |
| FMINL | FM Left Channel Input | AI |
| VMIC | Bias Voltage Output for Main Microphone | AO |
| MICIN[2:1] | Microphone Input | AI |
| VRA1 | Reference Voltage Output | AO |
| VRA2 | Reference Voltage Output | AO |
| AVCC | Analog Power Supply | P |
| VRP | Reference Voltage Output | AO |
| LINEINR | Linein Right Channel Input | AI |
| LINEINL | Linein Left Channel Input | AI |
| AGND | Analog Ground | G |
| HPOUTR | Headphone Right Channel Output | AO |
| HPOUTL | Headphone Left Channel Output | AO |
| HPCOM | Headphone Common Reference Output | AO |
| HPCOMFB | Headphone Common Reference Feedback Input | AI |
| HPBP | Headphone Bypass Output | AO |
| VCC-HP | Headphone Power Supply | P |
| GND-HP | Analog Ground | G |
| **KEYADC** | | |
| KEYADC[1:0] | ADC Input for Key | AI |
| **EMAC** | | |
| ERXD[3:0] | MII Receive Data Bit | I |
| ETXD[3:0] | MII Transmit Data Bit | O |
| ERXCK | MII Receive Clock | I |
| ERXERR | MII Receive Error | I |
| ERXDV | MII Receive Data Valid | I |
| EMDC | MII Management Data Clock | O |
| EMDIO | MII Management Data Input/Output | I/O |
| ETXEN | MII Transmit Enable | O |
| ETXCK | MII Transmit Clock | I |
| ECRS | MII Carrier Sense | I |
| ECOL | MII Collision Detect | I |
| ETXERR | MII Transmit Error | O |
| **GMAC** | | |
| RGMII_RXD3/RMII_NULL/ MII_RXD3 | RGMII Receive Data/MII Receive Data | I |
| RGMII_RXD2/RMII_NULL/ MII_RXD2 | RGMII Receive Data/MII Receive Data | I |
| RGMII_RXD1/RMII_RXD1/ MII_RXD1 | RGMII Receive Data/RMII Receive Data/MII Receive Data | I |
| RGMII_RXD0/RMII_RXD0/ MII_RXD0 | RGMII Receive Data/RMII Receive Data/MII Receive Data | I |
| RGMII_RXCK/RMII_RXER/ MII_RXCK | RGMII Receive Clock/RMII Receive Error/MII Receive Clock | I |
| RGMII_RXCTL/RMII_CRS_DV/ | RGMII Receive Control/RMII Carrier Sense Receive Data | I |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| MII_RXDV | Valid/MII Receive Data Valid | |
| RGMII_RXCK/RMII_RXER/ MII_RXCK | RGMII Receive Clock/RMII Receive Error/MII Receive Clock | I |
| RGMII_TXD3/RMII_NULL/ MII_TXD3 | RGMII Transmit Data/MII Transmit Data | O |
| RGMII_TXD2/RMII_NULL/ MII_TXD2 | RGMII Transmit Data/MII Transmit Data | O |
| RGMII_TXD1/RMII_TXD1/ MII_TXD1 | RGMII Transmit Data/RMII Transmit Data/MII Transmit Data | O |
| RGMII_TXD0/RMII_TXD0/ MII_TXD0 | RGMII Transmit Data/RMII Transmit Data/MII Transmit Data | O |
| RGMII_TXCTL/RMII_TXEN/ MII_TXEN | RGMII Transmit Control/RMII Transmit Enable/MII Transmit Enable | O |
| RGMII_TXCK/RMII_NULL/ MII_CRS | RGMII Transmit Clock/MII Carrier Sense | O, I |
| RGMII_NULL/RMII_TXCK/ MII_TXCK | RMII Transmit Clock/MII Transmit Clock | I |
| RGMII_CLKIN/RMII_NULL/ MII_COL | RGMII Reference Clock Input/MII Collision Detect | I |
| RGMII_NULL/RMII_NULL/ MII_TXER | MII Transmit Error | O |
| MDC | RGMII/MII/RMII Management Data Clock | O |
| MDIO | RGMII/MII/RMII Management Data Input/Output | I/O |
| **SPI(x=[3:0])** | | |
| SPIx_CS[1:0] | SPI Chip Select Signal (active low) | I/O |
| SPIx_CLK | SPI Clock Signal | I/O |
| SPIx_MOSI | SPI Master Data Out, Slave Data In | I/O |
| SPIx_MISO | SPI Master Data In, Slave Data Out | I/O |
| **UART** | | |
| UART0_TX | UART0 Data Transmit | O |
| UART0_RX | UART0 Data Receive | I |
| UART1_TX | UART1 Data Transmit | O |
| UART1_RX | UART1 Data Receive | I |
| UART1_RTS | UART1 Data Request to Send | O |
| UART1_CTS | UART1 Data Clear to Send | I |
| UART1_DTR | UART1 Data Terminal Ready | O |
| UART1_DSR | UART1 Data Set Ready | I |
| UART1_DCD | UART1 Data Carrier Detect | I |
| UART1_RING | UART1 Data Ring Indicator | I |
| UART2_TX | UART2 Data Transmit | O |
| UART2_RX | UART2 Data Receive | I |
| UART2_RTS | UART2 Data Request to Send | O |
| UART2_CTS | UART2 Data Clear to Send | I |
| UART3_TX | UART3 Data Transmit | O |
| UART3_RX | UART3 Data Receive | I |
| UART3_RTS | UART3 Data Request to Send | O |
| UART3_CTS | UART3 Data Clear to Send | I |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| UART4_TX | UART4 Data Transmit | O |
| UART4_RX | UART4 Data Receive | I |
| UART5_TX | UART5 Data Transmit | O |
| UART5_RX | UART5 Data Receive | I |
| UART6_TX | UART6 Data Transmit | O |
| UART6_RX | UART6 Data Receive | I |
| UART7_TX | UART7 Data Transmit | O |
| UART7_RX | UART7 Data Receive | I |
| **TWI(x=[4:0])** | | |
| TWIx_SCK | TWI Clock | I/O |
| TWIx_SDA | TWI Data/Address | I/O |
| **SD/MMC** | | |
| SDC0_D[3:0] | SDC0 Data Bit | I/O |
| SDC0_CLK | SDC0 Clock | O |
| SDC0_CMD | SDC0 Command Signal | I/O |
| SDC1_D[3:0] | SDC1 Data Bit | I/O |
| SDC1_CLK | SDC1 Clock | O |
| SDC1_CMD | SDC1 Command Signal | I/O |
| SDC2_D[7:0] | SDC2 Data Bit | I/O |
| SDC2_CLK | SDC2 Clock | O |
| SDC2_CMD | SDC2 Command Signal | I/O |
| SDC2_DS | SDC2 Data Strobe | I |
| SDC2_RST | SDC2 Reset | O |
| SDC3_D[3:0] | SDC3 Data Bit | I/O |
| SDC3_CLK | SDC3 Clock | O |
| SDC3_CMD | SDC3 Command Signal | I/O |
| **KEYPAD** | | |
| KP_IN[7:0] | Keypad Data Input | I |
| KP_OUT[7:0] | Keypad Data Output | O |
| **CIR(x=[1:0])** | | |
| CIRx_RX | CIR Data Receive | I |
| **PS2** | | |
| PS2_SCK[1:0] | PS2 Clock Signal | I/O |
| PS2_SDA[1:0] | PS2 Data Signal | I/O |
| **I2S** | | |
| I2S_DO[3:0] | I2S Data Output | O |
| I2S_DI | I2S Data Input | I |
| I2S_MCLK | I2S Master Clock | O |
| I2S_BCLK | I2S Bit Clock | I/O |
| I2S_LRCK | I2S Left/Right Channel Select Clock | I/O |
| I2S1_DO | I2S1 Data Output | O |
| I2S1_DI | I2S1 Data Input | I |
| I2S1_BCLK | I2S1 Bit Clock | I/O |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| I2S1_LRCK | I2S1 Left/Right Channel Select Clock | I/O |
| I2S1_MCLK | I2S1 Master Clock | O |
| **AC97** | | |
| AC97_DO | AC97 Data Output | O |
| AC97_DI | AC97 Data Input | I |
| AC97_MCLK | AC97 Master Clock | O |
| AC97_BCLK | AC97 Bit Clock | I |
| AC97_SYNC | AC97 Sync Signal | O |
| **OWA** | | |
| OWA_MCLK | OWA Master Clock | O |
| OWA_DO | OWA Data Output | O |
| **TSC(x=[1:0])** | | |
| TSx_D[7:0] | Transport Stream Data | I |
| TSx_CLK | Transport Stream Clock | I |
| TSx_ERR | Transport Stream Error Indicate | I |
| TSx_SYNC | Transport Stream Sync | I |
| TSx_DVLD | Transport Stream Data Valid | I |
| **SCR** | | |
| SMC_RST | Smart Card Reset | O |
| SMC_VPPEN | Smart Card Program Voltage Enable | O |
| SMC_VPPPP | Smart Card Program Control | O |
| SMC_DET | Smart Card Detect | I |
| SMC_VCCEN | Smart Card Power Enable | O |
| SMC_SLK | Smart Card Clock | O |
| SMC_SDA | Smart Card Data | I/O |
| **SATA** | | |
| SATA-TXP | SATA Positive Data Transmit | AO |
| SATA-TXM | SATA Negative Data Transmit | AO |
| SATA-RXP | SATA Positive Data Receive | AI |
| SATA-RXM | SATA Negative Data Receive | AI |
| REXT-SATA | SATA Reference | AO |
| SATA-CLKP | SATA Positive Clock | AI |
| SATA-CLKM | SATA Negative Clock | AI |
| VDD-SATA | 1.2V SATA Power Supply | P |
| VDD25-SATA | 2.5V SATA Power Supply | P |

# 5. Electrical Characteristics

## 5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings.

**CAUTION**

**Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.**

**Table 5-1. Absolute Maximum Ratings**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| Tstg | Storage Temperature | | -40 | 125 | °C |
| VCC-IO,VCC-PA, VCC-PC,VCC-PD, VCC-PE,VCC-PF, VCC-PG | DC Supply Voltage for I/O | | -0.3 | 3.6 | V |
| AVCC | DC Supply Voltage for Analog Part | | -0.3 | 3.6 | V |
| VCC-DRAM | Power Supply for DRAM | | -0.3 | 1.98 | V |
| VCC-USB | Power Supply for USB | | -0.3 | 3.6 | V |
| VCC-TVOUT | Power Supply for TV-OUT | | -0.3 | 3.6 | V |
| VCC-TVIN | Power Supply for TV-IN | | -0.3 | 3.6 | V |
| VCC-DSI | Power Supply for MIPI DSI | | -0.3 | 3.6 | V |
| VCC-PLL | Power Supply for PLL | | -0.3 | 3.6 | V |
| VCC-RTC | Power Supply for RTC | | -0.3 | 3.6 | V |
| VDD25-SATA | 2.5V Power Supply for SATA | | -0.3 | 3.0 | V |
| VDD-SATA | 1.2V Power Supply for SATA | | -0.3 | 1.4 | V |
| VDD-CPU | Power Supply for CPU | | -0.3 | 1.4 | V |
| VDD-SYS | Power Supply for System | | -0.3 | 1.4 | V |
| $V_{ESD}$ | Electrostatic Discharge | Human Body Model(HBM)(1) | -4000 | 4000 | V |
| | | Charged Device Model(CDM)(2) | -500 | 500 | V |
| $I_{Latch-up}$ | Latch-up I-test performance current-pulse injection on each IO pin(3) | | Pass | | |
| | Latch-up over-voltage performance voltage injection on each IO pin(4) | | Pass | | |

(1). Test method: JEDEC JS-001-2014 (Class-3A). JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2). Test method: JS-002-2014 (Class-C2A). JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

(3). Current test performance: Pins stressed per JEDEC JESD78D (Class I, Level A) and passed with I/O pin injection current as defined in JEDEC. Trigger current: ±400mA.
(4). Over voltage performance: Supplies stressed per JEDEC JESD78D (Class I, Level A) and passed voltage injection as defined in JEDEC. Trigger voltage: each VDD pin, stress at 1.5 x Vdd max.

## 5.2. Recommended Operating Conditions

All T3 modules are used under the operating conditions contained in Table 5-2.

**NOTE**

**Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.**

**Table 5-2. Recommended Operating Conditions**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ta | Ambient Operating Temperature | -40 | - | 85 | ℃ |
| VCC-IO | Digital GPIO Power for 3.3V Voltage | 3.0 | 3.3 | 3.6 | V |
| VCC-PA | Power Supply for GPIO A | 1.62<br>2.25<br>3.0 | 1.8<br>2.5<br>3.3 | 1.98<br>2.75<br>3.6 | V |
| VCC-PC | Power Supply for GPIO C | 1.62<br>3.0 | 1.8<br>3.3 | 1.98<br>3.6 | V |
| VCC-PD | Power Supply for GPIO D | 3.0 | 3.3 | 3.6 | V |
| VCC-PE | Power Supply for GPIO E | 1.62<br>2.52<br>3.0 | 1.8<br>2.8<br>3.3 | 1.98<br>3.08<br>3.6 | V |
| VCC-PF | Power Supply for GPIO F | 3.0 | 3.3 | 3.6 | V |
| VCC-PG | Power Supply for GPIO G | 1.62<br>2.52<br>3.0 | 1.8<br>2.8<br>3.3 | 1.98<br>3.08<br>3.6 | V |
| AVCC | DC Supply Voltage for Analog Part | 2.94 | 3.0 | 3.06 | V |
| VCC-DRAM | Power Supply for DDR2 | 1.7 | 1.8 | 1.9 | V |
| | Power Supply for DDR3 | 1.425 | 1.5 | 1.575 | V |
| | Power Supply for DDR3L | 1.283 | 1.35 | 1.45 | V |
| | Power Supply for LPDDR2 | 1.14 | 1.2 | 1.3 | V |
| | Power Supply for LPDDR3 | 1.14 | 1.2 | 1.3 | V |
| VCC-USB | Power Supply for USB | 3.0 | 3.3 | 3.6 | V |
| VCC-TVOUT | Power Supply for TV-OUT | 3.24 | 3.3 | 3.36 | V |
| VCC-TVIN | Power Supply for TV-IN | 3.24 | 3.3 | 3.36 | V |
| VDD-SATA | 1.2V Power Supply for SATA | 1.0 | 1.1 | 1.2 | V |
| VDD25-SATA | 2.5V Power Supply for SATA | 2.25 | 2.5 | 2.75 | V |
| VDD-EFUSE | Power Supply for eFuse | 3.0 | 3.3 | 3.6 | V |
| VCC-DSI | Power Supply for MIPI DSI | 3.0 | 3.3 | 3.6 | V |
| VCC-HP | Power Supply for Headphone | 3.0 | 3.3 | 3.6 | V |
| VCC-PLL | Power Supply for PLL | 3.0 | - | 3.3 | V |
| VCC-RTC | Power Supply for RTC | 3.0 | - | 3.3 | V |
| VDD-CPU | Power Supply for CPU | 1.0 | 1.1 | 1.3 | V |
| VDD-SYS | Power Supply for System | 1.0 | 1.1 | 1.3 | V |

| | | | | | |
|---|---|---|---|---|---|
| Tj | Junction Temperature Range | -40 | - | 120 | °C |

## 5.3. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of T3.

**Table 5-3. DC Electrical Characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital GPIO | High-Level Input Voltage | $V_{IH}$ | 0.7 * VCC-IO | - | VCC-IO + 0.3 | V |
| | Low-Level Input Voltage | $V_{IL}$ | -0.3 | - | 0.3 * VCC-IO | V |
| | Input Pull-up Resistance | $R_{PU}$ | 50 | 100 | 150 | kΩ |
| | Input Pull-down Resistance | $R_{PD}$ | 50 | 100 | 150 | kΩ |
| | High-Level Input Current | $I_{IH}$ | - | - | 10 | uA |
| | Low-Level Input Current | $I_{IL}$ | - | - | 10 | uA |
| | High-Level Output Voltage | $V_{OH}$ | VCC-IO -0.2 | - | VCC-IO | V |
| | Low-Level Output Voltage | $V_{OL}$ | 0 | - | 0.2 | V |
| | Tri-State Output Leakage Current | $I_{OZ}$ | -10 | - | 10 | uA |
| | Input Capacitance | $C_{IN}$ | - | - | 5 | pF |
| | Output Capacitance | $C_{OUT}$ | - | - | 5 | pF |

## 5.4. SDRAM I/O DC Electrical Characteristics

The SDRAM I/O pads support DDR3, DDR3L, LPDDR2, and LPDDR3 operational modes. The SDRAM Controller (DRAMC) is designed to be compatible with JEDEC-compliant SDRAMs. The DRAMC supports the following memory types:

- DDR3 SDRAM compliant to JESD79-3E DDR3 JEDEC standard release July, 2010
- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- LPDDR3 SDRAM compliant to JESD209-3B LPDDR3 JEDEC standard release August, 2013

**Table 5-4. DC Input Logic Level**

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC input logic high | $V_{IH(DC)}$ | VREF + 100 | - | - | mV |
| DC input logic low | $V_{IL(DC)}$ | - | - | VREF – 100 | mV |
| Input reference voltage | Vref | 0.49 * VDDQ | - | 0.51 * VDDQ | V |
| Input termination resistance(ODT) to $V_{DDQ}/2$ | $R_{TT}$ | 60 | 120 | Open | Ω |

**Table 5-5. Output DC Current Drive**

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output high voltage | $V_{OH}$ | 0.9 * VDDQ | - | V |
| DC output low voltage | $V_{OL}$ | - | 0.1 * VDDQ | V |

## 5.5. SDIO Electrical Parameters

The SDIO electrical parameters are related to different supply voltage.

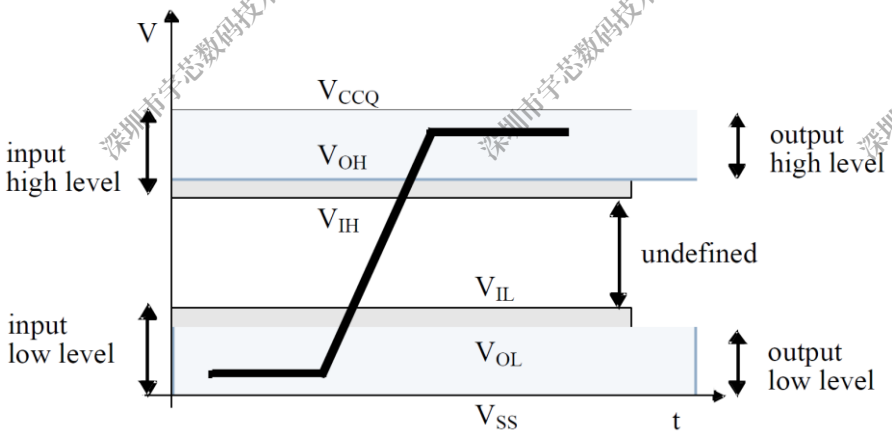



**Figure 5-1. SDIO Voltage Waveform**

Table 5-6 shows 3.3V SDIO electrical parameters..

**Table 5-6. 3.3V SDIO Electrical Parameters**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD | Power voltage | 2.7 | - | 3.6 | V |
| $V_{CCQ}$ | I/O voltage | 2.7 | | 3.6 | V |
| $V_{OH}$ | Output high-level voltage | 0.75 * $V_{CCQ}$ | - | - | V |
| $V_{OL}$ | Output low-level voltage | - | - | 0.125* $V_{CCQ}$ | V |
| $V_{IH}$ | Input high-level voltage | 0.625* $V_{CCQ}$ | - | $V_{CCQ}$ + 0.3 | V |
| $V_{IL}$ | Input low-level voltage | $V_{SS}$ – 0.3 | - | 0.25 * $V_{CCQ}$ | V |

Table 5-7 shows 1.8V SDIO electrical parameters.

**Table 5-7. 1.8V SDIO Electrical Parameters**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD | Power voltage | 2.7 | - | 3.6 | V |
| $V_{CCQ}$ | I/O voltage | 1.7 | | 1.95 | V |
| $V_{OH}$ | Output high-level voltage | $V_{CCQ}$ – 0.45 | - | - | V |
| $V_{OL}$ | Output low-level voltage | - | - | 0.45 | V |
| $V_{IH}$ | Input high-level voltage | 0.625 * $V_{CCQ}$ (1) | - | $V_{CCQ}$ + 0.3 | V |
| $V_{IL}$ | Input low-level voltage | $V_{SS}$ – 0.3 | - | 0.35 * $V_{CCQ}$ (2) | V |
| (1).0.7 * $V_{CCQ}$ for MMC4.3 or lower.<br>(2).0.3 * $V_{CCQ}$ for MMC4.3 or lower. | | | | | |

## 5.6. Audio Codec Electrical Parameters

Table 5-8 shows audio codec electrical parameters.

**Table 5-8. Audio Codec Typical Performance**

| Parameters | Input Conditions | Typ(L/R channel output) | Unit |
|---|---|---|---|
| **DAC To Headphone (32 Ω )** | | | |
| Output Level | 0dB 1kHz Sine | 620 | mVrms |
| SNR(A-weighted) | | 98 | dB |
| THD+N | | -80 | dB |
| **DAC To Headphone (16 Ω )** | | | |
| Output Level | 0dB 1kHz Sine | 530 | mVrms |

| | | | |
|---|---|---|---|
| SNR(A-weighted) | | 97 | dB |
| THD+N | | -79 | dB |
| **DAC To Headphone (No load)** | | | |
| Output Level | 0dB 1kHz Sine | 740 | mVrms |
| SNR(A-weighted) | | 98 | dB |
| THD+N | | -80 | dB |
| **DAC To PHONEOUTDIFF Via Output Mix(No load)** | | | |
| Output Level | 0dB 1kHz Sine | 1.78 | Vrms |
| SNR(A-weighted) | | 100 | dB |
| THD+N | | -80 | dB |
| **DAC To PHONEOUT Via Output Mix(600 Ω )** | | | |
| Output Level | 0dB 1kHz Sine | 1.18 | Vrms |
| SNR(A-weighted) | | 98 | dB |
| THD+N | | -79 | dB |
| **DAC To PHONEOUT Via Output Mix(300 Ω )** | | | |
| Output Level | 0dB 1kHz Sine | 885 | Vrms |
| SNR(A-weighted) | | 98 | dB |
| THD+N | | -77 | dB |
| **LINEIN ADDA To HPOUT Via Output Mix** | | | |
| Output Level | 2.5Vpp | 610 | mVrms |
| SNR(A-weighted) | | 92 | dB |
| THD+N | | -81 | dB |
| **FMIN ADDA To HPOUT Via Output Mix** | | | |
| Output Level | 2.5Vpp | 627 | mVrms |
| SNR(A-weighted) | | 92 | dB |
| THD+N | | -83 | dB |
| **MIC1-ADDA-PHONEONE** | | | |
| Output Level | 2.5Vpp | 756 | mVrms |
| SNR(A-weighted) | | 93 | dB |
| THD+N | | -83 | dB |
| **MIC2-ADDA-PHONEONE** | | | |
| Output Level | 2.5Vpp | 742 | mVrms |
| SNR(A-weighted) | | 90 | dB |
| THD+N | | -82 | dB |
| **DAC To HP (32Ω)(HP Gain 0x3C)** | | | |
| FScale Input Level | 0dB 1kHz Sine | 621 | mVrms |
| SNR(A-weighted) | | 98 | dB |
| THD+N | | -80 | dB |
| **DAC To HP (16Ω)(HP Gain 0x3B)** | | | |
| FScale Input Level | 0dB 1kHz Sine | 529 | mVrms |
| SNR(A-weighted) | | 97 | dB |

| | | | |
|---|---|---|---|
| THD+N | | -79 | dB |

# 5.7. PLL Electrical Characteristics

## 5.7.1. CPU PLL Electrical Parameters

**Table 5-9. CPU PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 60MHz ~2.1GHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 1.5ms |
| Max. Peak-to-Peak Supply Noise | 200ps |

## 5.7.2. Audio PLL Electrical Parameters

**Table 5-10. Audio PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 22.5792MHz,24.576MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 500us |
| Max. Peak-to-Peak Supply Noise | 200ps |

## 5.7.3. GPU PLL Electrical Parameters

**Table 5-11. GPU PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192MHz~600MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 500us |
| Max. Peak-to-Peak Supply Noise | 200ps |

## 5.7.4. Peripheral0/1 PLL Electrical Parameters

**Table 5-12. Peripheral0/1 PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 504MHz ~1.4GHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 500us |
| Max. Peak-to-Peak Supply Noise | 200ps |

### 5.7.5. MIPI PLL Electrical Parameters

**Table 5-13. MIPI PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 182MHz ~1.5GHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 500us |
| Max. Peak-to-Peak Supply Noise | 200ps |

### 5.7.6. DDR0/1 PLL Electrical Parameters

**Table 5-14. DDR0/1 PLL Electrical Parameters**

| Parameter | Value | |
|---|---|---|
| Clock Output Range | 192MHz ~1.6GHz | |
| Reference Clock | 24MHz | |
| Max. Lock Time | 2ms | |
| Max. Peak-to-Peak Supply Noise | 192MHz ~800MHz | 200ps |
| | 800MHz ~1.3GHz | 140ps |
| | 1.3GHz ~1.6GHz | 100ps |

### 5.7.7. Video0/1 PLL Electrical Parameters

**Table 5-15. Video0/1 PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192MHz ~600MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 500us |
| Max. Peak-to-Peak Supply Noise | 200ps |

### 5.7.8. VE PLL Electrical Parameters

**Table 5-16. VE PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192MHz ~600MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 500us |
| Max. Peak-to-Peak Supply Noise | 200ps |

### 5.7.9. DE PLL Electrical Parameters

**Table 5-17. DE PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192MHz ~600MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 500us |
| Max. Peak-to-Peak Supply Noise | 200ps |

### 5.7.10. SATA PLL Electrical Parameters

**Table 5-18. SATA PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 8MHz~300MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 2ms |
| Max. Peak-to-Peak Supply Noise | 140ps |

## 5.8. KEYADC Electrical Characteristics

KEYADC contains two-channels analog-to-digital converter (ADC) for key application. Table 5-19 lists KEYADC electrical characteristics.

**Table 5-19. KEYADC Electrical Characteristics**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| ADC Resolution | - | 6 | - | bits |
| Full-scale Input Range | 0 | - | 0.667*AVCC | V |
| Quantizing Error | - | 2 | - | LSB |
| Clock Frequency | - | - | 250 | Hz |
| Conversion Time | - | 14 | - | ADC Clock Cycles |

## 5.9. Oscillator Electrical Characteristics

T3 contains two external input clocks: X24MIN and X32KIN, two output clocks: X24MOUT and X32KOUT.
The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through X24MIN. Table 5-20 lists the 24MHz crystal specifications.

**Table 5-20. 24MHz Crystal Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $1/(t_{CPMAIN})$ | Crystal Oscillator Frequency Range | – | 24.000 | – | MHz |
| | Frequency Tolerance at 25 °C | -20 | – | +20 | ppm |
| | Oscillation Mode | Fundamental | | | – |

| | | | | | |
|---|---|---|---|---|---|
| | Maximum Change Over Temperature Range | -20 | – | +20 | ppm |
| $C_L$ | Equivalent Load Capacitance | 12 | 18 | 22 | pF |
| $C_O$ | Shunt Capacitance | – | 3 | – | pF |

The 32.768kHz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. The clock is provided through X32KIN. Table 5-21 lists the 32.768kHz crystal specifications.

**Table 5-21. 32.768kHz Crystal Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $1/(t_{CPMAIN})$ | Crystal Oscillator Frequency Range | – | 32.768 | – | kHz |
| | Frequency Tolerance at 25 °C | -20 | – | +20 | ppm |
| | Oscillation Mode | Fundamental | | | – |
| | Maximum Change Over Temperature Range | -20 | – | +20 | ppm |
| $C_L$ | Equivalent Load Capacitance | – | 12.5 | – | pF |
| $C_O$ | Shunt Capacitance | – | 1.1 | – | pF |

## 5.10. Maximum Current Consumption

Table 5-22 lists the peak power consumption of T3.

**Table 5-22. Maximum Current Consumption For Android 7.0**

| Parameter | Sub Parameter | Power Supply | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Internal Core Power | CPU | VDD-CPU | @1.1V | - | - | 2000 | mA |
| | SYS | VDD-SYS | @1.1V | - | - | 2000 | mA |
| GPIO Power | | VCC-IO, VCC-PA, VCC-PC, VCC-PD, VCC-PE, VCC-PF, VCC-PG | @3.3V<br>@2.8V<br>@2.5V<br>@1.8V | - | - | 300 | mA |
| Memory I/O Power | | VCC-DRAM | @1.5V | - | - | 400 | mA |
| Oscillator | | VCC-PLL | @3.0V | - | - | 40 | mA |
| USB 3.0V Power of PHY | | VCC-USB | @3.3V | - | - | 50 | mA |
| RTC Power | | VCC-RTC | @3.0V | - | - | 20 | mA |
| ADC Analog Power | | AVCC | @3.0V | - | - | 20 | mA |
| DAC Analog Power | | AVCC | @3.0V | - | - | | mA |
| PLL Power | | VCC-PLL | @3.0V | - | - | 40 | mA |

The maximum current consumption requirement under Linux is always smaller than the case under Android.

# 5.11. External Memory Electrical Characteristics

## 5.11.1. SDRAM AC Electrical Characteristics

### DDR3/DDR3L Parameters

Figure 5-2 shows the DDR3/DDR3L command and address timing diagram. The timing parameters for this diagram shows in Table 5-23.

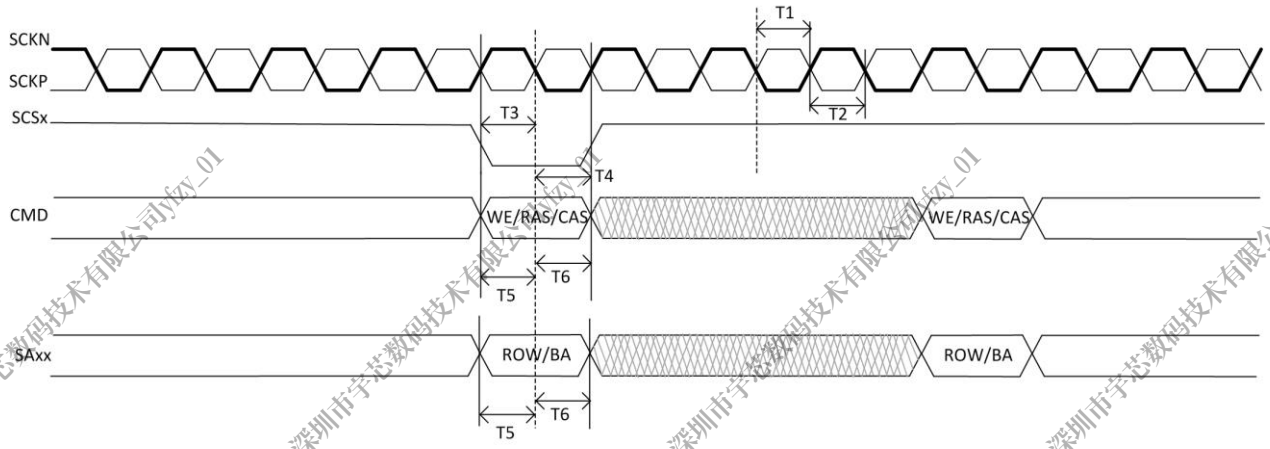



**Figure 5-2. DDR3/DDR3L Command and Address Timing**

**Table 5-23. DDR3/DDR3L Timing Parameters**

| ID | Parameter | Symbol | Clock = 576 MHz | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Suggest | Max | |
| T1 | SCKP clock high-level width | $t_{CH}$ | 0.47 | - | 0.53 | tck |
| T2 | SCKP clock low-level width | $t_{CL}$ | 0.47 | - | 0.53 | tck |
| T3 | CS setup time | $t_{IS}$ | 170 | 295 | - | ps |
| T4 | CS hold time | $t_{IH}$ | 120 | 245 | - | ps |
| T5 | Command and Address setup time to Clock edge | $t_{IS}$ | 170 | 295 | - | ps |
| T6 | Command and Address hold time to Clock edge | $t_{IH}$ | 120 | 245 | - | ps |

T1 and T2 are in reference to Vref level.
T3,T4,T5, and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-3 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram shows in Table 5-24.

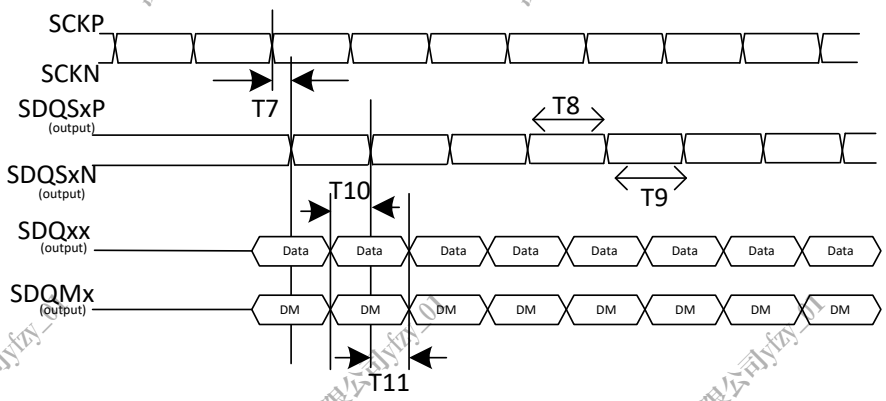



**Figure 5-3. DDR3/DDR3L Write Cycle**

**Table 5-24. DDR3/DDR3L Write Cycle Parameters**

| ID | Parameter | Symbol | Clock = 576 MHz | Unit |
|---|---|---|---|---|

| | | | Min | Suggest | Max | |
|---|---|---|---|---|---|---|
| T7 | SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge | $t_{DQSS}$ | -0.27 | - | 0.27 | $t_{CK}$ |
| T8 | SDQSxP high level width | $t_{DQSH}$ | 0.45 | - | 0.55 | $t_{CK}$ |
| T9 | SDQSxP low level width | $t_{DQSL}$ | 0.45 | - | 0.55 | $t_{CK}$ |
| T10 | Data setup time to SDQSxP/SDQSxN | $t_{DS}$ | 10 | 145 | - | ps |
| T11 | Data hold time to SDQSxP/SDQSxN | $t_{DH}$ | 45 | 180 | - | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T7,T8, and T9 are in reference to Vref level.
T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-4 shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram shows in Table 5-25.

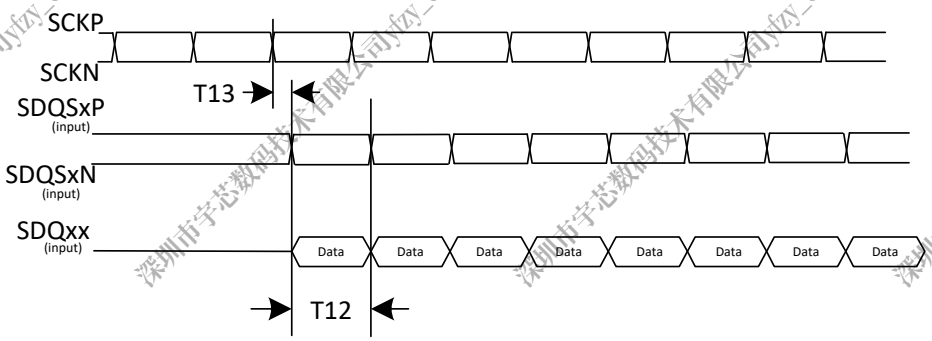



**Figure 5-4. DDR3/DDR3L Read Cycle**

**Table 5-25. DDR3/DDR3L Read Cycle Parameters**

| ID | Parameter | Symbol | Clock = 576 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| T12 | Read Data valid width | $t_{Data}$ | 200 | - | ps |
| T13 | SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge | $t_{DQSCK}$ | -225 | 225 | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T12 and T13 are in reference to Vref level.

**LPDDR3 Parameters**

Figure 5-5 shows the LPDDR3 command and address timing diagram. The timing parameters for this diagram shows in Table 5-26.

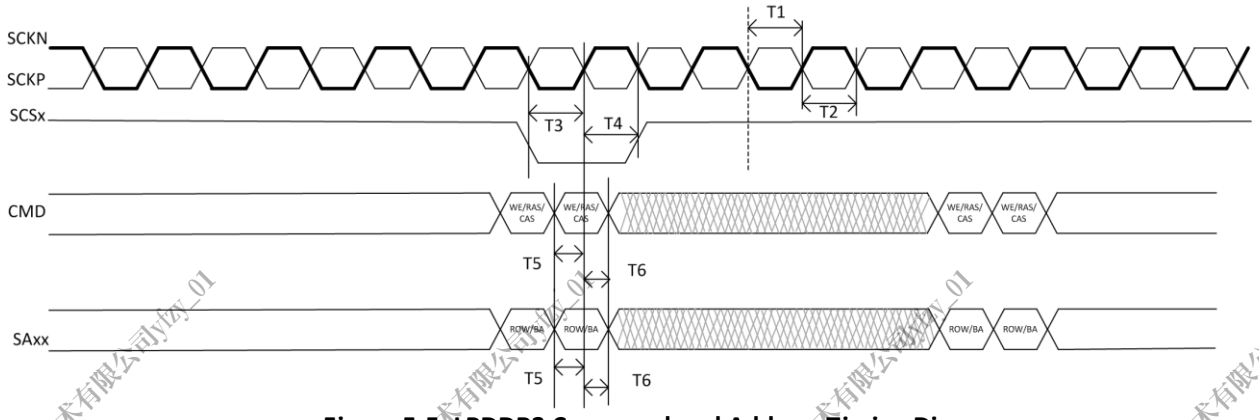



**Figure 5-5. LPDDR3 Command and Address Timing Diagram**

**Table 5-26. LPDDR3 Command and Address Timing Parameters**

| ID | Parameter | Symbol | Clock = 480 MHz | Unit |
|---|---|---|---|---|

| | | | Min | Suggest | Max | |
|---|---|---|---|---|---|---|
| T1 | Clock high pulse width | $t_{CH}$ | 0.45 | - | 0.55 | $t_{CK}$ |
| T2 | Clock low pulse width | $t_{CL}$ | 0.45 | - | 0.55 | $t_{CK}$ |
| T3 | SCSx input setup time | $t_{ISCS}$ | 195 | 347.5 | - | ps |
| T4 | SCSx input hold time | $t_{IHCS}$ | 220 | 372.5 | - | ps |
| T5 | Address and control input setup time | $t_{IAS}$ | 75 | 152.5 | - | ps |
| T6 | Address and control input hold time | $t_{IAH}$ | 100 | 177.5 | - | ps |

T1 and T2 are in reference to Vref level.
T3,T4,T5, and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-6 shows the LPDDR3 write timing diagram. The timing parameters for this diagram shows in Table 5-27.

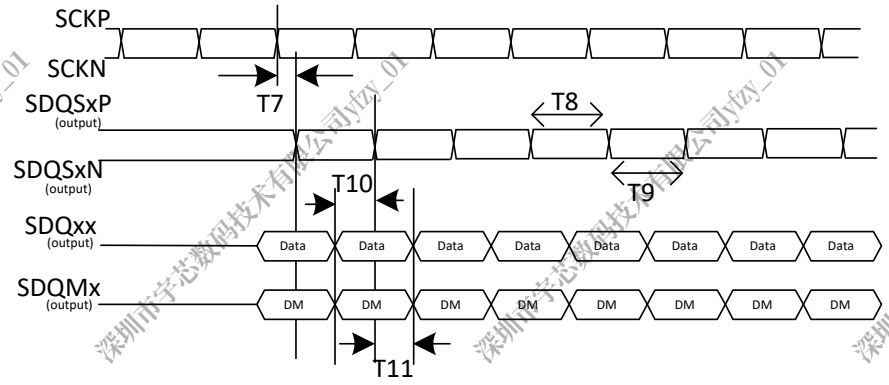



**Figure 5-6. LPDDR3 Write Cycle**

**Table 5-27. LPDDR3 Write Cycle Parameters**

| ID | Parameter | Symbol | Clock = 480 MHz | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Suggest | Max | |
| T7 | SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge | $t_{DQSS}$ | 0.75 | - | 1.25 | $t_{CK}$ |
| T8 | SDQSx input high-level width | $t_{DQSH}$ | 0.4 | - | - | $t_{CK}$ |
| T9 | SDQSx input low-level width | $t_{DQSL}$ | 0.4 | - | - | $t_{CK}$ |
| T10 | SDQxx and SDQMx input setup time | $t_{DS}$ | 75 | 152.5 | - | ps |
| T11 | SDQxx and SDQMx input hold time | $t_{DH}$ | 100 | 177.5 | - | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T7,T8, and T9 are in reference to Vref level.
T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-7 shows the LPDDR3 read timing diagram. The timing parameters for this diagram shows in Table 5-28.

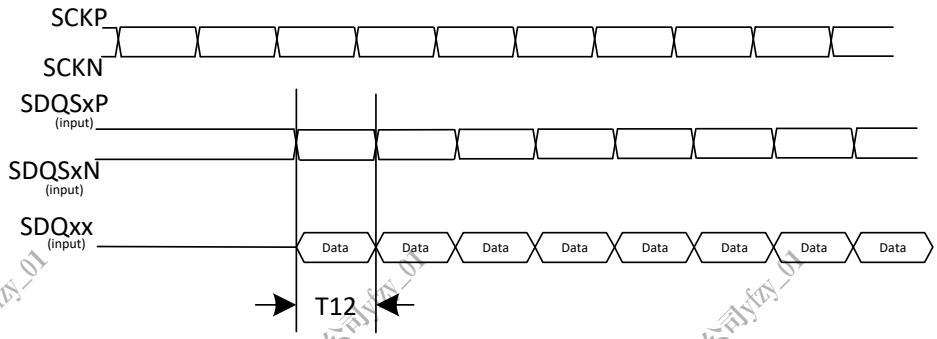



**Figure 5-7. LPDDR3 Read Cycle**

**Table 5-28. LPDDR3 Read Cycle Parameters**

| ID | Parameter | Symbol | Clock = 480 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |

| | | | | | |
|---|---|---|---|---|---|
| T12 | Read Data valid width | $t_{DATA}$ | 200 | - | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T12 is in reference to Vref level.

**LPDDR2 Parameters**

Figure 5-8 shows the LPDDR2 command and address timing diagram. The timing parameters for this diagram shows in Table 5-29.

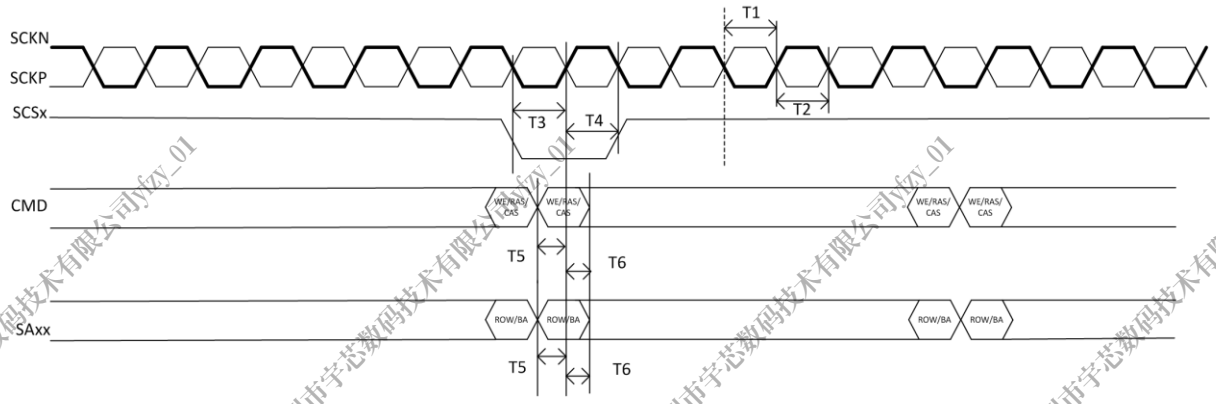



**Figure 5-8. LPDDR2 Command and Address Timing Diagram**

**Table 5-29. LPDDR2 Command and Address Timing Parameters**

| ID | Parameter | Symbol | Clock = 432 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| T1 | Clock high pulse width | $t_{CH}$ | 0.45 | 0.55 | $t_{CK}$ |
| T2 | Clock low pulse width | $t_{CL}$ | 0.45 | 0.55 | $t_{CK}$ |
| T3 | SCSx input setup time | $t_{IS}$ | 220 | - | ps |
| T4 | SCSx input hold time | $t_{IH}$ | 220 | - | ps |
| T5 | Address and control input setup time | $t_{IS}$ | 220 | - | ps |
| T6 | Address and control input hold time | $t_{IH}$ | 220 | - | ps |

All measurements are in reference to Vref level.

Figure 5-9 shows the LPDDR2 write timing diagram. The timing parameters for this diagram shows in Table 5-30.

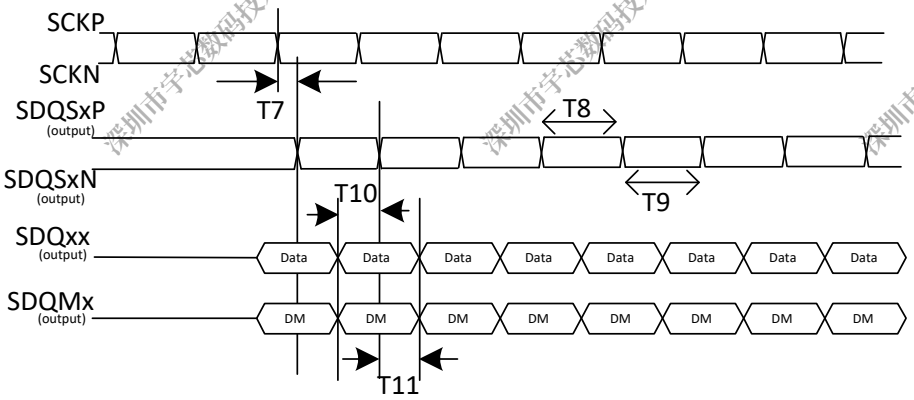



**Figure 5-9. LPDDR2 Write Cycle**

**Table 5-30. LPDDR2 Write Cycle Parameters**

| ID | Parameter | Symbol | Clock = 432 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| T7 | SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge | $t_{DQSS}$ | 0.75 | 1.25 | $t_{CK}$ |
| T8 | SDQSx input high-level width | $t_{DQSH}$ | 0.4 | - | $t_{CK}$ |

| | | | | | |
|---|---|---|---|---|---|
| T9 | SDQSx input low-level width | $t_{DQSL}$ | 0.4 | - | $t_{CK}$ |
| T10 | SDQxx and SDQMx input setup time | $t_{DS}$ | 210 | - | ps |
| T11 | SDQxx and SDQMx input hold time | $t_{DH}$ | 210 | - | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
All measurements are in reference to Vref level.

Figure 5-10 shows the LPDDR2 read timing diagram. The timing parameters for this diagram shows in Table 5-31.

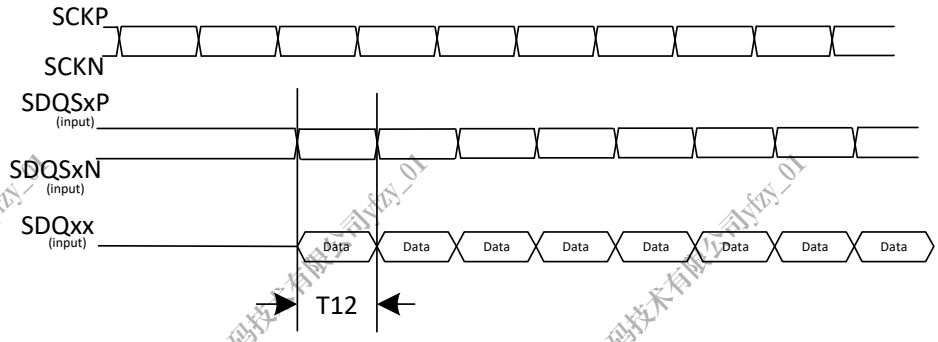



**Figure 5-10. LPDDR2 Read Cycle**

**Table 5-31. LPDDR2 Read Cycle Parameters**

| ID | Parameter | Symbol | Clock = 432 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| T12 | Read Data valid width | $t_{DATA}$ | 300 | - | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T12 is in reference to Vref level.

### 5.11.2. Nand AC Electrical Characteristics

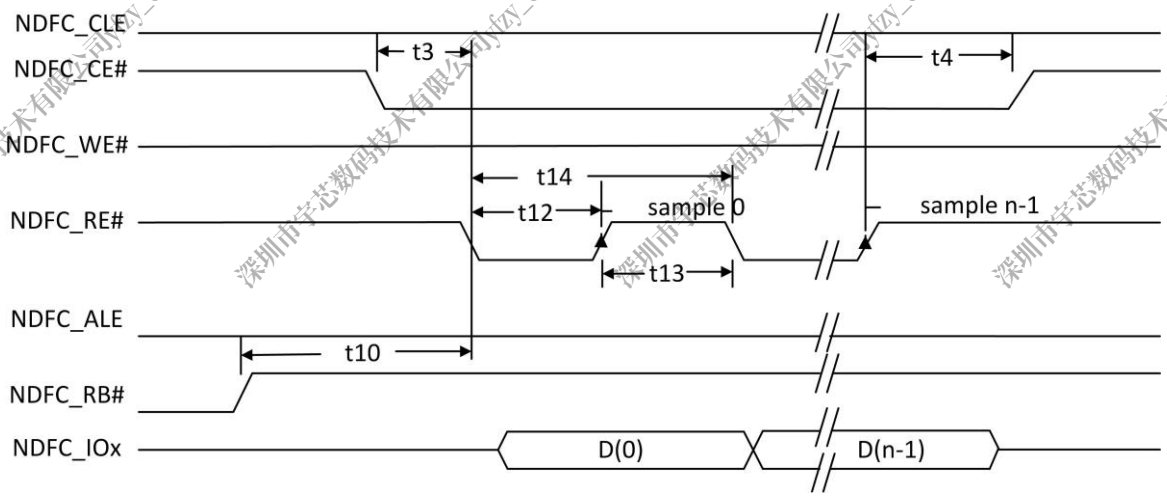



**Figure 5-11. Conventional Serial Access Cycle Timing (SAM0)**

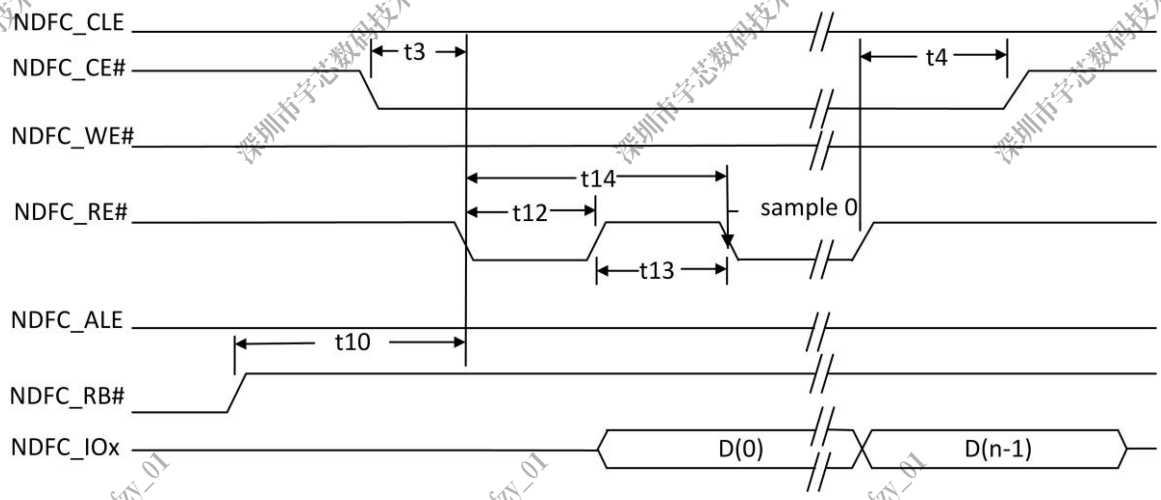



**Figure 5-12. EDO Type Serial Access after Read Cycle Timing (SAM1)**

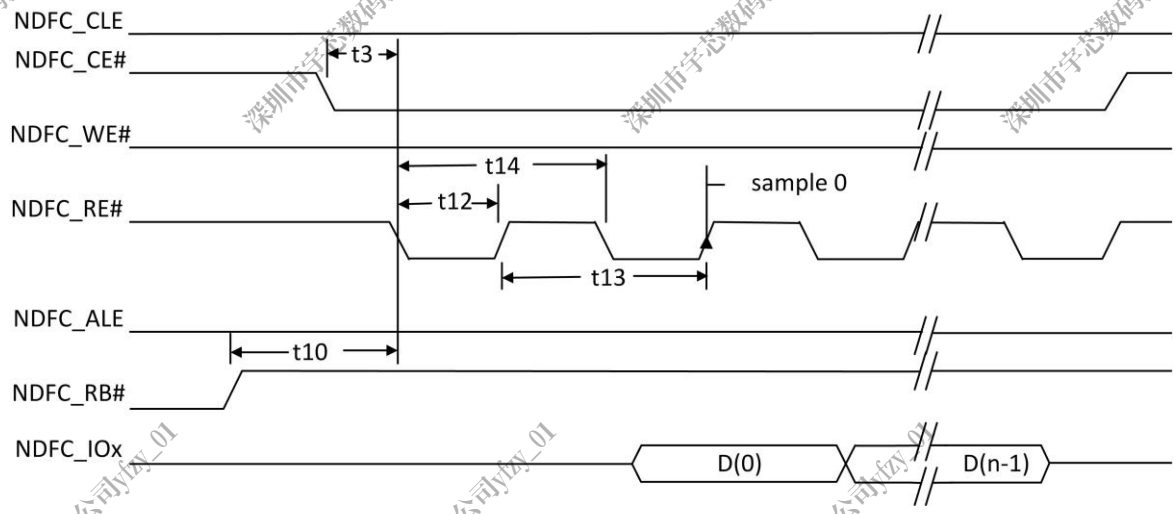



**Figure 5-13. Extending EDO Type Serial Access Mode Timing (SAM2)**

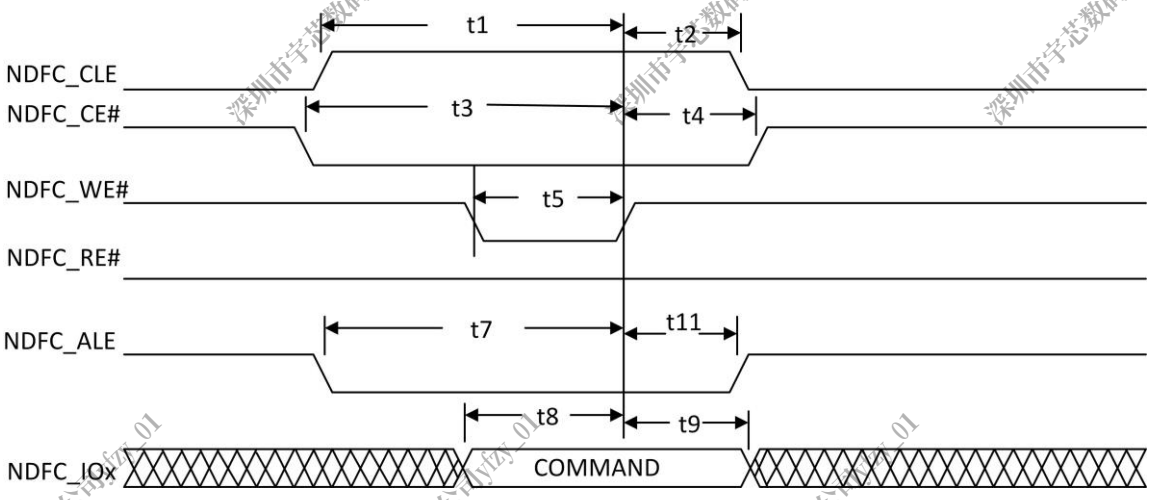



**Figure 5-14. Command Latch Cycle Timing**

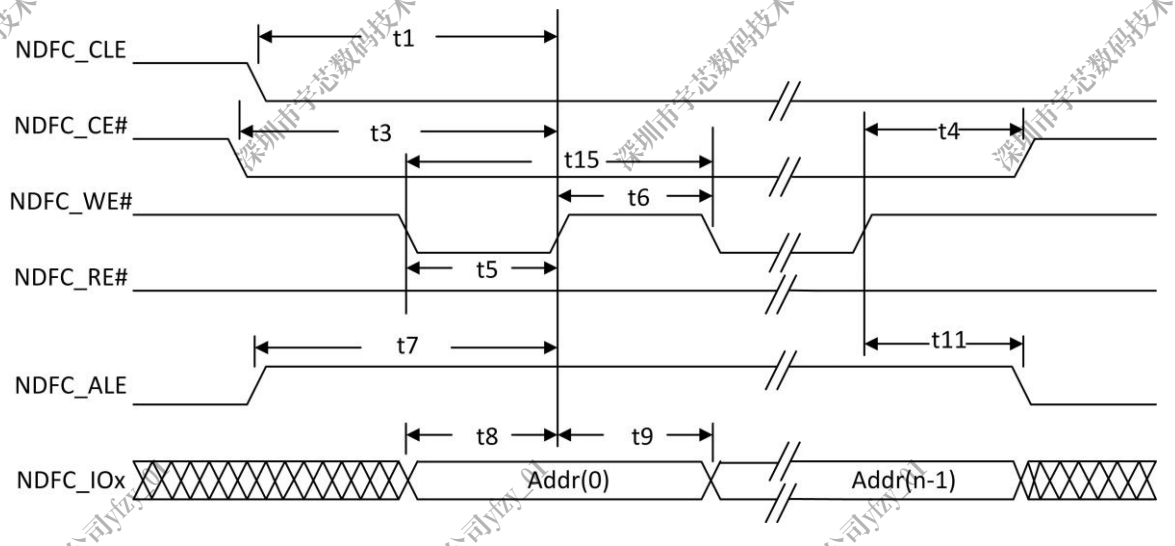



**Figure 5-15. Address Latch Cycle Timing**

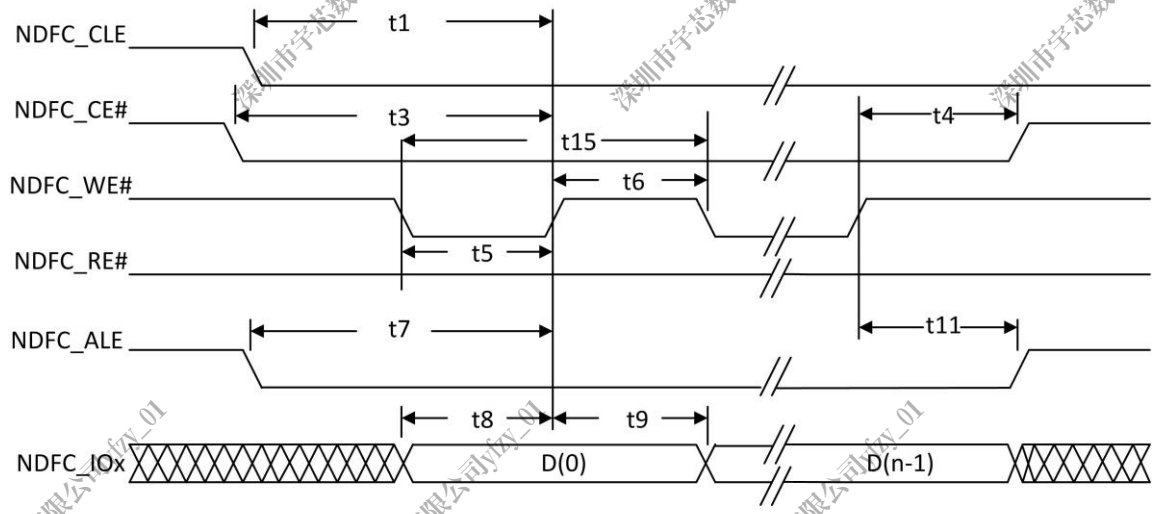



**Figure 5-16. Write Data to Flash Cycle Timing**

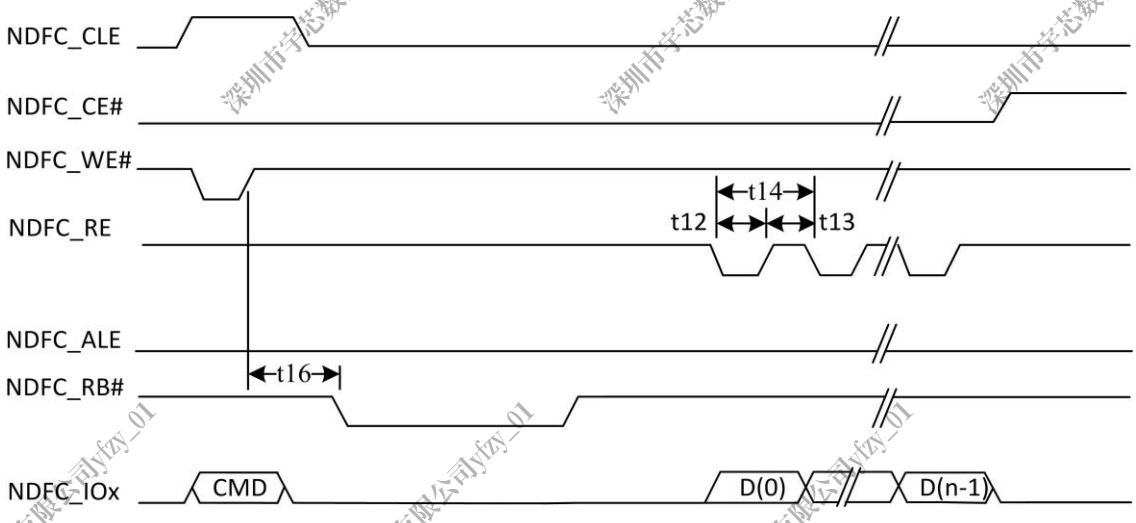



**Figure 5-17. Waiting R/B# Ready Timing**

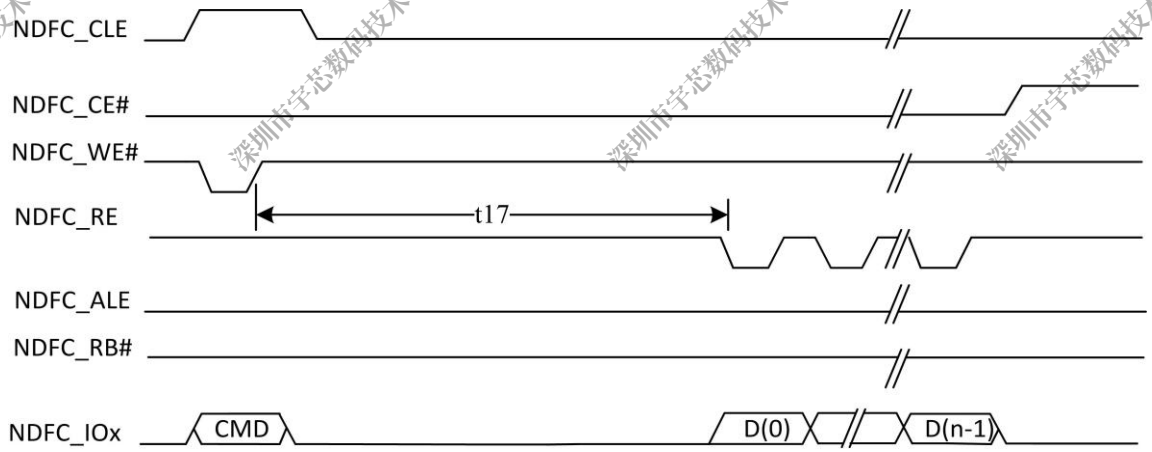



**Figure 5-18. WE# High to RE# Low Timing**

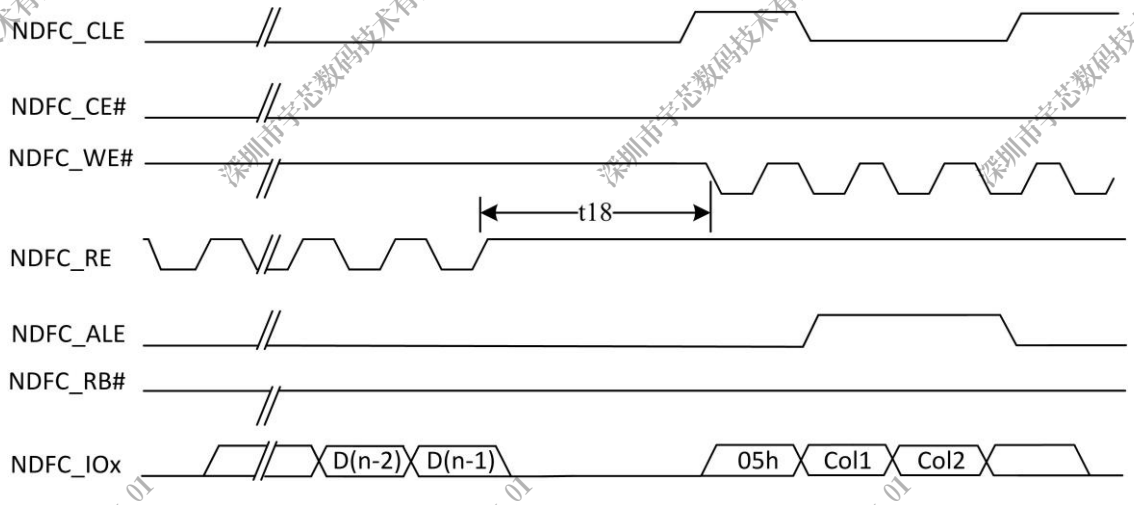



**Figure 5-19. RE# High to WE# Low Timing**

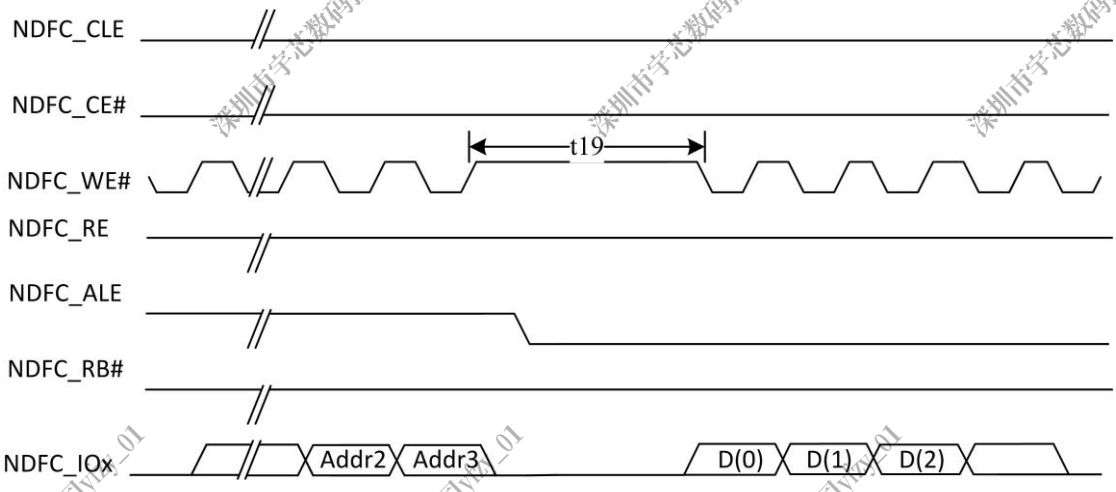



**Figure 5-20. Address to Data Loading Timing**

**Table 5-32. NAND Timing Constants**

| Parameter | Symbol | Timing | Unit |
|---|---|---|---|

| | | | |
|---|---|---|---|
| NDFC_CLE setup time | t1 | 2T | ns |
| NDFC_CLE hold time | t2 | 2T(1) | ns |
| NDFC_CE setup time | t3 | 2T | ns |
| NDFC_CE hold time | t4 | 2T | ns |
| NDFC_WE# pulse width | t5 | T | ns |
| NDFC_WE# hold time | t6 | T | ns |
| NDFC_ALE setup time | t7 | 2T | ns |
| Data setup time | t8 | T | ns |
| Data hold time | t9 | T | ns |
| Ready to NDFC_RE# low | t10 | 3T | ns |
| NDFC_ALE hold time | t11 | 2T | ns |
| NDFC_RE# pulse width | t12 | T | ns |
| NDFC_RE# hold time | t13 | T | ns |
| Read cycle time | t14 | 2T | ns |
| Write cycle time | t15 | 2T | ns |
| NDFC_WE# high to R/B# busy | t16 | T_WB(2) | ns |
| NDFC_WE# high to NDFC_RE# low | t17 | T_WHR(3) | ns |
| NDFC_RE# high to NDFC_WE# low | t18 | T_RHW(4) | ns |
| Address to Data Loading time | t19 | T_ADL(5) | ns |
| **NOTE (1):**T is the cycle of clock.<br>**NOTE (2),(3),(4),(5):**This values is configurable in Nand Flash controller. The value of T_WB could be 28T/44T/60T/76T, the value of T_WHR could be 0T/12T/28T/44T, the value of T_RHW could be 8T/24T/40T/56T, the value of T_ADL could be 0T/12T/28T/44T. | | | |

### 5.11.3. SMHC AC Electrical Characteristics

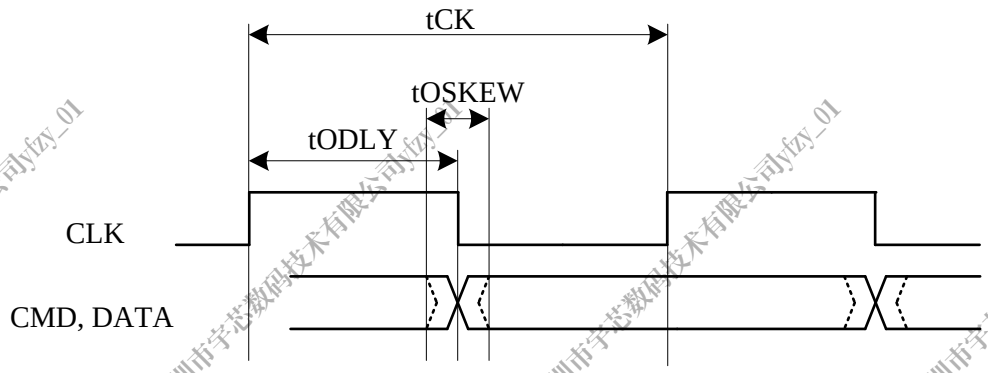



**Figure 5-21. SMHC in SDR Mode Output Timing**

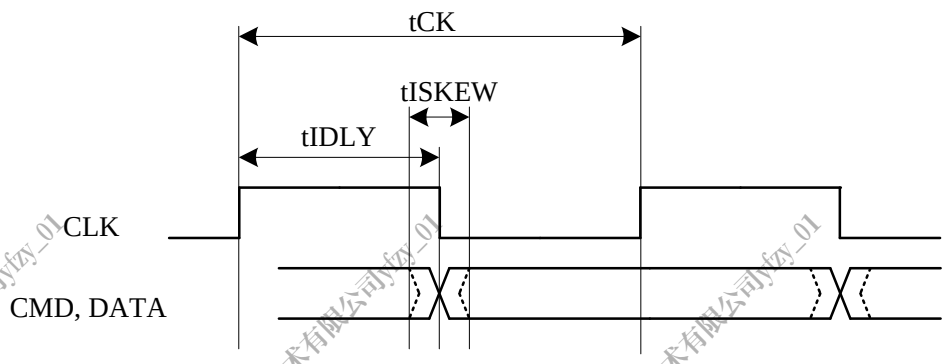



**Figure 5-22. SMHC in SDR Mode Input Timing**

**Table 5-33. SMHC Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty Cycle | DC | 45 | 50 | 55 | % |
| CMD, Data output delay time | tODLY | - | - | 12 | ns |
| Data output delay skew time | tOSKEW | - | - | 0.5 | ns |
| Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay. | tIDLY | - | - | 21 | ns |
| Data input skew time in SDR mode | tISKEW | - | - | 0.8 | ns |
| **Note (1)**: Output CMD, DATA is referenced to CLK. | | | | | |

# 5.12. External Peripherals Electrical Characteristics

## 5.12.1. LCD AC Electrical Characteristics

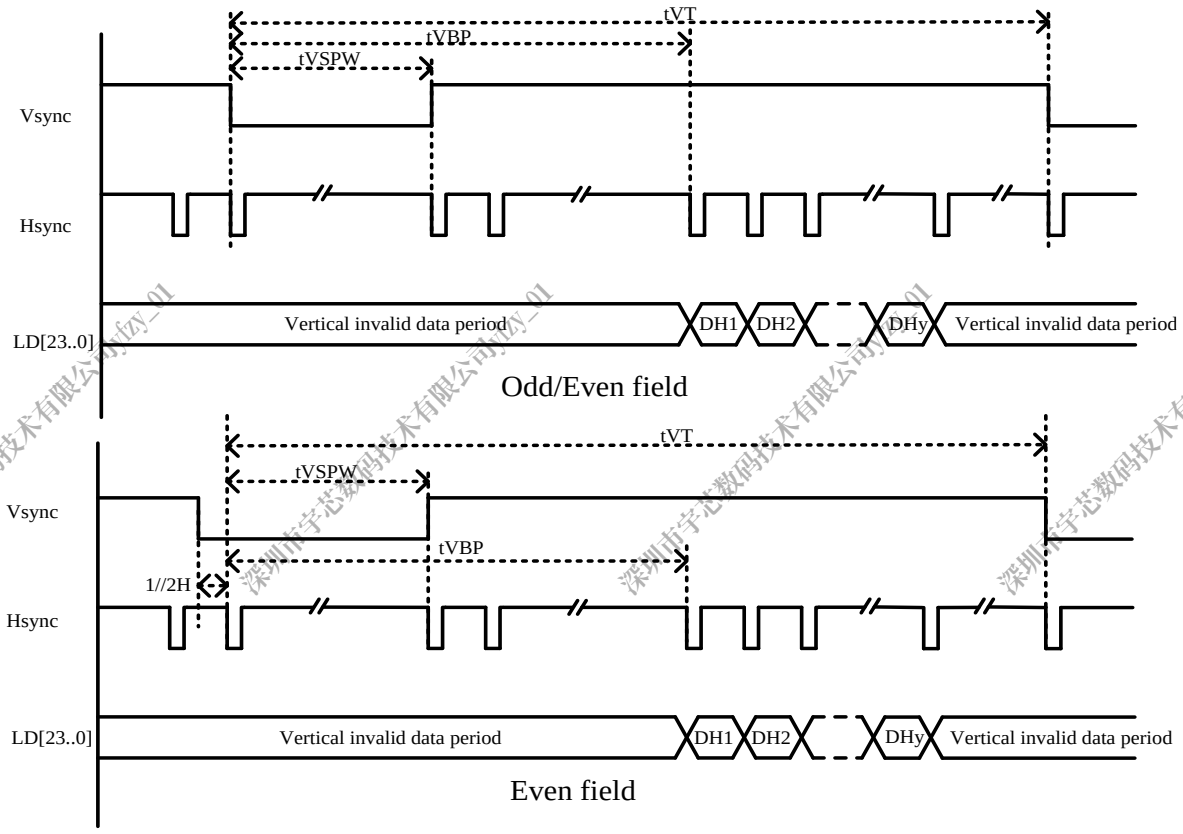



**Figure 5-23. HV_IF Interface Vertical Timing**

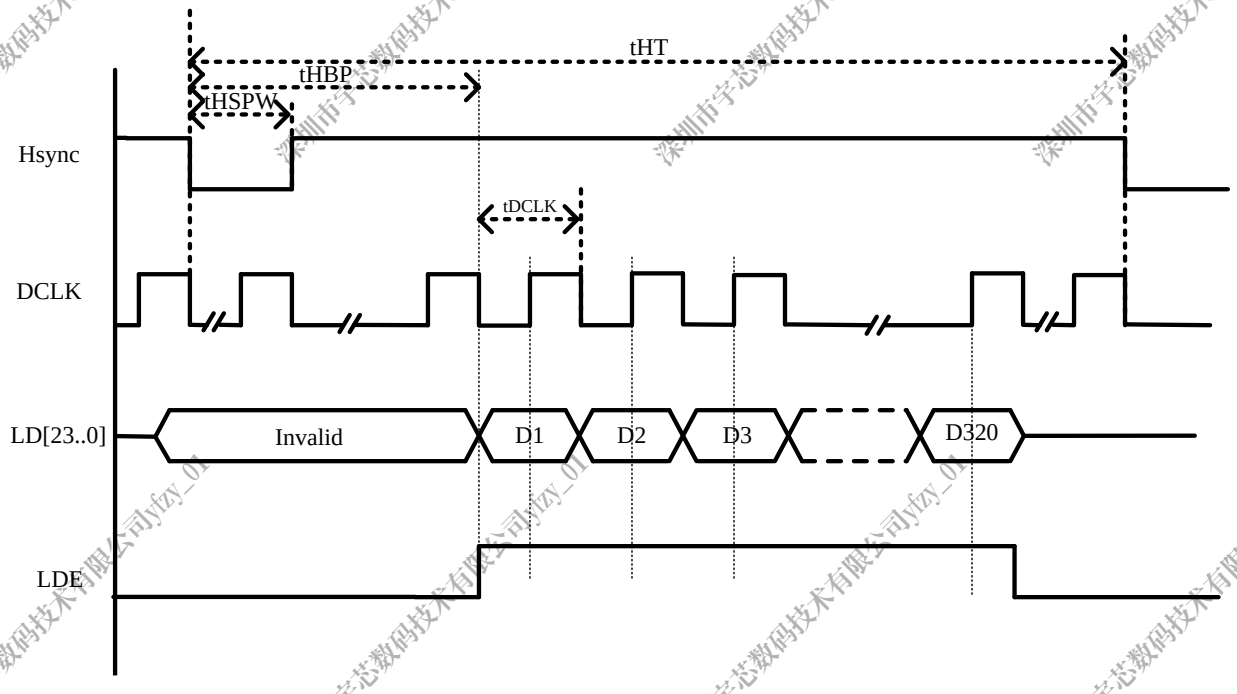



**Figure 5-24. HV_IF Interface Parallel Mode Horizontal Timing**

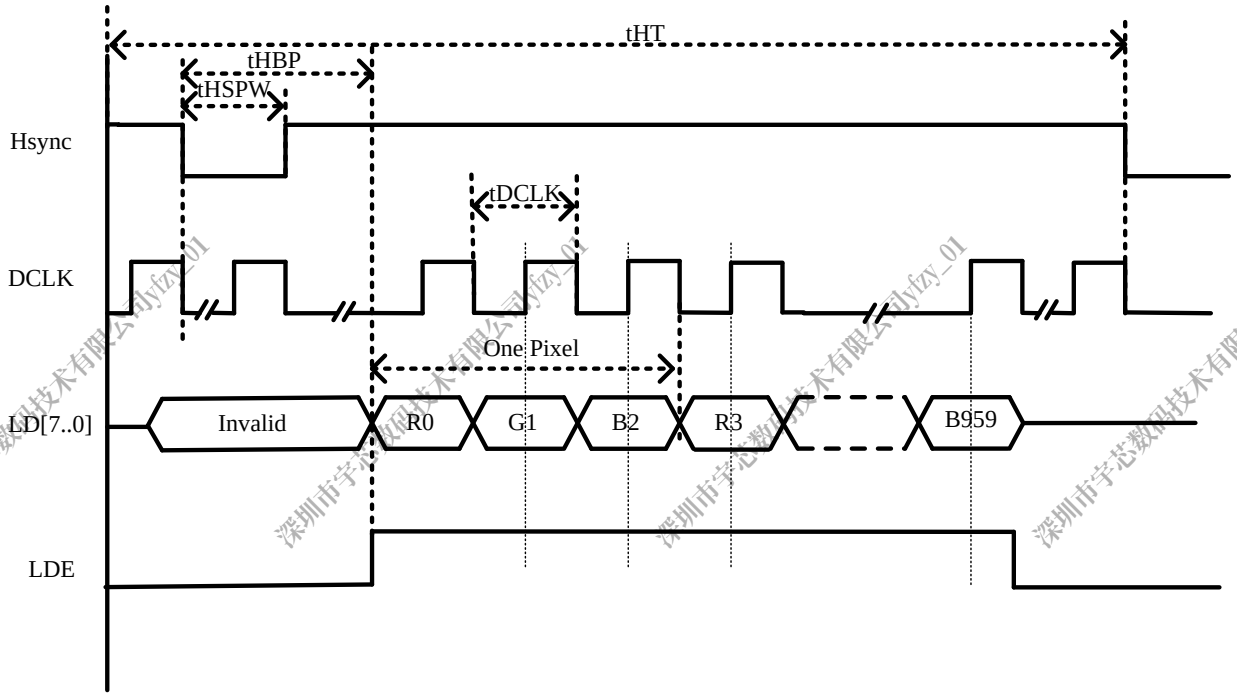



**Figure 5-25. HV_IF Interface Serial Mode Horizontal Timing**

**Table 5-34. LCD HV_IF Interface Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DCLK cycle time | tDCLK | 5 | - | - | ns |
| HSYNC period time | tHT | - | HT+1 | - | tDCLK |
| HSYNC width | tHSPW | - | HSPW+1 | - | tDCLK |
| HSYNC back porch | tHBP | - | HBP+1 | - | tDCLK |
| VSYNC period time | tVT | - | VT/2 | - | tHT |

| | | | | | |
|---|---|---|---|---|---|
| VSYNC width | tVSPW | - | VSPW+1 | - | tHT |
| VSYNC back porch | tVBP | - | VBP+1 | - | tHT |
| (1). Vsync: Vertical sync, indicates one new frame<br>(2). Hsync: Horizontal sync, indicate one new scan line<br>(3). DCLK: Dot clock, pixel data are sync by this clock<br>(4). LDE: LCD data enable<br>(5). LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel | | | | | |

### 5.12.2. CSI AC Electrical Characteristics

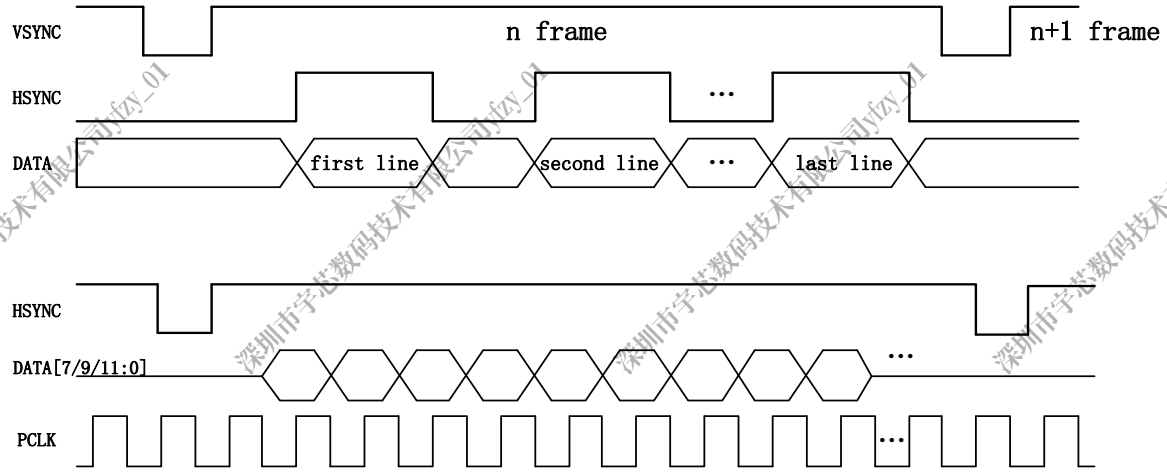



**Figure 5-26. 8/10/12-bit CMOS Sensor Interface Timing**
(clock rising edge sample. vsync valid = positive, hsycn valid = positive)

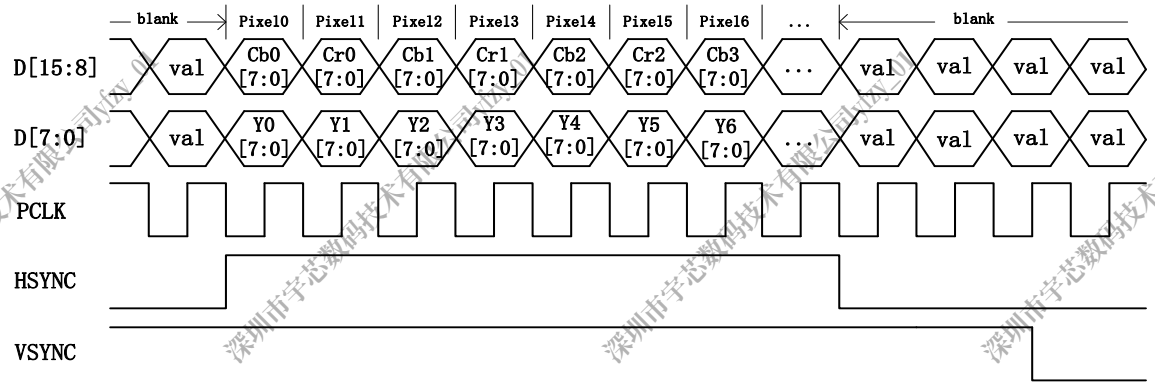



**Figure 5-27. 16-bit YCbCr4:2:2 with Separate Sync Timing**
(clock rising edge sample. vsync valid = positive, hsycn valid = positive)

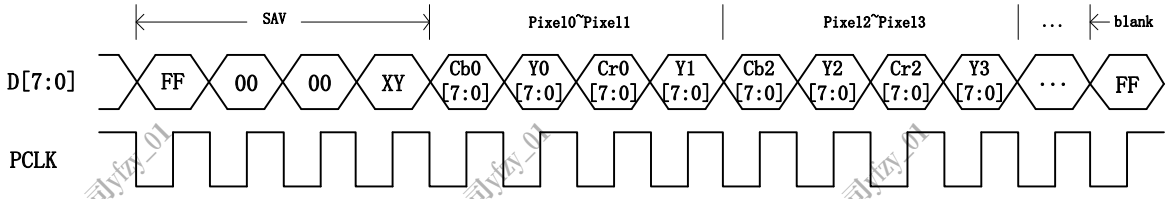



**Figure 5-28. 8-bit YCbCr4:2:2 with Embedded Syncs(BT656) Timing**

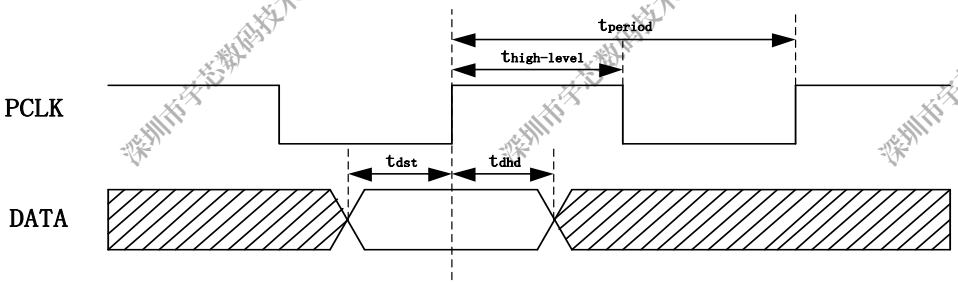



**Figure 5-29. Data Sample Timing**

**Table 5-35. CSI Interface Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Pclk Period | $t_{period}$ | 5.95 | - | - | ns |
| Pclk Frequency | $1/t_{period}$ | - | - | 168 | MHz |
| Pclk Duty | $t_{high-level}/t_{period}$ | 40 | 50 | 60 | % |
| Data input Setup time | $t_{dst}$ | 0.6 | - | - | ns |
| Data input Hold time | $t_{dhd}$ | 0.6 | - | - | ns |

## 5.12.3. EMAC/GMAC AC Electrical Characteristics

**MII Parameters**

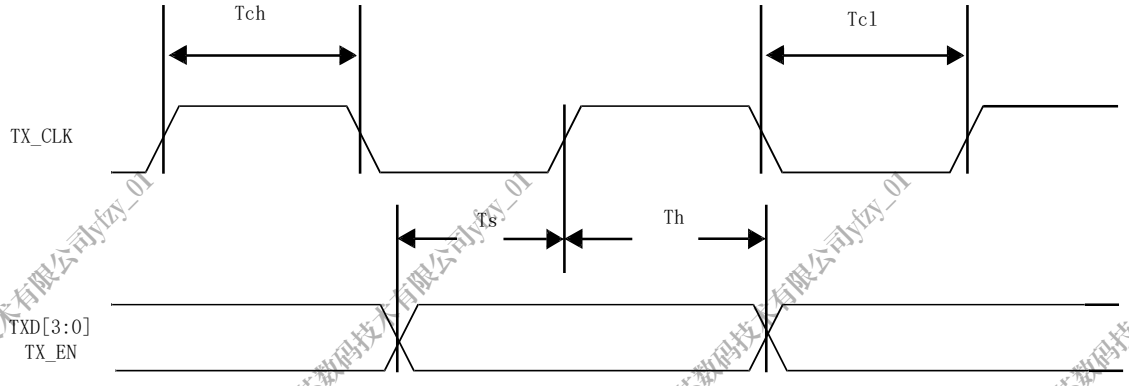



**Figure 5-30. MII Interface Transmit Timing**

**Table 5-36. MII Transmit Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Transmit Clock High Time,100M mode | Tch | - | 20 | - | ns |
| Transmit Clock Low Time,100M mode | Tcl | - | 20 | - | ns |
| TXEN/TXD setup time to TX_CLK | Ts | 10 | - | - | ns |
| TXEN/TXD hold time to TX_CLK | Th | 10 | - | - | ns |

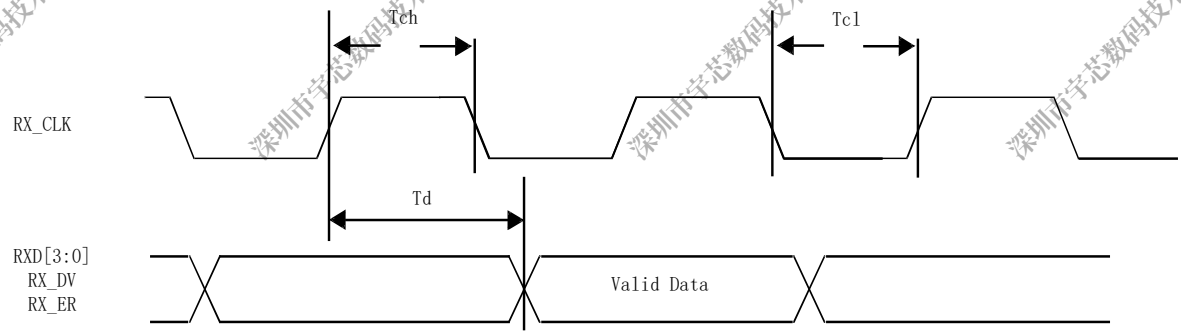



**Figure 5-31. MII Interface Receive Timing**

**Table 5-37. MII Receive Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Receive Clock High Time,100M mode | Tch | - | 20 | - | ns |
| Receive Clock Low Time,100M mode | Tcl | - | 20 | - | ns |
| RX_CLK to RXD[3:0]/RX_DV/RX_ER Delay | Td | 10 | - | 30 | ns |

**RMII Parameters**

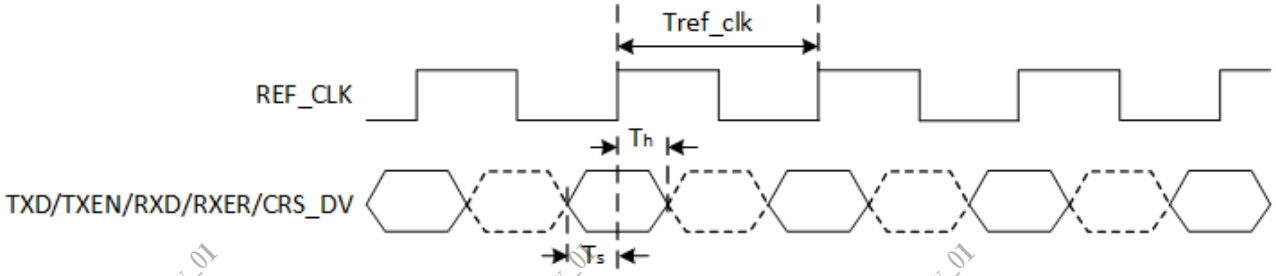



**Figure 5-32. RMII Interface Timing**

**Table 5-38. RMII Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Reference clock period | $T_{ref\_clk}$ | - | 20 | - | ns |
| TXD/TXEN/RXD/RXER/CRS_DV to REF_CLK setup time | Ts | 4 | - | - | ns |
| TXD/TXEN/RXD/RXER/CRS_DVTXD/TXEN to REF_CLK hold time | Th | 2 | - | - | ns |

**RGMII Parameters**

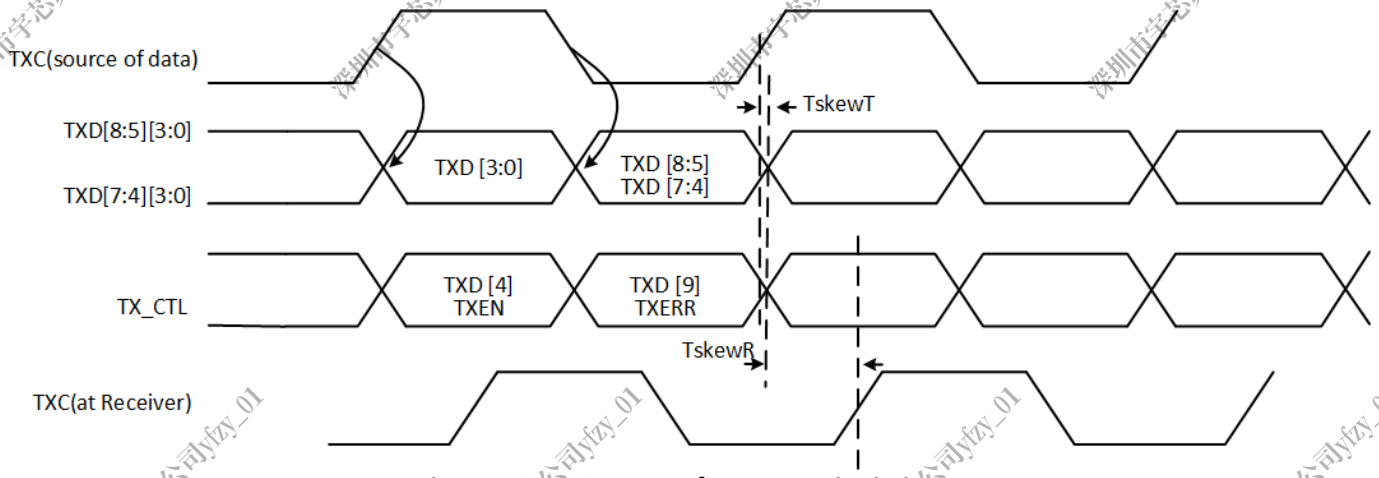



**Figure 5-33. RGMII Interface Transmit Timing**

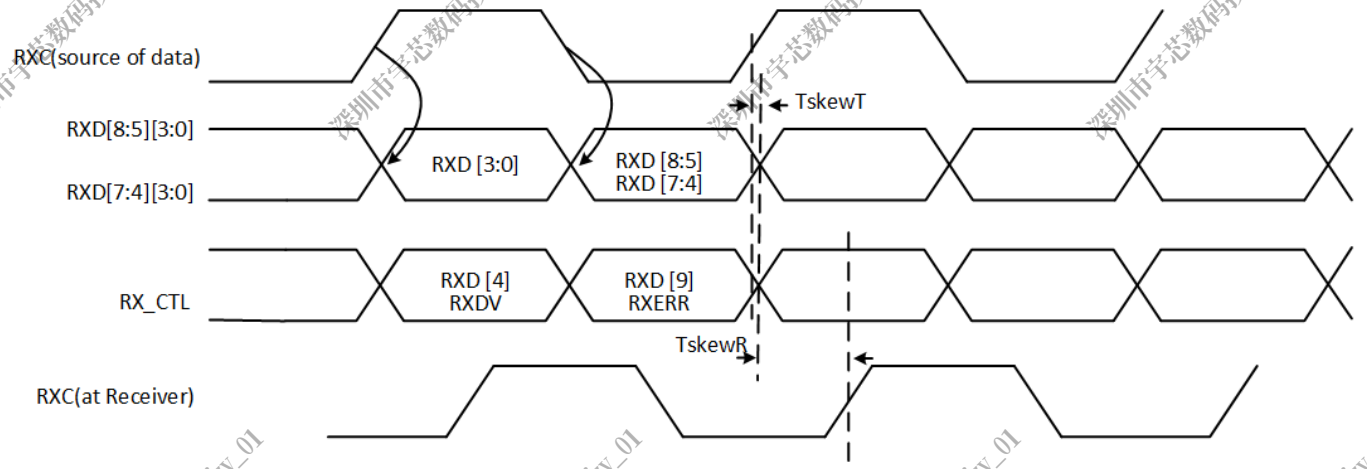



**Figure 5-34. RGMII Interface Receive Timing**

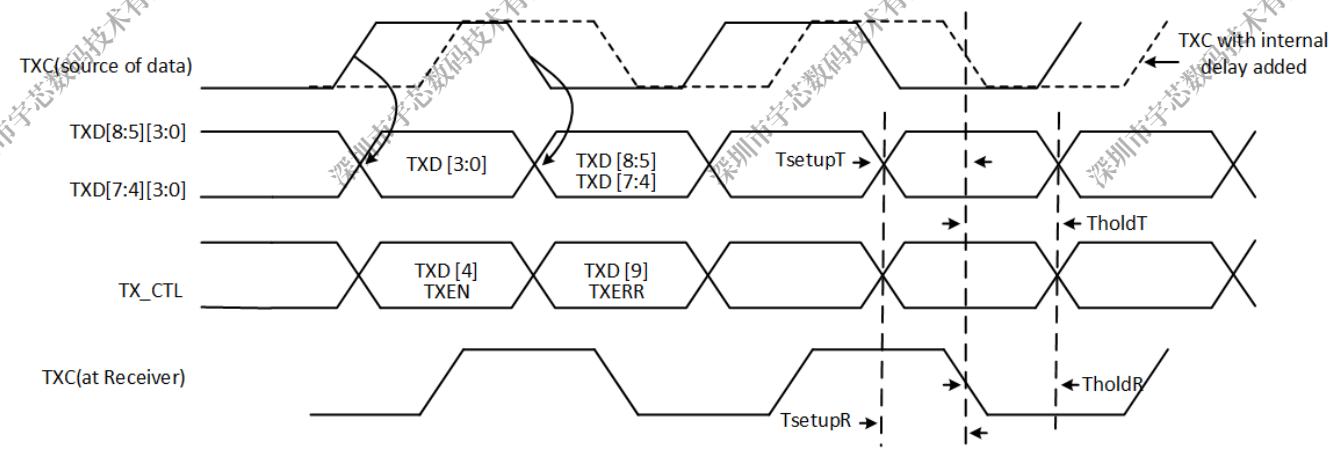



**Figure 5-35. RGMII-ID Interface Transmit Timing**

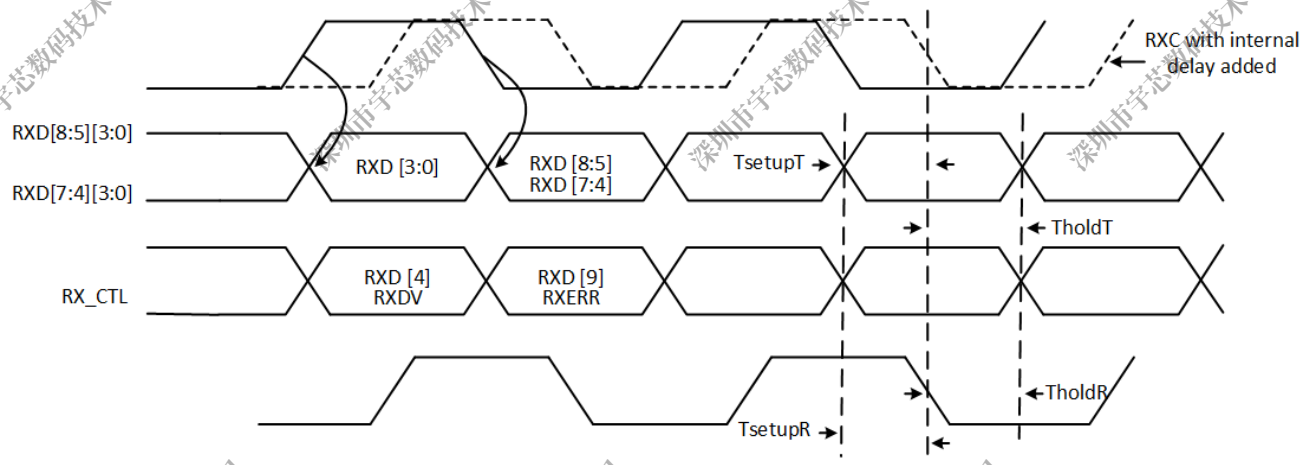



**Figure 5-36. RGMII-ID Interface Receive Timing**

**Table 5-39. RGMII Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to Clock output Skew (at Transmitter) | TskewT | -500 | 0 | 500 | ps |
| Data to Clock input Skew (at Receiver) | TskewR | 1.0 | 1.8 | 2.6 | ns |
| Data to Clock output Setup (at Transmitter – integrated delay ) | TsetupT | 1.2 | 2.0 | - | ns |
| Clock to Data output Hold (at Transmitter –integrated delay ) | TholdT | 1.2 | 2.0 | - | ns |
| Data to Clock input setup Setup (at Receiver –integrated delay ) | TsetupR | 1.0 | 2.0 | - | ns |
| Data to Clock input setup Setup (at Receiver –integrated delay ) | TholdR | 1.0 | 2.0 | - | ns |
| Clock Cycle Duration | Tcyc | 7.2 | 8 | 8.8 | ns |
| Duty Cycle for Gigabit | Duty_G | 45 | 50 | 55 | % |
| Duty Cycle for 10/100T | Duty_T | 40 | 50 | 60 | % |
| Rise / Fall Time (20-80%) | Tr/Tf | - | - | 75 | ns |
| Parameter | Symbol | Min | Typ | Max | Unit |
| Data to Clock output Skew (at Transmitter) | TskewT | -500 | 0 | 500 | ps |
| Data to Clock input Skew (at Receiver) | TskewR | 1.0 | 1.8 | 2.6 | ns |
| Data to Clock output Setup (at Transmitter – integrated delay ) | TsetupT | 1.2 | 2.0 | - | ns |
| Clock to Data output Hold (at Transmitter –integrated delay ) | TholdT | 1.2 | 2.0 | - | ns |
| Data to Clock input setup Setup (at Receiver –integrated delay ) | TsetupR | 1.0 | 2.0 | - | ns |
| Data to Clock input setup Setup (at Receiver –integrated delay ) | TholdR | 1.0 | 2.0 | - | ns |
| Clock Cycle Duration | Tcyc | 7.2 | 8 | 8.8 | ns |
| Duty Cycle for Gigabit | Duty_G | 45 | 50 | 55 | % |
| Duty Cycle for 10/100T | Duty_T | 40 | 50 | 60 | % |
| Rise / Fall Time (20-80%) | Tr/Tf | - | - | 75 | ns |

### 5.12.4. PS2 AC Electrical Characteristics

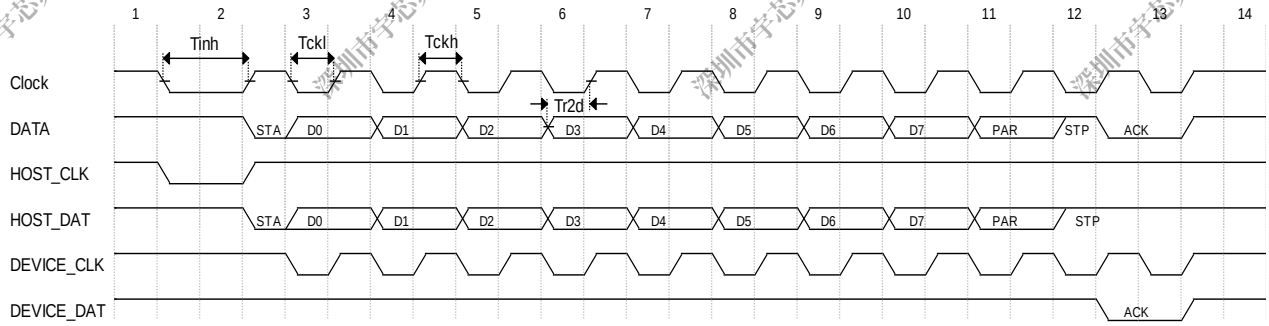



**Figure 5-37. PS2 Timing for Master Transmit Data and Device Receive Data**

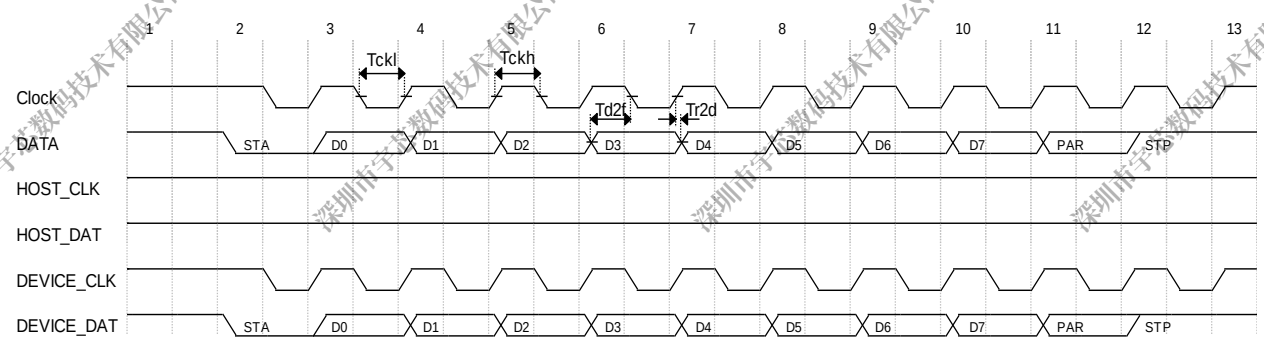



**Figure 5-38. PS2 Timing for Device Transmit Data and Master Receive Data**

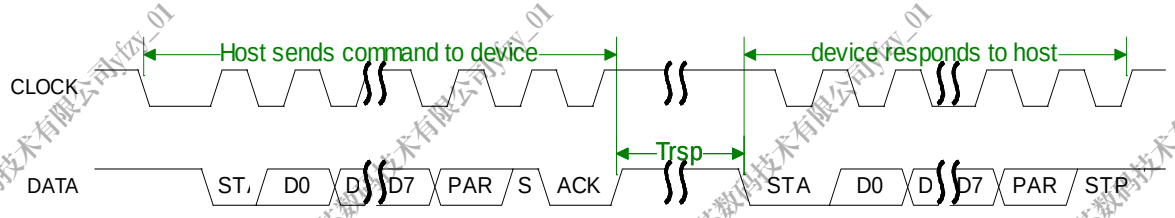



**Figure 5-39. PS2 Timing for Master Sending Command then Device Sending Response**

**Table 5-40. PS2 Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock Low time | Tckl | 30 | 40 | 50 | us |
| Clock High time | Tckh | 30 | 40 | 50 | us |
| Time for Host inhibit clock for send data request | Tinh | 100 | - | - | us |
| Data change to clock falling edge time during device to host transfer | Td2f | 5 | - | Tckh-5 | us |
| Clock rising edge to data change time during device to host transfer | Tr2d | 5 | - | Tckh-5 | us |
| Data change to clock rising edge time during host to device transfer | Td2r | 5 | - | Tckl-5 | us |
| Clock falling edge to data change time during host to device transfer | Tf2d | 5 | - | Tckl-5 | us |
| Host pull low Clock to Device drive Clock | Tc2c | - | - | 15 | ms |
| Time for packet to send | Tdata | - | - | 2 | ms |

| | | | | | |
|---|---|---|---|---|---|
| Time for device responding to the host command | Trsp | - | - | 20 | ms |

### 5.12.5. CIR AC Electrical Characteristics

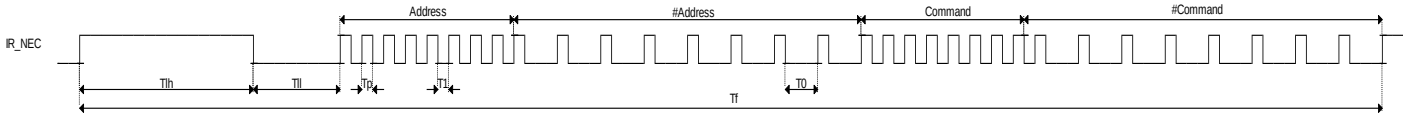



**Figure 5-40. CIR-RX Timing**

**Table 5-41. CIR-RX Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Frame Period | Tf | - | 67.5 | - | ms |
| Lead Code High Time | Tlh | - | 9 | - | ms |
| Lead Code Low Time | Tll | - | 4.5 | - | ms |
| Pulse Time | Tp | - | 560 | - | us |
| Logical 1 Low Time | T1 | - | 1680 | - | us |
| Logical 0 Low Time | T0 | - | 560 | - | us |

### 5.12.6. SPI AC Electrical Characteristics

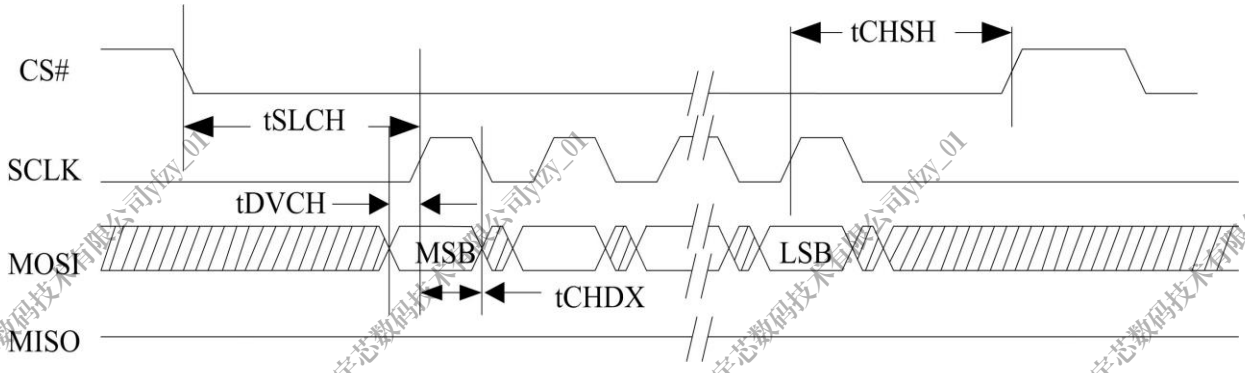



**Figure 5-41. SPI MOSI Timing**

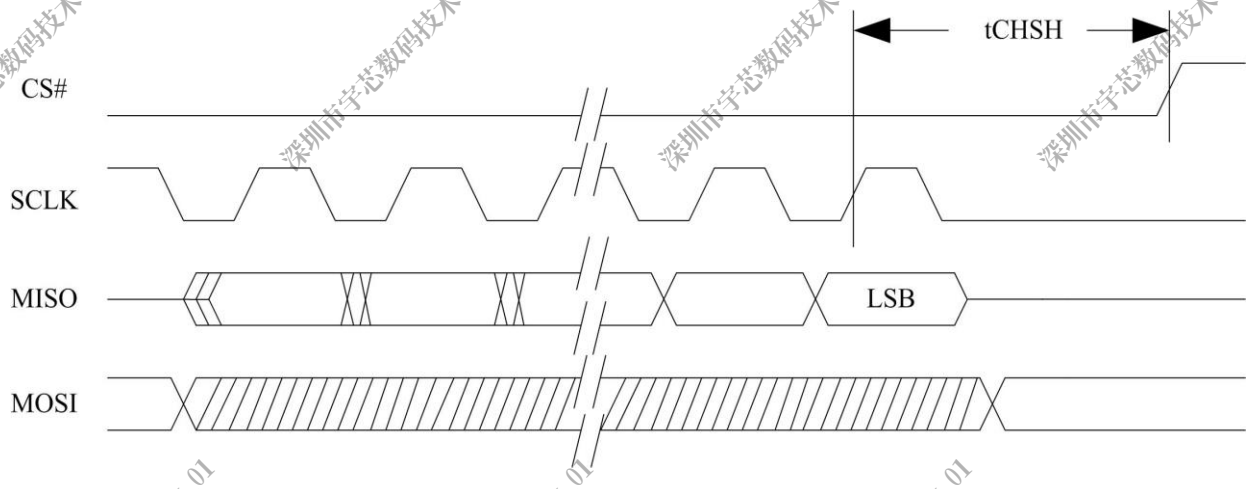



**Figure 5-42. SPI MISO Timing**

**Table 5-42. SPI Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CS# Active Setup Time | tSLCH | - | 2T | - | ns |
| CS# Active Hold Time | tCHSH | - | 2T(1) | - | ns |
| Data In Setup Time | tDVCH | - | T/2-3 | - | ns |
| Data In Hold Time | tCHDX | - | T/2-3 | - | ns |
| **Note (1)**:T is the cycle of clock. | | | | | |

## 5.12.7. UART AC Electrical Characteristics

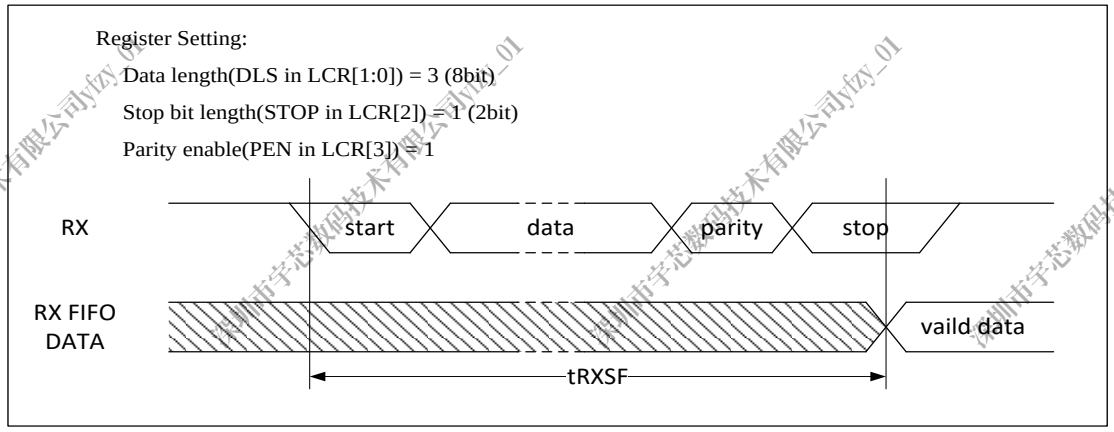



**Figure 5-43. UART RX Timing**

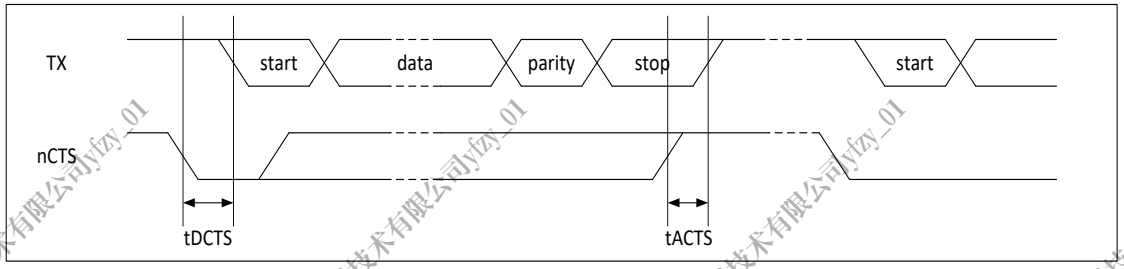



**Figure 5-44. UART nCTS Timing**

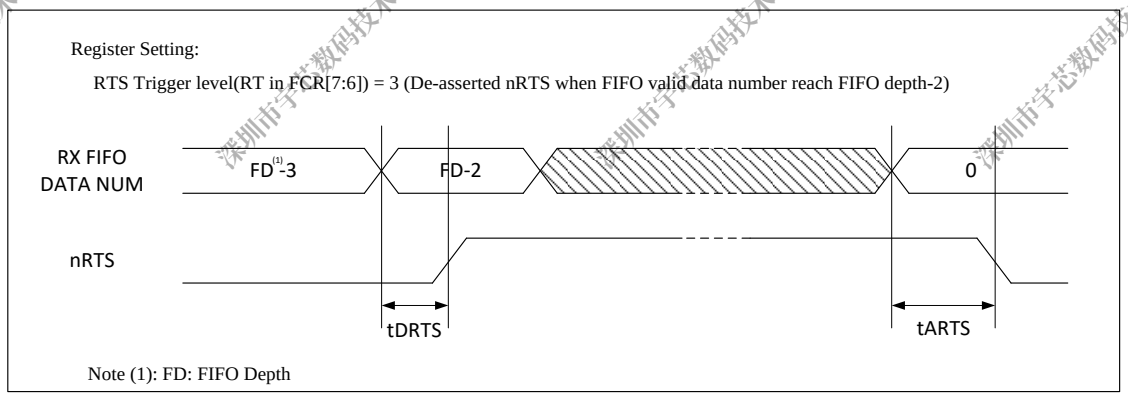



**Figure 5-45. UART nRTS Timing**

**Table 5-43. UART Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX start to RX FIFO | tRXSF | 10.5× BRP(1) | - | 11× BRP(1) | ns |
| Delay time of de-asserted nCTS to TX start | tDCTS | - | - | BRP(1) | ns |
| Step time of asserted nCTS to stop next transmission | tACTS | BRP(1)/4 | - | - | ns |
| Delay time of de-asserted nRTS | tDRTS | - | - | BRP(1) | ns |
| Delay time of asserted nRTS | tARTS | - | - | BRP(1) | ns |
| **Note (1)**: BRP(Baud-Rate Period). | | | | | |

## 5.12.8. TWI AC Electrical Characteristics

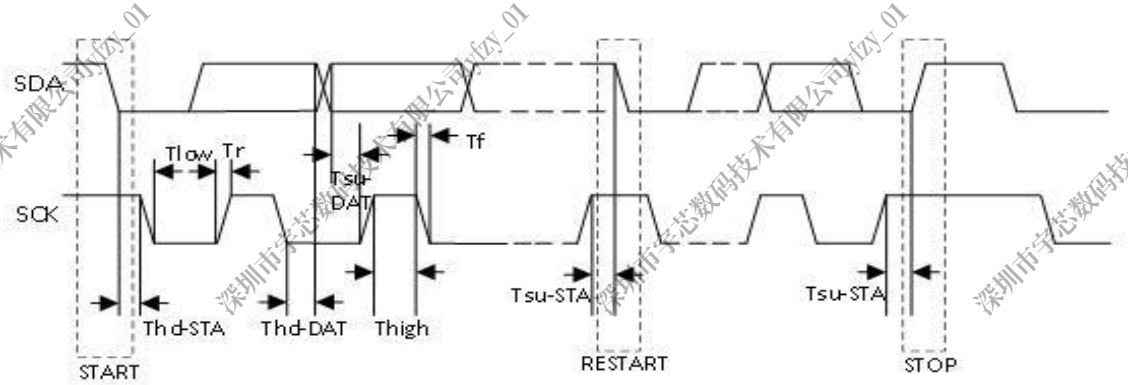



**Figure 5-46. TWI Timing**

**Table 5-44. TWI Timing Constants**

| Parameter | Symbol | Standard mode | | Fast mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| SCK clock frequency | Fsck | 0 | 100 | 0 | 400 | kHz |
| Setup time in Start | Tsu-STA | 4.7 | - | 0.6 | - | us |
| Hold time in Start | Thd-STA | 4.0 | - | 0.6 | - | us |
| Setup time in Data | Tsu-DAT | 250 | - | 100 | - | ns |
| Hold time in Data | Thd-DAT | 5.0 | - | - | - | ns |
| Setup time in Stop | Tsu-STO | 4.0 | - | 0.6 | - | us |
| SCK low level time | Tlow | 4.7 | - | 1.3 | - | us |

| Parameter | Symbol | Standard mode | | Fast mode | | Unit |
|---|---|---|---|---|---|---|
| SCK high level time | Thigh | 4.0 | - | 0.6 | - | ns |
| SCK/SDA falling time | Tf | - | 300 | 20 | 300 | ns |
| SCK/SDA rising time | Tr | - | 1000 | 20 | 300 | ns |

### 5.12.9. TSC AC Electrical Characteristics

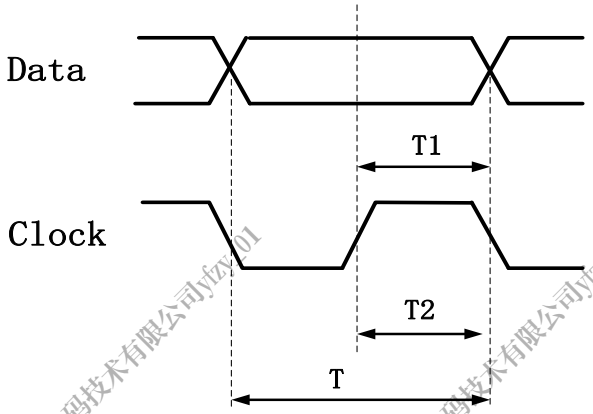



**Figure 5-47. TSC Data and Clock Timing**

**Table 5-45. TSC Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data hold time | T1 | T/2-T/10 | T(1)/2 | T/2+T/10 | us |
| Clock pulse width | T2 | T/2-T/10 | T/2 | T/2+T/10 | us |
| **Note (1):**T is the cycle of clock. | | | | | |

### 5.12.10. AC97 AC Electrical Characteristics

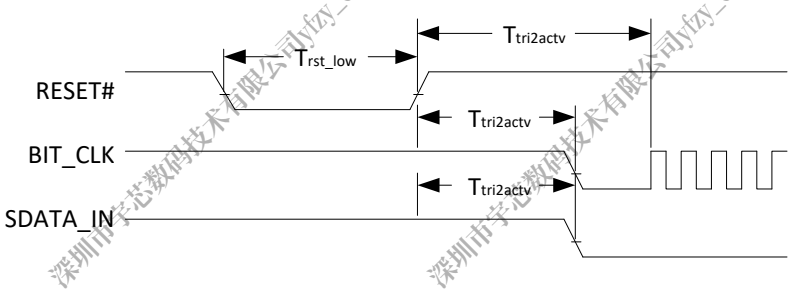



**Figure 5-48. AC97 Cold Reset Timing**

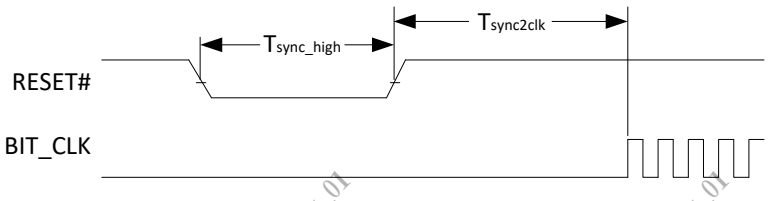



**Figure 5-49. AC97 Warm Reset Timing**

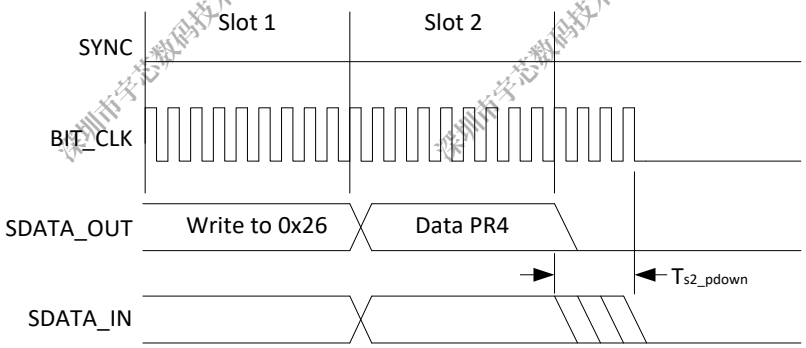



**Figure 5-50. AC-link Low Power Mode Timing**

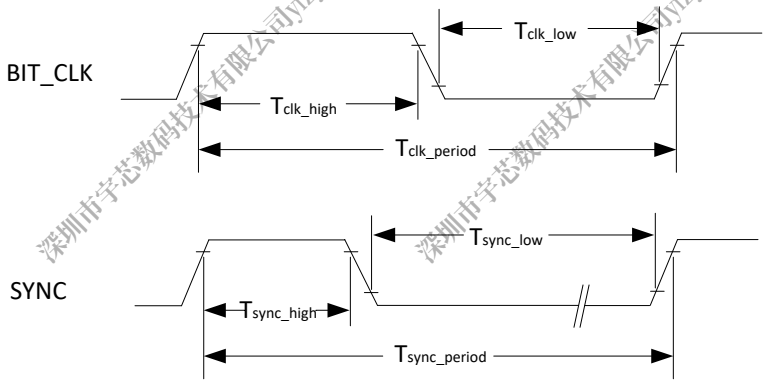



**Figure 5-51. BIT_CLK and SYNC Timing**

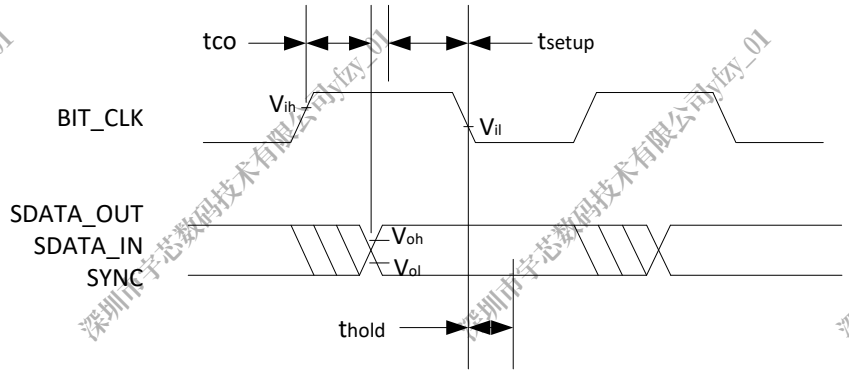



**Figure 5-52. AC-link Data Transmission Output and Input Timing**

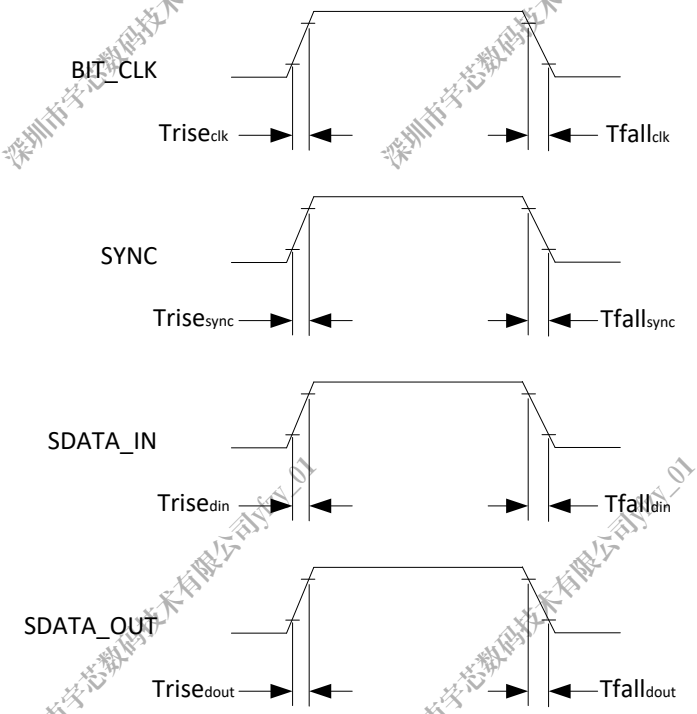



**Figure 5-53. Signal Rise and Fall Timing**

**Table 5-46. AC97 Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESET# active low pulse width | $T_{rst\_low}$ | 1.0 | - | - | us |
| RESET# inactive to SDATA_IN Or BIT_CLK active delay | $T_{tri2actv}$ | - | - | 25 | ns |
| RESET# inactive to BIT_CLK Startup delay | $T_{rst2clk}$ | 162.8 | - | - | ns |
| SYNC active high pulse width | $T_{sync\_high}$ | 1.0 | - | - | us |
| SYNC inactive to BIT_CLK startup delay | $T_{sync2clk}$ | 162.8 | - | - | ns |
| End of Slot 2 to BIT_CLK, SDATA_IN low | $T_{s2\_pdown}$ | - | - | 1.0 | us |
| BIT_CLK frequency | | - | 12.288 | - | MHz |
| BIT_CLK period | Tclk_period | - | 81.4 | - | ns |
| BIT_CLK output jitter | | - | - | 750 | ps |
| BIT_CLK high pulse width | Tclk_high | 36 | 40.7 | 45 | ns |
| BIT_CLK low pulse width | Tclk_low | 36 | 40.7 | 45 | ns |
| SYNC frequency | | - | 48.0 | - | kHz |
| SYNC period | Tsync_period | - | 20.8 | - | us |
| SYNC high pulse width | Tsync_high | - | 1.3 | - | us |
| SYNC low pulse width | Tsync_low | - | 19.5 | - | us |
| Output Valid Delay from rising edge of BIT_CLK | tco | - | - | 15 | ns |
| Input Setup to falling edge of BIT_CLK | tsetup | 10 | - | - | ns |
| Input Hold from falling edge of BIT_CLK | thold | 10 | - | - | ns |
| BIT_CLK combined rise or fall plus flight time (Primary Codec to Controller or Secondary) | | - | - | 7 | ns |

| | | | | | |
|---|---|---|---|---|---|
| SDATA combined rise or fall plus flight time (Output to Input) | | - | - | 7 | ns |
| BIT_CLK rise time | Triseclk | - | - | 6 | ns |
| BIT_CLK fall time | Tfallclk | - | - | 6 | ns |
| SYNC rise time | Trisesync | - | - | 6 | ns |
| SYNC fall time | Tfallsync | - | - | 6 | ns |
| SDATA_IN rise time | Trisedin | - | - | 6 | ns |
| SDATA_IN fall time | Tfalldin | - | - | 6 | ns |
| SDATA_OUT rise time | Trisedout | - | - | 6 | ns |
| SDATA_OUT fall time | Tfalldout | - | - | 6 | ns |
| (1). Worst case duty cycle restricted to 45/55<br>(2). Combined rise or fall plus flight times are provided for worst case scenario modeling purpose<br>(3). BIT_CLK rise/fall times with an external load of 75 pF<br>(4). SYNC and SDATA_OUT rise/fall times with a external load of 75 pF<br>(5). SDATA_IN rise/fall times with an external load of 60 pF<br>(6). Rise is from 10% to 90% of Vdd (Vol to Voh)<br>(7). Fall is from 90% to 10% of Vdd (Voh to Vol) | | | | | |

### 5.12.11. SCR AC Electrical Characteristics

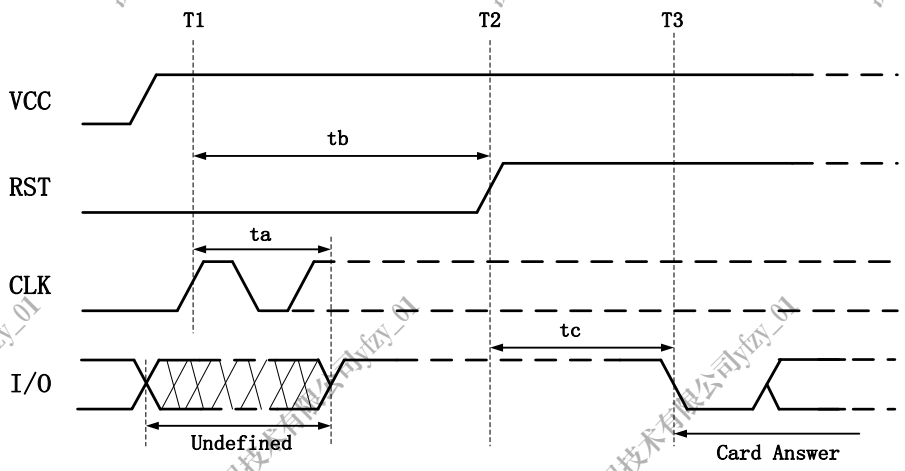



**Figure 5-54. SCR Activation and Cold Reset Timing**

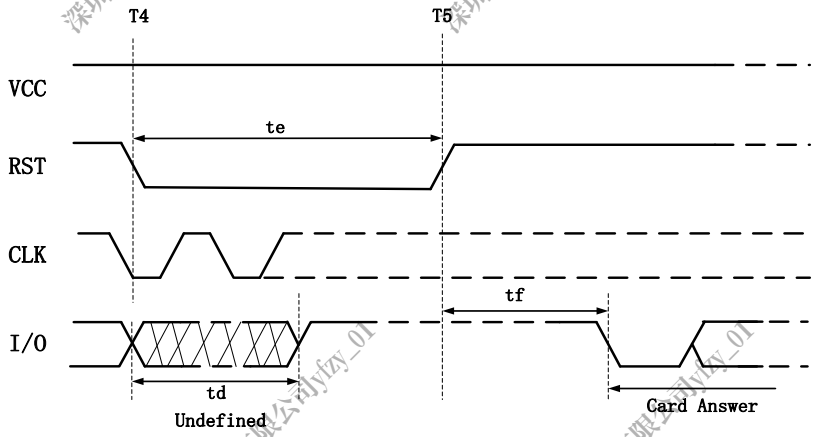



**Figure 5-55. SCR Warm Reset Timing**

**Table 5-47. SCR Timing Constants**

| Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|
| ta | - | - | 200/f | us |
| tb | 400/f | - | - | us |
| tc | 400/f | - | 40000/f | us |
| td | - | - | 200/f | us |
| te | 400/f | - | - | us |
| tf | 400/f | - | 40000/f | us |

(1). Activation: Before time T1
(2). Cold Reset: After time T1
(3). T1: The clock signal is applied to CLK at time T1.
(4). T2: The RST is put to state H.
(5). T3: The card begin answer at time T3
(6). ta: The card shall set I/O to state H within 200 clock cycles (delay ta) after the clock signal is applied to CLK (at time T1+ta).
(7). tb: The cold reset results from maintaining RST at state L for at least 400 clock cycles (delay tb) after the clock signal is applied to CLK (at time T1+tb).
(8). tc: The answer on I/O shall begin between 400 and 40000 clock cycles (delay tc) after the rising edge of the signal on RST (at time T2+tc).
(9). td: The card shall set I/O to state H within 200 clock cycles (delay td) after state L is applied to RST (at time T4+td).
(10). te: The controller initiates a warm reset (at time T4) by putting RST to state L for at least 400 clock cycles (delay te) while VCC remains powered and CLK provided with a suitable and stabled clock signal.
(11). tf: The card answer on I/O shall begin between 400 and 40000 clock cycles (delay tf) after the rising edge of the signal on RST (at time T5+tf).
(12). f is the frequency of clock.

## 5.13. Power-up and Power-down Sequence

The following figure shows an example of the power-up sequence for T3 device. During the entire power-up sequence, the AP_RESET# pin must be held on low until all power domains are stable. The other power domains not in Figure 5-56 can be turned on upon the software request.

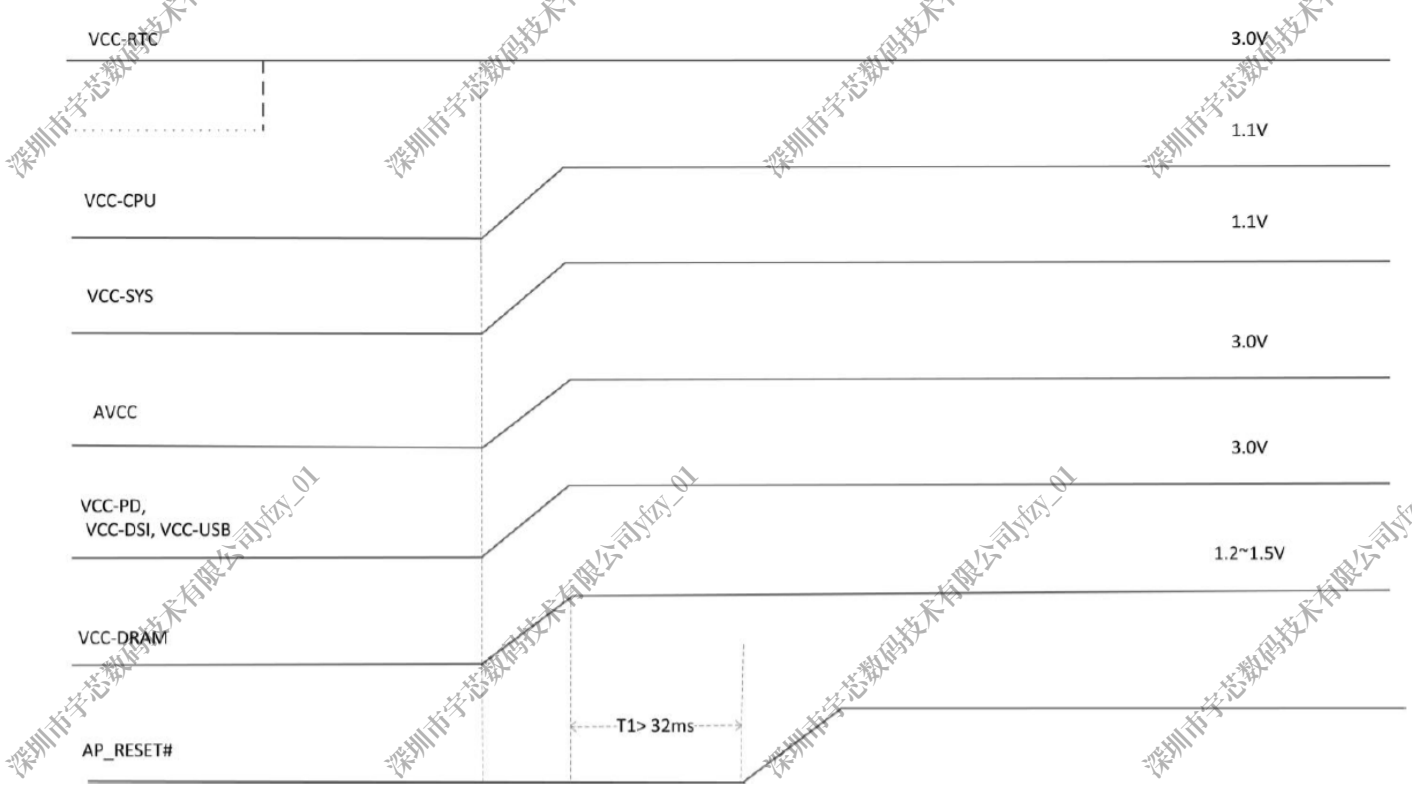



**Figure 5-56. T3 Power Up Sequence**

The power down solution is achieved by setting AP_RESET# to 0. When AP_RESET# powered down, then all power supplies start ramp down except VCC_RTC. The ramping down rate is decided by the load on the power supply.

# 6. Package Thermal Characteristics

For reliability and operability concerns, the absolute maximum junction temperature of T3 has to be below 125°C. The testing PCB is based on 4 layers. The following thermal resistance characteristics in Table 6-1 is based on JEDEC JESD51 standard, because the system design and temperature could be different with JEDEC JESD51, the simulating resulting data is a reference only, please prevail in the actual application condition test.

**Table 6-1. T3 Thermal Resistance Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance | - | 24 | - | °C/W |
| $\theta_{JB}$ | Junction-to-Board Thermal Resistance | - | 5.648 | - | °C/W |
| $\theta_{JC}$ | Junction-to-Case Thermal Resistance | - | 3.644 | - | °C/W |

(1). These values are based on a JEDEC-defined 2S2P system and will change based on environment as well as application.
(2). °C/W: degrees Celsius per watt.

# 7. Pin Assignment

## 7.1. Pin Map

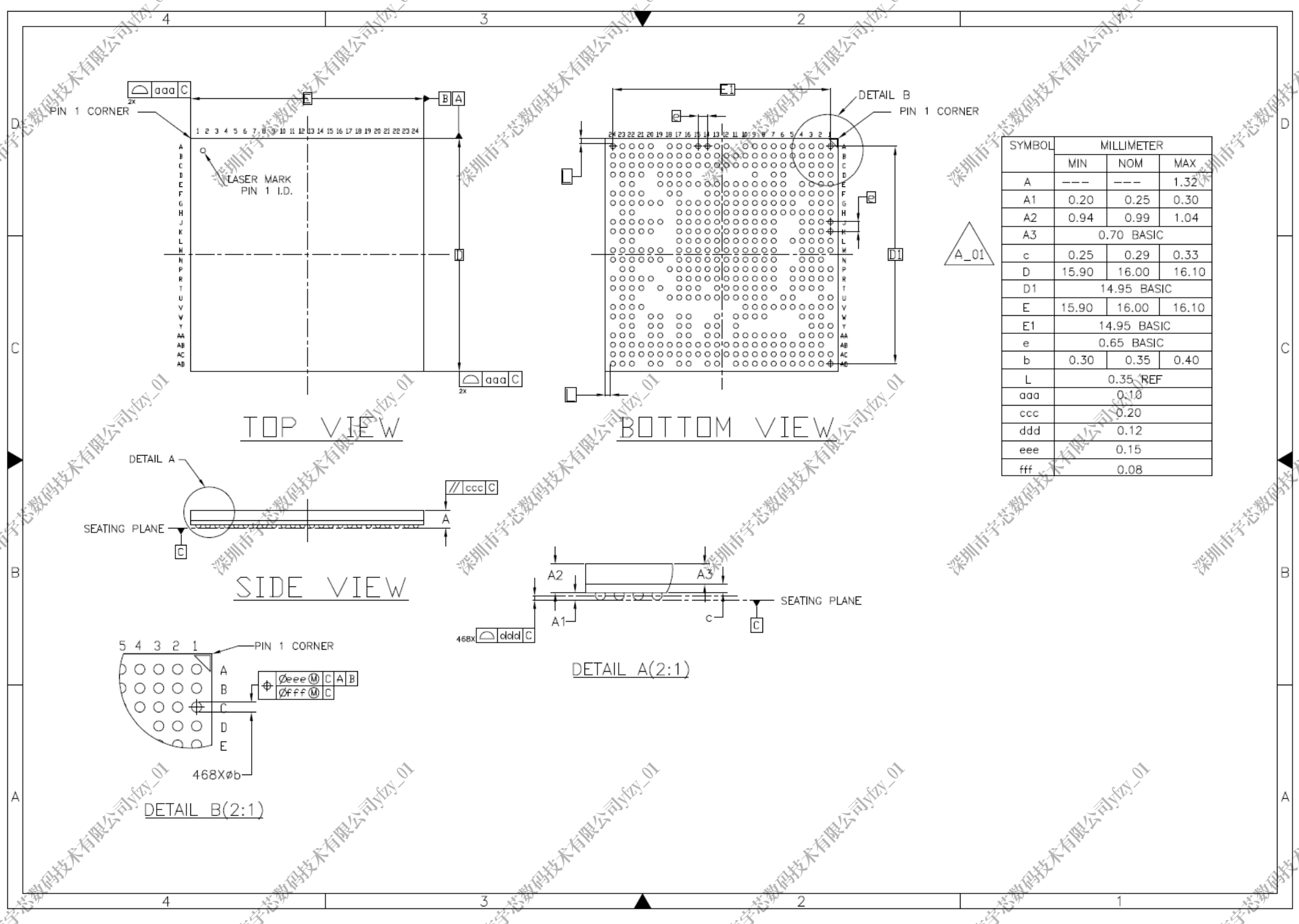
For T3, LFBGA 468 balls, 16 mm x 16 mm, 0.65 mm pitch package is offered. The pin maps are illustrated in Figure 7-1 for this package.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | SDQ11 | SDQ9 | SDQS1P | SDQ8 | SDQ10 | SDQM2 | SDQ18 | SDQ23 | SDQS2P | | SDQM3 | SDQ25 | SDQ27 | SDQS3P | SDQ24 | SDQ26 | PH26 | | X32KIN | PH15 | PH10 | PH9 | GND | A |
| B | SDQM1 | SDQ14 | SDQ12 | SDQS1N | SDQ15 | SDQ13 | SDQ16 | GND | SDQ21 | SDQS2N | SDQ20 | GND | SDQ28 | SDQ30 | SDQS3N | SDQ31 | SDQ29 | PH24 | PH27 | X32KOUT | PH14 | PH7 | PH8 | PH6 | B |
| C | SDQ6 | SDQ7 | SODT1 | GND | SCAS/SA0 | SCKE0 | SCKP | SCKN | SDQ19 | GND | SDQ17 | SDQ22 | SA12 | SA6 | GND | SBA0/ SA7 | GND | PH18 | PH23 | NMI | PH11 | PH13 | PH4 | PH5 | C |
| D | SDQ3 | SDQ1 | SCKE1 | | | SODT0 | GND | | SVREF | | | | | | | SA8 | SBA2 | PH17 | PH21 | | PH16 | PH12 | PH0 | PH2 | D |
| E | SDQS0P | SDQS0N | GND | SA15/ SCS1 | | SA4/SA11 | SA11/SA4 | SRST | SA14 | GND | SA10 | SA5 | GND | SBA1 | SRAS | GND | SA9 | PH25 | PH19 | | | PH3 | PH1 | | E |
| F | SDQ5 | SDQ0 | SCS0 | SA3 | GND | SA0/SCAS | GND | GND | GND | GND | GND | GND | SA7/ SBA0 | GND | | | GND | PH20 | | | PB21 | PB22 | PB23 | PB20 | F |
| G | SDQ2 | SDQ4 | SDQM0 | | SA2 | SWE | GND | GND | GND | GND | VCC-DRAM | VCC-DRAM | GND | VCC-DRAM | VCC-DRAM | VCC-DRAM | PH22 | | PB12 | PB13 | PB14 | PB17 | PB18 | PB19 | G |
| H | SZQ | GND | SA13 | GND | SA1 | GND | VCC-DRAM | GND | GND | VCC-DRAM | GND | VCC-DRAM | VCC-DRAM | GND | GND | GND | VCC-RTC | | | | | PB15 | PB16 | | H |
| J | MDSI-D0P | MDSI-D0N | MDSI-D2P | MDSI-D2N | | | GND | VCC-DRAM | GND | GND | GND | GND | GND | GND | VCC-IO | VCC-IO | VCC-IO | | PB11 | PB7 | PB8 | PB9 | PB10 | PB4 | J |
| K | MDSI-D1P | MDSI-D1N | MDSI-D3P | MDSI-D3N | | | JTAG-SEL | GND | GND | GND | GND | GND | GND | GND | GND | VCC-IO | VCC-IO | | | PB5 | PB6 | PB1 | PB2 | PB3 | K |
| L | MDSI-CKP | MDSI-CKN | PD12 | PD11 | PD10 | | FEL | VCC-DSI | GND | GND | GND | GND | GND | GND | GND | VCC-IO | VCC-PA | | | | | PB0 | PA0 | | L |
| M | PD1 | PD0 | PD8 | PD13 | | | VDD-EFUSEBP | VDD-EFUSE | GND | GND | VDD-SYS | VDD-SYS | GND | GND | GND | GND | GND | | PA1 | PA5 | PA4 | PA3 | PA2 | PA6 | M |
| N | | PD2 | PD14 | PD15 | | | VCC-PD | VCC-PD | GND-TVOUT | GND | VDD-SYS | VDD-SYS | GND | VDD-CPU | VDD-CPU | VDD-CPU | VDD-CPUFB | | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | N |
| P | PD4 | PD5 | PD7 | PD17 | PD16 | | VCC-TVIN | VCC-TVOUT | GND | GND | GND | VDD-SYS | GND | GND | VDD-CPU | VDD-CPU | VDD-CPU | GND | | | | PA14 | PA13 | | P |
| R | PD6 | PD8 | PD9 | PD19 | PD18 | | AVCC | VRA1 | VCC-HP | GND | GND | GND | VDD-SYS | GND | VDD-CPU | VDD-CPU | GND | | | PA17 | PA16 | PA15 | PI21 | RESET | R |
| T | | PD20 | PD23 | PD24 | PD25 | | VRA2 | VRP | VDD-SATA | VRP-TVIN | VCC-USB | VCC-PF | VCC-PLL | | VCC-PC | GND | VCC-PG | | PI16 | | PI20 | PI19 | PI17 | PI18 | T |
| U | PD21 | PD22 | | | PD26 | PD27 | | VCC33 | VDD25-SATA | VRN-TVIN | NC11 | TEST | GND | GND | VCC-PC | GND | VCC-PE | PI12 | | | | PI15 | PI14 | | U |
| V | TVOUT0 | TVOUT1 | TVOUT2 | TVOUT3 | PHONEOUTN | PHONEOUTP | AGND | GND-HP | NC8 | NC10 | | | | | | | | | | | PI13 | PI9 | PI10 | PI11 | V |
| W | | TVIN0 | TVIN3 | HPCOMFB | | | | HPBP | NC9 | REXT-SATA | PF2 | | PF5 | | | PC4 | PE2 | | PE3 | PI8 | | PI5 | PI6 | PI7 | W |
| Y | TVIN1 | TVIN2 | HPCOM | | | | | | | | PF1 | | PF4 | PC16 | | PC22 | PE1 | | PE4 | PG1 | | PI3 | PI4 | | Y |
| AA | HPOUTR | HPOUTL | LINEINL | KEYADC1 | | TPX1 | SATA-CLKM | SATA-RXP | SATA-TXP | USB2-DM | PF0 | | PF3 | PC21 | | PC19 | PE0 | | PE5 | PG0 | | PI0 | PI1 | PI2 | AA |
| AB | | LINEINR | MICIN1 | TPY2 | TPY1 | TPX2 | SATA-CLKP | SATA-RXM | SATA-TXM | USB2-DP | PF0 | PC3 | PC7 | GND | PC9 | PC18 | PC23 | PC20 | PE6 | PE10 | PG2 | PG4 | PG10 | PG11 | AB |
| AC | FMINL | FMINR | VMIC | NC7 | NC1 | NC3 | NC5 | USB0-DM | USB1-DM | PC1 | X24MOUT | PC6 | PC11 | PC8 | PC13 | PC17 | PC10 | PC5 | PE7 | PE11 | PG3 | PG5 | PG8 | PG9 | AC |
| AD | GND | MICIN2 | KEYADC0 | NC6 | NC0 | NC2 | NC4 | USB0-DP | USB1-DP | PC2 | X24MIN | | PC24 | PC12 | | PC14 | PC15 | | PE8 | PE9 | | PG6 | PG7 | GND | AD |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | |

**Figure 7-1. T3 Pin Map**

## 7.2. Package Dimension

Figure 7-2 shows the top, bottom, and side views of T3 package dimension.




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | --- | --- | 1.32 |
| A1 | 0.20 | 0.25 | 0.30 |
| A2 | 0.94 | 0.99 | 1.04 |
| A3 | 0.70 BASIC | | |
| c | 0.25 | 0.29 | 0.33 |
| D | 15.90 | 16.00 | 16.10 |
| D1 | 14.95 BASIC | | |
| E | 15.90 | 16.00 | 16.10 |
| E1 | 14.95 BASIC | | |
| e | 0.65 BASIC | | |
| b | 0.30 | 0.35 | 0.40 |
| L | 0.35 REF | | |
| aaa | 0.10 | | |
| ccc | 0.20 | | |
| ddd | 0.12 | | |
| eee | 0.15 | | |
| fff | 0.08 | | |

**Figure 7-2. T3 Package Dimension**

# 8. Carrier, Storage and Baking Information

## 8.1. Carrier

### 8.1.1. Matrix Tray Information

Table 8-1 shows the T3 matrix tray carrier information.

**Table 8-1. Matrix Tray Carrier Information**

| Item | Color | Size | Note |
|---|---|---|---|
| Tray | Black | 315mm x 136mm x 7.62mm | 84 Qty/Tray |
| Aluminum foil bags | Silvery white | 540mm x 300mm x 0.14mm | Surface impedance:$10^9\Omega$<br>Vacuum packing<br>Including HIC and desiccant<br>Printing: RoHS symbol |
| Pearl cotton cushion(Vacuum bag) | White | 12mm x 680mm x 185mm | |
| Pearl cotton cushion (The Gap between vacuum bag and inner box) | White | Left-Right:12mm x 180mm x 85mm<br>Front-Back:12mm x 350mm x 70mm | |
| Inner Box | White | 396mm x 196mm x 96mm | Printing: RoHS symbol<br>10 Tray/Inner box |
| Carton | White | 420mm x 410mm x 320mm | 6 Inner box/Carton |

HIC:


Desiccant:


RoHS symbol:


Product label:

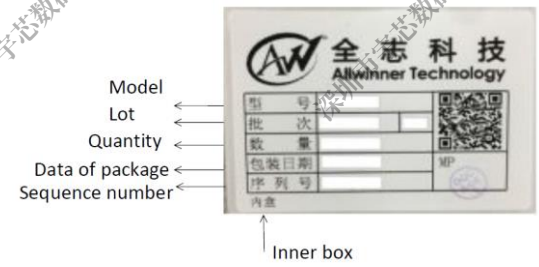



Table 8-2 shows the T3 packing quantity.

**Table 8-2. Packing Quantity Information**

| Sample | Size(mm) | Qty/Tray | Tray/Inner Box | Full Inner Box Qty | Inner Box/Carton | Full Carton Qty |
|---|---|---|---|---|---|---|
| T3 | 16 x 16 | 84 | 10 | 840 | 6 | 5040 |

Figure 8-1 shows tray dimension drawing of the T3.

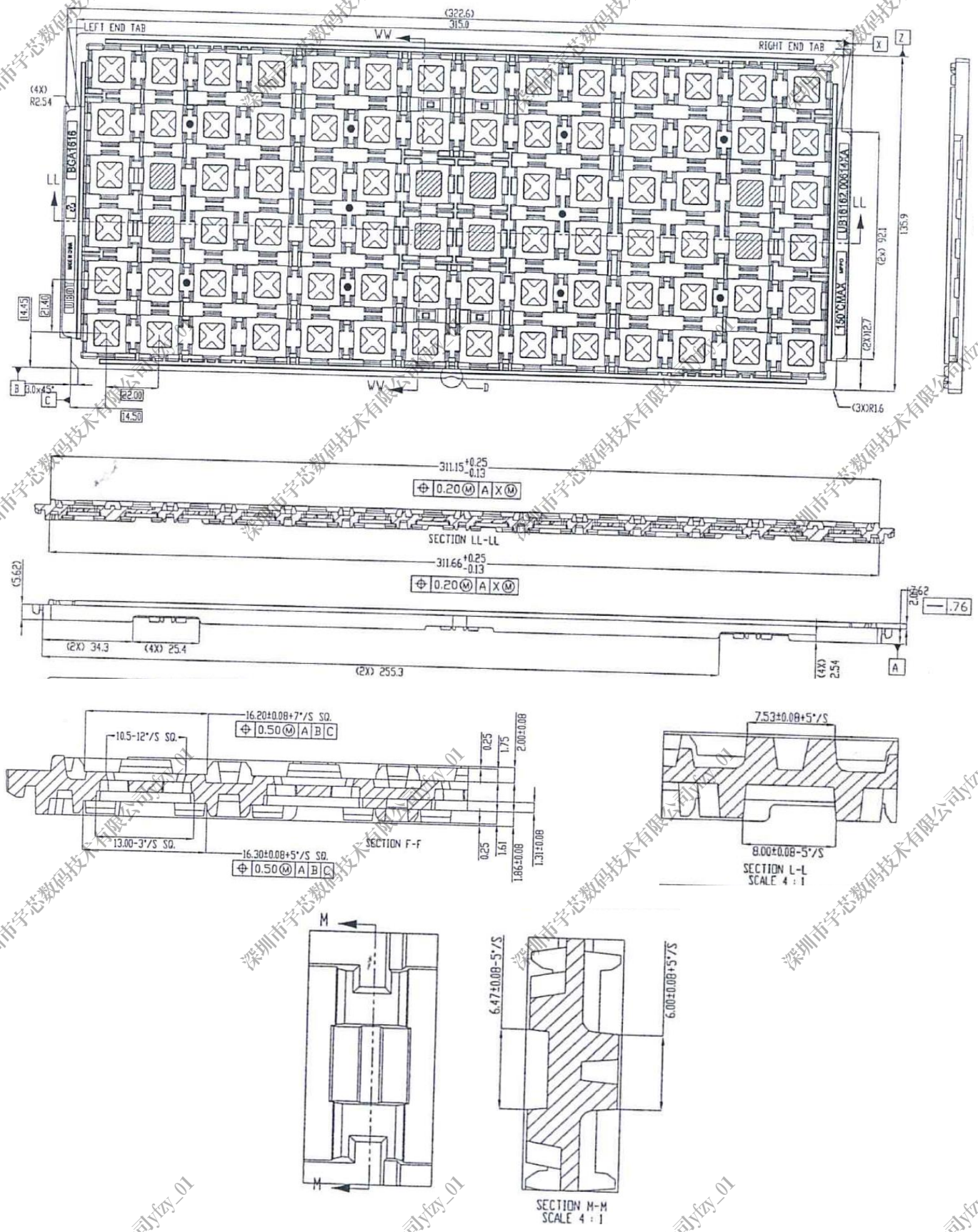



**Figure 8-1. Tray Dimension Drawing**

## 8.2. Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

### 8.2.1. Matrix Tray Information

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL are defined in Table 8-3.

**Table 8-3. MSL Summary**

| MSL | Out-of-bag floor life | Comments |
|---|---|---|
| 1 | Unlimited | ≤30°C / 85%RH |
| 2 | 1 year | ≤30°C / 60%RH |
| 2a | 4 weeks | ≤30°C / 60%RH |
| 3 | 168 hours | ≤30°C / 60%RH |
| 4 | 72 hours | ≤30°C / 60%RH |
| 5 | 48 hours | ≤30°C / 60%RH |
| 5a | 24 hours | ≤30°C / 60%RH |
| 6 | Time on Label(TOL) | ≤30°C / 60%RH |

**NOTE**
**The T3 device samples are classified as MSL3.**

### 8.2.2. Bagged Storage Conditions

The shelf life of the T3 device samples is defined in Table 8-4.

**Table 8-4. Bagged Storage Conditions**

| | |
|---|---|
| **Packing mode** | Vacuum packing |
| **Storage temperature** | 20°C ~26°C |
| **Storage humidity** | 40%~60%RH |
| **Shelf life** | 12 months |

### 8.2.3. Out-of-bag Duration

It is defined by the device MSL rating, the out-of-bag duration of the T3 is as follows.

**Table 8-5. Out-of-bag Duration**

| | |
|---|---|
| **Storage temperature** | 20°C ~26°C |
| **Storage humidity** | 40%~60%RH |
| **Moisture sensitive level(MSL)** | 3 |
| **Floor life** | 168 hours |

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

## 8.3. Baking

It is not necessary to bake the T3 if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded.
It is necessary to bake the T3 if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

It is necessary bake the T3 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that baking should not exceed 3 times.

# 9. Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, please contact with Allwinner FAE.

The lead-free reflow profile conditions are given in Table 9-1. The table is for reference only.

**Table 9-1. Lead-free Reflow Profile Conditions**

| | QTI typical SMT reflow profile conditions(for reference only) | |
|---|---|---|
| | **Step** | **Reflow condition** |
| Environment | N2 purge reflow usage (yes/no) | Yes, N2 purge used |
| | If yes, O2 ppm level | O2 < 1500 ppm |
| A | Preheat ramp up temperature range | 25°C -> 150°C |
| B | Preheat ramp up rate | 1.5~2.5 °C /sec |
| C | Soak temperature range | 150°C -> 190°C |
| D | Soak time | 80~110 sec |
| E | Liquidus temperature | 217°C |
| F | Time above liquidus | 60-90 sec |
| G | Peak temperature | 240-250°C |
| H | Cool down temperature rate | ≤4°C /sec |

Figure 9-1 shows the typical lead-free reflow profile.

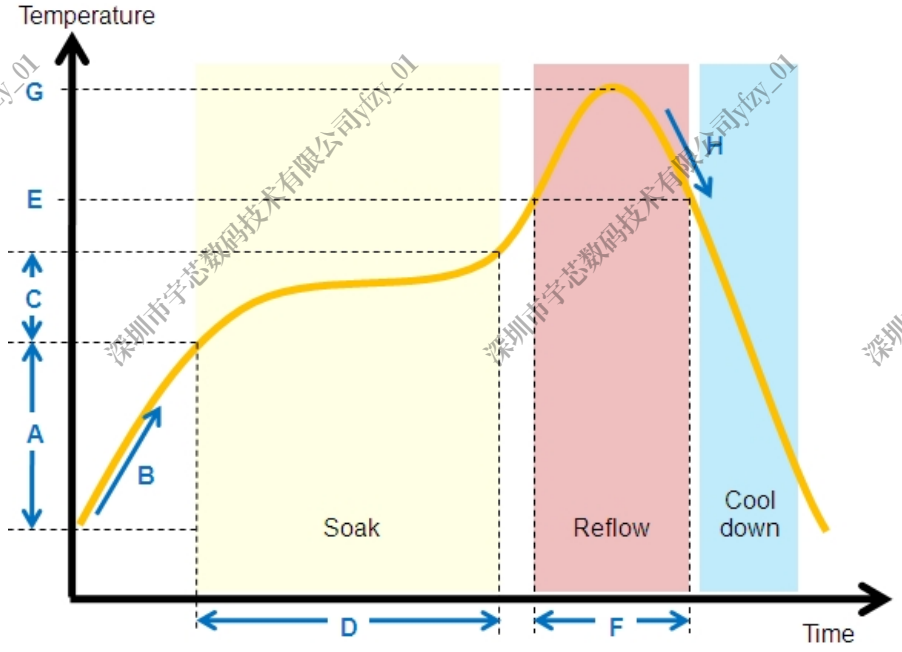



**Figure 9-1. Typical Lead-free Reflow Profile**

**NOTE**

**The above reflow profile is solder joint testing result, it is for reference only, please adjust depending on actual production conditions.**

The method of measuring the reflow soldering process is as follows:

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

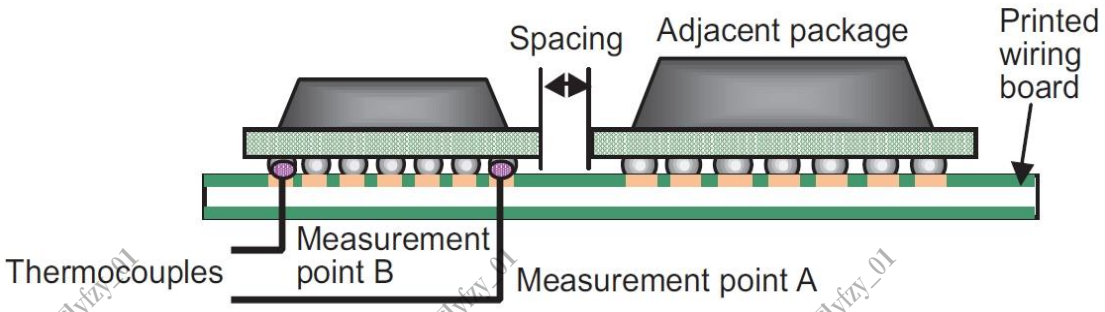



**Figure 9-2. Measuring the Reflow Soldering Process**

**NOTE**

**To measure the temperature of QFP-packaged chip, place the temperature probe directly at the pin.**

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

# 10. Part Marking

Figure 10-1 shows the T3 marking.

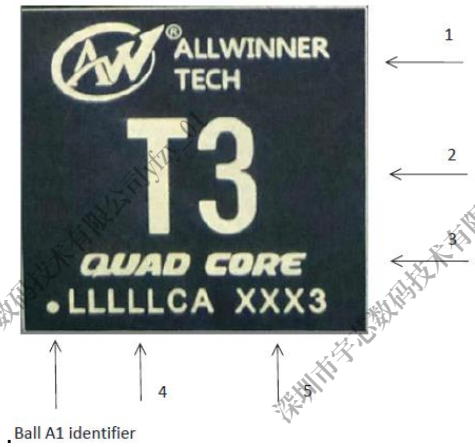



**Figure 10-1. T3 Marking**

Table 10-1 describes the T3 marking definitions.

**Table 10-1. T3 Marking Definitions**

| No. | Marking | Description | Fixed/Dynamic |
|---|---|---|---|
| 1 | ALLWINNER TECH | Allwinner logo or name | Fixed |
| 2 | T3 | Product name | Fixed |
| 3 | QUAD CORE | CPU core flag | Fixed |
| 4 | LLLLLCA | Lot number | Dynamic |
| 5 | XXX3 | Date code | Dynamic |

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