# 1. FEATURES

- AEC-Q100 (ADX112Q only)
- Ultra-small QFN package:
  2mm × 1.5mm × 0.4mm
- Small 3mm × 3mm MSOP package
- Wide supply range: 2V to 5.5V
- Low current consumption:
  - Continuous mode: Only 145μA
  - Single-shot mode: automatic power-down
- Programmable data rate: 8SPS to 860SPS
- Single-cycle settling
- Internal low-drift voltage reference
- Internal oscillator
- SPI-Compatible interface
- Internal PGA
- Four single-ended or two differential inputs
- Operating temperature range:
  –40°C to 125°C

# 2. APPLICATIONS

- Temperature measurement:
  - Thermocouple measurement
  - Cold-junction compensation
  - Thermistor measurement
- Portable instrumentation
- Battery voltage and current monitoring
- Factory automation and process controls

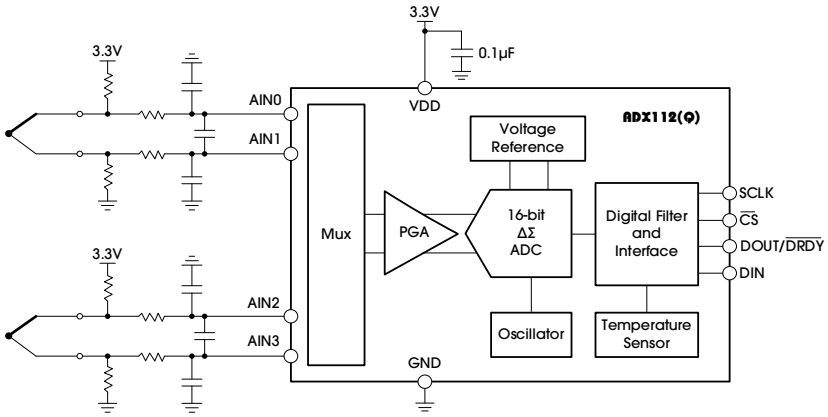
# 3. DESCRIPTION

The ADX112(Q) is a precision, low-power, 16-bit analog-to-digital converter (ADC) that provides all features necessary to measure the most common sensor signals in an MSOP-10 package or an ultra-small, leadless QFN-10 package. The ADX112(Q) integrates a programmable gain amplifier (PGA), voltage reference, oscillator, and high-accuracy temperature sensor. These features, along with a wide power supply range from 2V to 5.5V, make the ADX112(Q) ideally suited for power-constrained and space-constrained, sensor-measurement applications.

The ADX112(Q) can perform conversions at data rates up to 860 samples per second (SPS). The PGA offers input ranges from ±256mV to ±6.144V, allowing both large and small signals to be measured with high resolution. An input multiplexer (MUX) allows to measure two differential or four single-ended inputs. The high-accuracy temperature sensor can be used for system-level temperature monitoring or cold junction compensation for thermocouples.

The ADX112(Q) operates either in continuous conversion mode, or in a single-shot mode that automatically powers down after a conversion. Single-shot mode significantly reduces current consumption during idle periods. Data are transferred through a serial peripheral interface (SPI™). The ADX112(Q) is specified from –40°C to 125°C. See Table 1 for the order information.

K-Type Thermocouple Measurement
Using Integrated Temperature Sensor for Cold-Junction Compensation




Note: SPI is a trademark of Motorola, Inc.

Table 1 lists the order information.

## Table 1. Order Information

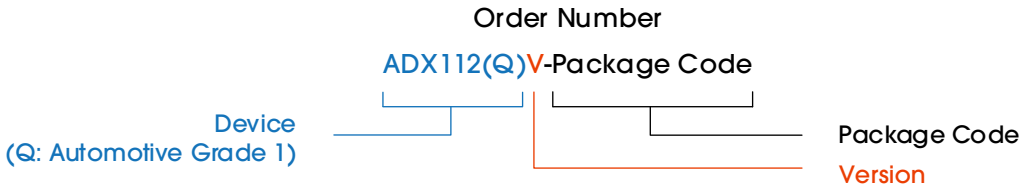
| ORDER NUMBER[1] | CH (#) | BITS | PACKAGE | BODY SIZE (mm) | MARK | ODR (SPS) | INTERFACE | COMPARATOR | TEMP SENSOR | 50/60 REJECTION | OP. TEMP (°C) | PKG. OPTION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADX112AMSOP10 | 2(4) | 16 | MSOP-10 | 3 × 3 | ADX112 | 860 | SPI | No | Yes | No | -40-125 | T/R-3000 |
| ADX112QAMSOP10[2] | 2(4) | 16 | MSOP-10 | 3 × 3 | ADX112Q | 860 | SPI | No | Yes | No | -40-125 | T/R-3000 |
| ADX112AQFN10 | 2(4) | 16 | QFN-10 | 2 × 1.5 | 112 | 860 | SPI | No | Yes | No | -40-125 | T/R-4000 |

## Table 2. Family Selection Guide

| ORDER NUMBER[1] | CH (#) | BITS | PACKAGE | BODY SIZE (mm) | MARK | ODR (SPS) | INTERFACE | COMPARATOR | TEMP SENSOR | 50/60 REJECTION | OP. TEMP (°C) | PKG. OPTION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADX111AMSOP10 | 2(4) | 16 | MSOP-10 | 3 × 3 | ADX111 | 860 | I²C | Yes | No | No | -40-125 | T/R-3000 |
| ADX111QAMSOP10[2] | 2(4) | 16 | MSOP-10 | 3 × 3 | ADX111Q | 860 | I²C | Yes | No | No | -40-125 | T/R-3000 |
| ADX111AQFN10 | 2(4) | 16 | QFN-10 | 2 × 1.5 | 111 | 860 | I²C | Yes | No | No | -40-125 | T/R-4000 |
| ADX113AMSOP10 | 2(4) | 16 | MSOP-10 | 3 × 3 | ADX113 | 860 | I²C | Yes | No | Yes | -40-125 | T/R-3000 |
| ADX114AMSOP10 | 2(4) | 16 | MSOP-10 | 3 × 3 | ADX114 | 3571 | SPI | No | Yes | Yes | -40-125 | T/R-3000 |
| ADX121AMSOP10 | 2(4) | 20 | MSOP-10 | 3 × 3 | ADX121 | 3571 | I²C | Yes | No | Yes | -40-125 | T/R-3000 |
| ADX121AQFN10[2] | 2(4) | 20 | QFN-10 | 2 × 1.5 | 121 | 3571 | I²C | Yes | No | Yes | -40-125 | T/R-4000 |
| ADX122AMSOP10 | 2(4) | 20 | MSOP-10 | 3 × 3 | ADX122 | 3571 | SPI | No | No | Yes | -40-125 | T/R-3000 |
| ADX122QAMSOP10[2] | 2(4) | 20 | MSOP-10 | 3 × 3 | ADX122Q | 3571 | SPI | No | No | Yes | -40-125 | T/R-3000 |
| ADX122AQFN10[2] | 2(4) | 20 | QFN-10 | 2 × 1.5 | 122 | 3571 | SPI | No | No | Yes | -40-125 | T/R-4000 |
| ADX128AMSOP10[2] | 2(4) | 20 | MSOP-10 | 3 × 3 | ADX128 | 7143 | SPI | No | No | Yes | -40-125 | T/R-3000 |
| ADX128AQFN10[2] | 2(4) | 20 | QFN-10 | 2 × 1.5 | 128 | 7143 | SPI | No | No | Yes | -40-125 | T/R-4000 |
| ADX125AMSOP10 | 2(4) | 20 | MSOP-10 | 3 × 3 | ADX125 | 3571 | I²C | Yes | Yes | Yes | -40-125 | T/R-3000 |
| ADX126AMSOP10 | 2(4) | 20 | MSOP-10 | 3 × 3 | ADX126 | 3571 | SPI | No | Yes | Yes | -40-125 | T/R-3000 |
| ADX125AQFN10[2] | 2(4) | 20 | QFN-10 | 2 × 1.5 | 125 | 3571 | I²C | Yes | Yes | Yes | -40-125 | T/R-4000 |
| ADX126AQFN10[2] | 2(4) | 20 | QFN-10 | 2 × 1.5 | 126 | 3571 | SPI | No | Yes | Yes | -40-125 | T/R-4000 |
| ADX131AQFN10[2] | 2(4) | 20 | QFN-10 | 2 × 1.5 | 131 | 440 | I²C | Yes | No | Yes | -40-125 | T/R-4000 |
| ADX132AQFN10[2] | 2(4) | 20 | QFN-10 | 2 × 1.5 | 132 | 440 | SPI | No | No | Yes | -40-125 | T/R-4000 |
| ADX123AMSOP10[2] | 2(4) | 20 | MSOP-10 | 3 × 3 | ADX123 | 3571 | Daisy Chain | No | No | Yes | -40-125 | T/R-3000 |

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

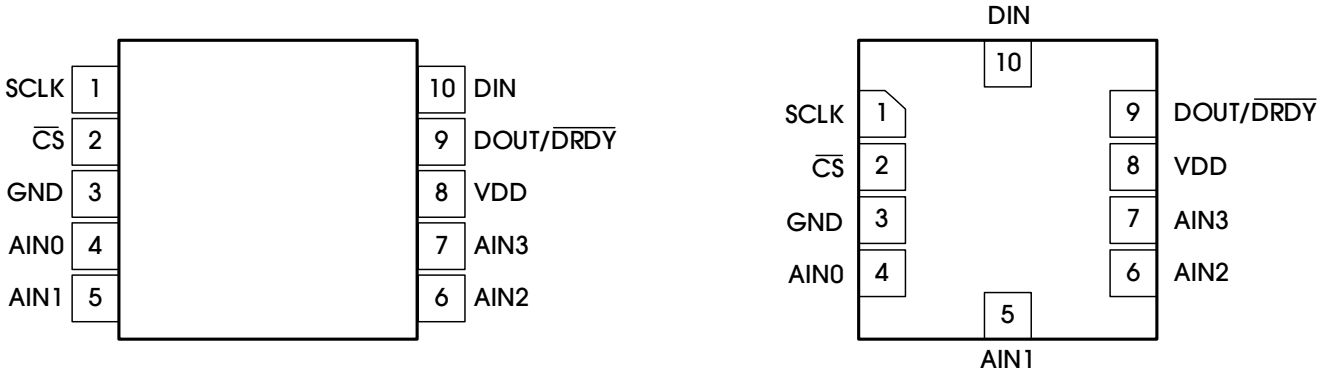
Note 1:




Note 2: Available in the future.

# 4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.




MSOP-10 Package QFN-10 Package

Figure 1. Pin Configuration

Table 3 lists the pin functions.

Table 3. Pin Functions

| NAME | POSITION | TYPE | DESCRIPTION |
|---|---|---|---|
| SCLK | 1 | Digital input | Serial clock input |
| $\overline{CS}$ | 2 | Digital input | Chip select; active low. Connect to GND if not used. |
| GND | 3 | Supply | Ground |
| AIN0 | 4 | Analog input | Analog input 0. Leave unconnected or tie to VDD if not used. |
| AIN1 | 5 | Analog input | Analog input 1. Leave unconnected or tie to VDD if not used. |
| AIN2 | 6 | Analog input | Analog input 2. Leave unconnected or tie to VDD if not used. |
| AIN3 | 7 | Analog input | Analog input 3. Leave unconnected or tie to VDD if not used. |
| VDD | 8 | Supply | Power supply. Connect a 100nF power supply decoupling capacitor to GND. |
| DOUT/$\overline{DRDY}$ | 9 | Digital output | Serial data output combined with data ready; active low. |
| DIN | 10 | Digital input | Serial data input |

# 5. SPECIFICATIONS

## 5.1 ABSOLUTE MAXIMUM RATINGS

Table 4 lists the absolute maximum ratings of the ADX112(Q).

Table 4. Absolute Maximum Ratings

| PARAMETER | DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|
| Power-Supply Voltage | VDD to GND | –0.3 | 7 | V |
| Analog Input Voltage | AIN0, AIN1, AIN2, AIN3 | GND – 0.3 | VDD + 0.3 | V |
| Digital Input Voltage | DIN, DOUT/$\overline{DRDY}$, SCLK, $\overline{CS}$ | GND – 0.3 | VDD + 0.3 | V |
| Input Current, Continuous | Any pin except power supply pins | –10 | 10 | mA |
| Temperature | Operating ambient, $T_A$ | –40 | 125 | °C |
| | Junction, $T_J$ | –40 | 150 | |
| | Storage, $T_{stg}$ | –60 | 150 | |

Note: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD RATINGS

Table 5 lists the ESD ratings of the ADX112(Q).

Table 5. ESD Ratings

| PARAMETER | SYMBOL | DESCRIPTION | VALUE | UNITS |
|---|---|---|---|---|
| Electrostatic Discharge | $V_{(ESD)}$ | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±6000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 RECOMMENDED OPERATING CONDITIONS

Table 6 lists the recommended operating conditions for the ADX112(Q).

Table 6. Recommended Operating Conditions

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Power Supply, VDD to GND | VDD | 2 | | 5.5 | V |
| ANALOG INPUTS(1) | | | | | |
| Full-Scale Input Voltage Range(2), $V_{IN} = V_{(AINP)} - V_{(AINN)}$ | FSR | See Table 13 | | | |
| Absolute Input Voltage | $V_{(AINx)}$ | GND | | VDD | V |
| DIGITAL INPUTS | | | | | |
| Input Voltage | | GND | | VDD | V |
| TEMPERATURE RANGE | | | | | |
| Operating Ambient Temperature | $T_A$ | –40 | | 125 | °C |

Note 1: $AIN_P$ and $AIN_N$ denote the selected positive and negative inputs. AINx denotes one of the four available analog inputs.
Note 2: This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3V or 5.5V (whichever is smaller) must be applied to the analog inputs of the device.

## 5.4 THERMAL INFORMATION

Table 7 lists the thermal information for the ADX112(Q).

Table 7. Thermal Information

| PARAMETER | SYMBOL | MSOP-10 | QFN-10 | UNITS |
|---|---|---|---|---|
| Junction-to-Ambient Thermal Resistance | $R_{\theta JA}$ | 150 | 119 | °C/W |
| Junction-to-Case (Top) Thermal Resistance | $R_{\theta JC(top)}$ | 54 | 60 | °C/W |
| Junction-to-Board Thermal Resistance | $R_{\theta JB}$ | 90 | 39 | °C/W |
| Junction-to-Top Characterization Parameter | $\psi_{JT}$ | 3 | 4 | °C/W |
| Junction-to-Board Characterization Parameter | $\psi_{JB}$ | 86 | 39 | °C/W |
| Junction-to-Case (Bottom) Thermal Resistance | $R_{\theta JC(bot)}$ | 90 | 45 | °C/W |

## 5.5 ELECTRICAL CHARACTERISTICS

Table 8 lists the electrical characteristics of ADX112(Q). Maximum and minimum specifications apply from $T_A$ = –40°C to 125°C. Typical specifications are at $T_A$ = 25°C. All specifications are at VDD = 3.3V, data rate = 8SPS, and full-scale range (FSR) = ±2.048V, unless otherwise noted.

Table 8. Electrical Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| ANALOG INPUTS | | | | | | |
| Common-Mode Input Impedance | | FSR = ±6.144V(1) | | 9 | | MΩ |
| | | FSR = ±4.096V(1) | | 7 | | |
| | | FSR = ±2.048V | | 6 | | |
| | | FSR = ±1.024V | | 5 | | |
| | | FSR = ±0.512V, FSR = ±0.256V | | 6 | | |
| Differential Input Impedance | | FSR = ±6.144V(1) | | 26 | | MΩ |
| | | FSR = ±4.096V(1) | | 17 | | |
| | | FSR = ±2.048V | | 3 | | |
| | | FSR = ±1.024V | | 1.5 | | |
| | | FSR = ±0.512V, FSR = ±0.256V | | 0.9 | | |
| SYSTEM PERFORMANCE | | | | | | |
| Resolution (No Missing Codes) | | | 16 | | | Bits |
| Data Rate | DR | | 8, 16, 32, 64, 128, 250, 475, 860 | | | SPS |
| Data Rate Variation | | All data rates | –10% | | 10% | |
| Output Noise | | | See NOISE PERFORMANCE section | | | |
| Integral Nonlinearity | INL | DR = 8SPS, FSR = ±2.048V(2) | | 0.5 | 1 | LSB |
| Offset Error | | FSR = ±2.048V, differential inputs | | ±0.1 | ±1.5 | LSB |
| | | FSR = ±2.048V, single-ended inputs | | –0.5 | | |
| Offset Drift(3) | | FSR = ±2.048V | | 0.002 | | LSB/°C |
| Offset Power-Supply Rejection | | FSR = ±2.048V, DC supply variation | | 0.2 | | LSB/V |
| Offset Channel Match | | Match between any two inputs | | 0.5 | | LSB |
| Gain Error(4) | | FSR = ±2.048V, $T_A$ = 25°C | | 0.01% | 0.1% | |
| Gain Drift(3)(4) | | FSR = ±0.256V | | 8 | | ppm/°C |
| | | FSR = ±2.048V | | 8 | 30 | |
| | | FSR = ±6.144V(1) | | 8 | | |
| Gain Power-Supply Rejection | | VDD = 3.3V to 5V | | 70 | | ppm/V |
| Gain Match(4) | | Match between any two gains | | 0.01% | 0.1% | |
| Gain Channel Match | | Match between any two inputs | | 0.01% | 0.1% | |
| Common-Mode Rejection Ratio | CMRR | At DC, FSR = ±0.256V | | > 110 | | dB |
| | | At DC, FSR = ±2.048V | | > 105 | | |
| | | At DC, FSR = ±6.144V(1) | | 100 | | |
| | | $f_{CM}$ = 50Hz | | 103 | | |
| | | $f_{CM}$ = 60Hz | | 104 | | |
| TEMPERATURE SENSOR | | | | | | |
| Temperature Range | | | –40 | | 125 | °C |
| Temperature Resolution | | | | 0.03125 | | °C/LSB |
| Accuracy | | $T_A$ = 0°C to 70°C | | 0.2 | ±0.5 | °C |
| | | $T_A$ = –40°C to 125°C | | 0.4 | ±1 | |
| | | vs. supply | | 0.03125 | ±0.25 | °C/V |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| DIGITAL INPUTS/OUTPUTS | | | | | | |
| High-Level Input Voltage | $V_{IL}$ | | 0.7 VDD | | VDD | V |
| Low-Level Input Voltage | $V_{IL}$ | | GND | | 0.3 VDD | V |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$ = 1mA | 0.8 VDD | | | V |
| Low-Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 1mA | GND | | 0.2 VDD | V |
| Input Leakage, High | $I_H$ | $V_{IL}$ = 5.5V | –10 | | 10 | μA |
| Input Leakage, Low | $I_L$ | $V_{IL}$ = GND | –10 | | 10 | μA |
| POWER SUPPLY | | | | | | |
| Supply Current | $I_{VDD}$ | Power down, $T_A$ = 25°C | | 0.65 | 1 | μA |
| | | Power down | | | 3.5 | |
| | | Operating, $T_A$ = 25°C | | 145 | 170 | |
| | | Operating | | | 300 | |
| Power Dissipation | $P_D$ | VDD = 5V | | 0.9 | | mW |
| | | VDD = 3.3V | | 0.5 | | |
| | | VDD = 2V | | 0.3 | | |

Note 1: This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3V or 5.5V (whichever is smaller) must be applied to this device.
Note 2: Best-fit INL; covers 98% of full-scale.
Note 3: Maximum value specified by characterization.
Note 4: Includes all errors from onboard PGA and voltage reference.

## 5.6 TIMING REQUIREMENTS: SERIAL INTERFACE

Table 9 lists the timing requirements for the serial interface. VDD = 2.0V to 5.5V, unless otherwise noted.

Table 9. Timing Requirements: Serial Interface

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Delay Time, $\overline{CS}$ Falling Edge to First SCLK Rising Edge(1) | $t_{CSSC}$ | 100 | | ns |
| Delay Time, Final SCLK Falling Edge to $\overline{CS}$ Rising Edge | $t_{SCCS}$ | 100 | | ns |
| Pulse Duration, $\overline{CS}$ High | $t_{CSH}$ | 200 | | ns |
| SCLK Period | $t_{SCLK}$ | 250 | | ns |
| Pulse Duration, SCLK High | $t_{SPWH}$ | 100 | | ns |
| Pulse Duration, SCLK Low(2) | $t_{SPWL}$ | 100 | | ns |
| | | | 28 | ms |
| Setup Time, DIN Valid before SCLK Falling Edge | $t_{DIST}$ | 50 | | ns |
| Hold Time, DIN Valid after SCLK Falling Edge | $t_{DIHD}$ | 50 | | ns |
| Hold Time, SCLK Rising Edge to DOUT Invalid | $t_{DOHD}$ | 0 | | ns |

Note 1: $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.
Note 2: Holding SCLK low longer than 28ms resets the SPI interface.

## 5.7 SWITCHING CHARACTERISTICS: SERIAL INTERFACE

Table 10 lists the switching characteristics of serial interface.

Table 10. Switching Characteristics: Serial Interface

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Propagation Delay Time, $\overline{CS}$ Falling Edge to DOUT Driven | $t_{CSDOD}$ | DOUT load = 20pF \| \| 100kΩ to GND | | | 100 | ns |
| Propagation Delay Time, SCLK Rising Edge to Valid New DOUT | $t_{DOPD}$ | DOUT load = 20pF \| \| 100kΩ to GND | 0 | | 50 | ns |
| Propagation Delay Time, $\overline{CS}$ Rising Edge to DOUT High Impedance | $t_{CSDOZ}$ | DOUT load = 20pF \| \| 100kΩ to GND | | | 100 | ns |

Figure 2 shows the serial interface timing.

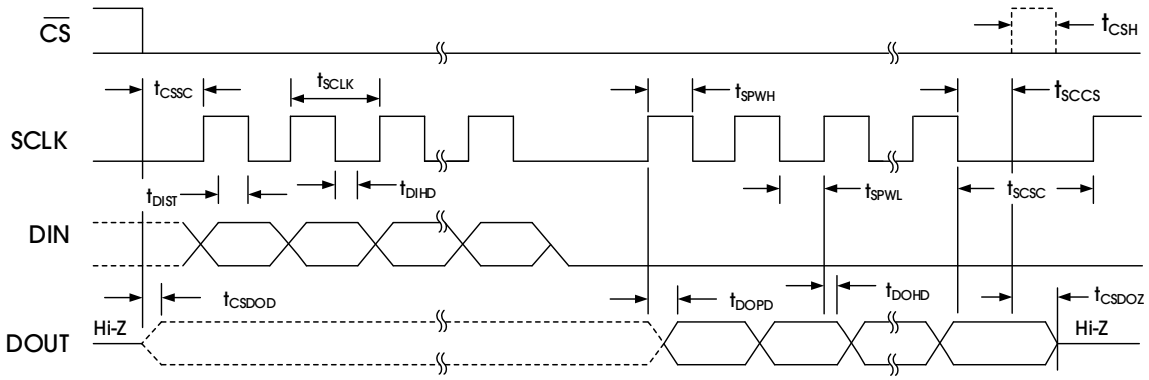



Figure 2. Serial Interface Timing

## 5.8 TYPICAL CHARACTERISTICS

$T_A$ = 25°C, VDD = 3.3V, FSR = ±2.048V, unless otherwise noted.

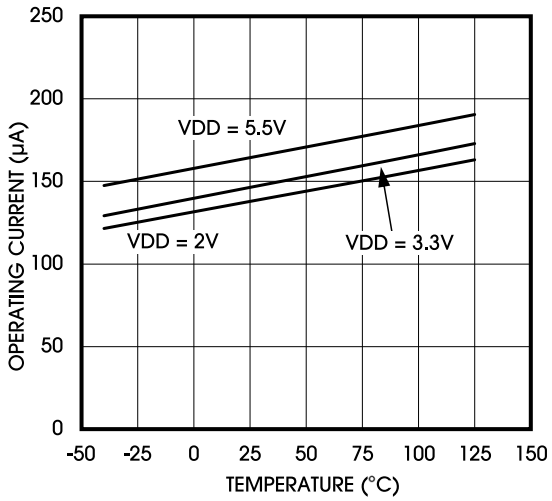



Figure 3. Operating Current vs. Temperature

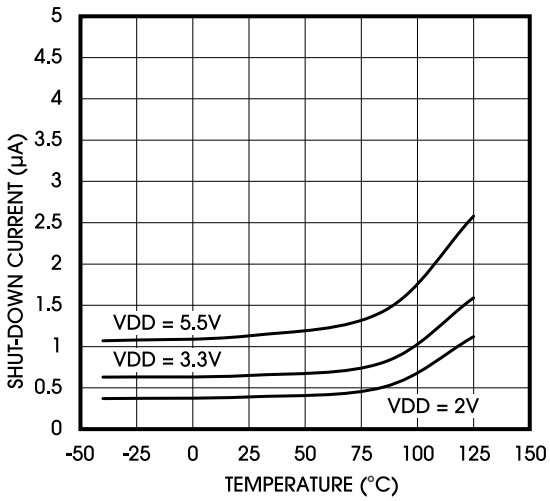



Figure 4. Power-Down Current vs. Temperature

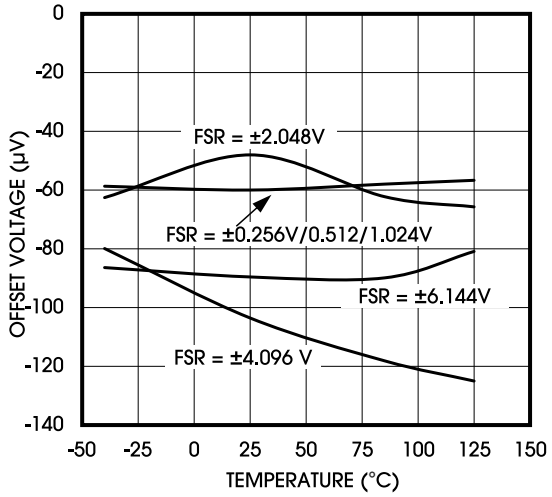



Figure 5. Single-Ended Offset Error vs. Temperature

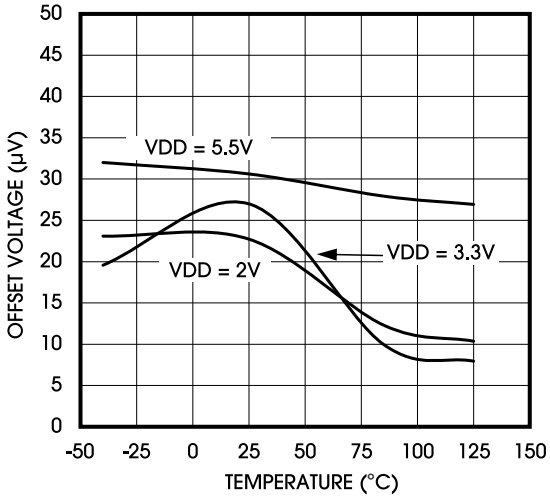



Figure 6. Differential Offset vs. Temperature

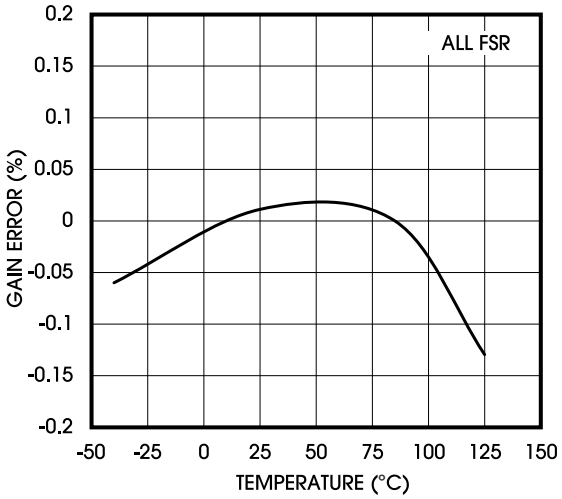



Figure 7. Gain Error vs. Temperature

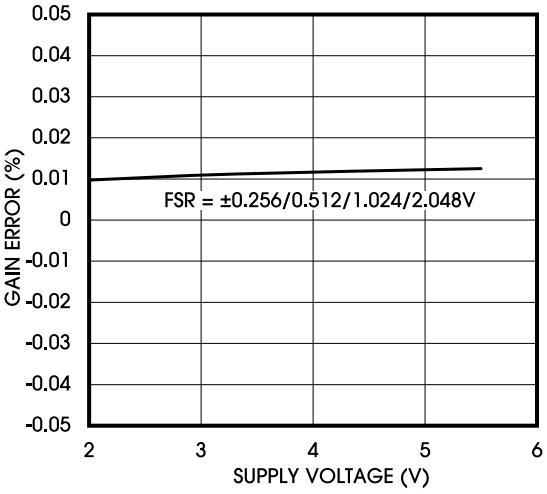



Figure 8. Gain Error vs. Supply Voltage

## 5.9 TYPICAL CHARACTERISTICS (CONTINUED)

$T_A$ = 25°C, VDD = 3.3V, FSR = ±2.048V, unless otherwise noted.

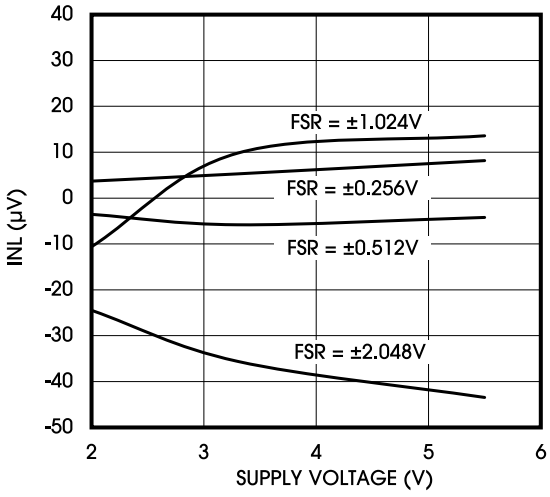



Figure 9. INL vs. Supply Voltage

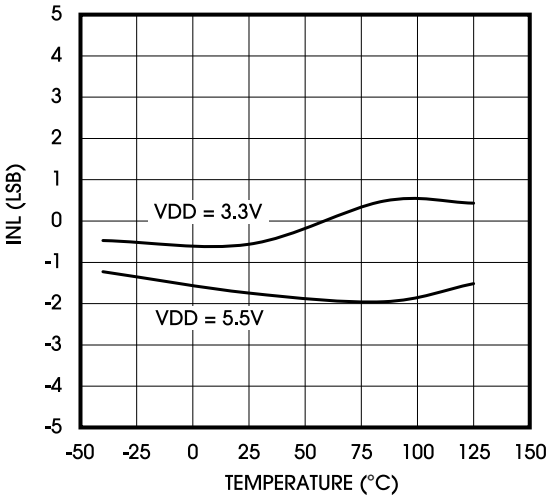



Figure 10. INL vs. Temperature

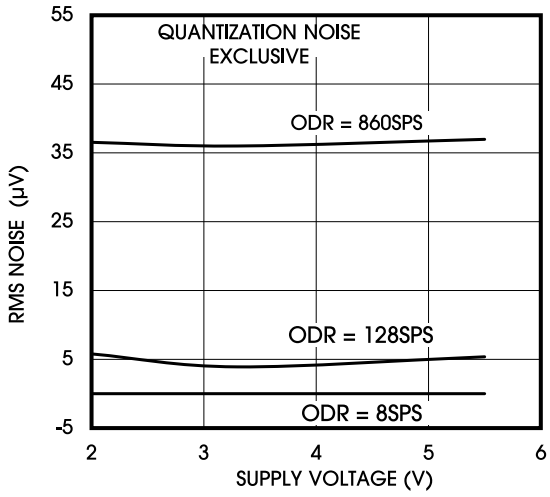



Figure 11. Noise vs. Supply voltage

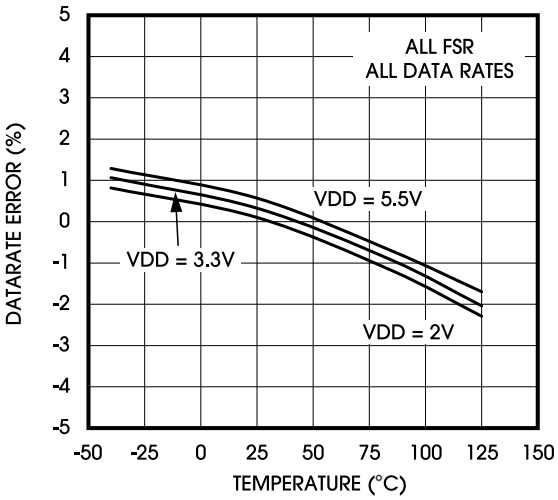



Figure 12. Data Rate vs. Temperature

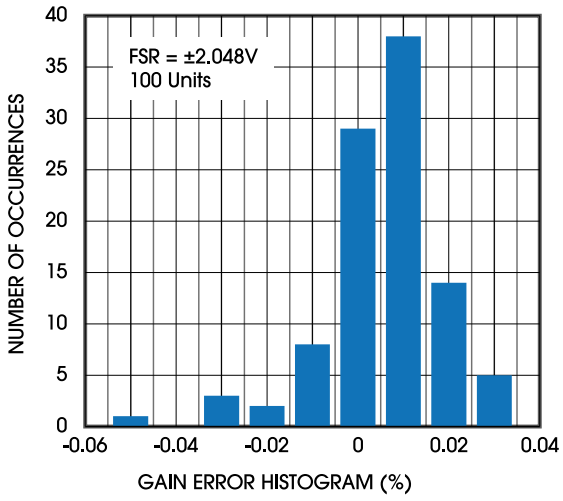



Figure 13. Gain Error Histogram

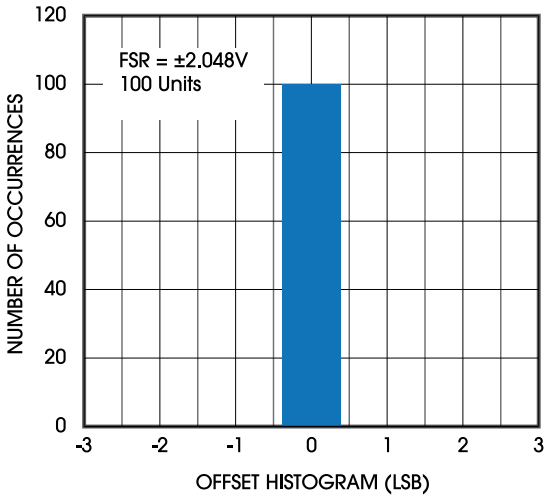



Figure 14. Offset Histogram

## 5.10 TYPICAL CHARACTERISTICS (CONTINUED)

$T_A$ = 25°C, VDD = 3.3V, FSR = ±2.048V, unless otherwise noted.

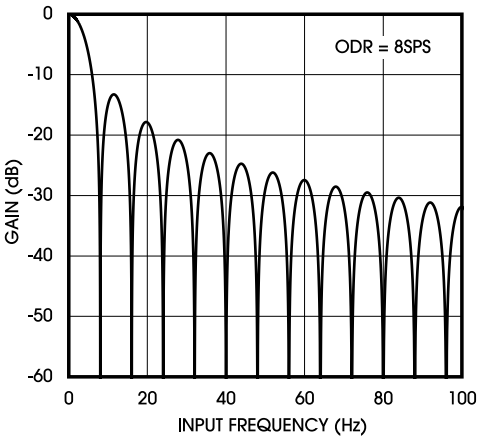



Figure 15. Digital Filter Frequency Response

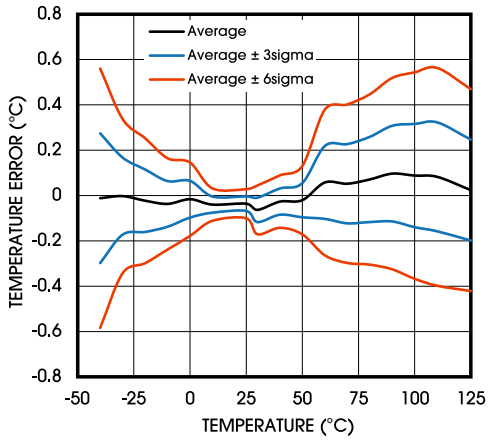



Figure 16. Temperature Sensor Error vs. Temperature

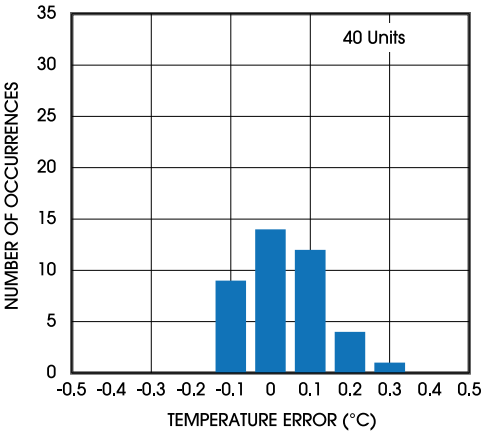



Figure 17. Temperature Sensor Error Histogram –40°C

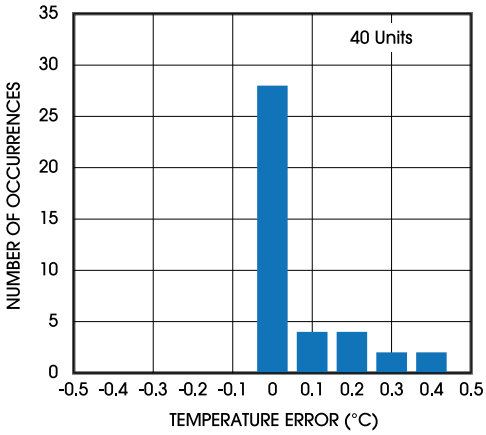



Figure 18. Temperature Sensor Error Histogram 0°C

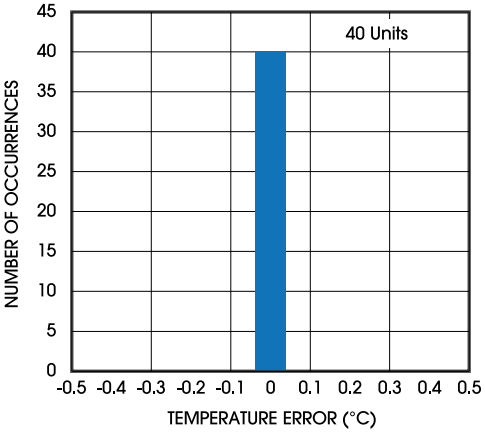



Figure 19. Temperature Sensor Error Histogram 25°C

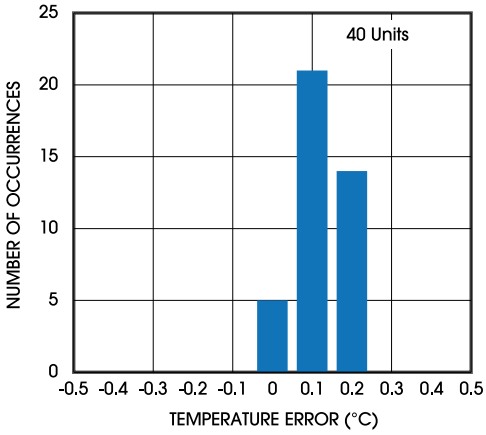



Figure 20. Temperature Sensor Error Histogram 80°C

## 5.11 TYPICAL CHARACTERISTICS (CONTINUED)

$T_A$ = 25°C, VDD = 3.3V, FSR = ±2.048V, unless otherwise noted.

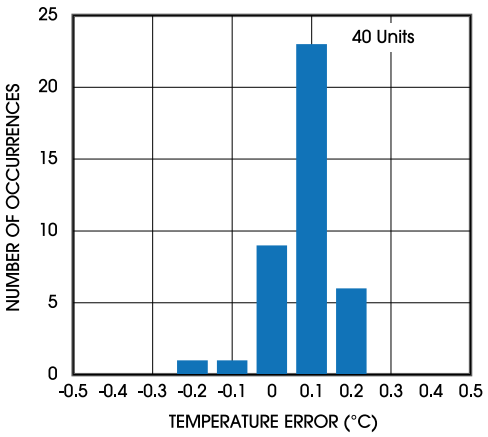



Figure 21. Temperature Sensor Error Histogram 125°C

# 6. PARAMETER MEASUREMENT INFORMATION

## 6.1 NOISE PERFORMANCE

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called oversampling ratio (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Table 11 and Table 12 summarize the device noise performance. Data are representative of typical noise performance at $T_A$ = 25°C with the inputs shorted together externally. Table 11 shows the input-referred noise in units of $\mu V_{RMS}$ for the conditions shown. Note that $\mu V_{PP}$ values are shown in parenthesis. Table 12 shows the corresponding data in effective number of bits (ENOB) calculated from $\mu V_{RMS}$ values using Equation 1. The noise-free bits calculated from peak-to-peak noise values using Equation 2 are shown in parenthesis.

$$ENOB = \ln (FSR / V_{RMS\text{-}Noise}) / \ln(2) \quad (1)$$

$$Noise\text{-}Free\ Bits = \ln (FSR / V_{PP\text{-}Noise}) / \ln (2) \quad (2)$$

Table 11. Noise in $\mu V_{RMS}$ ($\mu V_{PP}$) at VDD = 3.3V

| DATA RATE (SPS) | FSR (FULL-SCALE RANGE) | | | | | |
|---|---|---|---|---|---|---|
| | ±6.144V | ±4.096V | ±2.048V | ±1.024V | ±0.512V | ±0.256V |
| 8 | 187.5 (187.5) | 125 (125) | 62.5 (62.5) | 31.25 (31.25) | 15.625 (15.625) | 7.8125 (7.8125) |
| 16 | 187.5 (187.6) | 125 (125) | 62.5 (62.5) | 31.25 (31.25) | 15.625 (15.625) | 7.8125 (7.8125) |
| 32 | 187.5 (187.7) | 125 (125) | 62.5 (62.5) | 31.25 (31.25) | 15.625 (15.625) | 7.8125 (7.8125) |
| 64 | 187.5 (187.8) | 125 (125) | 62.5 (62.5) | 31.25 (31.25) | 15.625 (15.625) | 7.8125 (13.889) |
| 128 | 187.5 (187.9) | 125 (125) | 62.5 (62.5) | 31.25 (31.25) | 15.625 (17.333) | 7.8125 (15.625) |
| 250 | 187.5 (375) | 125 (250) | 62.5 (125) | 31.25 (62.5) | 15.625 (31.25) | 7.8125 (23.4375) |
| 475 | 187.5 (375) | 125 (250) | 62.5 (125) | 31.25 (62.5) | 15.625 (31.25) | 7.8125 (32.986) |
| 860 | 187.5 (520.8) | 125 (319.4) | 62.5 (152.7) | 31.25 (90.2) | 15.625 (38.19) | 8.6799 (45.138) |

Table 12. ENOB from RMS Noise (Noise-Free Bits from Peak-to-Peak Noise) at VDD = 3.3V

| DATA RATE (SPS) | FSR (FULL-SCALE RANGE) | | | | | |
|---|---|---|---|---|---|---|
| | ±6.144V | ±4.096V | ±2.048V | ±1.024V | ±0.512V | ±0.256V |
| 8 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) |
| 16 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) |
| 32 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) |
| 64 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (15.17) |
| 128 | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (15.85) | 16 (15) |
| 250 | 16 (15) | 16 (15) | 16 (15) | 16 (15) | 16 (15) | 16 (14.41) |
| 475 | 16 (15) | 16 (15) | 16 (15) | 16 (15) | 16 (15) | 16 (13.92) |
| 860 | 16 (14.52) | 16 (14.64) | 16 (14.7) | 16 (14.47) | 16 (14.71) | 15.9 (13.47) |

# 7. DETAILED DESCRIPTION

## 7.1 OVERVIEW

The ADX112(Q) is a very small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADX112(Q) consists of a ΔΣ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an SPI. This device is also a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. FUNCTIONAL BLOCK DIAGRAM shows the ADX112(Q) functional block diagram.

The ADX112(Q) ADC core measures a differential signal, $V_{IN}$, which is the difference of $V_{(AINP)}$ and $V_{(AINN)}$. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation in any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADX112(Q) has two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal conversion register. The device then enters a power-down state. This mode is intended to provide significant power savings in systems that require only periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

## 7.2 FUNCTIONAL BLOCK DIAGRAM

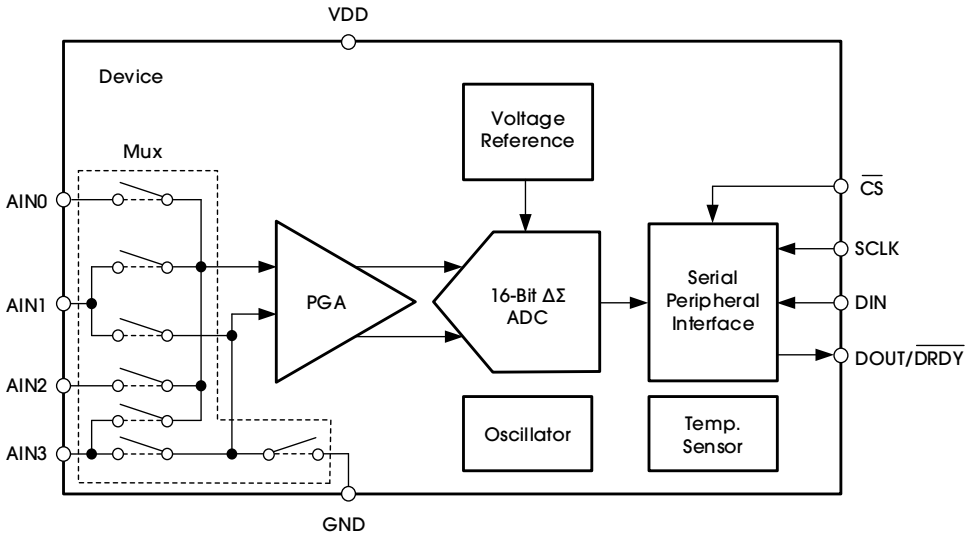



Figure 22. Functional Block Diagram

# 7.3 FEATURE DESCRIPTION

## 7.3.1 MULTIPLEXER

The ADX112(Q) contains an input multiplexer (mux), as shown in Figure 23. Either four single-ended or two differential signals can be measured. Additionally, AIN0, AIN1, and AIN2 can be measured differentially to AIN3. The multiplexer is configured by bits MUX(2:0) in the CONFIG REGISTER. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

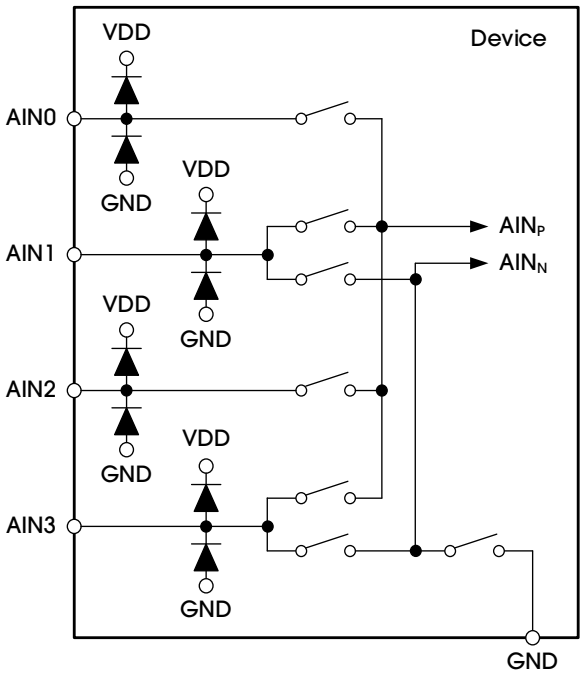



Figure 23. Input Multiplexer

When measuring single-ended inputs, the device does not output negative codes. These negative codes indicate negative differential signals; that is, $(V_{(AINP)} - V_{(AINN)}) < 0$. Electrostatic discharge (ESD) diodes to VDD and GND protect the ADX112(Q) inputs. To prevent the ESD diodes from turning on, keep the absolute voltage on any input within the range given in Equation 3:

$$GND - 0.3V < V_{(AINx)} < VDD + 0.3V \quad (3)$$

If the voltages on the input pins can possibly violate these conditions, use external Schottky diodes and series resistors to limit the input current to safe values (see Table 4).

Also, overdriving one unused input on the ADX112(Q) may affect conversions currently taking place on other input pins. If overdriving unused inputs is possible, clamp the signal with external Schottky diodes.

### 7.3.2 ANALOG INPUTS

The ADX112(Q) uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between $AIN_P$ and $AIN_N$. This frequency at which the input signal is sampled is called the sampling frequency or the modulator frequency ($f_{(MOD)}$). The ADX112(Q) has a 1MHz internal oscillator which is further divided by a factor of 4 to generate the modulator frequency at 250kHz. The capacitors used in this input stage are small, and to external circuitry, the average loading appears resistive. This structure is shown in Figure 24. The resistance is set by the capacitor values and the rate at which they are switched. Figure 25 shows the setting of the switches illustrated in Figure 24. During the sampling phase, switches $S_1$ are closed. This event charges $C_{A1}$ to $V_{(AINP)}$, $C_{A2}$ to $V_{(AINN)}$, and $C_B$ to ($V_{(AINP)}$ – $V_{(AINN)}$). During the discharge phase, $S_1$ is first opened and then $S_2$ is closed. Both $C_{A1}$ and $C_{A2}$ then discharge to approximately 0.7V and $C_B$ discharges to 0V. This charging draws a very small transient current from the source driving the ADX112(Q) analog inputs. The average value of this current can be used to calculate the effective impedance ($Z_{eff}$), where $Z_{eff} = V_{IN} / I_{AVERAGE}$.

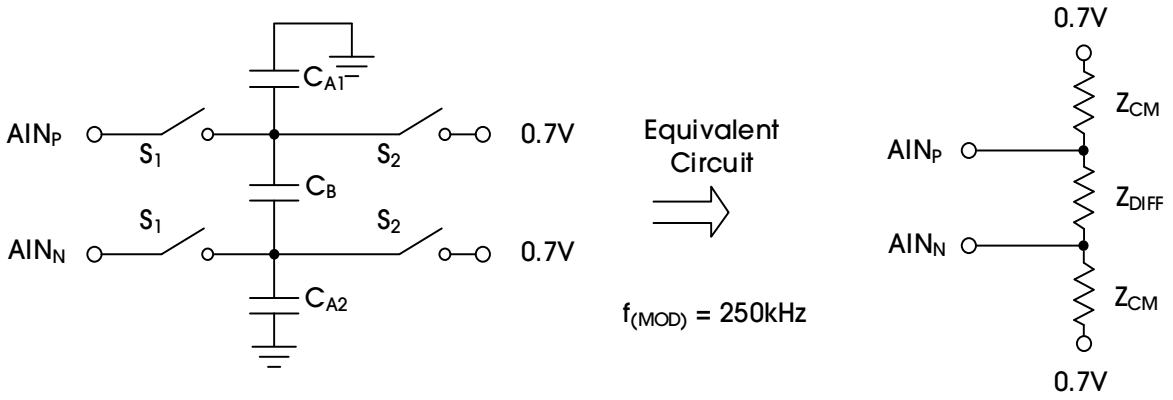



Figure 24. Simplified Analog Input Circuit

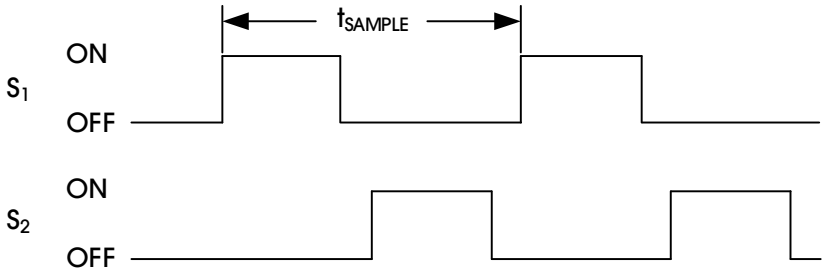



Figure 25. $S_1$ and $S_2$ Switch Timing

The common-mode input impedance is measured by applying a common-mode signal to the shorted $AIN_P$ and $AIN_N$ inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the full-scale range, but is approximately 6MΩ for the default full-scale range. In Figure 24, the common-mode input impedance is $Z_{CM}$.

The differential input impedance is measured by applying a differential signal to $AIN_P$ and $AIN_N$ inputs where one input is held at 0.7V. The current that flows through the pin connected to 0.7V is the differential current and scales with the full-scale range. In Figure 24, the differential input impedance is $Z_{DIFF}$.

Make sure to consider the typical value of the input impedance. Unless the input source has a low impedance, the ADX112(Q) input impedance may affect the measurement accuracy. For sources with high-output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

The clock oscillator frequency drifts slightly with temperature; therefore, the input impedances also drift. For most applications, this input impedance drift is negligible, and can be ignored.

### 7.3.3 FULL-SCALE RANGE (FSR) AND LSB SIZE

A programmable gain amplifier (PGA) is implemented before the ADX112(Q) ΔΣ core. The full-scale range is configured by three bits (PGA(2:0)) in the CONFIG REGISTER and can be set to ±6.144V, ±4.096V, ±2.048V, ±1.024V, ±0.512V, and ±0.256V. Table 13 shows the FSR together with the corresponding LSB size. LSB size is calculated from full-scale voltage by the formula shown in Equation 4. However, analog input voltages may never exceed the analog input voltage limits given in the ELECTRICAL CHARACTERISTICS. If a supply voltage of VDD greater than 4V is used, the ±6.144V full-scale range allows input voltages to extend up to the supply. Note though that in this case, or whenever the supply voltage is less than the full-scale range (for example, VDD = 3.3V and full-scale range = ±4.096V), a full-scale ADC output code cannot be obtained. This inability means that some dynamic range is lost.

$$LSB = FSR / 2^{16} \quad (4)$$

Table 13. Full-Scale Range and Corresponding LSB Size

| FSR | LSB SIZE |
|---|---|
| ±6.144V(1) | 187.5μV |
| ±4.096V(1) | 125μV |
| ±2.048V | 62.5μV |
| ±1.024V | 31.25μV |
| ±0.512V | 15.625μV |
| ±0.256V | 7.8125μV |

Note: This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3V must be applied to this device.

Analog input voltages must never exceed the analog input voltage limits given in the ABSOLUTE MAXIMUM RATINGS. If a VDD supply voltage is lower than the selected full-scale range, a full-scale ADC output code cannot be obtained. For example, with VDD = 3.3V and FSR = ±4.096V, only signals up to $V_{IN}$ = ±3.3V can be measured. The code range that represents voltages of $|V_{IN}| > 3.3V$ is not used in this case.

It is highly recommended to use full-scale range one step higher than VDD supply voltage as the maximum full-scale range. For example, VDD = 2V, and ±2.048V are the best settings for a maximum full-scale range. Full-scale range larger than ±2.048V has no benefit.

### 7.3.4 VOLTAGE REFERENCE

The ADX112(Q) has an integrated voltage reference. An external reference cannot be used with this device. Errors associated with the initial voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the ELECTRICAL CHARACTERISTICS.

### 7.3.5 OSCILLATOR

The ADX112(Q) has an integrated oscillator running at 1MHz. No external clock is required to operate the device. Note that the internal oscillator drifts over temperature and time. The output data rate will scale proportional with the oscillator frequency.

### 7.3.6 OUTPUT DATA RATE AND CONVERSION TIME

The ADX112(Q) offers programmable output data rates. Use the DR(2:0) bits in the CONFIG REGISTER to select output data rates of 8SPS, 16SPS, 32SPS, 64SPS, 128SPS, 250SPS, 475SPS, or 860SPS.

Conversions in the ADX112(Q) settle within a single cycle; thus, the conversion time is equal to 1 / DR.

### 7.3.7 TEMPERATURE SENSOR

The ADX112(Q) offers an integrated precision temperature sensor. The temperature sensor mode is enabled by setting bit TS_MODE = 1 in the CONFIG REGISTER. Temperature data are represented as a 14-bit result that is left-justified within the 16-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 14 bits are used to indicate the temperature measurement result. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary two's complement format, as shown in Table 14.

Table 14. 14-Bit Temperature Data Format

| TEMPERATURE (°C) | DIGITAL OUTPUT (BINARY) | HEX |
|---|---|---|
| 128 | 01 0000 0000 0000 | 1000 |
| 127.96875 | 00 1111 1111 1111 | 0FFF |
| 100 | 00 1100 1000 0000 | 0C80 |
| 75 | 00 1001 0110 0000 | 0960 |
| 50 | 00 0110 0100 0000 | 0640 |
| 25 | 00 0011 0010 0000 | 0320 |
| 0.25 | 00 0000 0000 1000 | 0008 |
| 0.03125 | 00 0000 0000 0001 | 0001 |
| 0 | 00 0000 0000 0000 | 0000 |
| –0.25 | 11 1111 1111 1000 | 3FF8 |
| –25 | 11 1100 1110 0000 | 3CE0 |
| –40 | 11 1011 0000 0000 | 3B00 |

#### 7.3.7.1 CONVERTING FROM TEMPERATURE TO DIGITAL CODES

For positive temperatures:
Two's complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 14-bit, left-justified format with the MSB = 0 to denote the positive sign.
Example: 50°C / (0.03125°C/count) = 1600 = 0640h = 00 0110 0100 0000

For negative temperatures:
Generate the two's complement of a negative number by complementing the absolute binary number and adding 1. Then denote the negative sign with the MSB = 1.
Example: |–25°C| / (0.03125°C/count) = 800 = 0320h = 00 0011 0010 0000
Two's complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

#### 7.3.7.2 CONVERTING FROM DIGITAL CODES TO TEMPERATURE

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by 0.03125°C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all of the bits. Then multiply the result by –0.03125°C.
Example: The device reads back 0960h: 0960h has an MSB = 0.
0960h × 0.03125°C = 2400 × 0.03125°C = 75°C

Example: The device reads back 3CE0h: 3CE0h has an MSB = 1.
Subtract 1 and complement the result: 3CE0h to 0320h
0320h × (–0.03125°C) = 800 × (–0.03125°C) = –25°C

# 7.4 DEVICE FUNCTIONAL MODES

## 7.4.1 RESET AND POWER-UP

When the ADX112(Q) powers up, a reset is performed. As part of the reset process, the ADX112(Q) sets all of its bits in the CONFIG REGISTER to the respective default settings. By default, the ADX112(Q) enters a power-down state at start-up. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADX112(Q) is intended to relieve systems with tight power-supply requirements from encountering a surge during power-up. It takes 500us to be ready from power-up.

## 7.4.2 OPERATING MODES

The ADX112(Q) operates in one of two modes: continuous-conversion or single-shot. The MODE bit in the CONFIG REGISTER selects the respective operating mode.

### 7.4.2.1 SINGLE-SHOT MODE AND POWER-DOWN

When the MODE bit in the CONFIG REGISTER is set to 1, the ADX112(Q) enters a power-down state, and operates in single-shot mode. This power-down state is the default state for the ADX112(Q) when power is first applied. Although powered down, the device still responds to commands. The ADX112(Q) remains in this power-down state until a 1 is written to the single-shot (SS) bit in the CONFIG REGISTER. When the SS bit is asserted, the device powers up, resets the SS bit to 0, and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. Writing a 1 to the SS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0 to the MODE bit in the CONFIG REGISTER.

### 7.4.2.2 CONTINUOUS-CONVERSION MODE

In continuous-conversion mode (MODE bit set to 0), the ADX112(Q) continuously performs conversions. When a conversion completes, the ADX112(Q) places the result in the CONVERSION REGISTER and immediately begins another conversion. To switch to single-shot mode, write a 1 to the MODE bit in the CONFIG REGISTER, or reset the device.

### 7.4.2.3 DUTY CYCLING FOR LOW POWER

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator can be averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the ADX112(Q) supports duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADX112(Q) in power-down state with a data rate set to 860SPS can be operated by a microcontroller that instructs a single-shot conversion every 125ms (8SPS). Because a conversion at 860SPS only requires approximately 1.2ms, the ADX112(Q) enters power-down state for the remaining 123.8ms. In this configuration, the ADX112(Q) consumes approximately 1/100th the power that is otherwise consumed in continuous conversion mode. The duty cycling rate is completely arbitrary and is defined by the master controller. The ADX112(Q) offers lower data rates that do not implement duty cycling and also offers improved noise performance if required.

# 7.5 PROGRAMMING

## 7.5.1 SERIAL INTERFACE

The SPI-compatible serial interface consists of either four signals ($\overline{CS}$, SCLK, DIN, and DOUT/$\overline{DRDY}$), or three signals (in which case $\overline{CS}$ may be tied low). The interface is used to read conversion data, read and write registers, and control device operation.

## 7.5.2 CHIP SELECT ($\overline{CS}$)

The chip select pin ($\overline{CS}$) selects the ADX112(Q) for SPI communication. This feature is useful when multiple devices share the same serial bus. Keep $\overline{CS}$ low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT/$\overline{DRDY}$ enters a high-impedance state. In this state, DOUT/$\overline{DRDY}$ cannot provide data-ready indication. In situations where multiple devices are present and DOUT/$\overline{DRDY}$ must be monitored, lower $\overline{CS}$ periodically. At this point, the DOUT/$\overline{DRDY}$ pin either immediately goes high to indicate that no new data are available, or immediately goes low to indicate that new data are present in the CONVERSION REGISTER and are available for transfer. New data can be transferred at any time without concern of data corruption. When a transmission starts, the current result is locked into the output shift register and does not change until the communication completes. This system avoids any possibility of data corruption.

## 7.5.3 SERIAL CLOCK (SCLK)

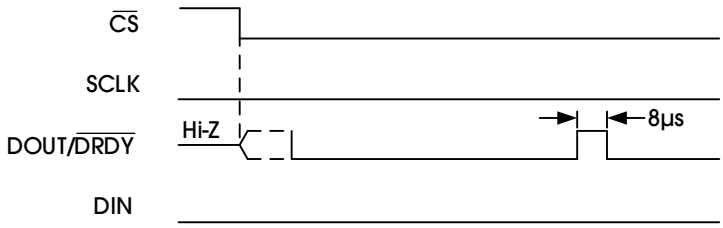
The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT/$\overline{DRDY}$ pins into and out of the ADX112(Q). Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. If SCLK is held low for 28ms, the serial interface resets and the next SCLK pulse starts a new communication cycle. This time-out feature can be used to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

## 7.5.4 DATA INPUT (DIN)

The data input pin (DIN) is used along with SCLK to send data to the ADX112(Q). The device latches data on DIN on the SCLK falling edge. The ADX112(Q) never drives the DIN pin.

### 7.5.5 DATA OUTPUT AND DATA READY (DOUT/$\overline{\text{DRDY}}$)

The data output and data ready pin (DOUT/$\overline{\text{DRDY}}$) is used with SCLK to read conversion and register data from the ADX112(Q). Data on DOUT/$\overline{\text{DRDY}}$ are shifted out on the SCLK rising edge. DOUT/$\overline{\text{DRDY}}$ is also used to indicate that a conversion is complete and new data are available. This pin transitions low when new data are ready for retrieval. DOUT/$\overline{\text{DRDY}}$ is also able to trigger a microcontroller to start reading data from the ADX112(Q). In continuous-conversion mode, DOUT/$\overline{\text{DRDY}}$ transitions high again 8µs before the next data ready signal (DOUT/$\overline{\text{DRDY}}$ low) if no data are retrieved from the device. This transition is shown in Figure 26. Complete the data transfer before DOUT/$\overline{\text{DRDY}}$ returns high.




Note: $\overline{\text{CS}}$ may be held low. If $\overline{\text{CS}}$ is low, DOUT/$\overline{\text{DRDY}}$ asserts low indicating new data are available.

Figure 26. DOUT/$\overline{\text{DRDY}}$ Behavior without Data Retrieval in Continuous Conversion Mode

When $\overline{\text{CS}}$ is high, DOUT/$\overline{\text{DRDY}}$ is configured by default with a weak internal pullup resistor. This feature reduces the risk of DOUT/$\overline{\text{DRDY}}$ floating near mid-supply and causing leakage current in the master device. To disable this pullup resistor and place the device into a high-impedance state, set the PULL_UP_EN bit to 0 in the CONFIG REGISTER.

### 7.5.6 DATA FORMAT

The ADX112(Q) provides 16 bits of data in binary two's complement format. A positive full-scale input produces an output code of 7FFFh and a negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 15 summarizes the ideal output codes for different input signals.

Table 15. Input Signal versus Ideal Output Code

| INPUT SIGNAL, $V_{IN}$ ($AIN_P$ – $AIN_N$) | IDEAL OUTPUT CODE (EXCLUDES THE EFFECTS OF NOISE, INL, OFFSET, AND GAIN ERRORS) |
|---|---|
| ≥ +FS ($2^{15}$ – 1) / $2^{15}$ | 7FFFh |
| +FS / $2^{15}$ | 0001h |
| 0 | 0 |
| –FS / $2^{15}$ | FFFFh |
| ≤ –FS | 8000h |

Figure 27 shows code transitions versus input voltage.

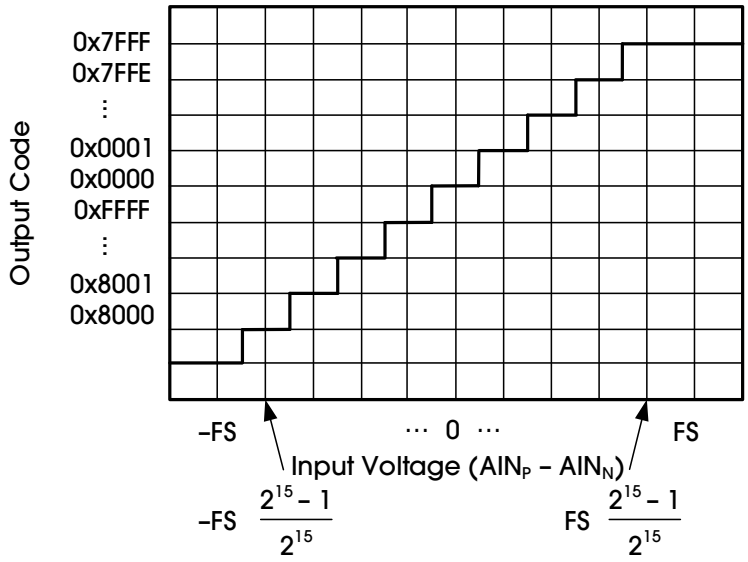



Figure 27. ADX112(Q) Code Transition Diagram

## 7.5.7 DATA RETRIEVAL

Data is written to and read from the ADX112(Q) in the same manner for both single-shot and continuous conversion modes, without having to issue any commands. The operating mode for the ADX112(Q) is selected by the MODE bit in the CONFIG REGISTER.

Set the MODE bit to 0 to put the device in continuous-conversion mode. In continuous-conversion mode, the device is constantly starting new conversions even when $\overline{CS}$ is high. Set the MODE bit to 1 for single-shot mode. In single-shot mode, a new conversion only starts by writing a 1 to the SS bit.

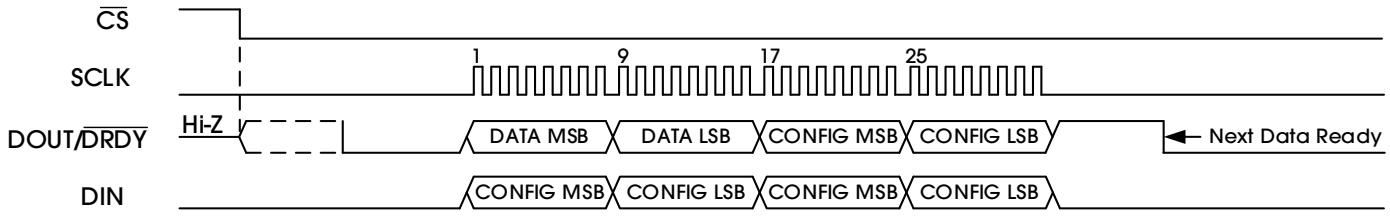
The conversion data are always buffered, and retain the current data until replaced by new conversion data. Therefore, data can be read at any time without concern of data corruption. When DOUT/$\overline{DRDY}$ asserts low, indicating that new conversion data are ready, the conversion data are read by shifting the data out on DOUT/$\overline{DRDY}$. The MSB of the data (bit 15) on DOUT/$\overline{DRDY}$ is clocked out on the first SCLK rising edge. At the same time that the conversion result is clocked out of DOUT/$\overline{DRDY}$, new Config register data are latched on DIN on the SCLK falling edge.

The ADX112(Q) also offers the possibility of direct readback of the Config register settings in the same data transmission cycle. One complete data transmission cycle consists of either 32 bits (when the Config register data readback is used) or 16 bits (only used when the $\overline{CS}$ line can be controlled and is not permanently tied low).

### 7.5.7.1 32-BIT DATA TRANSMISSION CYCLE

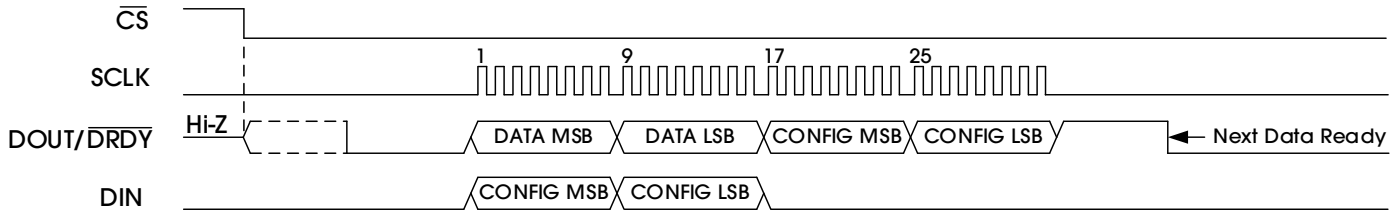
The data in a 32-bit data transmission cycle consists of four bytes: two bytes for the conversion result, and an additional two bytes for the CONFIG REGISTER readback. The device always reads the MSB first.

Write the same Config register setting twice during one transmission cycle as shown in Figure 28. If convenient, write the Config register setting once during the first half of the transmission cycle, and then hold the DIN pin either low (as shown in Figure 29) or high during the second half of the cycle. If no update to the Config register is required, hold the DIN pin either low or high during the entire transmission cycle. The Config register setting written in the first two bytes of a 32-bit transmission cycle is read back in the last two bytes of the same cycle.




Note: $\overline{CS}$ can be held low if the device does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 28. 32-Bit Data Transmission Cycle with Config Register Readback




Note: $\overline{CS}$ can be held low if the device does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 29. 32-Bit Data Transmission Cycle: DIN Held Low

### 7.5.7.2 16-BIT DATA TRANSMISSION CYCLE

If config register data are not required to be read back, the ADX112(Q) conversion data can also be clocked out in a short 16-bit data transmission cycle, as shown in Figure 30. Therefore, $\overline{CS}$ must be taken high after the 16th SCLK cycle. Taking $\overline{CS}$ high resets the SPI interface. The next time $\overline{CS}$ is taken low, data transmission starts with the currently buffered conversion result on the first SCLK rising edge. If DOUT/$\overline{DRDY}$ is low when data retrieval starts, the conversion buffer is already updated with a new result. Otherwise, if DOUT/$\overline{DRDY}$ is high, the same result from the previous data transmission cycle is read.

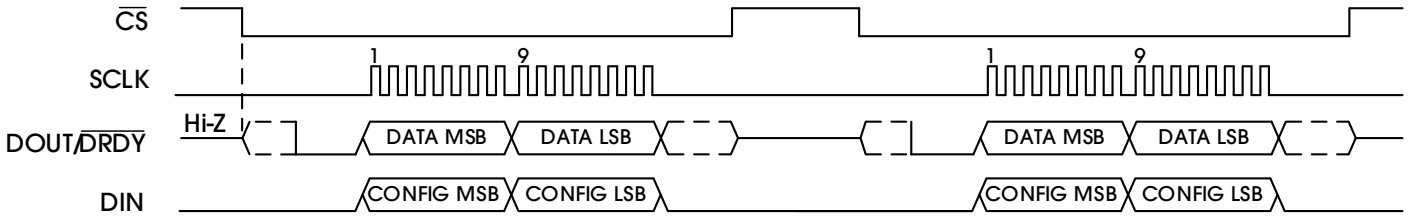



Figure 30. 16-Bit Data Transmission Cycle

# 8. REGISTER MAP

The ADX112(Q) has two registers that are accessible through the SPI interface. The CONVERSION REGISTER contains the result of the last conversion. The CONFIG REGISTER allows the user to change the ADX112(Q) operating modes and query the status of the devices.

## 8.1 CONVERSION REGISTER [RESET = 0000H]

The 16-bit CONVERSION register contains the result of the last conversion in binary twos' complement format. Following power-up, the CONVERSION register is cleared to 0, and remains 0 until the first conversion is completed. The register format is shown in Table 16.

Table 16. CONVERSION Register

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. CONVERSION Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15:0 | D(15:0) | R | 0000h | 16-bit conversion result |

## 8.2 CONFIG REGISTER [RESET = 058BH]

The 16-bit CONFIG register can be used to control the ADX112(Q) operating mode, input selection, data rate, full-scale range, and temperature sensor mode. The register format is shown in Table 18.

Table 18. CONFIG Register

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| SS | MUX(2:0) | | | PGA(2:0) | | | MODE |
| R/W-0h | R/W-0h | | | R/W-2h | | | R/W-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DR(2:0) | | | TS_MODE | PULL_UP_EN | NOP(1:0) | | Reserved |
| R/W-4h | | | R/W-0h | R/W-1h | R/W-1h | | R-1h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. CONFIG Register Field Descriptions

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15 | SS | R/W | 0h | Operational status or single-shot conversion start<br>This bit determines the operational status of the device. The operational status can only be written when in power-down state and has no effect when a conversion is ongoing.<br>When writing:<br>0 = No effect<br>1 = Start a single conversion (when in power-down state)<br>When reading:<br>0 = Device is currently performing a conversion.<br>1 = Device is not currently performing a conversion (default). |
| 14:12 | MUX(2:0) | R/W | 0h | Input multiplexer configuration<br>These bits configure the input multiplexer.<br>000 = $AIN_P$ is AIN0 and $AIN_N$ is AIN1 (default).<br>001 = $AIN_P$ is AIN0 and $AIN_N$ is AIN3.<br>010 = $AIN_P$ is AIN1 and $AIN_N$ is AIN3.<br>011 = $AIN_P$ is AIN2 and $AIN_N$ is AIN3.<br>100 = $AIN_P$ is AIN0 and $AIN_N$ is GND.<br>101 = $AIN_P$ is AIN1 and $AIN_N$ is GND.<br>110 = $AIN_P$ is AIN2 and $AIN_N$ is GND.<br>111 = $AIN_P$ is AIN3 and $AIN_N$ is GND. |
| 11:9 | PGA(2:0) | R/W | 2h | Programmable gain amplifier configuration<br>These bits configure the programmable gain amplifier.<br>000 = FSR is ±6.144V(1)<br>001 = FSR is ±4.096V(1)<br>010 = FSR is ±2.048V (default)<br>011 = FSR is ±1.024V<br>100 = FSR is ±0.512V<br>101 = FSR is ±0.256V<br>110 = FSR is ±0.256V<br>111 = FSR is ±0.256V |
| 8 | MODE | R/W | 1h | Device operating mode<br>This bit controls the ADX112(Q) operating mode.<br>0 = Continuous conversion mode<br>1 = Power-down and single-shot mode (default) |

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:5 | DR(2:0) | R/W | 4h | Data rate<br>These bits control the data rate setting.<br>000 = 8SPS<br>001 = 16SPS<br>010 = 32SPS<br>011 = 64SPS<br>100 = 128SPS (default)<br>101 = 250SPS<br>110 = 475SPS<br>111 = 860SPS |
| 4 | TS_MODE | R/W | 0h | Temperature sensor mode<br>This bit configures the ADC to convert temperature or input signals.<br>0 = ADC mode (default)<br>1 = Temperature sensor mode |
| 3 | PULL_UP_EN | R/W | 1h | Pullup enable<br>This bit enables a weak internal pullup resistor on the DOUT/$\overline{DRDY}$ pin only when $\overline{CS}$ is high. When enabled, an internal 400kΩ resistor connects the bus line to supply. When disabled, the DOUT/$\overline{DRDY}$ pin floats.<br>0 = Pullup resistor disabled on DOUT/$\overline{DRDY}$ pin<br>1 = Pullup resistor enabled on DOUT/$\overline{DRDY}$ pin (default) |
| 2:1 | NOP(1:0) | R/W | 1h | No operation<br>The NOP(1:0) bits control whether data are written to the Config register or not. For data to be written to the Config register, the NOP(1:0) bits must be '01'. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register.<br>00 = Invalid data, do not update the contents of the Config register.<br>01 = Valid data, update the Config register (default).<br>10 = Invalid data, do not update the contents of the Config register.<br>11 = Invalid data, do not update the contents of the Config register. |
| 0 | Reserved | R | 1h | Reserved<br>Writing either 0 or 1 to this bit has no effect.<br>Always reads back 1. |

Note: No more than VDD + 0.3V must be applied to this device.

# 9. APPLICATION AND IMPLEMENTATION

NOTE

Information in the following applications sections is not part of the AnalogySemi component specification, and AnalogySemi does not warrant its accuracy or completeness. AnalogySemi's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 APPLICATION INFORMATION

The ADX112(Q) is a precision, 16-bit ΔΣ ADC that offers many integrated features to ease the measurement of the most common sensor types including various type of temperature and bridge sensors. The following sections give example circuits and suggestions for using the ADX112(Q) in various situations.

### 9.1.1 SERIAL INTERFACE CONNECTIONS

The principle serial interface connections for the ADX112(Q) are shown in Figure 31.

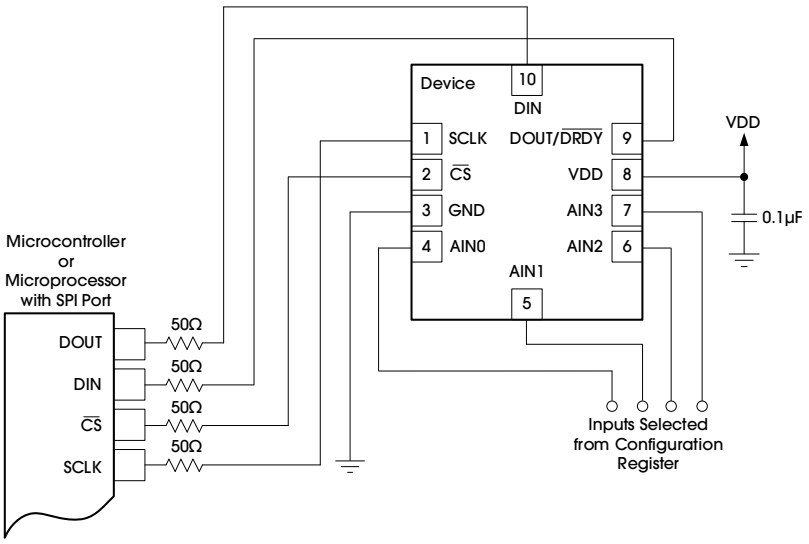



Figure 31. Typical Connections of the ADX112(Q)

Most microcontroller SPI peripherals can operate with the ADX112(Q). The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the ADX112(Q) can be found in the TIMING REQUIREMENTS: SERIAL INTERFACE section.

It is a good practice to place 50Ω resistors in the series path to each of the digital pins to provide some short circuit protection. Care must be taken to still meet all SPI timing requirements because these additional series resistors along with the bus parasitic capacitances present on the digital signal lines could slew the signals.

The fully-differential input of the ADX112(Q) is ideal for connecting to differential sources (such as thermocouples and thermistors) with a moderately low source impedance. Although the ADX112(Q) can read fully-differential signals, the device cannot accept negative voltages on either of its inputs because of ESD protection diodes on each pin. When an input exceeds supply or drops below ground, these diodes turn on to prevent any ESD damage to the device.

### 9.1.2 GPIO PORTS FOR COMMUNICATION

Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an SPI controller is not available, the ADX112(Q) can be connected to GPIO pins and the SPI bus protocol can be simulated. Using GPIO pins to generate the SPI interface only requires that the pins be configured as push or pull inputs or outputs. Furthermore, if the SCLK line is held low for more than 28ms, the communication times out. This condition means that the GPIO ports must be capable of providing SCLK pulses with no more than 28ms between pulses.

### 9.1.3 ANALOG INPUT FILTERING

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper anti-alias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the Nyquist frequency). These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter repeats at multiples of the sampling frequency, also known as the modulator frequency ($f_{(MOD)}$), as shown in Figure 32. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

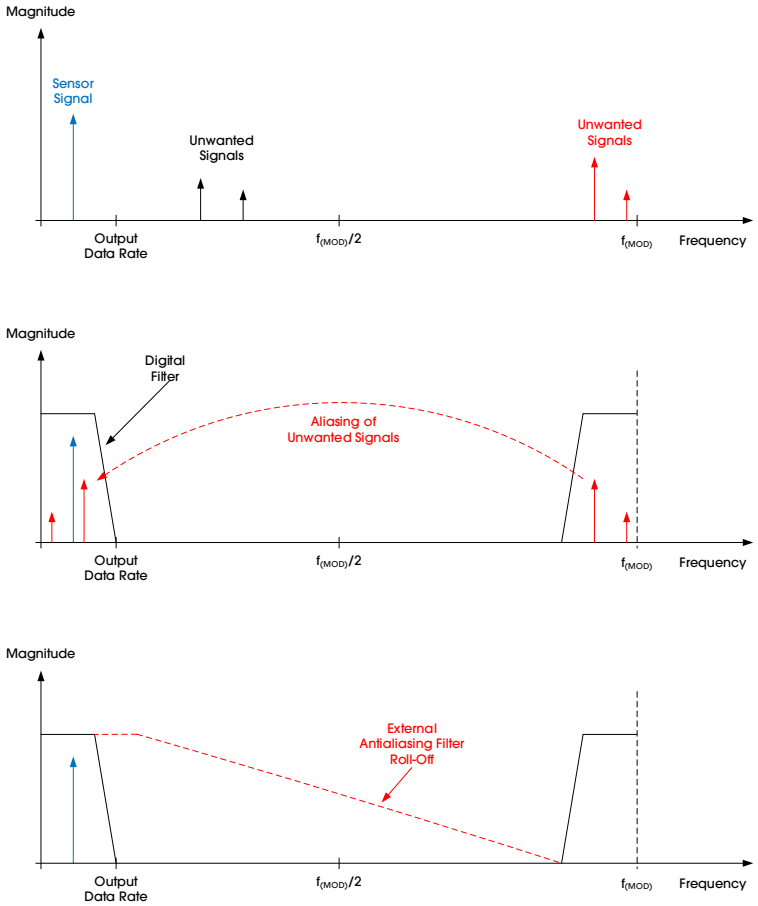



Figure 32. Effect of Aliasing

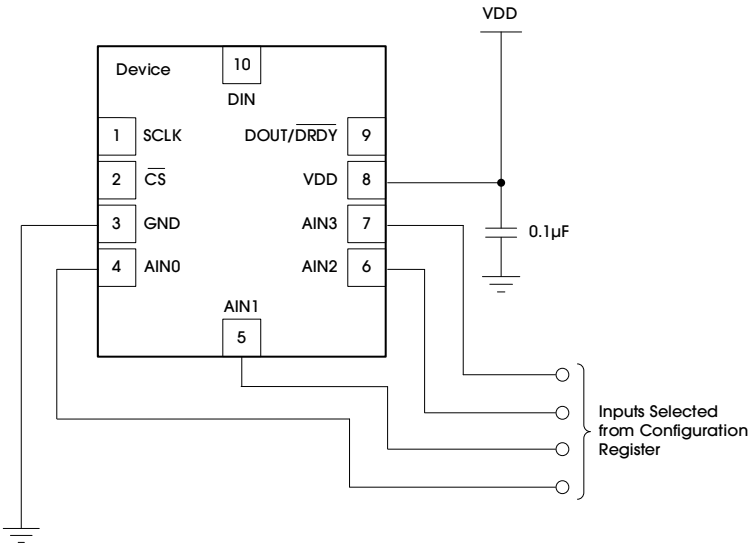
Many sensor signals are inherently bandlimited; for example, the output of a thermocouple has a limited rate of change. In this case, the sensor signal does not alias back into the pass-band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass-band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed-circuit-board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond $f_{(MOD)}$ / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADX112(Q) attenuates signals to a certain degree. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10x higher is generally a good starting point for a system design.

### 9.1.4 SINGLE-ENDED INPUTS

Although the ADX112(Q) has two differential inputs, the device can measure four single-ended signals. Figure 33 shows a single-ended connection scheme. The ADX112(Q) is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection in the CONFIG REGISTER. The single-ended signal can range from 0V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to this circuit because the ADX112(Q) can only accept positive voltages with respect to ground. The ADX112(Q) does not lose linearity within the input range.

The ADX112(Q) offers a differential input voltage range of ±FS. The single-ended circuit shown in Figure 33 however only uses the positive half of the ADX112(Q) FS input voltage range because differentially negative inputs are not produced. Because only half of the FS range is used, one bit of resolution is lost. For optimal noise performance, it is recommended to use differential configurations whenever possible. Differential configurations maximize the dynamic range of the ADC and provide strong attenuation of common-mode noise.



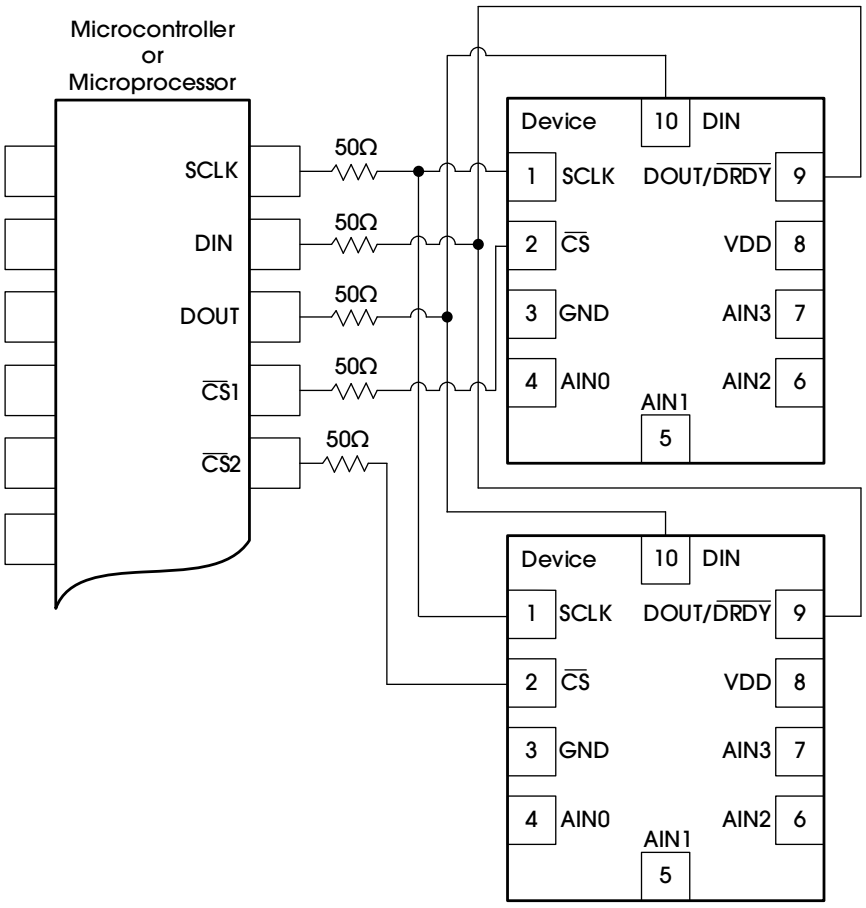

Note: Digital pin connections omitted for clarity.

Figure 33. Measuring Single-Ended Inputs

The ADX112(Q) is also designed to allow AIN3 to serve as a common point for measurements by adjusting the mux configuration. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration, the ADX112(Q) can operate with inputs where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because negative differential voltages are allowed when GND < $V_{(AIN3)}$ < VDD; however, common-mode noise attenuation is not offered.

### 9.1.5 CONNECTING MULTIPLE DEVICES

When connecting multiple ADX112(Q) devices to a single SPI bus, SCLK, DIN, and DOUT/$\overline{DRDY}$ can be safely shared by using a dedicated chip-select ($\overline{CS}$) for each SPI-enabled device. By default, when $\overline{CS}$ goes high for the ADX112(Q), DOUT/$\overline{DRDY}$ is pulled up to VDD by a weak pullup resistor. This feature is intended to prevent DOUT/$\overline{DRDY}$ from floating near mid-rail and causing excess current leakage on a microcontroller input. If the PULL_UP_EN bit in the CONFIG REGISTER is set to 0, the DOUT/$\overline{DRDY}$ pin enters a 3-state mode when $\overline{CS}$ transitions high. The ADX112(Q) cannot issue a data ready pulse on DOUT/$\overline{DRDY}$ when $\overline{CS}$ is high. To evaluate when a new conversion is ready from the ADX112(Q) when using multiple devices, the master can periodically drop $\overline{CS}$ to the ADX112(Q). When $\overline{CS}$ goes low, the DOUT/$\overline{DRDY}$ pin immediately drives either high or low. If the DOUT/$\overline{DRDY}$ line drives low on a low $\overline{CS}$, new data are currently available for clocking out at any time. If the DOUT/$\overline{DRDY}$ line drives high, no new data are available and the ADX112(Q) returns the last read conversion result. Valid data can be retrieved from the ADX112(Q) at any time without concern of data corruption. If a new conversion becomes available during data transmission, that conversion is not available for readback until a new SPI transmission is initiated.




NOTE: Power and input connections omitted for clarity.

Figure 34. Connecting Multiple ADX112(Q)

### 9.1.6 PSEUDO CODE EXAMPLE

The flow chart in Figure 35 shows a pseudo code sequence with the required steps to set up communication between the device and a microcontroller to take subsequent readings from the ADX112(Q). As an example, the default CONFIG REGISTER settings are changed to set up the device in FSR = ±0.512V, continuous conversion mode, and 64SPS data rate.

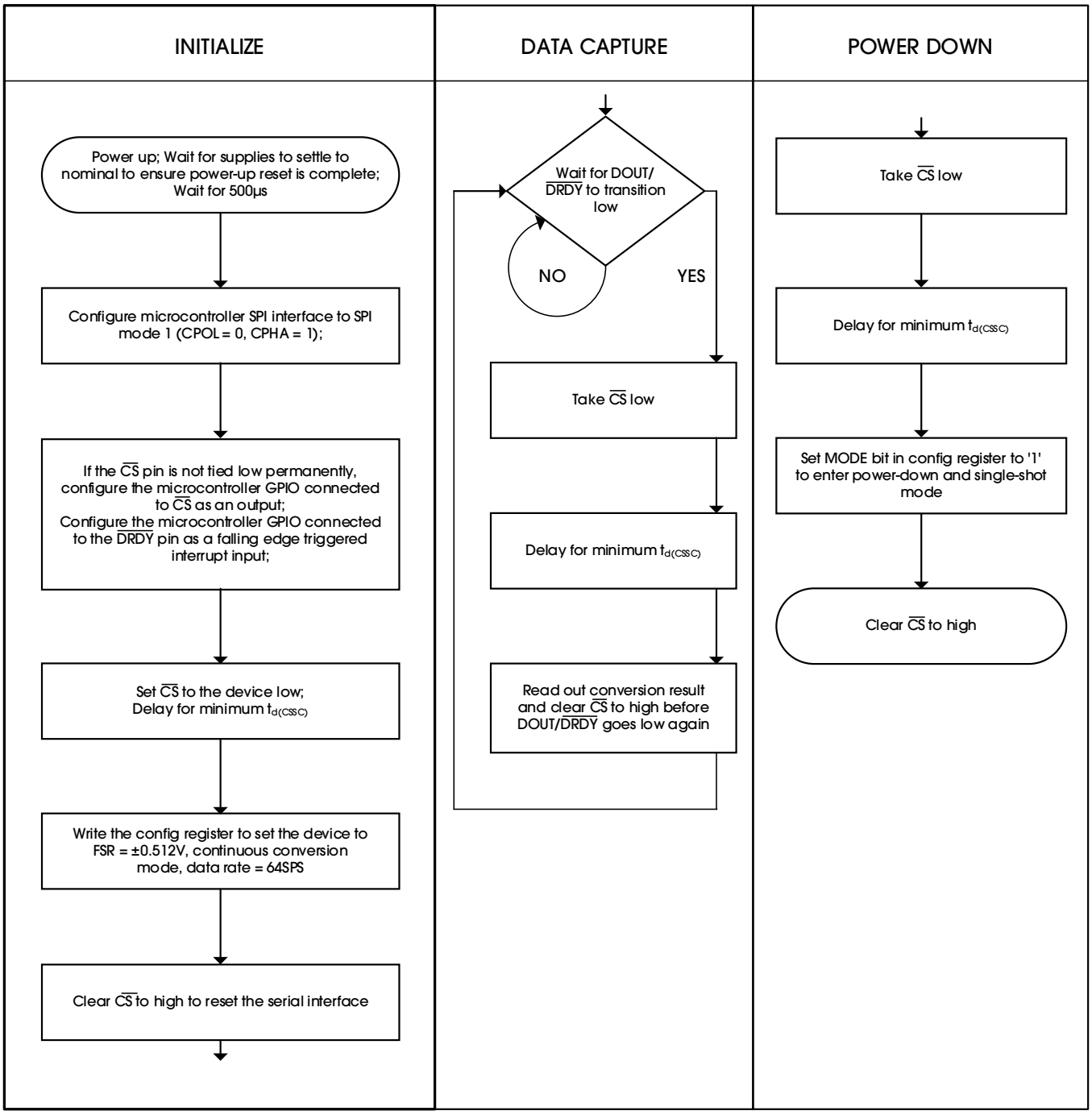



Figure 35. Pseudo Code Example Flow Chart

## 9.2 TYPICAL APPLICATION

Figure 36 shows the basic connections for an independent, two-channel thermocouple measurement system when using the internal high-precision temperature sensor for cold-junction compensation. Apart from the thermocouples, the only external circuitry required are biasing resistors, first-order low-pass, anti-aliasing filters, and a power supply decoupling capacitor.

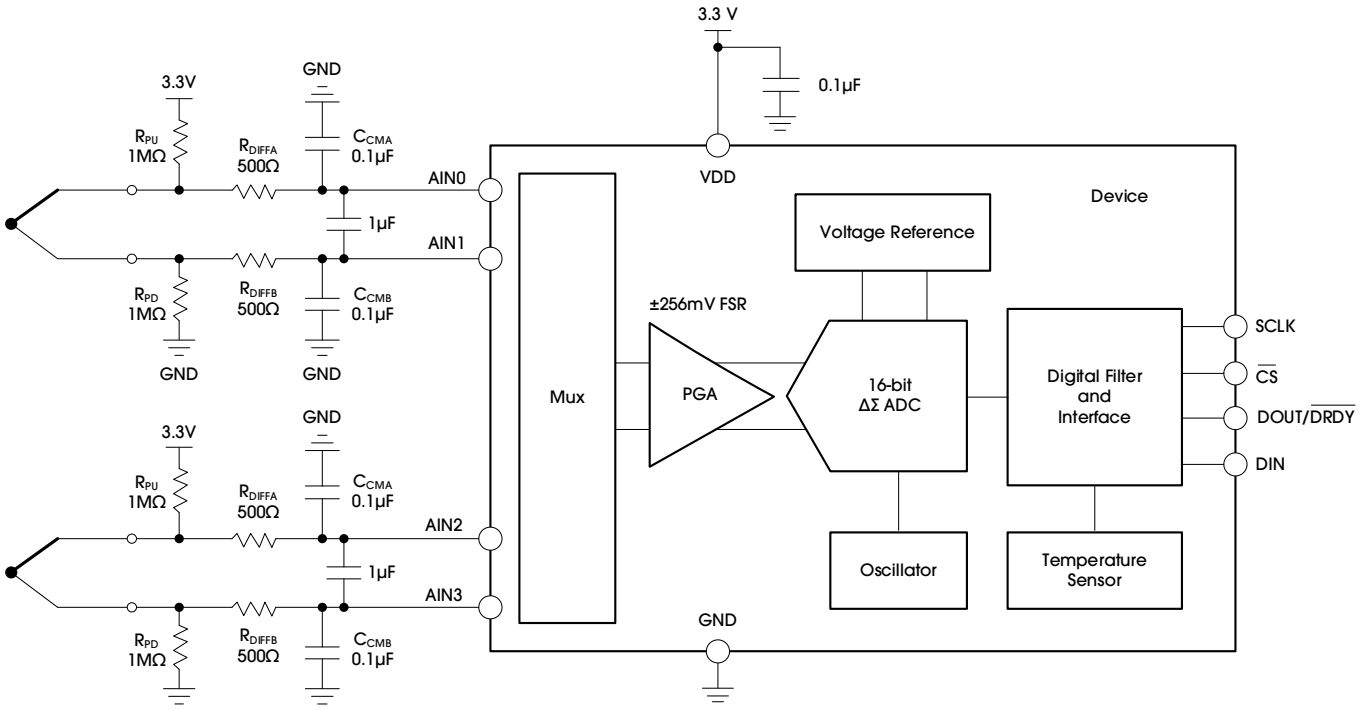



Figure 36. Two-Channel Thermocouple Measurement System

# 10. POWER SUPPLY RECOMMENDATIONS

The device requires a single power supply, VDD, to power both the analog and digital circuitry of the device.

## 10.1 POWER-SUPPLY SEQUENCING

Wait approximately 500µs after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

## 10.2 POWER-SUPPLY DECOUPLING

Good power-supply decoupling is important to achieve optimum performance. VDD must be decoupled with at least a 0.1µF capacitor, as shown in Figure 37. The 0.1µF bypass capacitor supplies the momentary bursts of extra current required from the supply when the ADX112(Q) is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. It is recommended to use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

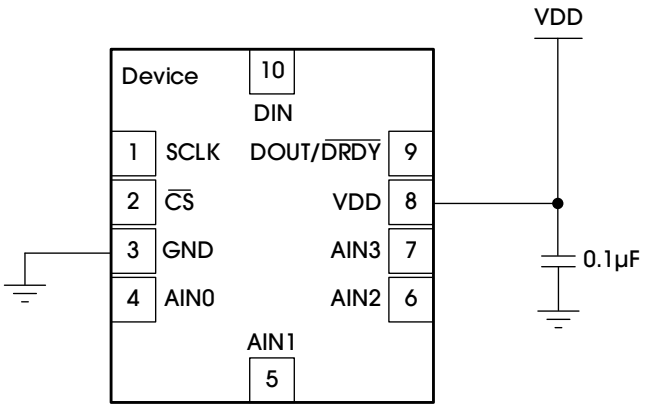



Figure 37. Power Supply Decoupling

# 11. LAYOUT

## 11.1 LAYOUT GUIDELINES

It is suggested to employ best design practices when laying out a printed-circuit-board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components (such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXes) from digital components (such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators). An example of good component placement is shown in Figure 38. Although Figure 38 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

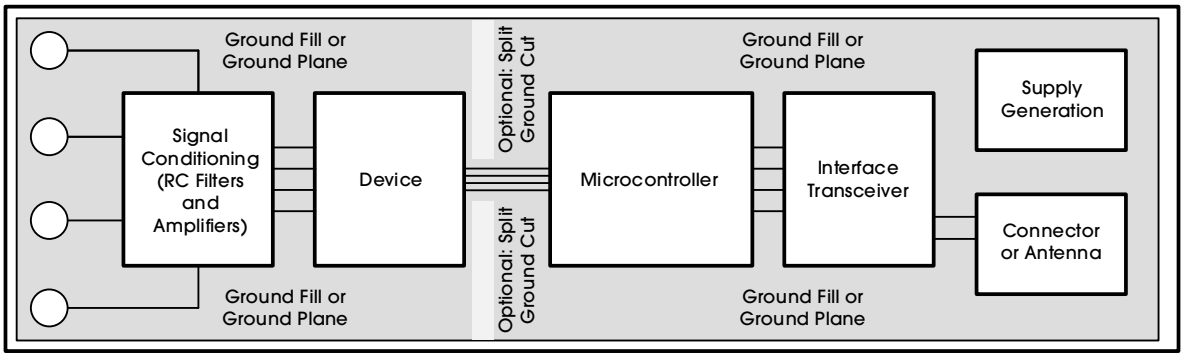



Figure 38. System Component Placement

The use of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation this option is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, generally it is recommended that the ground planes be connected together as close to the device as possible. A two-layer board is possible using common grounds for both analog and digital grounds. Additional layers can be added to simplify PCB trace routing. Ground fill may also reduce EMI and RFI issues.

It is also strongly recommended that digital components, especially RF portions, be kept as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid placing these traces near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature-sensing functions are much more significant than for ADC functions.

Supply pins must be bypassed to ground with a low-ESR ceramic capacitor. The optimum placement of the bypass capacitors is as close as possible to the supply pins. The ground-side connections of the bypass capacitors must be low-impedance connections for optimum performance. The supply current flows through the bypass capacitor terminal first and then to the supply pin to make the bypassing most effective.

Analog inputs with differential connections must have a capacitor placed differentially across the inputs. The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO), which have stable properties and low noise characteristics. Thermally isolate a copper region around the thermocouple input connections to create a thermally-stable cold junction. Obtaining acceptable performance with alternate layout schemes is possible as long as the above guidelines are followed.

## 11.2 LAYOUT EXAMPLE

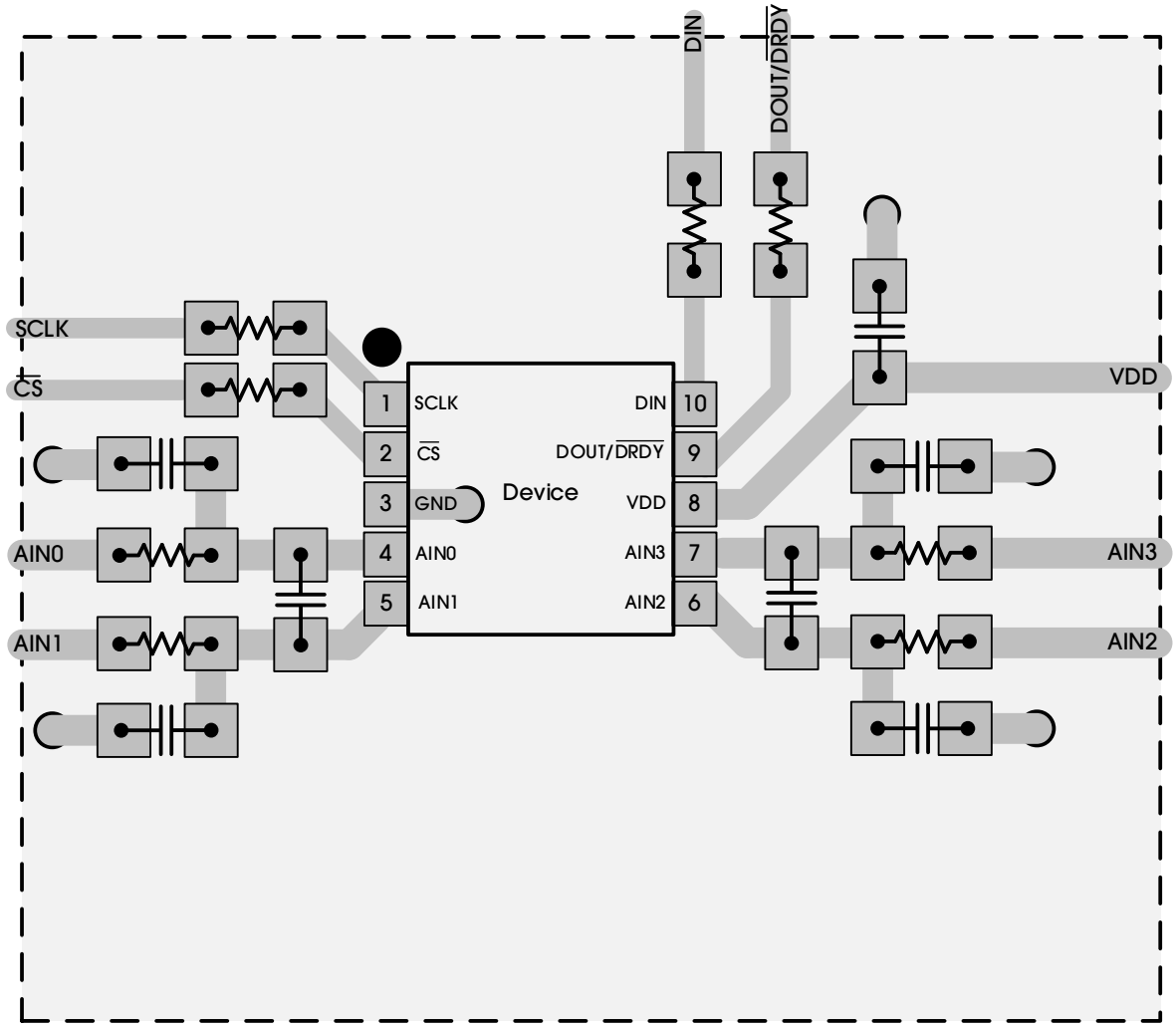



Figure 39. MSOP-10 Package

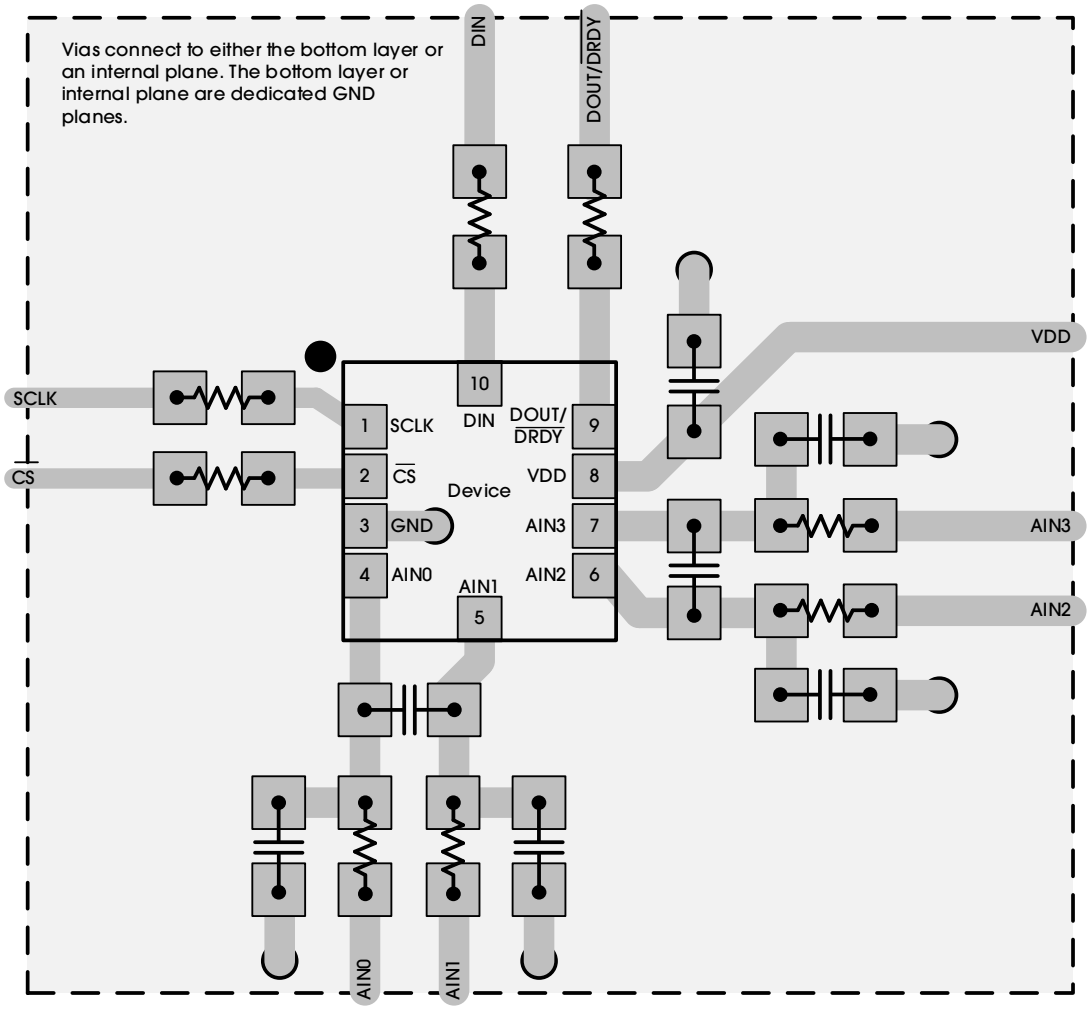



Figure 40. QFN-10 Package

# 12. PACKAGE INFORMATION

The ADX112(Q) is available in the MSOP-10 and QFN-10 packages.

## 12.1 MSOP-10 PACKAGE

Figure 41 shows the MSOP-10 package view.

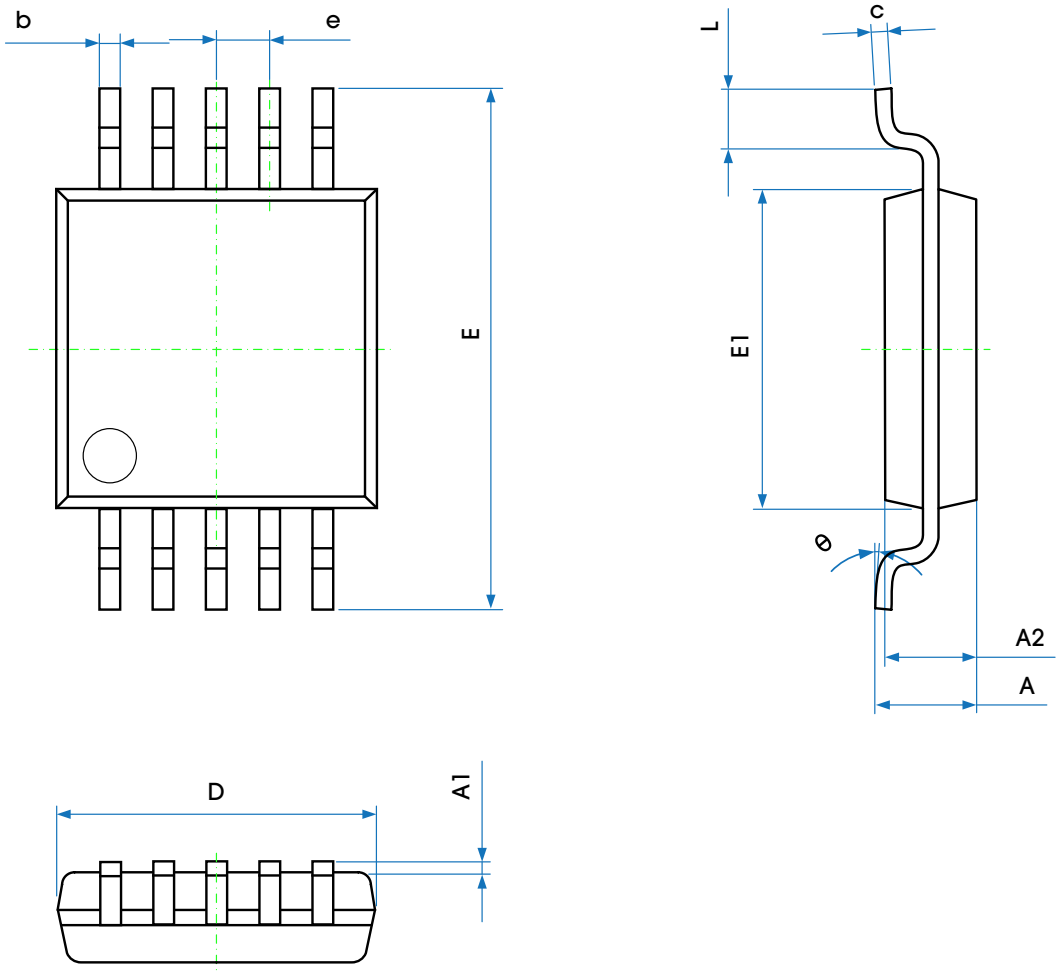



Figure 41. MSOP-10 Package View

Table 20 provides detailed information about the dimensions of the MSOP-10 package.

Table 20. Dimensions of the MSOP-10 Package

| SYMBOL | DIMENSIONS IN MILLIMETERS | | DIMENSIONS IN INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | — | 1.100 | — | 0.043 |
| A1 | 0.020 | 0.150 | 0.001 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| b | 0.180 | 0.330 | 0.007 | 0.013 |
| c | 0.090 | 0.230 | 0.004 | 0.009 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| e | 0.500 (BSC) | | 0.020 (BSC) | |
| E | 4.750 | 5.050 | 0.187 | 0.199 |
| E1 | 2.900 | 3.100 | 0.114 | 0.122 |
| L | 0.400 | 0.800 | 0.016 | 0.031 |
| θ | 0° | 6° | 0° | 6° |

## 12.2 QFN-10 PACKAGE

Figure 42 shows the QFN-10 package view.

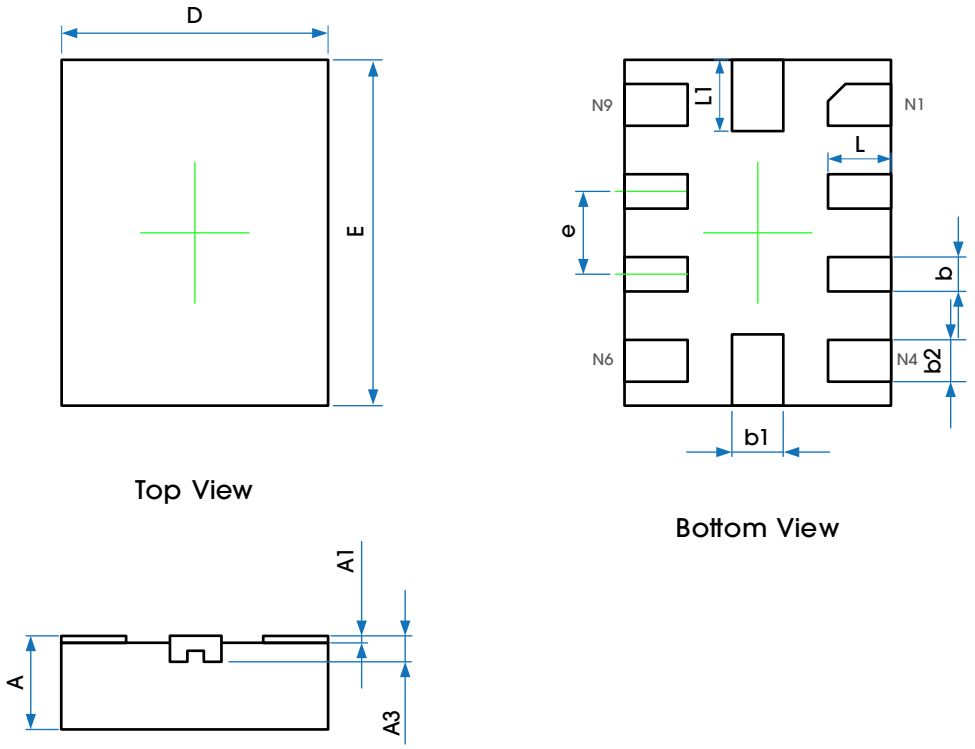



Figure 42. QFN-10 Package View

Table 21 provides detailed information about the dimensions of the QFN-10 package.

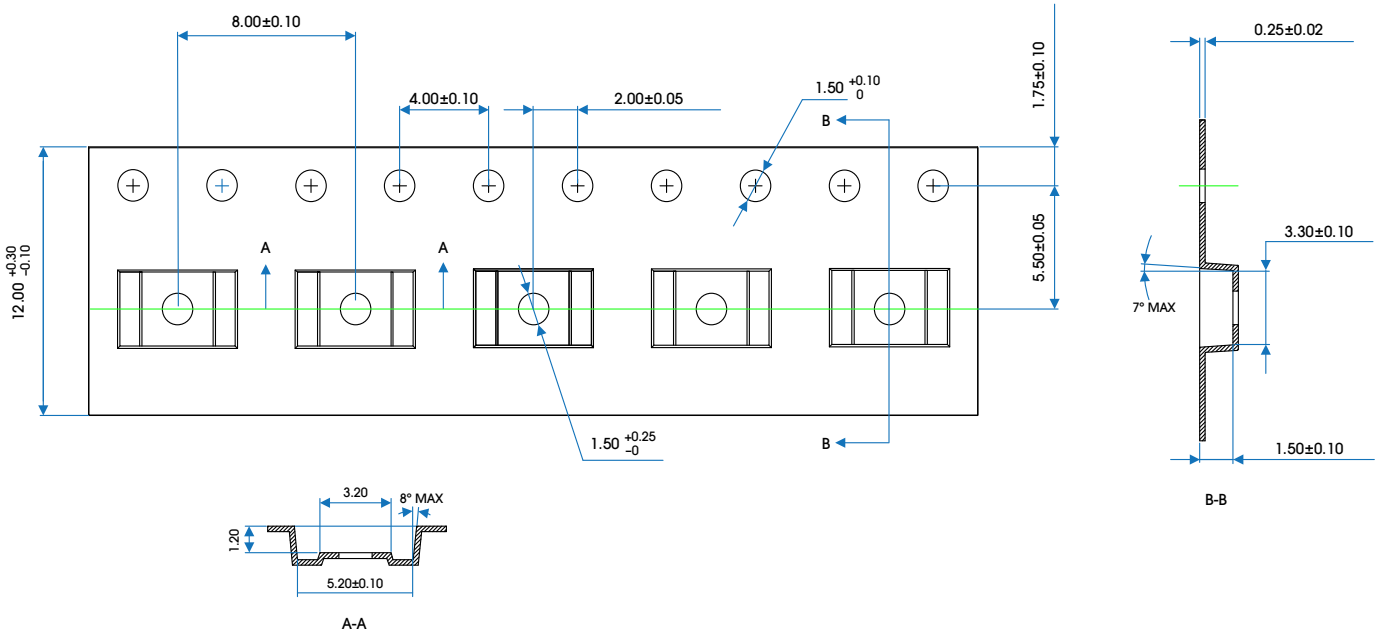
Table 21. Dimensions of the QFN-10 Package

| SYMBOL | DIMENSIONS IN MILLIMETERS | | DIMENSIONS IN INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.500 | 0.600 | 0.020 | 0.024 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.152REF. | | 0.006REF. | |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| b1 | 0.250 | 0.350 | 0.010 | 0.014 |
| b2 | 0.200 | 0.300 | 0.008 | 0.012 |
| D | 1.450 | 1.550 | 0.057 | 0.061 |
| E | 1.950 | 2.050 | 0.077 | 0.081 |
| e | 0.500TYP. | | 0.020TYP. | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |
| L1 | 0.350 | 0.450 | 0.014 | 0.018 |

# 13. TAPE AND REEL INFORMATION

## 13.1 MSOP-10 PACKAGE

Figure 43 illustrates the carrier tape of the MSOP-10 package.




Notes:
1. Cover tape width: 9.5 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 1mm in 100mm.
4. Mold#: MSOP-10 (3*3).
5. All dimensions: mm.
6. Direction of view:

Figure 43. Carrier Tape Drawing (MSOP-10 Package)

Table 22 provides information about tape and reel (MSOP-10 package).

Table 22. Tape and Reel Information (MSOP-10 Package)

| PACKAGE TYPE | REEL | QTY/REEL | REEL/ INNER BOX | INNER BOX/ CARTON | QTY/CARTON | INNER BOX SIZE (MM) | CARTON SIZE (MM) |
|---|---|---|---|---|---|---|---|
| MSOP-10 3*3 | 13'' | 3000 | 1 | 8 | 24000 | 358*340*50 | 430*380*390 |

Figure 44 shows the product loading orientation—pin 1 is assigned on the upper left corner.

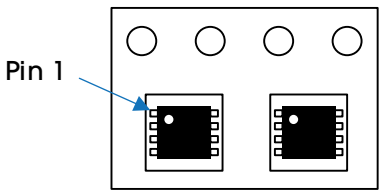
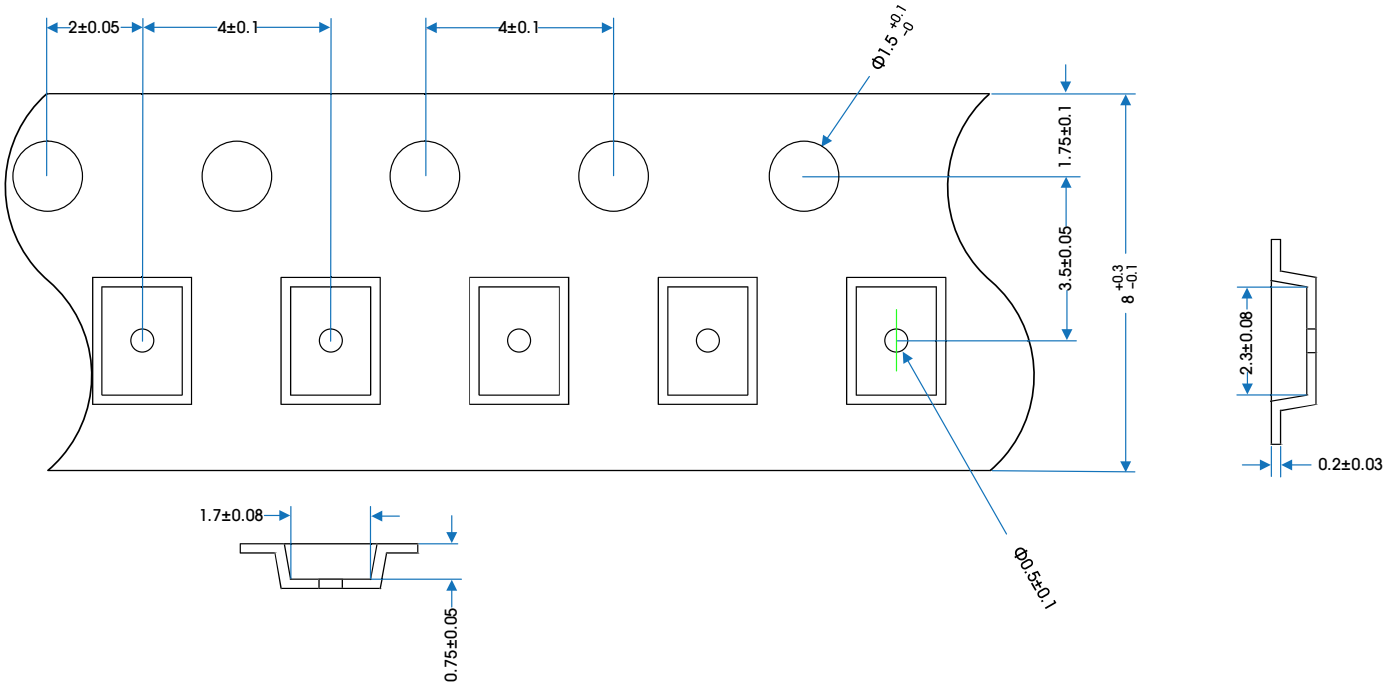



Figure 44. Product Loading Orientation (MSOP-10 Package)

## 13.2 QFN-10 PACKAGE

Figure 45 illustrates the carrier tape (QFN-10 package).




Notes:
1. Cover tape width: 5.5 ± 0.10.
2. Cumulative tolerance of 10 sprocket hole pitch: ±0.20 (max).
3. Camber: not to exceed 1mm in 100mm.
4. Mold#: QFN-10 (1.5*2).
5. All dimensions: mm.
6. Direction of view:

Figure 45. Carrier Tape Drawing (QFN-10 Package)

Table 23 provides information about tape and reel (QFN-10 package).

Table 23. Tape and Reel Information (QFN-10 Package)

| PACKAGE TYPE | REEL | QTY/REEL | REEL/ INNER BOX | INNER BOX/ CARTON | QTY/CARTON | INNER BOX SIZE (MM) | CARTON SIZE (MM) |
|---|---|---|---|---|---|---|---|
| QFN-10 1.5*2 | 7'' | 4000 | 10 | 4 | 160000 | 210*208*203 | 440*440*230 |

Figure 46 shows the product loading orientation—pin 1 is assigned on the upper left corner.

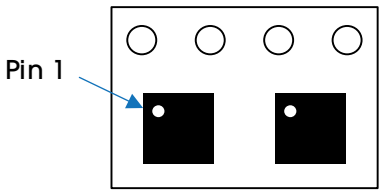



Figure 46. Product Loading Orientation (QFN-10 Package)

# REVISION HISTORY

| REVISION | DATE | DESCRIPTION |
|---|---|---|
| Rev A | 19 April 2022 | Rev A release. |
| Rev B | 08 August 2022 | 1. Updated the order information.<br>2. Updated Table 7.<br>3. Added Figure 15 through Figure 21.<br>4. Updated Table 19. |
| Rev C | 26 September 2022 | 1. Updated the device name.<br>2. Updated the FEATURES section.<br>3. Updated the order information. |