DESCRIPTION

The BDR2L00 is a single Phase MOSFET gate driver optimized to drive the gates of both high-side and low-side power MOSFETs.

The integrated bootstrap diode reduces external component count. With a wide operating voltage range, high or low side MOSFET gate drive voltage can be optimized for the best efficiency. Internal adaptive non-overlap circuit further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

The UVLO circuits prevent malfunction when VCC is lower than the specified threshold voltage.

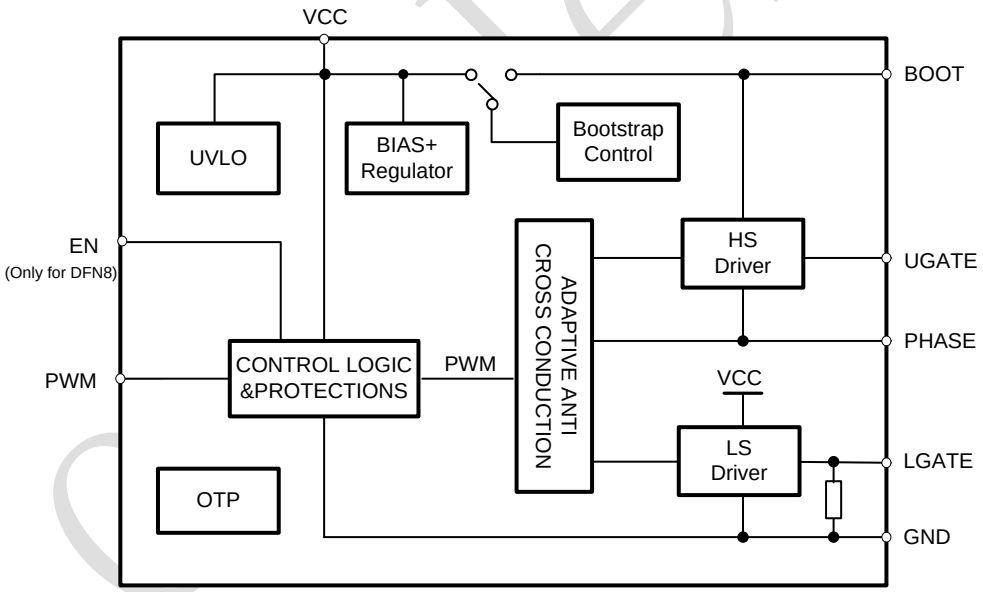
FEATURES

- Drive two N-MOSFETs
- High-Frequency operation (Up to 1MHz)
- PWM input capable of 3.3V and 5V
- Fast output rise time
- Internal bootstrap diode
- Adaptive shoot through protection
- Under-voltage lockout
- Internal thermal shutdown
- Small size package：SOP-8, DFN8(2x2, 3x3)
- These are Pb-Free Devices

APPLICATIONS

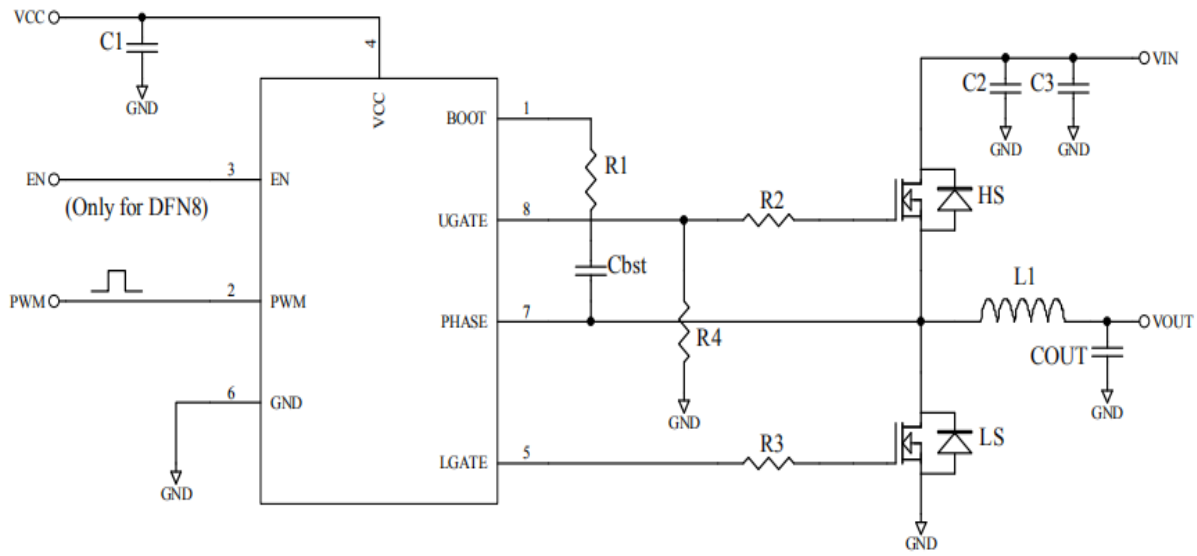
- Wireless Charger for 5W to 20W Systems
- Half or full bridge driver for N+N MOSFET

BLOCK DIAGRAM



APPLICATION CIRCUIT

SOP8/DFN8:



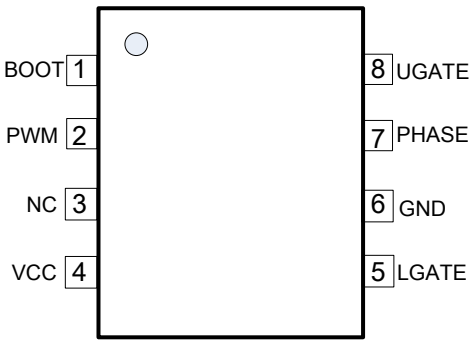
Reference Design of BOM:

Name	Value	Name	Value
C1	10uF	R1	0
C2	0.1uF	R2	5ohm
C3	22uF	R3	5ohm
Cbst	680nF	R4	10K

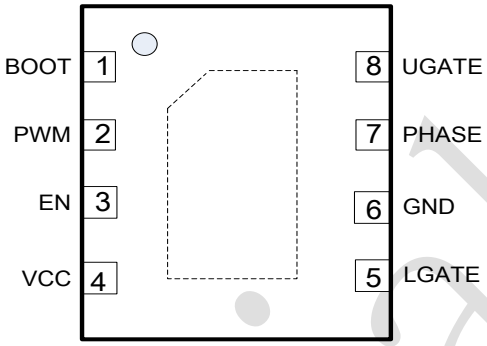
TRUTH TABLE

Package	EN	PWM	LGATE	UGATE
SOP8	-	L	H	L
	-	H	L	H
DFN8	L	-	L	L
	H	L	H	L
	H	H	L	H

PIN CONFIGURATION



SOP8



DFN8(2X2, 3X3)

PIN DESCRIPTION

Pin Name	Description	Pin No.	
		SOP8	DFN8
BOOT	Floating bootstrap supply pin for upper gate drive	1	1
PWM	Input PWM signal for controlling the Driver	2	2
NC	No internal connection	3	-
EN	Enable	-	3
VCC	Logic and low-side gate drivers power supply voltage	4	4
LGATE	Lower gate drive output	5	5
GND	Ground	6	6
PHASE	Connect this pin to the source of the high side MOSFET and the drain of the low side MOSFET	7	7
UGATE	Upper gate drive output	8	8

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
BDR2L00	8 Pins, SOP, 150mil	BDR2L00
BDR2L00	8 Pins, DFN, 2*2	BDR2L00
BDR2L00	8 Pins, DFN, 3*3	BDR2L00

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device or make the function abnormal. All the voltage parameters are absolute voltages referenced to IC PGND unless otherwise stated in the table.

Parameter	Symbol	Min.	Max.	Units
Logic & low-side supply voltage	VCC	-0.3	6.5	V
BOOT to PHASE	VBP	-0.3	5.5	
PHASE to GND	VP	-0.3	24	
UGATE	Vug	Vphase-0.3V	Vboot+0.3V	
LGATE	Vlg	GND-0.3V	VCC+0.3V	
Logic input voltage	PWM/EN	-0.3	6.5	
Thermal resistance, junction to ambient [1]	Rth_{JA}	-	TBD	°C/W
Junction temperature	T_J	-40	+150	°C
Storage temperature	T_S	-40	+150	°C
Soldering lead temperature (duration 10s)	TL	-	260	°C

Note 1: Rth_{JA} are only guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Logic & low-side supply voltage	VCC	3.3	-	5.5	V
Logic input voltage	PWM/EN	0	-	5.5	
Operating temperature	T_{oper}	-30	-	+85	°C

ELECTRICAL CHARACTERISTICS

VCC=5V, Ambient temperature T_A=25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low Side Power Supply Characteristics						
Quiescent VCC supply current in standby mode	I_{QVCC1}		-	110	-	uA
VCC supply under-voltage positive going threshold	V_{CCUV+}	-	2.0	2.2	2.6	V
VCC supply under-voltage lockout hysteresis	V_{CCHYS}	-	-	0.2	-	V
PWM Input						
PWM input voltage high	V_{IH}	-	2.5	-	-	V
PWM input voltage low	V_{IL}	-	-	-	0.8	V
Output disable hysteresis	V_{HYS}	-	-	300	-	mV
EN Input						
EN input voltage high	V_{IH}	-	2.5	-	-	V
EN input voltage low	V_{IL}	-	-	-	0.8	V
Output disable hysteresis	V_{HYS}	-	-	300	-	mV
Thermal Shutdown						
Thermal shutdown temperature	-	-	-	170	-	°C
Thermal shutdown hysteresis	-	-	-	20	-	
Driver						
UGATE drive source	R_{UGATE_sr}	BST-PHASE=5V, Ids=2A	-	2.8	-	Ω
UGATE drive sink	R_{UGATE_sk}	BST-PHASE=5V, Ids=2A	-	0.9	-	Ω
LGATE drive source	R_{LGATE_sr}	VCC=5V, Ids=2A	-	2.8	-	Ω
LGATE drive sink	R_{LGATE_sk}	VCC=5V, Ids=2A	-	0.9	-	Ω

APPLICATION INFORMATION

Theory of Operation

The BDR2L00 is an integrated driver and boot diode module designed for N+N half bridge driver. A single PWM input signal is all that is required to properly drive the high−side and low−side MOSFETs.

Low−Side Driver

The low-side driver is designed to drive a ground−referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to VCC and GND.

High−Side Driver

The high-side driver is designed to drive a floating low RDS(ON) N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (PHASE) pin.

The bootstrap circuit is comprised of the internal diode and an external bootstrap capacitor. When the BDR2L00 is starting up, the PHASE pin is at ground, so the bootstrap capacitor will charge up to VCC through the bootstrap diode. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the PHASE pin will rise. When the high−side MOSFET is fully on, the switch node will be at 12V, and the BST pin will be at 5V plus the charge of the bootstrap capacitor (approaching 17V).

The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot−through or cross conduction can damage the MOSFETs, and even a small amount of cross conduction will cause a decrease in the power conversion efficiency.

The BDR2L00 prevents cross conduction by monitoring the status of the MOSFETs and applying the appropriate amount of “dead−time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET.

When the PWM input pin goes high, the gate of the low−side MOSFET will go low after a propagation delay. The time it takes for the low−side MOSFET to turn off is dependent on the total charge on the low−side MOSFET gate.

Likewise, when the PWM input pin goes low, the gate of the high−side MOSFET will go low after the propagation delay. The time to turn off the high−side MOSFET is dependent on the total gate charge of the high−side MOSFET.

Enable (Only for DFN8)

If EN pin is low level, whatever the PWM pin is high or low, all circuits are shutdown. If EN pin is high level, the outputs are controlled by PWM pin.

Thermal Shutdown

If the driver temperature exceeds 170°C, the part will enter thermal shutdown and turn off both MOSFETs. Once the temperature falls below 150°C, the part will resume normal operation.

Power Supply Decoupling

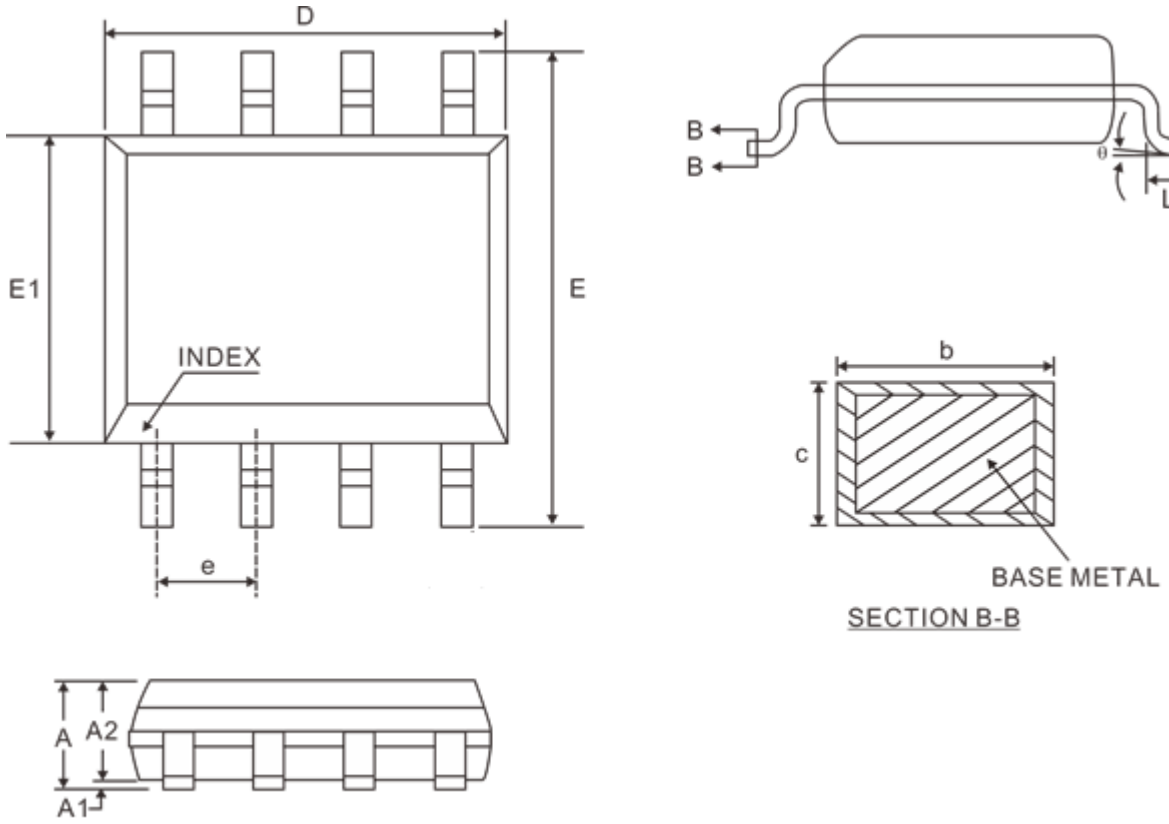
The BDR2L00 can source and sink relatively large current to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage (VCC) a low ESR capacitor should be placed near the power and ground pins. A 2.2uF to 10uF multilayer ceramic capacitor (MLCC) is usually sufficient.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}). The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 16 V rating is recommended. A bootstrap capacitance greater than 680nF and a minimum 16V rating is recommended. A good quality ceramic capacitor should be used.

PACKAGE INFORMATION

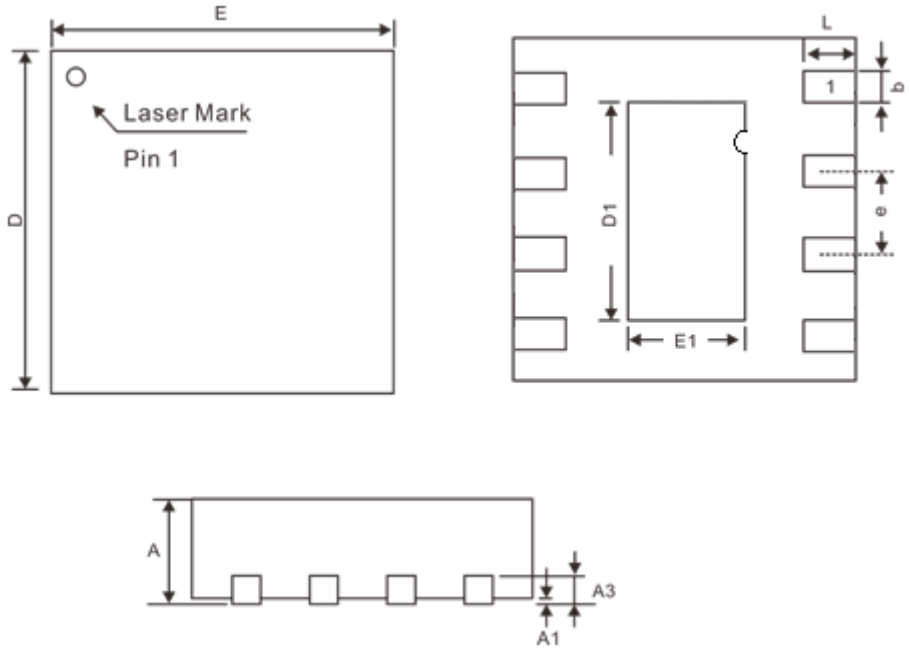
8 PINS, SOP, 150MIL



Symbol	Dimensions		
	Min.	Nom.	Max.
A	-	-	1.70
A1	0.00	-	0.15
A2	1.30	1.40	1.50
b	0.39	-	0.48
c	0.21	-	0.25
e	1.27 BSC		
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
L	0.40	-	1.27
L1	1.04 REF		
θ	0°	-	8°

Notes:
1. Refer to JEDEC MS-012 AA
2. All dimensions are in millimeter.

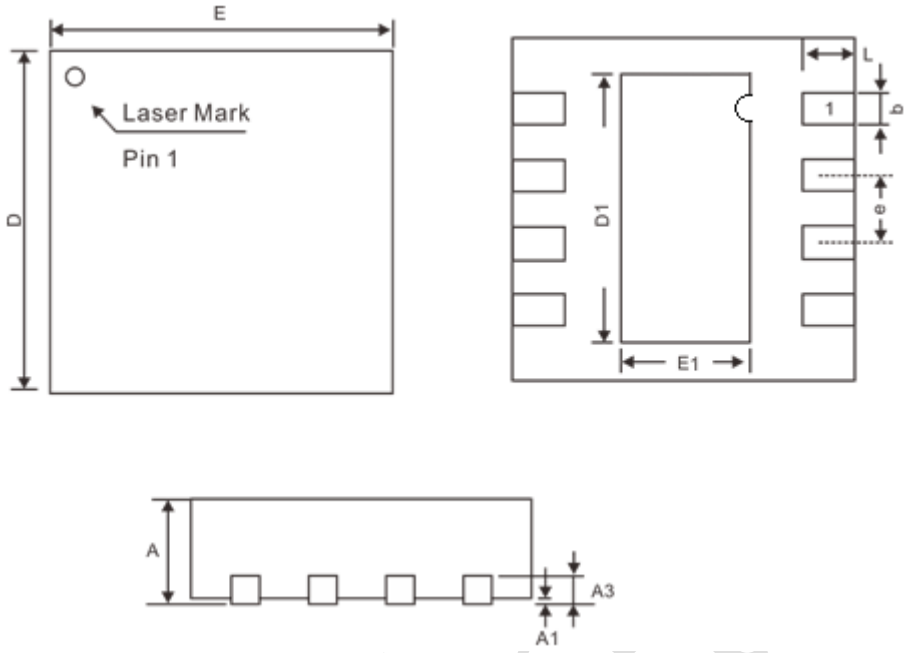
8-PINS, DFN, 2X2



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	0.70	0.80
A1	0	0.05
A3	0.153	0.253
b	0.18	0.30
D	1.90	2.10
E	1.90	2.10
e	0.50 TYP	
D1	1.10	1.30
E1	0.50	0.70
L	0.25	0.45

Note: Refer to JEDEC MO-229

8-PINS, DFN, 3X3



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	0.70	0.80
A1	0	0.05
A3	0.203 REF	
b	0.20	0.30
D	2.924	3.076
E	2.924	3.076
e	0.50 TYP	
D1	2.30	2.50
E1	1.60	1.80
L	0.324	0.476

Note: Refer to JEDEC MO-229

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