LMK00804B 低偏移 1 到 4 多路复用差动/LVCMOS 到 LVCMOS/TTL 扇出缓冲器

1 特性

- 4 个具有 7Ω 输出阻抗的 LVCMOS/LVTTL 输出
  - 附加抖动：125MHz 时为 0.04ps RMS（典型值）
  - 噪底：125MHz 时为 –166dBc/Hz（典型值）
  - 输出频率：350MHz（最大值）
  - 输出偏移：35ps（最大值）
  - 部件间偏移：700ps（最大值）
- 两个可选输入
  - CLK、nCLK 对接受 LVPECL、LVDS、HCSL、SSTL、LVHSTL 或 LVCMOS/LVTTL
  - LVCMOS_CLK 接受 LVCMOS/LVTTL
- 同步时钟启用
- 内核/输出电源：
  - 3.3V/3.3V
  - 3.3V/2.5V
  - 3.3V/1.8V
  - 3.3V/1.5V
- 封装：16 引线薄型小尺寸封装 (TSSOP)
- 工业温度范围：-40ºC 至 +85ºC

2 应用

- 无线和有线基础设施
- 网络和数据通信
- 服务器和计算
- 医疗成像
- 便携式测试和测量
- 高端 A/V

3 说明

LMK00804B 是一款低偏移、高性能时钟扇出缓冲器，可通过两个可选输入（可接受差分输入或单端输入）之一分配至多 4 个 LVCMOS/LVTTL 输出（3.3V、2.5V、1.8V 或 1.5V 四种电平）。 时钟使能输入在内部同步，以便在时钟使能端子被置为有效或置为无效时消除输出上的欠幅脉冲或毛刺脉冲。 禁用时钟后，输出将保持逻辑低电平状态。 单独的输出使能端子可控制输出处于激活状态或高阻态。 LMK00804B 具有低附加抖动和相位噪底，且兼具可靠的输出和部件间偏移特性，因此非常适合对高性能和可重复性有严格要求的应用。

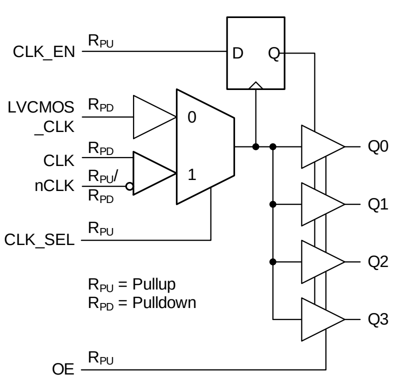
有关 CDCLVC1310 和 LMK00725 部件的介绍，另请参见Device Comparison Table。

器件信息

部件号	封装	封装尺寸（标称值）
LMK00804B	TSSOP (16)	5.00mm x 4.40mm

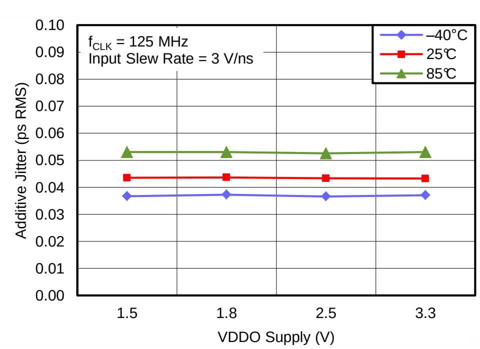
1. 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



(1) R_{PU} = 51kΩ（上拉电阻）， R_{PD} = 51kΩ（下拉电阻）。 请参见Figure 10

附加抖动与 **VDDO** 电源和温度间的关系



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5 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

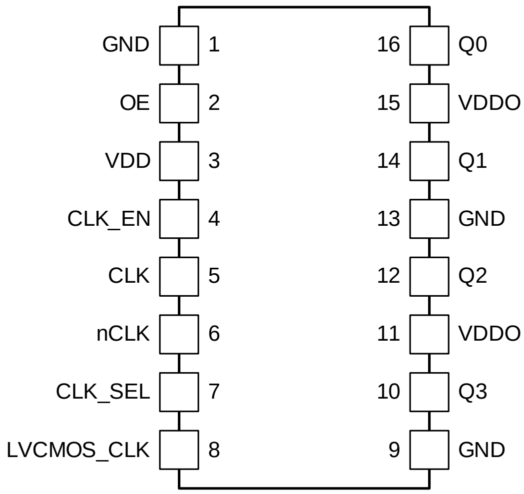
Changes from Original (June 2014) to Revision A	Page
• Added Device Comparison Table	3
• Changed Human Body Model (HBM) value from 2000 to 1000	4
• Changed Charged Device Model (CDM) value from 750 to 250	4

6 Device Comparison Table

PART NUMBER	DESCRIPTION
CDCLVC1310	10 outputs LVCMOS fanout buffer with Diff, Single-Ended, or Crystal Input
LMK00725	5 output LVPECL fanout buffer with Differential or Single-Ended Input

7 Pin Configuration and Functions

16 Pin
PW Package
Top View



Pin Functions

TERMINAL		TYPE(1)	DESCRIPTION
NAME	NUMBER		
GND	1, 9, 13	G	Power supply ground
OE	2	I, R_{PU}	Output enable input. 0 = Outputs in Hi-Z state 1 = Outputs in active state
VDD	3	P	Power supply terminal
CLK_EN	4	I, R_{PU}	Synchronous clock enable input. 0 = Outputs are forced to logic low state 1 = Outputs are enabled with LVCMOS/LVTT levels
CLK	5	I, R_{PD}	Non-inverting differential clock input 0.
nCLK	6	I, R_{PD}/R_{PU}	Inverting differential clock input 0. Internally biased to VDD/2 when left floating
CLK_SEL	7	I, R_{PU}	Clock select input. 0 = Select LVCMOS_CLK 1 = Select CLK, nCLK
LVCMOS_CLK	8	I, R_{PD}	Single-ended clock input. Accepts LVCMOS/LVTTL levels.
Q3, Q2, Q1, Q0	10, 12, 14, 16	O	Single-ended clock outputs with LVCMOS/LVTTL levels, 7Ω output impedance
VDDO	11, 15	P	Output supply terminals

(1) **G** = Ground, **I** = Input, **O** = Output, **P** = Power, **R_{PU}** = 51 kΩ pullup, **R_{PD}** = 51 kΩ pulldown.

8 Specifications

8.1 Pin Characteristics

		MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance		1		pF
R_{PU}	Input Pullup Resistance		51		kΩ
R_{PD}	Input Pulldown Resistance		51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)		2		pF
R_{OUT}	Output impedance		7		Ω

8.2 Absolute Maximum Ratings[1][2]

Over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VDD	Core Supply Voltage	–0.3		3.6	V
VDDO	Output Supply Voltage	–0.3		3.6	V
V_{IN}	Input Voltage Range	–0.3		VDD +0.3	V
T_J	Junction Temperature			150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

8.3 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge[1]	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[2]		1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[3]		250	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VDD	Core Supply Voltage	3.135	3.3	3.465	V
VDDO	Output Supply Voltage	3.135	3.3	3.465	V
		2.375	2.5	2.625	
		1.65	1.8	1.95	
		1.425	1.5	1.575	
T_A	Ambient Temperature	-40		85	°C
T_J	Junction Temperature			125	°C

8.5 Thermal Information

Over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[1]		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Package Thermal Impedance, Junction to Air (0 LFPM)			116	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.6 Power Supply Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
IDD	Power Supply Current through VDD			21	mA
IDDO	Power Supply Current through VDDO			5	mA

8.7 LVCMOS / LVTTL DC Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage	CLK_EN, CLK_SEL, OE		2		VDD + 0.3	V
		LVCMOS_CLK		2		VDD + 0.3	V
V_{IL}	Input Low Voltage	CLK_EN, CLK_SEL, OE		–0.3		0.8	V
		LVCMOS_CLK		–0.3		1.3	
I_{IH}	Input High Current	CLK_EN, CLK_SEL, OE	VDD = 3.465 V, V_{IN} = 3.465 V			5	µA
		LVCMOS_CLK	VDD = 3.465 V, V_{IN} = 3.465 V			150	
I_{IL}	Input Low Current	CLK_EN, CLK_SEL, OE	VDD = 3.465 V, V_{IN} = 0 V	–150			µA
		LVCMOS_CLK	VDD = 3.465 V, V_{IN} = 0 V	–5			
V_{OH}	Output High Voltage[1]		VDDO = 3.3 V ± 5%	2.6			V
			VDDO = 2.5 V ± 5%	1.8			
			VDDO = 1.8 V ± 0.15 V	1.5			
			VDDO = 1.5 V ± 5%	VDDO – 0.3			
V_{OL}	Output Low Voltage[1]		VDDO = 3.3 V ± 5%			0.5	V
			VDDO = 2.5 V ± 5%			0.5	
			VDDO = 1.8 V ± 0.15 V			0.4	
			VDDO = 1.5 V ± 5%			0.35	
I_{OZL}	Output Hi-Z Current Low			–5			µA
I_{OZH}	Output Hi-Z Current High					5	

(1) Outputs terminated with 50 Ω to VDDO/2.

8.8 Differential Input DC Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	Differential Input Voltage Swing, (V_{IH}-V_{IL})(1)			0.15		1.3	V
V_{ICM}	Input Common Mode Voltage(1)(2)			0.5		VDD – 0.85	V
I_{IH}	Input High Current(3)	nCLK	VDD = 3.465 V, V_{IN} = 3.465 V			150	µA
		CLK	VDD = 3.465 V, V_{IN} = 3.465 V			150	
I_{IL}	Input Low Current(3)	nCLK	VDD = 3.465 V , V_{IN} = 0 V	-150			µA
		CLK	VDD = 3.465 V, V_{IN} = 0 V	-5			

(1) V_{IL} should not be less than -0.3 V.
(2) Input common mode voltage is defined as V_{IH}.
(3) For I_{IH} and I_{IL} measurements on CLK or nCLK, one must comply with V_{ID} and V_{ICM} specifications by using the appropriate bias on nCLK or CLK.

8.9 Electrical Characteristics (VDDO = 3.3 V ± 5%)

Over recommended operating free-air temperature range (unless otherwise noted), VDD = VDDO = 3.3V ± 5%, All AC parameters measured at ≤ 350 MHz unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Maximum Output Frequency(1)(2)					350	MHz
t_{PDLH}	Propagation Delay, Low to High(3)	LVCMOS_CLK(4), CLK/nCLK(5)	0°C to 70°C	1.1		2.1	ns
			–40°C to 85°C	0.95		2.2	ns
$t_{SK(O)}$	Output Skew(2)(6)(7)		Measured on rising edge			35	ps
$t_{SK(PP)}$	Part-to-Part Skew(3)(7)(8)					700	ps
t_R/t_F	Output Rise/Fall Time(3)		20% to 80%	50		700	ps
J_{ADD}	Additive Jitter(9)		f=125 MHz, Input slew rate ≥ 3 V/ns, 12 kHz to 20 MHz integration band		0.04		ps RMS

(1) There is no minimum input / output frequency provided the input slew rate is sufficiently fast. Refer to *Input Slew Rate Considerations*.
(2) These AC parameters are specified by characterization. Not tested in production.
(3) These AC parameters are specified by design. Not tested in production
(4) Measured from the VDD/2 of the input to the VDDO/2 of the output.
(5) Measured from the differential input crossing point to VDDO/2 of the output.
(6) Defined as skew between outputs at the same supply voltage and with equal loading conditions. Measured at VDDO/2 of the output.
(7) Parameter is defined in accordance with JEDEC Standard 65.
(8) Calculation for part-to-part skew is the difference between the fastest and slowest t_{PD} across multiple devices, operating at the same supply voltage, same frequency, same temperature, with equal load conditions, and using the same type of inputs on each device.
(9) Buffer Additive Jitter: $J_{ADD} = SQRT(J_{SYSTEM}{}^2 - J_{SOURCE}{}^2)$, where J_{SYSTEM} is the RMS jitter of the system output (source+buffer) and J_{SOURCE} is the RMS jitter of the input source, and system output noise is not correlated to the input source noise. Additive jitter should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality ultra-low-noise oscillators. Please refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.

Electrical Characteristics (VDDO = 3.3 V ± 5%) (continued)

Over recommended operating free-air temperature range (unless otherwise noted), VDD = VDDO = 3.3V ± 5%, All AC parameters measured at ≤ 350 MHz unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN_{FLOOR}	Phase Noise Floor(10)	f = 125 MHz, Input slew rate ≥ 3 V/ns				dBc/Hz
		10 kHz offset		-155		
		100 kHz offset		-162		
		1 MHz offset		-166		
		10 MHz offset		-166		
		20 MHz offset		-166		
ODC	Output Duty Cycle(3)(11)	REF = CLK/nCLK	45%		55%	
		REF = LVCMOS_CLK, f ≤ 300 MHz	45%		55%	
t_{EN}	Output Enable Time			5		ns
t_{DIS}	Output Disable Time			5		ns

(10) Buffer Phase Noise Floor: PN_{FLOOR} (dBc/Hz) = 10 x log10[10^(PN_{SYSTEM}/10) – 10^(PN_{SOURCE}/10)], where PN_{SYSTEM} is the phase noise floor of the system output (source+buffer) and PN_{SOURCE} is the phase noise floor of the input source. Buffer Phase Noise Floor should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality ultra-low-noise oscillators. Please refer to System-Level Phase Noise and Additive Jitter Measurement for input source and measurement details.
(11) 50% Input duty cycle

8.10 Electrical Characteristics (VDDO = 2.5 V ± 5%)

Over recommended operating free-air temperature range (unless otherwise noted), VDD = 3.3V ± 5%, VDDO = 2.5V ± 5%, All AC parameters measured at ≤ 350 MHz unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Maximum Output Frequency(1) (2)					350	MHz
t_{PDLH}	Propagation Delay, Low to High(3)	LVCMOS_CLK(4), CLK/nCLK(5)	0°C to 70°C	1.1		2.1	ns
			–40°C to 85°C	0.95		2.2	
$t_{SK(O)}$	Output Skew(2)(6)(7)		Measured on rising edge			35	ps
$t_{SK(PP)}$	Part-to-Part Skew(3)(7)(8)					700	ps
t_R/t_F	Output Rise/Fall Time(3)		20% to 80%	50		700	ps
J_{ADD}	Additive Jitter(9)		f=125 MHz, Input slew rate ≥ 3 V/ns, 12 kHz to 20 MHz integration band		0.04		ps RMS
ODC	Output Duty Cycle(3)(10)		REF = CLK/nCLK	45%		55%	
			REF = LVCMOS_CLK, f ≤ 300 MHz	45%		55%	
t_{EN}	Output Enable Time				5		ns
t_{DIS}	Output Disable Time				5		ns

(1) There is no minimum input / output frequency provided the input slew rate is sufficiently fast. Refer to *Input Slew Rate Considerations*.
(2) These AC parameters are specified by characterization. Not tested in production.
(3) These AC parameters are specified by design. Not tested in production.
(4) Measured from the VDD/2 of the input to the VDDO/2 of the output.
(5) Measured from the differential input crossing point to VDDO/2 of the output.
(6) Defined as skew between outputs at the same supply voltage and with equal loading conditions. Measured at VDDO/2 of the output.
(7) Parameter is defined in accordance with JEDEC Standard 65.
(8) Calculation for part-to-part skew is the difference between the fastest and slowest t_{PD} across multiple devices, operating at the same supply voltage, same frequency, same temperature, with equal load conditions, and using the same type of inputs on each device.
(9) Buffer Additive Jitter: J_{ADD} = SQRT(J_{SYSTEM}^2 - J_{SOURCE}^2), where J_{SYSTEM} is the RMS jitter of the system output (source+buffer) and J_{SOURCE} is the RMS jitter of the input source, and system output noise is not correlated to the input source noise. Additive jitter should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality ultra-low-noise oscillators. Please refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.
(10) 50% Input Duty Cycle

8.11 Electrical Characteristics (VDDO = 1.8 V ± 0.15 V)

Over recommended operating free-air temperature range (unless otherwise noted), VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 0.15 V. All AC parameters measured at ≤ 350 MHz unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Maximum Output Frequency(1)(2)					350	MHz
t_{PDLH}	Propagation Delay, Low to High(3)	LVCMOS_CLK(4), CLK/nCLK(5)	0°C to 70°C	1.1		2.2	ns
			–40°C to 85°C	0.95		2.3	ns
$t_{SK(O)}$	Output Skew(2)(6)(7)		Measured on rising edge			35	ps
$t_{SK(PP)}$	Part-to-Part Skew(3)(7)(8)					700	ps
t_R/t_F	Output Rise/Fall Time(3)		20% to 80%	100		700	ps
J_{ADD}	Additive Jitter(9)		f=125 MHz, Input slew rate ≥ 3 V/ns, 12 kHz to 20 MHz integration band		0.04		ps RMS
ODC	Output Duty Cycle(3)(10)		REF = CLK/nCLK	45%		55%	
			REF = LVCMOS_CLK, f ≤ 300 MHz	45%		55%	
t_{EN}	Output Enable Time				5		ns
t_{DIS}	Output Disable Time				5		ns

(1) There is no minimum input / output frequency provided the input slew rate is sufficiently fast. Refer to *Input Slew Rate Considerations*.
(2) These AC parameters are specified by characterization. Not tested in production.
(3) These AC parameters are specified by design. Not tested in production.
(4) Measured from the VDD/2 of the input to the VDDO/2 of the output.
(5) Measured from the differential input crossing point to VDDO/2 of the output.
(6) Defined as skew between outputs at the same supply voltage and with equal loading conditions. Measured at VDDO/2 of the output.
(7) Parameter is defined in accordance with JEDEC Standard 65.
(8) Calculation for part-to-part skew is the difference between the fastest and slowest t_{PD} across multiple devices, operating at the same supply voltage, same frequency, same temperature, with equal load conditions, and using the same type of inputs on each device.
(9) Buffer Additive Jitter: $J_{ADD} = SQRT(J_{SYSTEM}^2 - J_{SOURCE}^2)$, where J_{SYSTEM} is the RMS jitter of the system output (source+buffer) and J_{SOURCE} is the RMS jitter of the input source, and system output noise is not correlated to the input source noise. Additive jitter should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality ultra-low-noise oscillators. Please refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.
(10) 50% Input Duty Cycle

8.12 Electrical Characteristics (VDDO = 1.5 V ± 5%)

Over recommended operating free-air temperature range (unless otherwise noted), VDD = 3.3V ± 5%, VDDO = 1.5V ± 5%, All AC parameters measured at ≤ 350 MHz unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Maximum Output Frequency[1][2]					350	MHz
t_{PDLH}	Propagation Delay, Low to High[3]	LVCMOS_CLK[4], CLK/nCLK[5]	0°C to 70°C	1.1		2.2	ns
			–40°C to 85°C	0.95		2.3	ns
$t_{SK(O)}$	Output Skew[2][6][7]		Measured on rising edge			35	ps
$t_{SK(PP)}$	Part-to-Part Skew[2][7][8]					1	ns
t_R/t_F	Output Rise/Fall Time[3]		20% to 80%	100		900	ps
J_{ADD}	Additive Jitter[9]		f=125 MHz, Input slew rate ≥ 3 V/ns, 12 kHz to 20 MHz integration band		0.04		ps RMS
ODC	Output Duty Cycle[3][10]		f ≤ 166 MHz	45%		55%	
			f > 166 MHz	42%		58%	
t_{EN}	Output Enable Time				5		ns
t_{DIS}	Output Disable Time				5		ns

(1) There is no minimum input / output frequency provided the input slew rate is sufficiently fast. Refer to *Input Slew Rate Considerations*.
(2) These AC parameters are specified by characterization. Not tested in production.
(3) These AC parameters are specified by design. Not tested in production.
(4) Measured from the VDD/2 of the input to the VDDO/2 of the output.
(5) Measured from the differential input crossing point to VDDO/2 of the output.
(6) Defined as skew between outputs at the same supply voltage and with equal loading conditions. Measured at VDDO/2 of the output.
(7) Parameter is defined in accordance with JEDEC Standard 65.
(8) Calculation for part-to-part skew is the difference between the fastest and slowest t_{PD} across multiple devices, operating at the same supply voltage, same frequency, same temperature, with equal load conditions, and using the same type of inputs on each device.
(9) Buffer Additive Jitter: $J_{ADD} = SQRT(J_{SYSTEM}^2 - J_{SOURCE}^2)$, where J_{SYSTEM} is the RMS jitter of the system output (source+buffer) and J_{SOURCE} is the RMS jitter of the input source, and system output noise is not correlated to the input source noise. Additive jitter should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality ultra-low-noise oscillators. Please refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.
(10) 50% Input Duty Cycle

8.13 Typical Characteristics

Unless otherwise noted: VDD = 3.3 V, VDDO = 3.3 V, T_A = 25°C

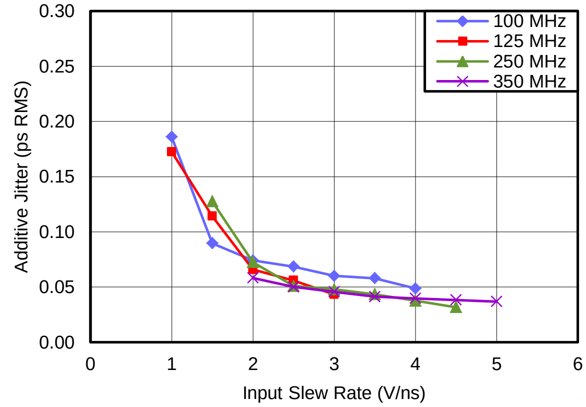


Figure 1. Additive Jitter vs Input Slew Rate

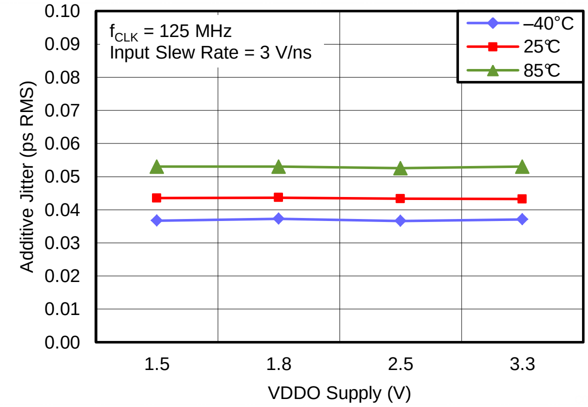


Figure 2. Additive Jitter vs VDDO Supply and Temperature

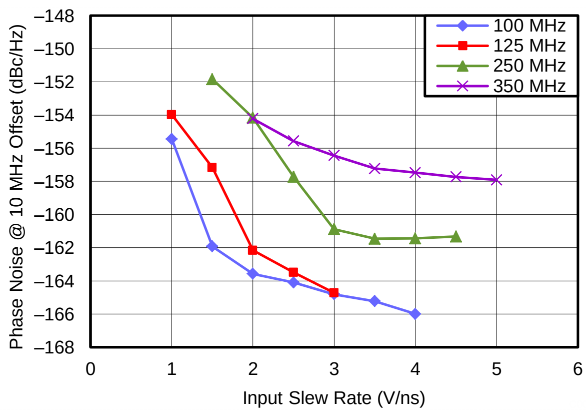


Figure 3. Phase Noise Floor vs Input Slew Rate

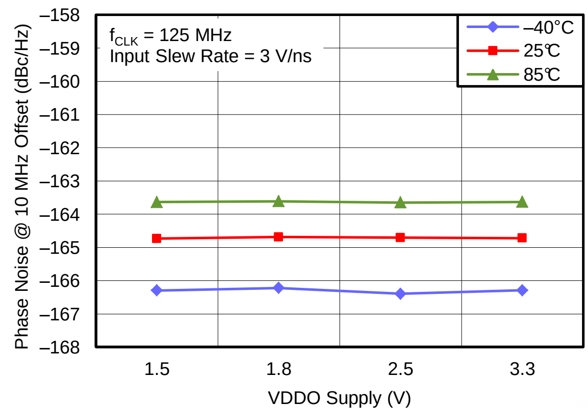
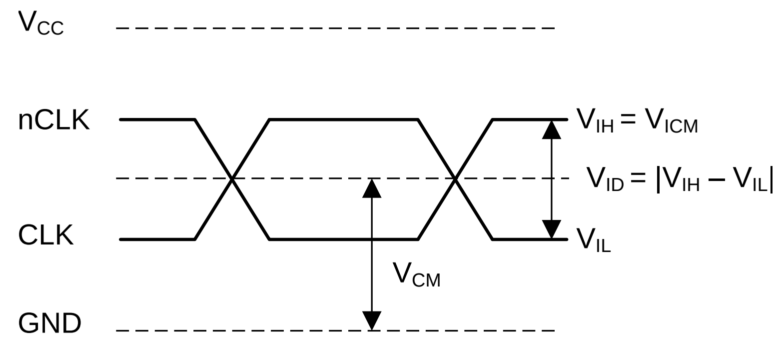


Figure 4. Phase Noise Floor vs VDDO Supply and Temperature

9 Parameter Measurement Information



NOTE: $V_{CM} = V_{ICM} - V_{ID}/2 = (V_{IH} + V_{IL})/2$

Figure 5. Differential Input Level

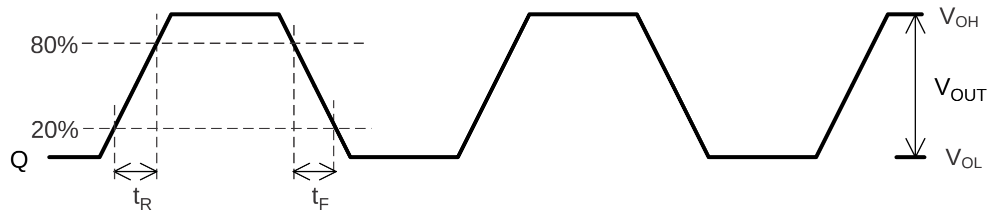


Figure 6. Output Voltage, and Rise and Fall Times

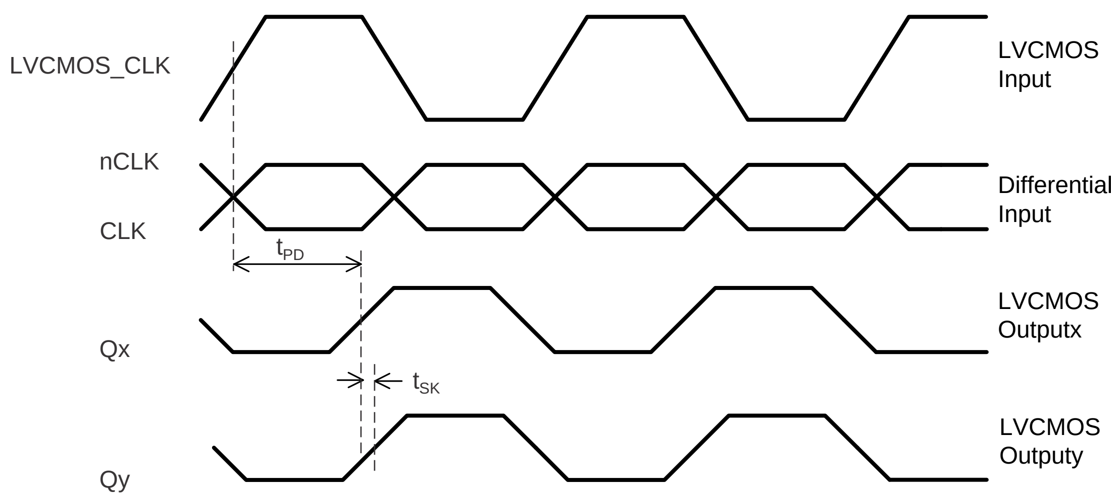


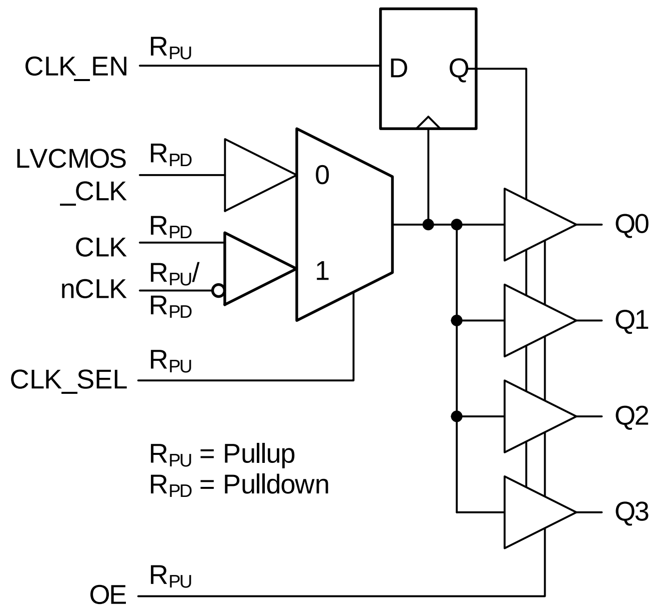
Figure 7. Output Skew and Propagation Delay

10 Detailed Description

10.1 Overview

The LMK00804B is a low skew, high performance clock fanout buffer which can distribute up to four LVCMOS/LVTTL outputs (3.3-V, 2.5-V, 1.8-V, or 1.5-V levels) from one of two selectable inputs, which can accept differential or single-ended inputs. The clock enable input is synchronized internally to eliminate runt or glitch pulses on the outputs when the clock enable terminal is asserted or de-asserted. The outputs are held in logic low state when the clock is disabled. A separate output enable terminal controls whether the outputs are active state or high-impedance state. The low additive jitter and phase noise floor, and guaranteed output and part-to-part skew characteristics make the LMK00804B ideal for applications demanding high performance and repeatability.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Clock Enable Timing

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 8. In the enabled mode, the output states are a function of the CLK/nCLK or LVCMOS_CLK inputs as described in *Clock Input Function*.

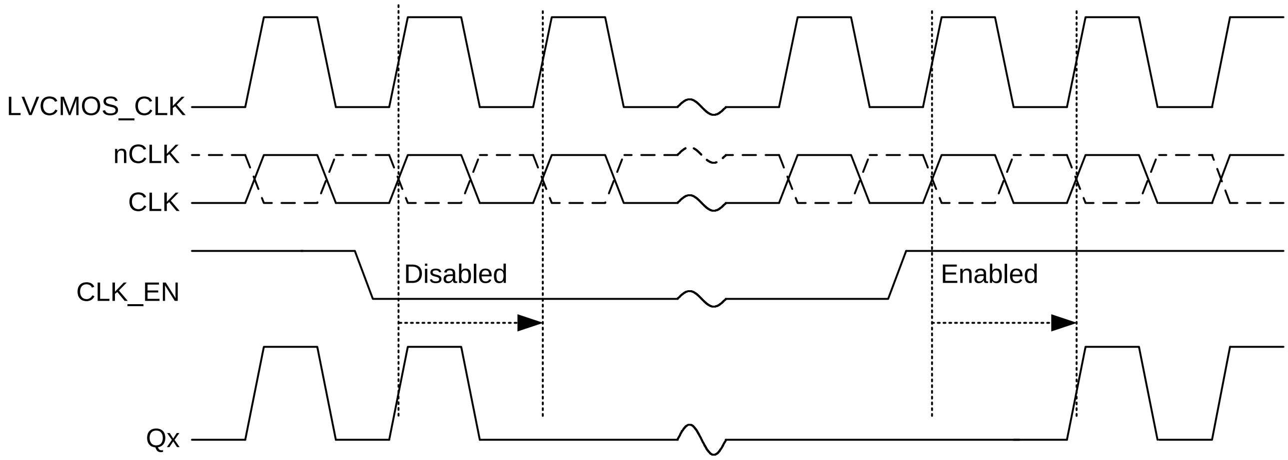


Figure 8. Clock Enable Timing Diagram

10.4 Device Functional Modes

The device can provide fan-out and level translation from differential or single-ended input to LVCMOS/LVTTL output, where the output VOH and VOL levels are determined by the VDDO output supply voltage and output load condition. Refer to the *Clock Input Function*.

10.4.1 Clock Input Function

Table 1.

INPUTS		OUTPUTS	INPUT to OUTPUT MODE	POLARITY
CLK (or LVCMOS_CLK)	nCLK	Qx		
0	1	LOW	Differential (or Single-Ended) to Single-Ended	Non-inverting
1	0	HIGH	Differential (or Single-Ended) to Single-Ended	Non-inverting
0	Floating or Biased	LOW	Single-Ended to Single-Ended	Non-inverting
1	Floating or Biased	HIGH	Single-Ended to Single-Ended	Non-inverting
Biased	0	HIGH	Single-Ended to Single-Ended	Inverting
Biased	1	LOW	Single-Ended to Single-Ended	Inverting

11 Applications and Implementation

11.1 Application Information

Refer to the following sections for output clock and input clock interface circuits.

11.2 Output Clock Interface Circuit

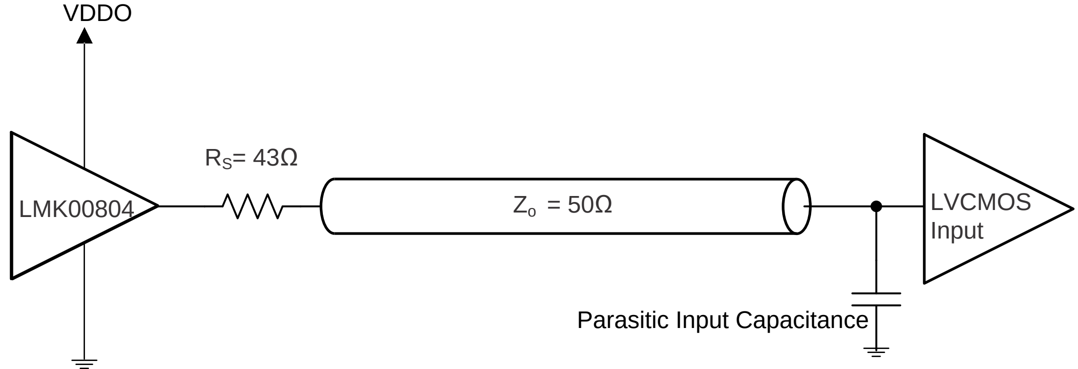


Figure 9. LVCMOS Output Configuration

11.3 Input Detail

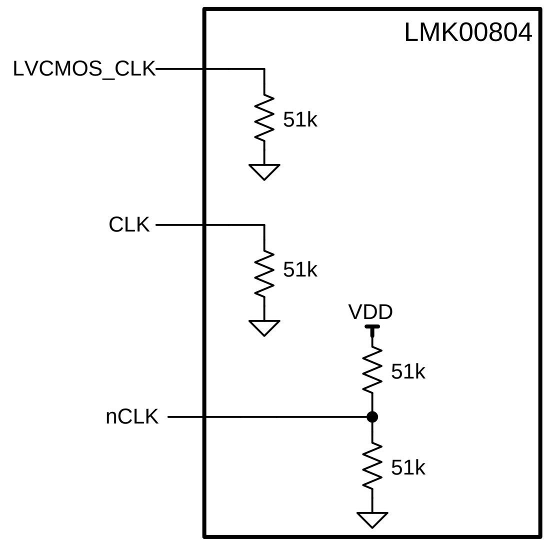


Figure 10. Clock Input Components

11.4 Input Clock Interface Circuits

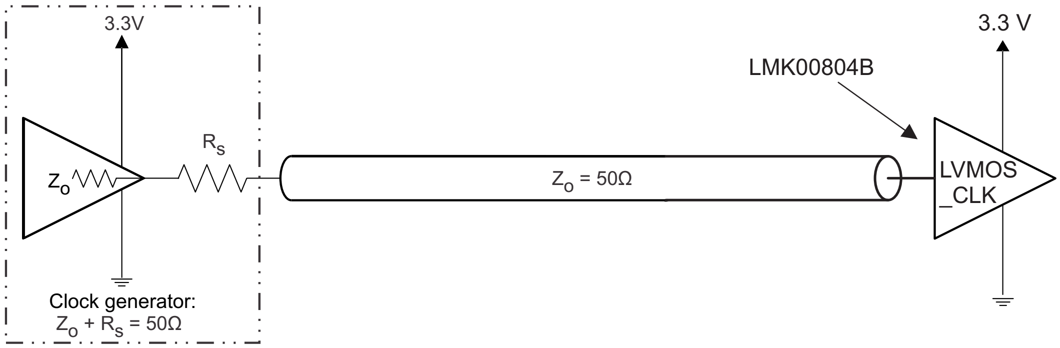
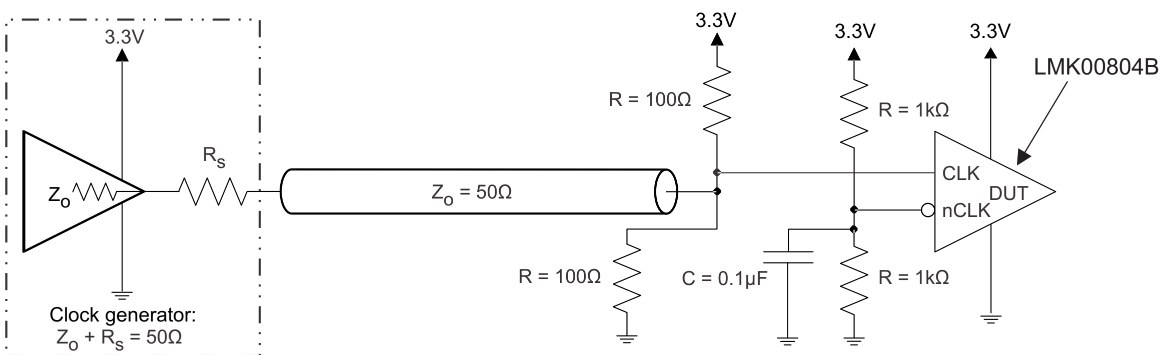


Figure 11. LVCMOS_CLK Input Configuration



(1) The Thevenin/split termination values (R = 100 Ω) at the CLK input may be adjusted to provide a small differential offset voltage (50 mV, for example) between the CLK and nCLK inputs to prevent input chatter if the LVCMOS driver is tri-stated. For example, using 105 Ω 1% to 3.3 V rail and 97.6 Ω 1% to GND will provide a –60 mV offset voltage (V_{nCLK}-V_{CLK}) and ensure a logic low state if the LVCMOS driver is tri-stated.

Figure 12. Single-Ended/LVCMOS Input DC Configuration

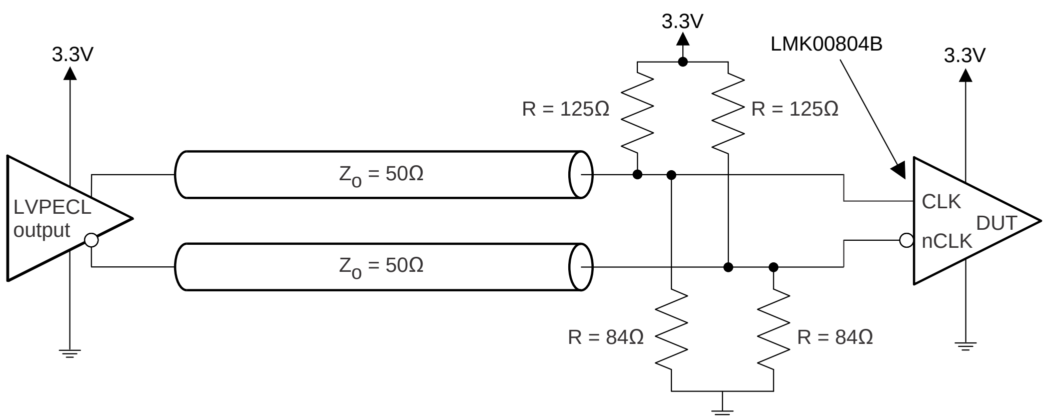


Figure 13. LVPECL Input Configuration

Input Clock Interface Circuits (continued)

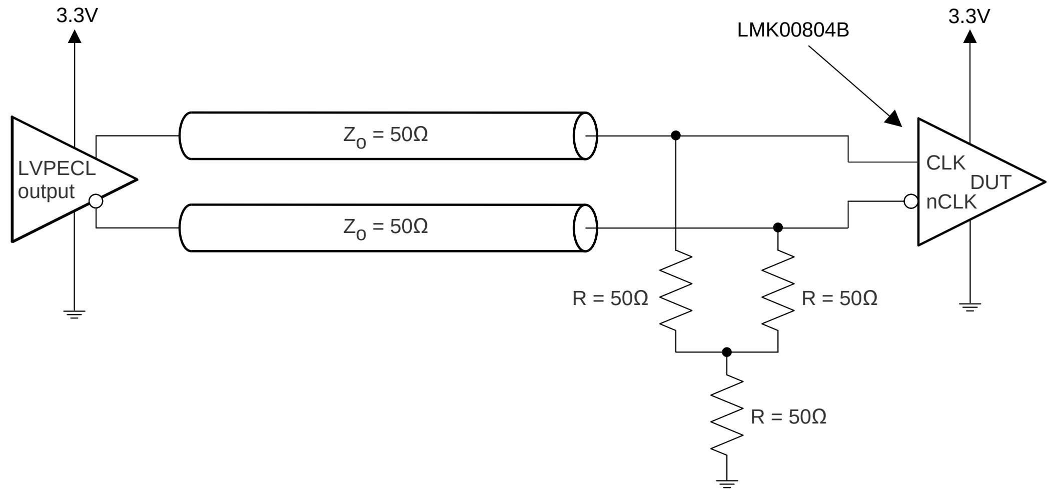


Figure 14. Alternative LVPECL Input Configuration

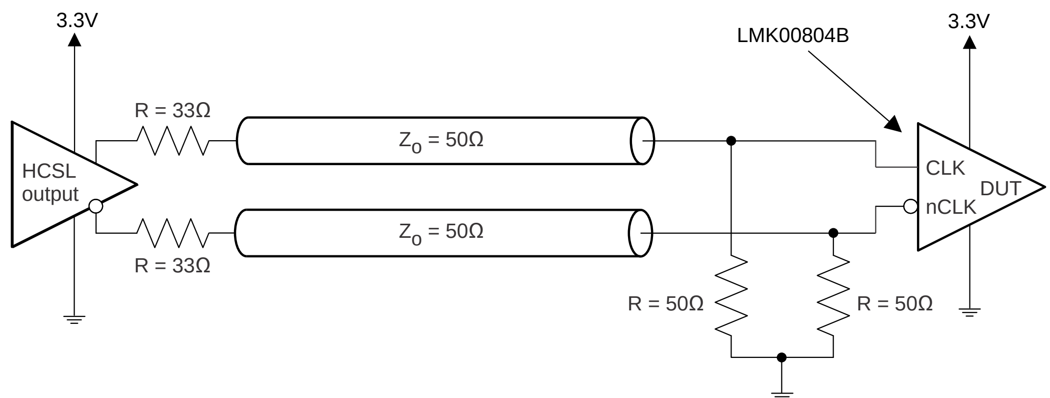


Figure 15. HCSL Input Configuration

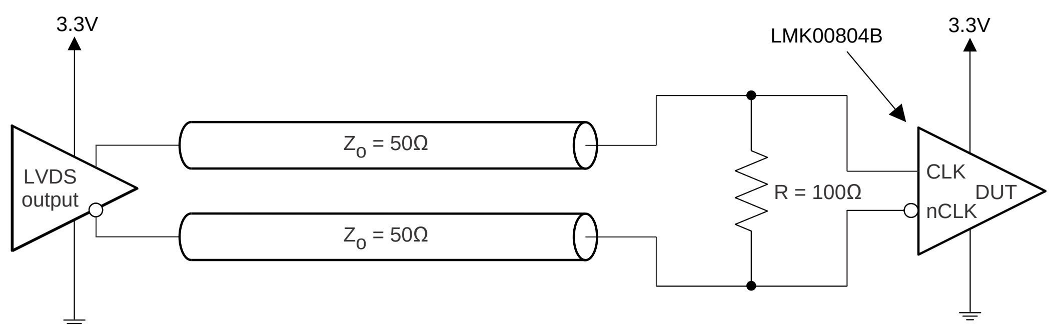


Figure 16. LVDS Input Configuration

Input Clock Interface Circuits (continued)

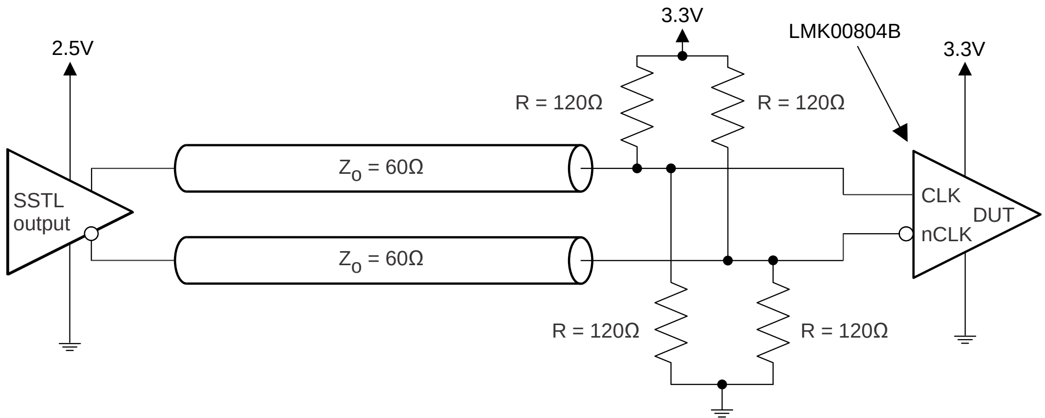


Figure 17. SSTL Input Configuration

11.5 Typical Applications

11.5.1 Design Requirements

For high-performance devices, limitations of the equipment influence phase-noise measurements. The noise floor of the equipment is often higher than the noise floor of the device. The real noise floor of the device is probably lower. It is important to understand that system-level phase noise measured at the DUT output is influenced by the input source and the measurement equipment.

For Figure 18 and Figure 19 system-level phase noise plots, a Rohde & Schwarz SMA100A low-noise signal generator was cascaded with an Agilent 70429A K95 single-ended to differential converter block with ultra-low phase noise and fast edge slew rate (>3 V/ns) to provide a very low-noise clock input source to the LMK00804B. An Agilent E5052 source signal analyzer with ultra-low measurement noise floor was used to measure the phase noise of the input source (SMA100A + 70429A K95) and system output (input source + LMK00804B). The input source phase noise is shown by the light yellow trace, and the system output phase noise is shown by the dark yellow trace.

11.5.2 Detailed Design Procedure

The additive phase noise or noise floor of the buffer (PN_{FLOOR}) can be computed as follows:

$$PN_{FLOOR}\ (dBc/Hz) = 10 \times \log10[10^{\wedge}(PN_{SYSTEM}/10) - 10^{\wedge}(PN_{SOURCE}/10)]$$

where

- PN_{SYSTEM} is the phase noise of the system output (source+buffer)
- PN_{SOURCE} is the phase noise of the input source (1)

The additive jitter of the buffer (J_{ADD}) can be computed as follows:

$$J_{ADD} = SQRT(J_{SYSTEM}^2 - J_{SOURCE}^2)$$

where:

- J_{SYSTEM} is the RMS jitter of the system output (source+buffer), integrated from 10 kHz to 20 MHz
- J_{SOURCE} is the RMS jitter of the input source, integrated from 10 kHz to 20 MHz (2)

Typical Applications (continued)

11.5.3 Application Curves

11.5.3.1 System-Level Phase Noise and Additive Jitter Measurement

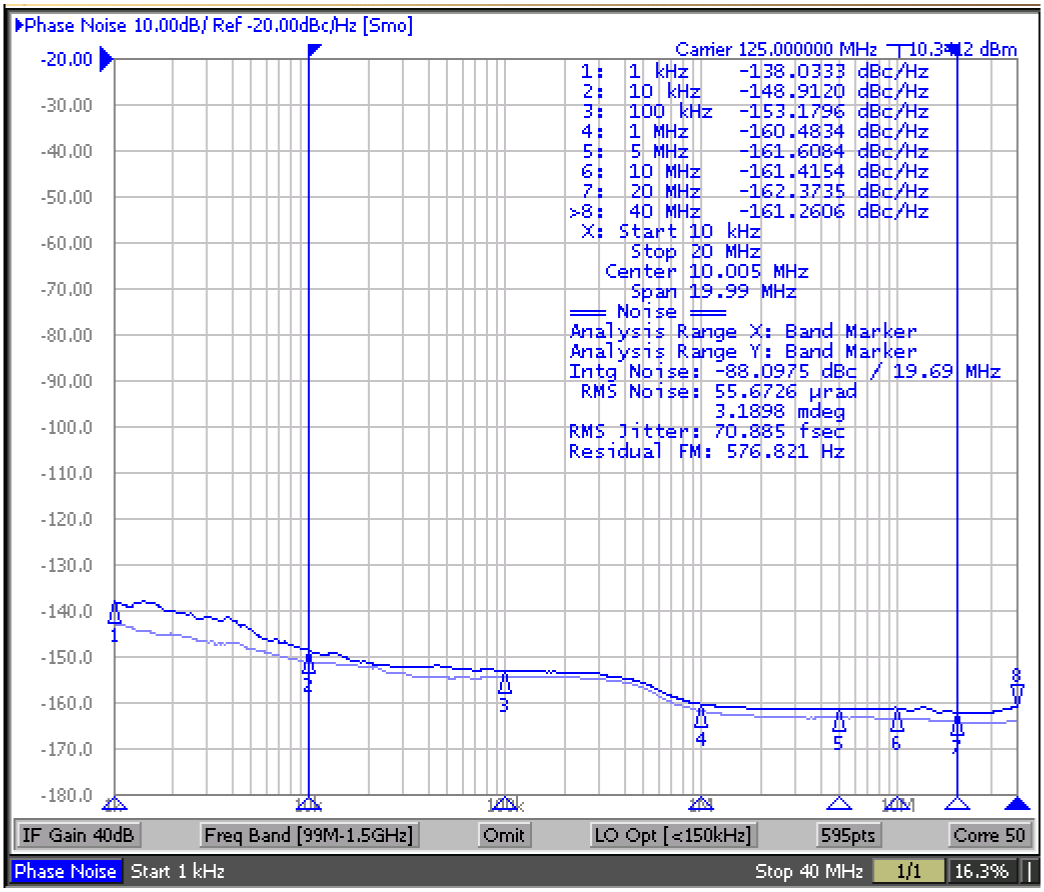


Figure 18.
125 MHz Input Phase Noise (57 fs rms, Light Blue), and Output Phase Noise (71 fs rms, Dark Blue), Additive Jitter = 42 fs rms

Typical Applications (continued)

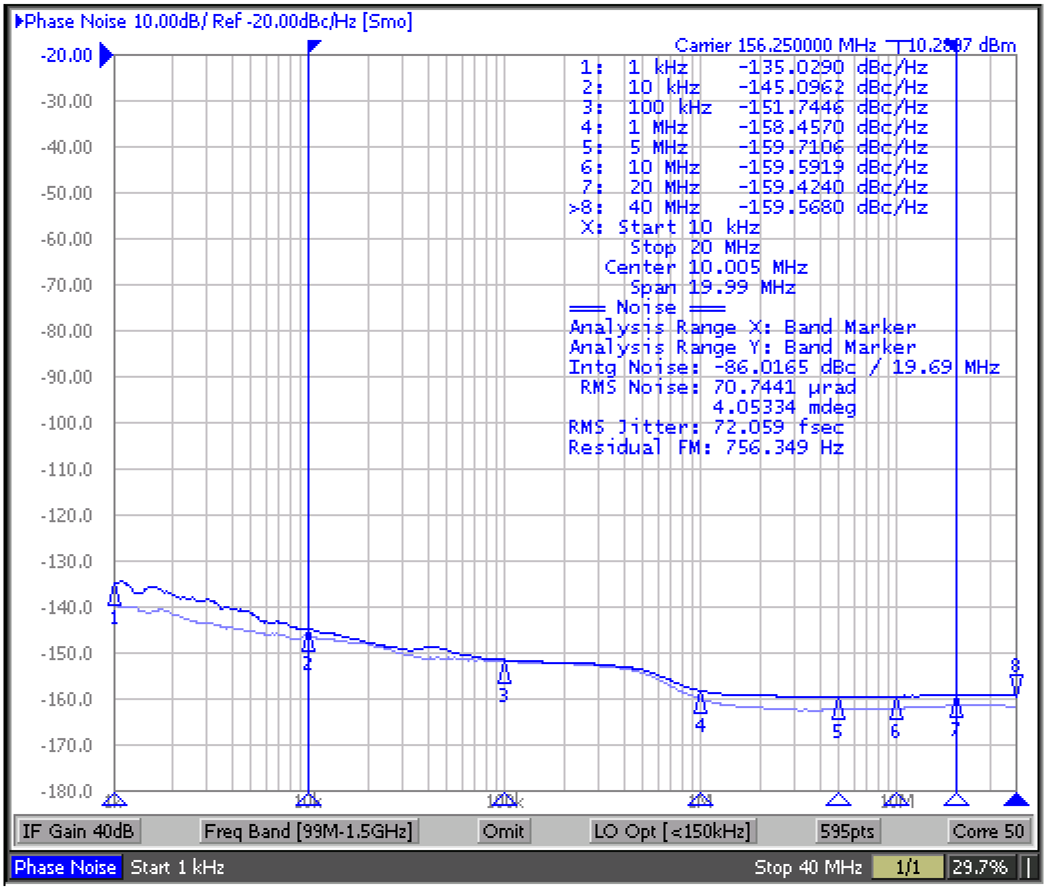


Figure 19.
156.25 MHz Input Phase Noise (57 fs rms, Light Blue), and Output Phase Noise (72 fs rms, Dark Blue), Additive Jitter = 44 fs rms

11.6 Do's and Don'ts

11.6.1 Power Considerations

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states
- Power required to charge any output load

The output load can be capacitive-only or capacitive and resistive. Use the following formula to calculate the power consumption of the device:

$$P_{Dev} = P_{stat} + P_{dyn} + P_{Cload} \quad (3)$$

$$P_{stat} = (I_{DD} \times V_{DD}) + (I_{DDO} \times V_{DDO}) \quad (4)$$

$$P_{dyn} + P_{Cload} = (I_{DDO,dyn} + I_{DDO,Cload}) \times V_{DDO}$$

where:

- $I_{DDO,dyn} = C_{PD} \times V_{DDO} \times f \times n$ [mA]
- $I_{DDO,Cload} = C_{load} \times V_{DDO} \times f \times n$ [mA] (5)

Example for power consumption of the LMK00804B: 4 outputs are switching, f = 100 MHz,

VDD = VDDO = 3.465 V and assuming C_{load} = 5 pF per output:

$$P_{Dev} = 90 \text{ mW} + 34 \text{ mW} = 124 \text{ mW} \quad (6)$$

$$P_{stat} = (21 \text{ mA} \times 3.465 \text{ V}) + (5 \text{ mA} \times 3.465 \text{ V}) = 90 \text{ mW} \quad (7)$$

$$P_{dyn} + P_{Cload} = (2.8 \text{ mA} + 6.9 \text{ mA}) \text{ x } 3.465 \text{ V} = 34 \text{ mW} \quad (8)$$

$$I_{DD,dyn} = 2 \text{ pF} \times 3.465 \text{ V} \times 100 \text{ MHz} \times 4 = 2.8 \text{ mA} \quad (9)$$

$$I_{DD,Cload} = 5 \text{ pF} \times 3.465 \text{ V x } 100 \text{ MHz} \times 4 = 6.9 \text{ mA} \quad (10)$$

NOTE

For dimensioning the power supply, consider the total power consumption. The total power consumption is the sum of device power consumption and the power consumption of the load.

Do's and Don'ts (continued)

11.6.2 Recommendations for Unused Input and Output Pins

- **CLK_SEL, CLK_EN, and OE:** These inputs all have internal pull-up (R_{PU}) according to Table 2 and can be left floating if unused. Table 2 shows the default floating state of these inputs:

Table 2. Input Floating Default States

INPUT	FLOATING STATE SELECTION
CLK_SEL	CLK/nCLK selected
CLK_EN	Synchronous outputs enable
OE	Outputs enabled

- **CLK/nCLK Inputs:** See Figure 10 for the internal connections. When using single ended input, take note of the internal pull-up and pull-down to make sure the unused input is properly biased. To interface a single-ended input to the CLK/nCLK input, the configuration shown in Figure 12 is recommended.
- **LVCMOS_CLK Input:** See Figure 10 for the internal connection. The internal pull-down (R_{PD}) resistor ensures a low state when this input is left floating.
- **Outputs:** Any unused output can be left floating with no trace connected.

11.6.3 Input Slew Rate Considerations

LMK00804B employs high-speed and low-latency circuit topology, allowing the device to achieve ultra-low additive jitter/phase noise and high-frequency operation. To take advantage of these benefits in the system application, it is optimal for the input signal to have a high slew rate of 3 V/ns or greater. Driving the input with a slower slew rate can degrade the additive jitter and noise floor performance. For this reason, a differential signal input is recommended over single-ended because it typically provides higher slew rate and common-mode-rejection. Refer to the “Additive Jitter vs. Input Slew Rate” plots in *Typical Characteristics*. Also, using an input signal with very slow input slew rate, such as less than 0.05 V/ns, has the tendency to cause output switching noise to feed-back to the input stage and cause the output to chatter. This is especially true when driving either input in single-ended fashion with a very slow slew rate, such as a sine-wave input signal.

12 Power Supply Recommendations

12.1 Power Supply Considerations

While there is no strict power supply sequencing requirement, it is generally best practice to sequence the core supply voltage (VDD) before the output supply voltage (VDDO).

12.1.1 Power-Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Use of filter capacitors eliminates the low-frequency noise from power supply, where the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power-supply system against induced fluctuations. The bypass capacitors also provide instantaneous current surges as required by the device, and should have low ESR. To use the bypass capacitors properly, place them very close to the power supply terminals and lay out traces with short loops to minimize inductance. TI recommends to adding as many high-frequency (for example, 0.1 µF) bypass capacitors as there are supply terminals in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver, preventing them from leaking into the board supply. Choosing an appropriate ferrite bead with very low DC resistance is important, because it is imperative to provide adequate isolation between the board supply and the chip supply. It is also imperative to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

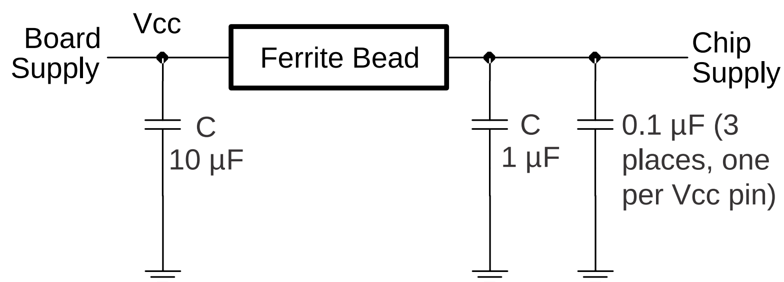


Figure 20. Power-Supply Decoupling

Power Supply Considerations (continued)

12.1.2 Thermal Management

For reliability and performance reasons, limit the die temperature to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125°C.

Assuming the conditions in the *Power Considerations* section and operating at an ambient temperature of 70°C with all outputs loaded, here is an estimate of the LMK00804B junction temperature:

$$T_J = T_A + P_{Total} \times \theta_{JA} = 70\ °C + (124\ mW \times 116\ °C/W) = 70\ °C + 14.4\ °C = 84.4\ °C \quad (11)$$

Here are some recommendations for improving heat flow away from the die:

- Use multi-layer boards
- Specify a higher copper thickness for the board
- Increase the number of vias from the top level ground plane under and around the device to internal layers and to the bottom layer with as much copper area flow on each level as possible
- Apply air flow
- Leave unused outputs floating

13 Layout

13.1 Layout Guidelines

13.1.1 Ground Planes

Solid ground planes are recommended as they provide a low-impedance return paths between the device and its bypass capacitors and its clock source and destination devices.

Avoid return paths of other system circuitry (for example, high-speed/digital logic, switching power supplies, and so forth) from passing through the local ground of the device to minimize noise coupling, which could induce added jitter and spurious noise.

13.1.2 Power Supply Pins

Follow the power supply schematic and layout example described in *Power-Supply Filtering*.

13.1.3 Differential Input Termination

- Place input termination or biasing resistors as close as possible to the CLK/nCLK pins.
- Avoid or minimize vias in the 50 Ω input traces to minimize impedance discontinuities. Intra-pair skew should be also be minimized on the differential input traces.
- If not used, CLK/nCLK inputs may be left floating.

13.1.4 LVCMOS Input Termination

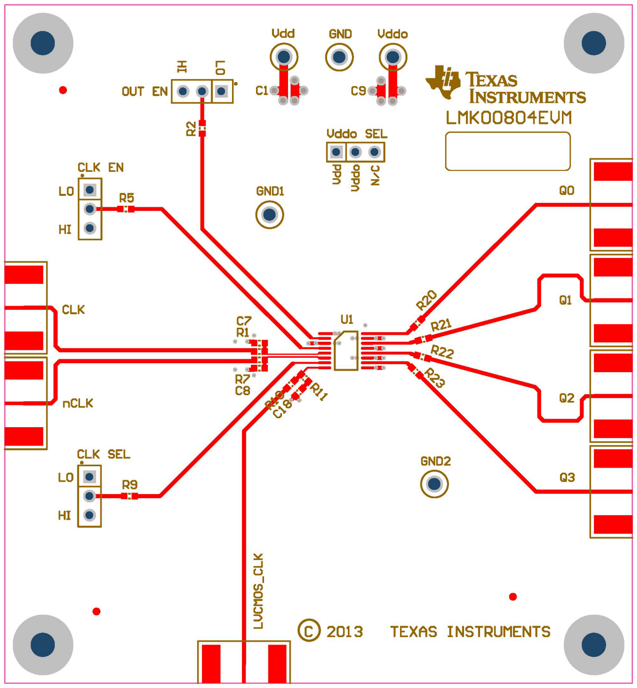
- When the LVCMOS_CLK input is driven from a LVCMOS driver that is series terminated to match the characteristic impedance of the trace, then input termination is not necessary; otherwise, place the input termination resistor as close as possible to the LVCMOS_CLK input.
- Avoid or minimize vias in the 50 Ω input trace to minimize impedance discontinuities.
- If not used, LVCMOS_CLK input may be left floating.

13.1.5 Output Termination

- Place 43 Ω series termination resistors as close as possible to the Qx outputs at the launch of the 50 Ω traces.
- Avoid or minimize vias in the 50 Ω input traces to minimize impedance discontinuities.
- If not used, any Qx output should be left floating and not routed.

13.2 Layout Example

Please refer to the LMK00804BEVM for a layout example. A sample PCB layer is shown below.



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: SV600950	REV: A	SVN REV: Not In VersionControl
LAYER NAME = Top Overlay			
PLOT NAME = Top Layer	GENERATED : 8/29/2013 12:57:54 PM		TEXAS INSTRUMENTS

Figure 21. Sample PCB Layout, Layer 1 (Top View)

14 器件和文档支持

14.1 器件支持

有关器件和文档支持，请直接访问 TI E2E 支持论坛查询时钟产品。

14.2 商标

All trademarks are the property of their respective owners.

14.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

14.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

15 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK00804BPW	ACTIVE	TSSOP	PW	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	K00804B	Samples
LMK00804BPWR	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	K00804B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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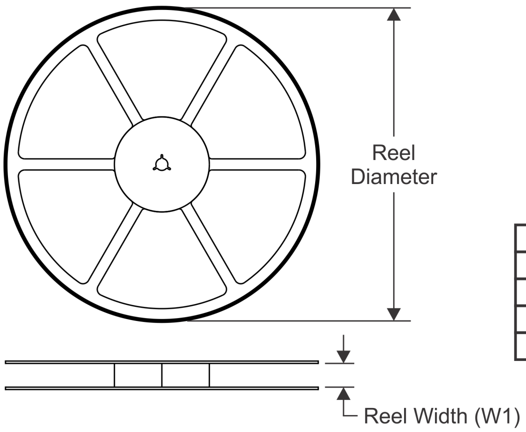
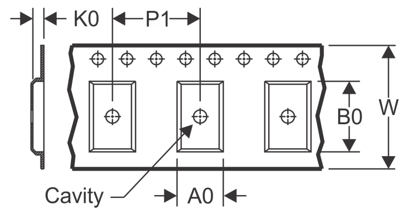
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

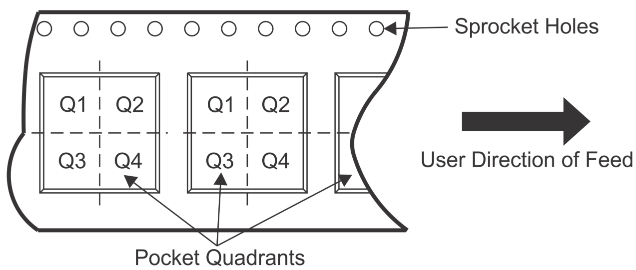


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

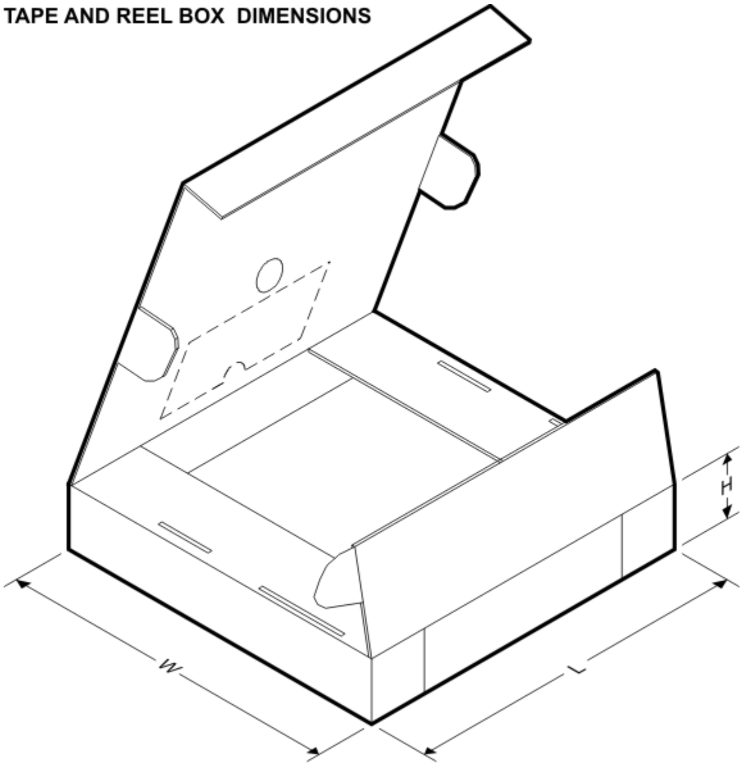
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK00804BPWR	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

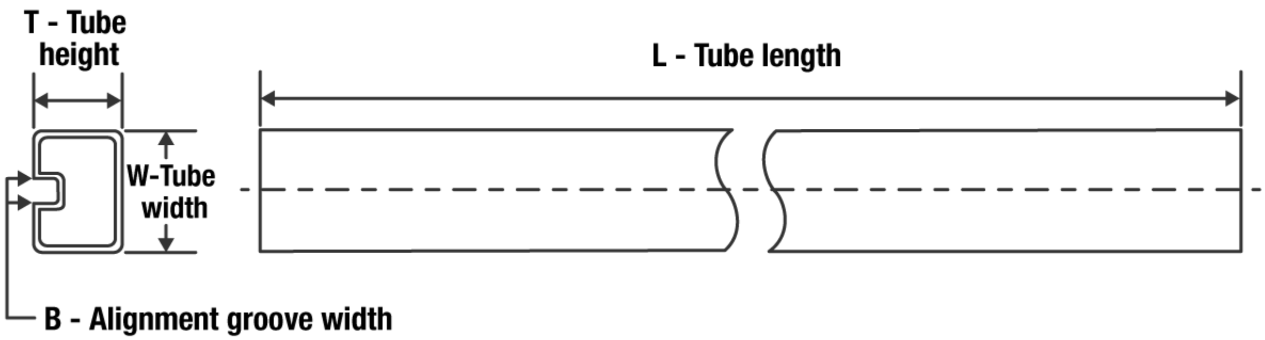
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

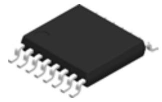
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK00804BPWR	TSSOP	PW	16	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

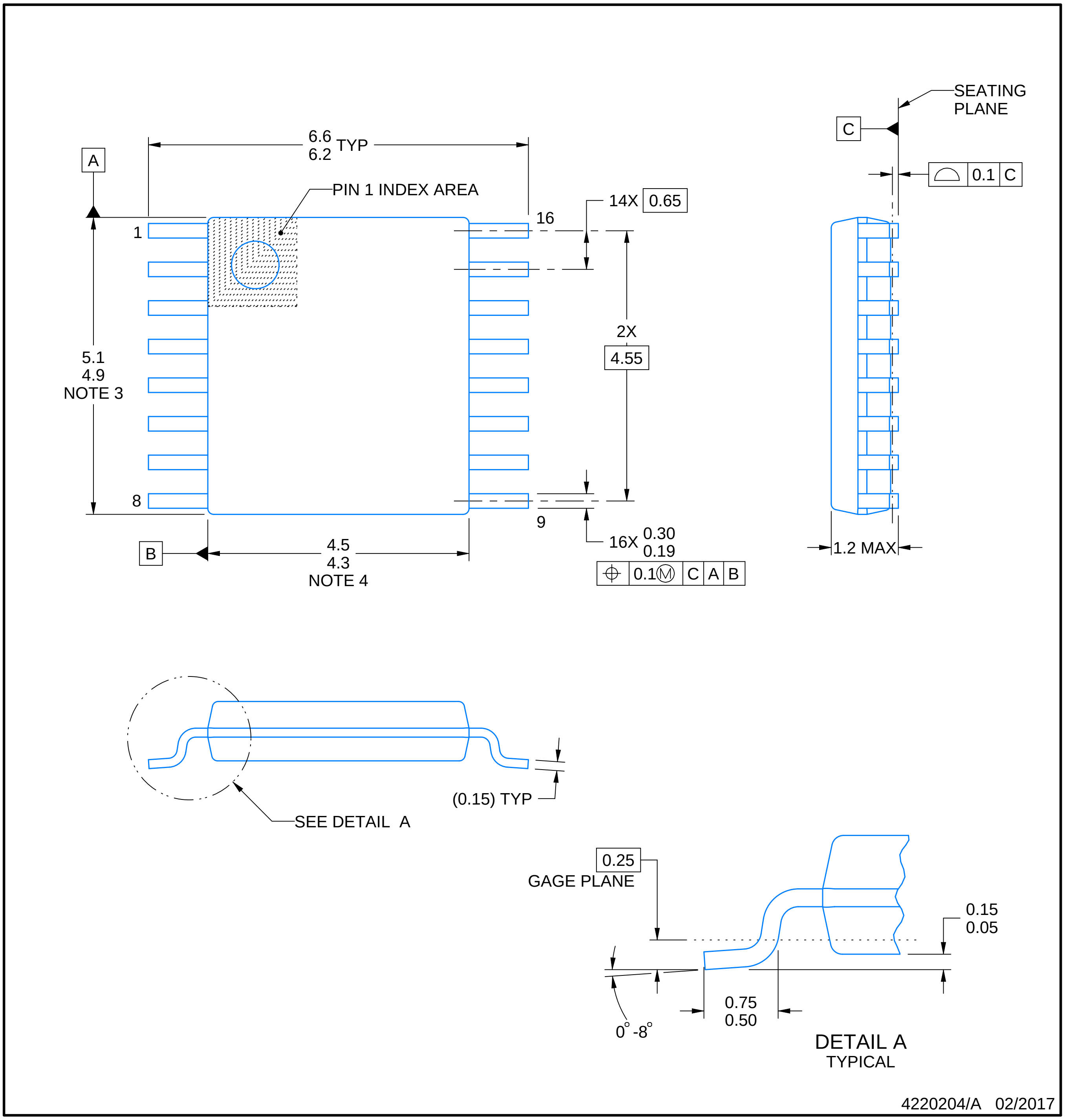
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMK00804BPW	PW	TSSOP	16	92	495	8	2514.6	4.06



PACKAGE OUTLINE

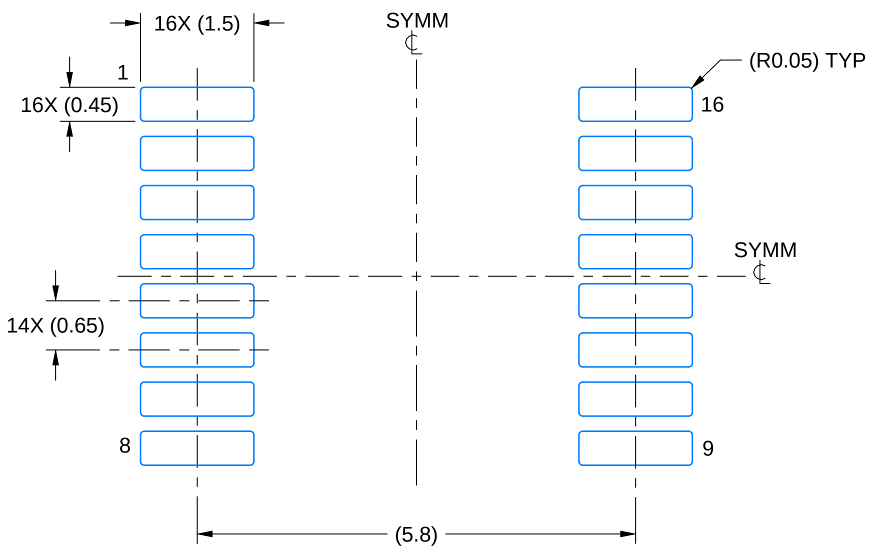
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

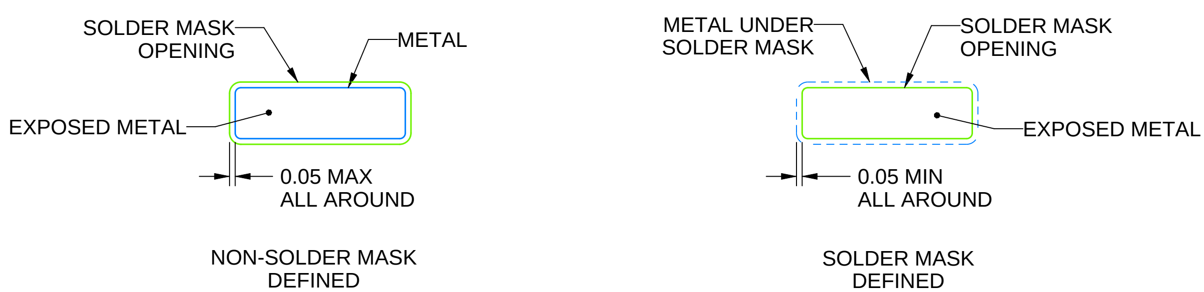


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

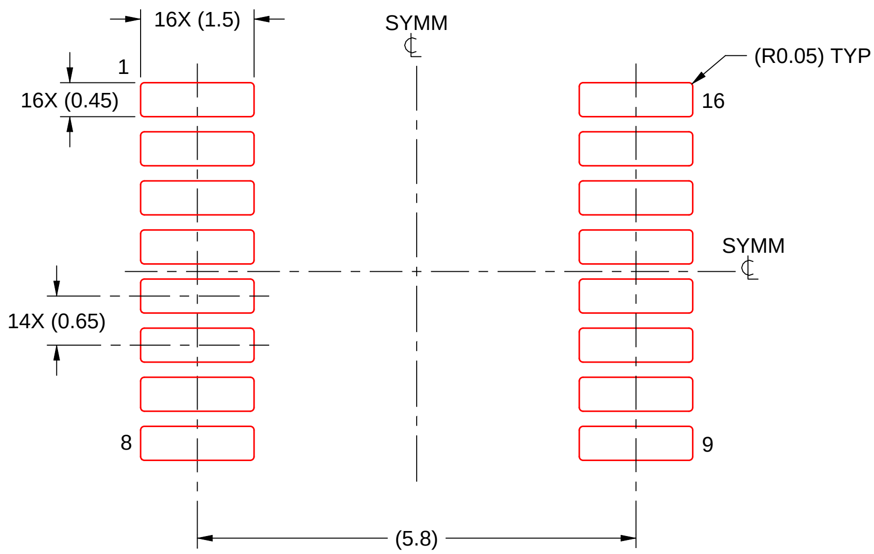


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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