



INA145

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Programmable Gain DIFFERENCE AMPLIFIER

FEATURES

- DIFFERENTIAL GAIN = 1V/V TO 1000V/V:
Set with External Resistors
- LOW QUIESCENT CURRENT: 570µA
- WIDE SUPPLY RANGE:
Single Supply: 4.5V to 36V
Dual Supplies: ±2.25V to ±18V
- HIGH COMMON-MODE VOLTAGE:
+8V at $V_S = +5V$
±28V at $V_S = ±15V$
- LOW GAIN ERROR: 0.01%
- HIGH CMR: 86dB
- SO-8 PACKAGE

DESCRIPTION

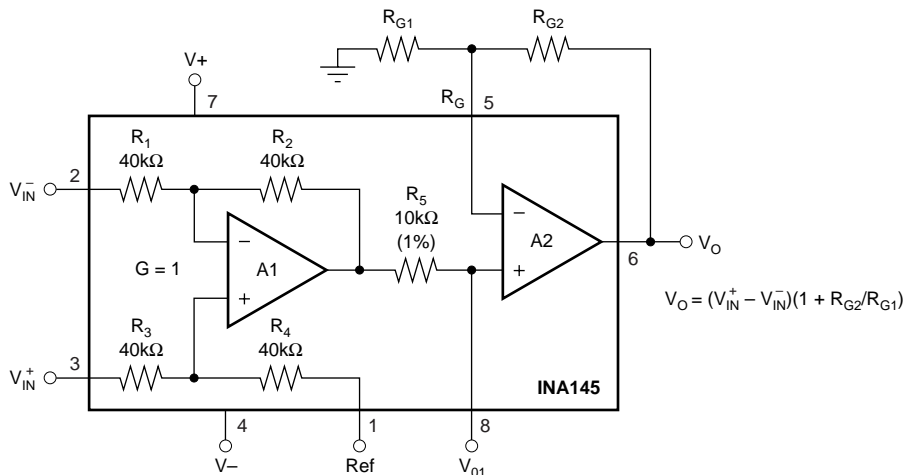
The INA145 is a precision, unity-gain difference amplifier consisting of a precision op amp and on-chip precision resistor network. Two external resistors set the gain from 1V/V to 1000V/V. The input common-mode voltage range extends beyond the positive and negative rails.

On-chip precision resistors are laser-trimmed to achieve accurate gain and high common-mode rejection. Excellent TCR tracking of these resistors assures continued high precision over temperature.

The INA145 is available in the SO-8 surface-mount package specified for the extended industrial temperature range, -40°C to +85°C.

APPLICATIONS

- CURRENT SHUNT MEASUREMENTS
- SENSOR AMPLIFIER
- DIFFERENTIAL LINE RECEIVER
- BATTERY POWERED SYSTEMS



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Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS: $V_S = \pm 2.25V$ to $\pm 18V$

Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+85^\circ C$

At $T_A = +25^\circ C$, $G = 1$, $R_L = 10k\Omega$ connected to ground and ref pin connected to ground unless otherwise noted.

PARAMETER	CONDITION	INA145UA			UNITS	
		MIN	TYP	MAX		
OFFSET VOLTAGE, V_O Input Offset Voltage vs Temperature vs Power Supply vs Time Offset Voltage, V_{O1}	RTI ^(1, 2) $V_{CM} = V_O = 0V$		± 0.2	± 1	mV	
		See Typical Curve				
	RTI ^(1, 2)	$V_S = \pm 1.35V$ to $\pm 18V$		± 20 ± 0.3 ± 0.4	± 60	$\mu V/V$ $\mu V/mo$ mV
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Over Temperature	$(V_{IN+}) - (V_{IN-}) = 0V$, $V_O = 0V$ $V_{CM} = 2(V-) to 2(V+) - 2V$, $R_S = 0\Omega$ $V_S = \pm 15V$	2(V-)		2(V+) - 2	V	
		76	86		dB	
		70	80		dB	
INPUT BIAS CURRENT⁽²⁾ Bias Current Offset Current	$V_{CM} = V_S/2$		± 50		nA	
			± 5		nA	
INPUT IMPEDANCE Differential (non-inverting input) Differential (inverting input) Common-Mode			80		k Ω	
			27		k Ω	
			40		k Ω	
NOISE Voltage Noise, $f = 0.1Hz$ to $10Hz$ Voltage Noise Density, $f = 1kHz$	RTI ^(1, 3)		2		$\mu Vp-p$	
			90		nV/\sqrt{Hz}	
GAIN Gain Equation Initial ⁽¹⁾ Gain Error vs Temperature vs Temperature Nonlinearity	$R_L = 100k\Omega$, $V_O = (V-)+0.15$ to $(V+)-1$, $G = 1$ $R_L = 100k\Omega$, $V_O = (V-)+0.25$ to $(V+)-1$, $G = 1$ $R_L = 10k\Omega$, $V_O = (V-)+0.3$ to $(V+)-1.25$, $G = 1$ $R_L = 10k\Omega$, $V_O = (V-)+0.5$ to $(V+)-1.25$, $G = 1$ $R_L = 10k\Omega$, $V_O = (V-)+0.3$ to $(V+)-1.25$, $G = 1$		$G = 1$ to 1000 $G = 1 + R_{G2}/R_{G1}$			V/V V/V
			1			%
			± 0.01	± 0.1		ppm/ $^\circ C$
			± 2	± 10		%
			± 0.01	± 0.1		ppm/ $^\circ C$
	± 2	± 10		% of FS		
		± 0.0002		± 0.005		
FREQUENCY RESPONSE Small Signal Bandwidth Slew Rate Settling Time, 0.1% 0.01% Overload Recovery	$G = 1$ $G = 10$ $G = 1$, 10V Step $G = 1$, 10V Step 50% Input Overload		500		kHz	
			50		kHz	
			0.45		V/ μs	
			40		μs	
			90		μs	
			40		μs	
OUTPUT, V_O Voltage Output Over Temperature Over Temperature Short-Circuit Current Capacitive Load	$R_L = 100k\Omega$, $G = 1$ $R_L = 100k\Omega$, $G = 1$ $R_L = 10k\Omega$, $G = 1$ $R_L = 10k\Omega$, $G = 1$ Continuous to Common Stable Operation	(V-) + 0.15		(V+) - 1	V	
		(V-) + 0.25		(V+) - 1	V	
		(V-) + 0.3		(V+) - 1.25	V	
		(V-) + 0.5		(V+) - 1.25	V	
			± 15			mA
	1000			pF		
POWER SUPPLY Specified Voltage Range, Dual Supplies Operating Voltage Range Quiescent Current Over Temperature	$V_{IN} = 0$, $I_O = 0$	± 2.25		± 18	V	
		± 1.35		± 18	V	
			± 570	± 700	μA	
				± 800	μA	
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance	θ_{JA}	-40		+85	$^\circ C$	
		-55		+125	$^\circ C$	
		-55		+125	$^\circ C$	
			150		$^\circ C/W$	

NOTES: (1) Referred to input pins (V_{IN+} and V_{IN-}), Gain = 1V/V. Specified with 10k Ω in feedback of A2. (2) Input offset voltage specification includes effects of amplifier's input bias and offset currents. (3) Includes effects of input bias current noise and thermal noise contribution of resistor network.

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SPECIFICATIONS: $V_S = +5V$ Single Supply

Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

At $T_A = +25^\circ\text{C}$, $G = 1$, $R_L = 10\text{k}\Omega$ connected to ground and ref pin connected to 2.5V unless otherwise noted.

PARAMETER	CONDITION	INA145UA			UNITS	
		MIN	TYP	MAX		
OFFSET VOLTAGE, V_O Input Offset Voltage V_{OS} vs Temperature $\Delta V_{OS}/\Delta T$ vs Power Supply Rejection Ratio PSRR vs Time Offset Voltage, V_{O1}	RTI ^(1, 2) $V_{CM} = V_O = 2.5V$		± 0.35	± 1	mV	
	$V_S = \pm 1.35V$ to $\pm 18V$		See Typical Curve			
			± 20	± 60	$\mu\text{V}/^\circ\text{C}$	
		RTI ^(1, 2)		± 0.3		$\mu\text{V}/\text{mo}$
			± 0.55		mV	
INPUT VOLTAGE RANGE Common-Mode Voltage Range ⁽³⁾ V_{CM} Common-Mode Rejection Ratio CMRR Over Temperature	$V_{IN+} - V_{IN-} = 0V$, $V_O = 2.5V$ $V_{CM} = -2.5V$ to $+5.5V$, $R_S = 0\Omega$	-2.5		5.5	V	
		76	86 80		dB dB	
INPUT BIAS CURRENT⁽²⁾ Bias Current I_B Offset Current I_{OS}			± 50		nA	
			± 5		nA	
INPUT IMPEDANCE Differential (non-inverting input) Differential (inverting input) Common-Mode			80		k Ω	
			27		k Ω	
			40		k Ω	
NOISE Voltage Noise, $f = 0.1\text{Hz}$ to 10Hz Voltage Noise Density, $f = 1\text{kHz}$ e_n	RTI ^(1, 4)		2		$\mu\text{Vp-p}$	
			90		$\text{nV}/\sqrt{\text{Hz}}$	
GAIN Gain Equation Initial ⁽¹⁾ Gain Error vs Temperature vs Temperature Nonlinearity	$R_L = 100\text{k}\Omega$, $V_O = 0.15V$ to $4V$, $G = 1$ $R_L = 100\text{k}\Omega$, $V_O = 0.25V$ to $4V$, $G = 1$ $R_L = 10\text{k}\Omega$, $V_O = 0.3V$ to $3.75V$, $G = 1$ $R_L = 10\text{k}\Omega$, $V_O = 0.5V$ to $3.75V$, $G = 1$ $R_L = 10\text{k}\Omega$, $V_O = +0.3$ to $+3.75$, $G = 1$		$G = 1$ to 1000 $G = 1 + R_{G2}/R_{G1}$		V/V	
			1		V/V	
			± 0.01	± 0.1	%	
			± 2	± 10	ppm/ $^\circ\text{C}$	
			± 0.01	± 0.1	%	
			± 2	± 10	ppm/ $^\circ\text{C}$	
		± 0.001	± 0.005	% of FS		
FREQUENCY RESPONSE Small Signal Bandwidth Slew Rate Settling Time, 0.1% 0.01% Overload Recovery	$G = 0.1$		500		kHz	
	$G = 1$		50		kHz	
	$G = 1$, 10V Step		0.45		V/ μs	
	$G = 1$, 10V Step		40		μs	
	50% Input Overload			90		μs
				40		μs
OUTPUT, V_O Voltage Output Over Temperature Over Temperature Short-Circuit Current Capacitive Load	$R_L = 100\text{k}\Omega$, $G = 1$ $R_L = 100\text{k}\Omega$, $G = 1$ $R_L = 10\text{k}\Omega$, $G = 1$ $R_L = 10\text{k}\Omega$, $G = 1$ Continuous to Common Stable Operation	0.15		4	V	
		0.25		4	V	
		0.3		3.75	V	
		0.5		3.75	V	
				± 15		mA
				1000		pF
POWER SUPPLY Specified Voltage Range, Single Supply Operating Voltage Range Quiescent Current Over Temperature	$V_{IN} = 0$, $I_O = 0$	+4.5		+36	V	
		+2.7		+36	V	
			550	700	μA	
				800	μA	
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance θ_{JA}		-40		+85	$^\circ\text{C}$	
		-55		+125	$^\circ\text{C}$	
		-55		+125	$^\circ\text{C}$	
			150		$^\circ\text{C}/W$	

NOTES: (1) Referred to input pins (V_{IN+} and V_{IN-}), Gain = 1/V. Specified with 10k Ω in feedback of A2. (2) Input offset voltage specification includes effects of amplifier's input bias and offset currents. (3) Common-mode voltage range with single supply is $2(V+) - 2V - V_{REF}$ to $-V_{REF}$. (4) Includes effects of input current noise and thermal noise contribution of resistor network.

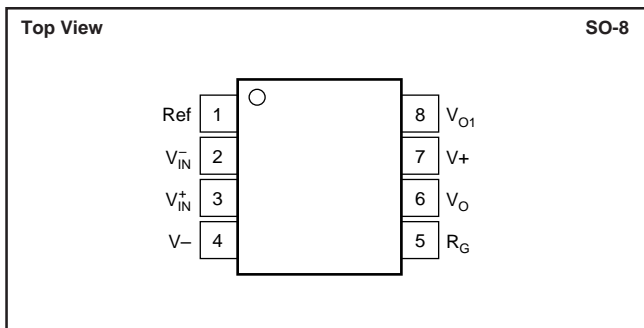
AMPLIFIER A1, A2 PERFORMANCE

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

At $T_A = +25^{\circ}\text{C}$, $G = 1$, $R_L = 10\text{k}\Omega$ connected to ground and ref pin connected to ground unless otherwise noted.

PARAMETER	CONDITION	INA145UA			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE, V_O Input Offset Voltage vs Temperature	$RTI^{(1,2)}$ $V_S = \pm 15\text{V}$, $V_{CM} = V_O = 0\text{V}$		± 0.5 ± 1		mV $\mu\text{V}/^{\circ}\text{C}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio	$V_{IN+} - V_{IN-} = 0\text{V}$, $V_O = 0\text{V}$ $V_{CM} = (V-) \text{ to } (V+) - 1$		$(V-) \text{ to } (V+) - 1$ 90		V dB
OPEN-LOOP GAIN Open Loop Gain			110		dB
INPUT BIAS CURRENT⁽²⁾ Bias Current Offset Current			± 50 ± 5		nA nA
RESISTOR AT A1 OUTPUT, V_{O1} Initial Error Temperature Drift Coefficient			10 ± 0.2 ± 50		k Ω % ppm/ $^{\circ}\text{C}$

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, $V+$ to $V-$	36V
Signal Input Terminals, Voltage	$\pm 80\text{V}$
Current	$\pm 1\text{mA}$
Output Short Circuit (to ground)	Continuous
Operating Temperature	-55°C to $+125^{\circ}\text{C}$
Storage Temperature	-55°C to $+150^{\circ}\text{C}$
Junction Temperature	$+150^{\circ}\text{C}$
Lead Temperature (soldering, 10s)	$+240^{\circ}\text{C}$

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

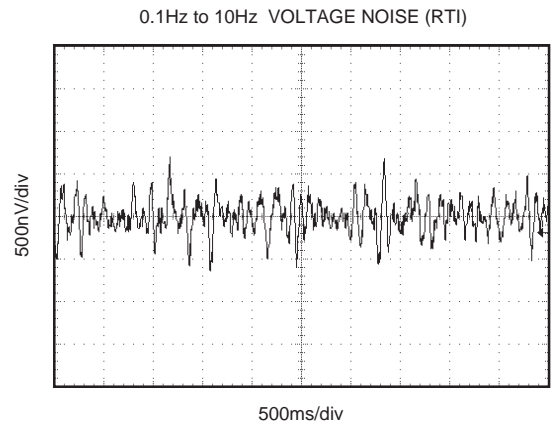
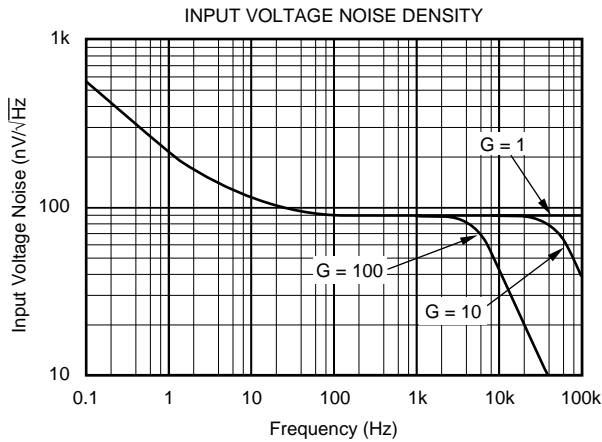
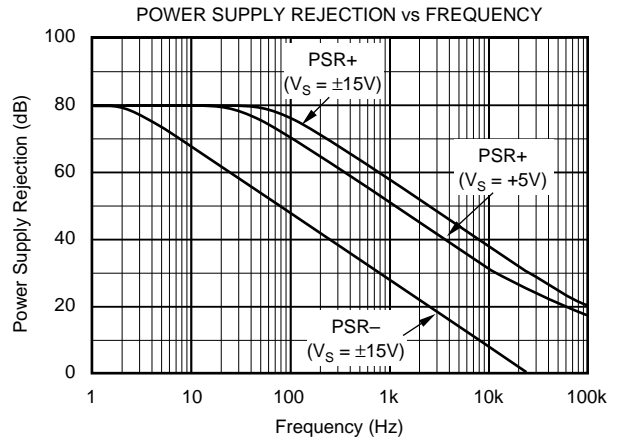
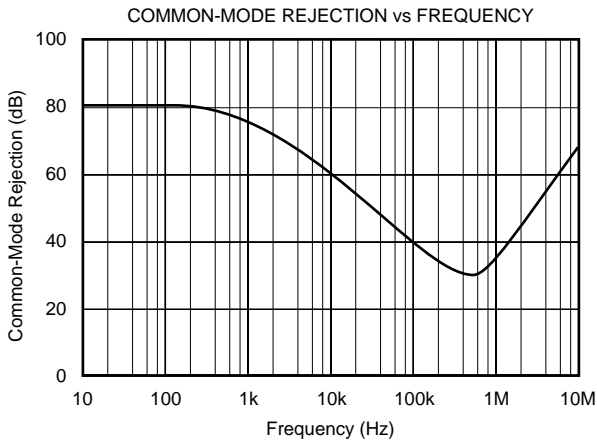
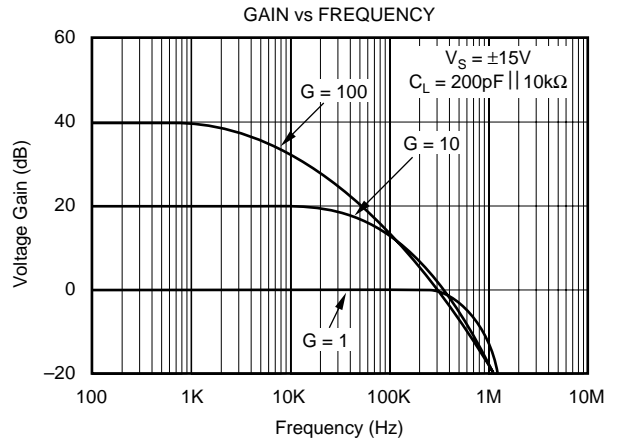
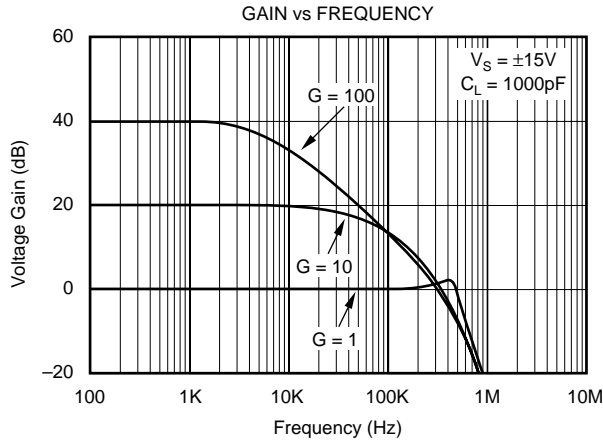
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
INA145UA	SO-8	182	-40°C to $+85^{\circ}\text{C}$	INA145UA	INA145UA	Rails
"	"	"	"	"	INA145UA/2K5	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA145UA/2K5" will get a single 2500-piece Tape and Reel.

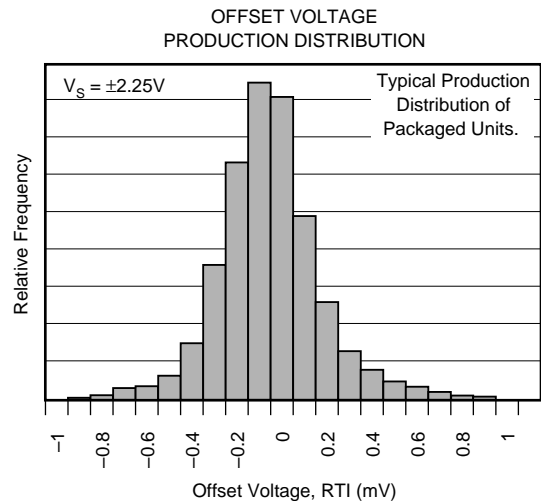
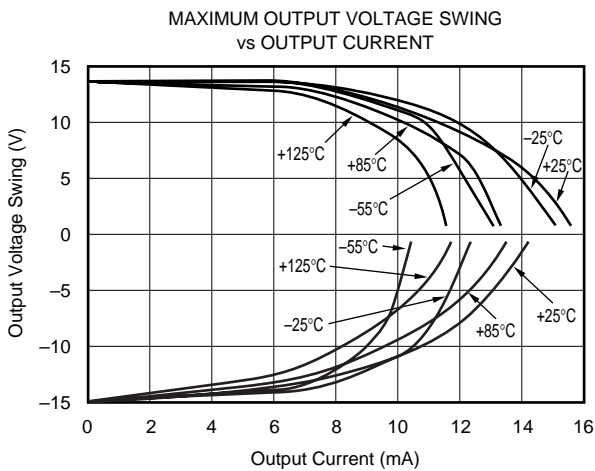
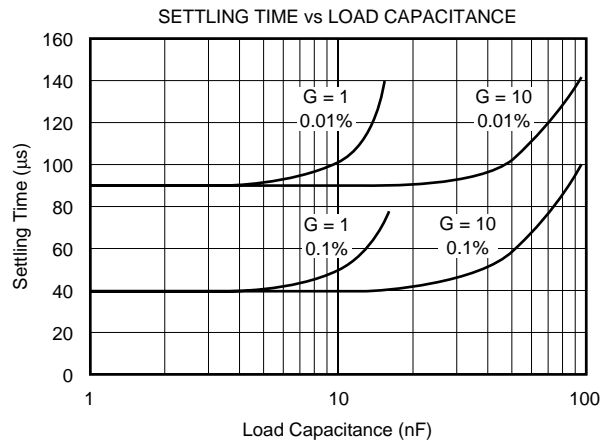
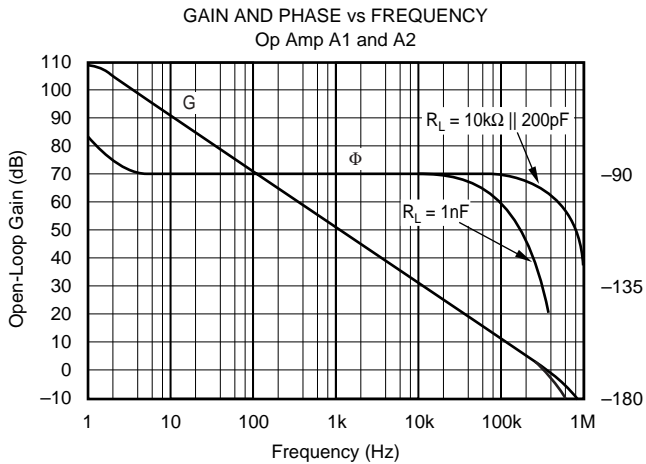
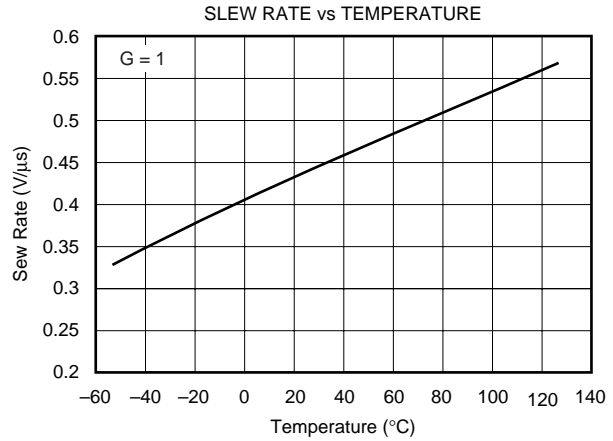
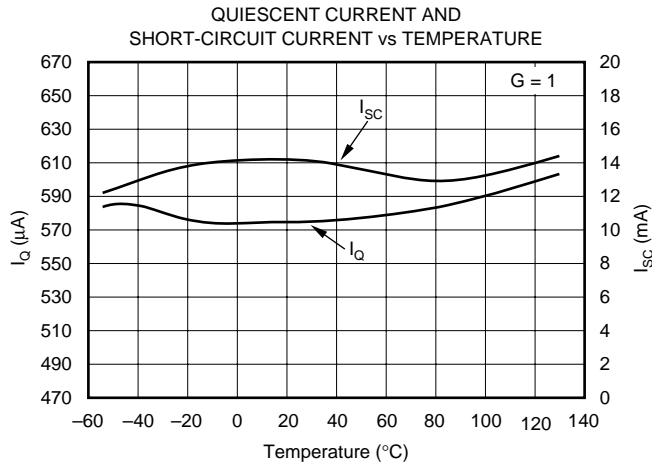
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 1$, $R_L = 10\text{k}\Omega$ connected to ground and Ref pin connected to ground, unless otherwise noted.



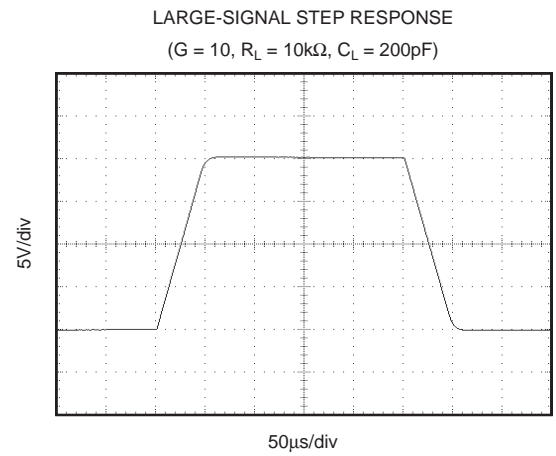
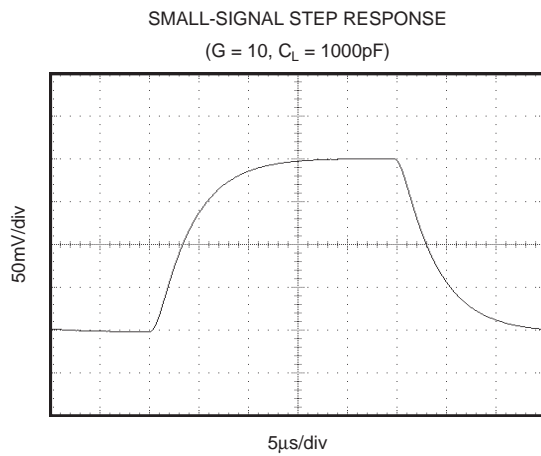
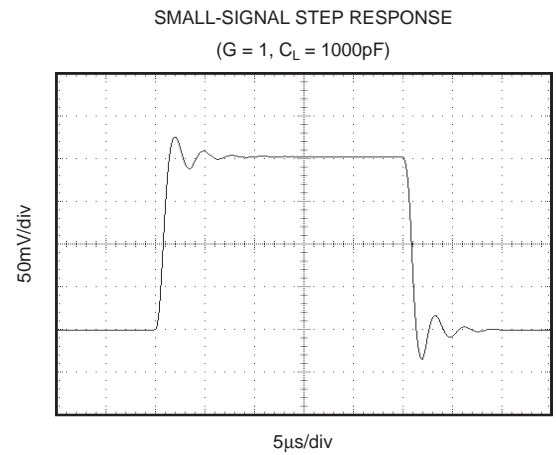
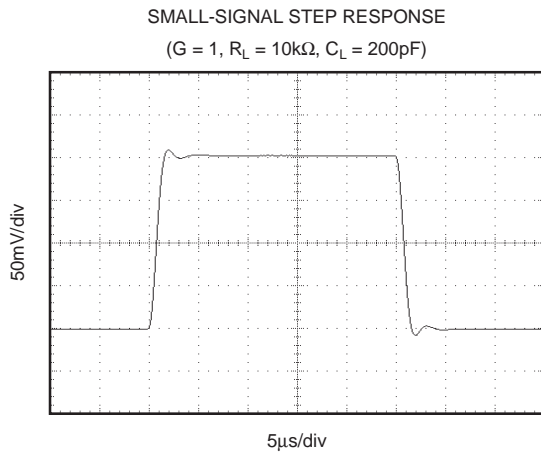
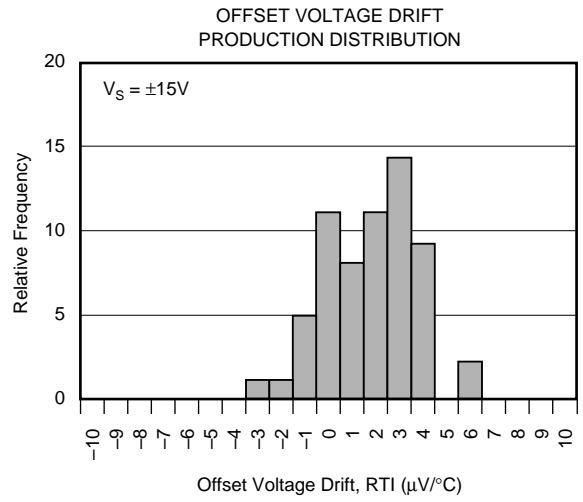
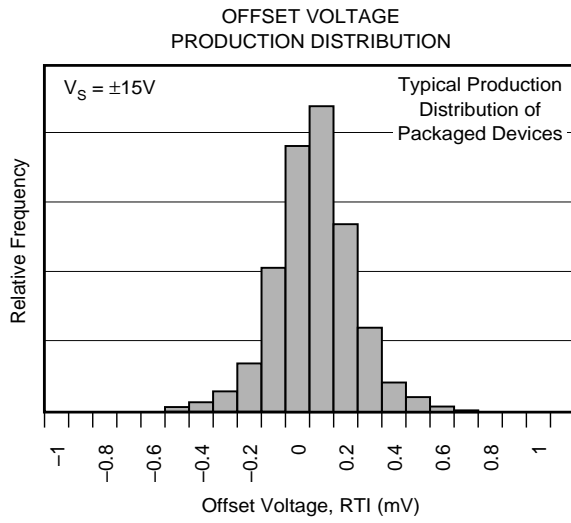
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 1$, $R_L = 10\text{k}\Omega$ connected to ground and Ref pin connected to ground, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $G = 1$, $R_L = 10\text{k}\Omega$ connected to ground and Ref pin connected to ground, unless otherwise noted.



APPLICATION INFORMATION

The INA145 is a programmable gain difference amplifier consisting of a gain of 1 difference amplifier and a programmable-gain output buffer stage. Basic circuit connections are shown in Figure 1. Power supply bypass capacitors should be connected close to pins 4 and 7, as shown. The amplifier is programmable in the range of $G = 1$ to $G = 1000$ with two external resistors.

The output of A1 is connected to the noninverting input of A2 through a $10\text{k}\Omega$ resistor which is trimmed to $\pm 1\%$ absolute accuracy. The A2 input is available for applications such as a filter or a precision current source. See application figures for examples.

OPERATING VOLTAGE

The INA145 is fully specified for supply voltages from $\pm 2.25\text{V}$ to $\pm 18\text{V}$, with key parameters guaranteed over the temperature range -40°C to $+85^\circ\text{C}$. The INA145 can be operated with single or dual supplies, with excellent performance. Parameters that vary significantly with operating voltage, load conditions, or temperature are shown in the typical performance curves.

SETTING THE GAIN

The gain of the INA145 is set by using two external resistors, R_{G1} and R_{G2} , according to the equation:

$$G = 1 + R_{G2}/R_{G1}$$

For a total gain of 1, A2 is connected as a buffer amplifier with no R_{G1} . A feedback resistor, $R_{G2} = 10\text{k}\Omega$, should be used in the buffer connection. This provides bias current cancellation (in combination with internal R_5) to assure specified offset voltage performance. Commonly used values are shown in the table of Figure 1. Resistor values for other gains should be chosen to provide a $10\text{k}\Omega$ parallel resistance.

COMMON-MODE RANGE

The input resistors of the INA145 provides an input common-mode range that extends well beyond the power supply rails. Exact range depends on the power supply voltage and the voltage applied to the Ref terminal (pin 1). To assure proper operation, the voltage at the non-inverting input of A1 (an internal node) must be within its linear operating range. Its voltage is determined by the simple 1:1 voltage divider between pin 3 and pin 1. This voltage must be between V_- and $(V_+) - 1\text{V}$.

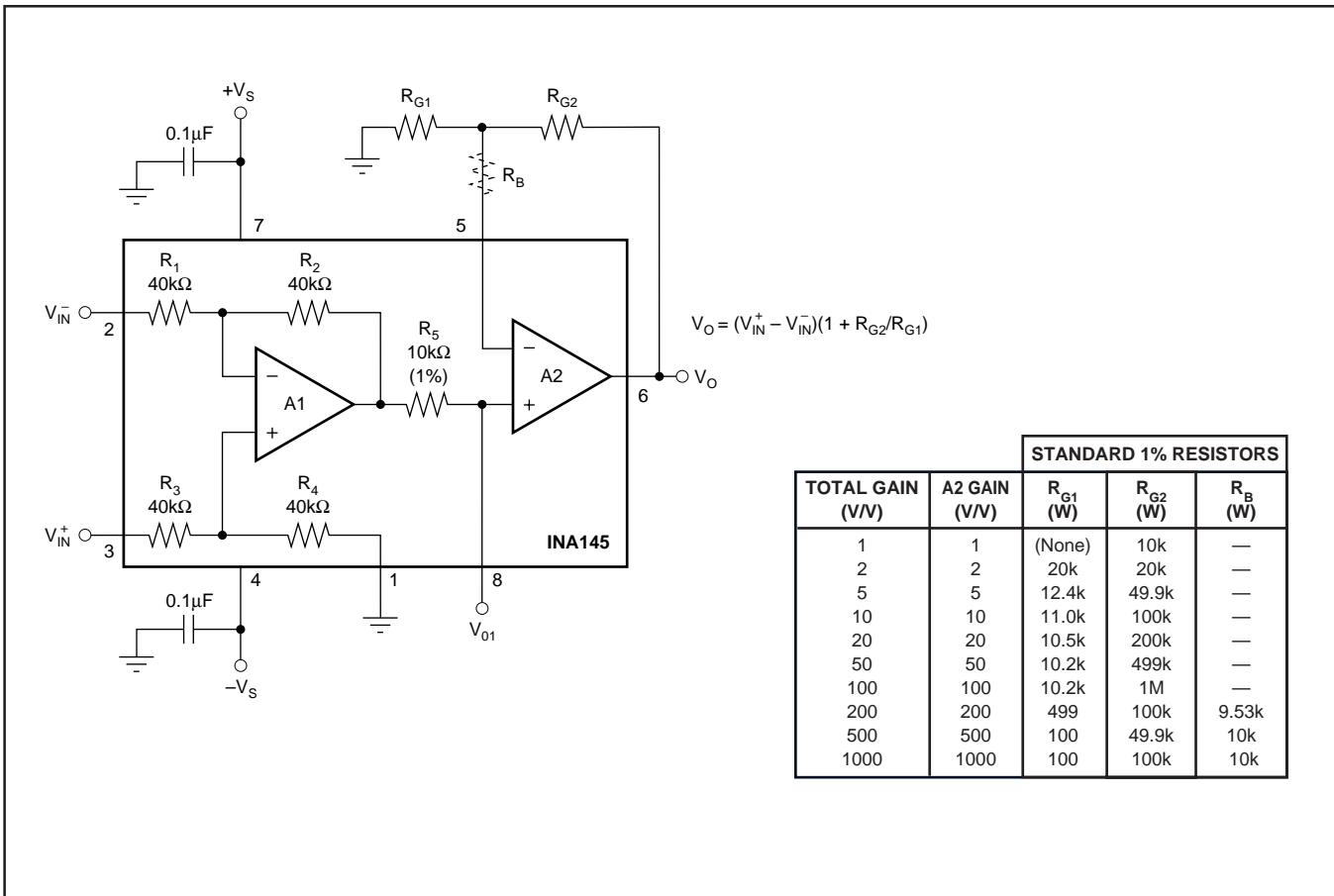


FIGURE 1. Basic Circuit Connections.

OFFSET TRIM

The INA145 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the offset voltage. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage. To maintain good common-mode rejection, the source impedance of a signal applied to the Ref terminal should be less than 10Ω and a resistor added to the positive input terminal should be 10 times that, or 100Ω . Alternatively, the trim voltage can be buffered with an op amp such as the OPA277.

INPUT IMPEDANCE

The input impedance of the INA145 is determined by the input resistor network and is approximately $40k\Omega$. The source impedance at the two input terminals must be nearly equal to maintain good common-mode rejection. A 5Ω mismatch in impedance between the two inputs will cause the typical common-mode rejection to be degraded to approximately 72dB . Figure 7 shows a common application measuring power supply current through a shunt resistor. The source impedance of the shunt resistor, R_S , is balanced by an equal compensation resistor, R_C .

Source impedances greater than 300Ω are not recommended, even if they are perfectly matched. Internal resistors are laser trimmed for accurate ratios, not to absolute values. Adding equal resistors greater than 300Ω can cause a mismatch in the total resistor ratios, degrading CMR.

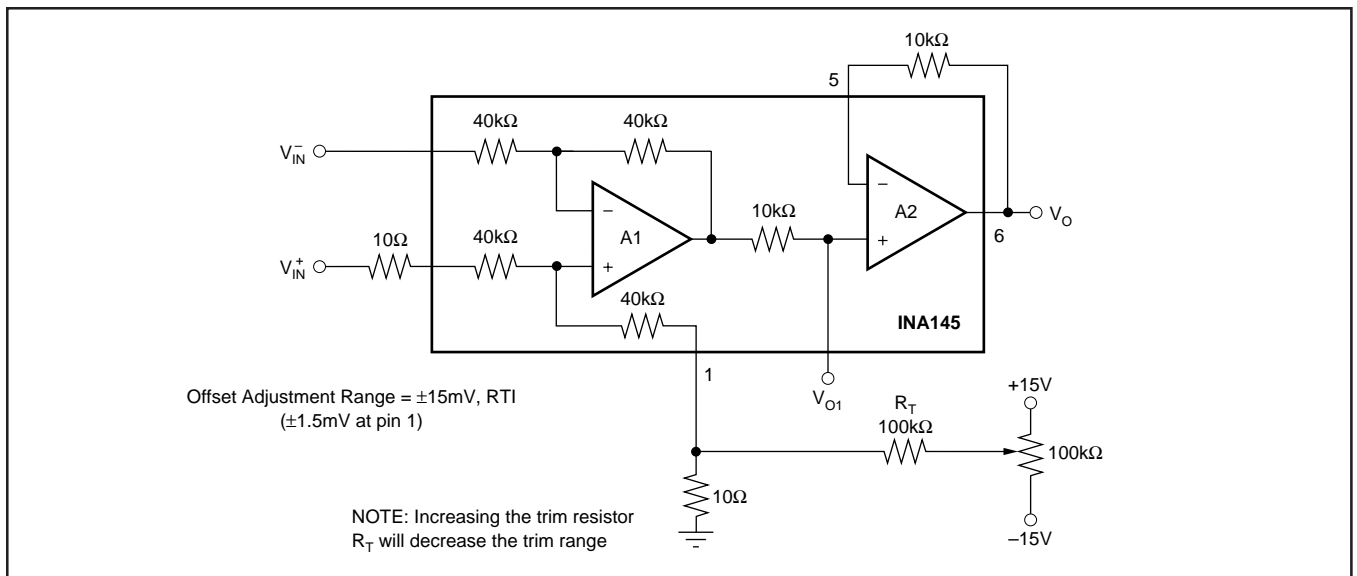


FIGURE 2. Optional Offset Trim Circuit.

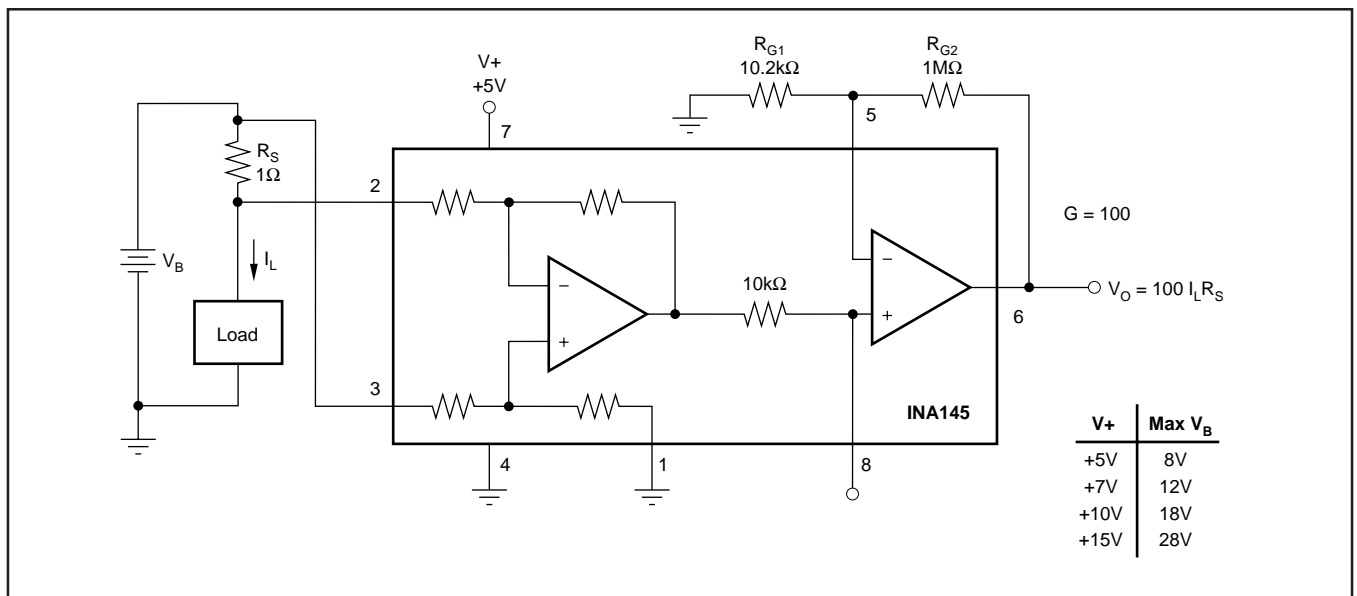


FIGURE 3. Measuring Current with Shunt Resistor.

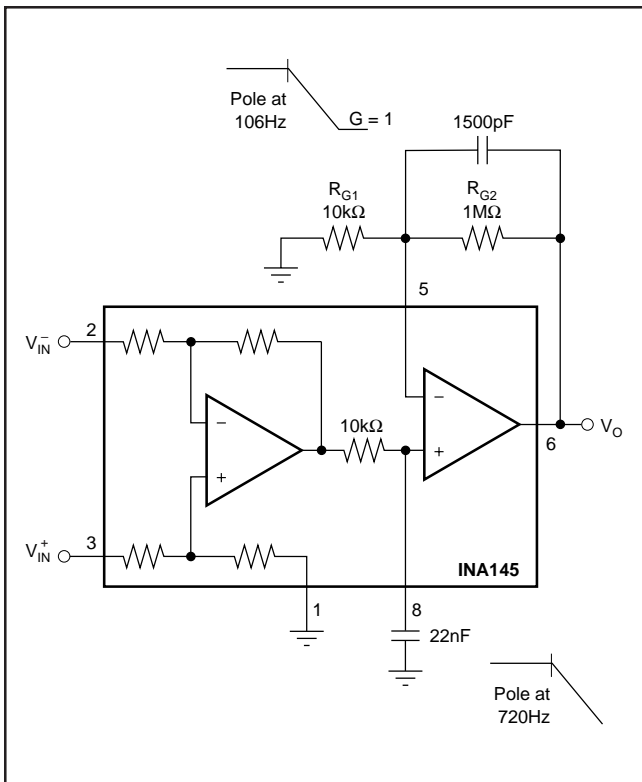


FIGURE 4. Noise Filtering.

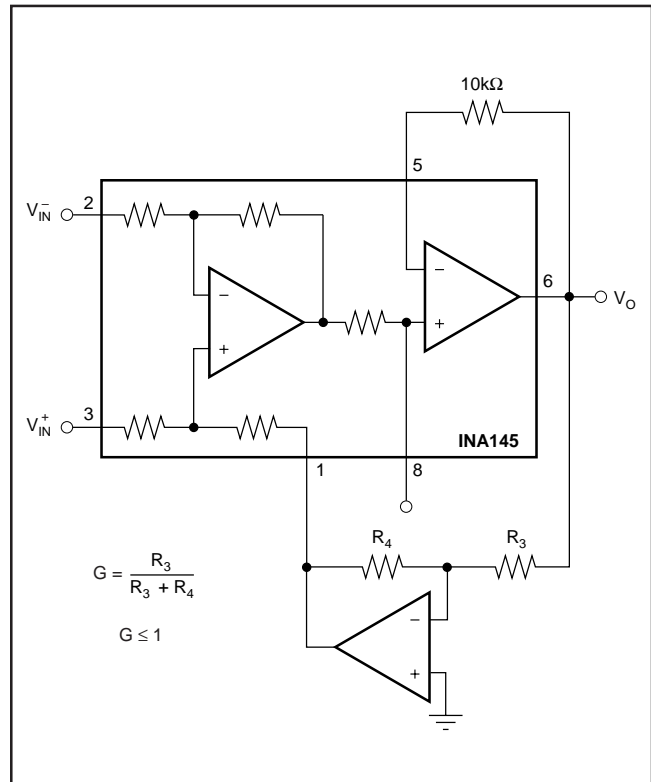


FIGURE 5. Creating Gains Less Than Unity.

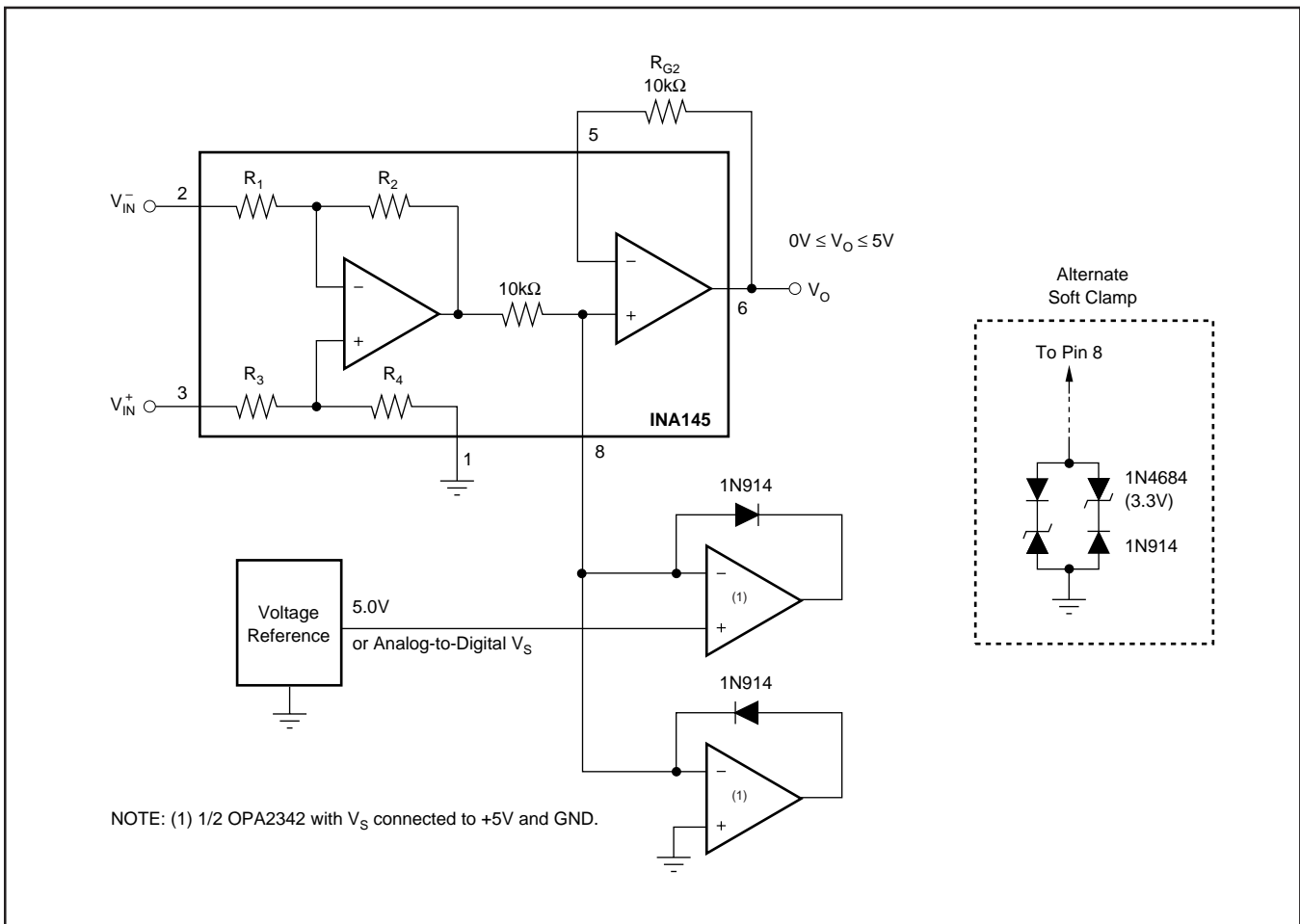


FIGURE 6. Clamp Circuits.

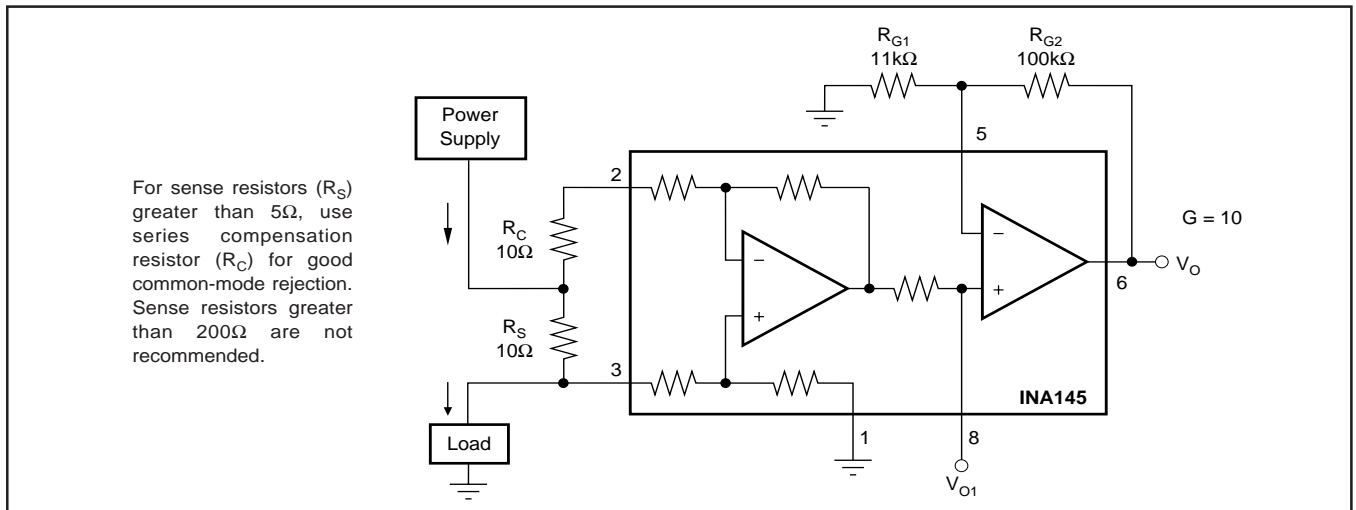


FIGURE 7. Current Monitor, $G = 1$.

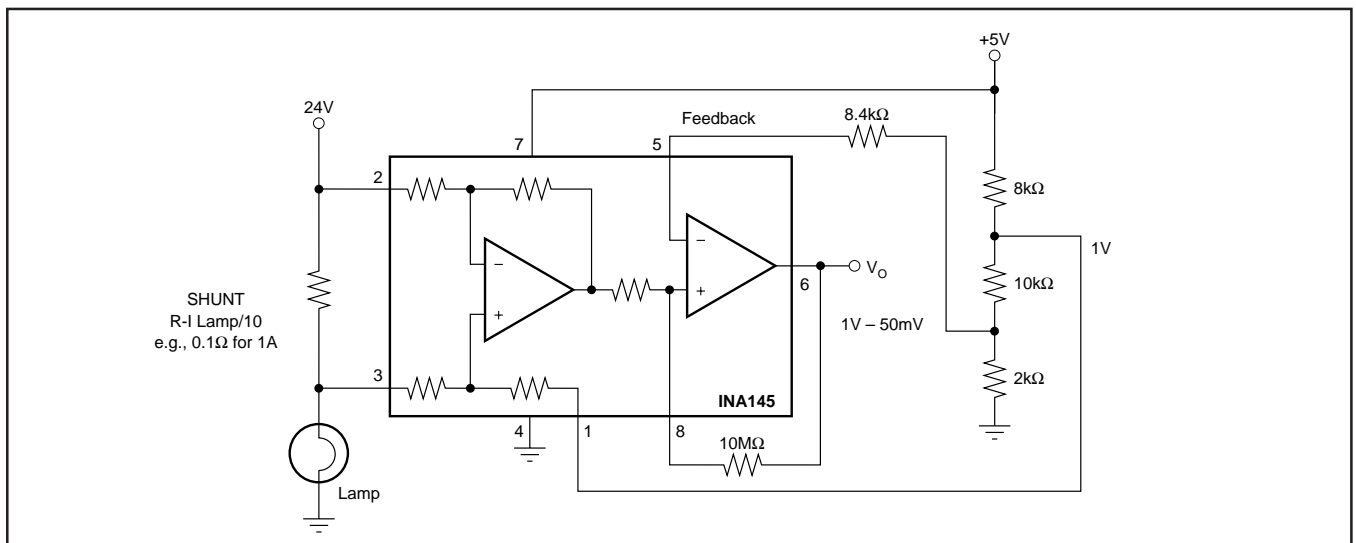


FIGURE 8. Comparator Output with Optional Hysteresis Application to Sense Lamp Burn-Out.

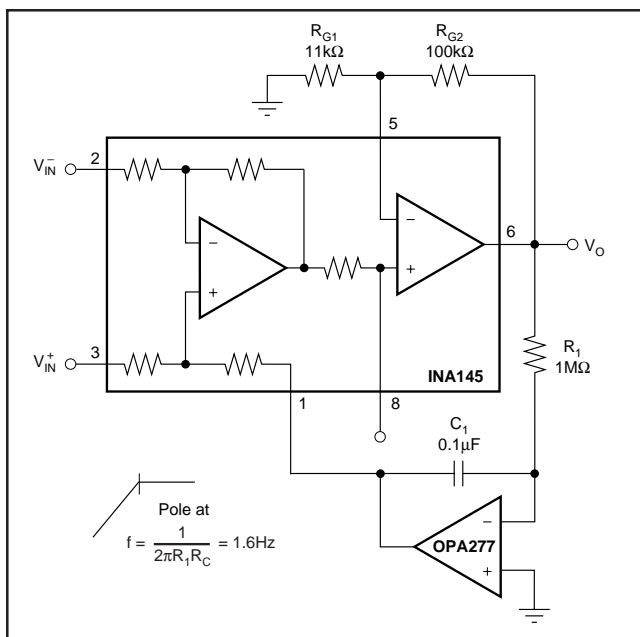


FIGURE 9. AC Coupling (DC Restoration).

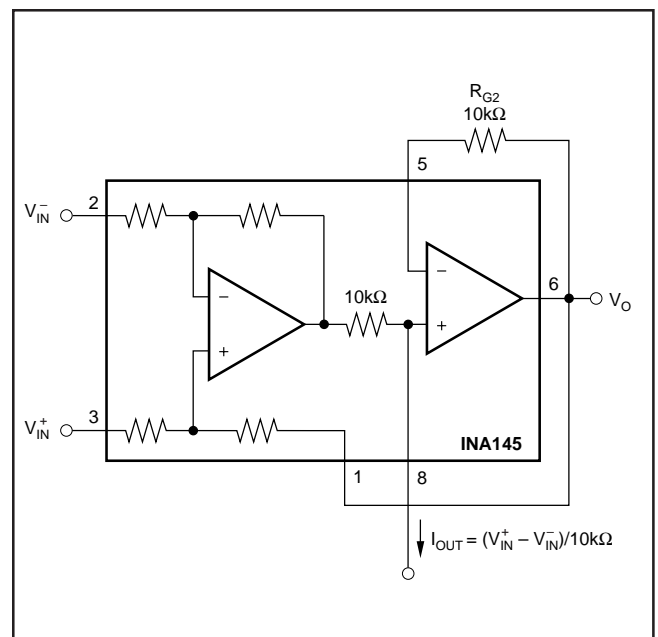




FIGURE 10. Precision Current Source.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA145UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 145UA	
INA145UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		INA 145UA	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA145UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA145UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA145UA	D	SOIC	8	75	506.6	8	3940	4.32

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