TPS9260x-Q1 单/双通道汽车前灯 LED 驱动器

1 特性

- 符合汽车类应用的 要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：环境工作温度范围为 –40°C 至 125°C
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 输入电压：4V - 40V（绝对最大值 45V）
- 输出电压：4V - 75V（绝对最大值 80V）
- 具有集成斜坡补偿的固定频率电流模式控制器
- 两个稳压环路、恒定电流输出和恒定电压输出（每个通道）
- 高侧电流感测：
  - 150mV 或 300mV 感测电压（EEPROM 选项）
  - ±6mV 偏移（实现大约4% 或 2% LED 电流精度）
- 输出电压感应、内部电压基准：2.2V ±5%
- 集成低侧 NMOS-FET 驱动器：峰值栅极驱动电流典型值0.7A
- 频率同步
- 支持脉宽调制 (PWM) 调光和模拟调光
- 诊断：
  - 可作为模拟输出的高侧电流（LED 电流）
  - 开路 LED 和对地短路检测
  - 短路输出保护
- 内部欠压和过压闭锁

2 应用范围

- 汽车用前灯 LED 驱动器
- 高亮 LED 设计

3 说明

TPS9260x-Q1 系列器件是一款单通道和双通道高侧电流 LED 驱动器。借助于完全保护和诊断功能，这一系列器件专门针对并且非常适合于汽车前照灯。每个独立驱动器的底部是峰值电流模式升压控制器。每个控制器由两个独立的反馈环路，一个带有高侧电流感测分路的电流反馈环路，以及一个带有外部电阻分压器网络的电压反馈环路。此控制器传送一个恒定输出电压或一个恒定输出电流。已连接的负载决定此器件是对恒定输出电流（如果此电路在电压设定点前达到电流设定点）还是对恒定输出电压（如果此电路首先达到电压设定点 (if the circuit reaches the voltage set-point is reached first)，例如，在开路负载条件下）进行调节。

每个控制器支持诸如升压、升压至电池电压、SEPIC 或反激式等所有典型拓扑结构。

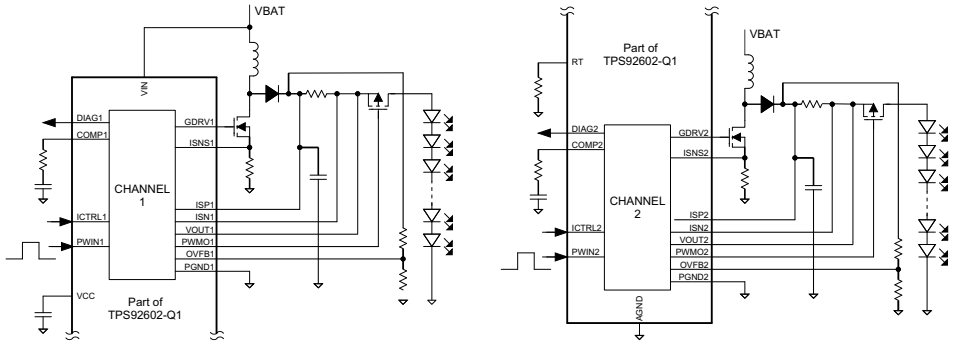
为了保护此电路，高侧 PMOS FET 驱动器用于 LED 灯串的 PWM 调光，并且在外部对地短路时切断电源。

器件信息(1)

器件型号	感测电压范围	通道
TPS92601-Q1、TPS92601B-Q1	15mV–150mV	1
TPS92601A-Q1(2)	30mV–300mV	1
TPS92602-Q1、TPS92602B-Q1	15mV–150mV	2
TPS92602A-Q1(2)	30mV–300mV	2

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。
(2) 器件目前仅提供预览。

图 1. 典型电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (January 2015) to Revision E — **Page**

- 更改了器件信息表 ... 1
- Changed the pinout diagrams ... 3
- Changed VCC to V_{CC} throughout the data sheet. ... 4

Changes from Revision C (September 2014) to Revision D — **Page**

- 已更改 将 TPS92601-Q1 的器件状态从“*产品预览*”更改为“*生产数据*” ... 1
- 已添加 除双通道文本内容以外，还在整个产品说明书中添加了单通道文本内容 ... 1
- Changed the *Handling Ratings* table to *ESD Ratings* and moved the storage temperature to the *Absolute Maximum Ratings* table ... 4
- Updated the units of the Q(GS) equation (Equation 37) ... 24
- Updated the units of the Q(GS) equation (Equation 71) and the resulting values ... 31
- Updated the $r_{DS(on)}$ values as a result of Equation 72 ... 31

Changes from Revision B (August 2014) to Revision C — **Page**

- Changed the package type for the TPS92601-Q1 and TPS92601A-Q1 ... 3

Changes from Revision A (April 2014) to Revision B — **Page**

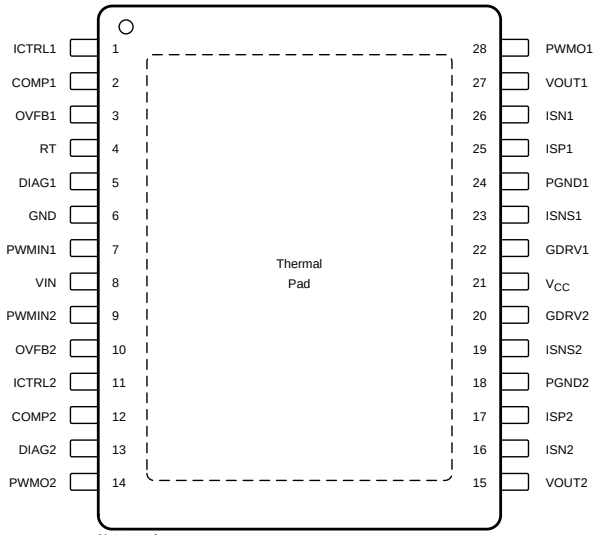
- 在“器件比较表”中添加了一列 ... 1
- 更改了器件信息表 ... 1
- Changed pinout diagram and combined Pin Function tables ... 3

Changes from Original (March 2014) to Revision A — **Page**

- Added all new content following the first page ... 3

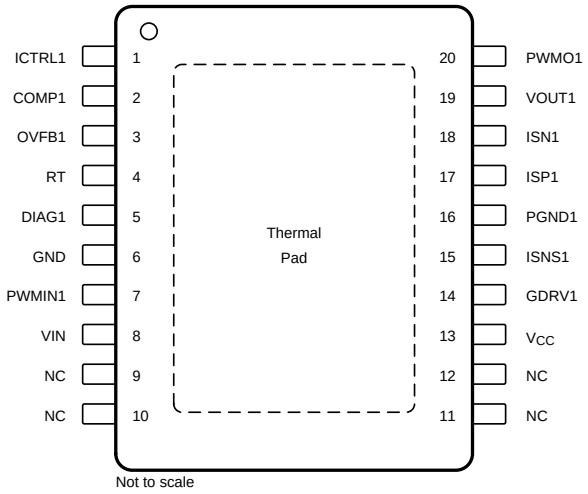
5 Pin Configuration and Functions

TPS92602x-Q1 PWP PowerPAD™ Package
28-Pin HTSSOP With Exposed Thermal Pad
Top View



NC – No internal connection

TPS92601x-Q1 PWP PowerPAD Package
20-Pin HTSSOP Package With Exposed Thermal Pad
Top View



NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS92601-Q1 TPS92601A-Q1 TPS92601B-Q1 20 PINS	TPS92602-Q1 TPS92602A-Q1 TPS92602B-Q1 28 PINS		
COMP1	2	2	O	Compensation network (channel 1)
COMP2	—	12	O	Compensation network (channel 2)
DIAG1	5	5	O	Diagnostic pin (open, short, LED current) (channel 1)
DIAG2	—	13	O	Diagnostic pin (open, short, LED current) (channel 2)
GDRV1	14	22	O	Gate driver NMOS-FET (channel 1)
GDRV2	—	20	O	Gate driver NMOS-FET (channel 2)
GND	6	6	—	Ground
ICTRL1	1	1	I	LED current-control pin, analog dimming (channel 1)
ICTRL2	—	11	I	LED current control pin, analog dimming (channel 2)
ISN1	18	26	I	Current-sense input – negative (channel 1)
ISN2	—	16	I	Current-sense input – negative (channel 2)
ISNS1	15	23	I	Overcurrent sense input (channel 1)
ISNS2	—	19	I	Overcurrent sense input (channel 2)
ISP1	17	25	I	Current-sense input – positive (channel 1)
ISP2	—	17	I	Current-sense input – positive (channel 2)
NC	9	—	—	No internal connection
	10			
	11			
	12			
OVFB1	3	3	I	Voltage-feedback input (channel 1)
OVFB2	—	10	I	Voltage feedback input (channel 2)
PGND1	16	24	—	Power ground (channel 1)

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	TPS92601-Q1 TPS92601A-Q1 TPS92601B-Q1 20 PINS	TPS92602-Q1 TPS92602A-Q1 TPS92602B-Q1 28 PINS		
PGND2	—	18	—	Power ground (channel 2)
PWMIN1	7	7	I	PWM input and channel enable or disable function (channel 1)
PWMIN2	—	9	I	PWM input and channel enable or disable function (channel 2)
PWMO1	20	28	O	PWM PMOS-FET driver output (channel 1)
PWMO2	—	14	O	PWM PMOS-FET driver output (channel 2)
RT	4	4	I	Oscillator pin and pin for external sync. frequency
V_{CC}	13	21	O	Gate-drive supply voltage (external decoupling capacitor)
VIN	8	8	I	Supply voltage
VOUT1	19	27	I	Connect to boost output voltage (channel 1)
VOUT2	—	15	I	Connect to boost output voltage (channel 2)
Thermal pad			—	Solder to achieve appropriate power dissipation. Connect to PGND.

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)(3)

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	VIN, PWMINx(4)	–0.3	40	V
Output voltage	VOUTx, ISPx, ISNx, PWMOx(4)	–0.3	80	V
Differential voltage	(VOUTx – PWMOx)(4)	–0.3	8.8	V
Grounds	PGNDx(4)	–0.3	0.3	V
Other pins	GDRVx, ISNSx(4)	–0.3	8.8	V
	OVFBx(4)	–0.3	80	V
	V_{CC}	–0.3	8.8	V
	ICTRLx, COMPx, RT, DIAGx(4)	–0.3	3.6	V
V_{CC} current	Gate-driver supply		220	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) The algebraic convention, whereby the most-negative value is a minimum and the most-positive value is a maximum.
(3) All voltages are with respect to ground (GND pin), unless otherwise specified.
(4) For the TPS9602-Q1 device, x = 1 or 2. For the TPS9601-Q1 device, x is blank.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Other pins	±500	
			Corner pins (1, 14, 15, 28 for TPS92602x-Q1; 1, 10, 11, 20 for TPS92601x-Q1)	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
	Supply voltage	VIN (first connection to battery, full functionality)	6	26	V
		VIN (battery voltage during cranking profile, full functionality)	4	26	V
		VIN	26	40	V
	Output sense	VOUTx, ISPx, ISNx(1)	4	75	V
	PWMIN	PWMINx: enable and disable functionality(1)	0	40	V
		PWMINx: PWM functionality(1)	0	7	V
	Other pins	ISNSx, OVFBx(1)	0	8	V
		V_{CC}	3	8	V
		ICTRLx, RT(1)	0	3.3	V
	Gate-driver supply current, V_{CC}(2)			100	mA
T_A	Ambient temperature range		–40	125	°C
T_J	Junction temperature range		–40	150	°C

(1) For the TPS9602-Q1 device, x = 1 or 2. For the TPS9601-Q1 device, x is blank.
(2) Note available current for low-side gate drivers to drive the external BOOST FETs

6.4 Thermal Information

THERMAL METRIC(1)		TPS92601-Q1 PWP (HTSSOP) 20 PINS	TPS92602-Q1 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37	37.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.4	19.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.7	16.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.5	16.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	2.6	°C/W

(1) For more information about traditional and new thermal metrics, seeSemiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{VDD} = 12 VDC, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
$V_{(VIN\_norm)}$	Input voltage range	Normal mode after initial start-up, VIN rising	6		40	V
$V_{(VIN\_crank)}$		Normal mode after initial start-up, VIN falling	4		40	
$V_{(UVLO)}$	Undervoltage lockout	PWM1 = PWM2 = High, VIN falling,$f_{(PWMOx)}$ < $V_{(VOUTx)}$ – 2 V		3.72	4	V
$V_{(UVsh)}$	Undervoltage shutdown	PWM1 = PWM2 = High, VIN falling, quiescent current < 2 µA		2.8	3.5	V
$V_{(OVSH)}$	Overvoltage shutdown	PWM1 = PWM2 = High, VIN falling, $V_{(PWMOx)}$ = $V_{(VOUTx)}$, $V_{(GRDVx)}$ = 0	40	40.7		V
SUPPLY CURRENT						
$I_{(stby)}$	Shutdown current	VIN = 12 V, PWMIN1 and PWMIN2 = low for > $t_{(CH\_OFF)}$, T_A = 25°C			2	µA
		VIN = 12 V, PWMIN1 and PWMIN2 = low for > $t_{(CH\_OFF)}$, T_A = 125°C			3	
$t_{(CH\_OFF)}$	Channel OFF timer	PWMINx = low	9.5	14	18	ms
$t_{(CH\_ON)}$	Channel ON timer	PWMINx = high, V_{CC} = 5.5 V			1	ms
I_{nom}	Normal-mode current in OVP loop	VIN = 12 V, PWMINx = high		8	12	mA

Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{VDD} = 12 VDC, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVER SUPPLY V_{CC}						
$V_{(VCC)}$	Output voltage	VIN > 6 V	5.5	6.6	7.4	V
$V_{(VCC\_dr)}$	Drop-out voltage	4 V < VIN < 8 V, $I_{(VCC)}$ < 50 mA			400	mV
$C_{(VCC)}$	V_{CC} buffer capacitance		2.2	10	20	µF
$I_{(VCC)}$	Output current (only for internal usage)				80	mA
$I_{(VCC\_LIM)}$	Current limit	V_{CC} shorted to ground	150		220	mA
GATE DRIVER – LOW-SIDE BOOST NMOS-FET						
$V_{GS(NMOS)}$	NMOS gate-source voltage	Gate-source voltage to switch on boost NMOS FET. Depends on V_{CC}	5.5	6.6	7.4	V
$D_{(MAX)}$	Maximum duty cycle			93.8%		
$t_{r(NMOS)}$	Gate driver rising	V_{CC} = 6.6 V, no load		22		ns
$t_{f(NMOS)}$	Gate driver falling	V_{CC} = 6 V, no load		8.5		ns
$r_{DS(on)(Source,Nmos)}$	Gate driver resistance, sourcing	V_{CC} = 6.6 V, 100-mA load		2.5	4	Ω
$r_{DS(on)(Sink,Nmos)}$	Gate driver resistance, sinking	V_{CC} = 6.6 V, 100-mA load		2.5	4	Ω
CURRENT LIMIT – NMOS FET						
$V_{(ISNSx)}$	Voltage limit threshold across sense-current resistor		83	100	115	mV
$t_{(ISNSx)}$	Leading edge blanking			200		ns
$I_{(ISNSx)}$	Current on ISNSx		40	50	65	µA
$A_{(PS)}$	VC current-mode gain (ΔV_{vc} / ΔV_{sns})			4		V/V
GATE DRIVER – HIGH-SIDE PWM PMOS-FET						
$I_{(PWMOx\_Source)}$	Peak source current	$V_{(OUT)}$ – $V_{(PWMOx)}$ = 6.5 V, $V_{(OUT)}$ = 40 V		150		mA
$I_{(PWMOx\_Sink)}$	Peak sink current	$V_{(OUT)}$ – $V_{(PWMOx)}$ = 0 V, $V_{(OUT)}$ = 40 V		10		mA
$V_{(PWMOx)}$	Output voltage		4		75	V
$V_{GS(PMOS)}$	PMOS gate-source voltage	PWMx = high, $V_{(OUT)}$ = 40 V	6	6.9	8	V
$V_{GS(NMOS)}$	NMOS gate-source voltage	Sufficient gate-source voltage to switch on the NMOS FET; this depends on V_{CC}.	5.5	6.6	7.4	V
$t_{r(PMOS)}$	HS gate driver rising	No load		1		µs
$t_{f(PMOS)}$	HS gate driver falling	No load		3		µs
PWM DIMMING						
$f_{(PWMIN)}$	Dimming frequency	See PWM dimming section	0.2	2		kHz
$V_{(thLOW)}$	Logic low	Switch off PMOS dimming FET (low below)			0.8	V
$V_{(thHIGH)}$	Logic high	Switch on PMOS dimming FET (high above)	2			V
$R_{(PWMIN\_pd)}$	Pulldown resistance at PWMINx pin		90	120	150	kΩ
	PWMIN to LED turnoff time			80		ns
	PWMIN to LED turnon time			60		ns
INTERNAL PLL OSCILLATOR						
$f_{(OSC)}$	Oscillator range		100		600	kHz
$\Delta f_{(OSC)}$	Oscillator accuracy	RT: 20-kΩ resistor. See Equation 2 and Figure 4 for $f_{(OSC)}$ vs RT	–20%		20%	
$f_{(EXT)}$	Ext. synchronization		100		600	kHz
$t_{(CLKpw)}$	Minimum clock input pulse duration				70	ns
$V_{(RTthLO)}$	RT low voltage				0.8	V
$V_{(RTthHI)}$	RT high voltage		2			V
$t_{(RTdelay)}$	RT rising edge to GDRV1 rising edge			35		ns
$t_{(PLLlock)}$	PLL lock-in time			200		µs

Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{VDD} = 12 VDC, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-SIDE CURRENT-SENSE ERROR AMPLIFIER VFBx < 2.1 V						
$V_{(SPSN,Com)}$	Common-mode voltage ISPx, ISNx		4		74	V
$V_{(SPSN\_Diff)}$	Full-scale sense voltage ISPx – ISNx	4 V < $V_{(SPSN\_Com)}$ < 75 V, VFBx < 2.1 V, TPS92601-Q1, TPS92602-Q1,TPS92601B-Q1, TPS92602B-Q1		150		mV
		4 V < $V_{(SPSN\_Com)}$ < 75 V, VFBx < 2.1 V, TPS92601A-Q1, TPS92602A-Q1		300		
$V_{(SPSN\_AC)}$	Sense-voltage accuracy	Common-mode voltage 4 V to 75 V	–6		6	mV
$I_{(BIAS\_SPSN)}$	Input bias current ISPx, ISNx	4 V < $V_{(SPSN\_Com)}$ < 75 V, $V_{(SPSN\_Diff)}$ = 150 mV		40		µA
$I_{(offset\_SPSN)}$	Input offset current ISPx, ISNx	TPS92601-1, TPS92602-Q1, TPS92601B-Q1, TPS92602B-Q1, 4 V < $V_{(SPSN\_Com)}$ < 75 V, $V_{(SPSN\_Diff)}$ = 150 mV		100	135	µA
		TPS92601A-Q1, TPS92602A-Q1, 4 V < $V_{(SPSN\_Com)}$ < 75 V, $V_{(SPSN\_Diff)}$ = 300 mV		175	200	
g_{MC}	Forward transconductance			1		mS
$A_{(HSCS)}$	HS current-sense gain	TPS92601-Q1, TPS92602-Q1, TPS92601B-Q1, TPS92602B-Q1		5		V/V
		TPS92601A-Q1, TPS92602A-Q1		2.5		V/V
CURRENT CONTROL ICTRL – ANALOG DIMMING FOR ALL PARAMETERS: VFBx < 2.1 V						
$I_{(DIM\_LIN)}$	Linear analog dimming range		10%		100%	
$K_{(DIMfactor)}$	Dimming factor, $V_{(ICTRL)}$ / $V_{(SNSPx)}$	TPS92601-Q1, TPS92602-Q1, TPS92601B-Q1, TPS92602B-Q1, T_A = 25ºC(1)	9.7	10	10.3	
		TPS92601-Q1, TPS92602-Q1, TPS92601B-Q1, TPS92602B-Q1, T_A = 125ºC(1)	9.5	10	10.5	
		TPS92601A-Q1, TPS92602A-Q1, T_A = 25ºC(1)	4.85	5	5.15	
		TPS92601A-Q1, TPS92602A-Q1, T_A = 125ºC(1)	4.75	5	5.25	
$V_{(ICTRLx)}$	Adjustable voltage range	See Figure 13	0		1.5	V
$R_{(ICTRLpd)}$	Pulldown resistance at ICTRLx pin		0.75	1	1.2	MΩ
ERROR AMPLIFIER - REFERENCE VOLTAGE						
$V_{(VFB)}$	Voltage feedback			2.2		V
$\Delta V_{(VFB)}$	Voltage FB accuracy		–5%		5%	
$I_{(BIAS)}$	Input bias current	VFB = 2.2 V			500	nA
$g_{(Mv)}$	Forward transconductance			1		mS
INTERNAL SOFT-START						
$t_{(softstart)}$	Soft-start time, internal soft-start	COMP 0 V to 1.5 V		3.5		ms
DIAGNOSIS – DIAGx PIN						
$V_{(OPLED)}$	Open LED failure	TPS92601-Q1, TPS92602-Q1, TPS92601B-Q1, TPS92602B-Q1		10		mV
		TPS92601A-Q1, TPS92602A-Q1		20		
$V_{(DIAG\_OP)}$	Low-level voltage, DIAGx pin	DIAGx pin pulled low, $I_{(DIAGx)}$ = 100 µA			0.15	V
$V_{(SHLED)}$	Shorted LED failure	TPS92601-Q1, TPS92602-Q1, TPS92601B-Q1, TPS92602B-Q1		225		mV
		TPS92601A-Q1, TPS92602A-Q1		450		
$V_{(DIAG\_SH)}$	High-level voltage, DIAGx pin	DIAGx pin pulled high, $I_{(DIAGx)}$ = 100 µA	3		3.47	V
$V_{(ILED1)}$	Range for tracking LED current on DIAGx pin	Voltage range on DIAGx pin (VIN > 6 V)	0.2		2.85	V
$V_{(ILED2)}$			0.2		2.85	
$V_{(DIAG\_AC)}$	Offset of DIAG output buffer	At input of DIAG buffer	–12		12	mV
$K_{(DIAG\_factor)}$	Factor $V_{(DIAG)}$ / $V_{(SPSN)}$	Within linear analog dimming range and DIAG tracking range. Exclusive offset $V_{(DIAG\_AC)}$, TPS92601-Q1, TPS92602-Q1, TPS92601B-Q1, TPS92602B-Q1		12.5		
		Within linear analog dimming range and DIAG tracking range. Exclusive offset $V_{(DIAG\_AC)}$, TPS92601A-Q1, TPS92602A-Q1		6.25		

(1) Within linear analog dimming range (10%–100%). Exclusive offset $V_{(SPSN\_AC)}$ = 6 mV

Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{VDD} = 12 VDC, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMPENSATION NETWORK – COMPx PIN						
$V_{(COMPx)}$	Compensation-network output-pin voltage		0		3.3	V
THERMAL SHUTDOWN						
$T_{(SD)}$	Thermal shutdown			165		°C
$T_{(HYS)}$	Hysteresis			20		°C

6.6 Typical Characteristics

Load is eight LEDs per channel at 500 mA, –40ºC ≤ T_A ≤ 125ºC, –40ºC ≤ T_J ≤ 150ºC, $C_{(COMP)}$ = 0.22 µF, unless otherwise noted.

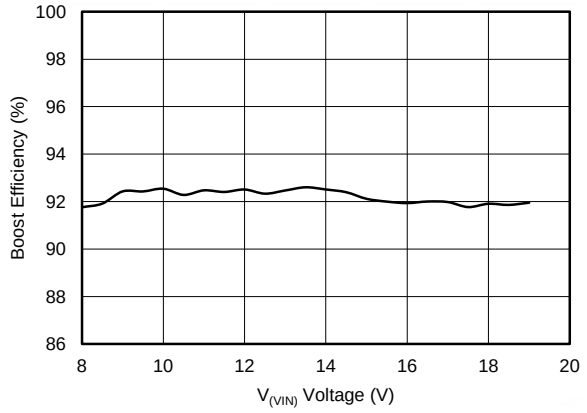


Figure 2. Boost Efficiency vs Input Voltage

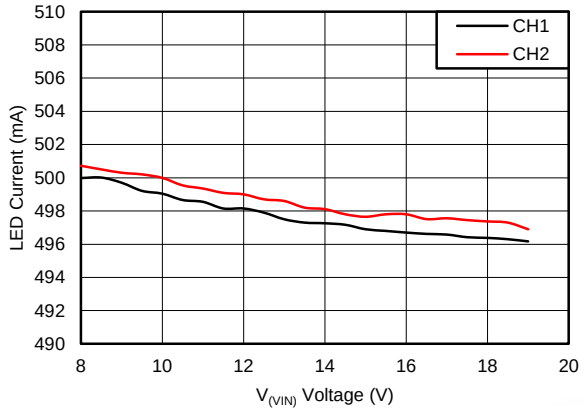


Figure 3. Line Regulation

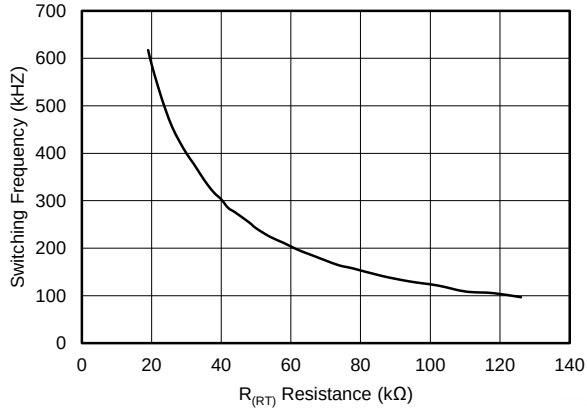
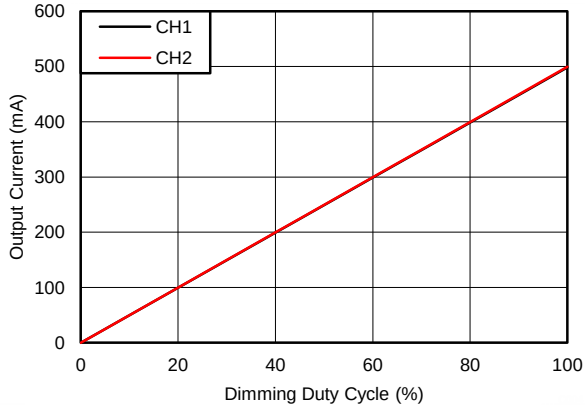


Figure 4. Switching Frequency vs $R_{(RT)}$ Resistance



$f_{(PWM)}$ = 200 Hz

Figure 5. $I_{(OUT)}$ vs PWM Dimming Duty Cycle

Typical Characteristics (continued)

Load is eight LEDs per channel at 500 mA, –40ºC ≤ T_A ≤ 125ºC, –40ºC ≤ T_J ≤ 150ºC, $C_{(COMP)}$ = 0.22 µF, unless otherwise noted.

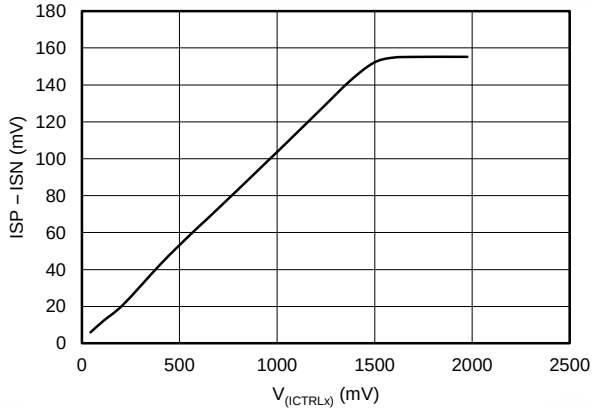


Figure 6. Analog Dimming: Differential Sense Voltage, $V_{(ISPx\ –\ ISNx)}$ vs $V_{(ICTRLx)}$

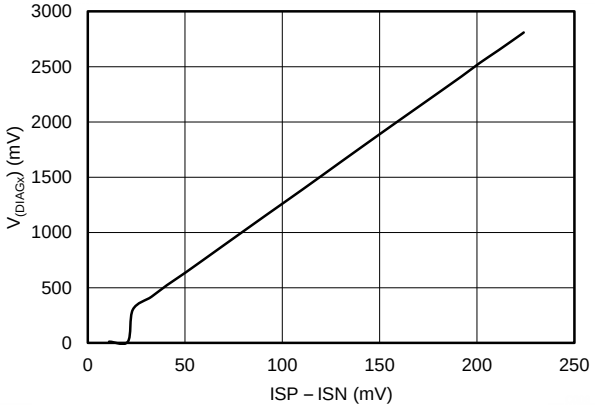
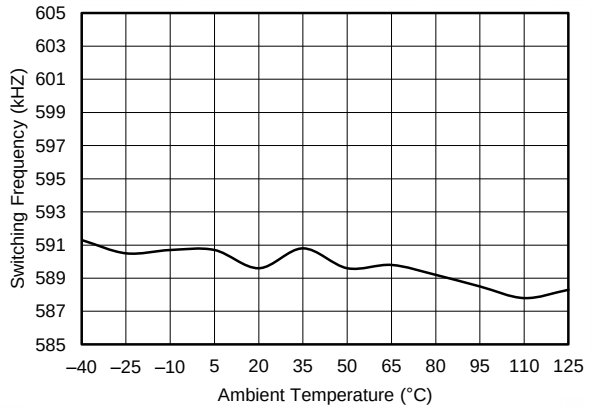


Figure 7. $V_{(DIAGx)}$ vs $V_{(ISPx\ –\ ISNx)}$



$R_{(RT)}$ = 20 kΩ

Figure 8. Switching Frequency vs Ambient Temperature

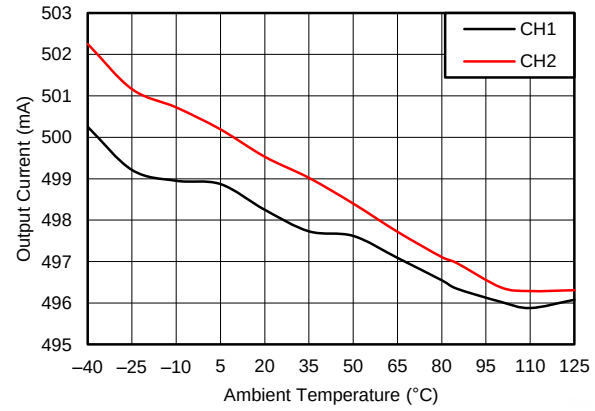


Figure 9. $V_{(ISPx\ –\ ISNx)}$ vs Ambient Temperature

7 Detailed Description

7.1 Overview

The TPS92602y-Q1 device is a dual-channel LED driver. The base of each independent driver is a peak-current-mode boost controller. The two boost controllers operate 180° out-of-phase in order to reduce ripple currents and radiation.

Each controller is independently configurable to regulate the output current (the typical case for driving LEDs) or to regulate the output voltage. Depending on the chosen configuration for each channel, one loop is active while the other loop only acts in case of a failure condition. In a constant-current application, the inactive voltage loop sets the maximum output-voltage limit (and hence becomes active in case of output overvoltage due to an open LED). In constant-voltage applications, the inactive current loop sets the maximum output current limit (and hence becomes active in case of output overcurrent because of an LED short to ground).

The TPS92601y-Q1 device is a single-channel version of the TPS92602y-Q1 device. Both devices have the same functions.

7.2 Functional Block Diagram

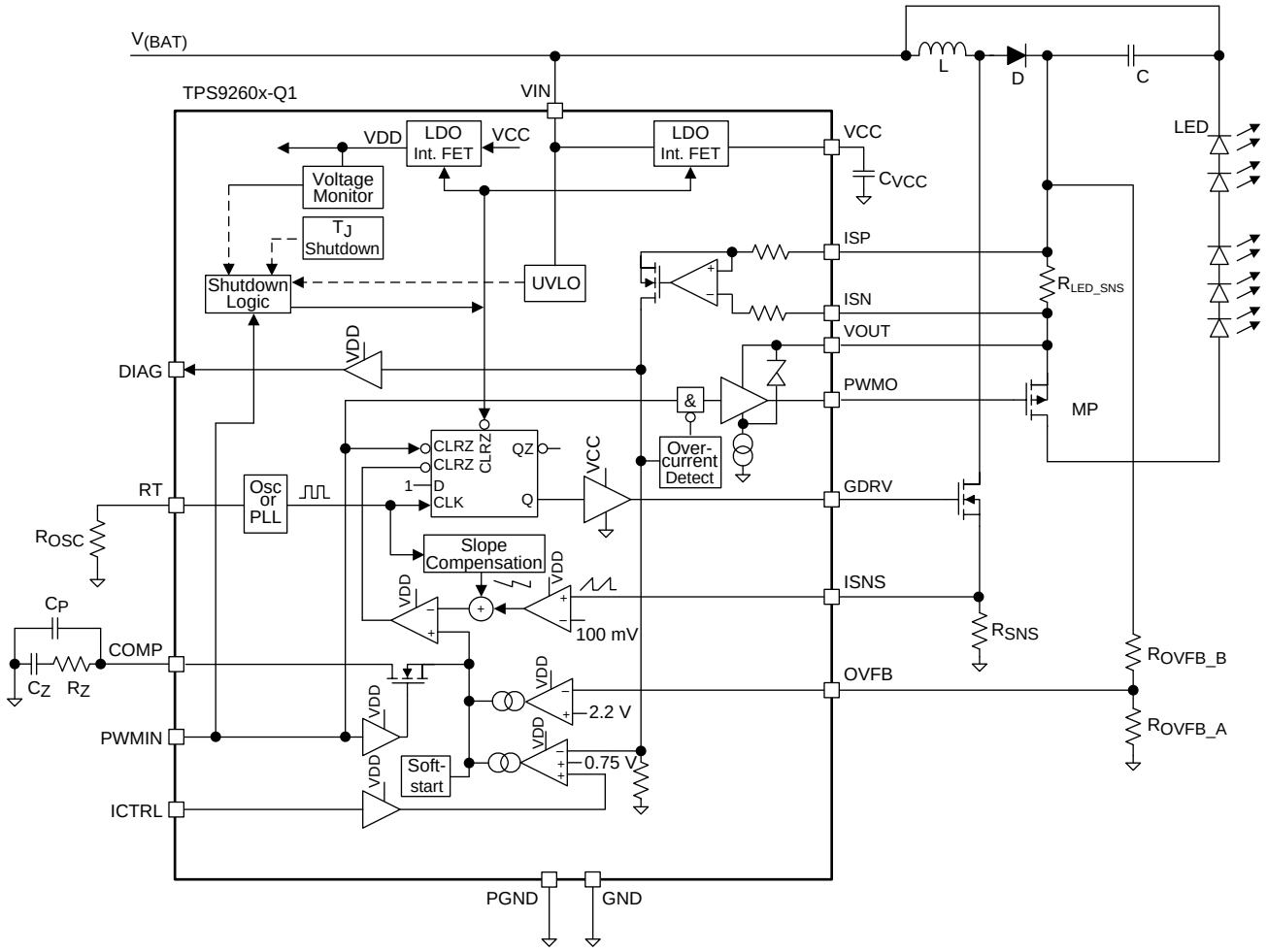
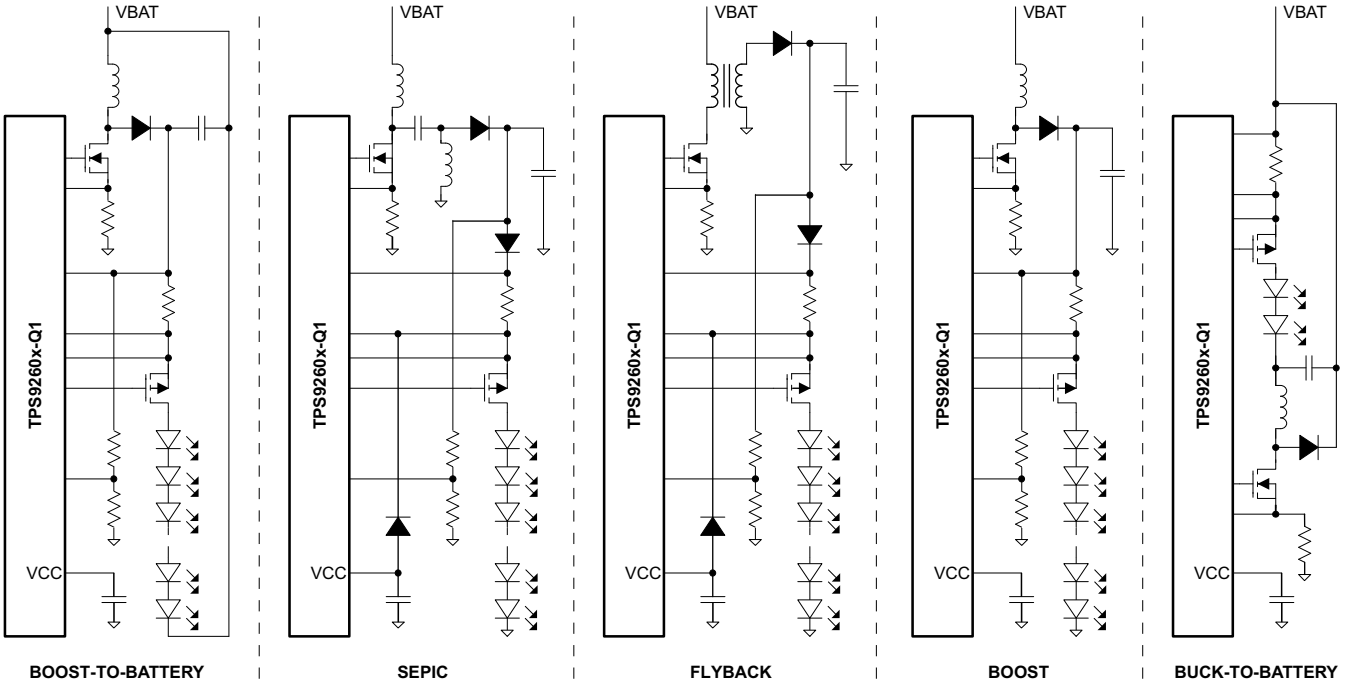


Figure 10. Block Diagram, TPS9260xy-Q1 in Boost-To-Battery Configuration

Functional Block Diagram (continued)



Note: The SEPIC and flyback topologies require two extra diodes per channel for start-up, because the minimum common-mode voltage of the current-regulation amplifier is 4 V.

Figure 11. Supported Topologies per Channel

7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

Each boost controller uses an adjustable fixed-frequency peak-current-mode control. In a constant-current application, the device senses the output current across an external shunt resistor at the ISPx and ISNx pins, amplifies and level-shifts it to ground-reference, and compares it to the voltage applied on the ICTRLx pin by the primary error amplifier, which drives the COMPx pin. In a constant-voltage application, the device compares the output voltage through external resistors on the OVFBx pin to an internal 2.2-V voltage reference by a secondary error amplifier, which drives the COMPx pin. Depending on the chosen application, only one of the error amplifiers is active.

An internal oscillator initiates the turnon of the external boost-power NMOS switch. The device compares the error-amplifier output to the switch current sensed on the ISNSx pin. When the power-switch current reaches the level set by the COMPx voltage, the power NMOS switch turns off. The COMPx pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMPx pin voltage to a maximum level.

7.3.2 Slope-Compensation Output Current

Each controller adds a compensating ramp to the switch-current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty-cycle range.

Feature Description (continued)

7.3.3 Boost-Current Limit

Each controller achieves peak-current-mode control using a comparator that monitors the current through the external boost FET at the ISNSx pin by comparing it with the voltage on the COMPx pin. A redundant current-limit comparator, which compares the voltage on the ISNSx pin with a typical 100-mV reference voltage, limits the current through the external boost FET. If the voltage on the ISNSx pin exceeds this typical 100-mV threshold, the on-cycle of the respective boost controller immediately terminates. The current-limit comparator has a lead-edge blanking time to avoid any unwanted triggering of the current limit during switch-on of the external boost FET. One can set the current-limit level with an external resistor, as calculated with the following equation.

$$I_{(Lim)} = \frac{100\ mV}{R_{(LIM)}} \tag{1}$$

7.3.4 Oscillator and PLL

The switching frequency is adjustable over a range from 100 kHz to 600 kHz by placing a resistor on the RT pin. The RT pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 2 or the curve in Figure 4. To reduce the solution size one would typically set the switching frequency as high as possible, but give consideration to tradeoffs of the supply efficiency, maximum input voltage, and minimum controllable on-time.

$$R_{RT}[k\Omega] = \frac{12.5\ MHz \times 1\ k\Omega}{f_{(OSC)}[MHz]} \tag{2}$$

One can also use the RT pin to synchronize the controllers to an external system clock, over a range from 100 kHz to 600 kHz. Apply a square wave to the RT pin to use this synchronization feature. The square wave must transition lower than 0.8 V and higher than 2 V on the RT pin and have an on-time greater than 70 ns and an off time greater than 70 ns. The synchronization frequency range is 100 kHz to 600 kHz. The rising edge of GDRV1 is synchronized to the falling edge of the RT pin signal.

Leaving the RT pin open or shorted to ground with no external system clock signal is present disables both boost controllers, and both PWM dimming FETs switch off. In order to recover from this global failure state, (for example, after the failure condition on the RT pin has been removed) there must be one global disable-and-enable cycle (active shutdown by pulling both PWMINx pins low for $t > t_{(CH\_OFF)}$, and setting one or both PWMINx pins high for $t > t_{(CH\_ON)}$).

7.3.5 Control Loop Compensation

Modeling of the TPS9260xy-Q1 control loop is like that for any current-mode controller. Using a first-order approximation, one can model the uncompensated loop as a single pole created by the output capacitor and, in the boost and buck-boost topologies, a right half-plane zero created by the inductor, where both have a dependence on the dynamic resistance of the LED string. There is also in the model a high-frequency pole which, however, is near the switching frequency and plays no part in the compensation design process. Therefore, the loop analysis neglects this high-frequency pole. Because TI recommends ceramic capacitors for use with LED drivers due to long lifetimes and high ripple-current rating, one can also neglect the ESR of the output capacitor in the loop analysis. Finally, there is a dc gain of the uncompensated loop which depends on internal controller gains and the external sensing network. A boost regulator serves as an example case. See the *Detailed Design Procedure* section for compensation of all topologies.

Equation 3 gives the whole-loop gain for a boost regulator.

$$T_u = T_{uo} \times \frac{\left(1 + \frac{s(j)}{\omega_{ezc}}\right) \times \left(1 - \frac{s(j)}{\omega_{ezrhp}}\right)}{\left(1 + \frac{s(j)}{\omega_{ep0}}\right)} \tag{3}$$

Equation 4 approximates the output pole (ω_{ep0}).

Feature Description (continued)

$$\omega_{ep0} = \frac{2}{r_{(D)} \times C_o}$$

where

- $r_{(D)}$: LED and $R_{(ILED\_SNS)}$ dynamic resistance
- C_O: Output capacitor (4)

Use Equation 5 to calculate the right half-plane zero (ω_{ezrhp}).

$$\omega_{ezrhp} = \frac{r_{(D)} \times D'^2}{L1} \quad (5)$$

Use Equation 6 to calculate the output capacitor and ESR zero (ω_{ezc}).

$$\omega_{ezc} = \frac{1}{r_{esr} \times C_o} \quad (6)$$

The EA transfer function with compensation capacitor and resistor of the system is described in Equation 7 is shown in Equation 7.

$$T_{uo} = Adc \times \frac{\left(1 + \frac{s(j)}{\omega ez1}\right)}{\left(1 + \frac{s(j)}{\omega ep1}\right) \times \left(1 + \frac{s(j)}{\omega ep2}\right)}$$

where

Adc is the error-amplifier (EA) dc gain (7)

Use Equation 8 to calculate the EA output with compensation capacitor pole (ω_{ep1}).

$$\omega_{ep1} = \frac{1}{R_{(o)} \times C_z}$$

where

$R_{(o)}$ is the EA output impendence (8)

The EA higher frequency pole (ω_{ep2} to filter the high-frequency noise, which is higher than whole-loop bandwidth) is shown in Equation 9.

$$\omega_{ep2} = \frac{1}{R_z \times C_p} \quad (9)$$

The EA output ESR zero (ω_{ez1}) is shown in Equation 10.

$$\omega_{ez1} = \frac{1}{R_z \times C_z} \quad (10)$$

Compensator design should give adequate phase margin (above 45°) at the crossover frequency. A simple compensator using a single capacitor at the COMP pin adds a dominant pole to the system, which ensures adequate phase margin if placed low enough. At high duty cycles, the RHP zero places extreme limits on the achievable bandwidth with this type of compensation. However, because an LED driver is essentially free of output transients (except catastrophic failures, open or short), the dominant pole approach, even with reduced bandwidth, is usually the best approach.

7.3.6 LED Open-Circuit Detection

An open LED in any channel interrupts the current flow of that channel. If the LED current in the sensing circuit falls below the defined threshold th_{OLED}, then the device pulls the DIAGx pin of the affected channel low (for example, for use as an interrupt to a microcontroller). The output-voltage regulation is with respect to the set point of the voltage-control loop (resistor divider network on the OVFBx pin). Removal of the failure releases the DIAGx pin automatically.

Feature Description (continued)

7.3.7 Output Short-Circuit and Overcurrent Detection

In case of an external short circuit of a boost output supply line to GND, the respective boost controller of the affected channel is no longer able to limit the current through the control loop. This is because of the conductive path from the supply voltage to the shorted output through the inductor and the boost diode.

To protect the external components from excessive currents, the controller of the affected channel interrupts the path to its output by switching off the high-side PWM-dimming PMOS-FET. The interruption occurs as soon as the high-side current-sense amplifier detects a common-mode voltage below 4 V, or when the voltage on the VOUTx pin is below 4 V, or once the high-side current-sense amplifier hits the shorted-output detection threshold $V_{(OPLED)}$. The protection of each channel operates in this way, independently of the other channel (see state-diagram in Figure 14). The device pulls the DIAGx pin of the affected channel high, and the controller of the affected channel remains in this channel-fail state. In order to reset the controller of the affected channel (for example, after removal of a short circuit) there must be one disable-and-enable cycle for the affected channel by pulling the PWMINx pin low for $t > t_{(CH\_OFF)}$, and setting it high for $t > t_{(CH\_ON)}$.

7.3.8 Measuring LED Current During a Non-Failure Condition

In regular operation mode, one can measure the actual output current of the controller with an external microcontroller by sensing the voltage at the DIAGx pin. The DIAGx pin voltage between 0.2 V and 2.85 V represents in a linear relation the output current measured by the current-sense block across the external shunt resistor. Parameter $DIAG_{factor}$ gives the scale factor of typically 12.5 (the TPS92601y-Q1 or TPS92602y-Q1 device with 150-mV full-scale current-sense voltage) or 6.25 (the TPS92601A-Q1 or TPS92602A-Q1 device with 300-mV full-scale current-sense voltage). Figure 12 gives the relation between the DIAGx pin voltage and the current-sense voltage.

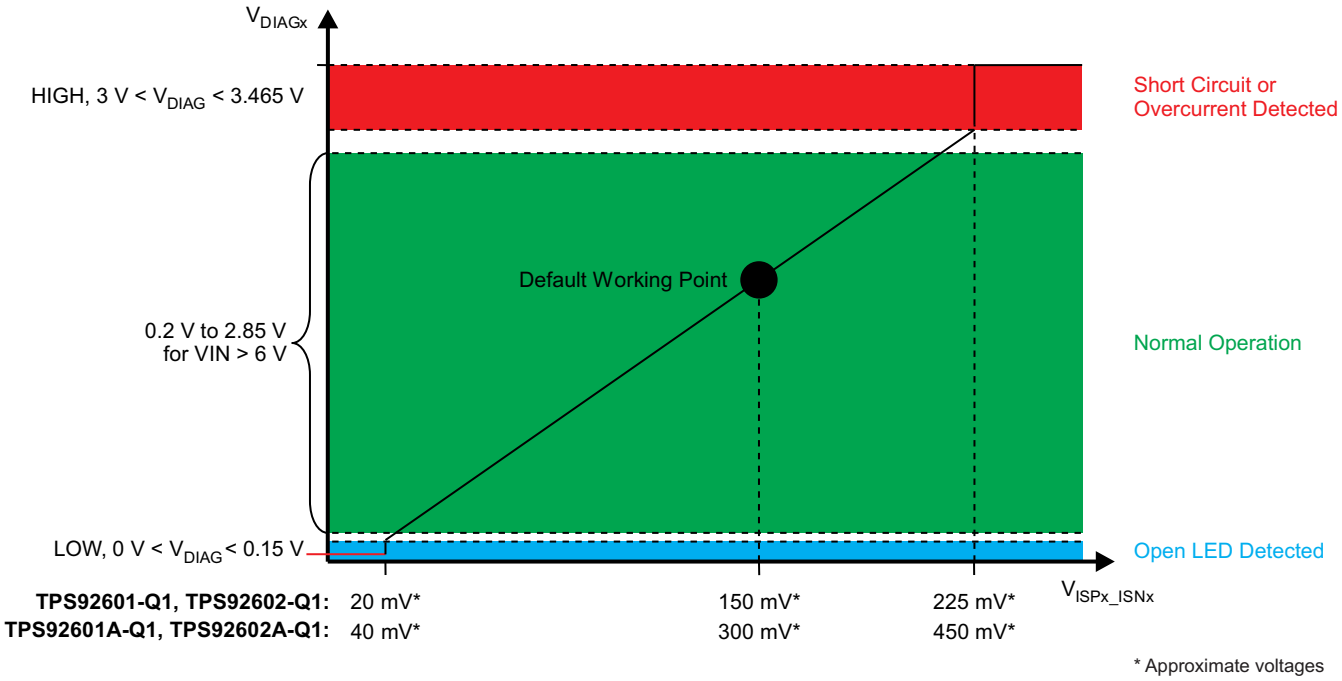


Figure 12. DIAGx Pin Function

When the device is in global shutdown mode (when both PWMINx pins go low for $t > t_{(CH\_OFF)}$), both DIAGx pins are low.

Feature Description (continued)

7.3.9 LED Dimming Options

The device offers two different approaches to regulate and control the brightness and the color of the LEDs: analog dimming and PWM dimming.

7.3.9.1 Analog Dimming

An analog voltage applied to the ICTRLx pin allows changing the output current for each channel on the fly from 10%–100% of full-scale. Typically, this approach is used to:

- Reduce the default current in a narrow range to adjust to different binning classes of the LEDs
- Reduce the current at high temperatures (protect LEDs from overtemperature)
- Reduce the current at low input voltages (for example, cranking-pulse breakdown of the supply)

Implementing this analog dimming function is possible with an analog approach (discrete resistor and NTC network) or with a more-flexible approach by using a microcontroller. Internally clamping the maximum voltage on the ICTRLx pin at 1.5 V simplifies the analog implementation. So applying any higher voltage has no effect on the output current (which remains at its current set point at 100% of full scale, that is, 150 mV or 300 mV drop at the external current shunt resistor).

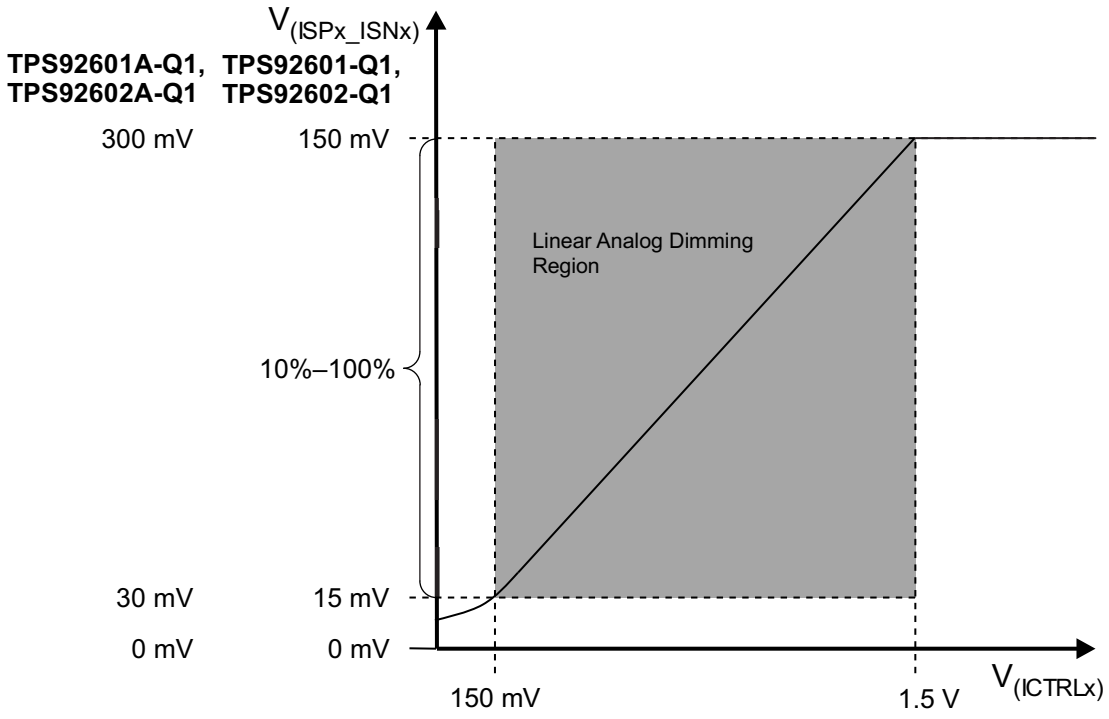


Figure 13. Analog Dimming – ICTRLx Pin

7.3.9.2 PWM Dimming

To change the brightness of an LED string by a certain magnitude without affecting the lighting-color of the LED, it is necessary to use PWM dimming topology. Turning the LEDs ON and OFF at a certain frequency with a certain duty cycle reduces the brightness without changing the LED current (so not affecting the color).

The integrated high-side PMOS-FET gate driver turns the LED string ON and OFF following the supplied signal frequency and duty cycle on the PWMIN pin. During the OFF time of the FET, the device stops the internal control loop by disconnecting the loop internally and then stores the value of the compensation network. This technique allows fastest recovery of the regulator with the following ON time, as the control loop restarts from the point at which it stopped. The average LED current during ON time is almost the same as the LED current with no PWM dimming (duty cycle 100%). For very low duty cycles, the time required by the controller to ramp up the inductor current form 0 A becomes more significant relative to the overall ON time, leading to lower average current. So for very low duty cycles, the relation between average current and duty cycle is no longer linear.

Feature Description (continued)

One must maintain a minimum on-time in order for PWM dimming to operate in the linear region of its transfer function. Because of disabling the controller during dimming, the PWM pulse must be long enough that the energy intercepted from the input is greater than or equal to the energy being put into the LEDs. For boost and boost-to-battery topologies, the minimum ON time (in seconds) for which the PWM dimming operates in the linear region is:

$$t_{(PWMON\_MIN)} = \frac{2 \times I_{(LED)} \times V_{(out)} \times L}{V_{(IN)}^2} \quad (11)$$

To ensure that the applied dimming-pulse duration matches with the effective dimming-pulse duration, TI recommends synchronizing the dimming pulses with the switching clock of the boost converter. Choose the external inductor and output capacitors according to the requirements for the minimum duty cycle.

7.4 Device Functional Modes

7.4.1 Undervoltage and Overvoltage Shutdown

During normal operation (6 V < $V_{(VIN)}$ < 40 V), when the supply voltage at the VIN pin drops below 4 V during cranking, each boost controller is disabled (when previously in normal operation). As long as the battery voltage stays above 3.5 V, both PWM dimming FETs are still controllable through the PWMINx pins, and the V_{CC} regulator is still active. The supply voltage recovering above 4 V re-enables each boost controller (which was working normally before the supply voltage drop). When supply voltage at the VIN pin drops below 3.5 V, the device enters standby due to battery undervoltage. From standby mode, re-enabling the device can only occur when the supply voltage is above 6 V and one or both PWMINx pins are high for t > $t_{(CH\_ON)}$). See the state diagram in Figure 14. When the supply voltage at the VIN pin goes above 40 V during load-dump, the device disables both boost controllers due to battery overvoltage, and switches both PWM dimming FETs off. The V_{CC} regulator is still active. Once the battery voltage is below 40 V, the device recovers from this global failure state after a global disable-and-enable cycle (active shutdown by pulling both PWMINx pins low for t > $t_{(CH\_OFF)}$, and setting one or both PWMINx pins high for t > $t_{(CH\_ON)}$). See the state diagram in Figure 14.

7.4.2 Overtemperature Shutdown

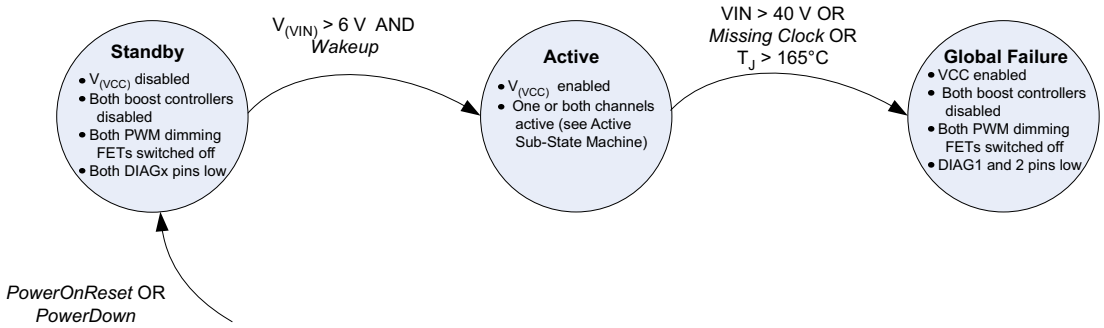
When the junction temperature rises above 165ºC, both boost controllers are disabled due to junction overtemperature, and both PWM dimming FETs are switched off. Once the junction temperature is below 145ºC, the device recovers from this global failure state or a global disable-and-enable cycle (active shutdown by pulling both PWMINx pins low for t > $t_{(CH\_OFF)}$, and setting one or both PWMINx pins high for t > $t_{(CH\_ON)}$). See the state diagram in Figure 14.

7.4.3 Device State Diagram

Figure 14 shows the state diagram of the device, with a short description of the device behavior in each state.

Device Functional Modes (continued)

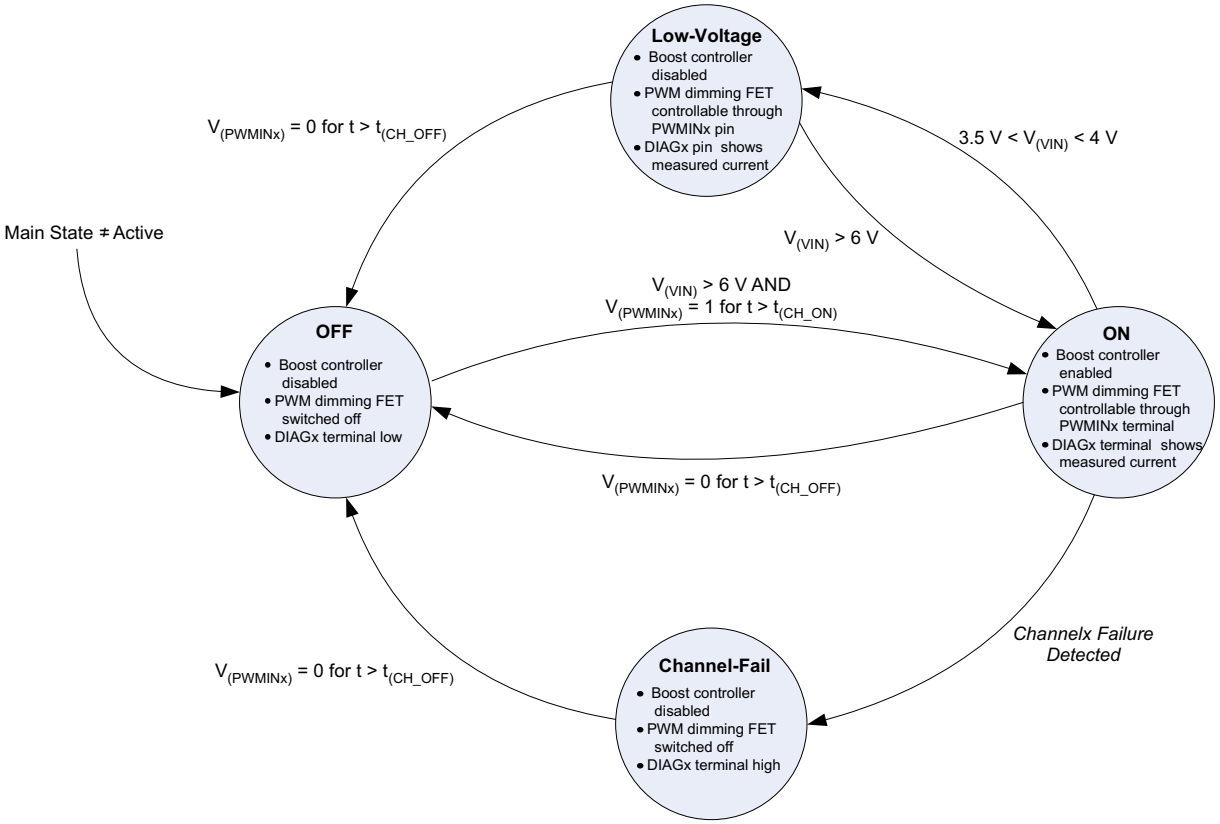
Main State Machine



WakeUp = ($V_{(PWMIN1)}$ = 1 for t > $t_{(CH\_ON)}$ OR $V_{(PWMIN2)}$ = 1 for t > $t_{(CH\_ON)}$)
PowerDown = ($V_{(PWMIN1)}$ = 0 for t > $t_{(CH\_ON)}$ AND $V_{(PWMIN2)}$ = 0 for t > $t_{(CH\_ON)}$)
Missing Clock = RT terminal open AND no sync pulse
PowerOnReset = $V_{(VIN)}$ < 3.5 V

Active Sub-State Machine

Each channel can independently follow this State Machine.



Channelx Failure Detected = ($V_{(VOUTx)}$ < 4 V OR $V_{(SPSNx\_Com)}$ < 4V OR $V_{(SPSNx\_Diff)}$ > $th_{(SHOUT)}$)

NOTE: In the case of an open LED on channel x, the DIAGx pin is low, but the boost controller and the PWM dimming FET of channel x work normally. Hence, the behavior is as in the ON state or the low-voltage state.

Figure 14. Device State Diagram

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section describes the application-level considerations when designing with the TPS9260xy-Q1 family of devices. For corresponding calculations, see the following section.

8.2 Typical Applications

In an application directly connected to a battery, if the application is a passenger car, $V_{(VIN)}$ is from 9 V to 16 V, and LED forward voltage is always higher than battery, then one can select the boost topology. If the LED forward voltage is between 9 V and 16 V, boost-to-battery or single-ended primary-inductance converter (SEPIC) topology is appropriate.

8.2.1 Boost Regulator With Separate or Paralleled Channels

A boost application is appropriate for a situation where $V_{(VIN)}$ is from 9 V to 16 V and LED forward voltage is always higher than battery the battery voltage. One can use the boost-regulator topology with each channel driving a separate LED string. For higher-current applications, connect both channels in parallel to drive a single LED string. The per-channel design parameters and calculations are the same in either case.

Typical Applications (continued)

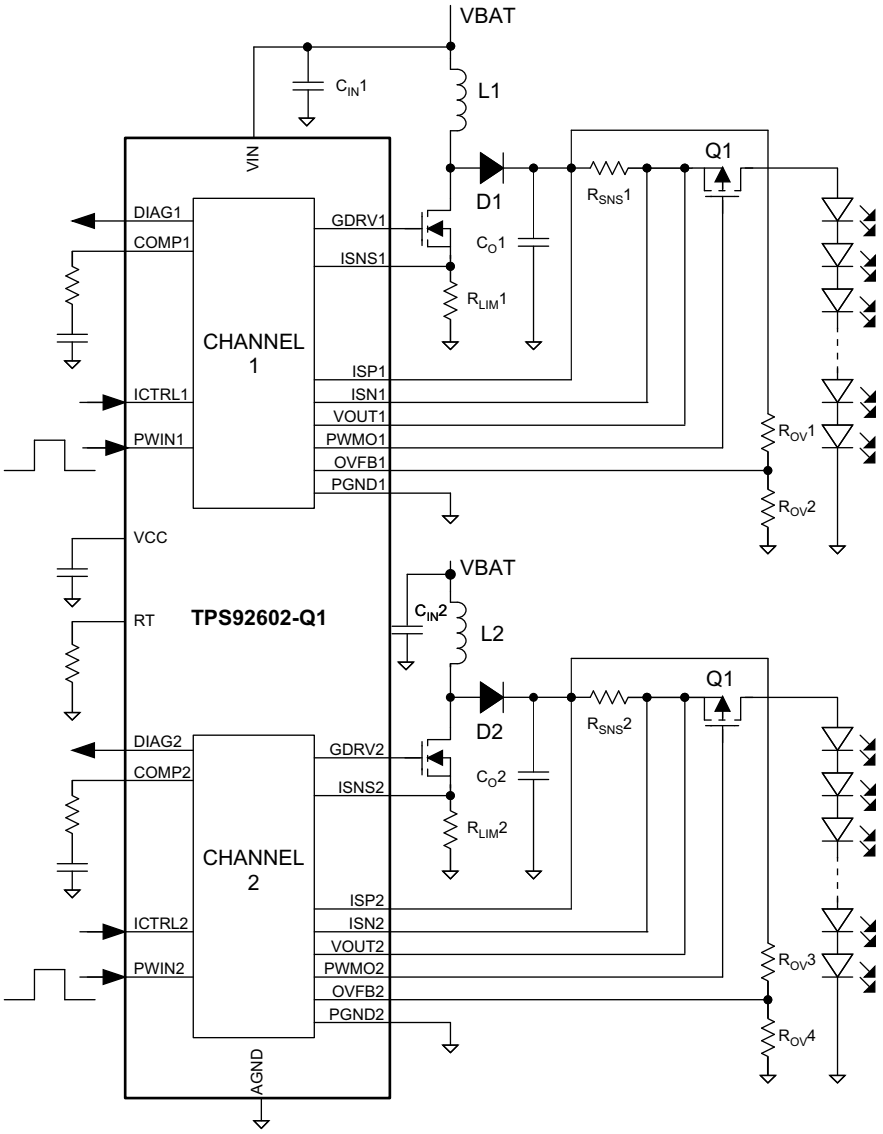


Figure 15. Boost Regulator (V_{IN} < V_O) Simplified Schematic, Separate Channels

Typical Applications (continued)

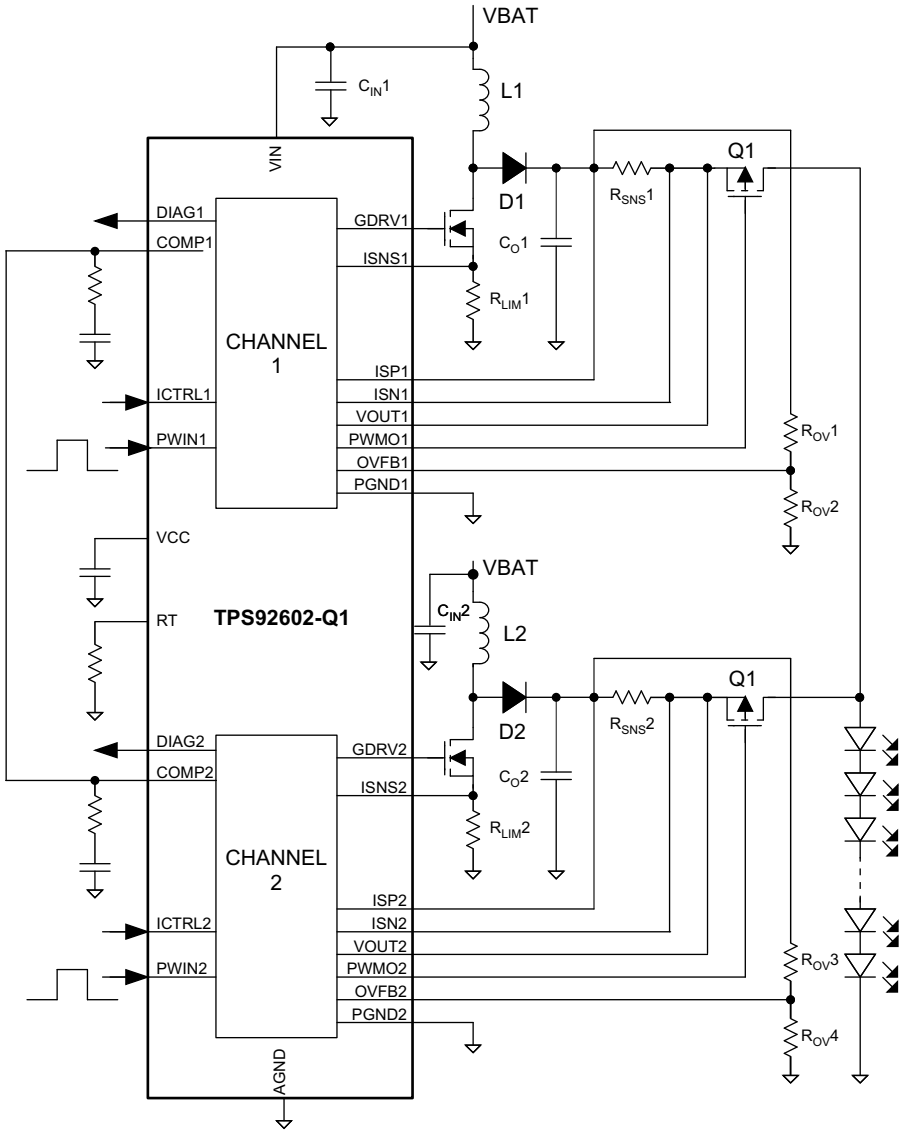


Figure 16. Boost Regulator (V_{IN} < V_O) Simplified Schematic, Paralleled Channels

Typical Applications (continued)

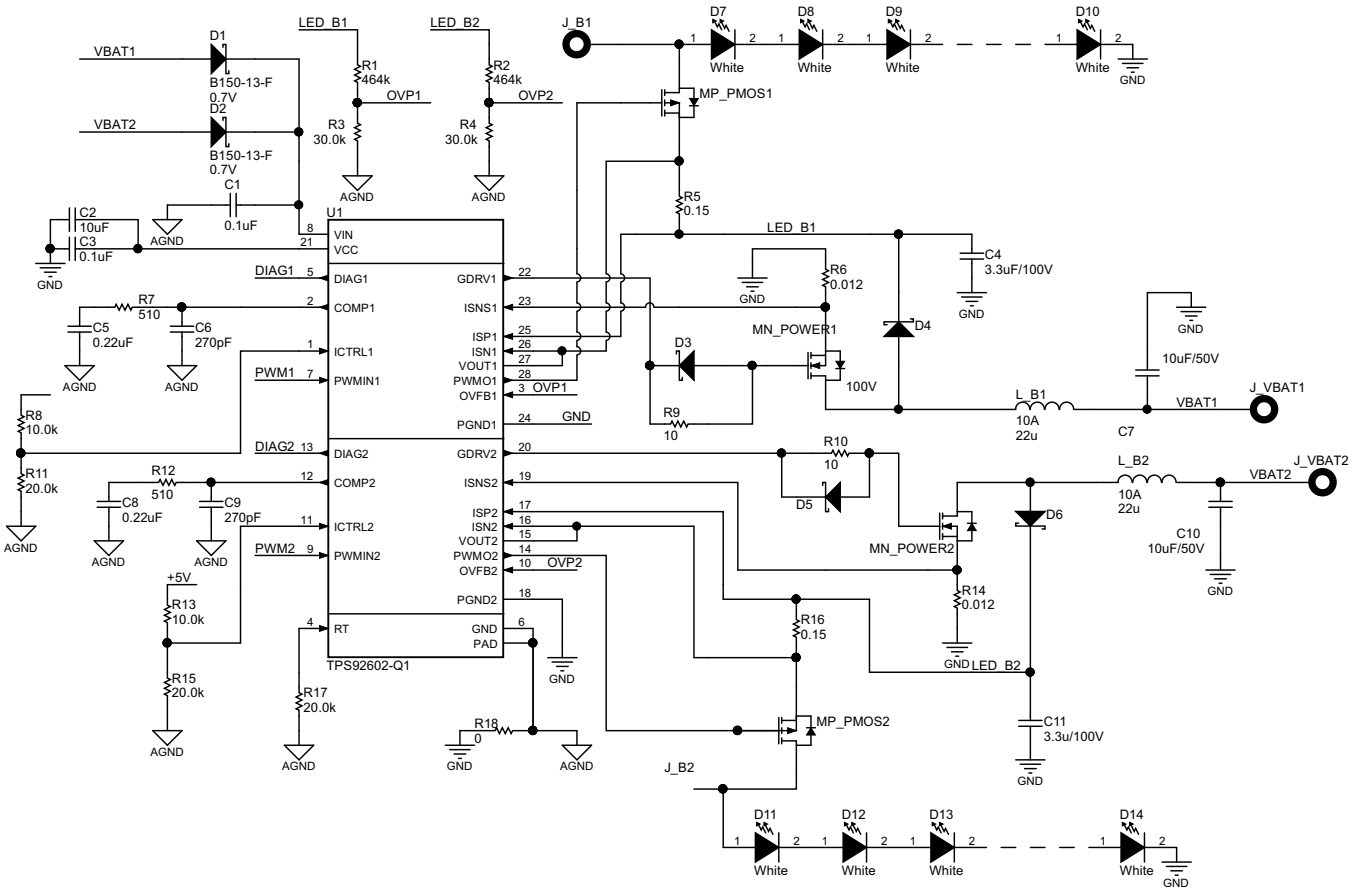


Figure 17. Boost Regulator (V_{IN} < V_O) Detailed Schematic

8.2.1.1 Design Requirements

For this boost regulator example, use the following as the design parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	Connect to battery (6 V to 16 V)
Output current per channel ($I_{(setting)}$)	1 A
Output voltage	30 V (9 white LEDs)
Input ripple voltage	400 mV
Output ripple current	±10%
Operating frequency	600 kHz

8.2.1.2 Detailed Design Procedure

To begin the design process, one must decide on a few parameters. The designer must know the following:

- Input voltage range
- Output current per channel
- Output voltage
- Input ripple voltage
- Output ripple current
- Operating frequency

8.2.1.2.1 Switching Frequency

The RT pin resistor sets the switching frequency of the TPS92602y-Q1 device. Use Equation 2 to calculate the required value for R17. The calculated value is 20.83 kΩ. Use the nearest standard value of 20 kΩ.

8.2.1.2.2 Maximum Output-Current Set Point

The constant output current of the TPS92602y-Q1 device is adjustable by using the external current-shunt resistor. In the application circuit of Figure 17, R5 is the channel 1 current-shunt resistor, and R16 is the channel-2 current shunt resistor. Equation 12 and Equation 13 calculate the resistors that determine maximum output current.

$$R_{(sense)} = V_{SPSN\_Diff} / I_{(setting)} \quad (12)$$

$$R5 = R16 = 150\ mV / 1\ A = 0.15\ \Omega \quad (13)$$

8.2.1.2.3 Output Overvoltage-Protection Set Point

The output overvoltage protection threshold of the TPS92602y-Q1 device is externally adjustable using a resistor divider network. In the application circuit of Figure 17, this divider network comprises R1 and R3 for channel1 and R2 and R4 for channel2. The following equation gives the relationship of the overvoltage-protection threshold ($V_{(OVPT)}$) to the resistor divider.

$$R1 / R3 = R2 / R4 = (V_{(OVPT)} - V_{(VFB)}) / V_{(VFB)} \quad (14)$$

The load is nine white LEDs, the forward voltage is about 30 V. For an overvoltage protection margin of 20%, $V_{(OVPT)}$ is: $V_{(OVPT)}$ = 30 × 1.2 = 36 V. So R1 / R3 = R2 / R4 = (36 – 2.2) / 2.2 = 15.36. Select R3 = R4 = 30 kΩ; then R1 = R2 = 460 kΩ. Use the nearest standard value of 464 kΩ.

8.2.1.2.4 Duty Cycle Estimation

Estimate the duty cycle of the main switching MOSFET using Equation 15 and Equation 16.

$$D_{(MIN)} \approx \frac{V_{(OUT)} - V_{(IN\text{-}max)} + V_{(FD)}}{V_{(OUT)} + V_{(FD)}} = \frac{30\ V - 16\ V + DMIN\ 0.5\ V}{30\ V + 0.5\ V} = 47.5\%$$

where

D is the duty cycle in these and all following equations (15)

$$D_{(MAX)} \approx \frac{V_{(OUT)} - V_{(IN\text{-}min)} + V_{(FD)}}{V_{(OUT)} + V_{(FD)}} = \frac{30\ V - 6\ V + 0.5\ V}{30\ V + 0.5\ V} = 80.3\% \quad (16)$$

Using an estimated forward drop of 0.5 V for a Schottky rectifier diode, the approximate duty cycle is 47.5% (minimum) to 80.3% (maximum).

8.2.1.2.5 Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current.

$$I_{(Lrip\text{-}max)} = 0.3 \times \frac{I_{(OUT\text{-}max)}}{1 - D_{(MIN)}} = 0.3 \times \frac{1}{1 - 0.475} = 0.571\ A \quad (17)$$

Estimate the minimum inductor size using Equation 18.

$$L_{(MIN)} >> \frac{V_{(IN\text{-}max)}}{I_{(Lrip\text{-}max)}} \times D_{(MIN)} \times \frac{1}{f_{(SW)}} = \frac{16\ V}{0.571\ A} \times 0.475 \times \frac{1}{600\ kHz} = 22.1\ \mu H \quad (18)$$

Select the nearest standard inductor value of 22 µH. Estimate the ripple current using Equation 19.

$$I_{(RIPPLE)} \approx \frac{V_{(IN)}}{L} \times D_{(MIN)} \times \frac{1}{f_{(SW)}} = \frac{16\ V}{22\ \mu H} \times 0.475 \times \frac{1}{600\ kHz} = 0.575\ A \quad (19)$$

$$I_{(RIPPLE\text{-}Vinmin)} \approx \frac{V_{(IN)}}{L} \times D_{(MIN)} \times \frac{1}{f_{(SW)}} = \frac{6\ V}{22\ \mu H} \times 0.475 \times \frac{1}{600\ kHz} = 0.365\ A \quad (20)$$

The worst-case peak-to-peak ripple current occurs at 47.5% duty cycle and is estimated as 0.575 A. Equation 21 estimates the worst-case rms current through the inductor.

$$I_{(Lrms)} = \sqrt{(I_{(L\text{-}avg)})^2 + \left(\left[\frac{1}{12} \times I_{(RIPPLE)}\right]\right)^2} \approx \sqrt{\left(\frac{I_{(OUT\text{-}max)}}{1 - D_{(MAX)}}\right)^2 + \left(\frac{1}{12} \times I_{(RIPPLE\text{-}Vinmin)}\right)^2}$$

$$= \sqrt{\left(\frac{1\ A}{1 - 0.803}\right) + \left(\frac{1}{12} \times 0.365\ A\right)^2} = 5.08\ A\ rms \quad (21)$$

The worst-case rms inductor current is 5.08 A rms. Equation 22 estimates the peak inductor current.

$$I_{(Lpeak)} \approx \frac{I_{(OUT\text{-}max)}}{1 - D_{(MAX)}} + \frac{1}{2} \times I_{(RIPPLE\text{-}Vinmin)} = \frac{1}{1 - 0.083} + 0.5 \times 0.365 = 5.26\ A \quad (22)$$

Select a 22-µH inductor with a minimum rms current rating of 5.08 A and minimum saturation current rating of 5.26 A. The selection is a Wurth 74435572200 inductor (shielded-drum core, ferrite, 22 µH, 11 A, 0.0146 Ω, SMD).

Equation 23 estimates the power dissipation of this inductor

$$P_{(L)} \approx (I_{(Lrms)})^2 \times DCR \quad (23)$$

The Wurth 74435572200 inductor with 14.6-mΩ DCR dissipates 404 mW of power.

8.2.1.2.6 Rectifier Diode Selection

The circuit uses a low-forward-voltage-drop Schottky diode as a rectifier diode to reduce power dissipation and improve efficiency. Use 80% derating for the diode on VOUTx to allow for for ringing on the switch node. Equation 24 gives the rectifier-diode minimum reverse-breakdown voltage.

$$V_{(BR)(R\text{-}min)} \geq \frac{V_{(VOPT)}}{0.8} = 1.25 \times 36\ V = 45\ V \quad (24)$$

The diode must have a reverse-breakdown voltage greater than 45 V. Equation 25 and Equation 26 estimate the rectifier diode peak and average currents.

$$I_{(D\text{-}avg)} \approx I_{(OUT\text{-}max)} = 1\ A \quad (25)$$

$$I_{(D\text{-}peak)} = I_{(L\text{-}peak)} = 5.26\ A \quad (26)$$

For this design, average current is 1 A and peak current is 5.26 A.

Equation 27 estimates the power dissipation in the diode.

$$P_{(D\text{-}max)} \approx V_{(F)} \times I_{(OUT\text{-}max)} = 0.5\ V \times 1\ A = 0.5\ W \quad (27)$$

For this design, the maximum power dissipation is estimated as 0.5 W. After reviewing 45-V and 60-V Schottky diodes, the selection is the 30BQ060PbF diode, Schottky, 60 V, 3 A, SMC. This diode has a forward voltage drop of 0.5 V at 1 A, so the conduction power dissipation is approximately 500 mW, less than half its rated power dissipation.

8.2.1.2.7 Output Capacitor Selection

Assume a maximum LED current ripple of 0.1 × $I_{(LED)}$. Also, assume that the dynamic impedance of the chosen LED is 0.2 Ω (1.8 Ω total for the nine-LED string). The total output-voltage ripple calculation is then as per Equation 28.

$$V_{(VOUT\text{-}ripple)} = 0.1\ A \times 1.8\ \Omega = 180\ mV \quad (28)$$

Assuming a ripple contribution of 95% from bulk capacitance, Equation 29 calculates the output capacitor.

$$C_{(OUT)} = \frac{I_{(OUT)} \times D}{V_{(VOUT\text{-}ripple)} \times 0.95} \times \frac{1}{f_{(SW)}} = \left(\frac{1\ A \times 0.803}{180\ mV \times 0.95}\right) \times \frac{1}{600\ kHz} = 7.83\ \mu F \quad (29)$$

$$ESR = \frac{V_{(VOUT\text{-}ripple)}}{I_{(L\text{-}peak)}} = \frac{9\ mV}{5.26\ A} = 1.71\ m\Omega \quad (30)$$

Use three 3.3-µF capacitors in parallel to achieve the minimum output capacitance of 10 µF. Ensure that the chosen capacitors meet the minimum bulk capacitance requirement at the operating voltage.

8.2.1.2.8 Input Capacitor Selection

Because a boost converter has continuous input current, the input capacitor senses only the inductor ripple current. Equation 31 and Equation 32 calculate the input capacitor values.

$$C_{(IN)} = \frac{I_{(L\text{-}RIPPLE)}}{4 \times v_{(IN\text{-}RIPPLE)} \times f_{(SW)}} = \frac{0.575\ A}{4 \times 60\ mV \times 600\ kHz} = 4\ \mu F \quad (31)$$

$$ESR = \frac{V_{(VIN\text{-}RIPPLE)}}{I_{(L\text{-}RIPPLE)}} = \frac{60\ mV}{2 \times 0.575\ A} = 52\ m\Omega \quad (32)$$

For this design, to meet a maximum input ripple of 60 mV requires a minimum 4-µF input capacitor with ESR less than 52 mΩ. Select a 10-µF X7R ceramic capacitor.

8.2.1.2.9 Current Sense and Current Limit

The maximum allowable current sense resistor value is limited by $R_{(ISNSx)}$. Equation 33 gives this limitation.

$$R_{(ISNSx)} = \frac{V_{(SNS)}}{1.3 \times I_{(L\text{-}peak)}} = \frac{100\ mV}{1.3 \times 5.26\ A} = 14.62\ m\Omega \quad (33)$$

Select a 15-mΩ resistor.

8.2.1.2.10 Switching MOSFET Selection

The TPS92602y-Q1 device drives a ground-referenced N-channel FET. The breakdown voltage is the output voltage plus any voltage spike, with 30% added for a safety margin as shown in Equation 34.

$$V_{(BD\text{-}MOS\text{-}min)} \geq V_{(VOPT)} \times 1.3 = 1.3 \times 36\ V = 46.8\ V \quad (34)$$

Select an N-channel FET with breakdown voltage of 50 V.

Estimate the $r_{DS(on)}$ and gate charge based on the desired efficiency target.

$$P_{(DISS\text{-}total)} \approx P_{(OUT)} \times \left(\frac{1}{\eta} - 1\right) = 30\ V \times 1\ A \times \left(\frac{1}{0.95} - 1\right) = 1.578\ W \quad (35)$$

For a target of 95% efficiency with a 16-V input voltage at 1 A, maximum power dissipation is limited to 1.578 W. The main power-dissipating devices are the MOSFET, inductor, diode, current-sense resistor and the integrated circuit, the TPS92602y-Q1 device.

$$P_{(FET)} < P_{(DISS\text{-}total)} - P_{(L)} - P_{(D)} - P_{(RSNS)} - V_{(IN\text{-}max)} \times I_{(VDD)} \quad (36)$$

This assumption leaves 740 mW of power dissipation for the MOSFET. Allowing half for conduction and half for switching losses, we can determine a target $r_{DS(on)}$ and $Q_{(GS)}$ for the MOSFET by Equation 37 and Equation 38.

$$Q_{(GS)} < \frac{3 \times P_{(FET)} \times I_{(DRIVE)}}{2 \times V_{(OUT)} \times I_{(OUT)} \times f_{(SW)}} = \frac{3 \times 0.5\ W \times 0.7\ A}{2 \times 30\ V \times 1\ A \times 600\ kHz} = 29.2\ nC \quad (37)$$

Calculate a target MOSFET gate-to-source charge of less than 29.2 nC to limit the switching losses to less than 250 mW.

$$r_{DS(on)} < \frac{P_{(FET)}}{2 \times \left(I_{(RMS)}\right)^2 \times D} = \frac{0.5\ W}{2 \times (5.08\ A)^2 \times 0.803} = 12\ m\Omega \quad (38)$$

Selecting a target MOSFET $r_{DS(on)}$ of 12 mΩ limits the conduction losses to less than 250 mW.

8.2.1.2.11 Loop Compensation

The COMP pin on the TPS92602y-Q1 device is for external compensation, allowing optimization of the loop response for each application. The COMP pin is the output of the internal transconductance amplifier. External resistor R7, along with ceramic capacitors C5 and C6 (see Figure 17), connect to the COMP pin to provide poles and zero. The poles and zero, along with the inherent pole and zero in a peak-current-mode control boost converter, determine the closed-loop frequency response. Thhis connection is important to converter stability and transient response. The first step is to calculate the pole and the right half-plane zero of the peak-current-mode boost converter by Equation 39 and Equation 40. To make the loop stable, the loop must have sufficient phase margin at the crossover frequency where the loop gain is 1. To avoid the effect of the right half-plane zero on loop stability, choose a crossover frequency less than 1/5 of $f_{(ZRHP)}$.

$$f_{(p)} = \frac{I_{(OUT)}}{2\pi \times V_{(OUT)} \times C_{(OUT)}} = \frac{1}{2\pi \times R_{(OUT)} \times C_{(OUT)}}$$

where

- $C_{(OUT)}$ is the bulk output capacitance calculated previously
- $R_{(OUT)}$ is the effective output impedance (39)

$$f_{(ZRHP)} = \frac{V_{(OUT)} \times (1-D)^2}{2\pi \times L \times I_{(OUT)}} \quad (40)$$

$$R_{(OUT)} = \frac{\left(R_{(LED)} + R_{(SENSE)}\right) \times V_{(LED)}}{\left(R_{(LED)} + R_{(SENSE)}\right) \times I_{(LED)} + V_{(LED)}}$$

where

$R_{(LED)}$ is the dynamic impedance of the LED string in ohms at the operating current (41)

The loop compensation consists of a series resistor and capacitor ($R_{(COMP)}$ and $C_{(COMP)}$) from COMP to SGND. $R_{(COMP)}$ sets the crossover frequency and $C_{(COMP)}$ sets the zero frequency of the integrator. For optimum performance, use the following equations:

$$g_{M(COMP)} = 1000 \quad (42)$$

$$R_{(COMP)} = \frac{f_{(ZRHP)} \times R_{(ISNSx)}}{5 \times f_{(p)} \times (1-D_{(MAX)}) \times R_{(SENSE)} \times 5 \times GM_{(COMP)}} \quad (43)$$

$$C_{(COMP)} = \frac{1}{2\pi \times R_{(COMP)} \times 5 \times f_{(p)}}$$

where

$f_{(p)}$ is the pole frequency of the power stage calculated by Equation 39 (44)

An output capacitor that is an electrolytic capacitor which has large ESR requires a capacitor to cancel the zero of the output capacitor. Equation 45 calculates the value of this capacitor.

$$C_6 = \frac{C_{(OUT)} \times R_{(ESR)}}{R_{(COMP)}} \quad (45)$$

8.2.1.3 Application Curves

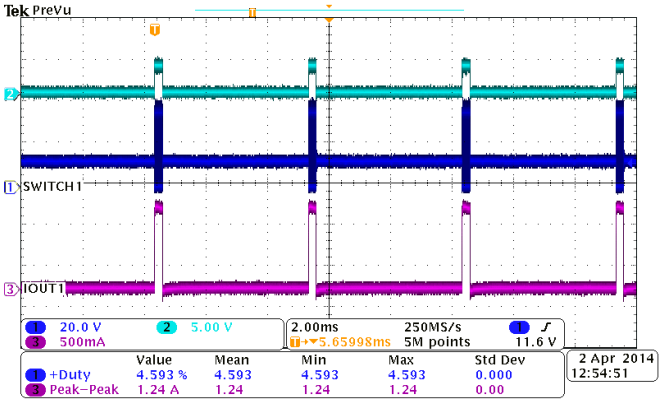


Figure 18. PWM Dimming at 200 Hz, 5% Duty Cycle

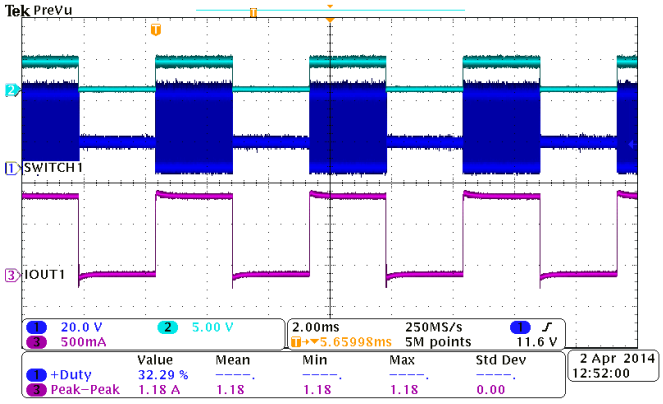


Figure 19. PWM Dimming at 200 Hz, 50% Duty Cycle

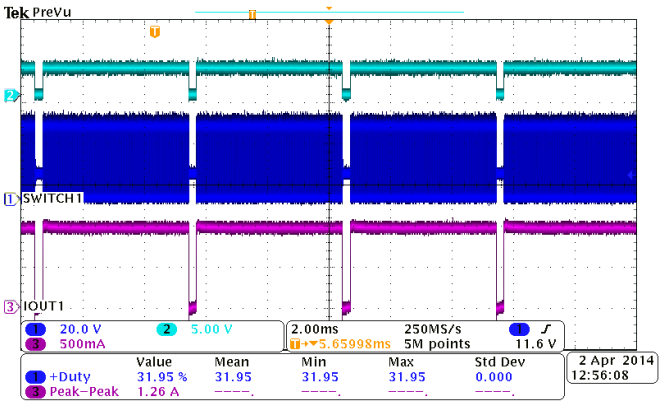


Figure 20. PWM Dimming at 200 Hz, 95% Duty Cycle

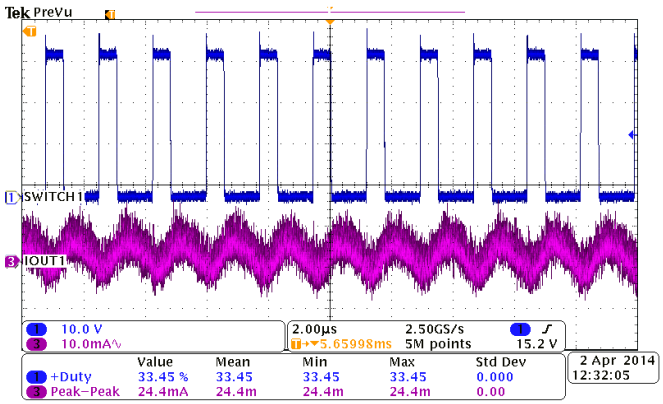


Figure 21. Switching and LED Current Ripple When $I_{(OUT)}$ = 1 A

8.2.2 Boost-to-Battery Regulator

When the LED forward voltage is between 9 V and 16 V, an appropriate selection is boost-to-battery topology, which can share the same layout and components as the boost topology, with just a different way to connect load.

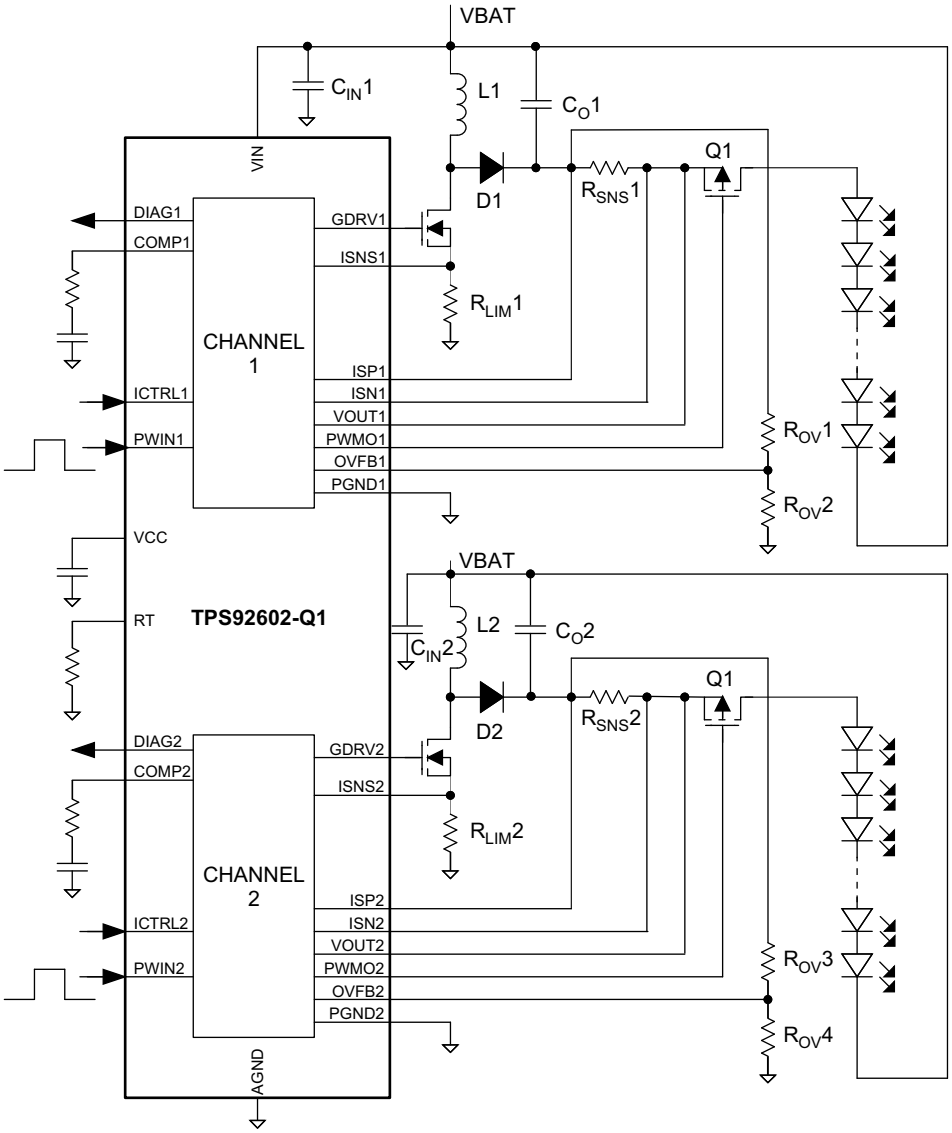


Figure 22. Boost-to-Battery Regulator Simplified Schematic

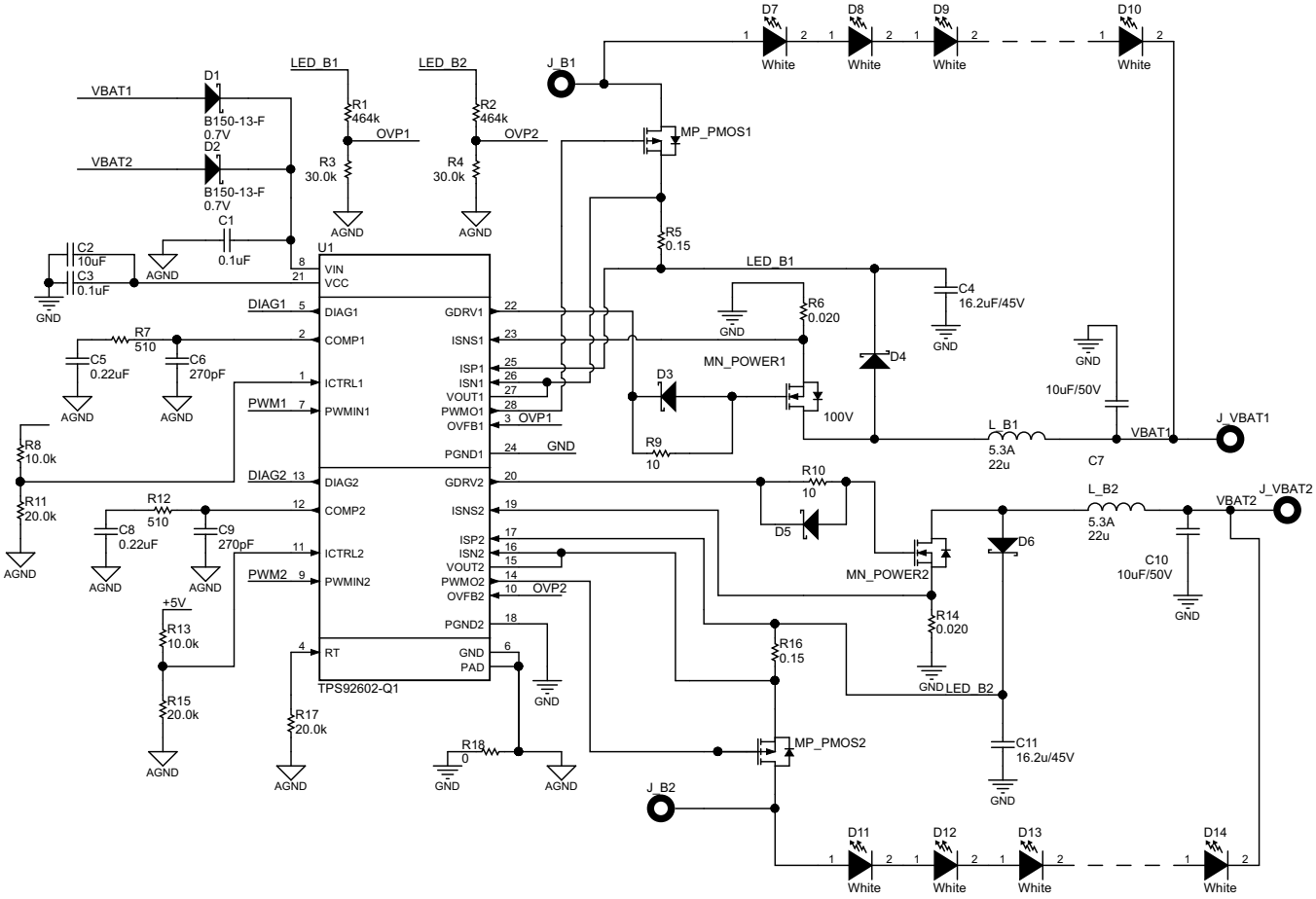


Figure 23. Boost-to-Battery Regulator Detailed Schematic

8.2.2.1 Design Requirements

For this boost-to-battery regulator example, use the following as the design parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	Connect to battery (6 V to 16 V)
Output current per channel ($I_{(setting)}$)	1 A
Output voltage	13.2 V (4 white LEDs)
Input ripple voltage	400 mV
Output ripple current	±10%
Operating frequency	600 kHz

8.2.2.2 Detailed Design Procedure

To begin the design process, one must decide on a few parameters. The designer must know the following:

- Input voltage range
- Output current per channel
- Output voltage
- Input ripple voltage
- Output ripple current
- Operating frequency

8.2.2.2.1 Switching Frequency

The RT pin resistor sets the switching frequency of the TPS92602y-Q1 device to 600 kHz. Use Equation 2 to calculate the required value for R17. The calculated value is 20.83 kΩ. Use the nearest standard value of 20 kΩ.

8.2.2.2.2 Maximum Output-Current Set Point

The output constant of the TPS92602y-Q1 device is adjustable by using the external current-shunt resistor. In the application circuit of Figure 23, R5 is the channel 1 current-shunt resistor, and R16 is the channel-2 current shunt resistor. Equation 46 and Equation 47 calculate the resistors that determine maximum output current.

$$R_{(sense)} = V_{SPSN\_Diff} / I_{(setting)} \quad (46)$$

$$R5 = R16 = 150\ mV / 1\ A = 0.15\ \Omega \quad (47)$$

8.2.2.2.3 Output Overvoltage-Protection Set Point

The output overvoltage protection threshold of the TPS92602y-Q1 device is externally adjustable using a resistor divider network. In the application circuit of Figure 23, this divider network comprises of R1 and R3 for channel1 and R2 and R4 for channel2. The following equation gives the relationship of the overvoltage-protection threshold ($V_{(OVPT)}$) to the resistor divider.

$$R1 / R3 = R2 / R4 = (V_{(OVPT)} - V_{(VFB)}) / V_{(VFB)} \quad (48)$$

The load is four white LEDs, the forward voltage is about 13.2 V, maximum $V_{(VIN)}$ is 16 V, so the maximum output is 13.2 + 16 = 29.2 V, which is close to 30 V. Allowing 20% margin for overvoltage protection, V(OVPT) is: $V_{(OVPT)}$ = 30 × 1.2 = 36 V. So R1 / R3 = R2 / R4 = (36 – 2.2) / 2.2 = 15.36. Select R3 = R4 = 30 kΩ; then R1 = R2 = 460 kΩ. Use the nearest standard value of 464 kΩ.

8.2.2.2.4 Duty Cycle Estimation

Estimate the duty cycle of the main switching MOSFET using Equation 49 and Equation 50.

$$D_{(MIN)} \approx \frac{V_{(LED)} + V_{(FD)}}{V_{(LED)} + V_{(MAX)} + V_{(FD)}} = \frac{13.2\ V + 0.5\ V}{30\ V + 16\ V + 0.5\ V} = 46.1\%$$

where

D is the duty cycle in these and all following equations (49)

$$D_{(MAX)} \approx \frac{V_{(LED)} + V_{(FD)}}{V_{(LED)} + V_{(MIN)} + V_{(FD)}} = \frac{13.2\ V + 0.5\ V}{13.2\ V + 6\ V + 0.5\ V} = 69.5\% \quad (50)$$

Using an estimated forward drop of 0.5 V for a Schottky rectifier diode, the approximate duty cycle is 46.1% (minimum) to 69.5% (maximum).

8.2.2.2.5 Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current.

$$I_{(Lrip\text{-}max)} = 0.3 \times \frac{I_{(OUT\text{-}max)}}{1 - D_{(MIN)}} = 0.3 \times \frac{1}{1 - 0.461} = 0.556\ A \quad (51)$$

Estimate the minimum inductor size using Equation 52

$$L_{(MIN)} >> \frac{V_{(IN\text{-}max)}}{I_{(Lrip\text{-}max)}} \times D_{(MIN)} \times \frac{1}{f_{(SW)}} = \frac{16\ V}{0.571\ A} \times 0.475 \times \frac{1}{600\ kHz} = 22.1\ \mu H \quad (52)$$

Select the nearest higher standard inductor value of 22 µH. Estimate the ripple current using Equation 53.

$$I_{(RIPPLE)} \approx \frac{V_{(IN)}}{L} \times D_{(MIN)} \times \frac{1}{f_{(SW)}} = \frac{16\ V}{22\ \mu H} \times 0.461 \times \frac{1}{600\ kHz} = 0.559\ A \quad (53)$$

$$I_{(RIPPLE\text{-}Vinmin)} \approx \frac{V_{(IN)}}{L} \times D_{(MIN)} \times \frac{1}{f_{(SW)}} = \frac{6\ V}{22\ \mu H} \times 0.695 \times \frac{1}{600\ kHz} = 0.316\ A \quad (54)$$

The worst-case peak-to-peak ripple current occurs at 46.1% duty cycle and is estimated as 0.559 A. Equation 55 estimates the worst-case rms current through the inductor.

$$I_{(Lrms)} = \sqrt{(I_{(L\text{-}avg)})^2 + \left(\left[\frac{1}{12} \times I_{(RIPPLE)}\right]\right)^2} \approx \sqrt{\left(\frac{I_{(OUT\text{-}max)}}{1 - D_{(MAX)}}\right)^2 + \left(\frac{1}{12} \times I_{(RIPPLE\text{-}Vinmin)}\right)^2}$$
$$= \sqrt{\left(\frac{1\ A}{1 - 0.695}\right) + \left(\frac{1}{12} \times 0.3316\ A\right)^2} = 3.28\ A\ rms \quad (55)$$

The worst-case rms inductor current is 3.28 A rms. Equation 56 estimates the peak inductor current.

$$I_{(Lpeak)} \approx \frac{I_{(OUT\text{-}max)}}{1 - D_{(MAX)}} + \frac{1}{2} \times I_{(RIPPLE\text{-}Vinmin)} = \frac{1}{1 - 0.695} + 0.5 \times 0.316 = 3.44\ A \quad (56)$$

Select a 22-µH inductor with a minimum rms current rating of 3.44 A and minimum saturation current rating of 3.44 A. The selection is a Wurth 7447709220 inductor (shielded-drum core, ferrite, 22 µH, 5.3 A, 0.0233 Ω, SMD).

Equation 57 estimates the power dissipation of this inductor

$$P_{(L)} \approx (I_{(Lrms)})^2 \times DCR \quad (57)$$

The Wurth 7447709220 inductor with 23.3-mΩ DCR dissipates 251 mW of power.

8.2.2.2.6 Rectifier Diode Selection

The circuit uses a low-forward-voltage-drop Schottky diode as a rectifier diode to reduce power dissipation and improve efficiency. Use 80% derating for the diode on VOUTx to allow for ringing on the switch node. Equation 58 gives the rectifier-diode minimum reverse-breakdown voltage.

$$V_{(BR)(R\text{-}min)} \geq \frac{V_{(VOPT)}}{0.8} = 1.25 \times 36\ V = 45\ V \quad (58)$$

The diode must have a reverse-breakdown voltage greater than 45 V. Equation 59 and Equation 60 estimate the rectifier diode peak and average currents.

$$I_{(D\text{-}avg)} \approx I_{(OUT\text{-}max)} = 1\ A \quad (59)$$

$$I_{(D\text{-}peak)} = I_{(L\text{-}peak)} = 3.44\ A \quad (60)$$

For this design, average current is 1 A and peak current is 3.44 A.

Equation 61 estimates the power dissipation in the diode.

$$P_{(D\text{-}max)} \approx V_{(F)} \times I_{(OUT\text{-}max)} = 0.5\ V \times 1\ A = 0.5\ W \quad (61)$$

For this design, the maximum power dissipation is estimated as 0.5 W. After reviewing 45-V and 60-V Schottky diodes, the selection is the 30BQ060PbF diode, Schottky, 60 V, 3 A, SMC. This diode has a forward voltage drop of 0.5 V at 1 A, so the conduction power dissipation is approximately 500 mW, less than half its rated power dissipation.

8.2.2.2.7 Output Capacitor Selection

Assume a maximum LED current ripple of 0.1 × $I_{(LED)}$. Also, assume that the dynamic impedance of the chosen LED is 0.2 Ω (0.8 Ω total for the four-LED string). The total output voltage ripple calculation is then as per Equation 62.

$$V_{(VOUT\text{-}ripple)} = 0.1\ A \times 0.8\ \Omega = 80\ mV \quad (62)$$

Assuming a ripple contribution of 95% from bulk capacitance, Equation 64 calculates the output capacitor.

$$C_{(OUT)} = \frac{I_{(OUT)} \times D}{V_{(VOUT\text{-}ripple)} \times 0.95} \times \frac{1}{f_{(SW)}} = \left(\frac{1\ A \times 0.695}{80\ mV \times 0.95}\right) \times \frac{1}{600\ kHz} = 15.2\ \mu F \quad (63)$$

$$ESR = \frac{V_{(VOUT\text{-}ripple)}}{I_{(L\text{-}peak)}} = \frac{4\ mV}{3.44\ A} = 1.16\ m\Omega \quad (64)$$

Use five 3.3-µF capacitors in parallel to achieve the minimum output capacitance of 15.2 µF. Ensure that the chosen capacitors meet the minimum bulk capacitance requirement at the operating voltage.

8.2.2.2.8 Input Capacitor Selection

Because a boost converter has continuous input current, the input capacitor senses only the inductor ripple current. The input capacitor value can be calculated by Equation 65 and Equation 66.

$$C_{(IN)} = \frac{I_{(L\text{-}RIPPLE)}}{4 \times v_{(IN\text{-}RIPPLE)} \times f_{(SW)}} = \frac{0.559\ A}{4 \times 60\ mV \times 600\ kHz} = 3.89\ \mu F \quad (65)$$

$$ESR = \frac{V_{(VIN\text{-}RIPPLE)}}{I_{(L\text{-}RIPPLE)}} = \frac{60\ mV}{2 \times 0.559\ A} = 53.67\ m\Omega \quad (66)$$

For this design, to meet a maximum input ripple of 60 mV requires a minimum 4-µF input capacitor with ESR less than 52 mΩ. Select a 10-µF X7R ceramic capacitor.

8.2.2.2.9 Current Sense and Current Limit

The maximum allowable current sense resistor value is limited by R(ISNSx). Equation 67 gives this limitation.

$$R_{(ISNSx)} = \frac{V_{(SNS)}}{1.3 \times I_{(L\text{-}peak)}} = \frac{100\ mV}{1.3 \times 3.44\ A} = 22.36\ m\Omega \quad (67)$$

Select a 20-mΩ resistor.

8.2.2.2.10 Switching MOSFET Selection

The TPS92602y-Q1 device drives a ground-referenced N-channel FET. The breakdown voltage is the output voltage plus any voltage spike, with 30% added for a safety margin as shown in Equation 68.

$$V_{(BD\text{-}MOS\text{-}min)} \geq V_{(VOPT)} \times 1.3 = 1.3 \times 36\ V = 46.8\ V \quad (68)$$

Select an N-channel FET with breakdown voltage of 50 V.

Estimate the $r_{DS(on)}$ and gate charge based on the desired efficiency target.

$$P_{(DISS\text{-}total)} \approx P_{(OUT)} \times \left(\frac{1}{\eta} - 1\right) = 13.2\ V \times 1\ A \times \left(\frac{1}{0.92} - 1\right) = 1.148\ W \quad (69)$$

For a target of 92% efficiency with a 16-V input voltage at 1 A, maximum power dissipation is limited to 1.148 W. The main power-dissipating devices are the MOSFET, inductor, diode, current-sense resistor and the integrated circuit, the TPS92602y-Q1 device.

$$P_{(FET)} < P_{(DISS\text{-}total)} - P_{(L)} - P_{(D)} - P_{(RSNS)} - V_{(IN\text{-}max)} \times I_{(VDD)} \quad (70)$$

This assumption leaves 600 mW of power dissipation for the MOSFET. Allowing half for conduction and half for switching losses, we can determine a target $r_{DS(on)}$ and $Q_{(GS)}$ for the MOSFET by Equation 71 and Equation 72.

$$Q_{(GS)} < \frac{3 \times P_{(FET)} \times I_{(DRIVE)}}{2 \times V_{(OUT)} \times I_{(OUT)} \times f_{(SW)}} = \frac{3 \times 0.4\ W \times 0.7\ A}{2 \times 13.2\ V \times 1\ A \times 600\ kHz} = 28.3\ nC \quad (71)$$

Calculate a target MOSFET gate-to-source charge of less than 28.3 nC to limit the switching losses to less than 200 mW.

$$r_{DS(on)} < \frac{P_{(FET)}}{2 \times \left(I_{(RMS)}\right)^2 \times D} = \frac{0.4\ W}{2 \times (3.28\ A)^2 \times 0.695} = 26.7\ m\Omega \quad (72)$$

Selecting a target MOSFET $r_{DS(on)}$ of 26.7 mΩ limits the conduction losses to less than 250 mW.

8.2.2.2.11 Loop Compensation

The COMP pin on the TPS92602y-Q1 device is for external compensation, allowing optimization of the loop response for each application. The COMP pin is the output of the internal transconductance amplifier. The external resistor R7, along with ceramic capacitors C5 and C6 (see Figure 23), connect to the COMP pin to provide poles and zero. The poles and zero, along with the inherent pole and zero in a peak-current-mode control boost converter, determine the closed-loop frequency response. This is important to converter stability and transient response. The first step is to calculate the pole and the right half-plane zero of the peak-current-mode boost converter by Equation 73 and Equation 74. To make the loop stable, the loop must have sufficient phase margin at the crossover frequency where the loop gain is 1. To avoid the effect of the right half-plane zero on the loop stability, choose the crossover frequency less than 1/5 of $f_{(ZRHP)}$.

$$f_{(p)} = \frac{I_{(OUT)}}{2\pi \times V_{(OUT)} \times C_{(OUT)}} = \frac{1}{2\pi \times R_{(OUT)} \times C_{(OUT)}}$$

where

- $C_{(OUT)}$ is the bulk output capacitance previously calculated
- $R_{(OUT)}$ is the effective output impedance (73)

$$f_{(ZRHP)} = \frac{V_{(OUT)} \times (1-D)^2}{2\pi \times L \times I_{(OUT)}} \quad (74)$$

$$R_{(OUT)} = \frac{\left(R_{(LED)} + R_{(SENSE)}\right) \times V_{(LED)}}{\left(R_{(LED)} + R_{(SENSE)}\right) \times I_{(LED)} + V_{(LED)}}$$

where

$R_{(LED)}$ is the dynamic impedance of the LED string in ohms at the operating current (75)

The loop compensation consists of a series resistor and capacitor ($R_{(COMP)}$ and $C_{(COMP)}$) from COMP to SGND. $R_{(COMP)}$ sets the crossover frequency and $C_{(COMP)}$ sets the zero frequency of the integrator. For optimum performance, use the following equations:

$$g_{M(COMP)} = 1000 \quad (76)$$

$$R_{(COMP)} = \frac{f_{(ZRHP)} \times R_{(ISNSx)}}{5 \times f_{(p)} \times (1-D_{(MAX)}) \times R_{(SENSE)} \times 5 \times GM_{(COMP)}} \quad (77)$$

$$C_{(COMP)} = \frac{1}{2\pi \times R_{(COMP)} \times 5 \times f_{(p)}}$$

where

$f_{(p)}$ is the pole frequency of the power stage calculated by Equation 73 (78)

An output capacitor that is an electrolytic capacitor which has large ESR requires a capacitor to cancel the zero of the output capacitor. Equation 79 calculates the value of this capacitor.

$$C_6 = \frac{C_{(OUT)} \times R_{(ESR)}}{R_{(COMP)}} \quad (79)$$

8.2.2.3 TPS92602y-Q1 Application Curves

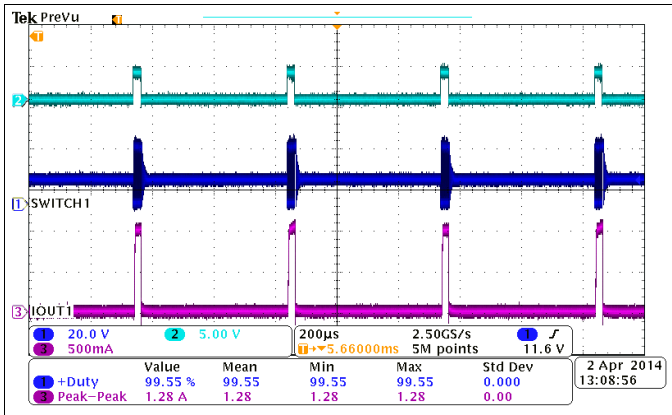


Figure 24. PWM Dimming at 2 kHz, 5% Duty Cycle

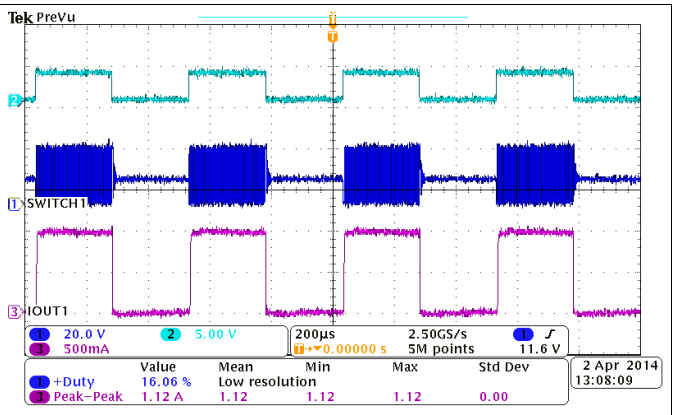


Figure 25. PWM Dimming at 2 kHz, 50% Duty Cycle

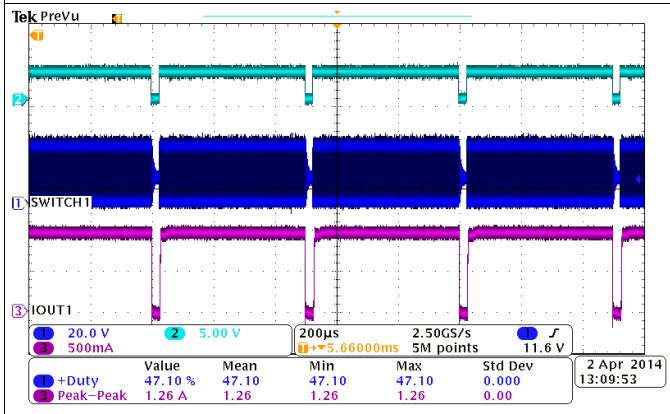


Figure 26. PWM Dimming at 2 kHz, 95% Duty Cycle

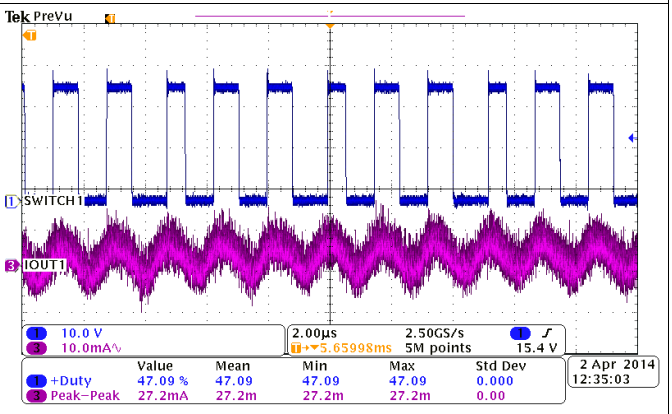


Figure 27. Switching and LED Current Ripple When $I_{(OUT)}$ = 1 A

9 Power Supply Recommendations

The design of the devices is for operation via direct connection to a battery, so the input-voltage supply range is from 4 V to 40 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS9260xy-Q1 family of devices, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

- The performance of any switching regulator depends as much on the layout of the PCB as the component selection. Following a few simple guidelines maximizes noise rejection and minimizes the generation of EMI within the circuit.
- Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing the following paths. The main path for discontinuous current in the TPS9260xy-Q1 buck regulator contains the input capacitor (C_{IN1}), the recirculating diode (D1), the N-channel MOSFET (Q1), and the sense resistor (R_{LIM1}). In the TPS9260xy-Q1 boost regulator, the discontinuous current flows through the output capacitor (C_{O1}), D1, Q1, and R_{LIM1}. In the buck-boost regulator, both loops are discontinuous and require careful attention to layout. Keep these loops as small as possible and the connections between all the components short and thick to minimize parasitic inductance. In particular, make the switch node (where L1, D1 and Q1 connect) just large enough to connect the components. To minimize excessive heating, place large copper pours adjacent to the short current path of the switch node.
- The RT, COMP, ISNS, ICTRL, OVFB, ISP, and ISN pins are all high-impedance inputs which couple external noise easily; therefore, minimize the loops containing these nodes whenever possible. In some applications, the LED or LED array can be far away (several inches or more) from the TPS9260xy-Q1 family of devices, or on a separate PCB connected by a wiring harness. When using an output capacitor where the LED array is large or separated from the rest of the regulator, place the output capacitor close to the LEDs to reduce the effects of parasitic inductance on the ac impedance of the capacitor.
- AGND and PGND must be separated and connected at the input GND connector.
- The TPS9260xy-Q1 family of devices has two independent channels. in order to avoid crosstalk, the POWER GND of CH1 and CH2 must be separated and connected at the input GND connector.

10.2 Layout Example

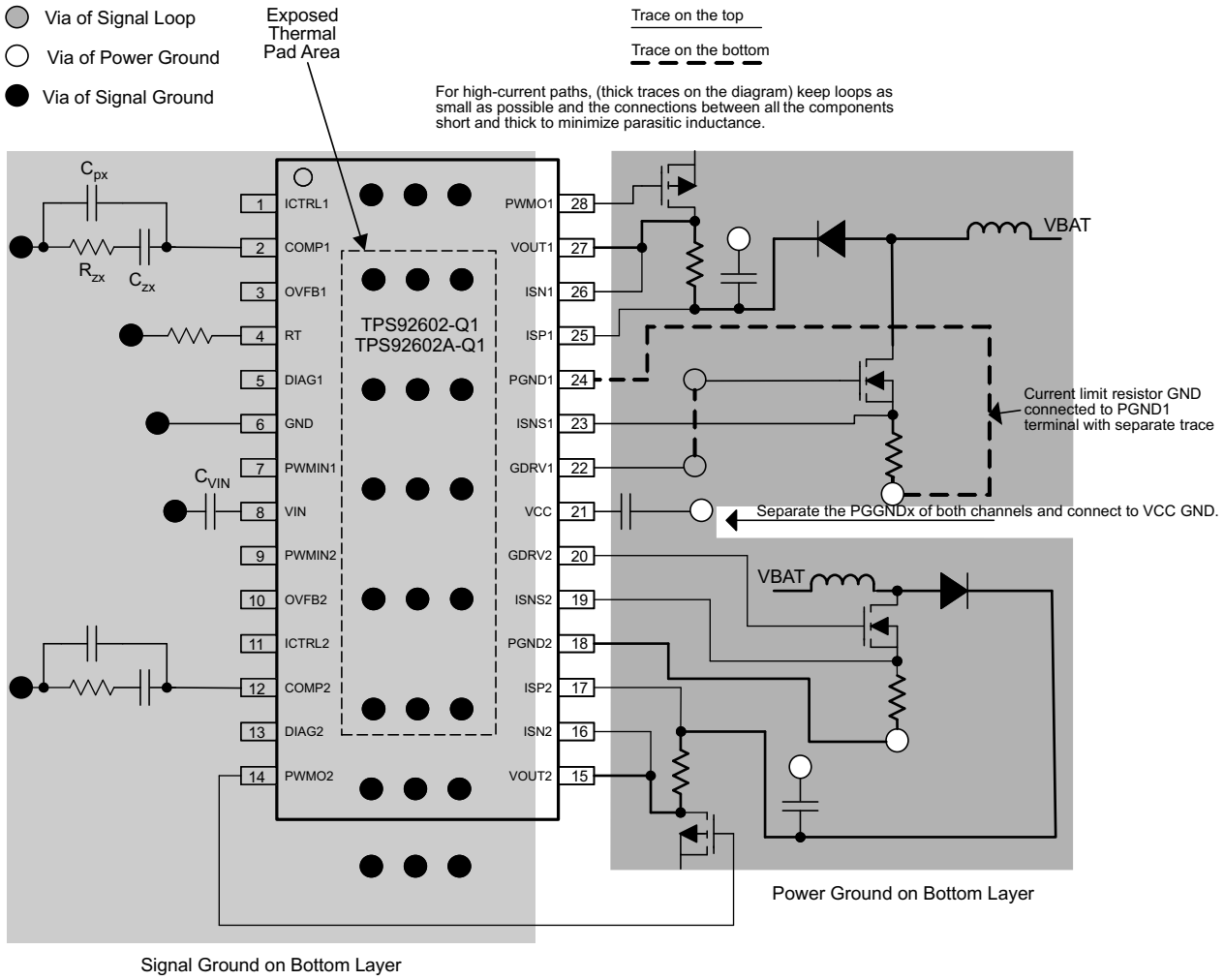


Figure 28. TPS92602y-Q1 Board Layout

11 器件和文档支持

11.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 3. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TPS92601-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS92601B-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS92602-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS92602B-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 商标

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查看左侧的导航面板。

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92601BQPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92601B	Samples
TPS92601QPWPRQ1	NRND	HTSSOP	PWP	20	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92601	
TPS92602BQPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS92602B	Samples
TPS92602QPWPRQ1	NRND	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS92602	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

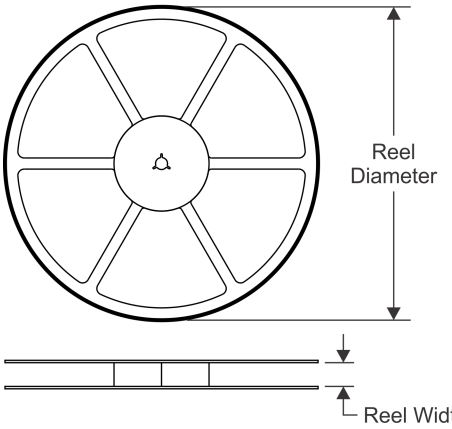
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

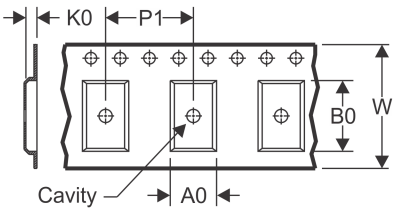
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

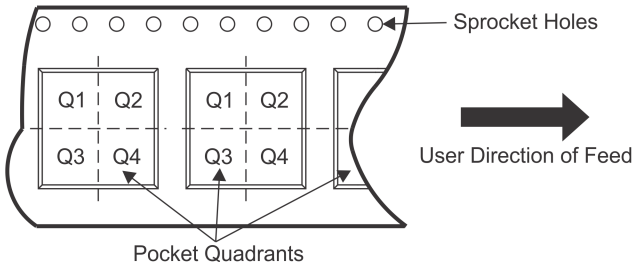


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

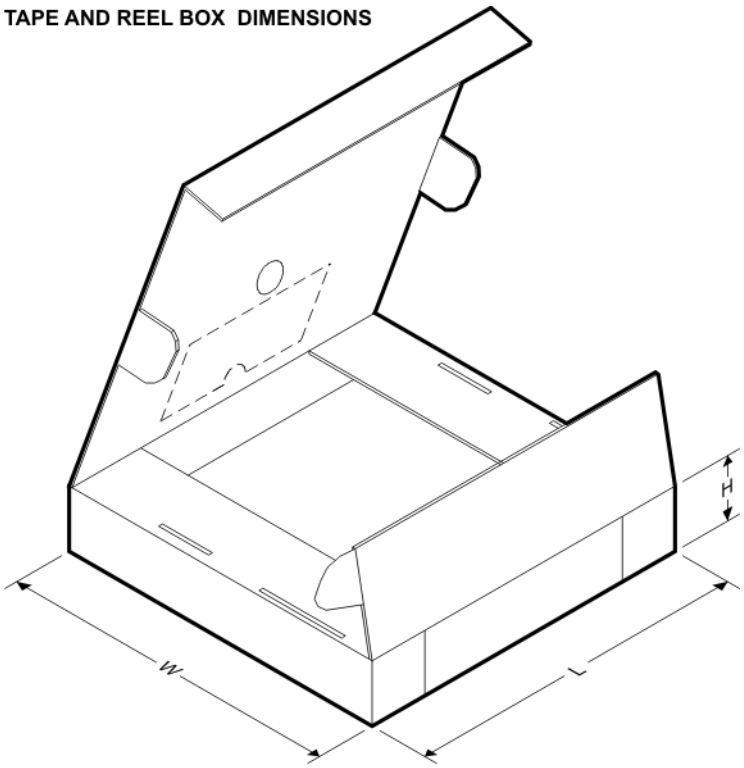
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92601BQPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS92601QPWPRQ1	HTSSOP	PWP	20	3000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS92602BQPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS92602QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92601BQPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS92601QPWPRQ1	HTSSOP	PWP	20	3000	350.0	350.0	43.0
TPS92602BQPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TPS92602QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

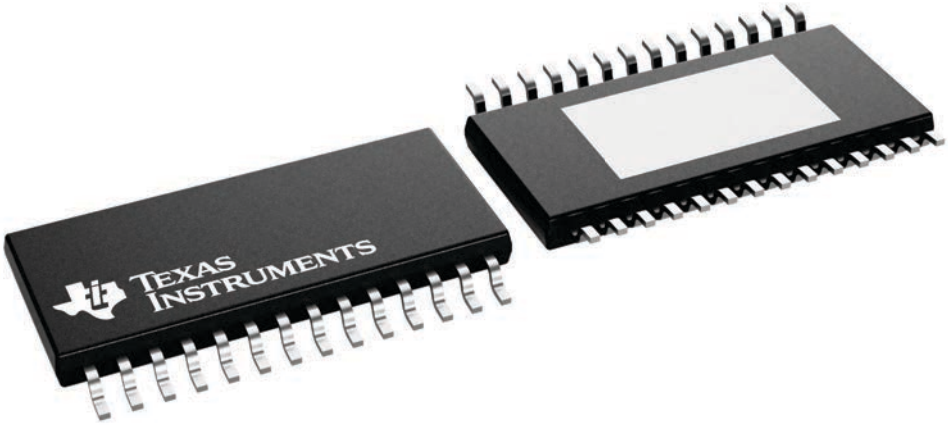
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

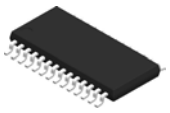
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

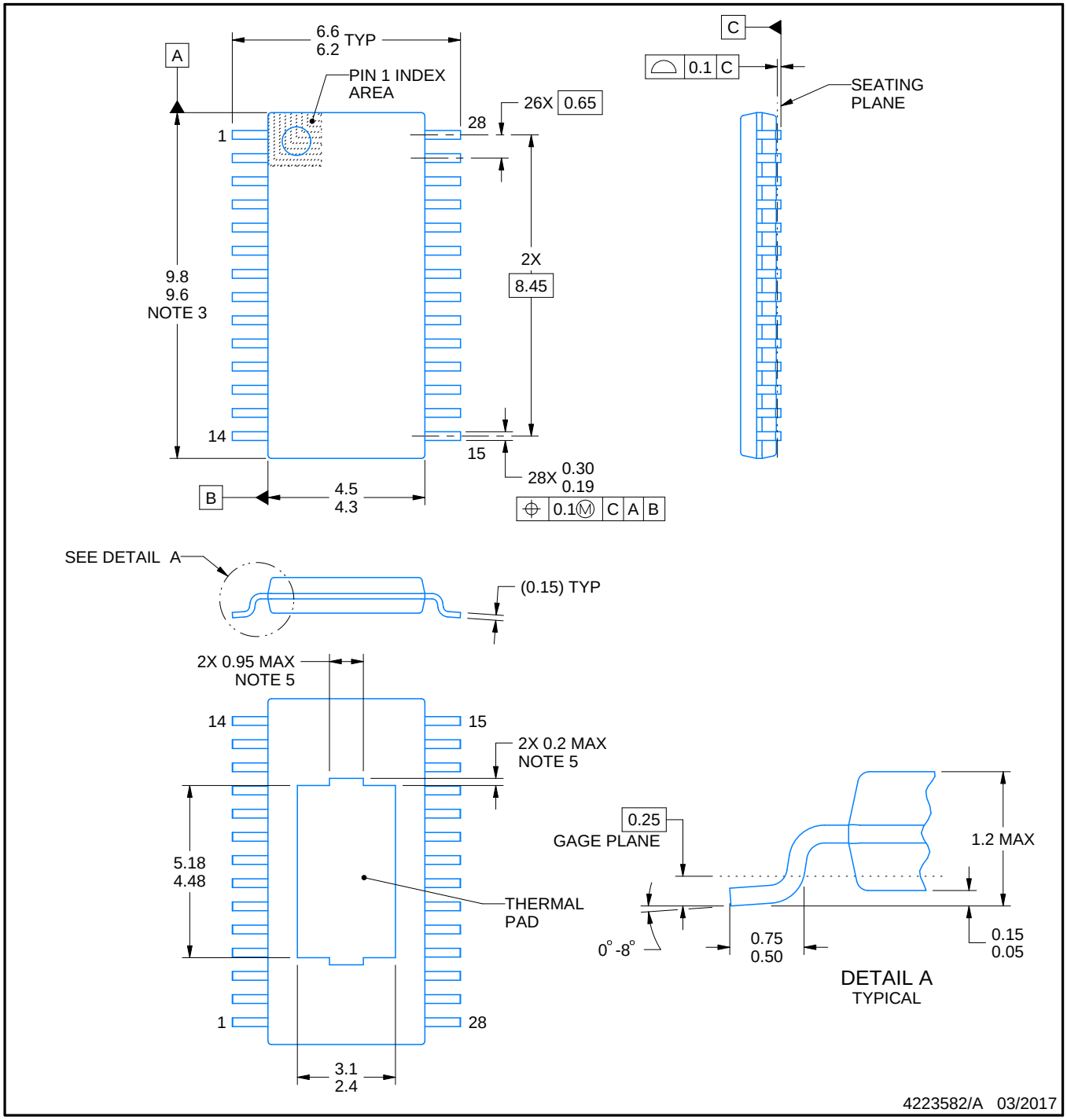
PACKAGE OUTLINE

PWP0028C



PowerPAD™ TSSOP - 1.2 mm max height

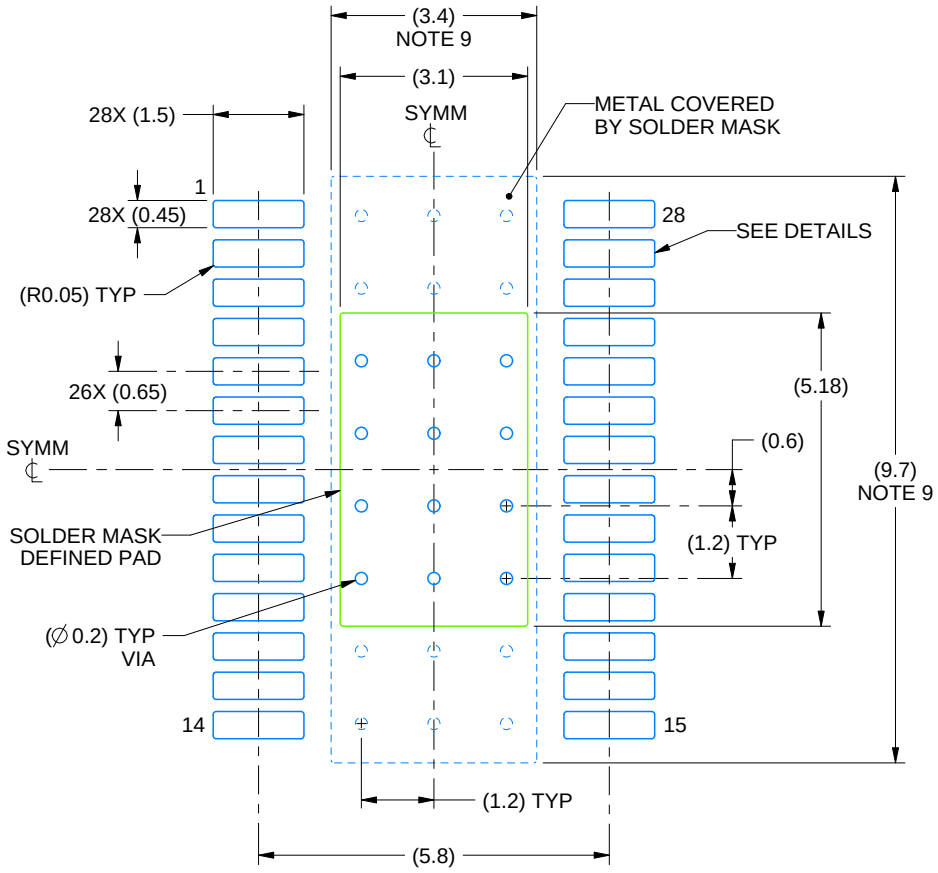
SMALL OUTLINE PACKAGE



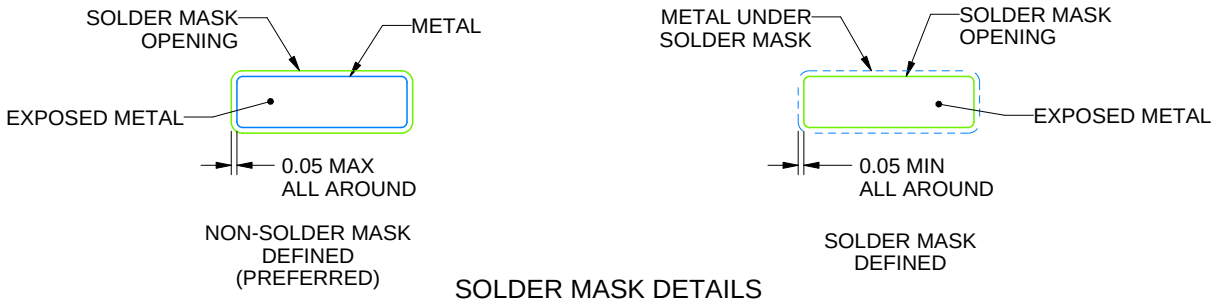
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

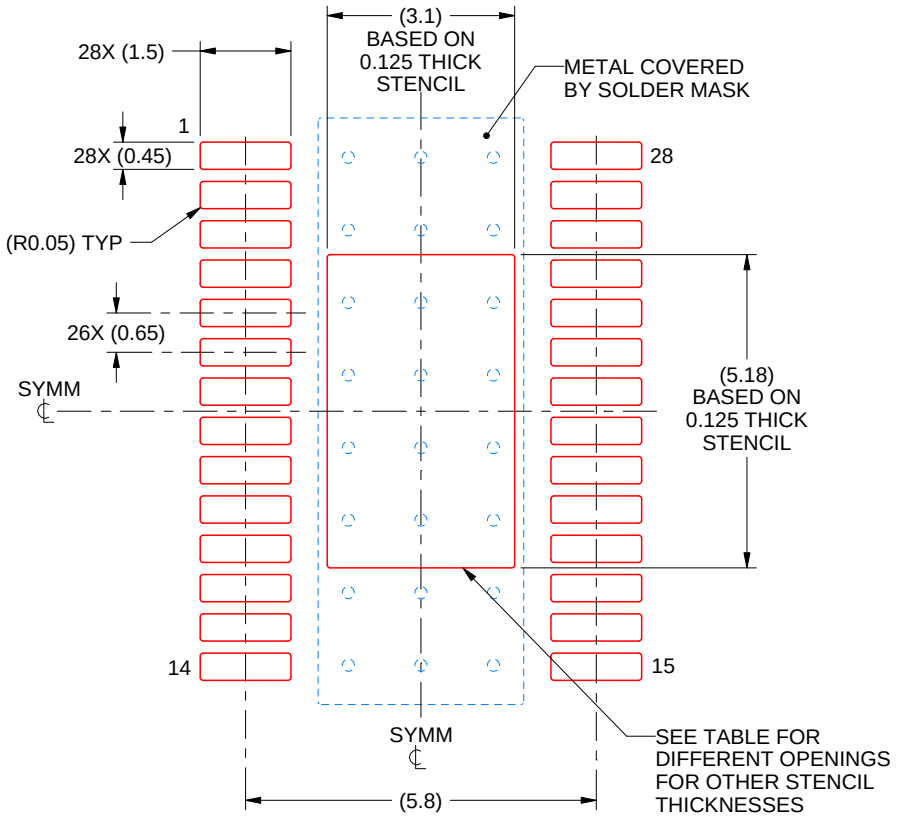


SOLDER MASK DETAILS

4223582/A 03/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

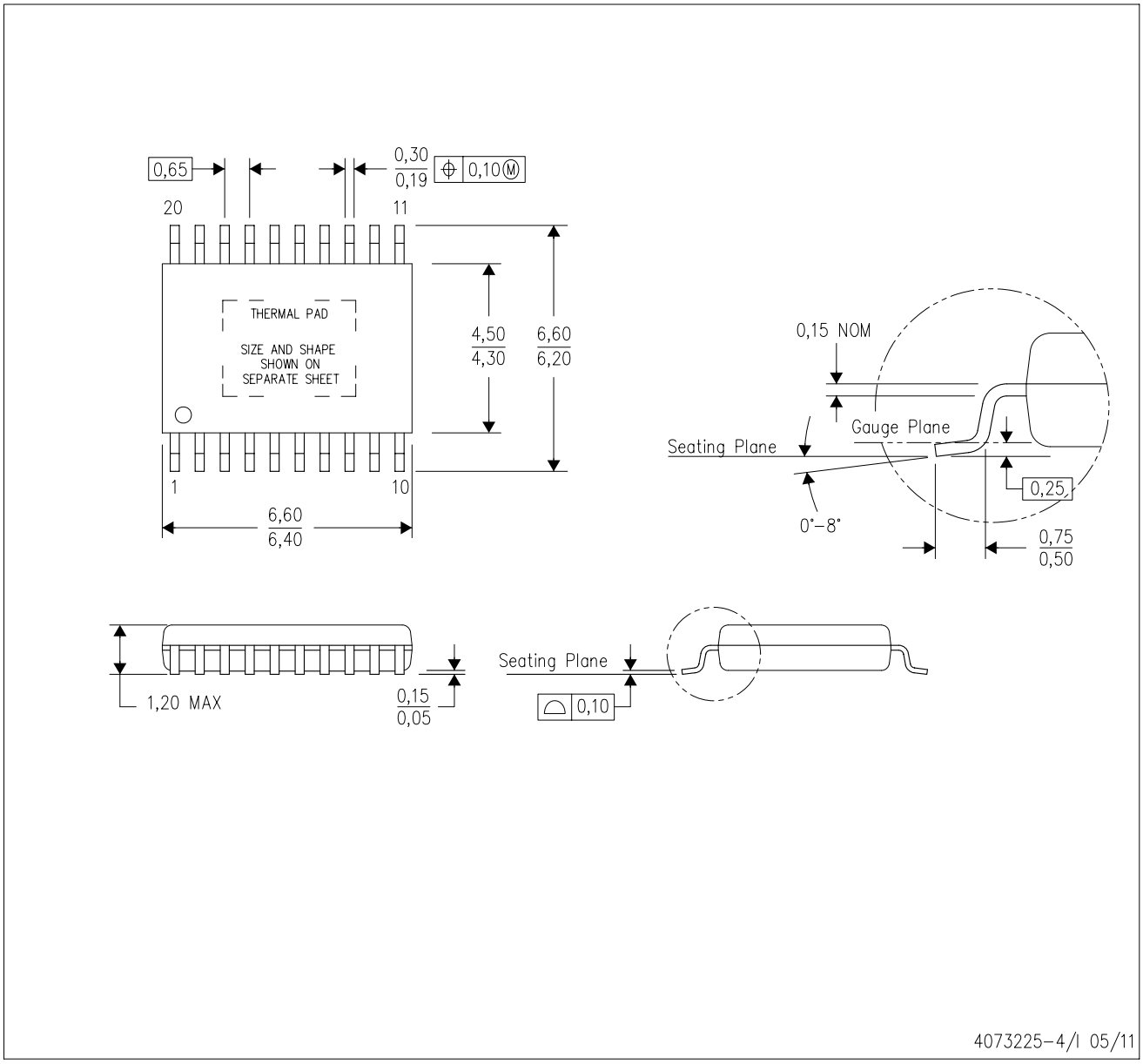
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 5.79
0.125	3.10 X 5.18 (SHOWN)
0.15	2.83 X 4.73
0.175	2.62 X 4.38

4223582/A 03/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

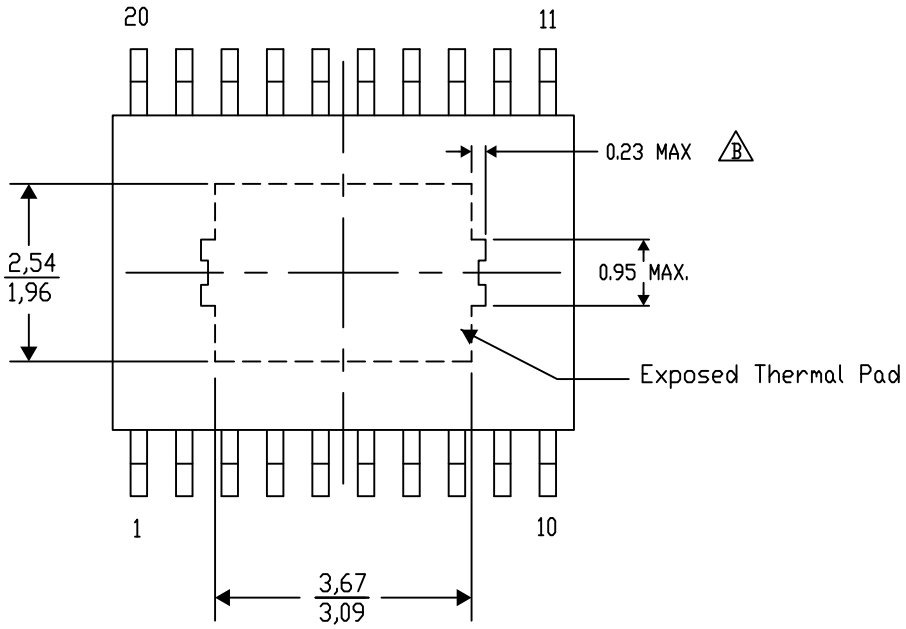
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

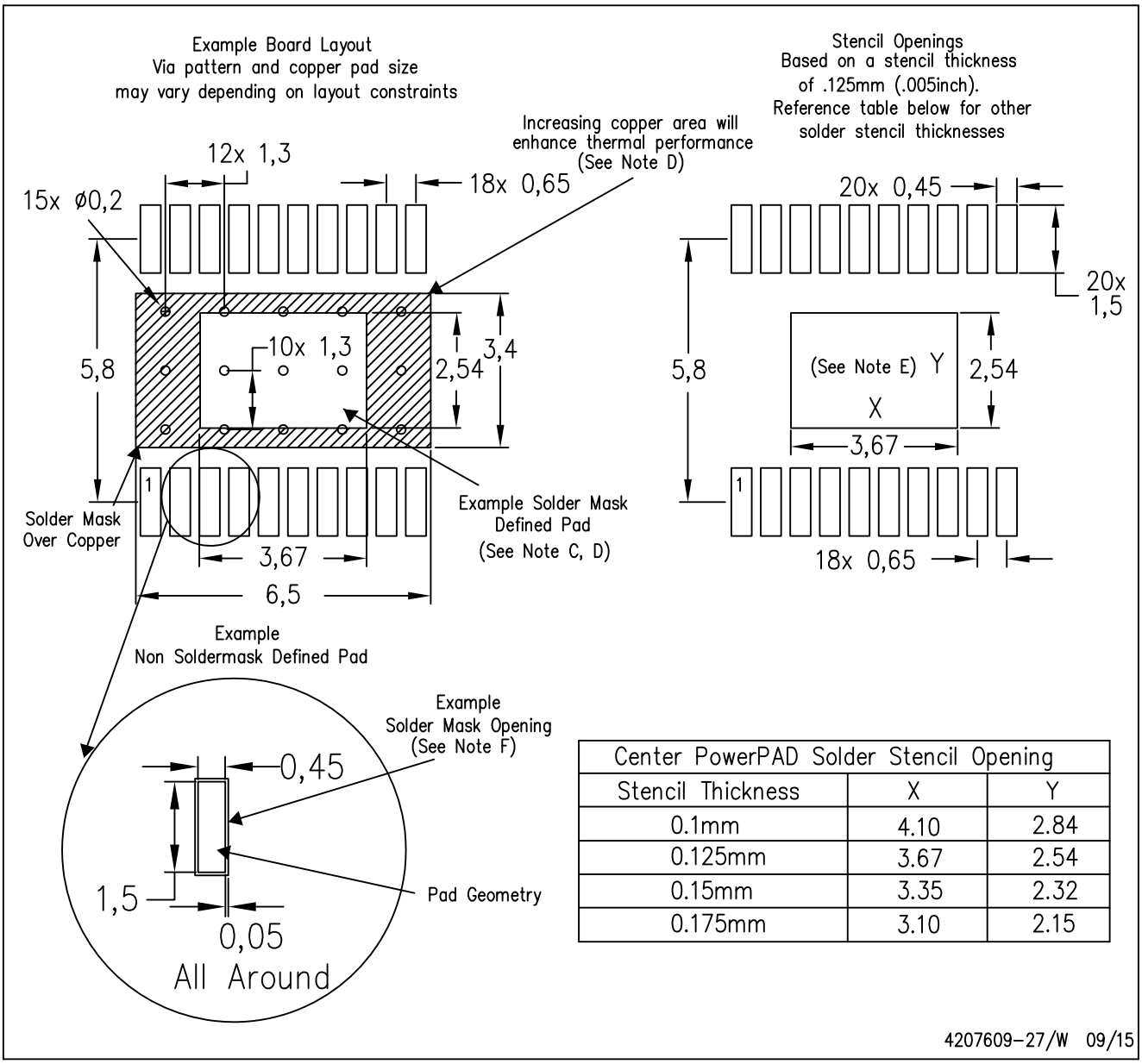
4206332–53/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.10	2.84
0.125mm	3.67	2.54
0.15mm	3.35	2.32
0.175mm	3.10	2.15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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