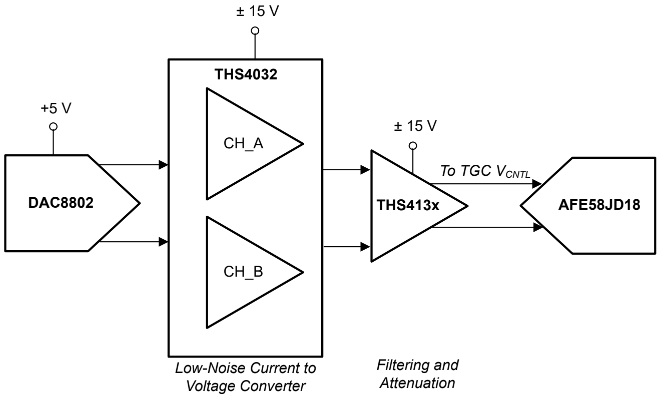
《THS413x 高速、低噪声、全差分 I/O 放大器》

1 特性

- 高级性能
  - 带宽：170MHz（V_{CC} = ±15V，G = 1V/V）
  - 压摆率：51 V/μs
  - 增益带宽积：215 MHz
  - 失真：–102dBc THD（$2V_{PP}$、250kHz 时）
- 电压噪声
  - 1/f 电压噪声拐角频率：350 Hz
  - 输入基准噪声 1.25nV/√Hz
- 单电源工作电压范围：5 V 至 30 V
- 静态电流（关断）：860μA (THS4130)

2 应用

- 单端至差分转换
- 差分 ADC 驱动器
- 差分抗混叠
- 差分发送器和接收器
- 输出电平转换器
- 医疗超声波



适用于超声波的时间增益控制 DAC 参考设计

3 说明

THS413x 器件属于全差分输入/差分输出器件系列，该系列器件使用德州仪器 (TI) 先进的高压互补双极工艺制造。

THS413x 由从输入到输出的真正全差分信号路径和高达 ±15V 的高电源电压构成。这种设计带来了出色的共模噪声抑制性能（800kHz 时为 95dB）和总谐波失真（$2V_{PP}$、250kHz 时为 −102dBc）。高电压差分信号链可通过宽电源电压范围提高裕量和动态范围，而无需为差分信号的每个极性添加单独的放大器。

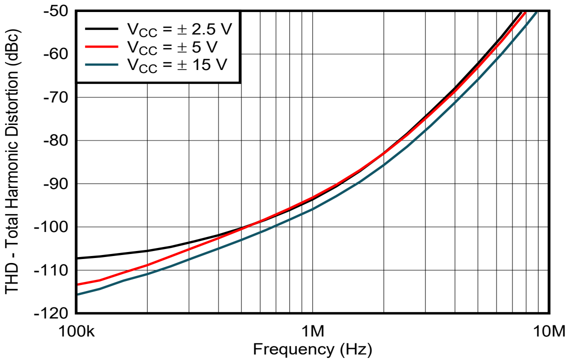
THS413x 具有 –40°C 至 +85°C 的宽额定运行温度范围。

器件信息(1)

器件型号	封装(2)	封装尺寸（标称值）
THS4130	SOIC (8)	4.90mm × 3.91mm
	MSOP (8)	3.00mm × 3.00mm
	MSOP-PowerPAD™ (8)	3.00mm × 3.00mm
THS4131	SOIC (8)	4.90mm × 3.91mm
	MSOP (8)	3.00mm × 3.00mm
	MSOP-PowerPAD (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 请参阅器件比较表。



V_{OUT} = $2V_{PP}$

总谐波失真与频率间的关系

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• Changed title of *Electrical Characteristics: THS413xD* to *Electrical Characteristics: THS413xD, THS413xDGK*	8
• Changed title of *Electrical Characteristics: THS413xDGK, THS413xDGN* table to *Electrical Characteristics: THS413xDGN*	10
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• Changed $R_{\theta JA}$ from 114.5°C/W to 126.3°C/W in *Thermal Information* table	8
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- Changed THD typical at V_{CC} = ±5 V, f = 250 kHz, V_O = $4V_{PP}$ from -91 dBc to -94 dBc *in Electrical Characteristics: THS413xD table* 8
- Changed THD typical at V_{CC} = ±5 V, f = 1 MHz, V_O = $4V_{PP}$ from -75 dBc to -79 dBc *in Electrical Characteristics: THS413xD table* 8
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- Changed SFDR typical at V_{CC} = ±2.5 V, V_O = 2 V_{PP} from 97 dB to 103 dB *in Electrical Characteristics: THS413xD table* 8
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- Added common-mode input resistance and differential input resistance specifications to *Electrical Characteristics: THS413xD* table 8
- Removed input capacitance, closed loop specification from *Electrical Characteristics: THS413xD* table 8
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- Changed minimum output current under V_{CC} = ±15 V, R_L = 7 Ω, T_A = full range, from 65 mA to 60 mA on *Electrical Characteristics: THS413xDGK, THS413xDGN* table........ 10
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- 添加了 *引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分........ 1

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- Changed footnote A in *Views of Thermally-Enhanced DGN Package* 32

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5 Device Comparison Tables

表 5-1. Available Device Packages

PACKAGED DEVICES			
T_A	SOIC (D)	MSOP PowerPAD™ (DGN)	MSOP (DGK)
0°C to +70°C	THS4130CD	THS4130CDGN	THS4130CDGK
	THS4131CD	THS4131CDGN	THS4131CDGK
−40°C to +85°C	THS4130ID	THS4130IDGN	THS4130IDGK
	THS4131ID	THS4131IDGN	THS4131IDGK

6 Pin Configuration and Functions

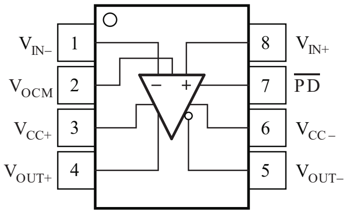


图 6-1. D, DGN, or DGK Package, 8-Pin SOIC, MSOP, or MSOP-PowerPAD THS4130 (Top View)

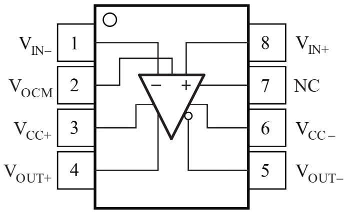


图 6-2. D, DGN, or DGK Package, 8-Pin SOIC, MSOP, or MSOP-PowerPAD THS4131 (Top View)

表 6-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	THS4130	THS4131		
NC	—	7	—	No connect
$\overline{PD}$	7	—	I	Active low power-down pin
V_{CC+}	3	3	I/O	Positive supply voltage pin
V_{CC-}	6	6	I/O	Negative supply voltage pin
V_{IN-}	1	1	I	Negative input pin
V_{OCM}	2	2	I	Common mode input pin
V_{OUT+}	4	4	O	Positive output pin
V_{OUT-}	5	5	O	Negative output pin
V_{IN+}	8	8	I	Positive input pin

(1) I = input, O = output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_I	Input voltage		$-V_{CC}$	$+V_{CC}$	V
V_{CC-} to V_{CC+}	Supply voltage			33	V
	Supply turn-on/off dV/dT[2]			1.7	V/µs
I_O [3]	Output current			150	mA
V_{ID}	Differential input voltage		-1.5	1.5	V
I_{IN}	Continuous Input Current			10	mA
T_J [4]	Maximum junction temperature			150	°C
T_J [5]	Maximum junction temperature, continuous operation, long-term reliability			125	°C
T_A	Operating free-air temperature	C-suffix	0	70	°C
		I-suffix	–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Staying below this specification ensures that the edge-triggered ESD absorption devices across the supply pins remain off.
(3) The THS413xmay incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about using the PowerPAD thermally-enhanced package.
(4) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(5) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

7.2 ESD Ratings

			VALUE	UNIT
THS4130: D, DGN, OR DGK PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1500	
THS4131: D, DGN, OR DGK PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{cc+} to V_{cc-}	Dual supply	±2.5		±15	V
	Single supply	5		30	
T_A	C-suffix	0		70	°C
	I-suffix	–40		85	

7.4 Thermal Information

THERMAL METRIC[1]		THS413x			UNIT
		D (SOIC)	DGN (MSOP-PowerPAD)	DGK (MSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.3	55.8	147.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.3	61.6	37.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.8	34.5	83.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.5	13.8	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.0	34.4	81.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	8.4	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics: THS413xD, THS413xDGK

V_{CC}= ±5 V, Gain = 1 V/V, R_F = 390 Ω, R_L = 800 Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3 dB), single-ended input, differential output, V_I = 63 mV_{PP}	V_{CC} = 5 V	Gain = 1, R_F = 390 Ω		165		MHz
		V_{CC} = ±5 V			166		
		V_{CC} = ±15 V			170		
		V_{CC} = 5 V	Gain = 2, R_F = 750 Ω		97		
		V_{CC} = ±5 V			98		
		V_{CC} = ±15 V			100		
SR	Slew rate[2]				67		V/µs
t_s	Settling time to 0.1%	Step voltage = 2 V			39		ns
	Settling time to 0.01%				61		
DISTORTION PERFORMANCE							
THD	Total harmonic distortion, differential input, differential output, V_O = 2 V_{PP}	V_{CC} = 5 V	f = 250 kHz		–101		dBc
			f = 1 MHz		–87		
		V_{CC} = ±5 V	f = 250 kHz		–100		
			f = 1 MHz		–87		
		V_{CC} = ±15 V	f = 250 kHz		–102		
			f = 1 MHz		–88		
	V_O = 4 V_{PP}	V_{CC} = ±5 V	f = 250 kHz		–94		
			f = 1 MHz		–79		
		V_{CC} = ±15 V	f = 250 kHz		–95		
			f = 1 MHz		–80		
SFDR	Spurious-free dynamic range, differential input, differential output, f = 250 kHz	V_O= 2 V_{PP}	V_{CC} = ±2.5		103		dBc
			V_{CC} = ±5		106		
			V_{CC} = ±15		108		
		V_O = 4 V_{PP}	V_{CC} = ±5		98		
			V_{CC} = ±15		100		
IMD3	Third intermodulation distortion	$V_{I(PP)}$ = 4 V, F_1 = 3 MHz, F_2 = 3.5 MHz			–53		dBc
OIP3	Third-order intercept				41.5		dB
NOISE PERFORMANCE							
V_n	Input voltage noise	f = 10 kHz			1.25		nV/√Hz

7.5 Electrical Characteristics: THS413xD, THS413xDGK (continued)

V_{CC}= ±5 V, Gain = 1 V/V, R_F = 390 Ω, R_L = 800 Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_n	Input current noise	f = 10 kHz			1.7		pA/√Hz
DC PERFORMANCE							
	Open-loop gain	T_A = +25°C		71	78		dB
		T_A = full range		69			
V_{OS}	Input offset voltage	T_A = +25°C			±0.2	2	mV
		T_A = full range(1)				3	
	Common-mode input offset voltage, referred to V_{OCM}				0.2	5.5	mV
	Input offset voltage drift	T_A = full range(1)			2		µV/°C
I_{IB}	Input bias current	T_A = full range(1)			5	15.4	µA
I_{OS}	Input offset current	T_A = full range(1)			100	500	nA
	Input offset current drift				1		nA/°C
INPUT CHARACTERISTICS							
CMRR	Common-mode rejection ratio	T_A = full range(1)		80	95		dB
V_{ICR}	Common-mode input voltage range			–3.77 to 4.3	–4 to 4.5		V
R_{I_CM}	Common-mode input resistance	Measured into each input terminal			215		MΩ
R_{I_DIFF}	Differential input resistance				10		kΩ
C_{I_CM}	Common-mode input capacitance, closed loop	Measured into each input terminal			1.4		pF
C_{I_DIFF}	Differential input capacitance, closed loop				2.5		
OUTPUT CHARACTERISTICS							
r_o	Output resistance	Open loop			41		Ω
	Output voltage swing	V_{CC} = 5 V, R_L = 1kΩ	T_A = +25°C	1.2 to 3.8	0.9 to 4.1		V
			T_A = full range(1)	1.3 to 3.7	±4		
		V_{CC} = ±5 V, R_L = 1kΩ	T_A = +25°C	±3.7			
			T_A = full range(1)	±3.6			
		V_{CC} = ±15 V, R_L = 1kΩ	T_A = +25°C	±11.5	±12.4		
			T_A = full range(1)	±11.2			
I_O	Output current	V_{CC} = 5 V, R_L = 7 Ω	T_A = +25°C	25	45		mA
			T_A = full range	20			
		V_{CC} = ±5 V, R_L = 7 Ω	T_A = +25°C	30	55		
			T_A = full range(1)	28			
		V_{CC} = ±15 V, R_L = 7 Ω	T_A = +25°C	65	85		
			T_A = full range(1)	60			
POWER SUPPLY							
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = +25°C		10.4	15	mA
			T_A = full range(1)			16	
		V_{CC} = ±15 V	T_A = +25°C		13		
$I_{CC(SD)}$	Quiescent current (shutdown) (THS4130 only)(3)	$\overline{PD}$ = –5 V	T_A = +25°C		0.86	1.4	mA
			T_A = full range(1)			1.5	
PSRR	Power-supply rejection ratio (dc)		T_A = +25°C	73	98		dB
			T_A = full range(1)	70			

(1) The full range temperature is 0°C to +70°C for the C-suffix, and –40°C to +85°C for the I-suffix.

(2) Slew rate is measured from an output level range of 25% to 75%.
(3) For detailed information on the behavior of the power-down circuit, see the Power-Down Mode section.

7.6 Electrical Characteristics: THS413xDGN

V_{CC}= ±5 V, R_L = 800Ω, and T_A = +25°C, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (– 3 dB), single-ended input, differential output, V_I = 63 mV_{PP}	V_{CC} = 5	Gain = 1, R_f = 390 Ω		125		MHz
		V_{CC} = ±5	Gain = 1, R_f = 390 Ω		135		
		V_{CC} = ±15	Gain = 1, R_f = 390 Ω		150		
	Small-signal bandwidth (– 3 dB), single-ended input, differential output, V_I = 63 mV_{PP}	V_{CC} = 5	Gain = 2, R_f = 750 Ω		80		
		V_{CC} = ±5	Gain = 2, R_f = 750 Ω		85		
		V_{CC} = ±15	Gain = 2, R_f = 750 Ω		90		
SR	Slew rate(2)	Gain = 1			52		V/µs
t_s	Settling time to 0.1%	Step voltage = 2 V, gain = 1			78		ns
	Settling time to 0.01%	Step voltage = 2 V, gain = 1			213		
DISTORTION PERFORMANCE							
THD	Total harmonic distortion, differential input, differential output, gain = 1, R_f = 390 Ω, R_L = 800 Ω, V_O= 2 V_{PP}	V_{CC} = 5	f = 250 kHz		–95		dBc
			f = 1 MHz		–81		
		V_{CC} = ±5	f = 250 kHz		–96		
			f = 1 MHz		–80		
		V_{CC} = ±15	f = 250 kHz		–97		
			f = 1 MHz		–80		
	V_O = 4 V_{PP}	V_{CC} = ±5	f = 250 kHz		–91		
			f = 1 MHz		–75		
		V_{CC} = ±15	f = 250 kHz		–91		
			f = 1 MHz		–75		
SFDR	Spurious-free dynamic range, differential input, differential output, gain = 1, R_f = 390 Ω, R_L = 800 Ω, f = 250 kHz	V_O= 2 V_{PP}	V_{CC} = ±2.5		97		dB
			V_{CC} = ±5		98		
			V_{CC} = ±15		99		
		V_O = 4 V_{PP}	V_{CC} = ±5		93		
			V_{CC} = ±15		95		
Third intermodulation distortion		$V_{I(PP)}$ = 4 V, G = 1, F1 = 3 MHz, F2 = 3.5 MHz			–53		dBc
Third-order intercept		$V_{I(PP)}$ = 4 V, G = 1, F1 = 3 MHz, F2 = 3.5 MHz			41.5		dB
NOISE PERFORMANCE							
V_n	Input voltage noise	f = 10 kHz			1.3		nV/√Hz
I_n	Input current noise	f = 10 kHz			1		pA/√Hz
DC PERFORMANCE							
	Open-loop gain	T_A = +25°C		71	78		dB
		T_A = full range		69			
$V_{(OS)}$	Input offset voltage	T_A = +25°C			0.2	2	mV
		T_A = full range				3	
	Common-mode input offset voltage, referred to V_{OCM}	T_A = +25°C			0.2	3.5	
	Input offset voltage drift	T_A = full range			4.5		µV/°C
I_{IB}	Input bias current	T_A = full range			2	6	µA

7.6 Electrical Characteristics: THS413xDGN (continued)

V_{CC}= ±5 V, R_L = 800Ω, and T_A = +25°C, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OS}	Input offset current	T_A = full range			100	500	nA
	Offset drift				2		nA/°C
INPUT CHARACTERISTICS							
CMRR	Common-mode rejection ratio	T_A = full range		80	95		dB
V_{ICR}	Common-mode input voltage range			–3.77 to 4.3	–4 to 4.5		V
R_I	Input resistance	Measured into each input terminal			34		MΩ
C_I	Input capacitance, closed loop				4		pF
r_o	Output resistance	Open loop			41		Ω
OUTPUT CHARACTERISTICS							
	Output voltage swing	V_{CC} = 5 V	T_A = +25°C	1.2 to 3.8	0.9 to 4.1		V
			T_A = full range	1.3 to 3.7	±4		
		V_{CC} = ±5 V	T_A = +25°C	±3.7			
			T_A = full range	±3.6			
		V_{CC} = ±15 V	T_A = +25°C	±10.5	±12.4		
			T_A = full range	±10.2			
I_O	Output current	V_{CC} = 5 V, R_L = 7 Ω	T_A = +25°C	25	45		mA
			T_A = full range	20			
		V_{CC} = ±5 V, R_L = 7 Ω	T_A = +25°C	30	55		
			T_A = full range	28			
		V_{CC} = ±15 V, R_L = 7 Ω	T_A = +25°C	65	85		
			T_A = full range	60			
POWER SUPPLY							
V_{CC}	Supply voltage range	Single supply		5		30	V
		Split supply		±2.5		±15	
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = +25°C		12.3	15	mA
			T_A = full range			16	
		V_{CC} = ±15 V	T_A = +25°C		14		
$I_{CC(SD)}$	Quiescent current (shutdown) (THS4130 only)(3)	V = –5 V	T_A = +25°C		0.86	1.4	mA
			T_A = full range			1.5	
PSRR	Power-supply rejection ratio (dc)		T_A = +25°C	73	98		dB
			T_A = full range	70			

(1) The full range temperature is 0°C to +70°C for the C-suffix, and –40°C to +85°C for the I-suffix.
(2) Slew rate is measured from an output level range of 25% to 75%.
(3) For detailed information on the behavior of the power-down circuit, see the *Power-Down Mode* section.

7.7 Typical Characteristics: THS413xD, THS413xDGK

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, G = +1 V/V, differential input, differential output and R_L = 800 Ω (unless otherwise noted)

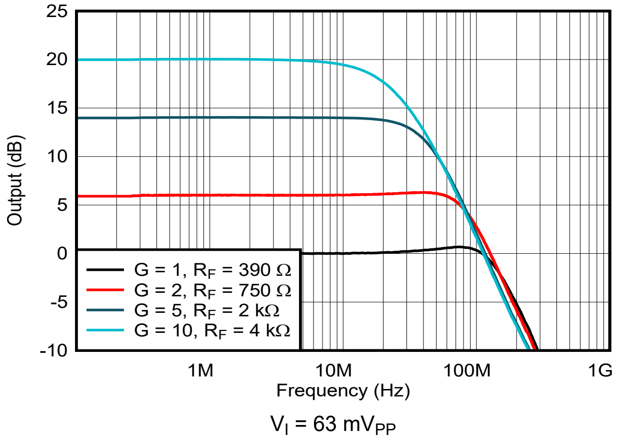


图 7-1. Small-Signal Frequency Response

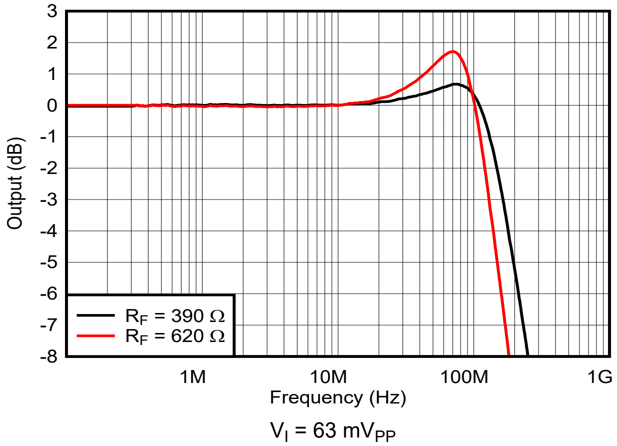


图 7-2. Small-Signal Frequency Response

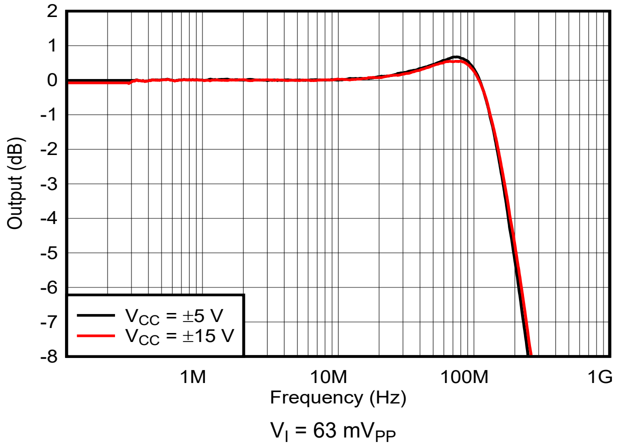


图 7-3. Small-Signal Frequency Response

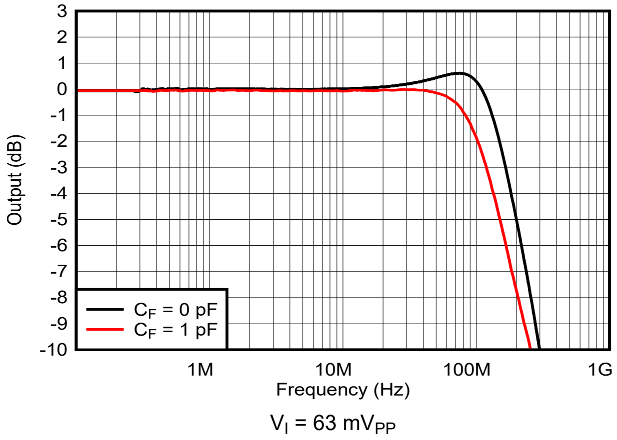


图 7-4. Small-Signal Frequency Response

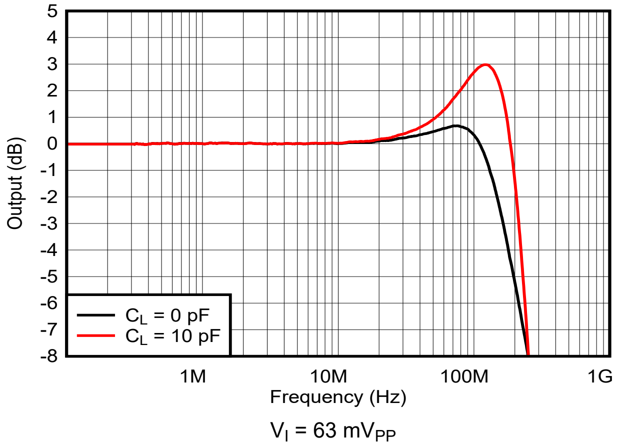


图 7-5. Small-Signal Frequency Response

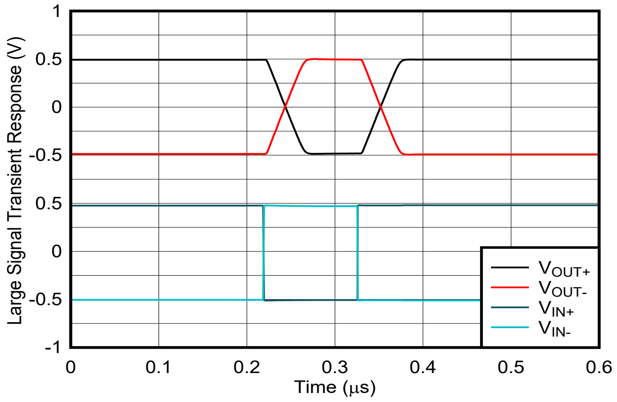


图 7-6. Large-Signal Transient Response (Differential In/Single Out)

7.7 Typical Characteristics: THS413xD, THS413xDGK (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, G = +1 V/V, differential input, differential output and R_L = 800 Ω (unless otherwise noted)

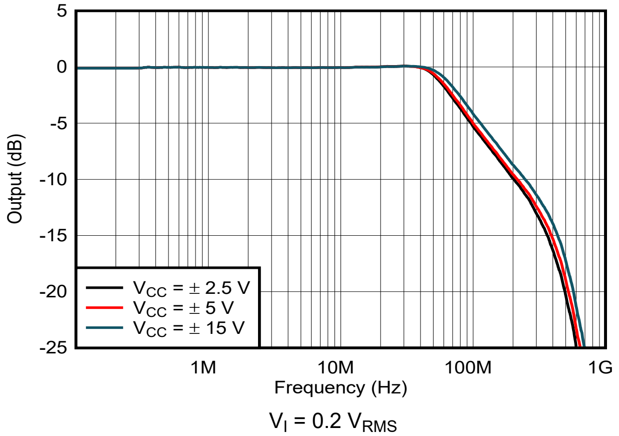


图 7-7. Large-Signal Frequency Response

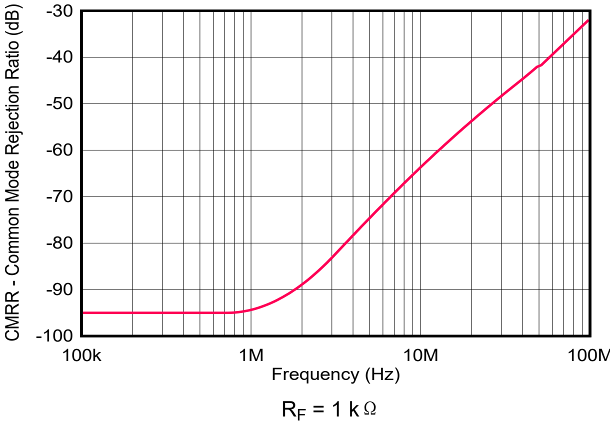


图 7-8. Common-Mode Rejection Ratio vs Frequency

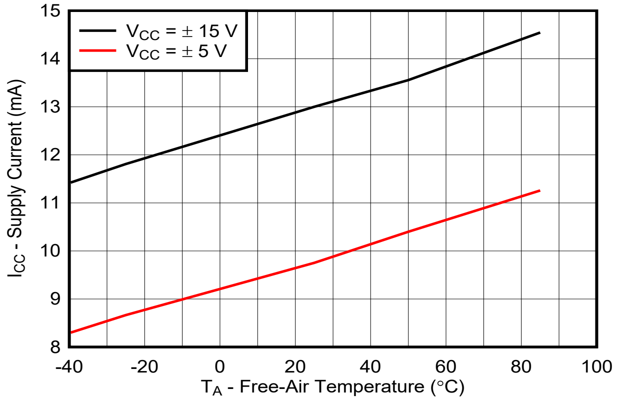


图 7-9. Supply Current vs Free-Air Temperature

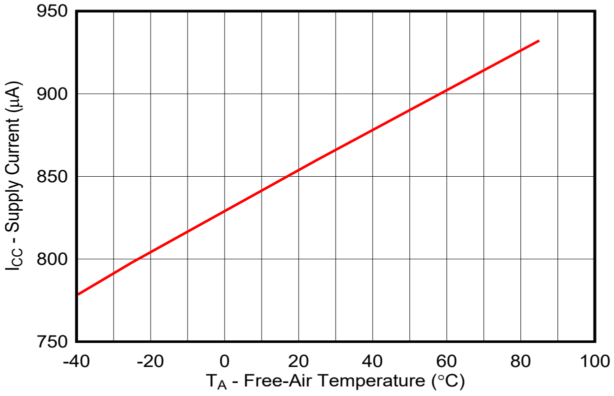


图 7-10. Supply Current vs Free-Air Temperature (Shutdown State)

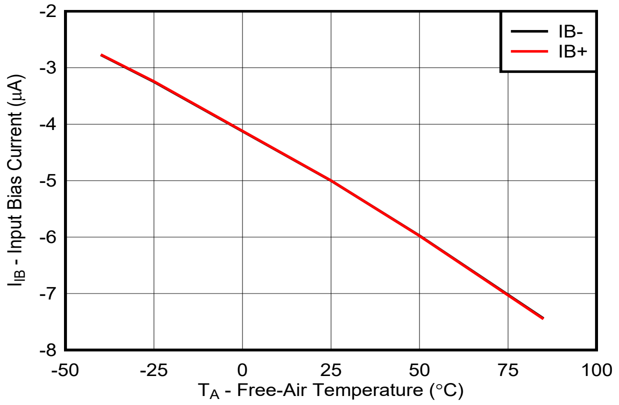


图 7-11. Input Bias Current vs Free-Air Temperature

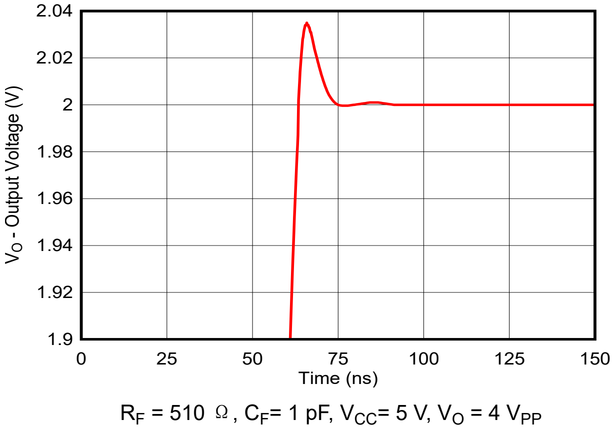
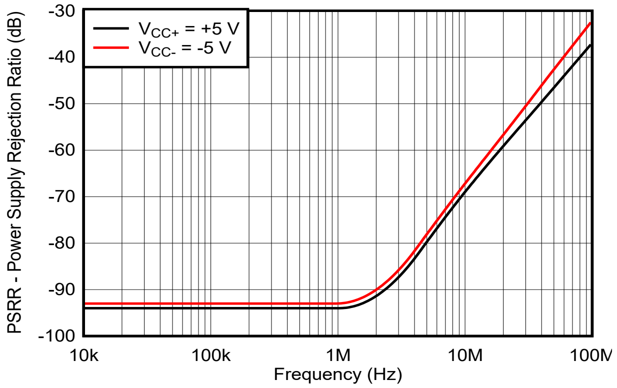


图 7-12. Settling Time

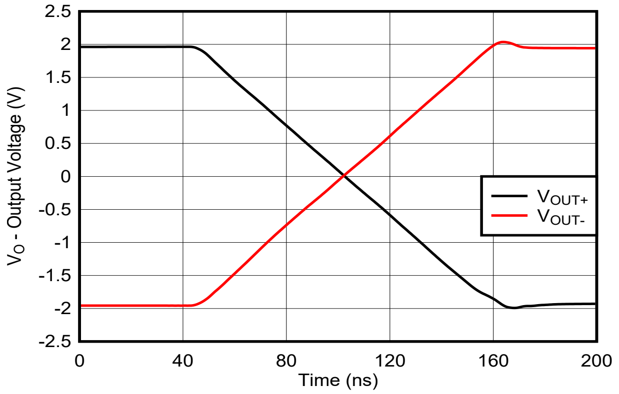
7.7 Typical Characteristics: THS413xD, THS413xDGK (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, G = +1 V/V, differential input, differential output and R_L = 800 Ω (unless otherwise noted)



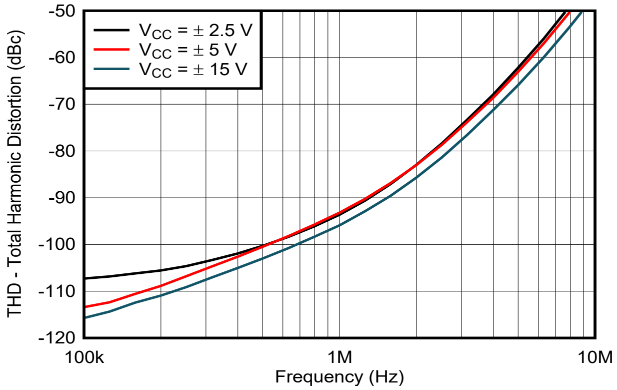
R_F = 330 Ω, R_L = 400 Ω

图 7-13. Power-Supply Rejection Ratio vs Frequency (Differential Out)



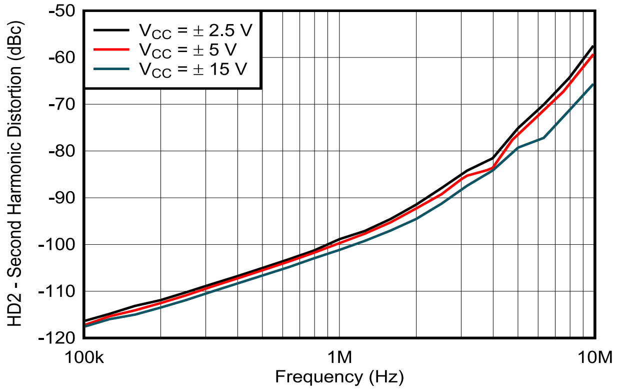
V_{I_Peak} = 2 V, C_L = 10 pF, V_{CC} = ±15 V

图 7-14. Large-Signal Transient Response



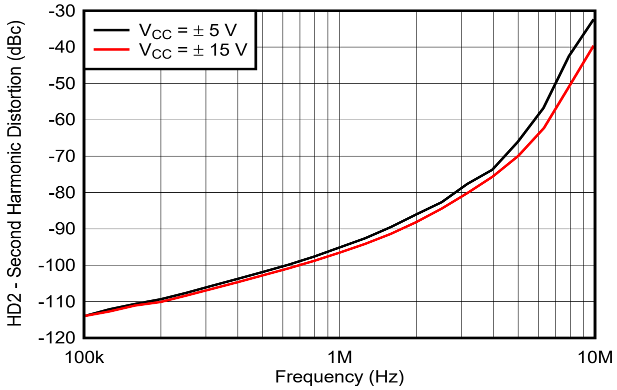
V_{OUT} = 2 V_{PP}

图 7-15. Total Harmonic Distortion vs Frequency



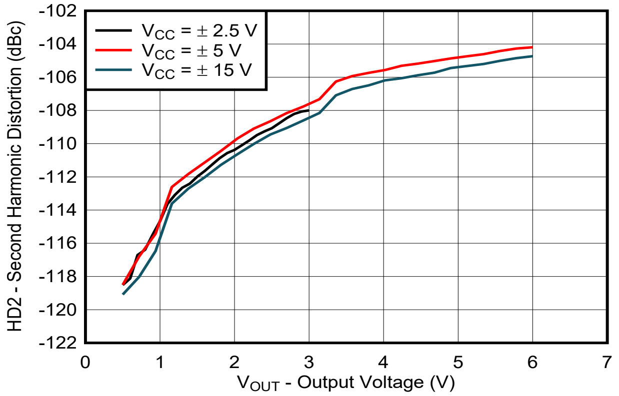
V_{OUT} = 2 V_{PP}, Single-ended Input, Differential Output

图 7-16. Second-Harmonic Distortion vs Frequency



V_{OUT} = 4 V_{PP}, Single-ended Input, Differential Output

图 7-17. Second-Harmonic Distortion vs Frequency

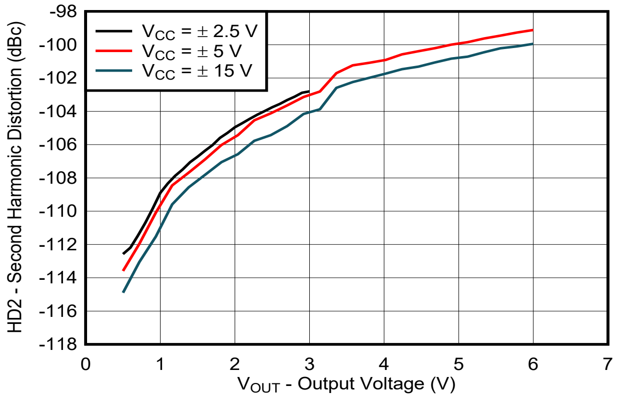


f = 250 kHz, Single-ended Input, Differential Output

图 7-18. Second-Harmonic Distortion vs Output Voltage

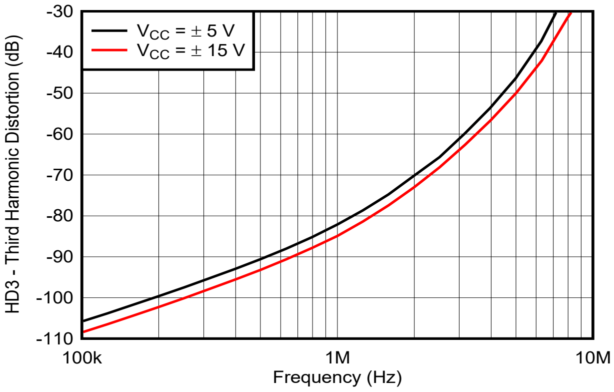
7.7 Typical Characteristics: THS413xD, THS413xDGK (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, G = +1 V/V, differential input, differential output and R_L = 800 Ω (unless otherwise noted)



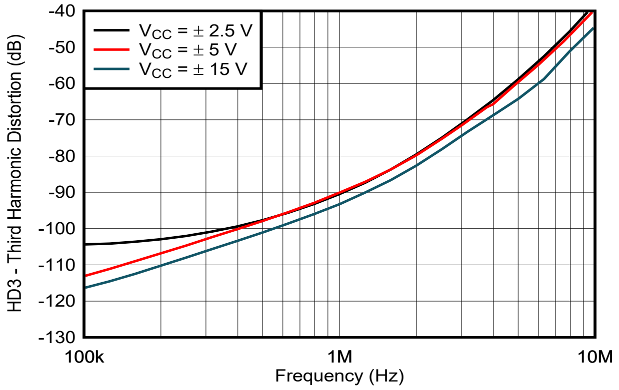
f = 500 kHz, Single-ended Input, Differential Output

图 7-19. Second-Harmonic Distortion vs Output Voltage



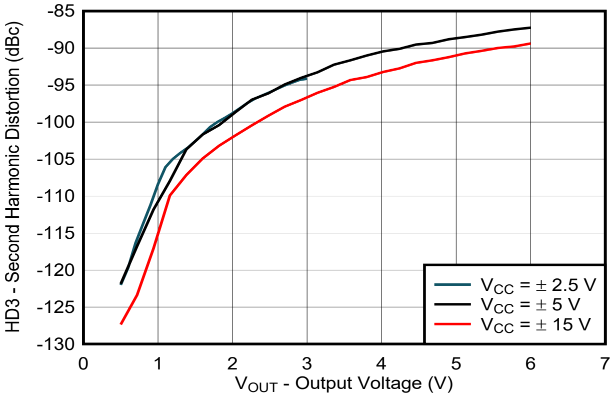
V_{OUT} = 4 V_{PP}, Single-ended Input, Differential Output

图 7-20. Third-Harmonic Distortion vs Frequency



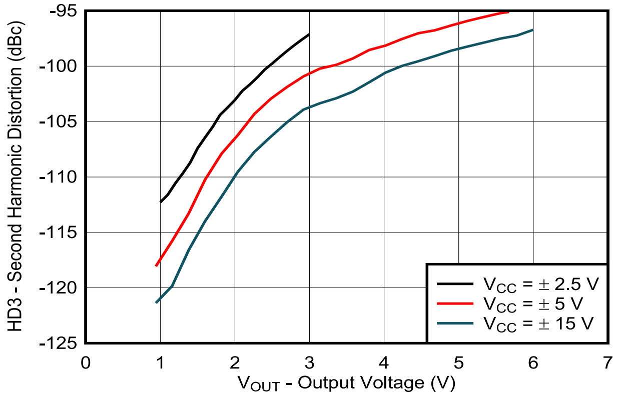
V_{OUT} = 2 V_{PP}, Single-ended Input, Differential Output

图 7-21. Third-Harmonic Distortion vs Frequency



f = 500 kHz, Single-ended Input, Differential Output

图 7-22. Third-Harmonic Distortion vs Output Voltage



f = 250 kHz, Single-ended Input, Differential Output

图 7-23. Third-Harmonic Distortion vs Output Voltage

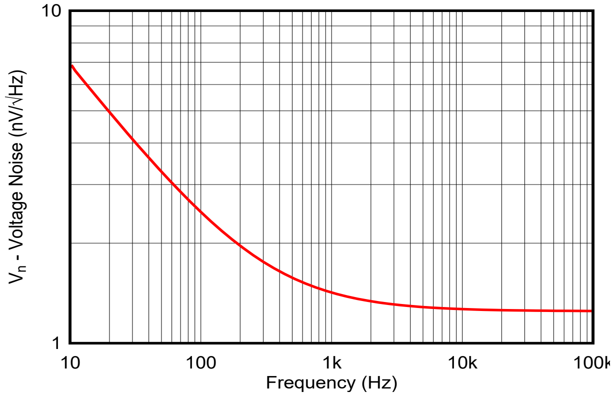


图 7-24. Voltage Noise vs Frequency

7.7 Typical Characteristics: THS413xD, THS413xDGK (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, G = +1 V/V, differential input, differential output and R_L = 800 Ω (unless otherwise noted)

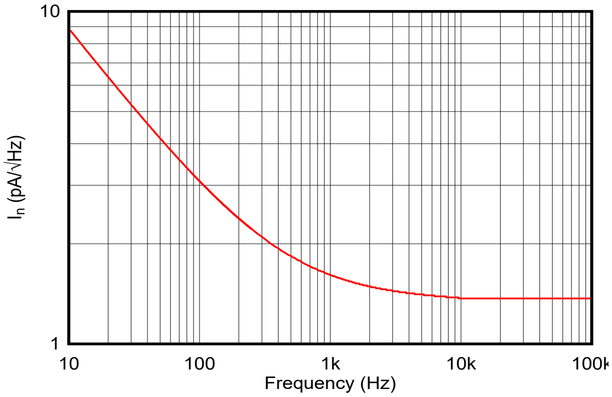
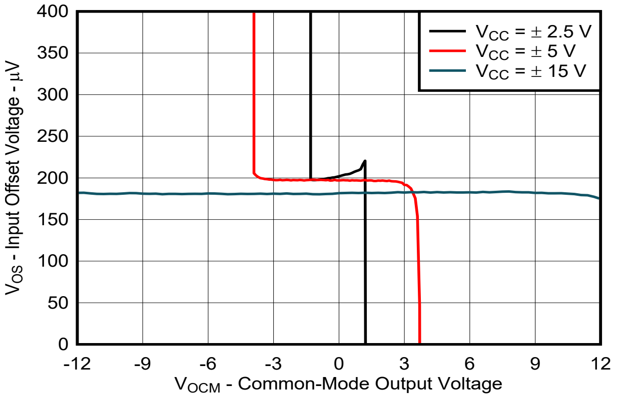
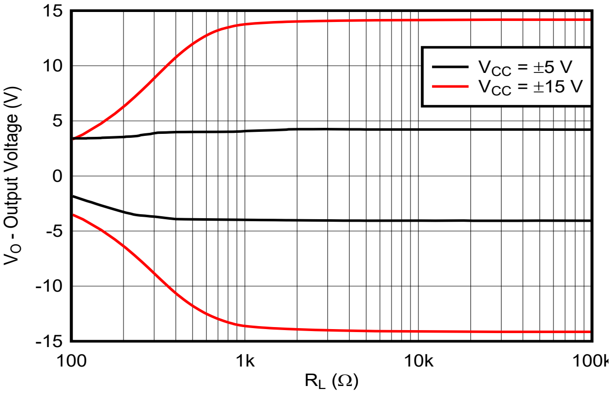


图 7-25. Current Noise vs Frequency



R_F = 1 kΩ

图 7-26. Input Offset Voltage vs Common-Mode Output Voltage



R_F = 1 kΩ, G = 2 V/V

图 7-27. Output Voltage vs Differential Load Resistance

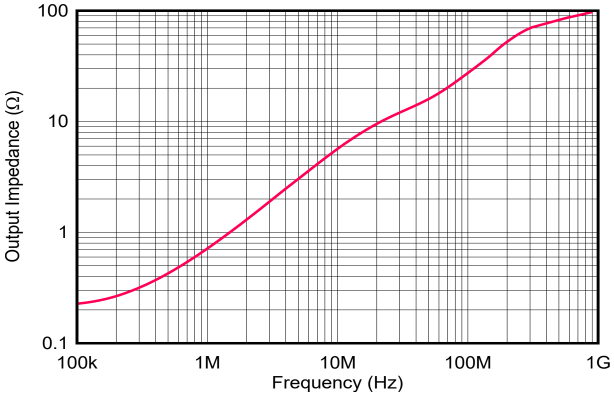


图 7-28. Output Impedance vs Frequency

7.8 Typical Characteristics: THS413xDGN

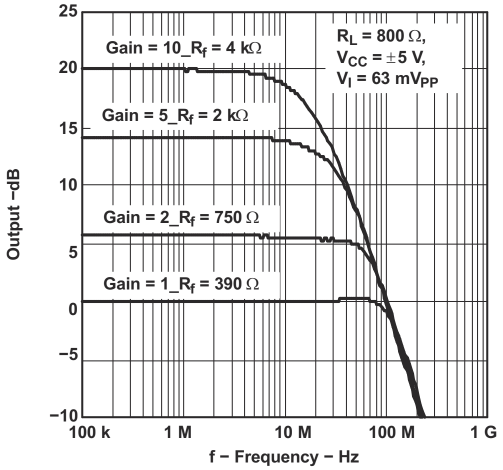


图 7-29. Small-Signal Frequency Response

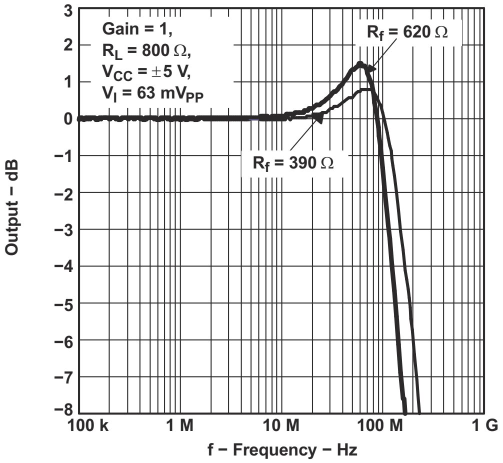


图 7-30. Small-Signal Frequency Response

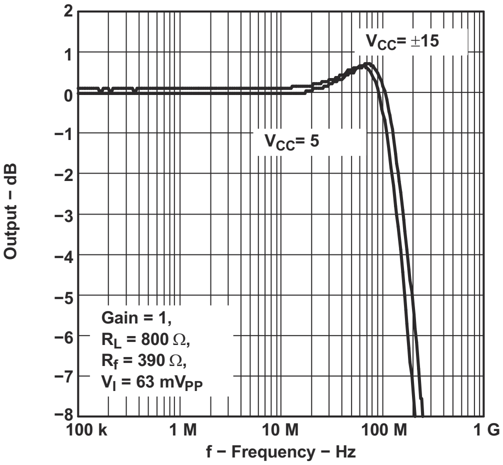


图 7-31. Small-Signal Frequency Response (Various Supplies)

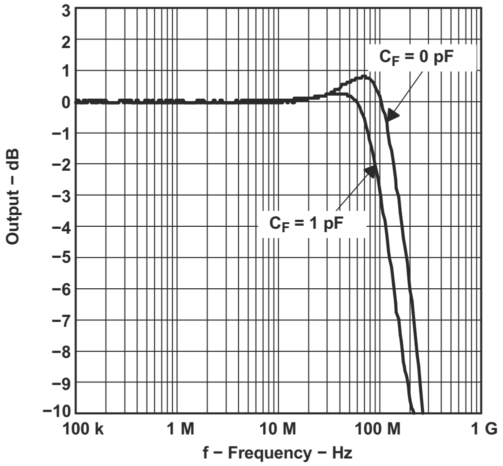


图 7-32. Small-Signal Frequency Response (Various C_F)

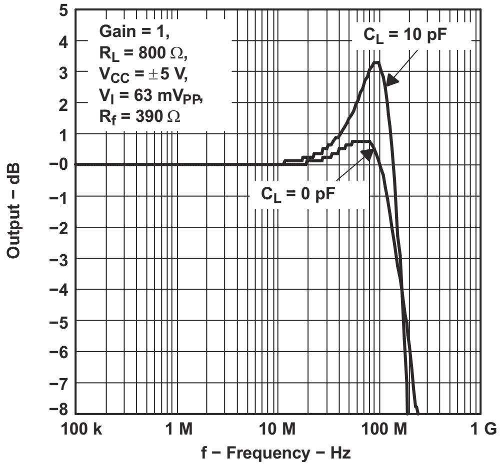


图 7-33. Small-Signal Frequency Response (Various C_L)

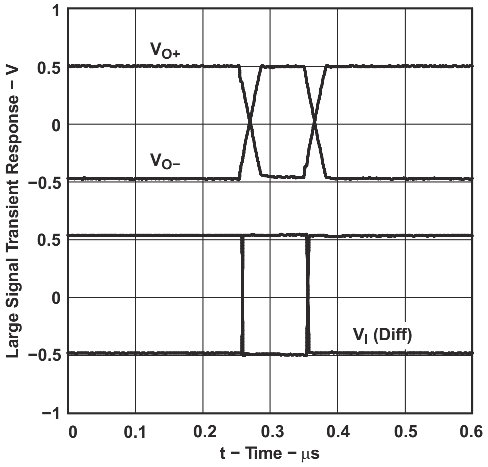


图 7-34. Large-Signal Transient Response (Differential In/Single Out)

7.8 Typical Characteristics: THS413xDGN (continued)

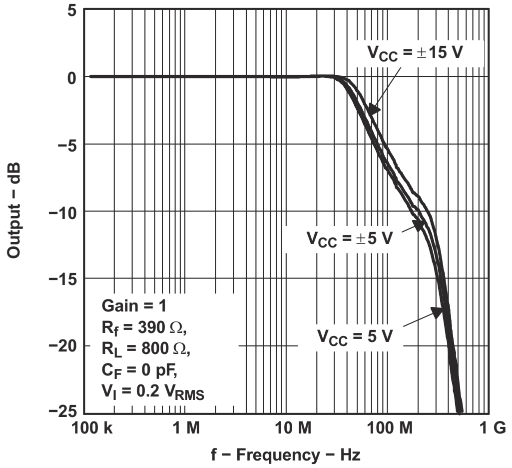


图 7-35. Large-Signal Frequency Response

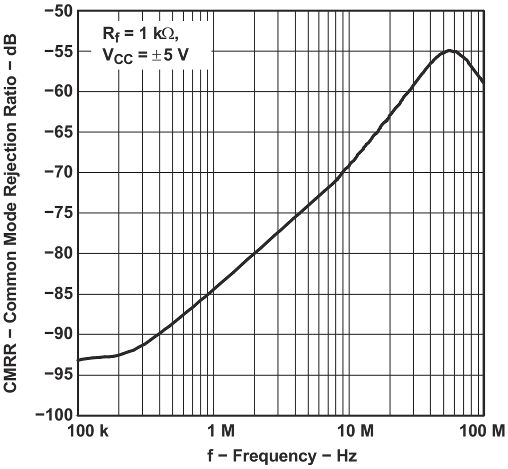


图 7-36. Common-Mode Rejection Ratio vs Frequency

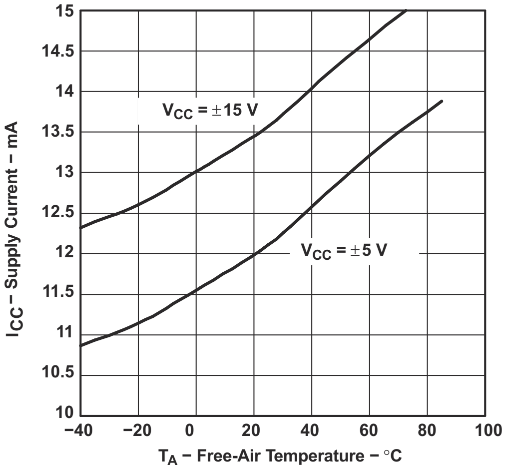


图 7-37. Supply Current vs Free-Air Temperature

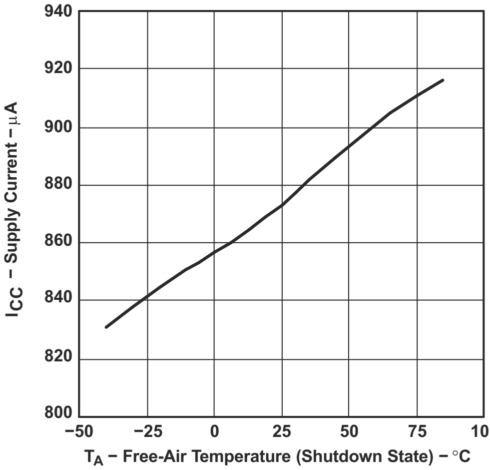


图 7-38. Supply Current vs Free-Air Temperature (Shutdown State)

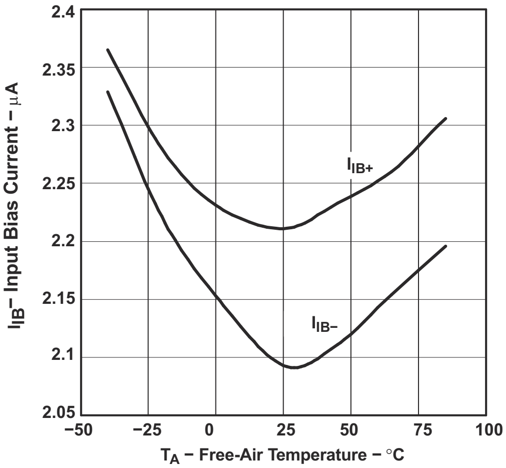


图 7-39. Input Bias Current vs Free-Air Temperature

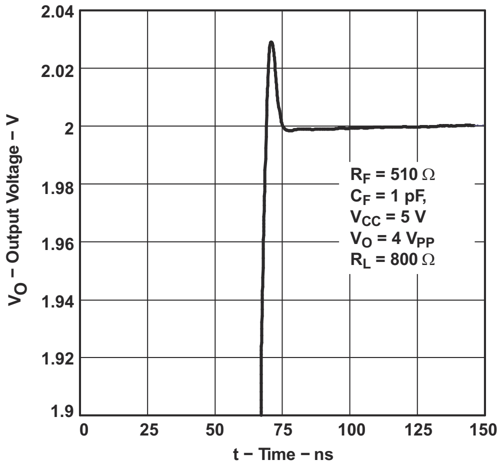


图 7-40. Settling Time

7.8 Typical Characteristics: THS413xDGN (continued)

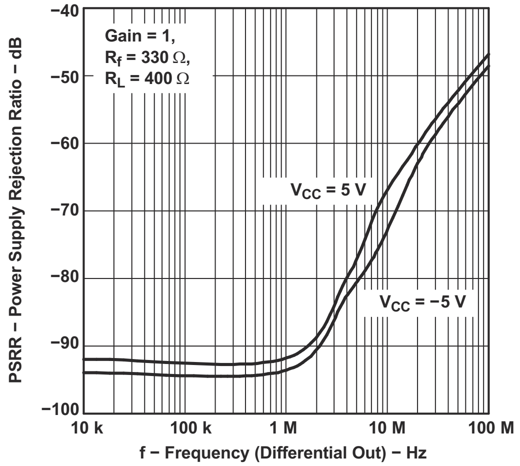


图 7-41. Power-Supply Rejection Ratio vs Frequency (Differential Out)

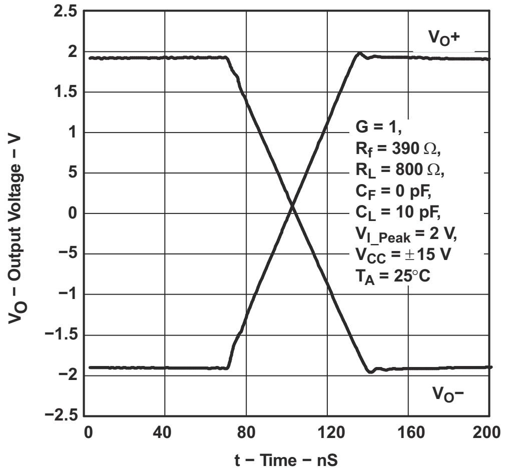


图 7-42. Large-Signal Transient Response

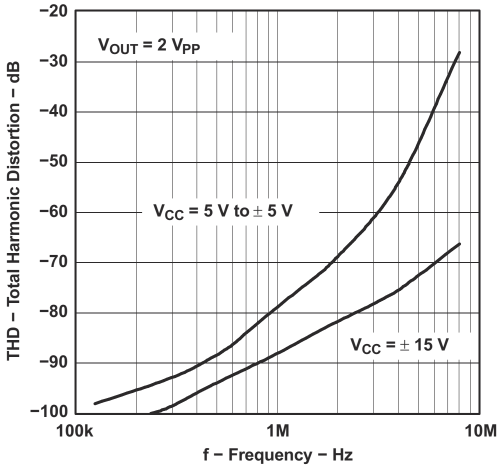


图 7-43. Total Harmonic Distortion vs Frequency

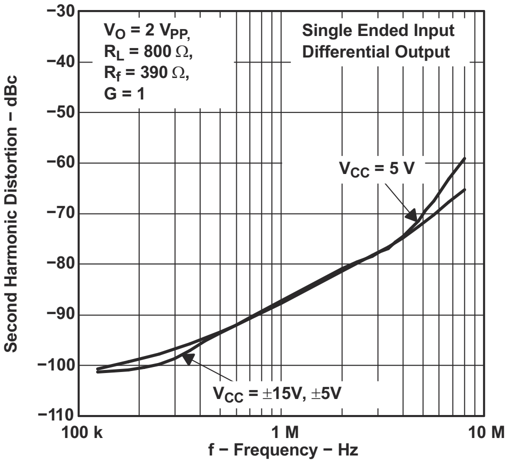


图 7-44. Second-Harmonic Distortion vs Frequency

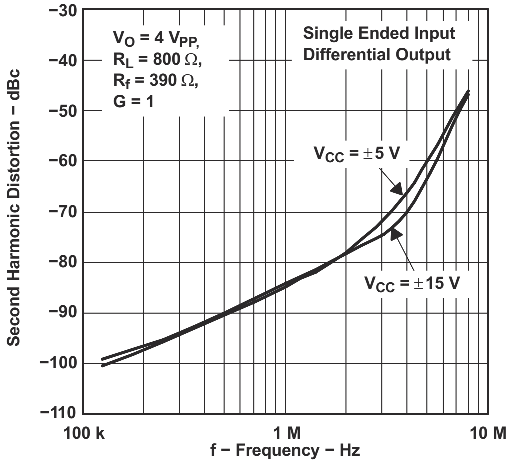


图 7-45. Second-Harmonic Distortion vs Frequency

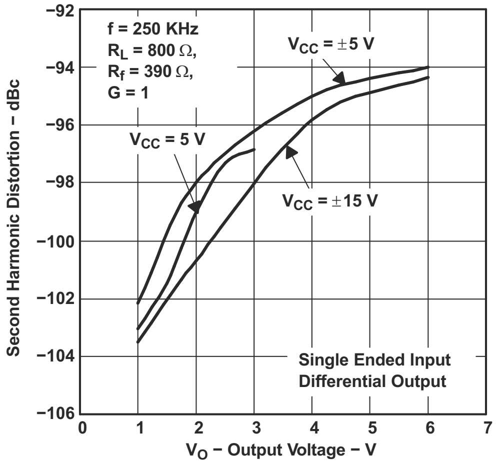


图 7-46. Second-Harmonic Distortion vs Output Voltage

7.8 Typical Characteristics: THS413xDGN (continued)

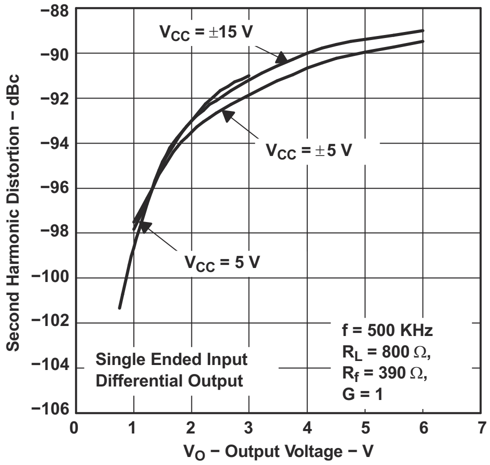


图 7-47. Second-Harmonic Distortion vs Output Voltage

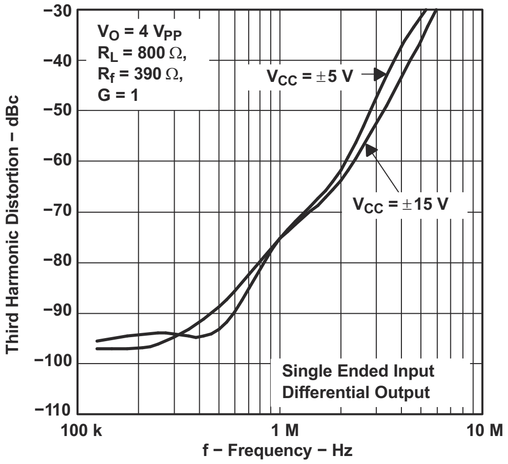


图 7-48. Third-Harmonic Distortion vs Frequency

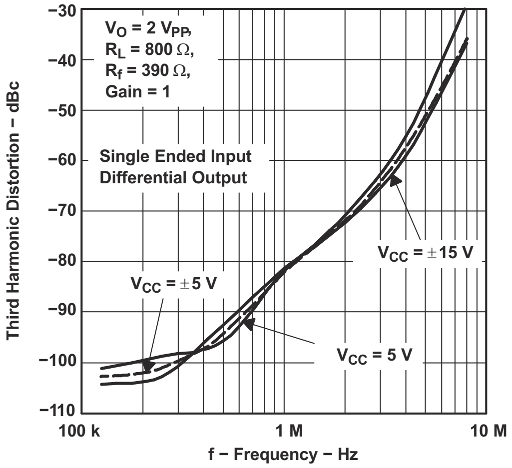


图 7-49. Third-Harmonic Distortion vs Frequency

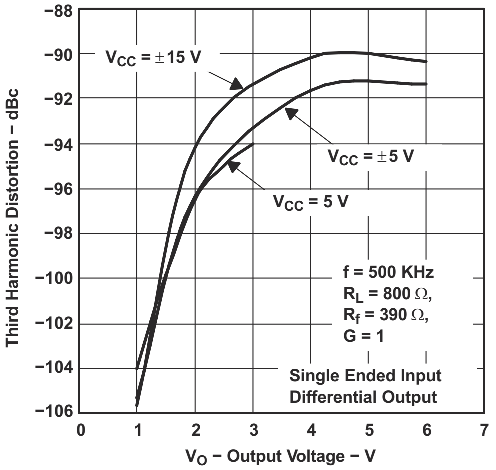


图 7-50. Third-Harmonic Distortion vs Output Voltage

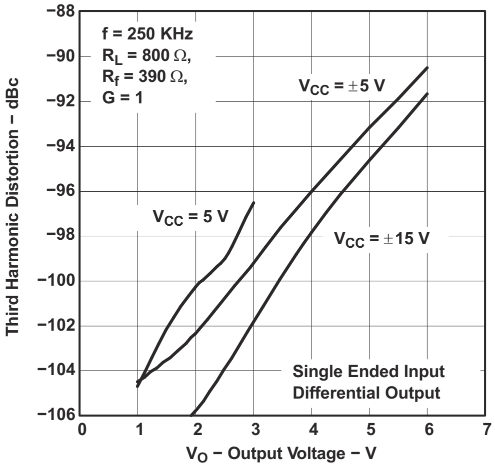


图 7-51. Third-Harmonic Distortion vs Output Voltage

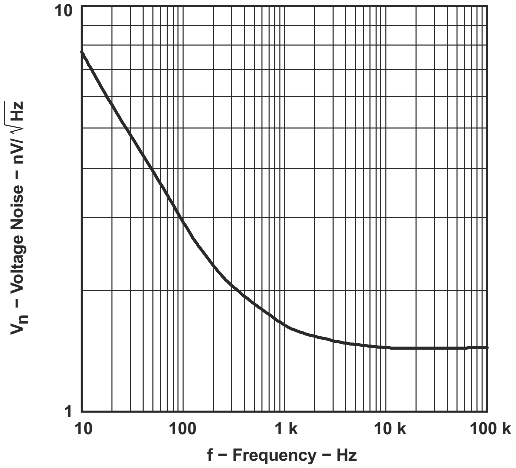


图 7-52. Voltage Noise vs Frequency

7.8 Typical Characteristics: THS413xDGN (continued)

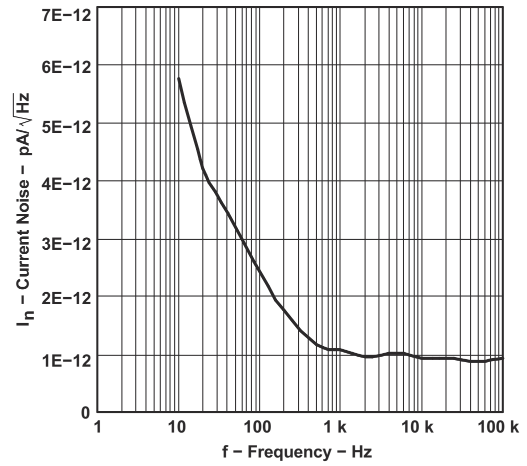


图 7-53. Current Noise vs Frequency

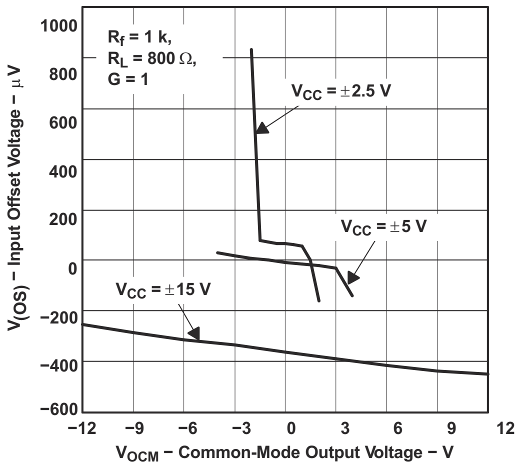


图 7-54. Input Offset Voltage vs Common-Mode Output Voltage

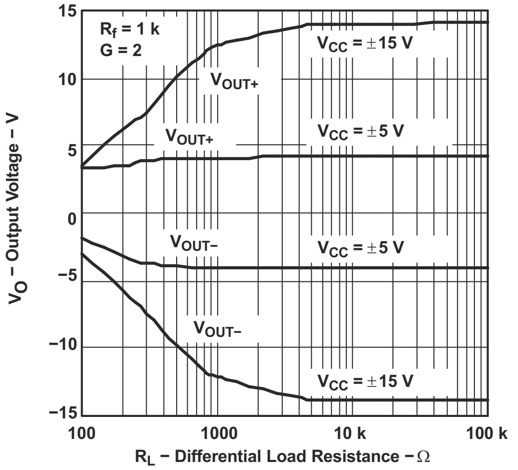


图 7-55. Output Voltage vs Differential Load Resistance

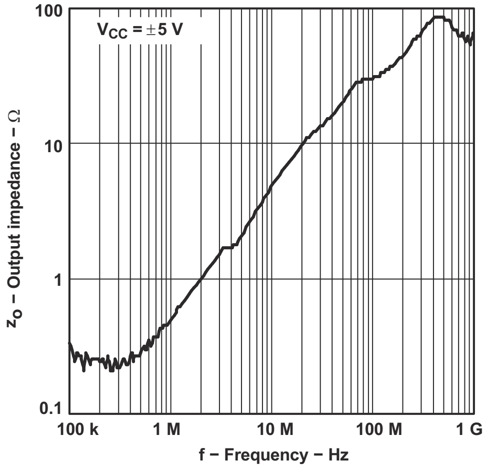


图 7-56. Output Impedance vs Frequency

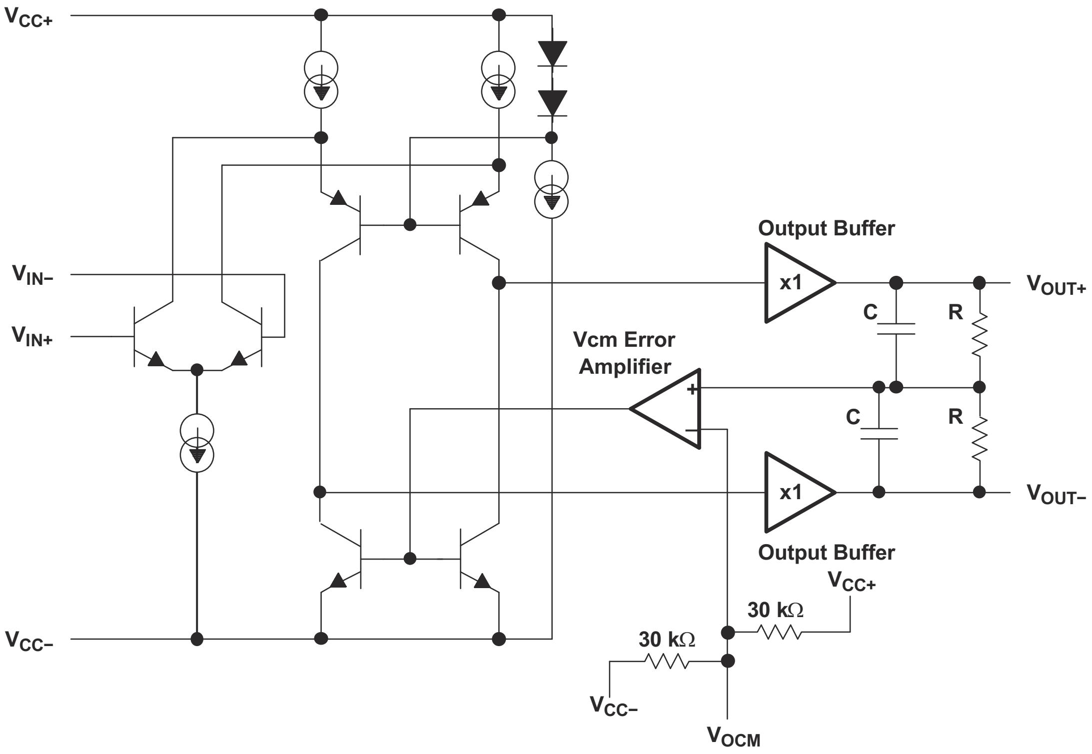
8 Detailed Description

8.1 Overview

8.1.1 Fully-Differential Amplifiers

The THS413x is a fully differential amplifier (FDA). Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order non-linearities, and increased dynamic range. FDAs not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing. For more information on the basic theory of operation for FDAs, refer to the *Fully Differential Amplifiers* application note.

8.2 Functional Block Diagram



8.3 Feature Description

图 8-1 and 图 8-2 depict the differences between the operation of the THS413x in two different modes. FDAs can work with either differential or single-ended inputs.

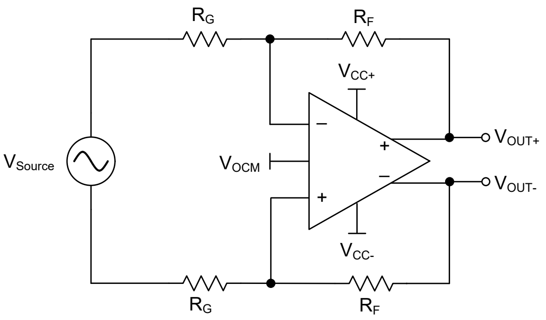


图 8-1. Amplifying Differential Input Signals

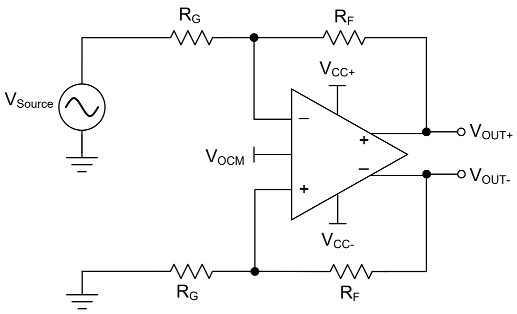


图 8-2. Amplifying Single-ended Input Signals

8.4 Device Functional Modes

8.4.1 Power-Down Mode

The Power-Down mode is used when power saving is required. The power-down terminal ($\overline{PD}$) found on the THS4130 is an active low input. If left unconnected, an internal 250 kΩ resistor to V_{CC+} keeps the device turned on. The threshold voltage for the power-down function is approximately 1.4 V above V_{CC-}. This means that if the $\overline{PD}$ terminal is 1.4 V above V_{CC-}, then the device is active. If the $\overline{PD}$ terminal is less than 1.4 V above V_{CC-}, then the device is off. It is recommended to pull the terminal to V_{CC-} to turn the device off. 图 8-3 shows the simplified version of the power-down circuit. While in the Power-Down mode, the amplifier goes into a high-impedance state. The amplifier's output impedance is typically greater than 1 MΩ in the Power-Down mode.

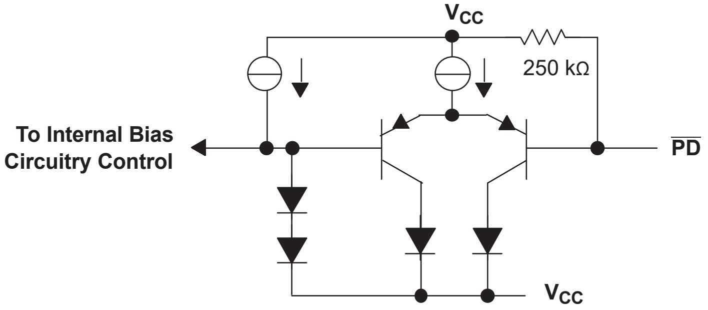
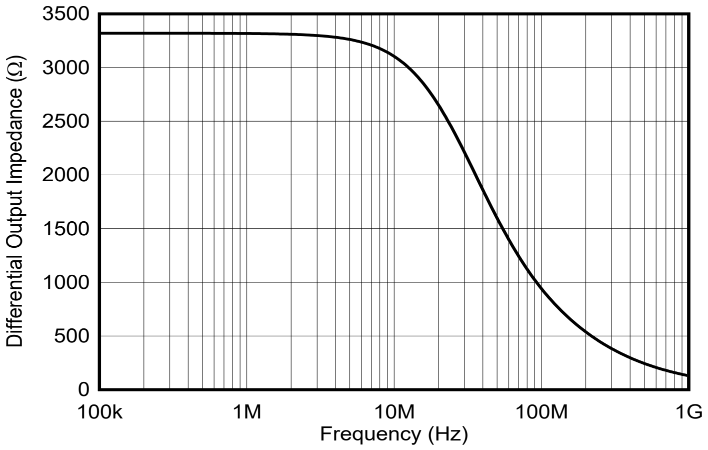


图 8-3. Simplified Power-Down Circuit

Similar to an opamp in an inverting configuration, the output impedance of an FDA is determined by its feedback network configuration. In addition, the THS4130 has an internal 10 kΩ resistor at each output that is tied to the V_{CM} error amplifier (see 节 8.2). The differential output impedance is equal to [(2*R_F + 2*R_G) || 20 kΩ]. 图 8-4 shows the closed loop output impedance of the THS4130 when in power-down.



V_{CC} = ±5 V, G = 1 V/V, R_F = 1kΩ, $\overline{PD}$ = V_{CC-}

图 8-4. Output Impedance (in Power-Down) vs Frequency

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.1.1 Output Common-Mode Voltage

The output common-mode voltage pin sets the dc output voltage of the THS413x. A voltage applied to the V_{OCM} pin from a low-impedance source can be used to directly set the output common-mode voltage. If the V_{OCM} pin is left floating, then it defaults to the mid-rail voltage, defined as:

$$\frac{(V_{CC+})+(V_{CC-})}{2} \tag{1}$$

To minimize common-mode noise, connect a 0.1-µF bypass capacitor to the V_{OCM} pin. Output common-mode voltage causes additional current to flow in the feedback resistor network. Since this current is supplied by the output stage of the amplifier, this creates additional power dissipation. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current may be significant in some applications and may dictate use of the MSOP PowerPAD package to effectively control self-heating.

9.1.1.1 Resistor Matching

Resistor matching is important in FDAs to maintain good output balance. An ideal differential output signal implies the two outputs of the FDA should be exactly equal in amplitude and shifted 180° in phase. Any imbalance in amplitude or phase between the two output signals results in an undesirable common-mode signal at the output. The output balance error is a measure of how well the outputs are balanced and is defined as the ratio of the output common-mode voltage to the output differential signal.

$$Output\ Balance\ Error = \frac{\left(\frac{V_{OUT+} - V_{OUT-}}{2}\right)}{V_{OUT+} - V_{OUT-}} \tag{2}$$

At low frequencies, resistor mismatch is the primary contributor to output balance errors. Additionally CMRR, PSRR, and HD2 performance diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to optimize performance. 表 9-1 provides the recommended resistor values to use for a particular gain.

表 9-1. Recommended Resistor Values

Gain (V/V)	R_G (Ω)	R_F (Ω)
1	390	390
2	374	750
5	402	2010
10	402	4020

9.1.2 Driving a Capacitive Load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The THS413x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in 图 9-1. A minimum value of 20 Ω should work well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

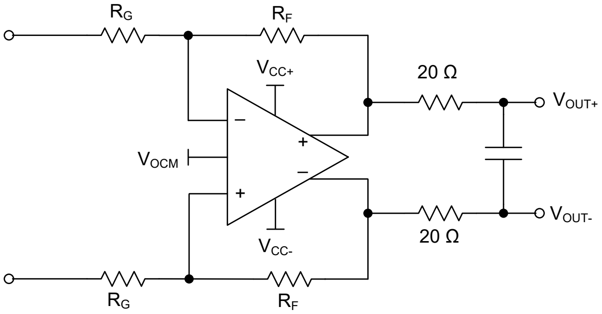


图 9-1. Driving a Capacitive Load

9.1.3 Data Converters

Driving data converters are one of the most popular applications for fully-differential amplifiers. 图 9-2 shows a typical configuration of an FDA attached to a differential analog-to-digital converter (ADC).

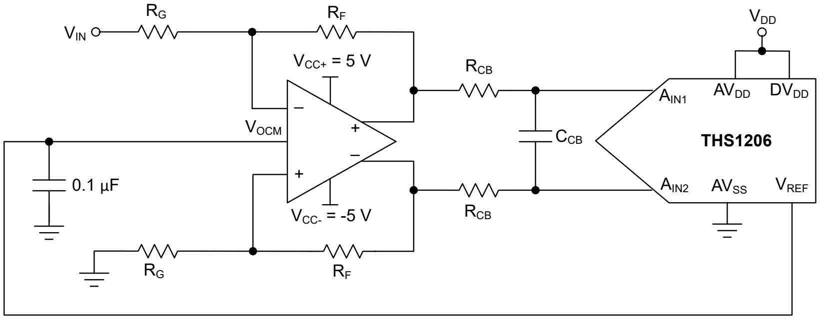


图 9-2. Fully-Differential Amplifier Attached to a Differential ADC

FDAs can operate with a single supply. V_{OCM} defaults to the mid-rail voltage, $V_{CC}/2$. The differential output may be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then it is recommended to connect it directly to the V_{OCM} of the amplifier using a bypass capacitor to reduce broadband common-mode noise.

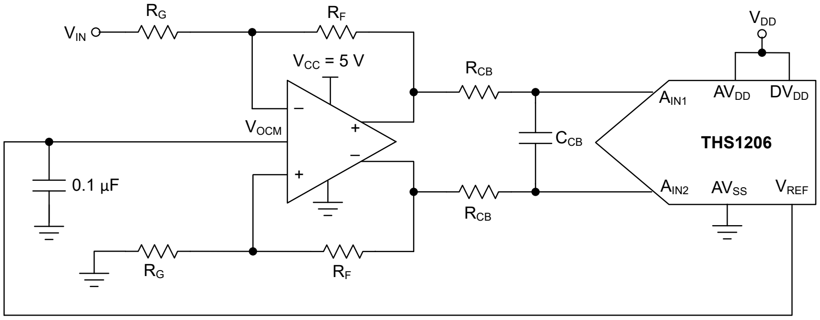


图 9-3. Fully-Differential Amplifier Using a Single Supply

9.1.4 Single-Supply Applications

For proper operation, the input common-mode voltage to the input terminal of the amplifier should not exceed the common-mode input voltage range. However, some single-supply applications may require the input voltage to exceed the common-mode input voltage range. In such cases, the circuit configuration of 图 9-4 is suggested to bring the common-mode input voltage within the specifications of the amplifier.

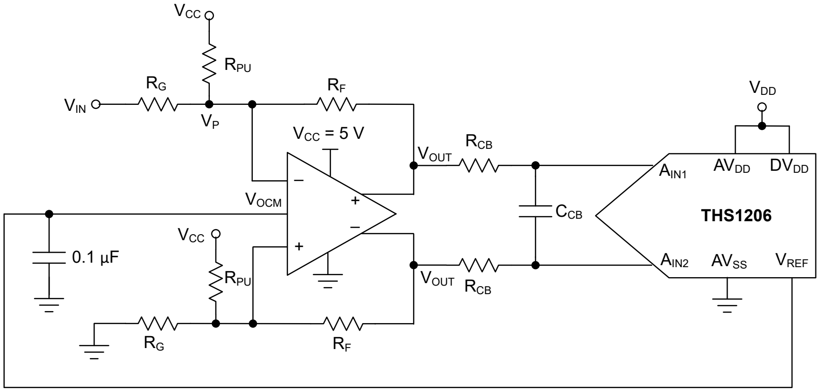


图 9-4. Circuit With Improved Common-Mode Input Voltage

方程式 3 is used to calculate R_{PU}:

$$R_{PU} = \frac{V_P - V_{CC}}{(V_{IN} - V_P)\frac{1}{R_G} + \left(V_{OUT} - V_P\right)\frac{1}{R_F}} \tag{3}$$

9.2 Typical Application

For signal conditioning in ADC applications, it is important to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high-frequency noise with the frequency of operation. 图 9-5 shows a method by which the noise may be filtered in the THS413x.

图 9-5 shows a typical application design example for the THS413x device in active low-pass filter topology driving and ADC.

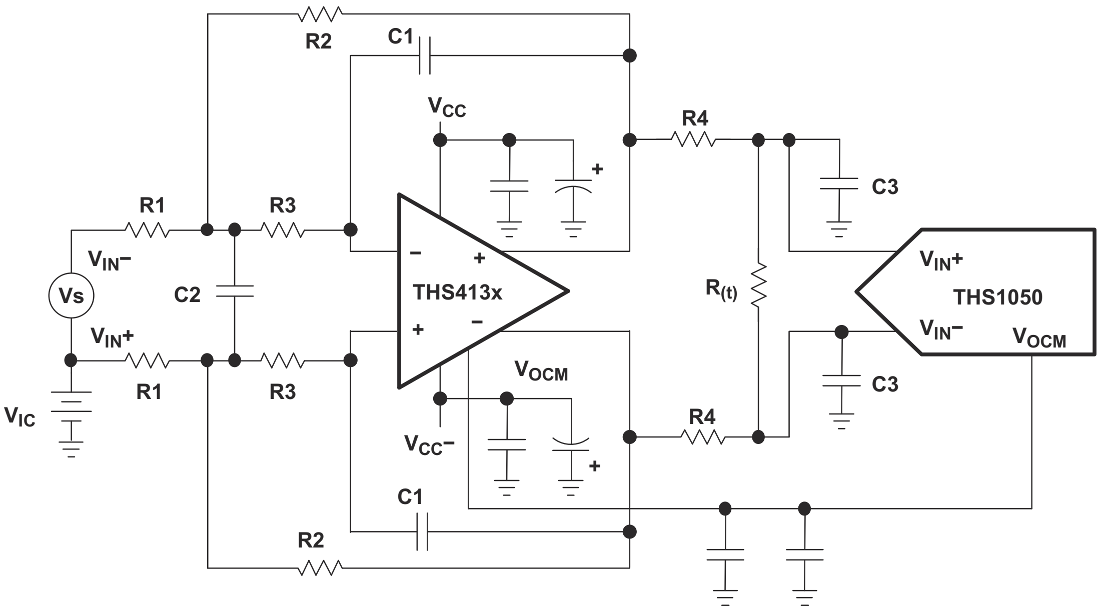


图 9-5. Antialias Filtering

9.2.1 Design Requirements

表 9-2 shows example design parameters and values for the typical application design example in 图 9-5.

表 9-2. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±2.5 V to ±15 V
Amplifier topology	Voltage feedback
Output control	DC coupled with output common mode control capability
Filter requirement	500 kHz, Multiple feedback low pass filter

9.2.2 Detailed Design Procedure

9.2.2.1 Active Antialias Filtering

图 9-5 shows a multiple-feedback (MFB) lowpass filter. The transfer function for this filter circuit is:

$$H_d(f) = \left(\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1} \right) \times \left(\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi fR4RtC3}{2R4 + Rt}} \right) \quad \text{Where } K = \frac{R2}{R1} \tag{4}$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}} \quad \text{and } Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1} \tag{5}$$

K sets the pass band gain, fc is the cutoff frequency for the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \quad \text{and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re} \tag{6}$$

where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$\text{FSF} \times \text{fc} = \frac{1}{2\pi RC\sqrt{2 \times mn}} \text{ and } Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)} \quad (7)$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

9.2.3 Application Curve

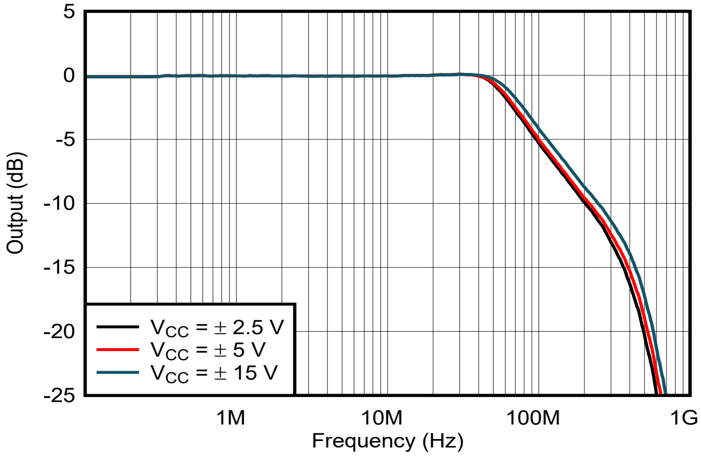


图 9-6. Large-Signal Frequency Response

10 Power Supply Recommendations

The THS413x device was designed to operate on power supplies ranging from ±2.5 V to ±15 V (single-ended supplies of 5 V to 30 V). TI recommends using a power-supply accuracy of 5% or better. When operated on a board with high-speed digital signals, it is important to provide isolation between digital signal noise and the analog input pins. The THS413x is connected to power supplies through pin 3 (V_{CC+}) and pin 6 (V_{CC-}). Each supply pin should be decoupled to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane the vias should be configured for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, the THS413x device should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

11 Layout

11.1 Layout Guidelines

To achieve the levels of high-frequency performance of the THS413x device, follow proper printed-circuit board (PCB) high-frequency design techniques. The following is a general set of guidelines. In addition, a THS413x device evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes—it is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling—use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this

distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.

- Short trace runs or compact part placements—optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inputs of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.

11.2 Layout Example

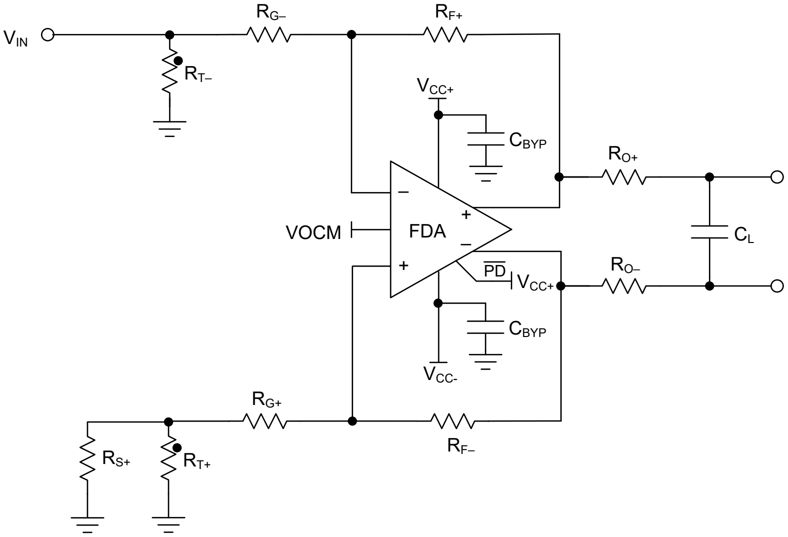


图 11-1. Representative Schematic for Layout

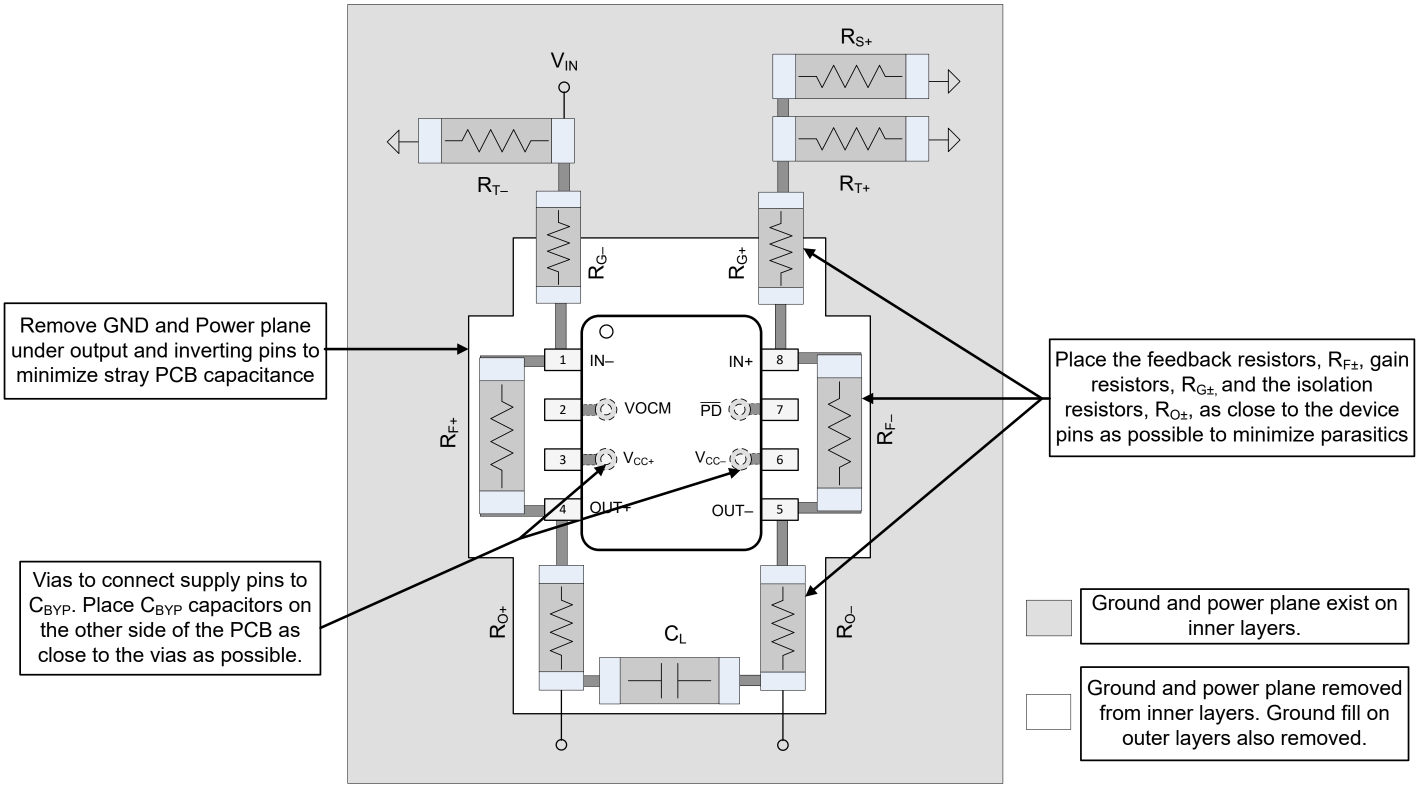


图 11-2. Layout Recommendations

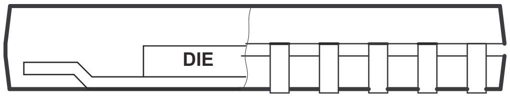
11.3 General PowerPAD Design Considerations

The THS413x is available in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted (see 图 11-3 **a** and 图 11-3 **b**). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see 图 11-3 **c**). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

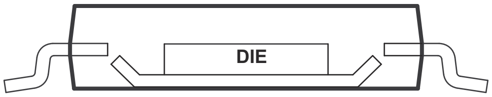
The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the previously awkward mechanical methods of heatsinking.

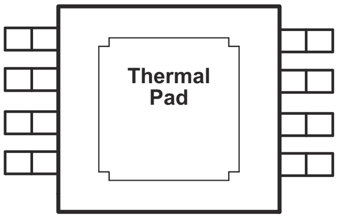
More complete details of the PowerPAD installation process and thermal management techniques can be found in *PowerPAD Thermally-Enhanced Package*. This document can be found on the TI website (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to SLMA002 when ordering.



Side View (a)



End View (b)



Bottom View (c)

A. The thermal pad (PowerPAD) is electrically isolated from all other pins and can be connected to any potential from V_{CC-} to V_{CC+}. Typically, the thermal pad is connected to the ground plane because this plane tends to physically be the largest and is able to dissipate the most amount of heat.

图 11-3. Views of Thermally-Enhanced DGN Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Design Guide for 2.3 nV/ √Hz, Differential, Time Gain Control (TGC) DAC Reference Design for Ultrasound* design guide
- Texas Instruments, *EVM User's Guide for High-Speed Fully-Differential Amplifier* user's guide
- Texas Instruments, *Fully Differential Amplifiers* application note
- Texas Instruments, *Maximizing Signal Chain Distortion Performance Using High Speed Amplifiers* application note
- Texas Instruments, *PowerPAD Thermally-Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *TI Precision Labs - Fully Differential Amplifiers* video series

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

PowerPAD™ are trademarks of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4130CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4130C	Samples
THS4130CDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4130C	Samples
THS4130CDGK	LIFEBUY	VSSOP	DGK	8	80	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	0 to 70	ATP	
THS4130CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130CDGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOB	Samples
THS4130ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4130IDGK	LIFEBUY	VSSOP	DGK	8	80	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASO	
THS4130IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOC	Samples
THS4130IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4131CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples
THS4131CDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples
THS4131CDGK	LIFEBUY	VSSOP	DGK	8	80	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	0 to 70	ATQ	
THS4131CDGKG4	LIFEBUY	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ATQ	
THS4131CDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	0 to 70	ATQ	Samples
THS4131CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOD	Samples
THS4131CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4131ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples
THS4131IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples
THS4131IDGK	LIFEBUY	VSSOP	DGK	8	80	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP	
THS4131IDGKG4	LIFEBUY	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP	
THS4131IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOE	Samples
THS4131IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

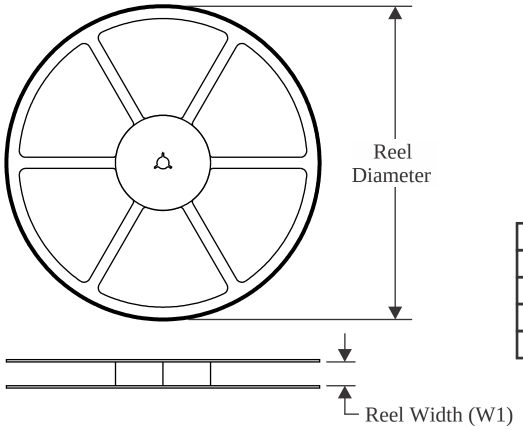
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

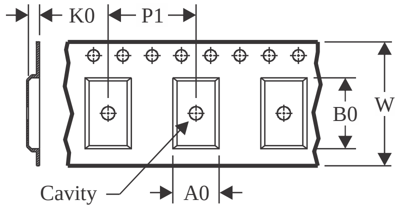
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

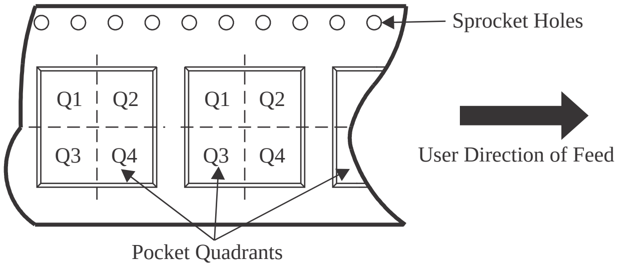


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

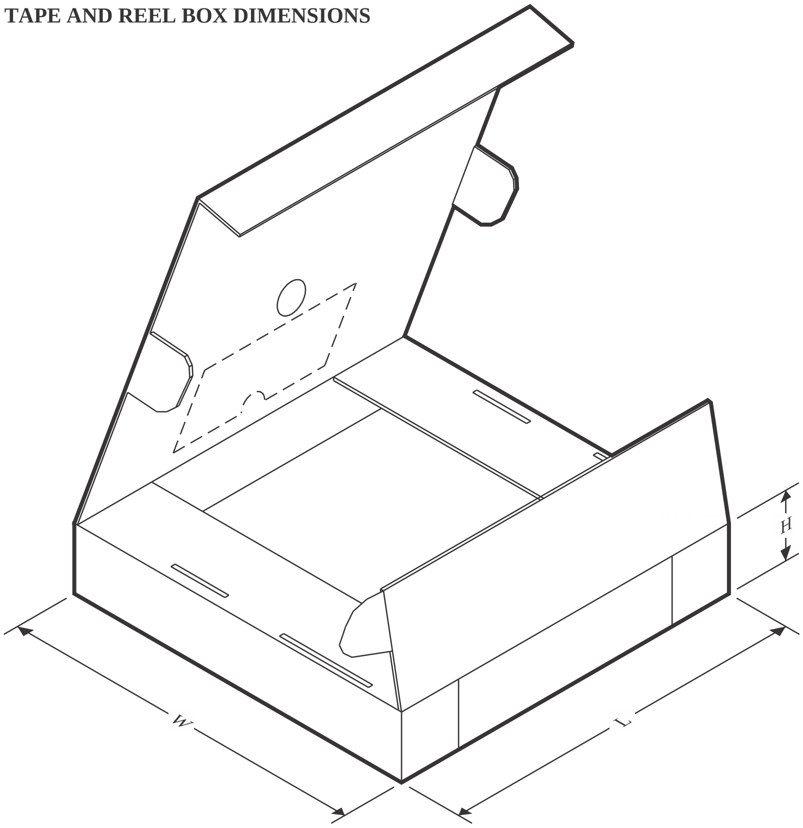
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4130CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

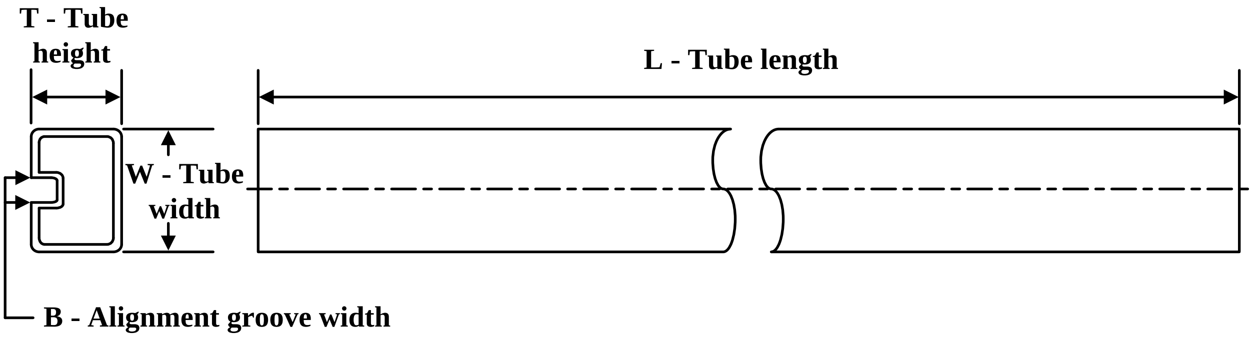
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4130CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4130IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4130IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4130IDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4131CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4131CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4131CDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4131IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4131IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4131IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4130CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4130CDG4	D	SOIC	8	75	505.46	6.76	3810	4
THS4130CDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THS4130ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4130IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THS4131CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4131CDG4	D	SOIC	8	75	505.46	6.76	3810	4
THS4131CDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THS4131CDGKG4	DGK	VSSOP	8	80	330	6.55	500	2.88
THS4131ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4131IDG4	D	SOIC	8	75	505.46	6.76	3810	4
THS4131IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THS4131IDGKG4	DGK	VSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

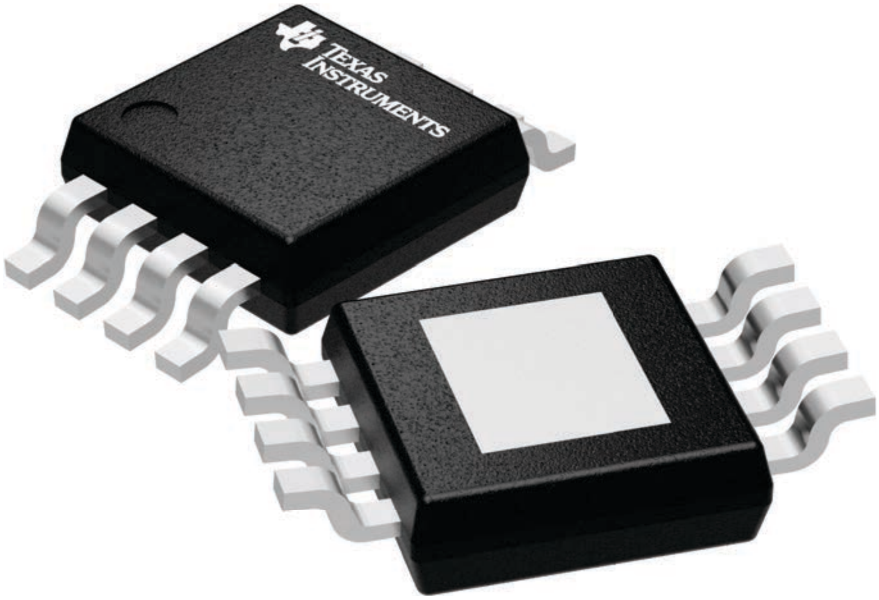
DGN 8

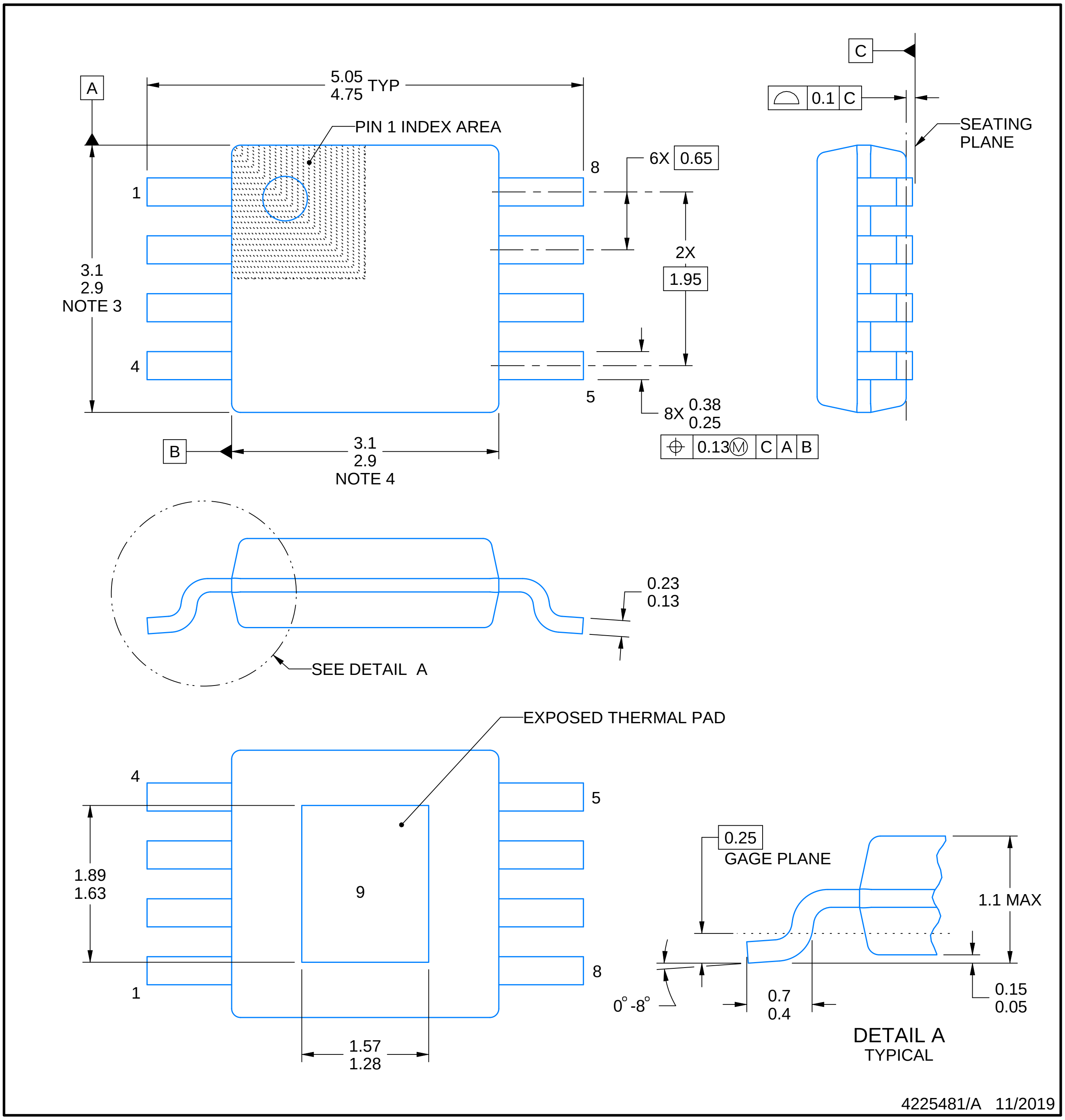
PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

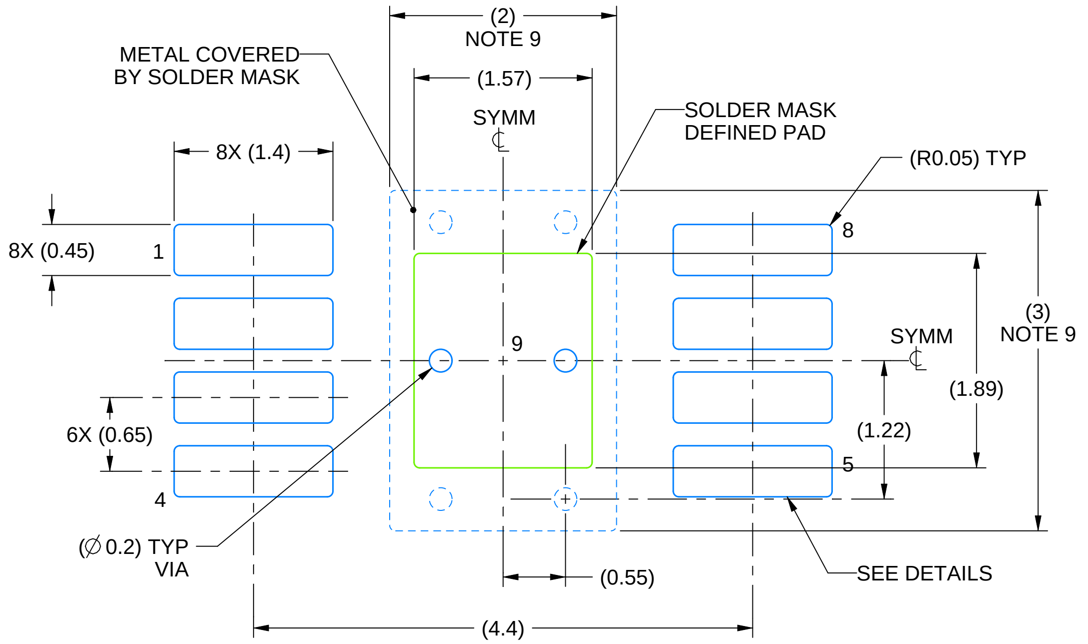




PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

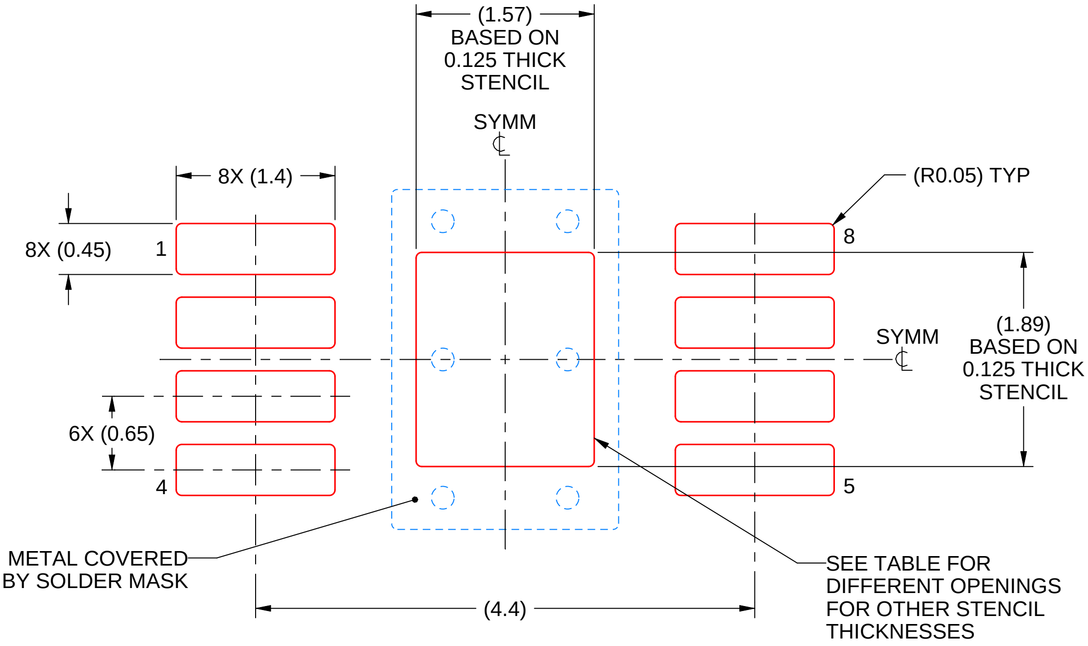
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

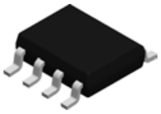


SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

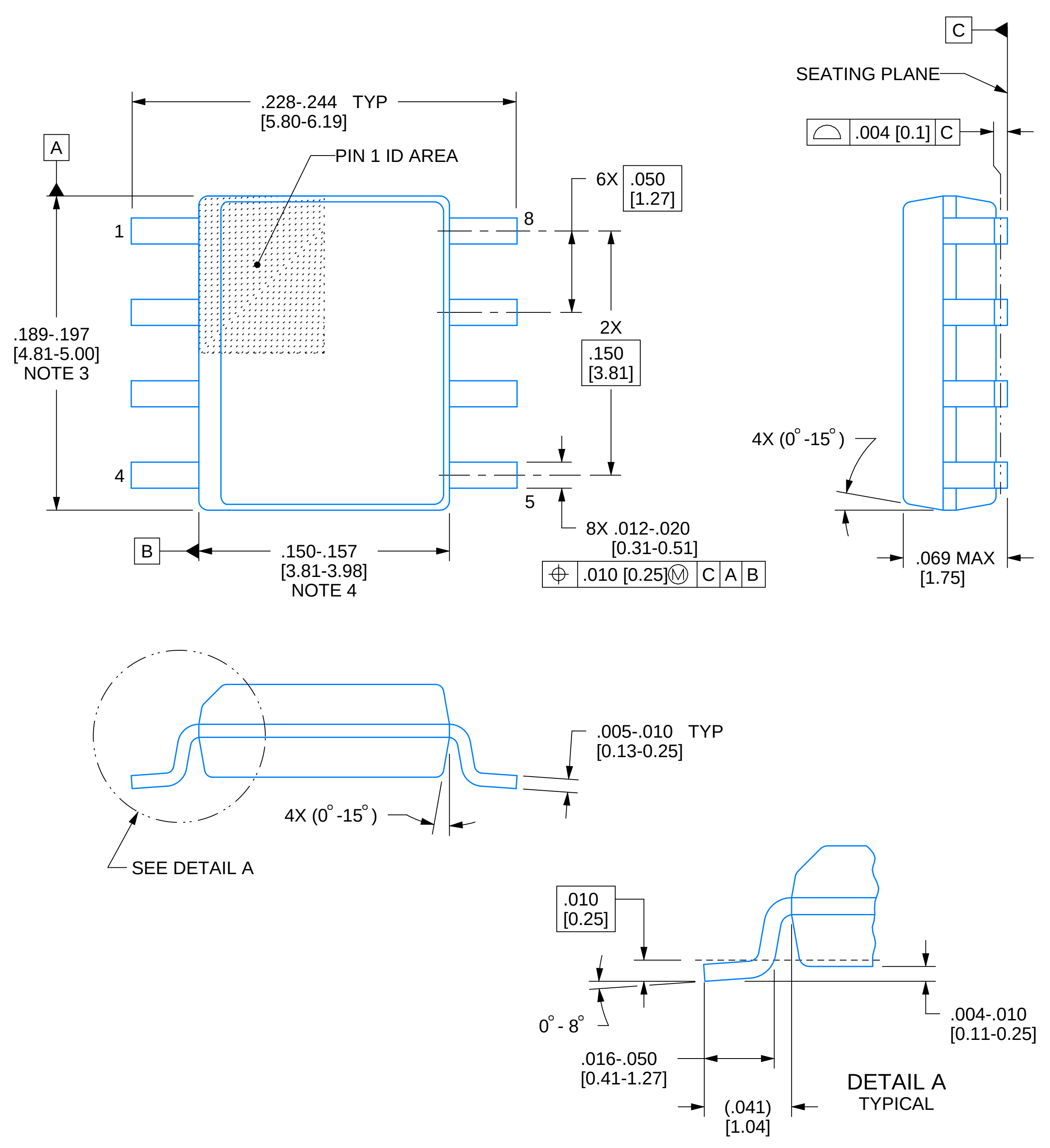


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

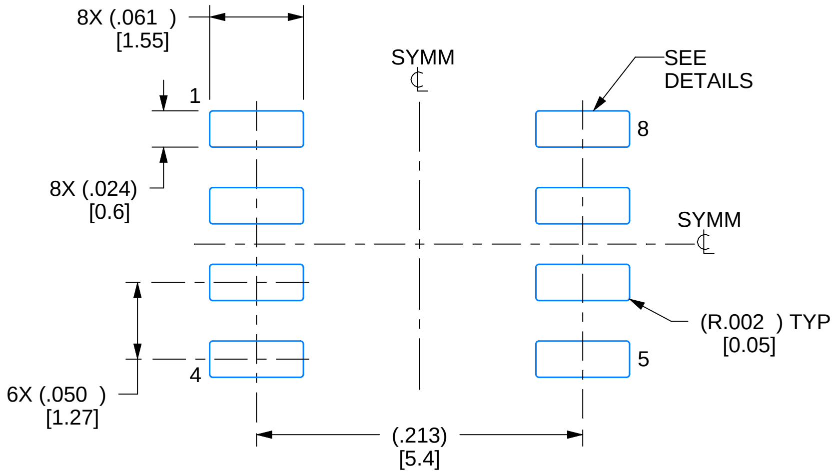
SMALL OUTLINE INTEGRATED CIRCUIT



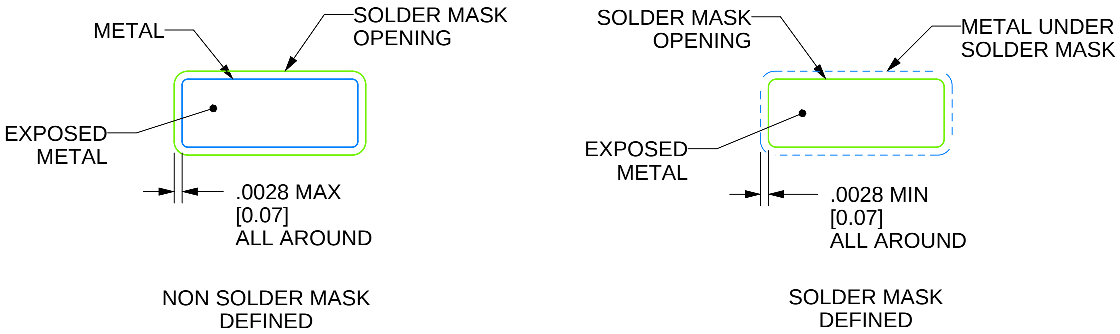
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



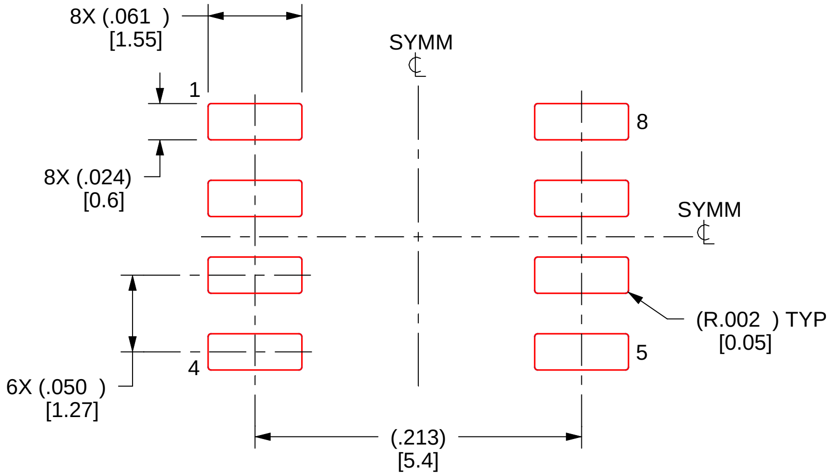
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



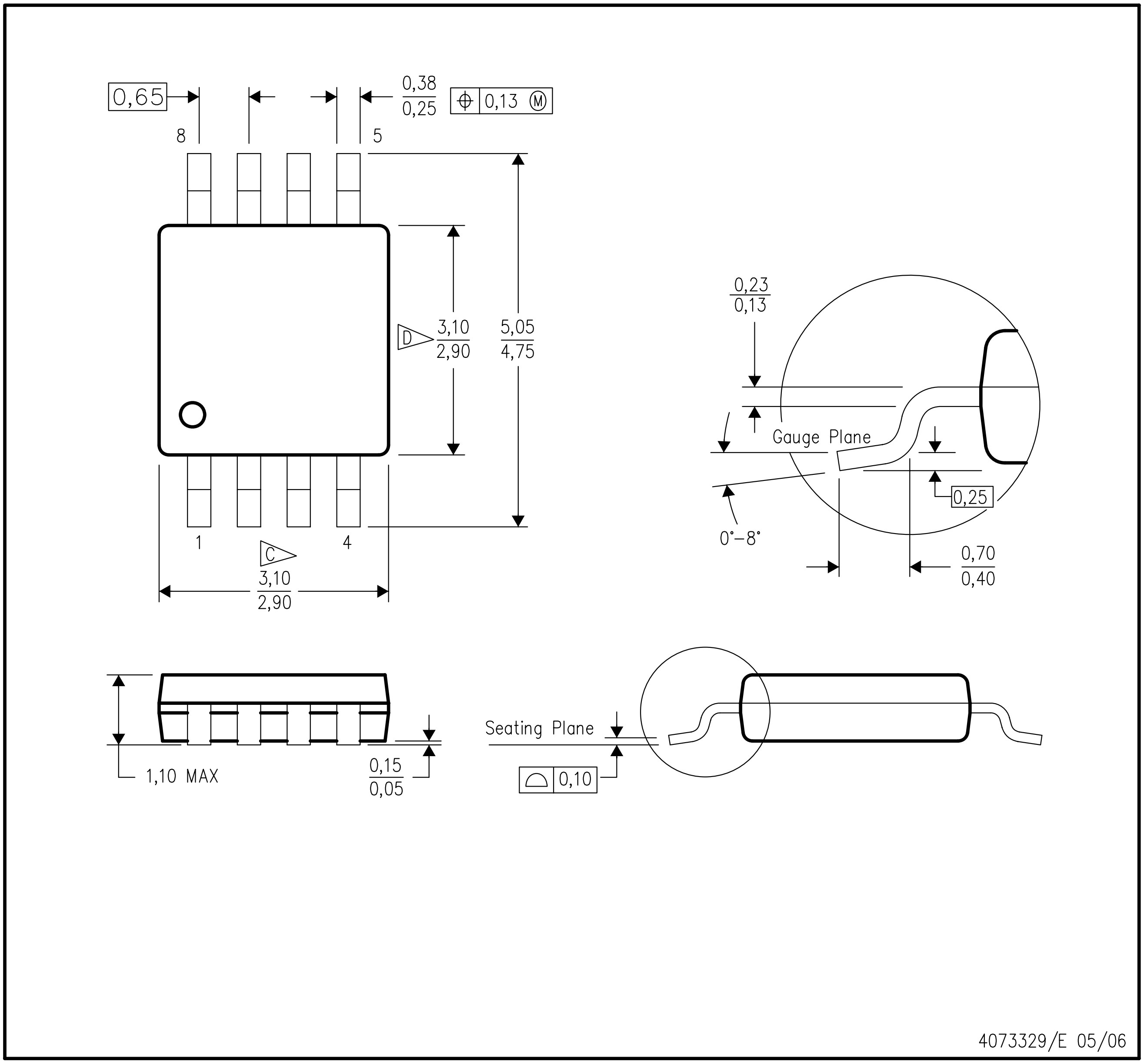
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265