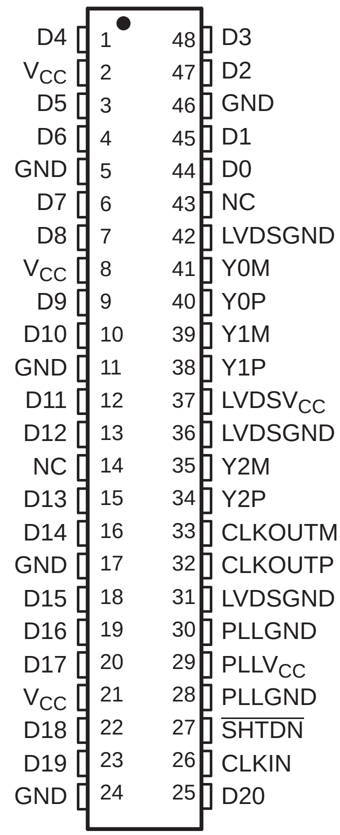
LVDS SERDES TRANSMITTER

Check for Samples: SN65LVDS95

FEATURES

- **3:21 Data Channel Compression at up to 1.428 Gigabits/s Throughput**
- **Suited for Point-to-Point Subsystem Communication With Very Low EMI**
- **21 Data Channels Plus Clock in Low-Voltage TTL and 3 Data Channels Plus Clock Out Low-Voltage Differential**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant Data Inputs**
- **'LVDS95 Has Rising Clock Edge Triggered Inputs**
- **Bus Pins Tolerate 6-kV HBM ESD**
- **Packaged in Thin Shrink Small-Outline Package With 20 Mil Terminal Pitch**
- **Consumes <1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 20 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Inputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Industrial Temperature Qualified T_A = –40°C to 85°C**
- **Replacement for the National DS90CR215**

DGG PACKAGE
(TOP VIEW)



DESCRIPTION

The SN65LVDS95 LVDS serdes (serializer/deserializer) transmitter contains three 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and four low-voltage differential signaling (LVDS) line drivers in a single integrated circuit. These functions allow 21 bits of single-ended LVTTL data to be synchronously transmitted over 4 balanced-pair conductors for receipt by a compatible receiver, such as the SN65LVDS96.

When transmitting, data bits D0 through D20 are each loaded into registers of the SN65LVDS95 on the rising edge of the input clock signal (CLKIN). The frequency of CLKIN is multiplied seven times and then used to serially unload the data registers in 7-bit slices. The three serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

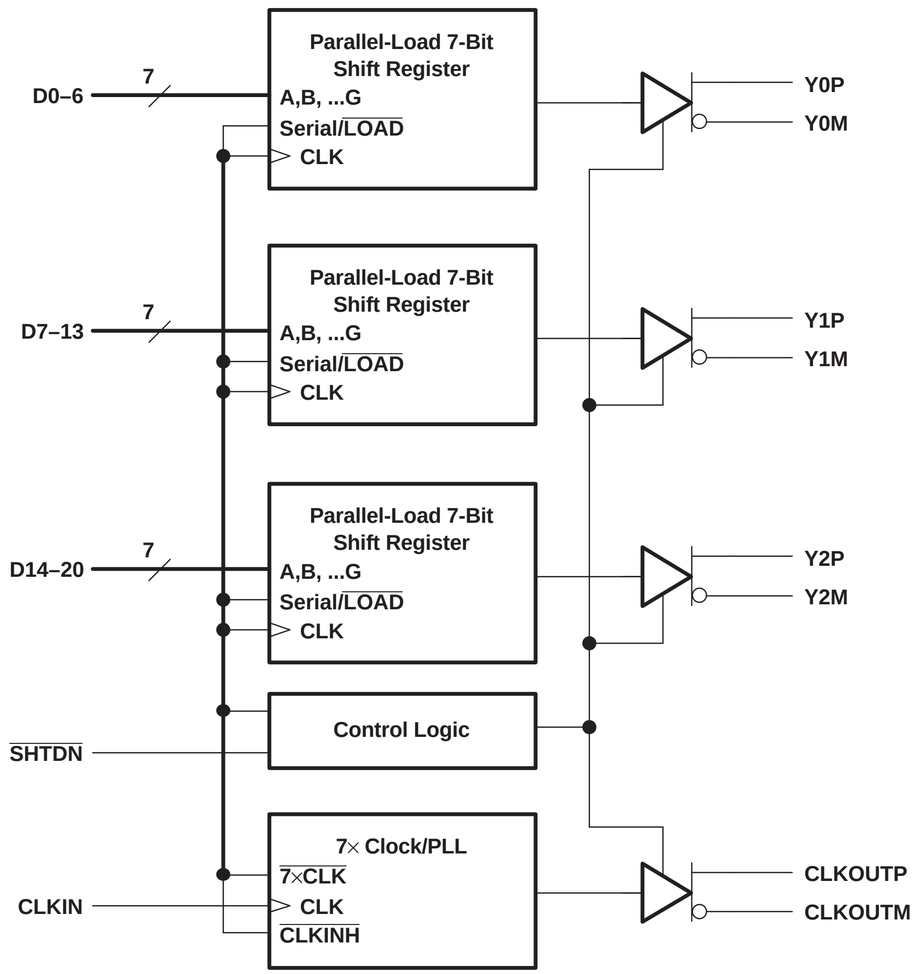
The SN65LVDS95 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear ($\overline{SHTDN}$) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN65LVDS95 is characterized for operation over ambient air temperatures of –40°C to 85°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



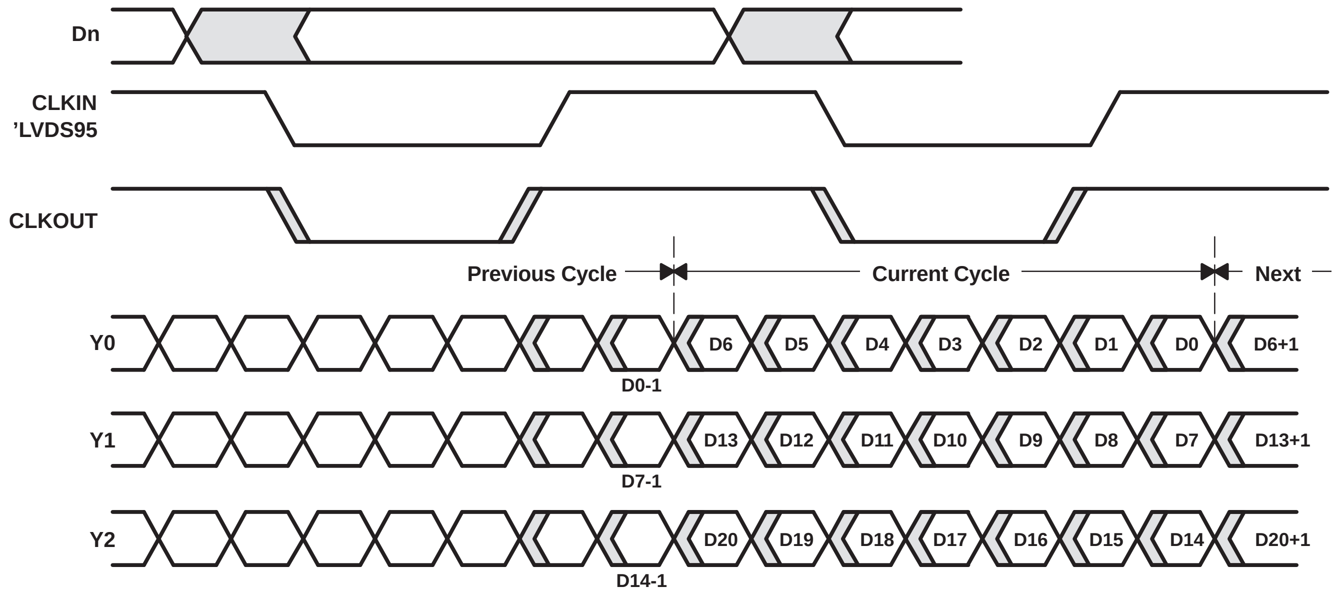
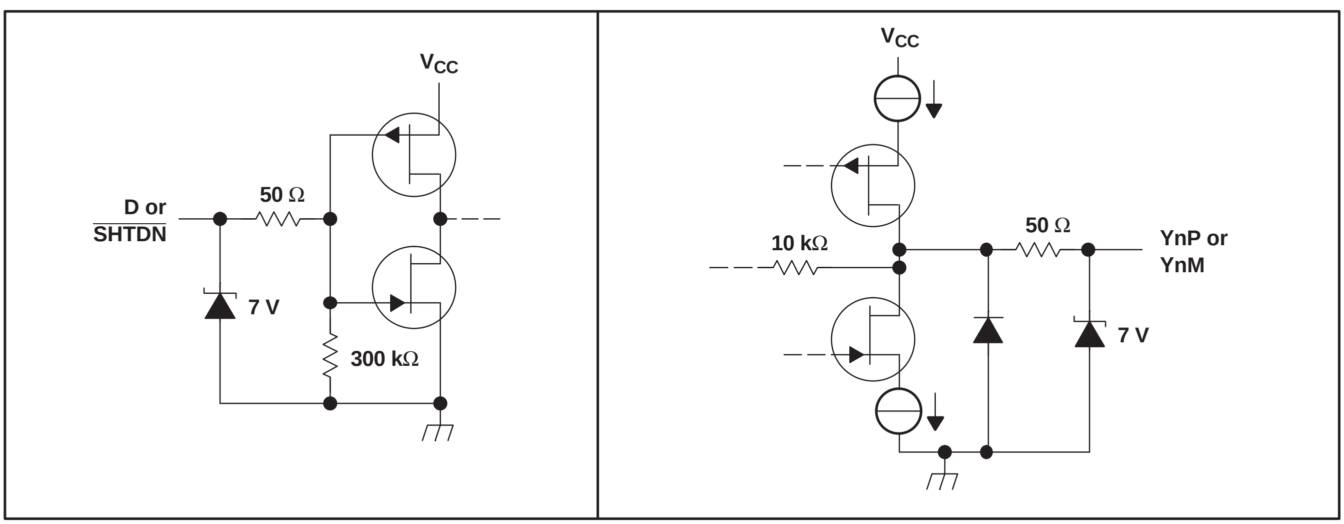


Figure 1. 'LVDS95 Load and Shift Sequences

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}	Supply voltage range(2)		–0.5 V to 4 V
V_O	Voltage range at any output terminal		–0.5 V to V_{CC} + 0.5 V
V_I	Voltage range at any input terminal		–0.5 V to 5.5 V
	Electrostatic discharge(3)	Bus pins (Class 3A)	6 KV
		Bus pins (Class 2B)	400 V
		All pins (Class 3A)	6 KV
		All pins (Class 2B)	200 V
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.
(3) This rating is measured using MIL-STD-883C Method, 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGG	1316 mW	13.1 mW/°C	724 mW	526 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
Z_L	Differential load impedance	90		132	Ω
T_A	Operating free-air temperature	40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IT}	Input voltage threshold			1.4		V
$\|V_{OD}\|$	Differential steady-state output voltage magnitude	R_L = 100 Ω, See Figure 3	247		454	mV
$\Delta\|V_{OD}\|$	Change in the steady-state differential output voltage magnitude between opposite binary states	R_L = 100 Ω, See Figure 3			50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 3		80	150	mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$			20	μA
I_{IL}	Low-level input current	V_{IL} = 0 V			±10	μA
I_{OS}	Short-circuit output current	V_{OY} = 0 V			±24	mA
		V_{OD} = 0 V			±12	mA
I_{OZ}	High-impedance state output current	V_O = 0 V to V_{CC}			±10	μA
$I_{CC(AVG)}$	Quiescent current (average)	Disabled, all inputs at GND			280	μA
		Enabled, R_L = 100 Ω (4 places), Worst-case pattern (see Figure 4), t_c = 15.38 ns		85	110	mA
C_i	Input capacitance			3		pF

(1) All typical values are V_{CC} = 3.3 V, T_A = 25°C.

TIMING REQUIREMENTS

		MIN	NOM	MAX	UNIT
t_c	Input clock period	14.7	t_c	50	ns
t_w	High-level input clock pulse width duration	$0.4t_c$		$0.6t_c$	ns
t_t	Input signal transition time			5	ns
t_{su}	Data setup time, D0 through D27 before CLKIN↑ ('95) (see Figure 2)	3			ns
t_h	Data hold time, D0 through D27 after CLKIN↑ ('95) (see Figure 2)	1.5			ns

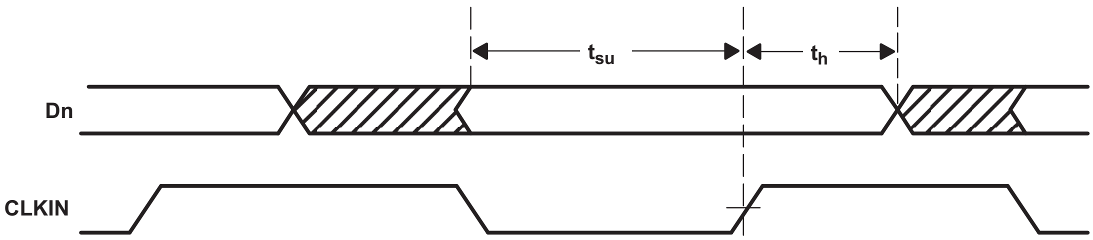
SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_0	Delay time, CLKOUT serial bit position 0	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps(2), See Figure 5	–0.20	0	0.20	ns
t_1	Delay time, CLKOUT↑ serial bit position 1		$1/7t_c$–0.20		$1/7t_c$+0.20	ns
t_2	Delay time, CLKOUT↑ serial bit position 2		$2/7t_c$–0.20		$2/7t_c$+0.20	ns
t_3	Delay time, CLKOUT↑ serial bit position 3		$3/7t_c$–0.20		$3/7t_c$+0.20	ns
t_4	Delay time, CLKOUT↑ serial bit position 4		$4/7t_c$–0.20		$4/7t_c$+0.20	ns
t_5	Delay time, CLKOUT↑ serial bit position 5		$5/7t_c$–0.20		$5/7t_c$+0.20	ns
t_6	Delay time, CLKOUT↑ serial bit position 6		$6/7t_c$–0.20		$6/7t_c$+0.20	ns
$t_{sk(o)}$	Output skew, t_n –n/7 t_c		–0.20		0.20	ns
t_7	Delay time, CLKIN↑ to CLKOUT↑	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps(2), See Figure 5		4.2		ns
$\Delta t_{C(O)}$	Output clock cycle-to-cycle jitter(3)	t_c = 15.38 ns + 0.75 sin(2π500E3t) ±0.05 ns, See Figure 6		±80		ps
		t_c = 15.38 ns + 0.75 sin(2π2E6t) ±0.05 ns, See Figure 6		±300		ps
t_w	High-level output clock pulse duration			4/7 t_c		ns
t_t	Differential output voltage transition time (t_r or t_f)	See Figure 3	260	700	1500	ps
t_{en}	Enable time, $\overline{\text{SHTDN}}$↑ to phase lock (Yn valid)	See Figure 7		1		ms
t_{dis}	Disable time, $\overline{\text{SHTDN}}$↓ to off-state (CLKOUT low)	See Figure 8		250		ns

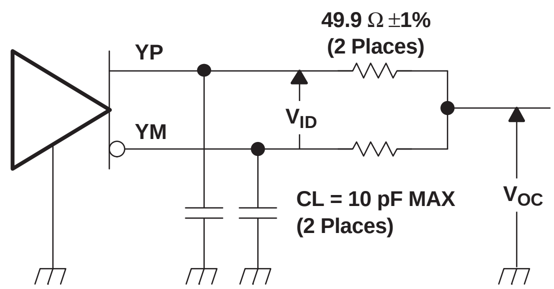
(1) All typical values are V_{CC} = 3.3 V, T_A = 25°C.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) The output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.

PARAMETER MEASUREMENT INFORMATION



NOTE: All input timing is defined at 1.4 V on an input signal with a 10% to 90% rise or fall time of less than 5 ns.

Figure 2. Setup and Hold Time Definition



NOTE: The lumped instrumentation capacitance for any single ended voltage measurement is less than or equal to 10 pF. When making measurements at YP or YM, the complementary output shall be similarly loaded.

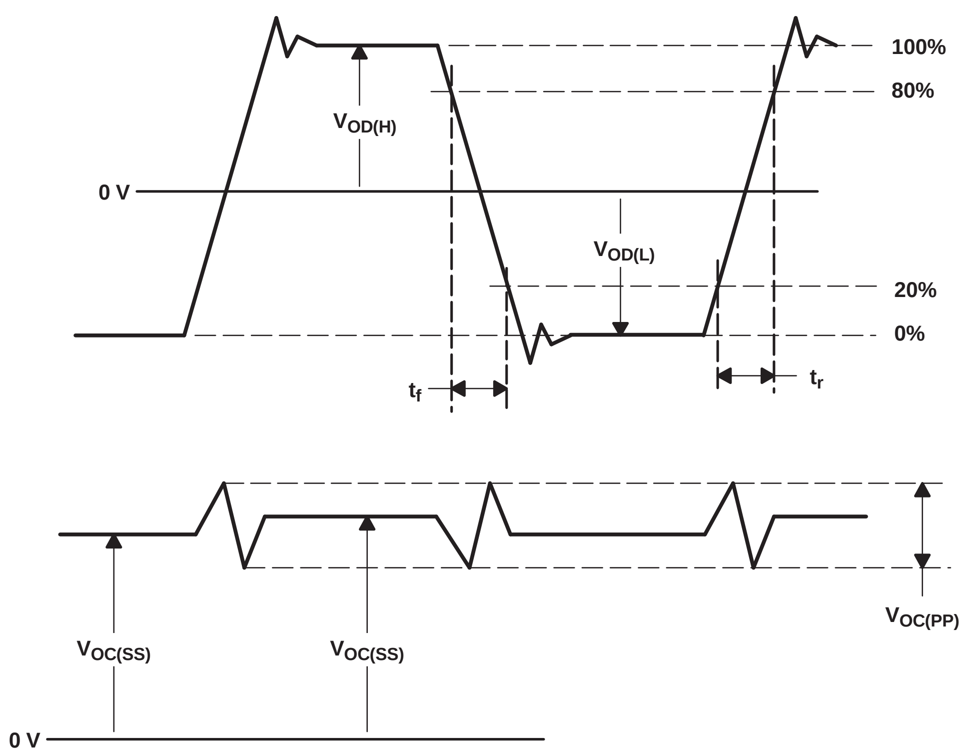
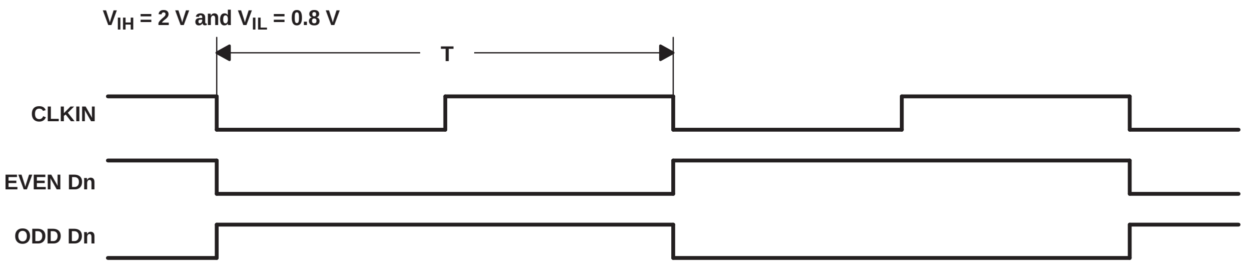


Figure 3. Test Load and Voltage Definitions for LVDS Outputs

PARAMETER MEASUREMENT INFORMATION (continued)



(1) The worst-case test pattern produces nearly the maximum switching frequency for all of the LV-TTL outputs.

Figure 4. Worst-Case Power Test Pattern

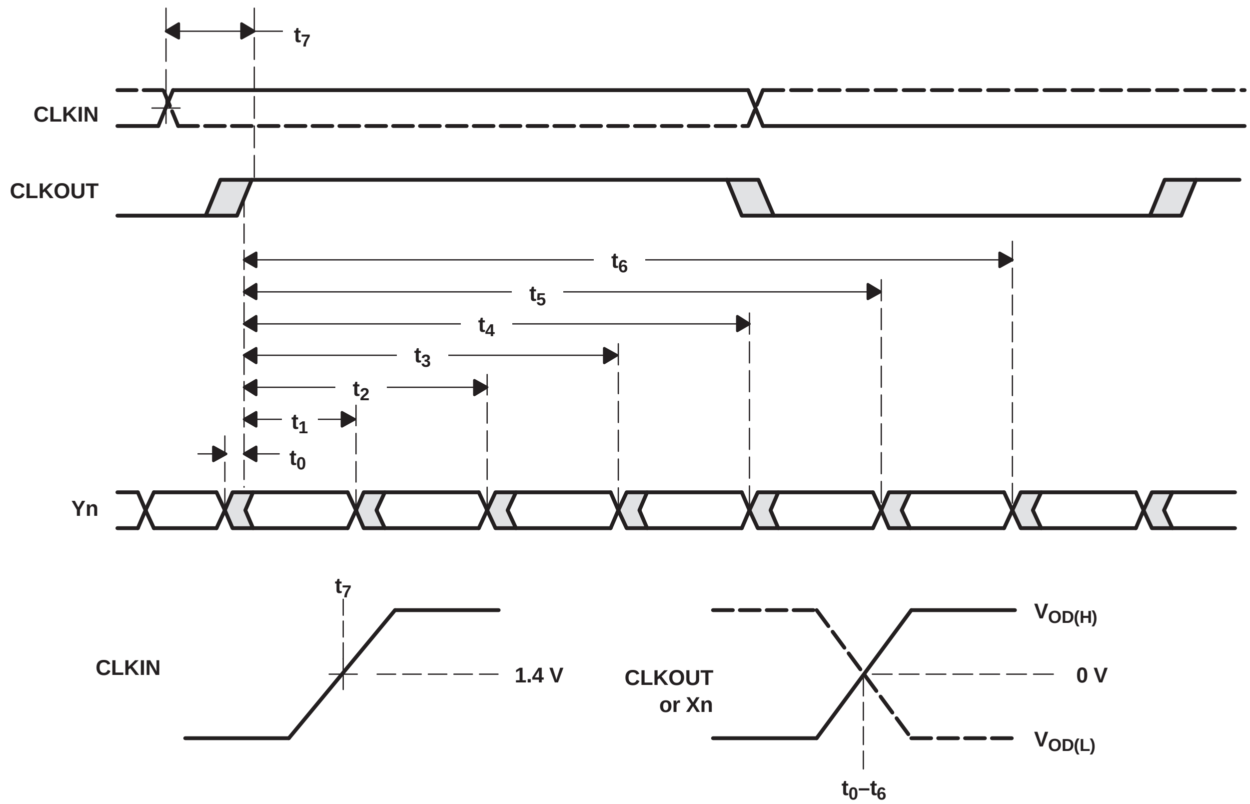


Figure 5. Timing Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

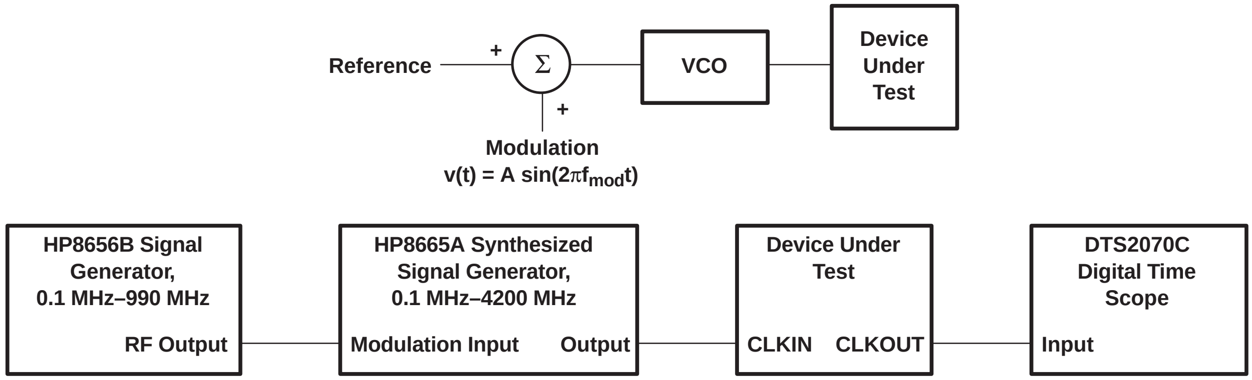


Figure 6. Clock Jitter Test Setup

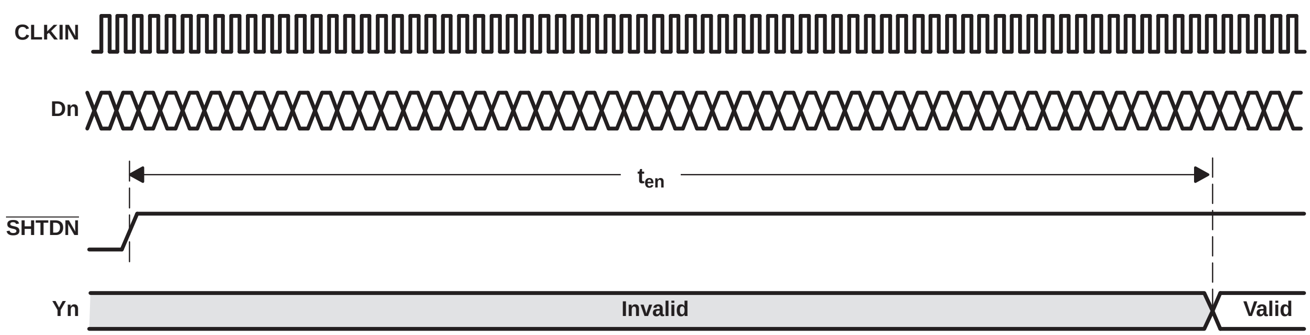


Figure 7. Enable Time Measurement Definition

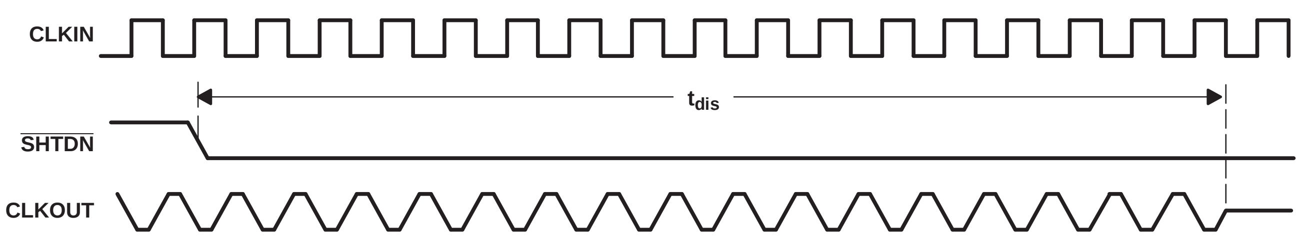


Figure 8. Disable Time Measurement Definition

TYPICAL CHARACTERISTICS

WORST-CASE SUPPLY CURRENT vs FREQUENCY

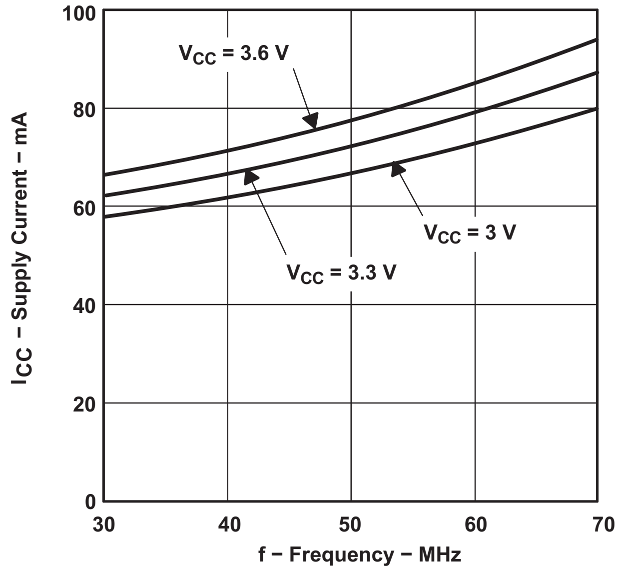


Figure 9.

APPLICATION INFORMATION

16-BIT BUS EXTENSION

In a 16-bit bus application (Figure 10), TTL data and clock coming from bus transceivers that interface the backplane bus arrive at the Tx parallel inputs of the LVDS serdes transmitter. The clock associated with the bus is also connected to the device. The on-chip PLL synchronizes this clock with the parallel data at the input. The data is then multiplexed into three different line drivers which perform the TTL to LVDS conversion. The clock is also converted to LVDS and presented to a separate driver. This synchronized LVDS data and clock at the receiver, which recovers the LVDS data and clock, performs a conversion back to TTL. Data is then demultiplexed into a parallel format. An on-chip PLL synchronizes the received clock with the parallel data, and then all are presented to the parallel output port of the receiver.

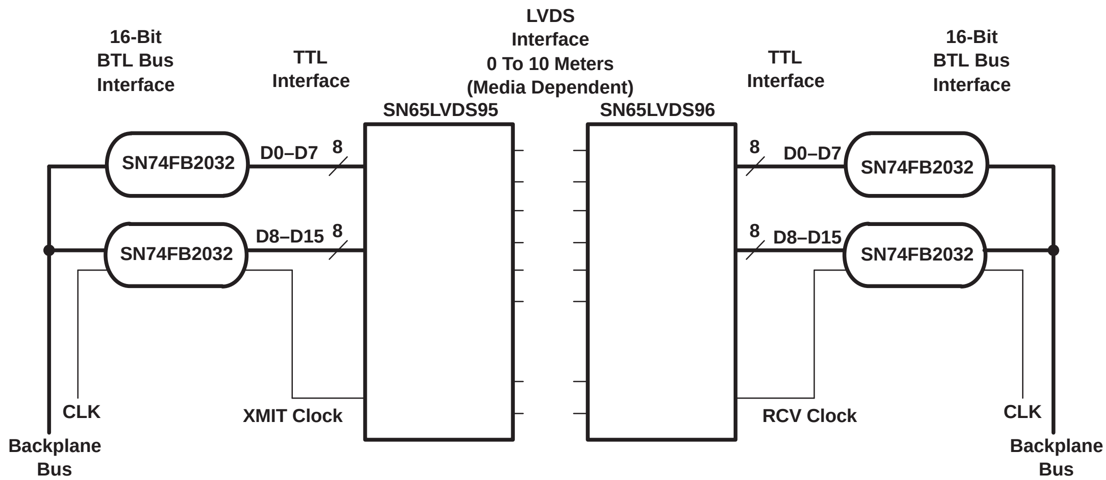


Figure 10. 16-Bit Bus Extension

16-BIT BUS EXTENSION WITH PARITY

In the previous application we did not have a checking bit that would provide assurance that the data crosses the link. If we add a parity bit to the previous example, we would have a diagram similar to the one in Figure 11. The device following the SN74FB2032 is a low cost parity generator. Each transmit-side transceiver/parity generator takes the LVTTL data from the corresponding transceiver, performs a parity calculation over the byte, and then passes the bits with its calculated parity value on the parallel input of the LVDS serdes transmitter. Again, the on-chip PLL synchronizes this transmit clock with the eighteen parallel bits (16 data + 2 parity) at the input. The synchronized LVDS data/parity and clock arrive at the receiver.

The receiver performs the conversion from LVDS to LVTTL and the transceiver/parity generator performs the parity calculations. These devices compare their corresponding input bytes with the value received on the parity bit. The transceiver/parity generator will assert its parity error output if a mismatch is detected.

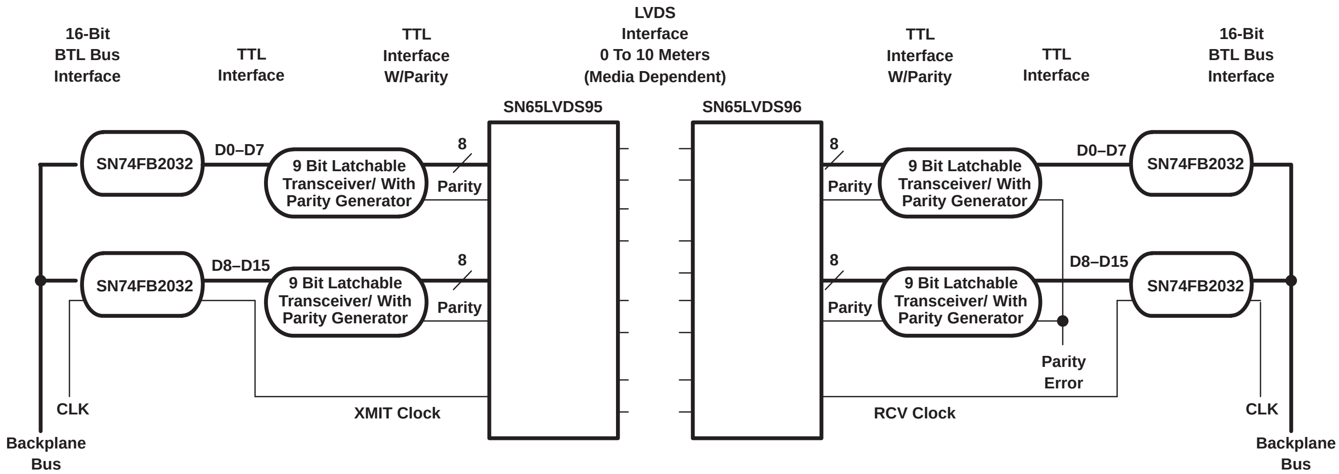


Figure 11. 16-Bit Bus Extension With Parity

LOW COST VIRTUAL BACKPLANE TRANSCEIVER

Figure 12 represents LVDS serdes in an application as a virtual backplane transceiver (VBT). The concept of a VBT can be achieved by implementing individual LVDS serdes chipsets in both directions of subsystem serialized links.

Depending on the application, the designer will face varying choices when implementing a VBT. In addition to the devices shown in Figure 12, functions such as parity and delay lines for control signals could be included. Using additional circuitry, half-duplex or full-duplex operation can be achieved by configuring the clock and control lines properly.

The designer may choose to implement an independent clock oscillator at each end of the link and then use a PLL to synchronize LVDS serdes's parallel I/O to the backplane bus. Resynchronizing FIFOs may also be required.

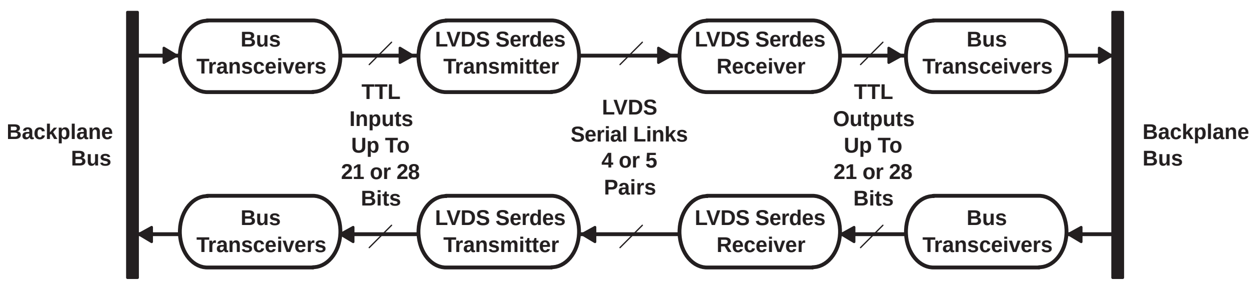


Figure 12. Virtual Backplane Transceiver

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS95DGG	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SN65LVDS95	Samples
SN65LVDS95DGGG4	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SN65LVDS95	Samples
SN65LVDS95DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SN65LVDS95	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LVDS95 :

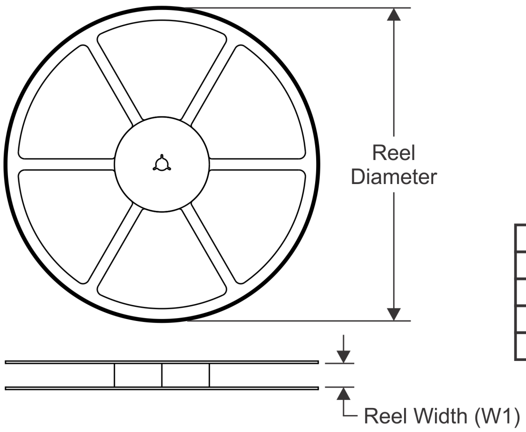
- Automotive : SN65LVDS95-Q1
- Enhanced Product : SN65LVDS95-EP

NOTE: Qualified Version Definitions:

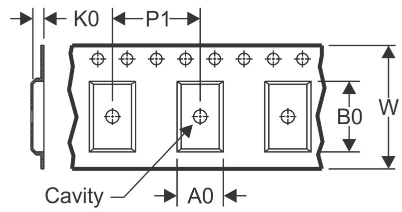
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

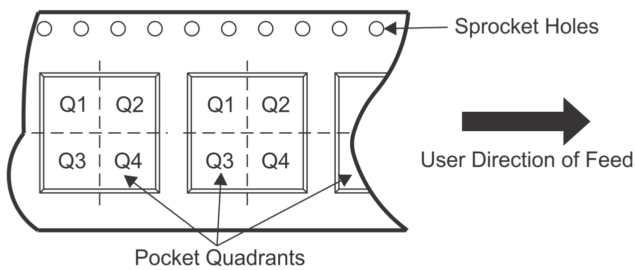


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

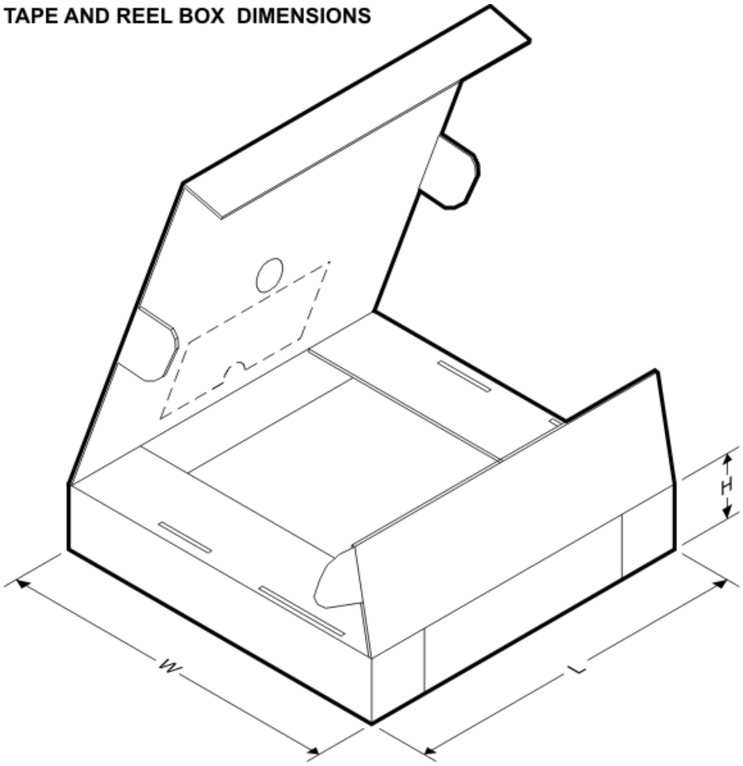
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS95DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

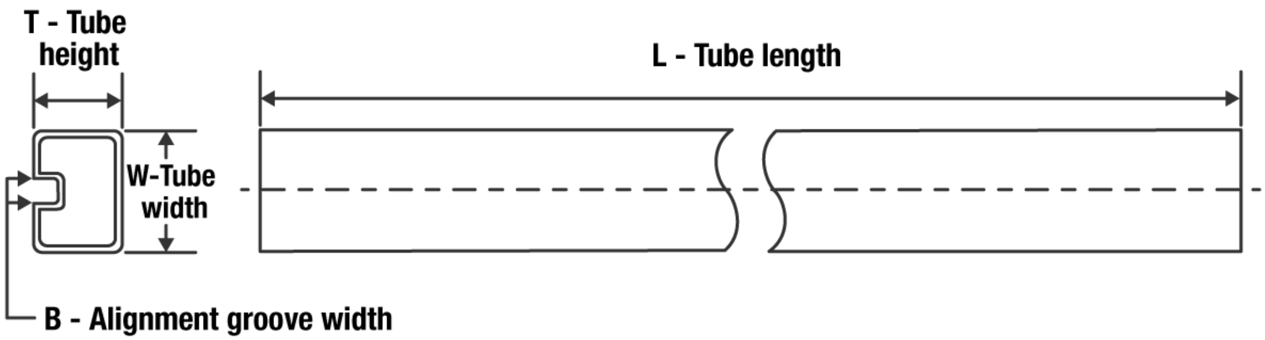
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

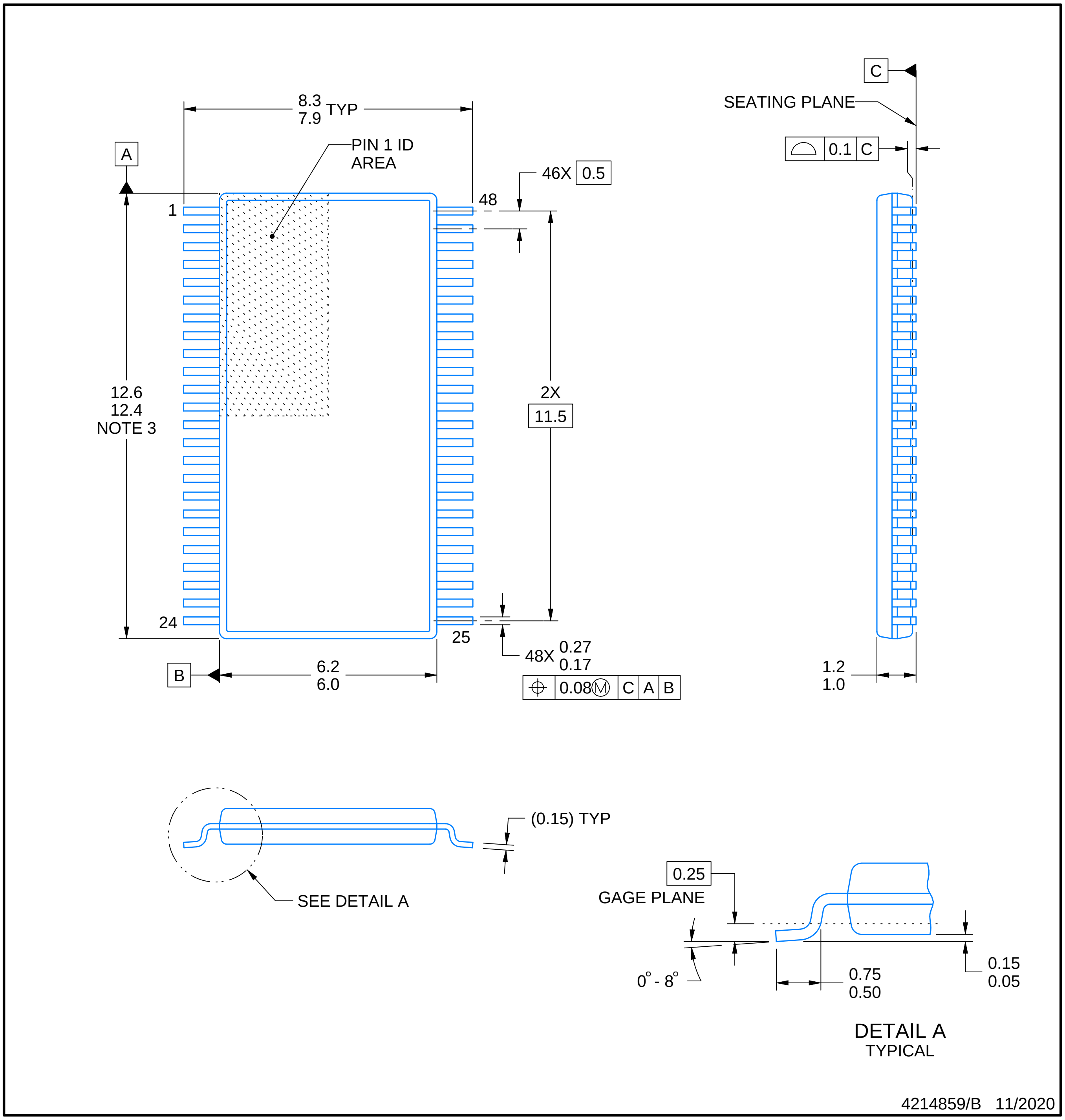
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS95DGGR	TSSOP	DGG	48	2000	350.0	350.0	43.0

TUBE



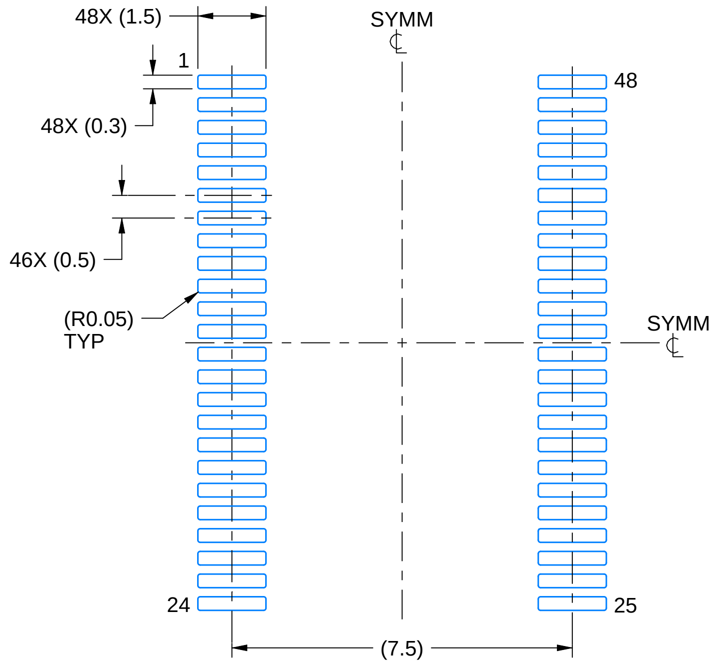
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS95DGG	DGG	TSSOP	48	40	530	11.89	3600	4.9
SN65LVDS95DGGG4	DGG	TSSOP	48	40	530	11.89	3600	4.9

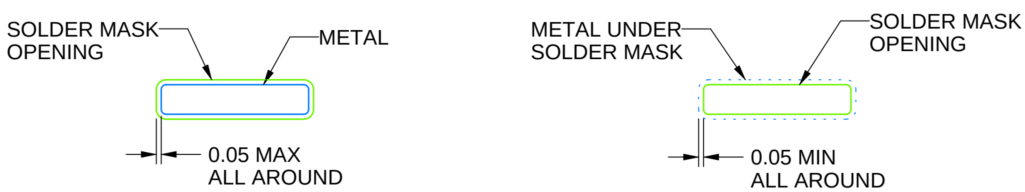


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED

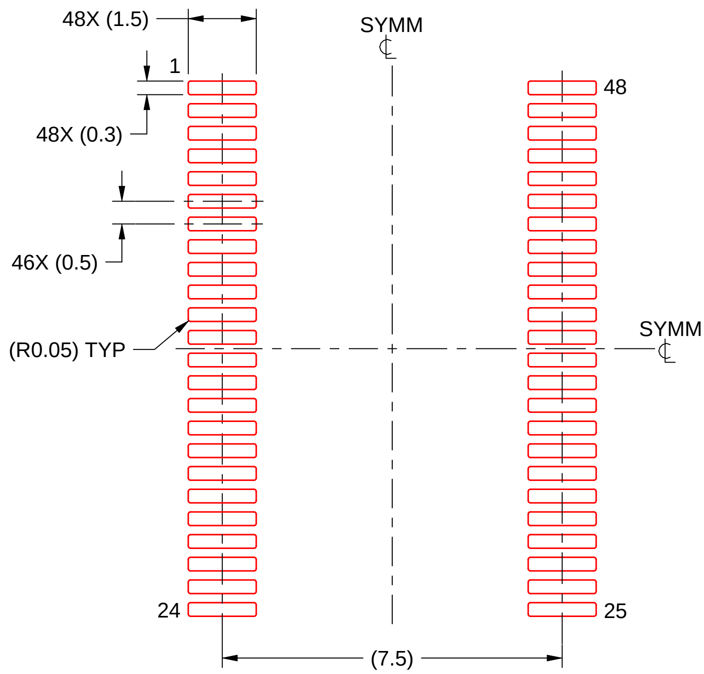
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

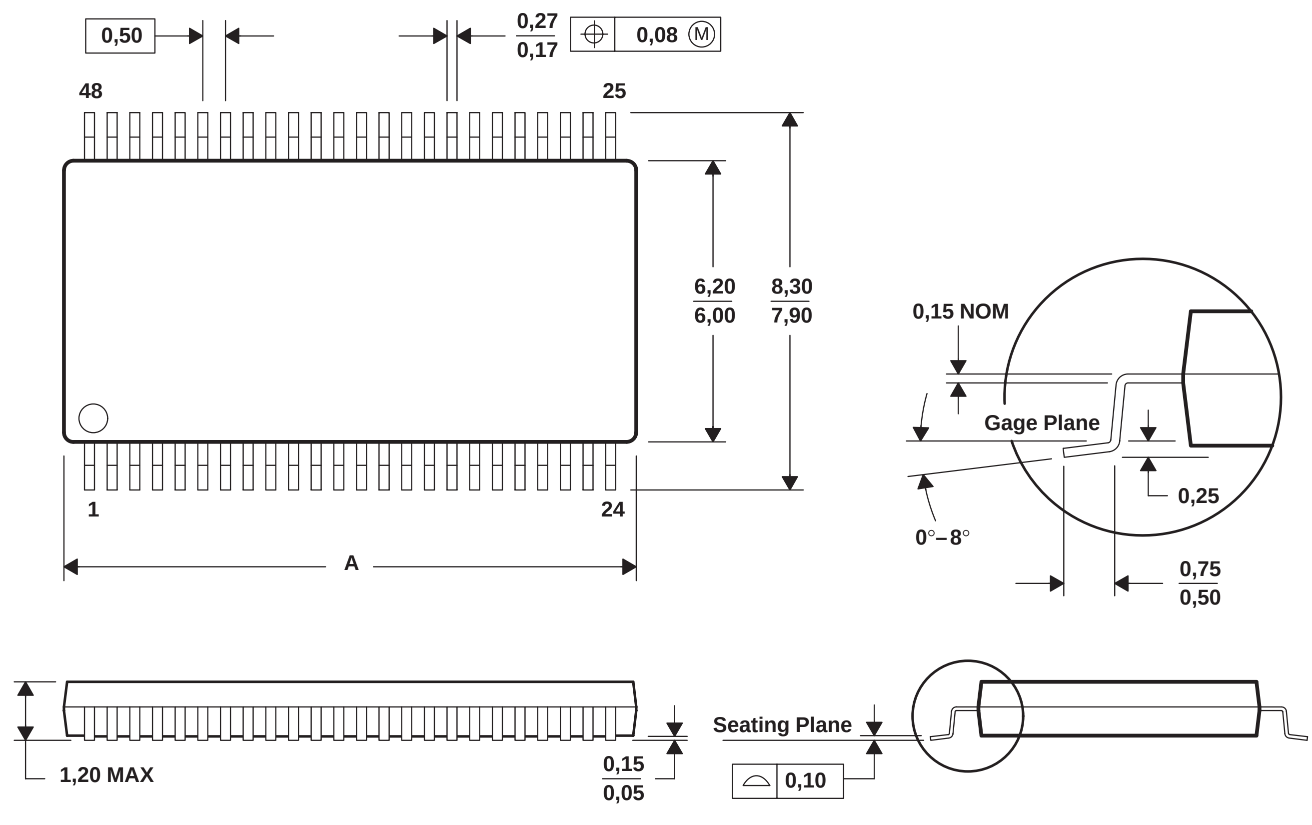
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153