# LMP848x 具有电压输出的高精度 76V 高侧电流感测放大器

## 1 特性

- 典型值：$T_A$ = 25°C
- 双向或单向感测
- 共模电压范围：4.0V 至 76V
- 电源电压范围：4.5V 至 76V
- 固定增益：20、60 和 100V/V
- 增益精度：±0.1%
- 偏移：±80µV
- 带宽 (−3dB)：270kHz
- 静态电流：小于 100µA
- 缓冲后的高电流输出：大于 5mA
- 输入偏置电流：7µA
- PSRR（直流）：122dB
- CMRR（直流）：124dB
- 温度范围：−40°C 至 125°C

## 2 应用

- 高侧电流感测
- 车辆电流测量
- 电信
- 电机控制
- 激光或发光二极管 (LED) 驱动器
- 电源管理
- 太阳能面板监控

## 3 说明

LMP8480 和 LMP8481 是精密的高侧电流感测放大器，可将作用于电流感测电阻两端较小的差分电压放大为高输入共模电压。这些放大器专为双向 (LMP8481) 或单向 (LMP8480) 电流 应用而设计， 并支持共模电压范围为 4V 至 76V 且带宽为 270kHz 的输入信号。由于工作电源电压范围与输入共模电压范围之间有重叠，因此 LMP848x 可由同一受监视的电压进行供电。该优势使得我们无需再将中间电源电压路由至电流正受监视的负载点，从而减少组件数并节省板空间。
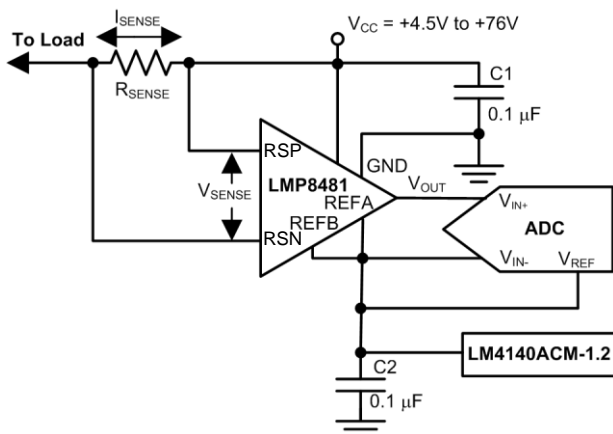
LMP848x 系列包含 20、60 和 100 等各种固定增益，适用于在各种温度下都需实现高精度的 应用 。低输入偏移电压允许在不影响系统误差的情况下使用较小的感应电阻器。凭借 −40°C 至 125°C 的宽工作温度范围，LMP848x 成为汽车、电信、工业和消费类 应用的理想之选。LMP8480 和 LMP8481 是 MAX4080 和 MAX4081 的引脚到引脚替代产品，可提升偏移电压、扩大基准调节范围并提高输出驱动能力。LMP8480 和 LMP8481 采用 8 引脚 VSSOP 封装。

### 器件信息[1]

| 器件型号 | 封装 | 封装尺寸（标称值） |
| --- | --- | --- |
| LMP8480 | VSSOP (8) | 3.00mm x 3.00mm |
| LMP8481 | VSSOP (8) | 3.00mm x 3.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路原理图



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## 目录

## 4 修订历史记录

**Changes from Revision D (April 2016) to Revision E** **Page**

• 已删除 删除了最后一个 特性 项目 ....................................................................................................................... 1
• Deleted LMP8480-H row from *Device Comparison Table* ................................................................................. 3
• Changed REFA to REFB and REFB to REFA for pins 6 and 7, respectively, in *Pin Functions* table ................... 3
• Deleted NCQ column from *Thermal Information* table ....................................................................................... 4
• Changed bidirectional to unidirectional is description of Figure 22 in *Basic Connections* section ...................... 13

**Changes from Revision C (September 2015) to Revision D** **Page**

• 更改了*典型应用原理图*：调换了 RSN 和 RSP 标签 ............................................................................................ 1
• Changed conditions of *Electrical Characteristics* table ...................................................................................... 5
• Added unit to R$_{OUT}$ parameter in *Electrical Characteristics* table ................................................................ 5
• Changed first paragraph of *Overview* section ................................................................................................... 10

**Changes from Revision B (December 2014) to Revision C** **Page**

• 已删除 删除了 LMP8480 和 LMP8481 的 WSON 封装选项 ................................................................................ 1
• Deleted -F version (50x gain) for LMP8480 and LMP8481 .................................................................................. 3
• Deleted WSON package options for LMP8480 and LMP8481 ............................................................................. 3

**Changes from Revision A (August 2012) to Revision B** **Page**

• 已添加 引脚配置和功能部分，*ESD* 额定值表，特性 说明 部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分 .................................................................. 1

# 5 Device Comparison Table

| DEVICE NAME | GAIN | POLARITY |
|---|---|---|
| LMP8480-T | x20 | Unidirectional |
| LMP8480-S | x60 | Unidirectional |
| LMP8481-T | x20 | Bidirectional or unidirectional |
| LMP8481-S | x60 | Bidirectional or unidirectional |
| LMP8481-H | x100 | Bidirectional or unidirectional |

# 6 Pin Configuration and Functions

**LMP8480 VSSOP Package**
**8 Pins**
**Top View**

| | | |
|---|---|---|
| $R_{SP}$ | 1 | 8 | $R_{SN}$ |
| $V_{CC}$ | 2 | 7 | NC |
| NC | 3 | 6 | NC |
| GND | 4 | 5 | $V_{OUT}$ |

LMP8480

**LMP8481 VSSOP Package**
**8 Pins**
**Top View**

| | | |
|---|---|---|
| RSP | 1 | 8 | RSN |
| $V_{CC}$ | 2 | 7 | REFA |
| NC | 3 | 6 | REFB |
| GND | 4 | 5 | $V_{OUT}$ |

LMP8481
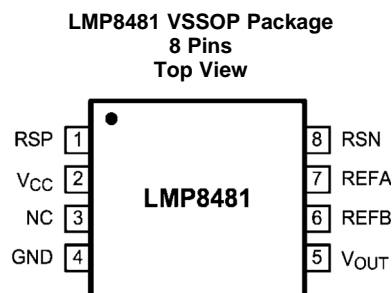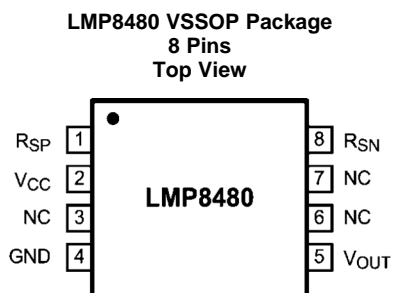
**Pin Functions**

| PIN NO. | PIN NAME | I/O | DESCRIPTION | |
|---|---|---|---|---|
| 1 | $R_{SP}$ | I | Positive current sense input | |
| 2 | VCC | P | Positive supply voltage | |
| 3 | NC | — | No connection – not internally connected | |
| 4 | GND | P | Ground | |
| 5 | $V_{OUT}$ | O | Output | |
| 6 | NC or REFB | I | LMP8480: no connection | LMP8481: reference voltage "B" input |
| 7 | NC or REFA | I | LMP8480: no connection | LMP8481: reference voltage "A" input |
| 8 | $R_{SN}$ | I | Negative current sense input | |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2][3]

|  | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage ($V_{CC}$ to GND) | | −0.3 | 85 | V |
| $R_{SP}$ or $R_{SN}$ to GND | | −0.3 | 85 | V |
| $V_{OUT}$ to GND | | −0.3 to the lesser of ($V_{CC}$ + 0.3) or +20 | | V |
| $V_{REF}$ pins (LMP8481 only) | Other $V_{REF}$ pin tied to ground | −0.3 | 12 | V |
| | Applied to both $V_{REF}$ pins tied together | −0.3 | 6 | |
| Differential input voltage | | −85 | 85 | V |
| Current into output pin | | −20[4] | 20 | mA |
| Current into any other pins | | −5[4] | 5 | mA |
| Operating temperature | | −40 | 125 | °C |
| Junction temperature | | -40 | 150 | °C |
| Storage temperature | | −65 | 150 | °C |

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation $P_{DMAX}$ = ($T_{J(MAX)}$ −$T_A$)/ $\theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(4) When the input voltage (VIN) at any pin exceeds power supplies (VIN < GND or VIN > VS ), the current at that pin must not exceed 5 mA, and the voltage (VIN) has to be within the *Absolute Maximum Ratings* for that pin. The 20-mA package input current rating limits the number of pins that can safely exceed the power supplies with current flow to four pins.

## 7.2 ESD Ratings

|  | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

Expected normal operating conditions over free-air temperature range (unless otherwise noted)[1]

|  | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage ($V_{CC}$) | | 4.5 | 76 | V |
| Common mode voltage | | 4.0 | 76 | V |
| Reference input (LMP8481 only) | $V_{REFA}$ and $V_{REFB}$ tied together | −0.3 to the lesser of ($V_{CC}$ − 1.5) or +6 | | V |
| | Single $V_{REF}$ pin with other $V_{REF}$ pin grounded | −0.3 or +12 where the average of the two $V_{REF}$ pins is less than the lesser of ($V_{CC}$ − 1.5) or +6 | | |

(1) Exceeding the *Recommended Operating Conditions* for extended periods of time may effect device reliability or cause parametric shifts.

## 7.4 Thermal Information

| THERMAL METRIC[1] | LMP8480, LMP8481 DGK (VSSOP) 8 PINS | UNIT |
|---|---|---|
| $R_{\theta JA}$  Junction-to-ambient thermal resistance | 185 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics

unless otherwise specified, all limits specified for at $T_A$ = 25°C, $V_{CC}$ = 4.5 V to 76 V, 4.5 V ≤ $V_{CM}$ ≤ 76 V, $R_L$ = 100 kΩ, $V_{SENSE}$ = ($V_{RSP} - V_{RSN}$) = 0 V[1]

| PARAMETER | | TEST CONDITIONS | | MIN[2] | TYP[3] | MAX[2] | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input offset voltage (RTI) | VCC = $V_{RSP}$ = 48 V, $\Delta V$ = 100 mV | $T_A$ = 25°C | | ±80 | ±265 | µV |
| | | | –40°C ≤ $T_A$ ≤ 125°C | | | ±900 | |
| $TCV_{OS}$ | Input offset voltage drift[4] | | | | ±6 | | µV°C |
| $I_B$ | Input bias current[5] | $V_{CC}$ = $V_{RSP}$ = 76 V, per input | | | 6.3 | | µA |
| | | $V_{CC}$ = $V_{RSP}$ = 76 V, per input, –40°C ≤ $T_A$ ≤ 125°C | | | | 12 | |
| $I_{LEAK}$ | Input leakage current | $V_{CC}$ = 0, $V_{RSP}$ = 86 V, both inputs together | | | 0.01 | | µA |
| | | $V_{CC}$ = 0, $V_{RSP}$ = 86 V, both inputs together, –40°C ≤ $T_A$ ≤ 125°C | | | | 2 | |
| $V_{SENSE(MAX)}$ | Differential input voltage across sense resistor[6] | $V_{CC}$ = 16 | -T version, –40°C ≤ $T_A$ ≤ 125°C | | | 667 | mV |
| | | | -F version, –40°C ≤ $T_A$ ≤ 125°C | | | 267 | |
| | | | -S version, –40°C ≤ $T_A$ ≤ 125°C | | | 222 | |
| | | | -H version, –40°C ≤ $T_A$ ≤ 125°C | | | 133 | |
| $A_V$ | Gain | -T version | | | 20 | | V/V |
| | | -T version, –40°C ≤ $T_A$ ≤ 125°C | | 19.8 | | 20.2 | |
| | | -S version | | | 60 | | |
| | | -S version, –40°C ≤ $T_A$ ≤ 125°C | | 59.5 | | 60.5 | |
| | | -H version | | | 100 | | |
| | | -H version, –40°C ≤ $T_A$ ≤ 125°C | | 99.2 | | 100.8 | |
| | Gain error | $V_{CC}$ = $V_{RSP}$ = 48 V | $T_A$ = 25°C | | | ±0.6% | |
| | | | –40°C ≤ $T_A$ ≤ 125°C | | | ±0.8% | |
| DC PSRR | DC power supply rejection ratio | $V_{RSP}$ = 48 V, $V_{CC}$ = 4.5 to 76 V | | | 122 | | dB |
| | | $V_{RSP}$ = 48 V, $V_{CC}$ = 4.5 to 76 V, –40°C ≤ $T_A$ ≤ 125°C | | 100 | | | |
| DC CMRR | DC common mode rejection ratio | $V_{CC}$ = 48 V, $V_{RSP}$ = 4.5 to 76 V | | | 124 | | dB |
| | | $V_{CC}$ = 48 V, $V_{RSP}$ = 4.5 to 76 V, –40°C ≤ $T_A$ ≤ 125°C | | 100 | | | |
| | | $V_{CC}$ = 48 V, $V_{RSP}$ = 4 V to 76 V | | | 124 | | |
| CMVR | Input common mode voltage range | CMRR > 100 dB, –40°C ≤ $T_A$ ≤ 125°C | | 4 | | 76 | V |
| $R_{OUT}$ | Output resistance / load regulation | $V_{SENSE}$ = 100 mV | | | 0.1 | | Ω |
| $V_{OMAX}$ | Maximum output voltage (headroom) ($V_{OMAX}$ = $V_{CC}$ – $V_{OUT}$) | $V_{CC}$ = 4.5 V, $V_{RSP}$ = 48 V, $V_{SENSE}$ = +1 V, $I_{OUT}$ (sourcing) 500 µA | | | 230 | 500 | mV |

(1)  *Electrical Characteristics* table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. **No** specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2)  All limits are specified by testing, design, or statistical analysis.
(3)  Typical values represent the most likely parametric norm at the time of characterization. Actual typical values can vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4)  Offset voltage temperature drift is determined by dividing the change in $V_{OS}$ at the temperature extremes by the total temperature change.
(5)  Positive bias current corresponds to current flowing into the device.
(6)  This parameter is specified by design and/or characterization and is not tested in production.

## Electrical Characteristics (continued)

unless otherwise specified, all limits specified for at $T_A$ = 25°C, $V_{CC}$ = 4.5 V to 76 V, 4.5 V ≤ $V_{CM}$ ≤ 76 V, $R_L$ = 100 kΩ, $V_{SENSE}$ = ($V_{RSP}$ − $V_{RSN}$) = 0 V[1]

| PARAMETER | | TEST CONDITIONS | MIN[2] | TYP[3] | MAX[2] | UNIT |
|---|---|---|---|---|---|---|
| $V_{OMIN}$ | Minimum output voltage | $V_{CC}$ = $V_{RSP}$ = 48 V, $V_{SENSE}$ = −1 V, $I_{OUT}$ (sinking) = 10 μA | | 3 | | mV |
| | | $V_{CC}$ = $V_{RSP}$ = 48 V, $V_{SENSE}$ = −1 V, $I_{OUT}$ (sinking) = 10 μA, −40°C ≤ $T_A$ ≤ 125°C | | | 15 | |
| | | $V_{CC}$ = $V_{RSP}$ = 4.5 V, $V_{SENSE}$ = −1 V, $I_{OUT}$ (sinking) = 10 μA | | 3 | | |
| | | $V_{CC}$ = $V_{RSP}$ = 48 V, $V_{SENSE}$ = −1 V, $I_{OUT}$ (sinking) = 100 μA | | 18 | | |
| | | $V_{CC}$ = $V_{RSP}$ = 48 V, $V_{SENSE}$ = −1 V, $I_{OUT}$ (sinking) = 100 μA, −40°C ≤ $T_A$ ≤ 125°C | | | 55 | |
| | | $V_{CC}$ = $V_{RSP}$ = 4.5 V, $V_{SENSE}$ = −1 V, $I_{OUT}$ (sinking) = 100 μA | | 18 | | |
| $V_{OLOAD}$ | Output voltage with load | $V_{CC}$ = 28 V, $V_{RSP}$ = 28 V, $V_{SENSE}$ = 600 mV, $I_{OUT}$ (sourcing) = 500 μA | | 12 | | V |
| $V_{OLREG}$ | Output load regulation | $V_{CC}$ = 20, $V_{RSP}$ = 16 V, $V_{OUT}$ = 12, $\Delta I_L$ = 200 nA to 8 mA | | 0.001% | | |
| $I_{CC}$ | Supply current | $V_{OUT}$ = 2 V, $R_L$ = 10 MΩ, $V_{CC}$ = $V_{RSP}$ = 76 V | | 88 | | μA |
| | | $V_{OUT}$ = 2 V, $R_L$ = 10 MΩ, $V_{CC}$ = $V_{RSP}$ = 76 V, −40°C ≤ $T_A$ ≤ 125°C | | | 155 | |
| BW | −3-dB bandwidth | $R_L$ = 10 MΩ, $C_L$ = 20 pF | | 270 | | kHz |
| SR | Slew rate[7] | $V_{SENSE}$ from 10 mV to 80 mV, $R_L$ = 10 MΩ, $C_L$ = 20 pF | | 1 | | V/μs |
| $e_{ni}$ | Input referred voltage noise | f = 1 kHz | | 95 | | nV/√Hz |
| $t_{SETTLE}$ | Output settling time to 1% of final value | $V_{SENSE}$ = 10 mV to 100 mV and 100 mV to 10 mV | | 20 | | μs |
| $t_{PU}$ | Power-up time | $V_{CC}$ = $V_{RSP}$ = 48 V, $V_{SENSE}$ = 100 mV, output to 1% of final value | | 50 | | μs |
| $t_{RECOVERY}$ | Saturation recovery time | Output settles to 1% of final value, the device does not experience phase reversal when overdriven | | 50 | | μs |
| $C_{LOAD}$ | Max output capacitance load | No sustained oscillations | | 500 | | pF |

(7)    The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

## 7.6 Typical Characteristics

unless otherwise specified, $T_A$ = 25°C, $V_{CC}$ = 4.5 V to 76 V, 4.5 V < $V_{CM}$ < 76 V, $R_L$ = 100 kΩ, $V_{SENSE}$ = ($V_{RSP}$ − $V_{RSN}$) = 0 V, for all gain options
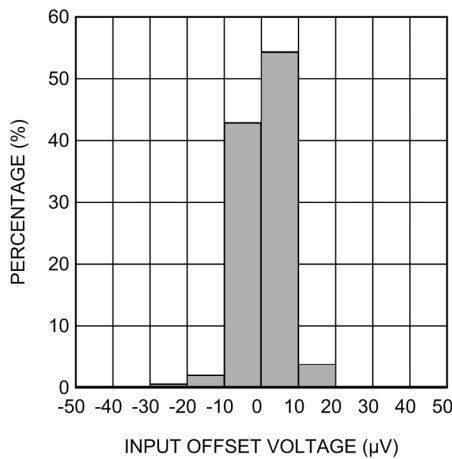

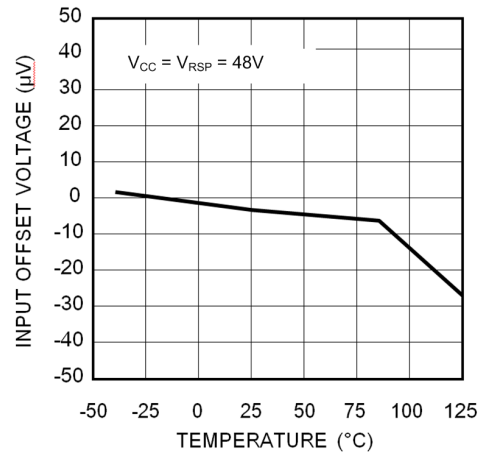
Figure 1. Offset Voltage Histogram

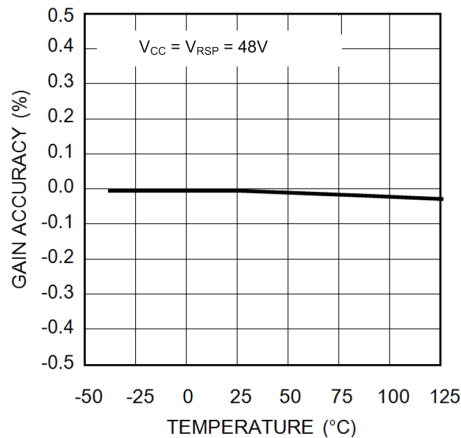

Figure 2. Typical Offset Voltage vs Temperature



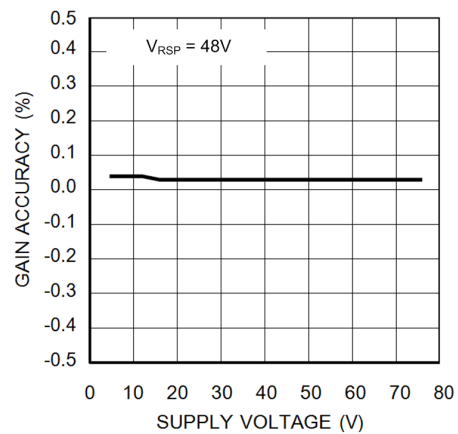Figure 3. Typical Gain Accuracy vs Temperature
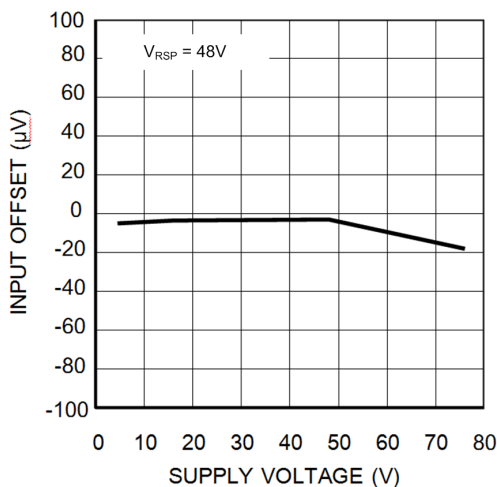


Figure 4. Typical Gain Accuracy vs Supply Voltage
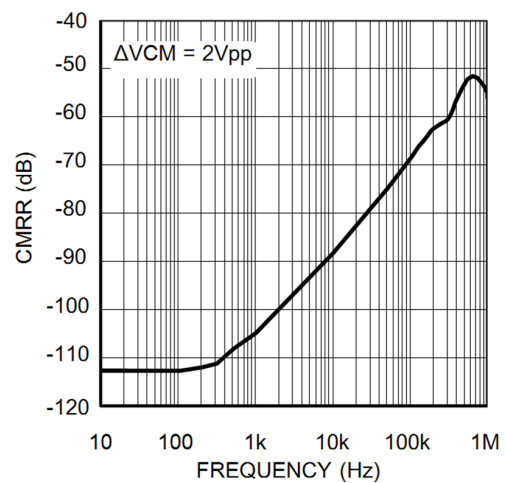


Figure 5. Typical Offset Voltage vs Supply Voltage



Figure 6. AC Common-Mode Rejection Ratio vs Frequency

## Typical Characteristics (continued)

unless otherwise specified, $T_A$ = 25°C, $V_{CC}$ = 4.5 V to 76 V, 4.5 V < $V_{CM}$ < 76 V, $R_L$ = 100 kΩ, $V_{SENSE}$ = ($V_{RSP}$ − $V_{RSN}$) = 0 V, for all gain options
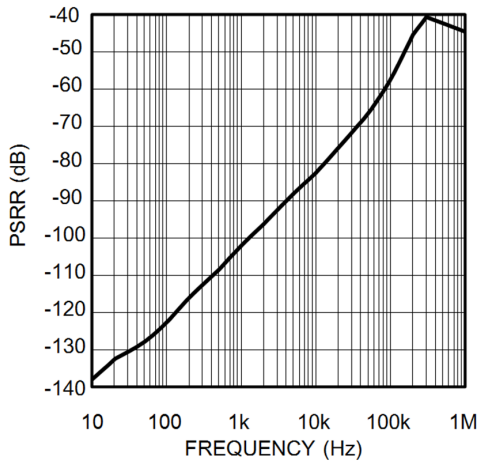


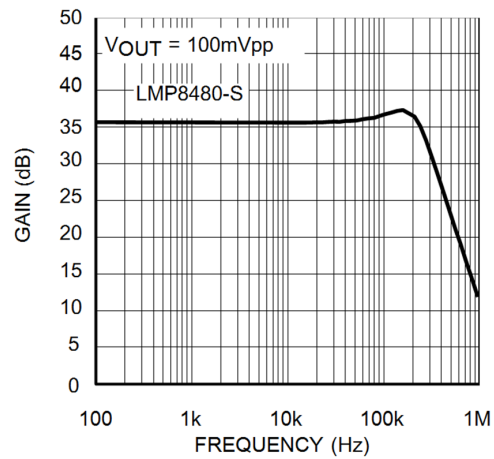Figure 7. AC Power Supply Rejection Ratio vs Frequency



Figure 8. Small Signal Gain vs Frequency
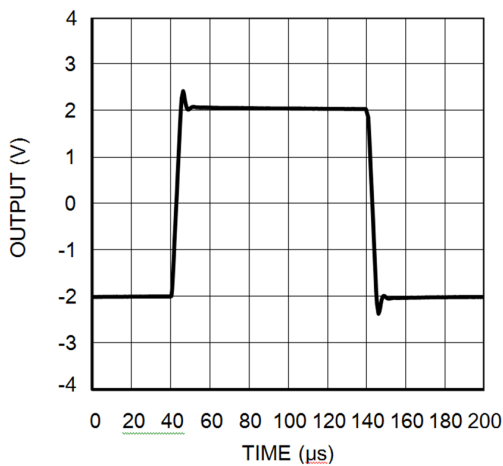


Figure 9. Large Signal Pulse Response
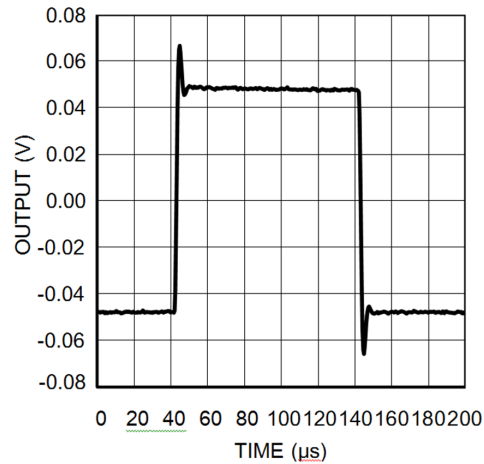


Figure 10. Small Signal Pulse Response
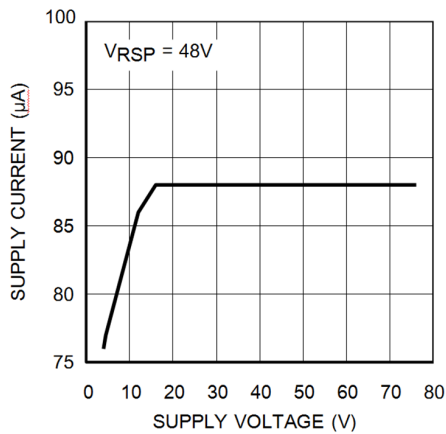


Figure 11. Supply Current vs Supply Voltage
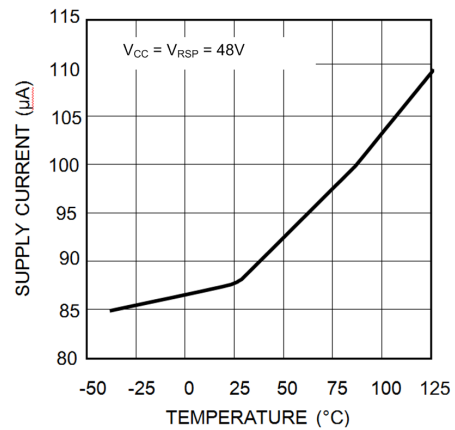


Figure 12. Supply Current vs Temperature

## Typical Characteristics (continued)

unless otherwise specified, $T_A$ = 25°C, $V_{CC}$ = 4.5 V to 76 V, 4.5 V < $V_{CM}$ < 76 V, $R_L$ = 100 kΩ, $V_{SENSE}$ = ($V_{RSP}$ − $V_{RSN}$) = 0 V, for all gain options
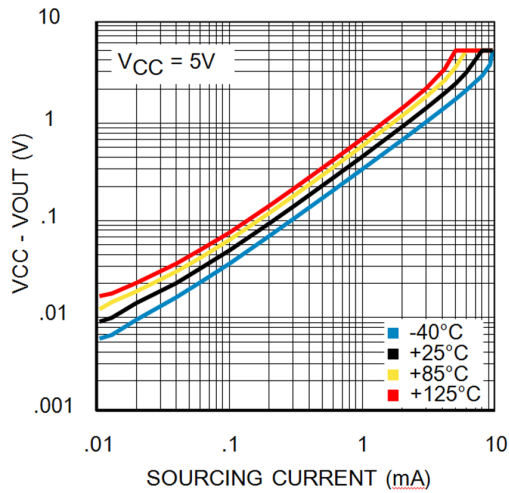


Figure 13. Saturated Output Sourcing Current at 4.5 V
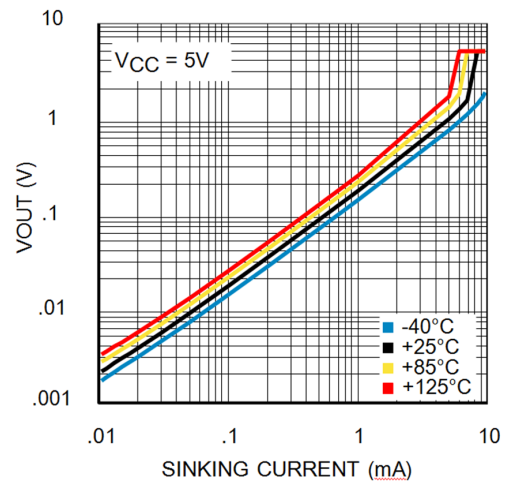


Figure 14. Saturated Output Sinking Current at 4.5 V
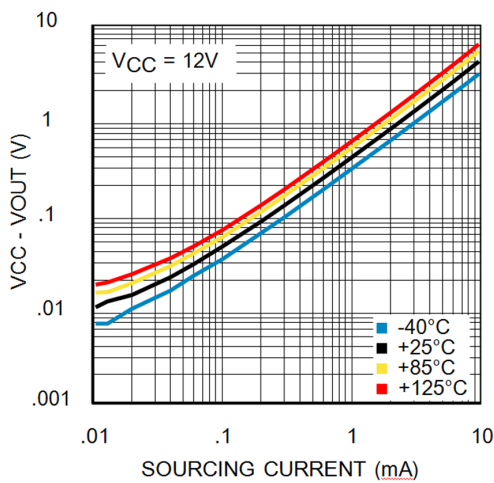


Figure 15. Saturated Output Sourcing Current at 12 V
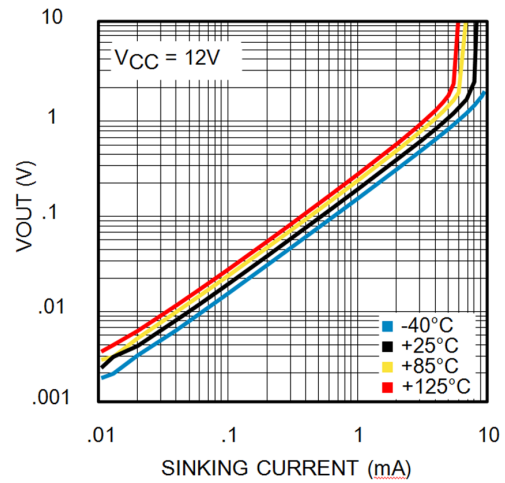


Figure 16. Saturated Output Current Sinking at 12 V

# 8 Detailed Description

## 8.1 Overview

The LMP8480 and LMP8481 are single-supply, high-side current sense amplifiers with available fixed gains of x20, x60 and x100. The power supply range is 4.5 V to 76 V, and the common-mode input voltage range is capable of 4.0-V to 76-V operation. The supply voltage and common-mode range are completely independent of each other, which causes the LMP848x supply voltage to be extremely flexible because the LMP848x supply voltage can be greater than, equal to, or less than the load source voltage, and allows the device to be powered from the system supply or the load supply voltage.

The LMP8480 and LMP8481 supply voltage does not have to be larger than the load source voltage. A 76-V load source voltage with a 5-V supply voltage is perfectly acceptable.

### 8.1.1 Theory of Operation

The LMP8480 and LMP8481 are comprised of two main stages. The first stage is a differential input current to voltage converter, followed by a differential voltage amplifier and level-shifting output stage. Also present is an internal 14-V low-dropout regulator (LDO) to power the amplifiers and output stage, as well as a reference divider resistor string to allow the setting of the reference level.

As Figure 18 illustrates, the current flowing through $R_{SENSE}$ develops a voltage drop called $V_{SENSE}$. The voltage across the sense resistor, $V_{SENSE}$, is then applied to the input $R_{SP}$ and $R_{SN}$ pins of the amplifier.

Internally, the voltage on each input pin is converted to a current by the internal precision thin-film input resistors $R_{GP}$ and $R_{GN}$. A second set of much higher value $V_{CM}$ sense resistors between the inputs provide a sample of the input common-mode voltage for internal use by the differential amplifier.

$V_{SENSE}$ is applied to the differential amplifier through $R_{GP}$ and $R_{GN}$. These resistors change the input voltage to a differential current. The differential amplifier then servos the resistor currents through the MOSFETs to maintain a zero balance across the differential amplifier inputs.

With no input signal present, the currents in $R_{GP}$ and $R_{GN}$ are equal. When a signal is applied to $V_{SENSE}$, the current through $R_{GP}$ and $R_{GN}$ are imbalanced and are no longer equal. The amplifier then servos the MOSFETS to correct this current imbalance, and the extra current required to balance the input currents is then reflected down into the two lower 400-kΩ *tail* resistors. The difference in the currents into the tail resistors is therefore proportional to the amplitude and polarity of $V_{SENSE}$. The tail resistors, being larger than the input resistors for the same current, then provide voltage gain by changing the current into a proportionally larger voltage. The gain of the first stage is then set by the tail resistor value divided by $R_G$ value.

The differential amplifier stage then samples the voltage difference across the two 400-kΩ tail resistors and also applies a further gain-of-five and output level-shifting according to the applied reference voltage ($V_{REF}$).

The resulting output of the amplifier will be equal to the differential input voltage times the gain of the device, plus any voltage value applied to the two VREF pins.

The resistor values in the schematic are ideal values for clarity and understanding. Table 1 shows the actual values used that account for parallel combinations and loading. This table can be used for calculating the effects of any additional external resistance.

The LMP8480 is identical to the LMP8481, except that both the $V_{REF}$ pins are grounded internally.

**Table 1. Actual Internal Resistor Values**

| GAIN OPTION | $R_{GP}$ AND $R_{GN}$ (Each) | $R_{VCMSENSE}$ (Each) | $R_{TAIL}$ (Each) | DIFFERENTIAL AMP FB (Each) | $V_{REFx}$ RESISTORS (Each) |
|---|---|---|---|---|---|
| 20x | 98.38 k | 491.9 k | 393.52 k | 1967.6 k | 98.38 k |
| 60x | 32.793 k | 172.165 k | 393.52 k | 1967.6 k | 98.38 k |
| 100x | 19.676 k | 98.38 k | 393.52 k | 1967.6 k | 98.38 k |

## 8.2   Functional Block Diagrams
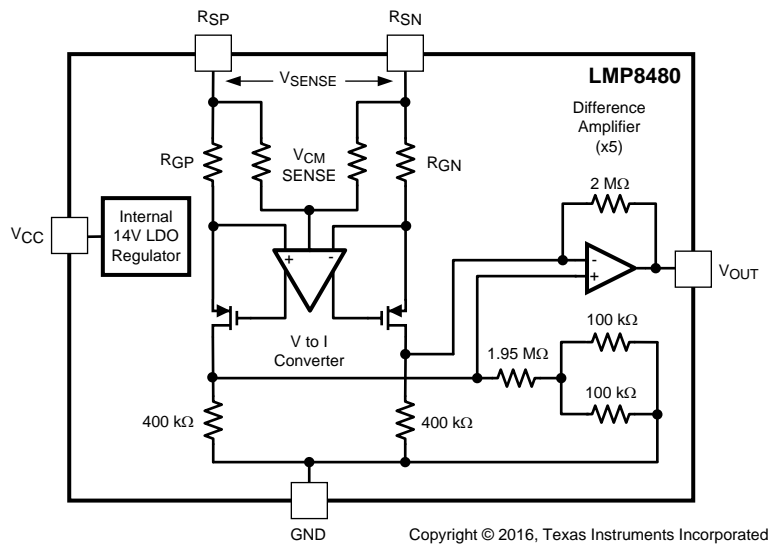


**Figure 17.   LMP8480 Block Diagram**
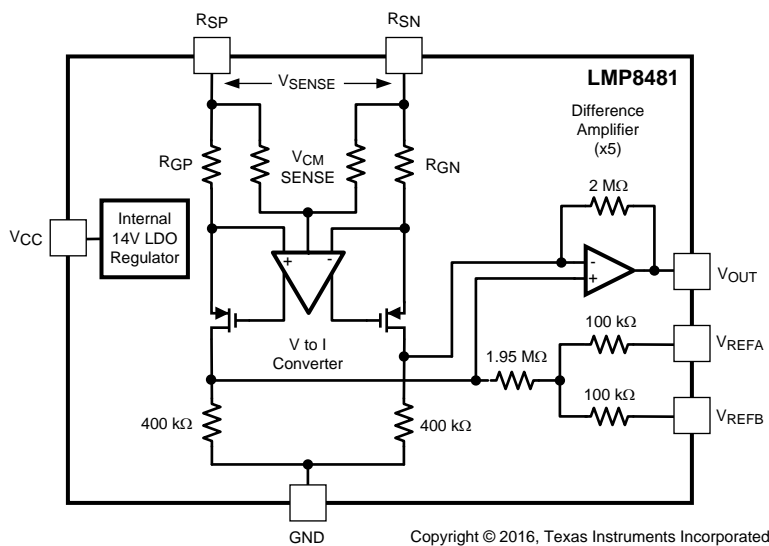


**Figure 18.   LMP8481 Block Diagram**

## 8.3 Feature Description

### 8.3.1 Basic Connections

Figure 19 through Figure 22 show the basic connections for several different configurations.

Figure 19 shows the basic connections for the LMP8480 for unidirectional applications. The output is at zero with zero sense voltage.
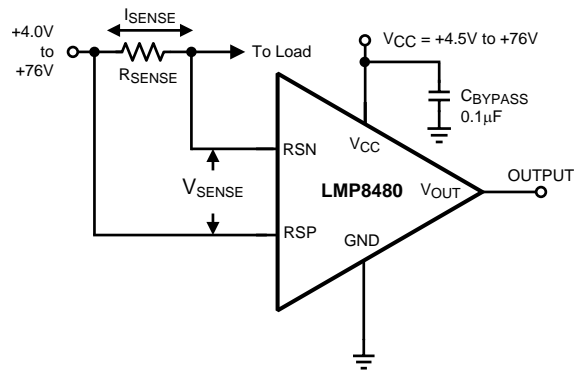


**Figure 19. LMP8480 Basic Connections (Unidirectional)**

Figure 20 shows the basic connections for the LMP8481 for bidirectional applications using an external reference input. At zero input voltage, the output is at the applied reference voltage ($V_{REF}$), moving positive or negative from the zero reference point.
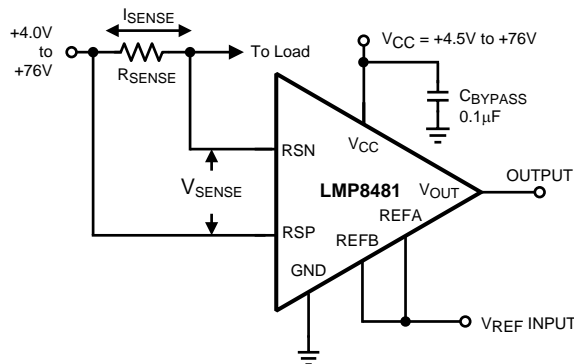


**Figure 20. LMP8481 Basic Connections for External 1:1 $V_{REF}$ Input (Bidirectional)**

Figure 21 shows the basic connections for the LMP8481 for bidirectional applications centering the output at one-half the applied $V_{REF}$ or $V_{CC}$ voltage. If $V_{REFA}$ is connected to $V_{CC}$, then the output zero point is $V_{CC}$ / 2. If $V_{REFA}$ is connected to the ADC $V_{REF}$ line, then the zero output is at mid-scale for the ADC.
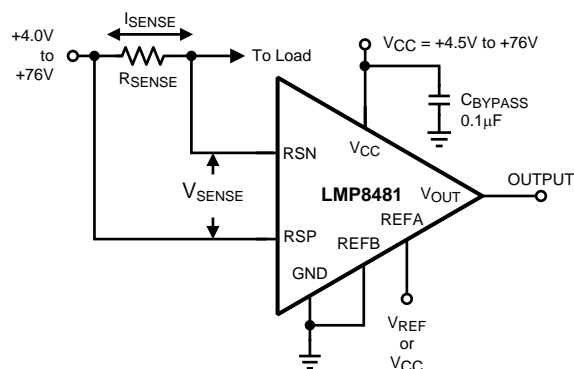


**Figure 21. LMP8481 Basic Connections for Mid-Bias ($V_{REF}$ / 2) Input (Bidirectional)**

# Feature Description (continued)

Figure 22 shows the how to connect the LMP8481 for unidirectional applications, thus making the LMP8481 equivalent to the LMP8480 in Figure 19.
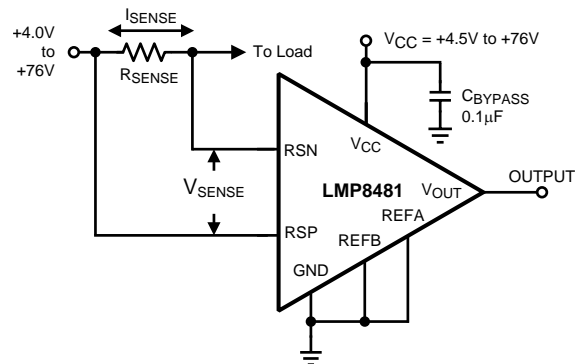


**Figure 22. LMP8481 Connections for Unidirectional Configuration (Equivalent to LMP8480 Unidirectional)**

### 8.3.2  Selection of the Sense Resistor

The accuracy of the current measurement depends heavily on the accuracy of the shunt resistor $R_{SENSE}$. The value of $R_{SHUNT}$ depends on the application and is a compromise between small-signal accuracy, maximum permissible voltage drop, and allowable power dissipation in the current measurement circuit.

The use of a 4-terminal or Kelvin sense resistor is highly recommended; see the *Layout Guidelines* section.

For best results, the value of the resistor is calculated from the maximum expected load current $I_{LMAX}$ and the expected maximum output swing $V_{OUTMAX}$, plus a few percent of headroom. See the *Maximum Output Voltage* section for details about the maximum output voltage limits.

High values of $R_{SENSE}$ provide better accuracy at lower currents by minimizing the effects of amplifier offset. Low values of $R_{SENSE}$ minimize load voltage loss, but at the expense of accuracy at low currents. A compromise between low current accuracy and load circuit losses must generally be made.

The maximum $V_{SENSE}$ voltage that must be generated across the $R_{SENSE}$ resistor is shown in Equation 1:

$$V_{SENSE} = V_{OUTMAX} / A_V \tag{1}$$

> **NOTE**
> The maximum $V_{SENSE}$ voltage must be no more than 667 mV.

From this maximum $V_{SENSE}$ voltage, the $R_{SENSE}$ value can be calculated from Equation 2:

$$R_{SENSE} = V_{SENSE} / I_{LMAX} \tag{2}$$

Take care not exceed the maximum power dissipation of the resistor. The maximum sense resistor power dissipation is shown in Equation 3:

$$P_{RSENSE} = V_{SENSE} \times I_{LMAX} \tag{3}$$

Using a 2-3x minimum safety margin is recommended in selecting the power rating of the resistor.

### 8.3.3  Using PCB Traces as Sense Resistors

While it may be tempting to use a known length of PCB trace resistance as a sense resistor, it is not recommended.

The temperature coefficient of copper is typically 3300-4000 ppm/°K, and can vary over PCB process variations and require measurement correction (possibly requiring ambient temperature measurements).

A typical surface mount sense resistor tempco is in the 50 ppm to 500 ppm/°C range offering more measurement consistency and accuracy over the copper trace. Special low-tempco resistors are available in the 0.1 to 50 ppm range, but at a higher cost.

## Feature Description (continued)

### 8.3.4 $V_{REFA}$ and $V_{REFB}$ Pins (LMP8481 Only)

The voltage applied to the $V_{REFA}$ and $V_{REFB}$ pins controls the output zero reference level. Depending on how the pins are configured, the output reference level can be set to GND, or $V_{CC}$ / 2, or external $V_{REF}$ / 2, or the average of two different input references.

The reference inputs consist of a pair of divider resistors with equal values to a common summing point, $V_{REF}$', as shown in Figure 23. Assuming $V_{SENSE}$ is zero, the output is at the same value as $V_{REF}$'.
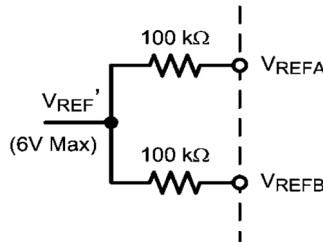


**Figure 23. $V_{REF}$ Input Resistor Network**

$V_{REF}$' is the voltage at the resistor tap-point that is directly applied to the output as an offset. With the two $V_{REF}$ inputs tied together, the output zero voltage has a 1:1 ratio relationship with $V_{REF}$.

$$V_{OUT} = ( (V_{RSP} - V_{RSN}) \times Av ) + V_{REF'} \tag{4}$$

Where:

$$V_{REF'} = V_{REFA} = V_{REFB} \text{ (Equal Inputs)} \tag{5}$$

or:

$$V_{REF'} = ( V_{REFA} + V_{REFB} ) / 2 \text{ (Different Inputs)} \tag{6}$$

### *8.3.4.1 One-to-One (1:1) Reference Input*

To directly set the reference level, the two inputs are connected to the external reference voltage. The applied $V_{REF}$ is reflected 1:1 on the output, as shown in Figure 24.
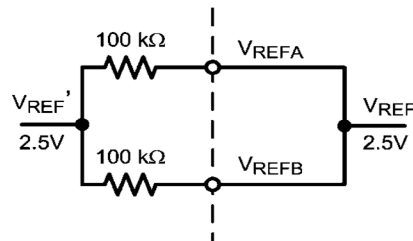


**Figure 24. Applying 1:1 Direct Reference Voltage**

## Feature Description (continued)

### 8.3.4.2 Setting Output to One-Half $V_{CC}$ or external $V_{REF}$

For mid-range operation, $V_{REFB}$ must be tied to ground and $V_{REFA}$ can be tied to $V_{CC}$ or an external A/D reference voltage. The output is set to one-half the reference voltage. For example, a 5-V reference results in a 2.5-V output zero reference.
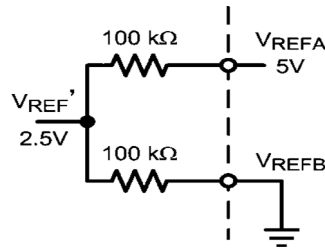


**Figure 25. Applying a Divided Reference Voltage**

$$V_{REF'} = (V_{REFA} - V_{REFB}) / 2 \tag{7}$$

When the reference pins are biased at different voltages, the output is referenced to the average of the two applied voltages.

The reference pins must always be driven from clean, stable sources, such as A/D reference lines or clean supply lines. Any noise or drifts on the reference inputs are directly reflected in the output. Take care if the power supply is used as the reference source so as to not introduce supply noise, drift or sags into the measurement.

Different resistor divider ratios can be set by adding external resistors in series with the internal 100-kΩ resistors, though the temperature coefficient (tempco) of the external resistors may not tightly track the internal resistors and there are slight errors over temperature.

The LMP8480 is identical to the LMP8481, except that both the $V_{REF}$ pins are grounded internally. The LMP8481 can replace the LMP8480 if both $V_{REF}$ pins are grounded.

### 8.3.5 Reference Input Voltage Limits (LMP8481 Only)

The maximum voltage on either reference input pin is limited to VCC or 12 V, whichever is less.

The average voltage on the two $V_{REF}$ pins, and thus the actual output reference voltage level, is limited to a maximum of 1.5 V below VCC, or 6 V, whichever is less. Beware that supply voltages of less than 7.5 V have a diminishing $V_{REF}$ maximum.

Both $V_{REFA}$ and $V_{REFB}$ can both be grounded to provide a ground referenced output (thus functionally duplicating the LMP8480).

Note that there can be a dynamic error in the $V_{REF}$ to output level matching of up to 100 µV/V. Normally this error is not an issue for fixed references, but if the reference voltage is dynamically adjusted during operation, this error must be taken into account during calibration routines. This error varies in both amplitude and polarity part-to-part, but the slope is generally linear.

### 8.3.6 Low-Side Current Sensing

The LMP8480 and LMP8481 are not recommended for low-side current sensing at ground level. The voltage on either input pin must be a minimum of 4.0 V above the ground pin for proper operation. The output level may not be valid for common-mode voltages below 4 V. This minimum voltage requirement must be taken into consideration for monitoring or feedback applications where the load-supply voltage can dip below 4 V or be switched completely off.

## Feature Description (continued)

### 8.3.7 Input Series Resistance

Because the input stage uses precision resistors to convert the voltage on the input pin to a current, any resistance added in series with the input pins changes the gain. If a resistance is added in series with an input, the gain of that input does not track that of the other input, causing a constant gain error.

TI does not recommend using external resistances to alter the gain because external resistors do not have the same thermal matching as the internal thin film resistors.

If resistors are purposely added for filtering, resistance must be added equally to both inputs and the user must be aware that the gain changes slightly. See the end of the *Theory of Operation* section for the internal resistor values. External resistances must be kept below 10 Ω.

### 8.3.8 Minimum Output Voltage

The amplifier output cannot swing to exactly 0 V. There is always a minimum output voltage set by the output transistor saturation and input offset errors. This voltage creates a minimum output swing around the zero current reading resulting from the output saturation. The user must be aware of this output swing when designing any servo loops or data acquisition systems that may assume 0 V = 0 A. If a true zero is required, use the LMP8481 with a VREF set slightly above ground (> 50 mV); see the *Swinging Output Below Ground* section for a possible solution to this issue.

### 8.3.9 Swinging Output Below Ground

If a negative supply is available, a pulldown resistor can be added from the output to the negative voltage to allow the output to swing a few millivolts below ground. Adding a pulldown resistor allows the ADC to resolve true zero and recover codes that normally are lost to the negative output saturation limit.
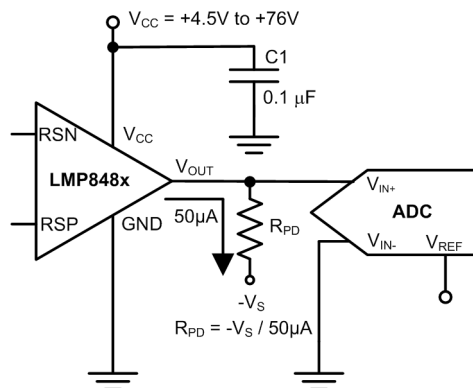


**Figure 26. Output Pulldown Resistor Example**

A minimum of 50 µA must be sourced (pulled) from the output to a negative voltage. The pulldown resistor can be calculated from:

$$R_{PD} = -V_S / 50 \text{ µA} \tag{8}$$

For example, if a −5-V supply is available, use a pulldown resistor of 5 V / 50 µA = 100 kΩ. Adding this resistor allows the output to swing to approximately 10 mV below ground.

This technique can also reduce the maximum positive swing voltage. Do not forget to include the parallel loading effects of the pulldown any output load. Exceeding −100 mV on the output is not recommended. Source currents greater than 100 µA must be avoided to prevent self-heating at high-supply voltages. Pulldown resistor values must not be so low as to heavily load the output during positive output excursions. This mode of operation is not directly specified and is not ensured.

## Feature Description (continued)

### 8.3.10 Maximum Output Voltage

The LMP8481 has an internal precision 14-V low-dropout regulator that limits the maximum amplifier output swing to approximately 250 mV below $V_{CC}$ or 13.7 V (whichever is less). This regulator effectively clamps the maximum output to slightly less than 13.7 V even with a $V_{CC}$ greater than 14 V; see *Typical Application With a Resistive Divider* section for more information.

## 8.4 Device Functional Modes

### 8.4.1 Unidirectional vs Bidirectional Operation

Unidirectional operation is where the load current only flows in one direction ($V_{SENSE}$ is always positive). Application examples are PA monitoring, non-inductive load monitoring, and laser or LED drivers. Unidirectional operation allows the output zero reference to be true zero volts on the output. The LMP8480 is designed for unidirectional applications where the setting of VREF is not required; see the *Unidirectional Application With the LMP8480* section for more details.

Bidirectional operation is where the load current can flow in both directions ($V_{SENSE}$ can be positive or negative). Application examples are battery-charging or regenerative motor monitoring. The LMP8481 is designed for bidirectional applications and has a pair of VREF pins to allow the setting of the output zero reference level ($V_{REF}$); see the *Unidirectional Application With the LMP8480* section for more details.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The LMP848x amplifies the voltage developed across a current-sensing resistor when current passes through it. Flexible offset inputs allow adjusting the functionality of the output for multiple configurations, as discussed throughout this section.

### 9.1.1 Input Common-Mode and Differential Voltage Range

The input common-mode range, where common-mode range is defined as the voltage from ground to the voltage on $R_{SP}$ input, must be in the range of 4.0 V to 76 V. Operation below 4.0 V on either input pin introduces severe gain error and nonlinearities.

The maximum differential voltage (defined as the voltage difference between $R_{SP}$ and $R_{SN}$) must be 667 mV or less. The theoretical maximum input is 700 mV (14 V / 20).

Taking the inputs below 4 V does not damage the device, but the output conditions during this time are not predictable and are not ensured.

If the load voltage (Vcm) is expected to fall below 4 V as part of normal operation, preparations must be made for invalid output levels during this time.

## 9.2 Typical Applications

### 9.2.1 Unidirectional Application With the LMP8480
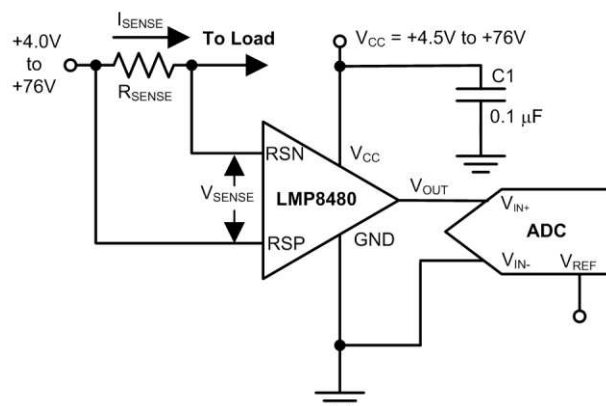


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**Figure 27. Unidirectional Application with the LMP8480**

#### 9.2.1.1 Design Requirements

The LMP8480 is designed for unidirectional current sense applications. The output of the amplifier is equal to the differential input voltage times the fixed device gain.

#### 9.2.1.2 Detailed Design Procedure

The output voltage can be calculated from Equation 9:

$$\text{VOUT} = (\,(V_{RSP} - V_{RSN}) \times Av\,) \tag{9}$$

## Typical Applications (continued)

Note that the minimum zero reading is limited by the lower output swing and input offset. The LMP8480 is functionally identical to the LMP8481, but with the $V_{REFA}$ and $V_{REFB}$ nodes grounded internally. The LMP8481 can replace the LMP8480 if both the $V_{REF}$ inputs (pins 6 and 7) are grounded.

### 9.2.1.3 Application Curve
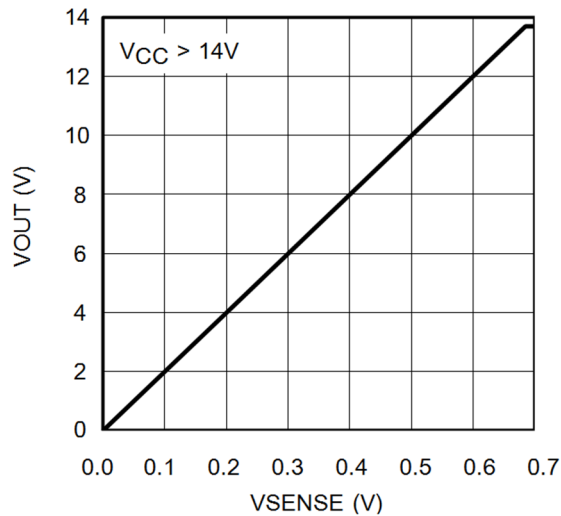


**Figure 28. Unidirectional Transfer Function for Gain-of-20 Option**

### 9.2.2 Bidirectional Current Sensing Using the LMP8481
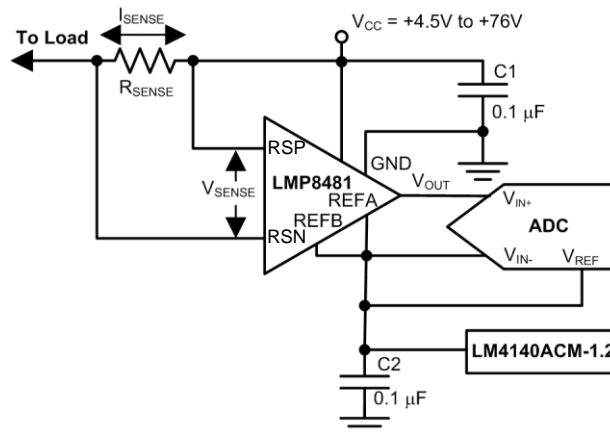


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**Figure 29. Bidirectional Current Sensing Using the LMP8481**

#### 9.2.2.1 Design Requirements

Bidirectional operation is required where the measured load current can be positive or negative. Because $V_{SENSE}$ can be positive or negative, and the output cannot swing negative, the zero output level must be level-shifted above ground to a known zero reference point. The LMP8481 allows for the setting this reference point.

## Typical Applications (continued)

### 9.2.2.2 *Detailed Design Procedure*

The $V_{REFA}$ and $V_{REFB}$ pins set the zero reference point. The output zero reference point is set by applying a voltage to the REFA and REFB pins; see the *Unidirectional Application With the LMP8480* section. The *$V_{REFA}$ and $V_{REFB}$ Pins (LMP8481 Only)* section describes the output transfer function with a 1.2-V reference applied to the gain-of-20 option.

### 9.2.2.3 *Application Curve*
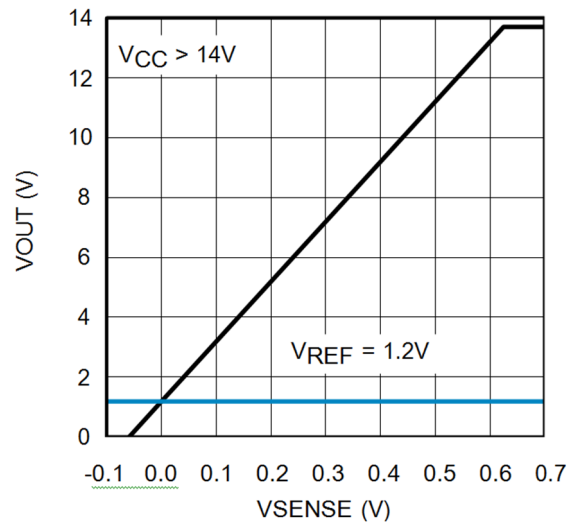


**Figure 30. Bidirectional Transfer Function Using a 1.2-V Reference Voltage**

### 9.2.3 Typical Application With a Resistive Divider

Take care if the output is driving an A/D input with a maximum A/D maximum input voltage lower than the amplifier supply voltage because the output can swing higher than the planned load maximum resulting from input transients or shorts on the load and overload or possibly damage the A/D input.

A resistive attenuator, as shown in Figure 31, can be used to match the maximum swing to the input range of the A/D converter.
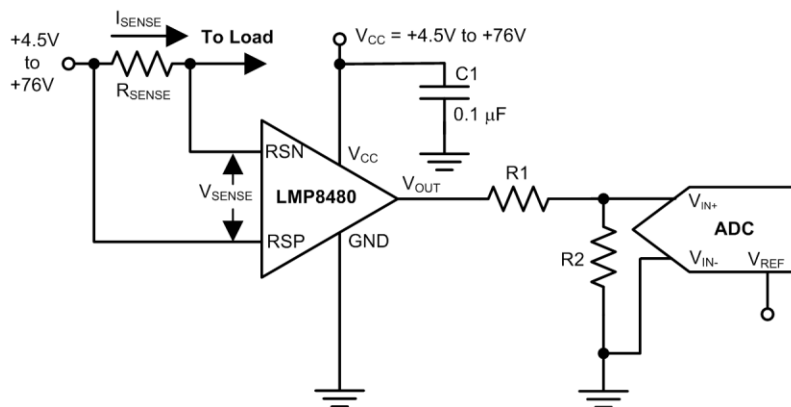
**Figure 31. Typical Application With Resistive Divider Example**

# 10   Power Supply Recommendations

## 10.1   Power Supply Decoupling

In order to decouple the LMP848x from ac noise on the power supply, TI recommends using a 0.1-μF bypass capacitor between the $V_{CC}$ and GND pins. This capacitor must be placed as close as possible to the supply pins. In some cases, an additional 10-μF bypass capacitor can further reduce the supply noise.

Do not forget that these bypass capacitors must be rated for the full supply and load source voltage. TI recommends that the working voltage of the capacitor (WVDC) be at least two times the maximum expected circuit voltage.

# 11   Layout

## 11.1   Layout Guidelines

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors (< 100 mΩ), any trace resistance shared with the load current can cause significant errors.

The amplifier inputs must be directly connected to the sense resistor pads using Kelvin or 4-wire connection techniques. The traces must be one continuous piece of copper from the sense resistor pad to the amplifier input pin pad, and ideally on the same copper layer with minimal vias or connectors. These recommendations can be important around the sense resistor if any significant heat gradients are being generated.

To minimize noise pickup and thermal errors, the input traces must be treated as a differential signal pair and routed tightly together with a direct path to the input pins. The input traces must be run away from noise sources, such as digital lines, switching supplies or motor drive lines. Remember that these traces can contain high voltage, and must have the appropriate trace routing clearances.

Because the sense traces only carry the amplifier bias current (approximately 7 μA at room temperature), the connecting input traces can be thinner, signal level traces. Excessive resistance in the trace must also be avoided.

The paths of the traces must be identical, including connectors and vias, so that these errors are equal and cancel.

The sense resistor heats up when the load increases. When the resistor heats up, the resistance generally goes up, which causes a change in the readings. The sense resistor must have as much heatsinking as possible to remove this heat through the use of heatsinks or large copper areas coupled to the resistor pads. A reading drifting over time after turn-on can usually be traced back to sense resistor heating.

## 11.2   Layout Example
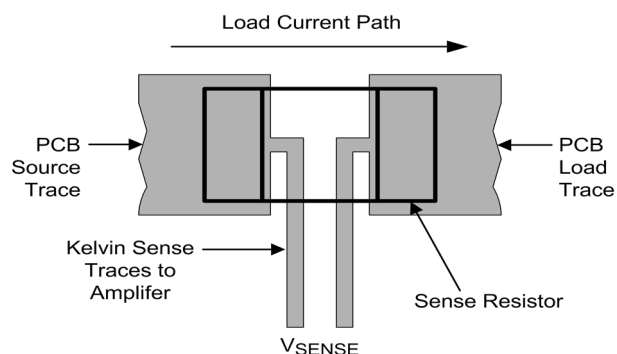


**Figure 32.  Kelvin or 4−Wire Connection to the Sense Resistor**

## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 开发支持

*LMP8480/1 PSPICE 模型*

*LMP8480/1 TINA 参考设计*

《基于 SPICE 的 TINA-TI 模拟仿真程序》

LMP8480/1 评估板产品页面

*LMP8480/1 评估板手册*

### 12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 **2.** 相关链接

| 器件 | 产品文件夹 | 立即订购 | 技术文档 | 工具和软件 | 支持和社区 |
|---|---|---|---|---|---|
| LMP8480 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| LMP8481 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

### 12.3 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

### 12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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### 12.5 商标

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### 12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMP8480MM-T/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AV8A | Samples |
| LMP8480MME-S/NOPB | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AY8A | Samples |
| LMP8480MME-T/NOPB | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AV8A | Samples |
| LMP8480MMX-S/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AY8A | Samples |
| LMP8480MMX-T/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AV8A | Samples |
| LMP8481MM-H/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AH9A | Samples |
| LMP8481MM-S/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AA9A | Samples |
| LMP8481MM-T/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AT9A | Samples |
| LMP8481MME-H/NOPB | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AH9A | Samples |
| LMP8481MME-S/NOPB | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AA9A | Samples |
| LMP8481MME-T/NOPB | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AT9A | Samples |
| LMP8481MMX-H/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AH9A | Samples |
| LMP8481MMX-S/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AA9A | Samples |
| LMP8481MMX-T/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | AT9A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMP8480MM-T/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8480MME-S/NOPB | VSSOP | DGK | 8 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8480MME-T/NOPB | VSSOP | DGK | 8 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8480MMX-S/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8480MMX-T/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8481MM-H/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8481MM-S/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8481MM-T/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8481MME-H/NOPB | VSSOP | DGK | 8 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8481MME-S/NOPB | VSSOP | DGK | 8 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8481MME-T/NOPB | VSSOP | DGK | 8 | 250 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8481MMX-H/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8481MMX-S/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMP8481MMX-T/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMP8480MM-T/NOPB | VSSOP | DGK | 8 | 1000 | 208.0 | 191.0 | 35.0 |
| LMP8480MME-S/NOPB | VSSOP | DGK | 8 | 250 | 208.0 | 191.0 | 35.0 |
| LMP8480MME-T/NOPB | VSSOP | DGK | 8 | 250 | 208.0 | 191.0 | 35.0 |
| LMP8480MMX-S/NOPB | VSSOP | DGK | 8 | 3500 | 356.0 | 356.0 | 35.0 |
| LMP8480MMX-T/NOPB | VSSOP | DGK | 8 | 3500 | 356.0 | 356.0 | 35.0 |
| LMP8481MM-H/NOPB | VSSOP | DGK | 8 | 1000 | 208.0 | 191.0 | 35.0 |
| LMP8481MM-S/NOPB | VSSOP | DGK | 8 | 1000 | 208.0 | 191.0 | 35.0 |
| LMP8481MM-T/NOPB | VSSOP | DGK | 8 | 1000 | 208.0 | 191.0 | 35.0 |
| LMP8481MME-H/NOPB | VSSOP | DGK | 8 | 250 | 208.0 | 191.0 | 35.0 |
| LMP8481MME-S/NOPB | VSSOP | DGK | 8 | 250 | 208.0 | 191.0 | 35.0 |
| LMP8481MME-T/NOPB | VSSOP | DGK | 8 | 250 | 208.0 | 191.0 | 35.0 |
| LMP8481MMX-H/NOPB | VSSOP | DGK | 8 | 3500 | 356.0 | 356.0 | 35.0 |
| LMP8481MMX-S/NOPB | VSSOP | DGK | 8 | 3500 | 356.0 | 356.0 | 35.0 |
| LMP8481MMX-T/NOPB | VSSOP | DGK | 8 | 3500 | 356.0 | 356.0 | 35.0 |

## DGK (S−PDSO−G8)　　　　PLASTIC SMALL−OUTLINE PACKAGE

0,65

8

5

0,38
0,25

⊕ 0,13 Ⓜ

D▷ 3,10
2,90

5,05
4,75

1

4

C▷

3,10
2,90

0,23
0,13

Gauge Plane

0°−8°

0,25

0,70
0,40

1,10 MAX

0,15
0,05

Seating Plane

⌒ 0,10

4073329/E 05/06

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　C▷ Body length does not include mold flash, protrusions, or gate burrs.　Mold flash, protrusions, or gate burrs shall
　　　　　　not exceed 0.15 per end.
　　　D▷ Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
　　　　　E.　Falls within JEDEC MO−187 variation AA, except interlead flash.

DGK (S–PDSO–G8)                    PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

├──┤(0,65)TYP.

8
5
(4,4)

PKG
C̶

1
4

PKG
C̶

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

├── (0,45)

(1,45)

├──┤(0,05)
All Around

Pad Geometry
(See Note C)

8X(0,45) ──┤

├── ├──┤(0,65)TYP.

8X(1,45)

PKG
C̶
(4,4)

PKG
C̶

4221236/A  11/13

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Publication IPC–7351 is recommended for alternate designs.
        D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations.  Refer to IPC–7525 for other stencil recommendations.
        E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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