

具有一个 PLL、四个差分输出、两个输入和内部 EEPROM 的 CDCE6214-Q1 超低功耗时钟发生器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
 - 温度等级 2：-40°C 至 +105°C
- 提供功能安全
 - 可帮助进行功能安全系统设计的文档
- 通过 RMS 抖动和杂散 (12kHz - 20MHz, $F_{out} > 100\text{MHz}$) 可将高性能、低功耗分数 N PLL 配置如下：
 - 整数模式：
 - 差分输出：典型值 350fs, 最大值 600fs
 - LVC MOS 输出：典型值 1.05ps, 最大值 1.5ps
 - 分数模式：
 - 差分输出：典型值 1.7ps, 最大值 2.1ps
 - LVC MOS 输出：典型值 2.0ps, 最大值 4.0ps
- 支持有 SSC 的 PCIe Gen1/2/3/4 和无 SSC 的 Gen 1/2/3/4/5
- 内部 VCO 频率范围为 2.335GHz 至 2.625GHz
- 典型功耗：4 输出通道为 65mA, 单输出通道为 23mA。
- 通用时钟输入、两个用于提供冗余支持的基准输入
 - 差分交流耦合或 LVC MOS：10MHz 至 200MHz
 - 晶振：10MHz 至 50MHz
- 灵活的输出时钟分配
 - 4 通道分频器：多达 5 个独特输出频率，范围为 24kHz 至 328.125MHz
 - OUT0 - OUT4 引脚具有类似 LVDS、LP-HCSL 或 LVC MOS 输出
 - 无毛刺输出分频器切换和输出通道同步
 - 通过 GPIO 和寄存器实现独立输出使能端
- 频率裕量选项
 - DCO 模式：频率以 10ppb 或更小的阶跃幅度递增/递减
- 完全集成的可配置环路带宽：100kHz 至 1.6MHz
- 单电源或混合电源可进行电平转换：1.8V/2.5V/3.3V
- 可配置 GPIO 和灵活配置选项

- 兼容 I²C 的接口：频率高达 400kHz
- 具有两个页面和外部选择引脚的集成 EEPROM。可现场编程。

- 支持 100 Ω 系统
- 电磁辐射低
- 小尺寸：24 引脚 VQFN (4mm × 4mm)

2 应用

- PCIe 第 1 至 5 代时钟
- 高级驾驶辅助系统 (ADAS) - 传感器融合
- 信息娱乐和仪表组 - 汽车音响主机 - eAVB
- 数据中心和企业计算、PC 与笔记本电脑
- 企业机器 - 多功能打印机
- 测试和测量、手持设备

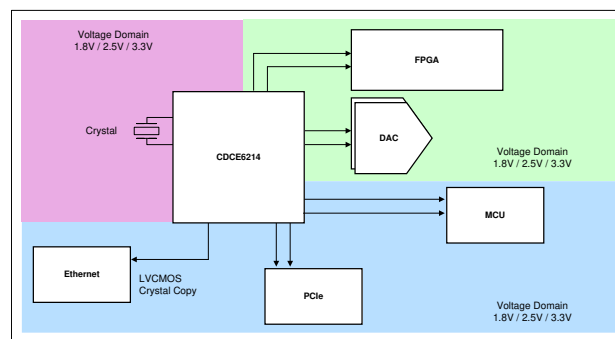
3 说明

CDCE6214-Q1 是一款适合汽车应用的四通道、超低功耗、中级抖动时钟发生器，可生成五个在各种驱动器模式之间可选的独立时钟输出。输入源可以是单端或差分输入时钟源，也可以是晶振。CDCE6214-Q1 具有一个分数 N PLL，可在任何输入频率下合成不相关的基础频率。CDCE6214-Q1 可通过 I²C 接口进行配置。无串行接口时，可以在引脚模式下将 GPIO 引脚用于对产品进行独特配置。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|-------------|-----------|-----------------|
| CDCE6214-Q1 | VQFN (24) | 4.00mm × 4.00mm |

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



应用示例 CDCE6214-Q1



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision A (December 2019) to Revision B (October 2021) | Page |
|--|------|
| • 向特性部分添加了功能安全要点..... | 1 |

| Changes from Revision * (August 2019) to Revision A (December 2019) | Page |
|---|------|
| • 将数据表状态从“预告信息”更改为：量产数据..... | 1 |

5 说明 (续)

片上 EEPROM 可用于更改配置，通过引脚可预选配置。该器件可提供频率裕量选项和无干扰运行功能，以支持系统设计验证测试 (DVT) 和以太网音频/视频桥接 (eAVB)。通过将分数反馈分频器转为 DCO 模式，任何输出通道上均可使用精细频率裕量。

内部电源调节功能可提供出色的电源纹波抑制 (PSRR)，从而降低供电网络的成本和复杂性。模拟和数字核心块由 1.8V、2.5V 或 3.3V $\pm 5\%$ 电源供电运行，输出块由 1.8V、2.5V 或 3.3V $\pm 5\%$ 电源供电运行。

CDCE6214-Q1 采用小外形封装，具有超低功耗，可根据单个基准实现高性能时钟树。工厂和用户可编程的 EEPROM 特性使得 CDCE6214-Q1 成为一款低功耗、方便易用、瞬时启动的时钟器件。

6 Pin Configuration and Functions

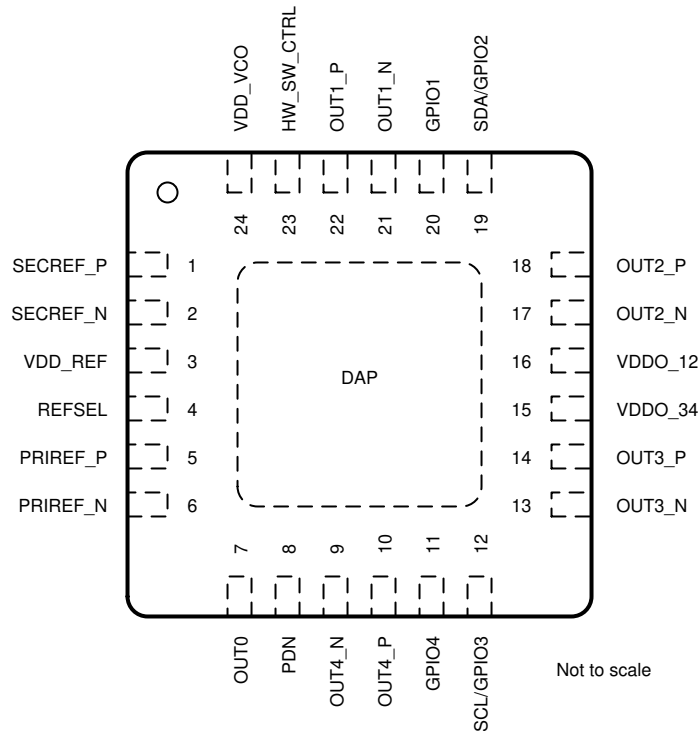


图 6-1. CDCE6214-Q1 RGE Package 24-Pin VQFN Top View

表 6-1. Pin Functions

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|--------------------|-----|----------------------|--|
| NAME | NO. | | |
| POWER | | | |
| DAP | — | G | Die Attach Pad. The DAP is an electrical connection and provides a thermal dissipation path. For proper electrical and thermal performance of the device, the DAP must be connected to PCB ground plane. |
| VDD_REF | 3 | P | 1.8 V/2.5 V/3.3 V Power Supply for Reference Input and Digital. |
| VDD_VCO | 24 | P | 1.8 V/2.5 V/3.3 V Power Supply for PLL/VCO. |
| VDDO_12 | 16 | P | 1.8 V/2.5 V/3.3 V Power Supply for OUT1 and OUT2 channels |
| VDDO_34 | 15 | P | 1.8 V/2.5 V/3.3 V Power Supply for OUT0, OUT3, and OUT4 channels |
| INPUT BLOCK | | | |
| HW_SW_CTRL RL | 23 | I, R _{PUPD} | Manual selection pin for EEPROM pages (3-state). Weak Pullup/Pulldown. R _{PUP} = 50 k Ω . R _{PD} = 50 k Ω . |

表 6-1. Pin Functions (continued)

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|-------------------------------------|-----|----------------------|--|
| NAME | NO. | | |
| PRIREF_P | 5 | I | Primary reference clock. Accepts a differential or single-ended input. Input pins need AC-coupling capacitors and internally biased in differential mode. For LVCMOS, input should be provided on PRIREF_P and the non-driven input pin should be pulled down to ground. Internal biasing for differential mode is disabled in single-ended mode. |
| PRIREF_N | 6 | I | |
| REFSEL | 4 | I, R _{PUPD} | Manual selection pin of reference input (3-state). Weak Pullup/Pulldown. R _{PU} = 50 k Ω . R _{PD} = 50 k Ω . |
| SECREP_P | 1 | I | Secondary reference clock. Accepts a differential or single-ended input or XTAL. Input pins need AC-coupling capacitors and internally biased in differential mode. For XTAL input, connect crystal between SECREP_P and SECREP_N pin. SECREP_P is XOUT, SECREP_N is XIN. This device do not need any power limiting resistor on XOUT. For LVCMOS input, input should be provided on SECREP_P, and the non-driven input pin should be pulled down to ground. Internal biasing for differential mode is disabled in single-ended and XTAL mode. |
| SECREP_N | 2 | | |
| OUTPUT BLOCK | | | |
| OUT0 | 7 | O | LVCMOS Output 0. Reference Input can be bypassed into this output. Output slew-rate configurable on all LVCMOS outputs. |
| OUT1_P | 22 | O | LVDS-like/LP-HCSL/LVCMOS Output Pair 1. Programmable driver with LVDS-like/LP-HCSL or 2x LVCMOS outputs. |
| OUT1_N | 21 | | |
| OUT2_P | 18 | O | LVDS-like/LP-HCSL Output Pair 2. Programmable driver with LVDS-like/LP-HCSL outputs. |
| OUT2_N | 17 | | |
| OUT3_P | 14 | O | LVDS-like/LP-HCSL Output Pair 3. Programmable driver with LVDS-like/LP-HCSL outputs. |
| OUT3_N | 13 | | |
| OUT4_P | 10 | O | LVDS-like/LP-HCSL/LVCMOS Output Pair 4. Programmable driver with LVDS-like/LP-HCSL or 2x LVCMOS outputs. |
| OUT4_N | 9 | | |
| DIGITAL CONTROL / INTERFACES | | | |
| GPIO1 | 20 | I/O, R _{PU} | STATUS output or GPIO1 input. Weak pullup resistor when configured as Input. R _{PU} = 50 k Ω . Pullup resistor disabled in output mode. |
| GPIO4 | 11 | I/O, R _{PU} | STATUS output or GPIO4 input. Weak pullup resistor when configured as Input. R _{PU} = 50 k Ω . Pullup resistor disabled in output mode. |
| PDN | 8 | I, R _{PU} | Device Power-down/RESET (active low) or SYNCN. Weak pullup resistor. R _{PU} = 50 k Ω . Pullup resistor disabled in output mode. |
| SDA/GPIO2 | 19 | I/O | I ² C Serial Data (bidirectional, open-drain) or GPIO2 input. Requires an external pullup resistor to VDD_REF in I ² C mode. I ² C slave address is initialized from on-chip EEPROM. Fail-safe Input. |
| SCL/GPIO3 | 12 | I | I ² C Serial Clock or GPIO3 input. Requires an external pullup resistor to VDD_REF in I ² C mode. Fail-safe Input. |

(1) Type:

- G = Ground
- P = Power
- I = Input
- I/O = Input/Output
- O = Output
- I, RPUPD = Input with Resistive Pullup and Pulldown
- I, RPU = Input with Resistive Pullup
- I/O, RPU = Input/Output with Resistive Pullup

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---|----------------------|------|-----------------------------|------|
| VDD_REF, VDD_VCO, VDDO_12, VDDO_34 | Supply Voltage | -0.3 | 3.63 | V |
| PRIREF_P, PRIREF_N, SECREP_P, SECREP_N | Input Voltage | -0.3 | VDD_REF + 0.3 | V |
| GPIO1, SDA/GPIO2, SCL/GPIO3, GPIO4, REFSEL, HW_SW_CTRL, PDN | Input Voltage | -0.3 | VDD_REF + 0.3 | V |
| OUT0, OUT1_P, OUT1_N, OUT2_P, OUT2_N, OUT3_P, OUT3_N, OUT4_P, OUT4_N ⁽²⁾ | Output Voltage | -0.3 | VDDO_X ⁽²⁾ + 0.3 | V |
| T _J | Junction Temperature | | 125 | °C |
| T _{stg} | Storage temperature | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) VDDO_X refers to the output supply for a specific output channel, where X denotes the channel index.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002, HBM ESD Classification Level 2 ⁽¹⁾ | 2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5 | 750 | V |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-------------------|--|------|---------------|-------|------|
| VDD_VCO | Core supply voltage | 1.71 | 1.8, 2.5, 3.3 | 3.465 | V |
| VDDO_12, VDDO_34 | Output supply voltage | 1.71 | 1.8, 2.5, 3.3 | 3.465 | V |
| VDD_REF | Reference supply voltage | 1.71 | 1.8, 2.5, 3.3 | 3.465 | V |
| T _A | Ambient temperature | -40 | | 105 | °C |
| T _J | Junction temperature | -40 | | 125 | °C |
| T _{LOCK} | Continuous lock over temperature (without VCO calibration) | | | 145 | °C |
| t _{RAMP} | Maximum supply voltage ramp time ⁽¹⁾ | 0.1 | | 30 | ms |

(1) VDD pin should monotonically reach 95% of its final value within supply ramp time. All VDD pins were tied together for this evaluation. For non-monotonic or slower power supply ramp, it is recommended to pull-down PDN pin until VDD pins have reached 95% of its final value. PDN pin has a 50 kΩ pullup resistor. When PDN pin cannot be actively controlled, TI recommends to add a capacitor to GND on PDN pin to delay the release of reset.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | CDCE6214-Q1 | UNIT |
|-------------------------------|--|-------------|------|
| | | RGE (VQFN) | |
| | | 24 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 32.5 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 32.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 12.2 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 2.0 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.4 | °C/W |

| THERMAL METRIC ⁽¹⁾ | | CDCE6214-Q1 | UNIT |
|-------------------------------|--|-------------|------|
| | | RGE (VQFN) | |
| | | 24 PINS | |
| ψ_{JB} | Junction-to-board characterization parameter | 12.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report, SPRA953.

7.5 EEPROM Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------------------|-----------|-----|-----|--------|
| η_{EEcyc} | EEPROM programming cycles | each word | 10 | | cycles |
| t_{EEret} | EEPROM data retention | | 10 | | years |

7.6 Reference Input, Single-Ended Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|-----------------------|----------------------|---------------|---------------|------|
| f_{IN_Ref} | Reference frequency | 10 | | 200 | MHz |
| V _{IH} | Input high voltage | LVC MOS Input Buffer | 0.8 × VDD_REF | | V |
| V _{IL} | Input low voltage | LVC MOS Input Buffer | | 0.2 × VDD_REF | V |
| dV _{IN} /dT | Input slew rate | 20% - 80% | 1 | | V/ns |
| IDC | Input duty cycle | | 40 | 60 | % |
| I _{IN_LEAKAGE} | Input leakage current | | -100 | 100 | μA |
| C _{IN_REF} | Input capacitance | at 25°C | | 5 | pF |

7.7 Reference Input, Differential Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--|-----------------------|------|-----|------|
| f_{IN_Ref} | Reference frequency | 10 | | 200 | MHz |
| V _{IN_DIFF} | Differential input voltage swing, peak-to-peak | VDD_REF = 2.5 V/3.3 V | 0.4 | 1.6 | V |
| V _{IN_DIFF} | Differential input voltage swing, peak-to-peak | VDD_REF = 1.8 V | 0.4 | 1.0 | V |
| dV _{IN} /dT | Input slew rate | 20% - 80% | 1 | | V/ns |
| IDC | Input duty cycle | | 40 | 60 | % |
| I _{IN_LEAKAGE} | Input leakage current | | -100 | 100 | μA |
| C _{IN_REF} | Input capacitance | at 25°C | | 5 | pF |

7.8 Reference Input, Crystal Mode Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------------|---|-----|------|------|
| f_{IN_Xtal} | Crystal frequency | Fundamental mode | 10 | 50 | MHz |
| Z _{ESR} | Crystal equivalent series resistance | f_{XTAL} = 10 MHz to 16 MHz | | 60 | Ω |
| Z _{ESR} | Crystal equivalent series resistance | f_{XTAL} = 16 MHz to 30 MHz | | 50 | Ω |
| Z _{ESR} | Crystal equivalent series resistance | f_{XTAL} = 30 MHz to 50 MHz | | 30 | Ω |
| C _L | Crystal load capacitance | Using on-chip load capacitance. A supported Crystal is within | 5 | 12.8 | pF |
| P _{XTAL} | Crystal tolerated drive power | A supported crystal tolerates up to | | 200 | μW |
| C _{XIN_LOAD} | On-Chip load capacitance | Programmable in typ. 200 fF steps | 3 | 9.1 | pF |

(1) For detailed application report on configuring the XTAL Input, please refer to [SNAA331: CDCI6214 and CDCE6214-Q1 design with crystal input](#).

7.9 General-Purpose Input Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|-----------------------------------|--|---------------|-----|---------------|------|
| V _{IH} | Input high voltage | | 0.8 × VDD_REF | | | V |
| V _{IL} | Input low voltage | | | | 0.2 × VDD_REF | V |
| I _{IH} | Input high level current | V _{IH} = VDD_REF, GPIO[1:4], PDN | -5 | | 5 | μA |
| I _{IL} | Input low level current | V _{IL} = GND, GPIO[2:3] | -5 | | 5 | μA |
| I _{IL} | Input low level current | V _{IL} = GND, GPIO[1], GPIO[4], PDN | -100 | | 100 | μA |
| dV _{IN} /dT | Input slew rate | 20% - 80% | 0.5 | | | V/ns |
| T _{PULSE_WIDT H} | Pulse width for correct operation | | 10 | | | ns |
| R _{PU} | Pullup Resistance | Pins PDN, GPIO[1], GPIO[4] | 30 | 55 | 80 | kΩ |
| C _{IN} | Pin Capacitance | | | | 10 | pF |

7.10 Triple Level Input Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------|---------------------------|----------------|---------------|----------------|------|
| V _{IH} | Input high voltage | | 0.8 × VDD_REF | | | V |
| V _{IM} | Input mid voltage | Float pin | 0.41 × VDD_REF | 0.5 × VDD_REF | 0.58 × VDD_REF | V |
| V _{IL} | Input low voltage | | | | 0.2 × VDD_REF | V |
| I _{IH} | Input high level current | V _{IH} = VDD_REF | 20 | 50 | 100 | μA |
| I _{IL} | Input low level current | V _{IL} = GND | -100 | -50 | -20 | μA |

7.11 Logic Output Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---------------------|-----------------|---------------|-----|---------------|------|
| VOH | Output high voltage | | 0.8 × VDD_REF | | | V |
| VOL | Output low voltage | | | | 0.2 × VDD_REF | V |

7.12 Phase Locked Loop Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|---------------------------------|------|-----|------|-------|
| f _{PDF} | Phase Detector Frequency | Integer and Fractional PLL mode | 1 | | 100 | MHz |
| f _{VCO} | Voltage Controlled Oscillator Frequency | | 2335 | | 2625 | MHz |
| f _{BW} | Configurable closed-loop PLL Bandwidth | REF = 25 MHz | 100 | | 1600 | kHz |
| K _{VCO} | Voltage-Controlled Oscillator Gain | f _{VCO} = 2.4 GHz | | 140 | | MHz/V |
| K _{VCO} | Voltage-Controlled Oscillator Gain | f _{VCO} = 2.5 GHz | | 175 | | MHz/V |
| Δ T _{CL} | Allowable Temperature Drift for Continuous Lock ⁽¹⁾ | dT/dt ≤ 20 K / min | | | 145 | °C |
| f _{MAX-ERROR} | Maximum frequency error with frac-N PLL | | | | 0.1 | ppm |

- (1) The maximum allowable temperature drift for continuous lock: how far the temperature can drift in either direction from the value it was at the time, when the On-Chip VCO was calibrated while the PLL stays in lock throughout the temperature drift. The internal VCO calibration takes place: at device start-up, when the device is reset using the RESET pin and when REGISTER bit is changed. This implies the device will work over the entire frequency range, but if the temperature drifts more than the 'maximum allowable temperature drift for continuous lock', then it is necessary to re-calibrate the VCO, using the appropriate REGISTER bit, to ensure the PLL stays in lock. Regardless of what temperature the part was initially calibrated at, the temperature can never drift outside the ambient temperature range of -40° C to 105° C.

7.13 Closed-Loop Output Jitter Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---------------------------------|--|-----|------|------|------|
| t _{RJ_CL} | RMS Phase Jitter | RMS jitter with spurs from 12 kHz to 20 MHz, Input Crystal = 25 MHz, Differential OUTx > 100 MHz, int-PLL | | 350 | 600 | fs |
| t _{RJ_CL} | RMS Phase Jitter ⁽¹⁾ | RMS jitter with spurs from 12 kHz to 20 MHz, Input Crystal = 25 MHz, Differential OUTx > 100 MHz, frac-PLL | | 1600 | 2100 | fs |
| t _{RJ_CL, PCIE} | RMS Phase Jitter | PCIe Gen 3 Filter applied, XIN = Crystal 25 MHz, OUTx = 100 MHz, frac-N PLL with and without SSC, LP-HCSL or LVDS output | | 475 | 1000 | fs |

- (1) F_{IN} = 25MHz, F_{OUT} = 161.1328MHz, F_{PPD} = 25MHz, RMS Noise = 1.83ps. F_{IN} = 25MHz, F_{OUT} = 161.1328MHz, F_{PPD} = 50MHz, RMS Noise = 1.33ps. F_{IN} = 25MHz, F_{OUT} = 148.5MHz, F_{PPD} = 25MHz, RMS Noise = 1.74ps. F_{IN} = 25MHz, F_{OUT} = 148.5MHz, F_{PPD} = 50MHz, RMS Noise = 1.43ps. F_{IN} = 25MHz, F_{OUT} = 148.3516MHz, F_{PPD} = 25MHz, RMS Noise = 1.6ps. F_{IN} = 25MHz, F_{OUT} = 148.3516MHz, F_{PPD} = 50MHz, RMS Noise = 1.5ps. F_{IN} = 25MHz, F_{OUT} = 106.5MHz, F_{PPD} = 25MHz, RMS Noise = 0.8ps. F_{IN} = 25MHz, F_{OUT} = 106.5MHz, F_{PPD} = 50MHz, RMS Noise = 1.3ps.

7.14 Input and Output Isolation

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---------------------------|---|-----|-----|-----|------|
| P _{ISOLATION} | Reference input isolation | Crosstalk between reference inputs, PRIREF = 27MHz LVCMOS, SECREP = 25MHz XTAL | | -64 | | dB |
| P _{ISOLATION} | Reference input isolation | Crosstalk between reference inputs, PRIREF = 100MHz LVDS, SECREP = 25MHz LVCMOS | | -72 | | dB |
| P _{ISOLATION} | Clock output isolation | Crosstalk between clock outputs, OUT1 = 100MHz LP-HCSL, OUT2 = 156.25MHz LVDS, PFD = 25MHz, int-PLL | | -65 | | dB |
| P _{ISOLATION} | Clock output isolation | Crosstalk between clock outputs, OUT1 = 156.25MHz LVDS, OUT0 = 25MHz LVCMOS | | -42 | | dB |

7.15 Buffer Mode Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|---|------|-----|-----|------|
| t _{RJ_ADD} | Additive RMS Phase Jitter, System Level | int. Range from 10 kHz to 20 MHz, REF = HCSL 100 MHz with 0.5 V/ns, OUTx = 100 MHz LP-HCSL | | | 350 | fs |
| t _{PROP, LVCMOS} | Input-to-output propagation delay | REF = LVCMOS 25 MHz, OUTx = 25 MHz LVCMOS | | 1 | | ns |
| t _{PROP, Differential} | Input-to-output propagation delay ⁽¹⁾ | REF = AC-LVDS 100 MHz, OUTx = 100 MHz. Measured on OUT0 | | 2.3 | | ns |
| t _{PROP-VARIATION} | Input-to-output delay variation in ZDB mode | ZDB mode, LVCMOS input = LVCMOS output = 25 MHz, PLL BW = 300 kHz to 900 kHz across temperature | -400 | | 400 | ps |

- (1) OUT1/OUT4 and OUT2/OUT3 are matched pair-wise. OUT1/OUT4 has LVCMOS buffer while OUT2/OUT3 do not have LVCMOS buffer. There is an additional skew 150 ps- 250 ps between OUT1/OUT4 and OUT2/OUT3.

7.16 PCIe Spread Spectrum Generator

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------------|------------------------------------|-----|------|-----|------|
| f _{SSC-RATE} | SSC modulation rate | OUTx = 100 MHz | 30 | 31.5 | 33 | kHz |
| P _{AMPL-RED} | SSC amplitude reduction | OUTx = 100 MHz, -0.25% Down spread | | 6.8 | | dB |
| P _{AMPL-RED} | SSC amplitude reduction | OUTx = 100 MHz, -0.50% Down spread | | 9.9 | | dB |
| f _{SSC-STEP} | Down and Center spread SSC step size | OUTx = 100 MHz | | 0.25 | | % |

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|---|--|------|-----|-----|------|
| f _{SSC_FREQ_DEVIATION} | Down spread minimum/maximum deviation | OUTx = 100 MHz. F _{PFD} = 25 MHz, 50 MHz, 100 MHz | -0.5 | | 0 | % |
| f _{SSC_FREQ_DEVIATION} | Center spread minimum/maximum deviation | OUTx = 100 MHz. F _{PFD} = 25 MHz, 50 MHz, 100 MHz | -0.5 | | 0.5 | % |

7.17 LVCMOS Output Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--------------------------------------|---|--------------|-------|--------------|------|
| f _{O_LVCMOS} | Output frequency | 2 pF to GND, normal mode | 0.024 | | 200 | MHz |
| V _{OH_LVCMOS} | Output high voltage | I _{OH} = 1 mA, VDDO_x is corresponding supply voltage. | 0.8 × VDDO_x | | | V |
| V _{OL_LVCMOS} | Output low voltage | I _{OL} = 1 mA, VDDO_x is corresponding supply voltage. | | | 0.2 × VDDO_x | V |
| I _{OH} | Output high current | Vout = 0.8 × VDDO_x, VDDO_x = 1.8 V | | -6 | | mA |
| I _{OH} | Output high current | Vout = 0.8 × VDDO_x, VDDO_x = 2.5 V | | -8.5 | | mA |
| I _{OH} | Output high current | Vout = 0.8 × VDDO_x, VDDO_x = 3.3 V | | -11.2 | | mA |
| I _{OL} | Output low current | Vout = 0.2 × VDDO_x, VDDO_x = 1.8 V | | 6 | | mA |
| I _{OL} | Output low current | Vout = 0.2 × VDDO_x, VDDO_x = 2.5 V | | 8.5 | | mA |
| I _{OL} | Output low current | Vout = 0.2 × VDDO_x, VDDO_x = 3.3 V | | 11.2 | | mA |
| T _{RISE-FALL} | Output rise/fall time | 20/80%, C _L = 5 pF, normal mode | 300 | 500 | 700 | ps |
| T _{RISE-FALL} | Output rise/fall time | 20/80%, C _L = 5 pF, slow mode, measured on OUT0 | | 1000 | | ps |
| T _{SKEW} | Output-to-output skew ⁽¹⁾ | LVCMOS-to-LVCMOS outputs, same divide value | | 100 | | ps |
| T _{SKEW} | Output-to-output skew ⁽¹⁾ | LVCMOS-to-Differential outputs, same divide value | | 400 | | ps |
| ODC | Output duty cycle | Not in PLL bypass mode | 45 | | 55 | % |
| R _{ON_LVCMOS} | Output impedance | Normal mode | 45 | 60 | 75 | Ω |
| R _{ON_LVCMOS} | Output impedance | Slow mode | 50 | 65 | 85 | Ω |

(1) OUT1/OUT4 and OUT2/OUT3 are matched pair-wise. OUT1/OUT4 has LVCMOS buffer while OUT2/OUT3 do not have LVCMOS buffer. OUT1/OUT4 is matched within T_{OUT-SKEW}. OUT2/OUT3 is matched within T_{OUT-SKEW}.

7.18 LP-HCSL Output Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|-------|-----|---------|------|
| f _{O_HCSL} | Output frequency | | 0.024 | | 328.125 | MHz |
| V _{OH} | Output high voltage ⁽³⁾ | | 660 | | 850 | mV |
| V _{OL} | Output low voltage | | -150 | | 150 | mV |
| Z _{DIFF} | Differential Output Impedance ⁽³⁾ | | 90 | 100 | 110 | Ω |
| V _{CROSS} | Absolute crossing point | 12-in, 100 Ω ±10% diff. trace with 2 pF±5%/pin in FR4. | 250 | | 550 | mV |
| ΔV _{CROSS} | Relative crossing point variation | with respect to average crossing point | | | 140 | mV |
| dV/dt | Slew rate for rising and falling edge | differential, at V _{CROSS} +/-150 mV, f _{O_HCSL} =100 MHz ⁽¹⁾ | 1 | | 4 | V/ns |
| ΔdV/dt | Slew rate matching | single-ended, at V _{CROSS} +/-75 mV, f _{O_HCSL} =100 MHz ⁽¹⁾ | | | 20 | % |
| V _{rb} | Output ringback voltage | Measured on differential output at 100 MHz and specifies minimum voltage from zero crossing | -100 | | 100 | mV |
| T _{stable} | Time elapsed until ringback | Minimum time until ringback is allowed | 500 | | | ps |
| ODC | Output duty cycle | Not in PLL bypass mode | 45 | | 55 | % |
| T _{OUT-SKEW} | Output skew ⁽²⁾ | Same divide value, LP-HCSL to LP-HCSL | | 100 | | ps |

(1) PCIe test load slew rate

- (2) OUT1/OUT4 and OUT2/OUT3 are matched pair-wise. OUT1/OUT4 has LVCMOS buffer while OUT2/OUT3 do not have LVCMOS buffer. OUT1/OUT4 is matched within $T_{OUT-SKEW}$. OUT2/OUT3 is matched within $T_{OUT-SKEW}$. There is an additional skew 150 ps- 250 ps between OUT1/OUT4 and OUT2/OUT3.
- (3) Differential Output characteristic is trimmed in factory and trim settings are stored in EEPROM. Parameter not valid in Fall-back mode.

7.19 LVDS Output Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V \pm 5%, 2.5 V \pm 5%, 3.3 V \pm 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|--|-------|------|---------|------|
| $f_{O_PRG_AC}$ | Output frequency | | 0.024 | | 328.125 | MHz |
| V_{CM} | Output common mode ⁽²⁾ | VDDO_X = 2.5 V, 3.3 V | 1.025 | 1.2 | 1.375 | V |
| V_{CM} | Output common mode ⁽²⁾ | VDDO_X = 1.8 V | 0.85 | 0.95 | 1.05 | V |
| V_{OD} | Differential output voltage ⁽²⁾ | VDDO_X = 1.8 V ($F_{out} < 200$ MHz), 2.5 V, 3.3 V. | 0.25 | 0.30 | 0.45 | V |
| V_{OD} | Differential output voltage ⁽²⁾ | VDDO_X = 1.8 V & $F_{out} > 200$ MHz | 0.22 | 0.30 | 0.45 | V |
| t_{RF} | Output rise/fall times | LVDS (20% to 80%) | 450 | 650 | 900 | ps |
| ODC | Output duty cycle | Not in PLL bypass mode | 45 | | 55 | % |
| $T_{OUT-SKEW}$ | Output skew ⁽¹⁾ | Same divide value, LVDS to LVDS output | | 100 | | ps |

- (1) OUT1/OUT4 and OUT2/OUT3 are matched pair-wise. OUT1/OUT4 has LVCMOS buffer while OUT2/OUT3 do not have LVCMOS buffer. OUT1/OUT4 is matched within $T_{OUT-SKEW}$. OUT2/OUT3 is matched within $T_{OUT-SKEW}$. There is an additional skew 150 ps- 250 ps between OUT1/OUT4 and OUT2/OUT3.
- (2) Output Common Mode voltage and Differential output swing is dependent upon register settings DIFFBUF_IBIAS_TRIM, LVDS_CMTRIM_DEC and LVDS_CMTRIM_INC. Parameters defined for DIFFBUF_IBIAS_TRIM=6h, LVDS_CMTRIM_DEC=0h and LVDS_CMTRIM_INC=0h. Output Common Mode tested at DC.

7.20 Output Synchronization Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V \pm 5%, 2.5 V \pm 5%, 3.3 V \pm 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|---|-----|-----|-----|------|
| t_{SU_SYNC} | Setup time SYNC pulse | with respect to PLL reference rising edge at 100 MHz with R=1 | 3 | | | ns |
| t_{H_SYNC} | Hold time SYNC pulse | with respect to PLL reference rising edge at 100 MHz with R=1 | | | 3 | ns |
| t_{PWH_SYNC} | High pulse width for SYNC | With R = 1, at least 2 PFD periods + 24 feedback pre-scaler periods | 60 | | | ns |
| t_{PWL_SYNC} | Low pulse width for SYNC | With R = 1, at least 1 PFD period | 6 | | | ns |
| t_{EN} | Individual output enable time ⁽¹⁾ | tri-state to first valid rising edge | | | 4 | nCK |
| t_{DIS} | Individual output disable time ⁽¹⁾ | last valid falling edge to tri-state | | | 4 | nCK |

- (1) Output clock cycles of respective output channel. Global output enable handled by digital logic, additional propagation will be added.

7.21 Power-On Reset Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V \pm 5%, 2.5 V \pm 5%, 3.3 V \pm 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------------------|---|-------|-----|-------|------|
| $V_{THRESHOLD}$ | POR threshold voltage ⁽¹⁾ | | 0.875 | | 1.275 | V |
| $t_{STARTUP}$ | Start-up time | Start-up time after VDD reaches 95% to the time outputs are toggling with correct frequency (input = crystal or external clock) | | 9 | | ms |
| t_{VDD} | Power supply ramp time ⁽²⁾ | timing requirement for any VDD pin while PDN=LOW | 0.1 | | 30 | ms |

- (1) POR threshold voltage is the power supply voltage at which the internal reset is deasserted. It is qualified internally with PDN.
- (2) VDD pin should monotonically reach 95% of its final value within supply ramp time. Parameters specified by characterization. All VDD pins were tied together for this evaluation. For non-monotonic or slower power supply ramp, it is recommended to pull-down PDN pin until VDD pins have reached 95% of its final value. PDN pin has a 50 k Ω pullup resistor. When PDN pin cannot be actively controlled, TI recommends to add a capacitor to GND on PDN pin to delay the release of reset.

7.22 I²C-Compatible Serial Interface Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---------------------------|-----------------------------|---------------|---------------|-----|------|
| V _{IH} | Input Voltage, Logic High | | 0.7 × VDD_REF | | | V |
| V _{IL} | Input Voltage, Logic Low | | | 0.3 × VDD_REF | | V |
| I _{IH} | Input Leakage Current | VDD_REF ± 10% | -5 | | 5 | μA |
| V _{OL} | Low Level Output Voltage | at 3 mA sink current | | | 0.4 | V |
| C _{IN} | Input Capacitance | | | | 10 | pF |
| C _{OUT} | Output Capacitance | max bus capacitance per pin | | | 400 | pF |

7.23 Timing Requirements, I²C-Compatible Serial Interface

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|------------------------------------|---|------------------|-----|----------------|------|
| t _{PW_G} | Pulse Width of Suppressed Glitches | | | | 50 | ns |
| f _{SCL} | SCL Clock Frequency | Standard | | 100 | | kHz |
| f _{SCL} | SCL Clock Frequency | Fast-mode | | 400 | | kHz |
| t _{SU_STA} | Setup Time Start Condition | SCL=V _{IH} before SDA=V _{IL} | | 0.6 | | μs |
| t _{H_STA} | Hold Time Start Condition | SCL=V _{IL} after SCL=V _{IL} . After this time, the first clock edge is generated. | | 0.6 | | μs |
| t _{SU_SDA} | Setup Time Data | SDA valid after SCL=V _{IL} , f _{SCL} =100 kHz | 250 | | | ns |
| t _{SU_SDA} | Setup Time Data | SDA valid after SCL=V _{IL} , f _{SCL} =400 kHz | 100 | | | ns |
| t _{H_SDA} | Hold Time Data ⁽¹⁾ | SDA valid before SCL=V _{IH} | 0 ⁽²⁾ | | ⁽³⁾ | μs |
| t _{VD_SDA} | Valid Data or Acknowledge Time | f _{SCL} =100 kHz ⁽³⁾ | | | 3.45 | μs |
| t _{VD_SDA} | Valid Data or Acknowledge Time | f _{SCL} =400 kHz ⁽²⁾ | | | 0.9 | μs |
| t _{PWH_SCL} | Pulse Width High, SCL | f _{SCL} =100 kHz | 4.0 | | | μs |
| t _{PWH_SCL} | Pulse Width High, SCL | f _{SCL} =400 kHz | 0.6 | | | μs |
| t _{PWL_SCL} | Pulse Width Low, SCL | f _{SCL} =100 kHz | 4.7 | | | μs |
| t _{PWL_SCL} | Pulse Width Low, SCL | f _{SCL} =400 kHz | 1.3 | | | μs |
| t _{IR} | Input Rise Time | | | | 300 | ns |
| t _{IF} | Input Fall Time | | | | 300 | ns |
| t _{OF} | Output Fall Time | 10 pF ≤ C _{OUT} ≤ 400 pF | | | 250 | ns |
| t _{SU_STOP} | Setup Time Stop Condition | | | 0.6 | | μs |
| t _{BUS} | Bus-Free Time | Time between a Stop and a Start condition | | 1.3 | | μs |

- (1) t_{H_SDA} is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
- (2) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH(min)} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (3) The maximum t_{H_SDA} could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode, but must be less than the maximum of t_{VD_SDA} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{PWL_SCL}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.

7.24 Power Supply Characteristics

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

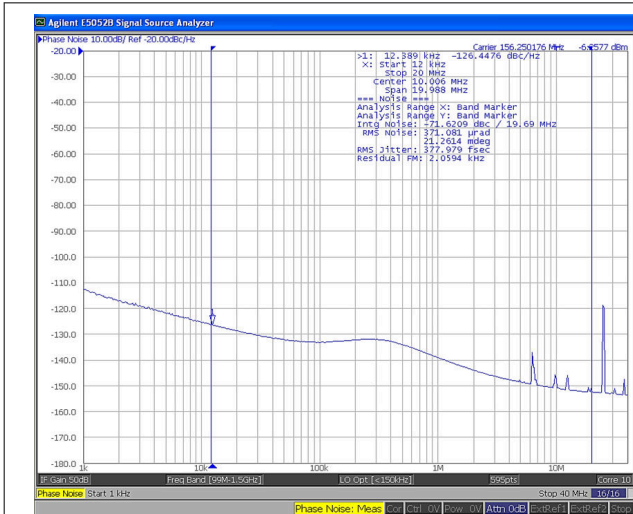
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|------------------------|--|-----|------|-----|------|
| I _{DD_REF} | VDD_REF supply current | 25 MHz XTAL, DBL ON | | 8 | | mA |
| I _{DD_VCO} | VCO and PLL current | f _{VCO} =2400 MHz, PSA = PSB = 4 and N-divider = 48 | | 14 | | mA |
| I _{DD_OUT} | Output Channel Current | IOD=6, LP-HCSL, 100MHz on OUT3 and OUT4, 25MHz on OUT0 | | 22 | | mA |
| I _{DD_OUT} | Output Channel Current | IOD = 6, LP-HCSL, 100 MHz on OUT1 and OUT2 | | 17.5 | | mA |
| I _{DD_PDN} | Power down current | using reset pin / bits | | 2.8 | 5 | mA |

VDD_VCO, VDDO_12, VDDO_34, VDD_REF = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5% and T_A = -40°C to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|------------------------------|--|-----|-----|-----|------|
| I _{DD_TYP} | Typical current | 4 x 100 MHz LVDS case using crystal input and doubler, SSC off | | 50 | 70 | mA |
| I _{DD_TYP} | Typical current | 4 x 100 MHz LP-HCSL case using crystal input and doubler, SSC off | | 65 | 90 | mA |
| L _{PSNR} | Power supply noise rejection | OUTx = 100 MHz differential, on one of VDDx injected sine wave at f _{INJ} = 100 kHz | | -61 | | dB |
| L _{PSNR} | Power supply noise rejection | OUTx = 100 MHz differential, on one of VDDx injected sine wave at f _{INJ} = 1 MHz | | -57 | | dB |

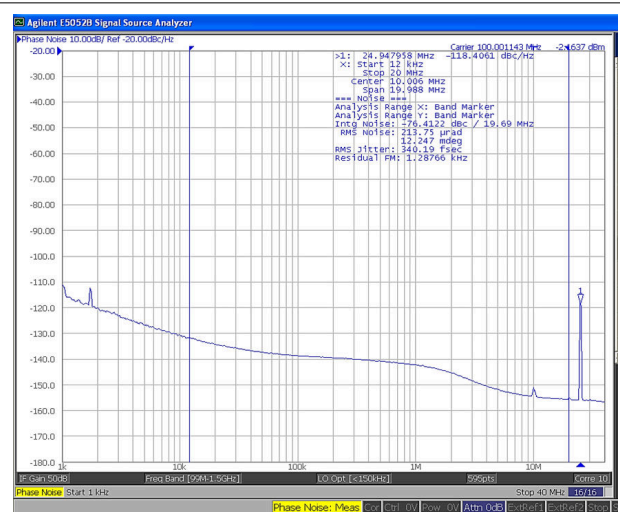
7.25 Typical Characteristics

Measured at room temperature



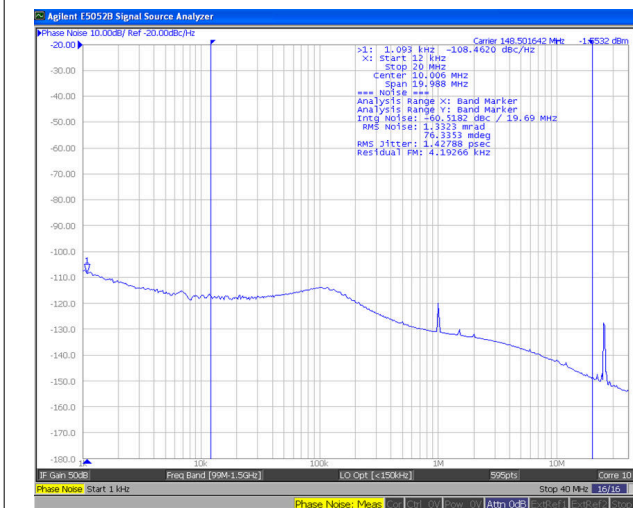
Reference: Crystal Closed-Loop Phase 156.25-MHz LVDS
Input 25 MHz Noise from 2.5-GHz
VCO

图 7-1. 156.25-MHz LVDS Output



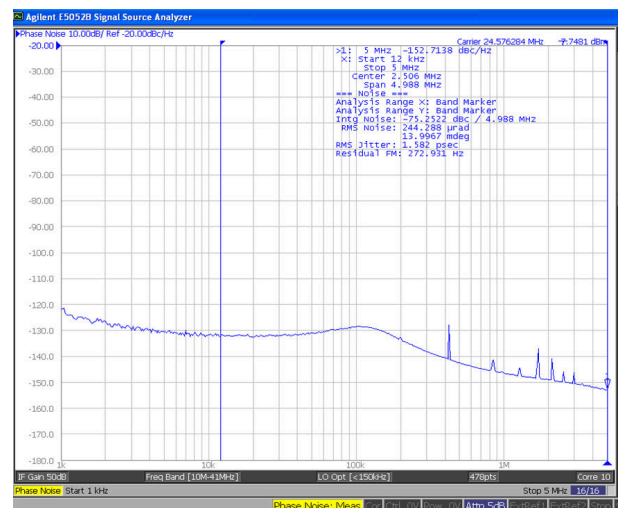
Reference: Crystal Closed-Loop Phase 100-MHz LP-HCSL
Input 25 MHz Noise from 2.4-GHz
VCO

图 7-2. 100-MHz LP-HCSL Output



Reference: Crystal Closed-Loop Phase 148.5-MHz LVDS
Input 25 MHz Noise from 2.376-GHz VCO

图 7-3. 148.5-MHz LVDS Output



Reference: Crystal Closed-Loop Phase 24.576-MHz
Input 25 MHz Noise from 2.4576-GHz VCO

图 7-4. 24.576-MHz LVCMOS Output

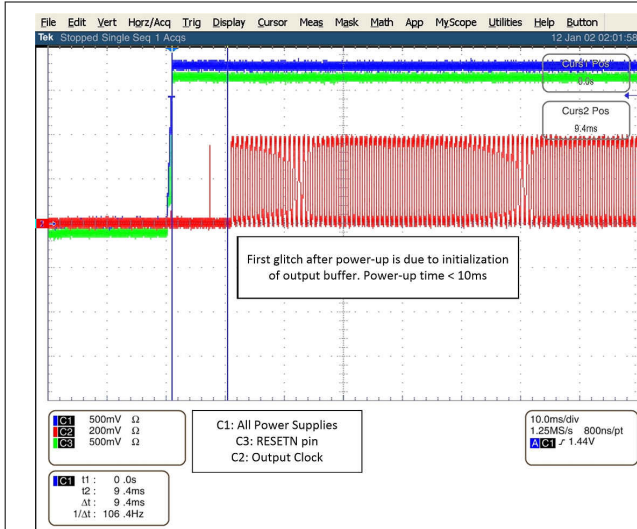


图 7-5. All Power Supply = 1.8 V, VDD Ramp Time = 1 ms

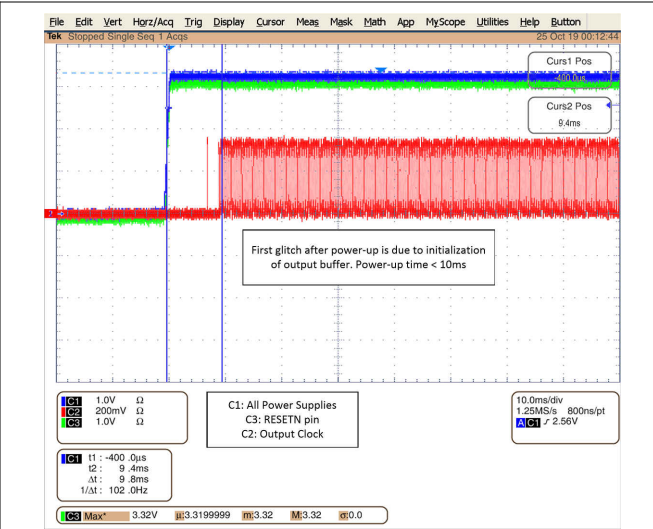


图 7-6. All Power Supply = 3.3 V, VDD Ramp Time = 1 ms

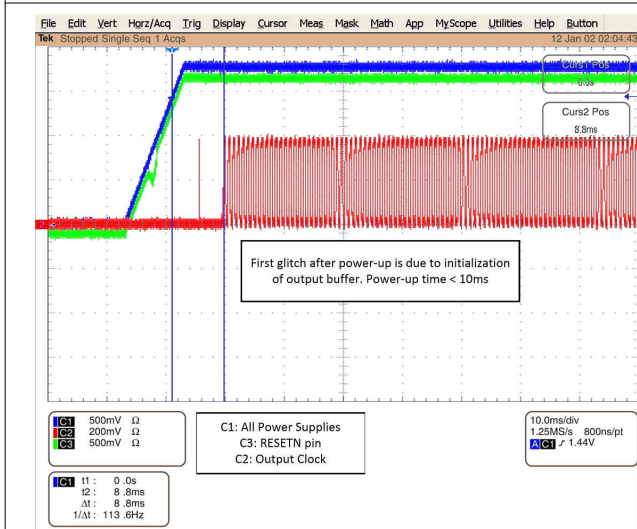


图 7-7. All Power Supply = 1.8 V, VDD Ramp Time = 10 ms

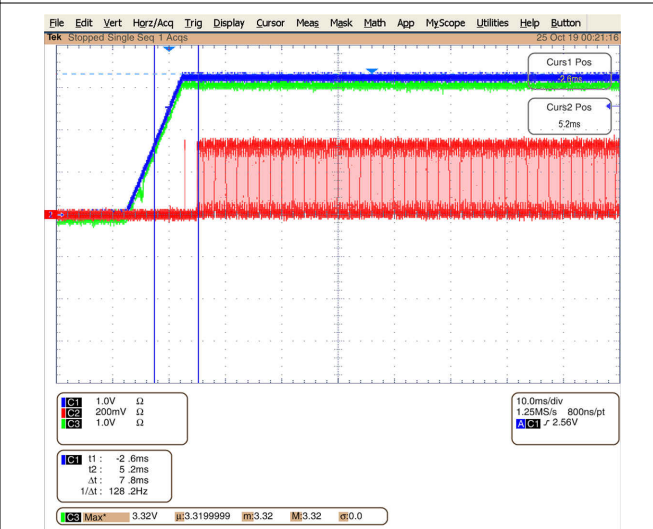


图 7-8. All Power Supply = 3.3 V, VDD Ramp Time = 10 ms

8 Parameter Measurement Information

8.1 Reference Inputs

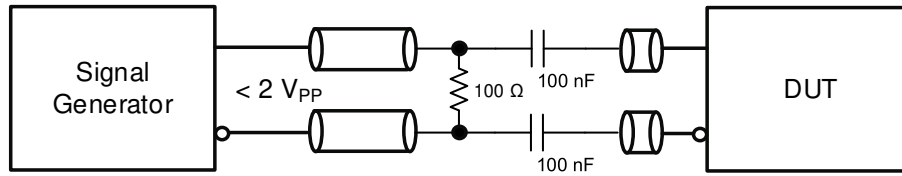


图 8-1. Differential AC-Coupled Input

8.2 Outputs

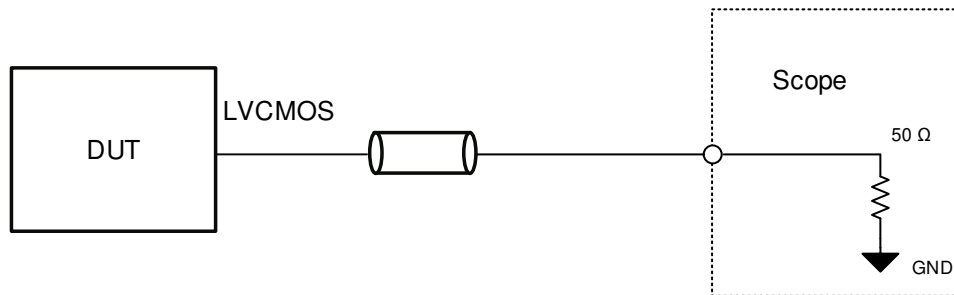


图 8-2. LVC MOS Output Test Configuration

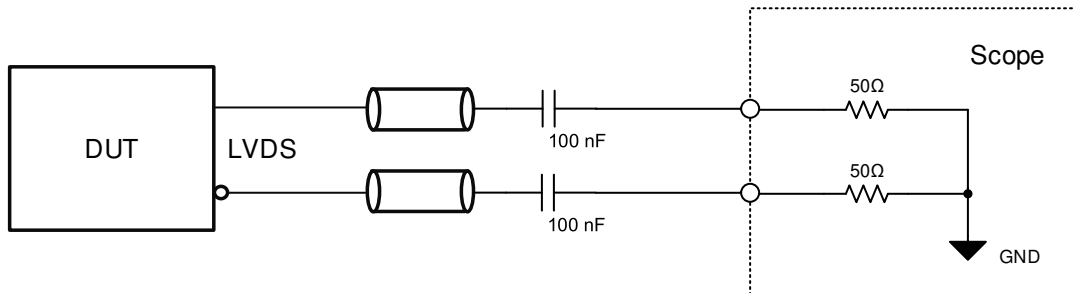


图 8-3. LVDS Output Test Configuration, AC-Coupled

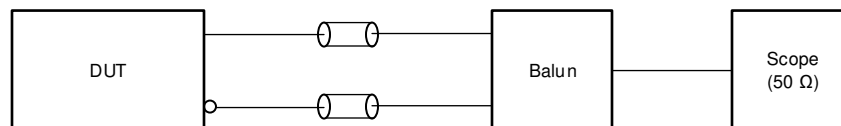


图 8-4. LP-HCSL Test Configuration, DC-Coupled

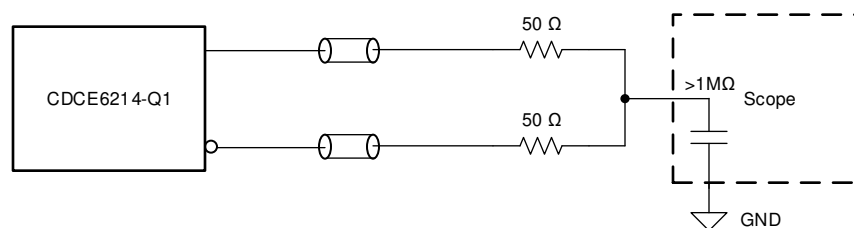


图 8-5. LVDS Common Mode Voltage, DC-Coupled

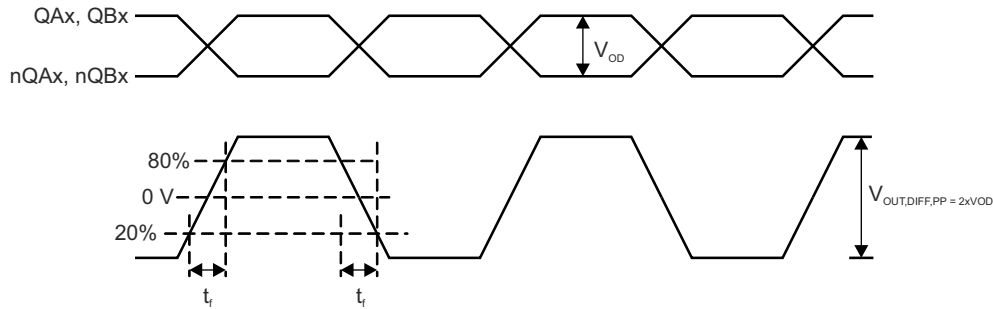


图 8-6. Differential Output Voltage and Rise/Fall Time

8.3 Serial Interface

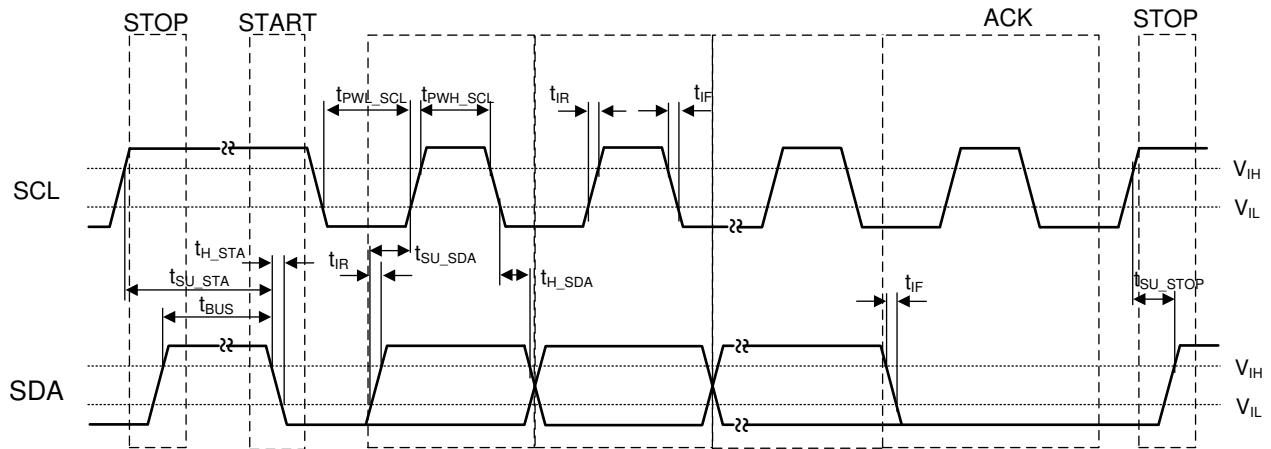


图 8-7. I²C Timing

8.4 PSNR Test

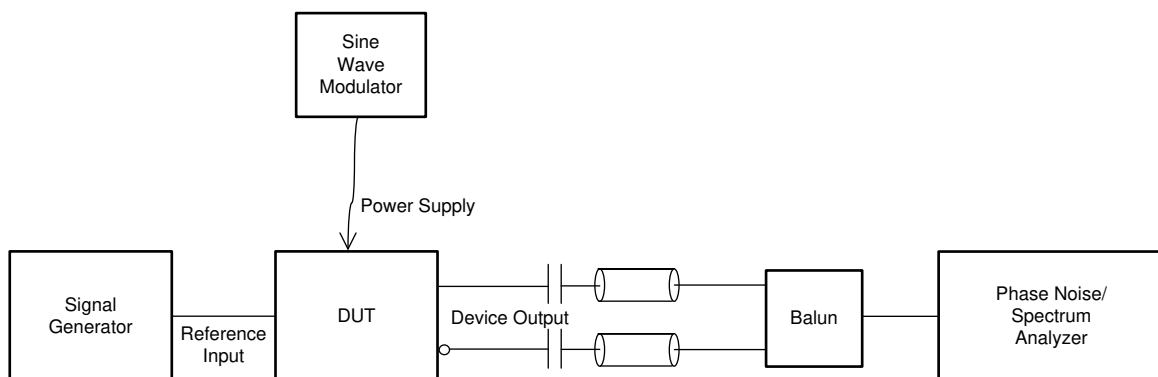


图 8-8. PSNR Test Configuration

8.5 Clock Interfacing and Termination

8.5.1 Reference Input

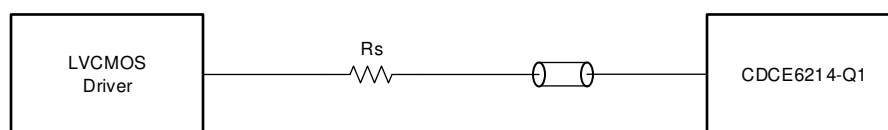


图 8-9. Single-Ended LVCMOS to Reference

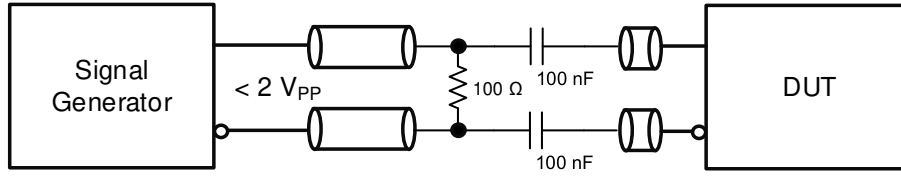


图 8-10. Differential Input to Reference

8.5.2 Outputs

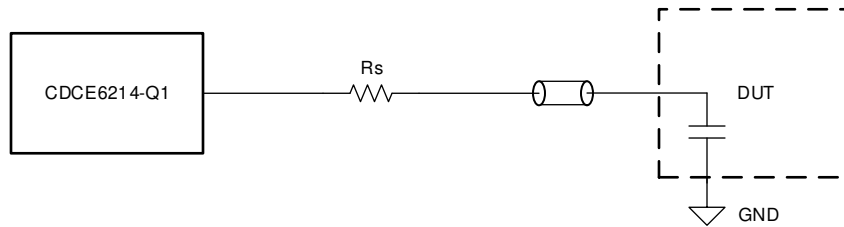


图 8-11. LVCMOS Output

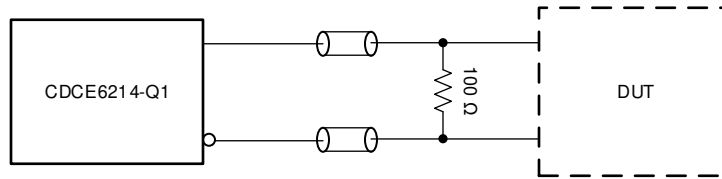


图 8-12. LVDS Output - DC-Coupled. Place 100Ω close to the DUT

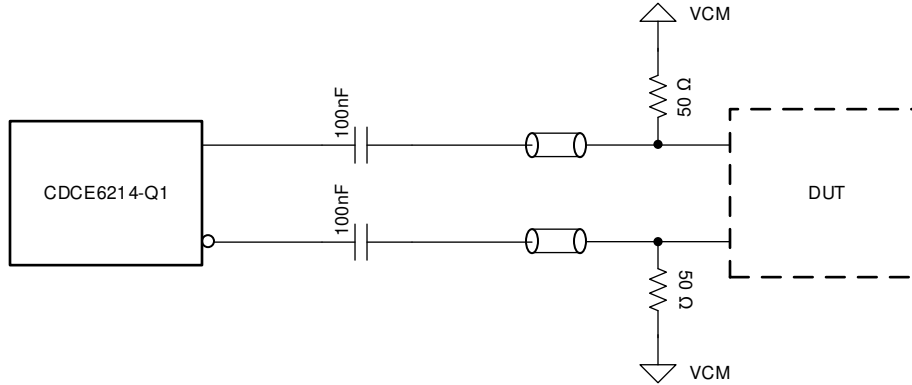


图 8-13. LVDS Output - AC-Coupled

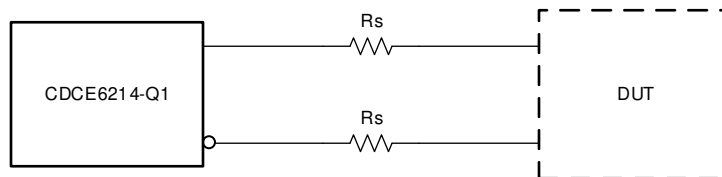


图 8-14. LP-HCSL Output

9 Detailed Description

9.1 Overview

The CDCE6214-Q1 automotive clock generator is a Phase-Locked Loop (PLL) with integrated voltage controlled Oscillator (VCO) and integrated loop filter with selectable input reference. Input reference supports XTAL, Differential and single-ended LVCMOS inputs. The PLL consists of Frac-N PLL with integrated VCO range of 2335MHz - 2625MHz. The output of the VCO is connected to the clock distribution network, which includes multiple frequency dividers and multiplexers. The output of these network is connected to four output channels with configurable differential and single ended buffers. There are 4 power supply pins which can be independently configured to 1.8V/2.5V/3.3V. CDCE6214-Q1 can be configured using the I²C serial interface or built-in EEPROM at power up. This device supports various modes such as Digitally Controlled Oscillator (DCO) through GPIO/I2C and Internal/external Zero Delay mode.

9.2 Functional Block Diagram

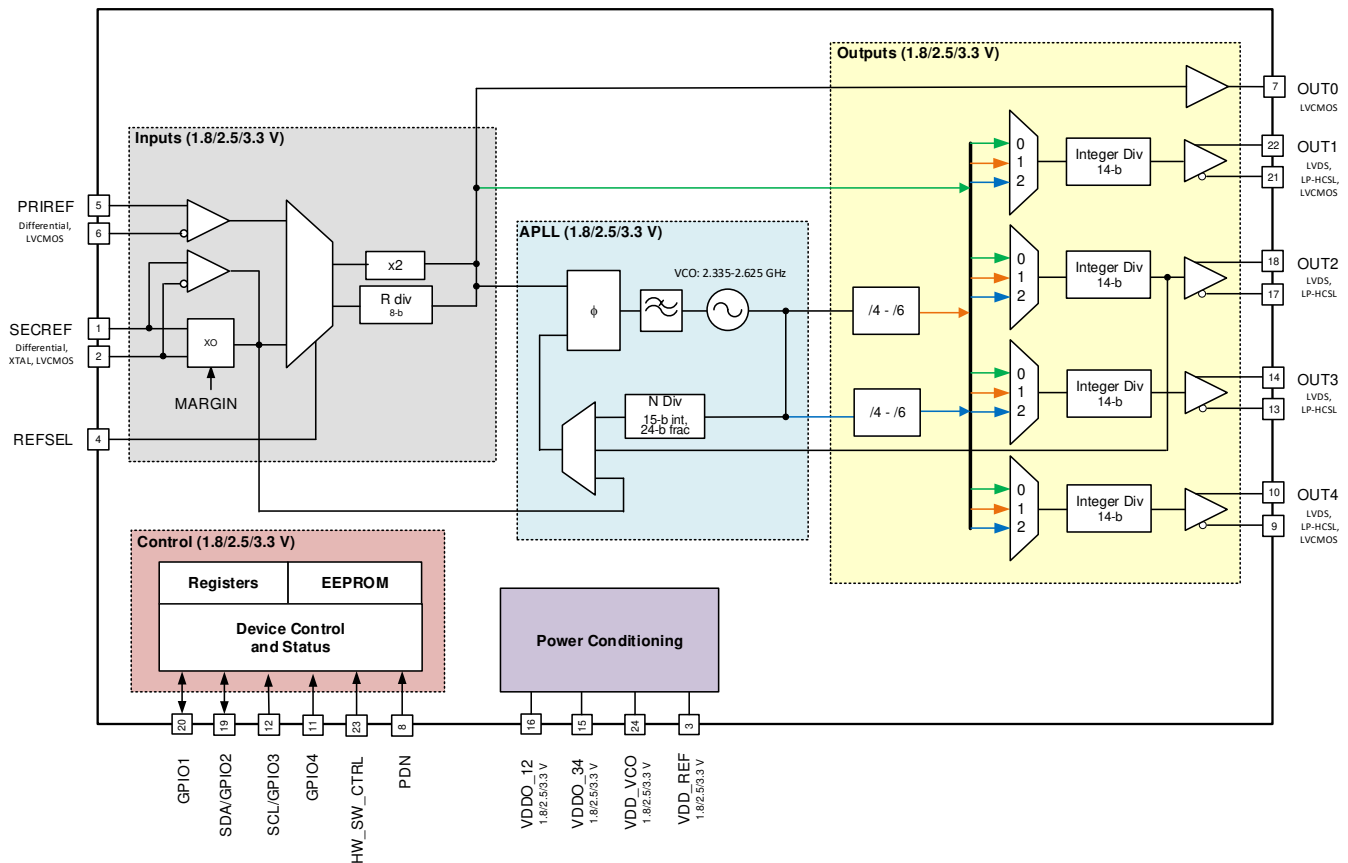


图 9-1. CDCE6214-Q1 Clock Generator With 2 Inputs, 1 Fractional-N PLL, and 4 Outputs

9.3 Feature Description

The following sections describe the individual blocks of the CDCE6214-Q1 ultra low power clock generator.

9.3.1 Reference Block

A reference clock to the PLL is fed to pins 1 (SECREP_P) and 2 (SECREP_N) or to pins 5 (PRIREF_P) and 6 (PRIREF_N). There are multiple input stages to accommodate various clock references. Pins 1 and 2 can be used to connect a XTAL across it or provide an external single-ended LVCMOS clock or a differential clock. These modes are selectable through register programming. When differential mode is selected, appropriated biasing is applied to the pin. In case of differential mode, external AC-coupling capacitor is needed. When XTAL or LVCMOS mode is selected, biasing circuitry is disengaged. Pins 5 and 6 can be used to provide an external single-ended LVCMOS clock or a differential clock.

The reference MUX selects the reference clock for the PLL. Setting REFSEL pin = L selects SECREF input, while setting REFSEL pin = H selects PRIREF Input. Alternatively, this can be configured through the register settings.

表 9-1. Reference Input Selection

| REGISTER BIT ADDRESS | REGISTER BIT FIELD NAME | VALUE | DESCRIPTION |
|----------------------|-------------------------|----------|---|
| R2[1:0] | REFSEL_SW | 0h or 1h | Input Reference Mux controlled through Pin 4 (REFSEL) |
| | (Default: 0h) | 2h | Pin1/Pin 2 SECREF Input selected. This is independent of Pin 4 status. |
| | | 3h | Pin 5/Pin 6 PRIREF Input selected. This is independent of Pin 4 status. |
| R24[1:0] | IP_SECREF_BUF_SEL | 0h | XO enabled. Valid for SECREF pins. |
| | (Default: 0h) | 1h | LVC MOS Buffer enabled. Valid for SECREF pins. |
| | | 2h or 3h | Differential Buffer enabled. Valid for SECREF pins. |
| R24[15] | IP_PRIREF_BUF_SEL | 0h | LVC MOS Buffer enabled. Valid for PRIREF pins. |
| | (Default: 0h) | 1h | Differential Buffer enabled. Valid for PRIREF pins. |

A reference divider or a clock-doubler can be engaged to further multiply (2x) or divide the reference clock to the PLL. IP_RDIV[7:0] can be used to set the value of the divider. Setting this to 00h would enable the doubler.

The output clock from the reference block can be bypassed to the OUT0 and other output channels. The bypassed clock is selectable between the Input clock or PFD clock. More details available in [表 9-9](#).

The SECREF_P and SECREF_N pins provide a crystal oscillator stage to drive a fundamental mode crystal in the range of 10 MHz to 50 MHz. The crystal input stage integrates a tunable load capacitor array up to 9 pF and programmable through R24[12:8]. The drive capability of the oscillator is programmable through R24[5:2].

The LVC MOS input buffer threshold voltage follows VDD_REF. This device can be used as a level shifter because the outputs have separate supplies.

9.3.1.1 Zero Delay Mode, Internal and External Path

The CDCE6214-Q1 can operate in Zero Delay Mode with internal as well as external feedback. In Zero Delay Mode, PRIREF clock is used as the reference clock to the PFD. SECREF input clock can be used to feed an external source as feedback clock to the PFD. External feedback path is recommended for zero delay operation. Moreover there is an additional internal feedback path which is sourced from output channel 2. It is expected that the Input-output propagation delay would be higher in Internal zero-delay mode than external zero delay mode.

表 9-2. Zero Delay Operation ^{1 2 3}

| OPERATION | REFSEL | R2[1:0] - REFSEL_SW | R24[1:0] - IP_SECREF_BUF_SEL | R24[15] - IP_PRIREF_BUF_SEL | R0[8] - ZDM_EN | R0[10] - ZDM_CLOCKSEL | DESCRIPTION |
|------------------------------|--------|---------------------|------------------------------|-----------------------------|----------------|-----------------------|------------------------------|
| Normal Operation, XTAL Input | L | 0h or 1h or 2h | 0h | X | 0h | 0h | Normal Operation, XTAL Input |

¹ In zero delay mode, all dividers should be programmed such that PLL can lock. On power-up in zero-delay mode, PLL would lock automatically

² For internal Zero delay mode, channel 2 is required. Channel 2 should not be powered down

³ "X" allows any possible bit-field value. It has no impact on the functionality

表 9-2. Zero Delay Operation ^{1 2 3} (continued)

| OPERATION | REFSEL | R2[1:0] - REFSEL_SW | R24[1:0] - IP_SECREF_BUF_SEL | R24[15] - IP_PRIREF_BUF_SEL | R0[8] - ZDM_EN | R0[10] - ZDM_CLOCKSEL | DESCRIPTION |
|--|--------|---------------------|------------------------------|-----------------------------|----------------|-----------------------|--|
| Normal Operation, Differential Input | L | 0h or 1h or 2h | 2h or 3h | X | 0h | 0h | SECREF/ Differential Input |
| Normal Operation, Differential Input | H | 0h or 1h or 3h | X | 1h | 0h | 0h | PRIREF/ Differential Input |
| Normal Operation, LVCMOS Input | L | 0h or 1h or 2h | 1h | X | 0h | 0h | SECREF/ LVCMOS Input |
| Normal Operation, LVCMOS Input | H | 0h or 1h or 3h | X | 0h | 0h | 0h | PRIREF/ LVCMOS Input |
| External Zero Delay Mode, Differential Input | H | 0h or 1h or 3h | 2h or 3h | 1h | 1h | 1h | Input Clock on PRIREF, Feedback clock on SECREF |
| External Zero Delay Mode, LVCMOS Input | H | 0h or 1h or 3h | 1h | 0h | 1h | 1h | Input Clock on PRIREF, Feedback clock on SECREF |
| Internal Zero Delay Mode, Differential Input | H | 0h or 1h or 3h | X | 1h | 1h | 0h | Input clock on PRIREF |
| Internal Zero Delay Mode, Differential Input | H | 0h or 1h or 3h | X | 0h | 1h | 0h | Input clock in PRIREF |

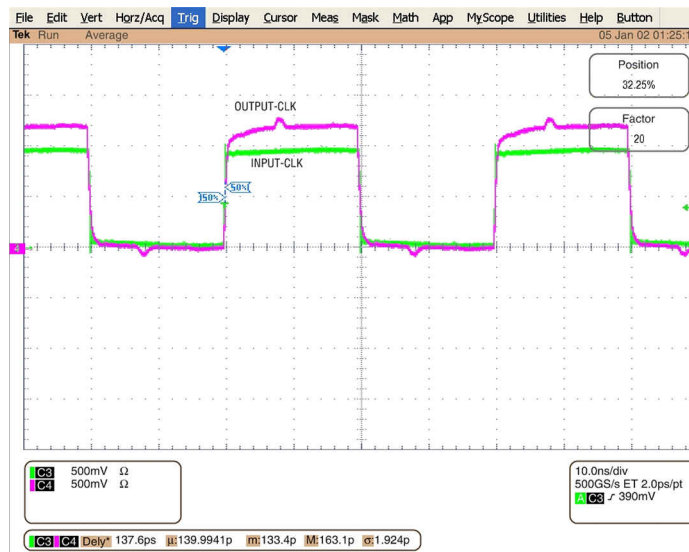


图 9-2. Input/Output Alignment in External Zero Delay Mode for LVCMOS Output

- ¹ In zero delay mode, all dividers should be programmed such that PLL can lock. On power-up in zero-delay mode, PLL would lock automatically
- ² For internal Zero delay mode, channel 2 is required. Channel 2 should not be powered down
- ³ "X" allows any possible bit-field value. It has no impact on the functionality

9.3.2 Phase-Locked Loop (PLL)

The CDCE6214-Q1 has a fully-integrated Phase-Locked Loop (PLL) circuit. The error between a reference phase and an internal feedback phase is compared at the phase-frequency-detector. The comparison result is fed to a charge pump that is connected to an integrated loop filter. The control voltage resulting from the loop filter tunes an internal Voltage-Controlled Oscillator (VCO). The frequency of the VCO is fed through a feedback divider (N-counter) back to the PFD.

- Integer and Fractional-N PLL mode of operation.
- First-, Second-, or Third-Order MASH operation in Fractional mode.
- 24-bit Numerator and Denominator can be used to generate fractional frequencies with 0 ppb frequency accuracy.
- PFD operates between 1 MHz and 100 MHz.
- Live Lock Detector (R7[0] or PLL_LOCK in GPIO) provides PLL Lock status (in fractional mode and SSC enabled, lock detect window need to be widened. R50[10:8] = 7h). Additionally, sticky bit lock detect (R7[1]) detects if there was any temporary loss of lock.
- Integrated selectable loop filter components.
- For a 25-MHz PFD frequency, PFD bandwidth between 100 kHz and 1.6 MHz can be achieved to optimize PLL to input reference.
- Voltage-controlled oscillator (VCO) ranges from 2335 MHz to 2615 MHz.
- Supports 0.25% and 0.5% center and down spread Spread Spectrum Clocking (SSC) generation. Further, VCO also supports up to 0.5% SSC references at 100 MHz for PCIe clocking.

表 9-3. Common Clock Generator Loop Filter Settings

| f _{VCO} IN MHz | f _{PFD} IN MHz | BW IN MHz | PHASE MARGIN IN ° | DAMPING FACTOR | I _{CP} IN mA | C _{Pcap} IN pF | R _{Res} IN kΩ | C _{Zcap} IN pF |
|-------------------------|-------------------------|-----------|-------------------|----------------|-----------------------|-------------------------|------------------------|-------------------------|
| 2400 | 25 | 0.469 | 70 | 0.5 | 0.60 | 16.1 | 2.5 | 580 |
| 2400 | 50 | 0.938 | 70 | 2 | 0.60 | 8.2 | 2.5 | 276 |
| 2400 | 100 | 1.60 | 70 | 0.5 | 0.80 | 8.2 | 2.5 | 303 |
| 2457.6 | 61.44 | 1.04 | 70 | 1.15 | 0.60 | 9.2 | 2.0 | 331 |
| 2500 | 25 | 0.49 | 70 | 0.4 | 0.60 | 13.5 | 2.5 | 497 |
| 2500 | 50 | 0.93 | 70 | 1.0 | 0.60 | 11.7 | 2.5 | 386 |
| 2400 | 50 | 400 | 65 | 0.1 | 0.40 | 11.7 | 1.5 | 636 |

表 9-4. Common PLL Divider Settings ⁴

| INPUT FREQUENCY IN MHz | f _{PFD} IN MHz | OUTPUT FREQUENCY IN MHz | f _{VCO} | N-COUNTER DIVIDER VALUE | NUMERATOR | DENOMINATOR | PSA | OUTPUT DIVIDER |
|------------------------|-------------------------|-------------------------|------------------|-------------------------|-----------|-------------|-----|----------------|
| 25 | 50 | 100 | 2400 | 48 | NA | NA | 4 | 6 |
| 25 | 25 | 100 | 2400 | 96 | NA | NA | 4 | 6 |
| 25 | 50 | 156.25 | 2500 | 50 | NA | NA | 4 | 4 |
| 25 | 25 | 25 | 2400 | 96 | NA | NA | 4 | 24 |
| 25 | 25 | 24.576 | 2457.6 | 98 | 5071614 | 16682942 | 4 | 25 |
| 25 | 25 | 148.5 | 2376 | 95 | 664983 | 16624579 | 4 | 4 |

9.3.2.1 PLL Configuration and Divider Settings

$$f_{PFD} = F_{in} / F_{factor}$$

F_{factor} is determined by R25[7:0] - ip_ref_div. F_{factor} = 0.5 when ip_ref_div=0, F_{factor} = ip_ref_div, otherwise.

$$f_{VCO} = f_{PFD} \times (N + Num/Den).$$

N is set by R30[14:0] - PLL_NDIV. Num is the numerator of the fraction, set by {R32[7:0],R31[15:0]}. Den is the denominator of the fraction, set by R34[7:0],R33[15:0]. When {R34[7:0],R33[15:0]} = 0, Den=2²⁴.

⁴ Fractional Mode settings are based on DCO mode step size of 0.1ppm

The sigma delta modulator supports different order of MASH to shape the quantization noise. For Integer mode, R27[1:0] is set as 0h. For fractional mode, it can be set to 1h, 2h or 3h for first, second and third order, respectively.

In integer mode, PLL is configured in single-ended PFD configuration by setting R51[6]=1h. In Fractional mode, PLL should be configured in Differential PFD configuration by setting R51[6]=0h. Further, R51[10] is set as 1h in fractional mode and 0h in Integer mode.

9.3.2.2 Spread Spectrum Clocking

The energy of the harmonics from the rectangular clock signal can be spread over a certain frequency range. This frequency deviation leads to lowered average amplitude of the harmonics. This can help to mitigate electromagnetic interference (EMI) challenges in a system when the receiver supports this mode of operation. The modulation shape is triangular.

The SSC clock is generated through the fractional-N PLL. When SSC is enabled, SSC clock is available on all clock sourced from the PLL. Reference clock or PFD clock is available on the OUT1 – OUT4 pins.

Down spread and center spread are supported. The following modes are supported.

- PFD frequencies: Either 25 MHz or 50 MHz.
- Down spread: -0.25% and $\pm 0.5\%$
- Center spread: $\pm 0.25\%$ and $\pm 0.5\%$

Pre-configured settings are available to select any of these combinations.

Using these pre-configured settings, fmod of 31.5 kHz is synthesized for 100-MHz output clock.

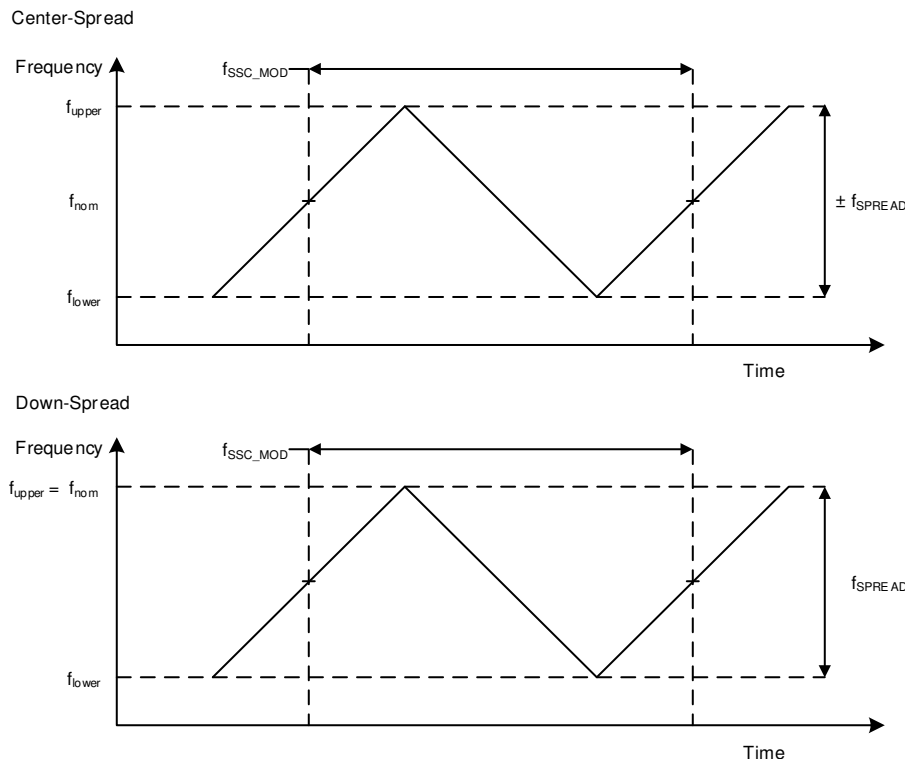


图 9-3. Spread Spectrum Clock

表 9-5. Spread Spectrum Settings ^{5 6}

| R41[15] - SSC_EN | R42[5] - SSC_TYPE | R42[3:1] - SSC_SEL | DESCRIPTION |
|------------------|-------------------|--------------------|---|
| 0h | X | X | No SSC modulation at output |
| 1h | 0h | X | Down spread SSC modulation. SSC spread is determined by ssc_sel |
| 1h | 1h | X | Center spread SSC modulation. SSC spread is determined by ssc_sel |
| 1h | X | 0h | 25-MHz PFD, +/- 0.25% for Center spread, -0.25% for Down spread. |
| 1h | X | 1h | 25-MHz PFD, +/- 0.50% for Center spread, -0.50% for Down spread. |
| 1h | X | 2h | 50-MHz PFD, +/- 0.25% for Center spread, -0.25% for Down spread. |
| 1h | X | 3h | 50-MHz PFD, +/- 0.50% for Center spread, -0.50% for Down spread. |
| 1h | X | 4h-7h | Do not use |

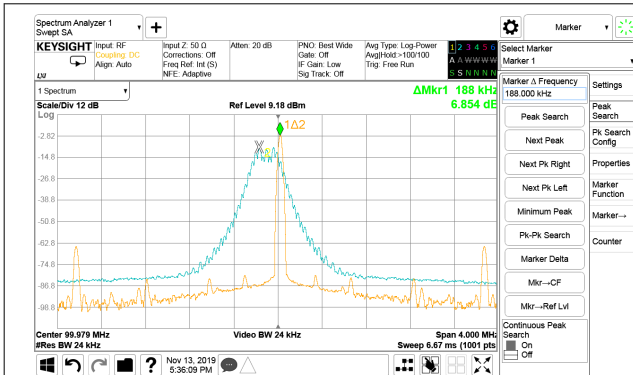


图 9-4. 100 MHz With - 0.25% Down Spread With and Without Trace

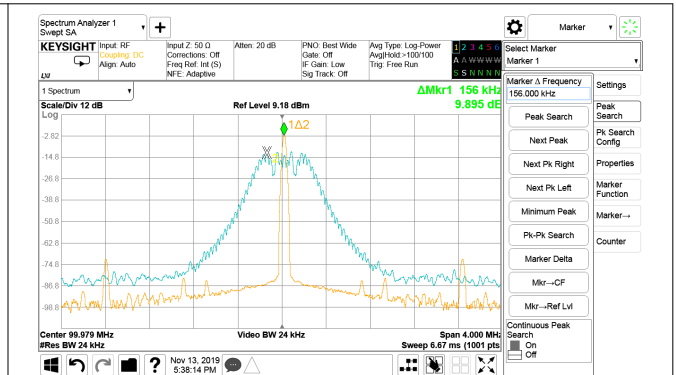


图 9-5. 100 MHz With +/- 0.25% Center Spread With and Without Trace

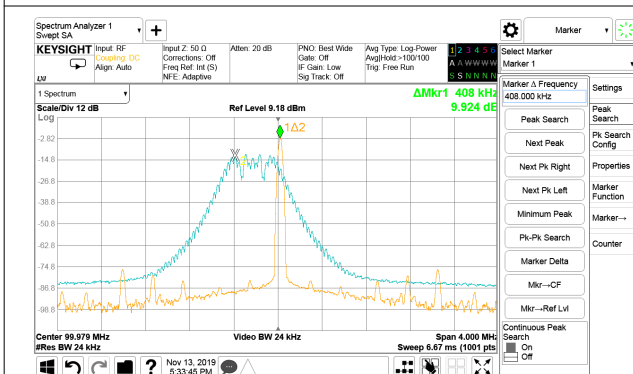


图 9-6. 100 MHz With - 0.5% Down Spread With and Without Trace

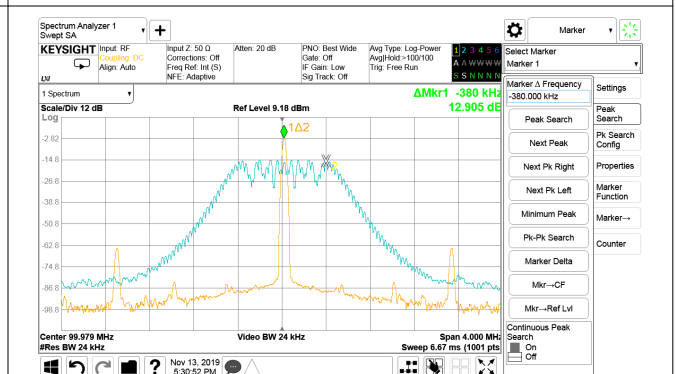


图 9-7. 100 MHz With +/- 0.5% Center Spread With and Without Trace

⁵ X signifies that this bitfield can take any value
⁶ For any other SSC spread and modulation rate, please contact TI representative.

表 9-6. PCI Express Compliance Measurement

| NO. | CLASS | DATA RATE | ARCHITECTURE | MEASURED PNA METHOD | MEASURED SCOPE METHOD | SPEC LIMIT | RESULT |
|-----|-------|-----------|--------------|---------------------|-----------------------|------------|--------|
| 1 | Gen4 | 16 Gb/s | CC | 195 fs | 260 fs | 500 fs | PASS |
| 2 | Gen4 | 16 Gb/s | SRIS | - | 490 fs | 500 fs | PASS |
| 3 | Gen5 | 32 Gb/s | CC | 87 fs | 111 fs | 150 fs | PASS |
| 4 | Gen5 | 32 Gb/s | SRIS | - | 157 fs | * | * |

9.3.2.3 Digitally-Controlled Oscillator/ Frequency Increment and Decrement - Serial Interface Mode and GPIO Mode

In this mode, the output clock frequency can be incremented or decremented by a fixed frequency step. The frequency step size is determined by the register R43[15:0]. This value is added or subtracted to the numerator of the sigma-delta modulator. Various bit fields as shown in **BROKEN_LINK** can be used to exercise this functionality. Every rising edge of **FREQ_INC** signal increases the output frequency, while every rising edge of **FREQ_DEC** signal decreases the output frequency. There are two ways to trigger the increment or decrement:

1. Appropriate configuration of the GPIOs and sending **FREQ_INC/FREQ_DEC** signal through an external microcontroller or ASIC.
2. Using register bit fields controlled through serial interface.

表 9-7. Register Settings for Frequency Increment/Decrement Functionality

| REGISTER BIT ADDRESS | REGISTER BIT FIELD NAME | DESCRIPTION |
|----------------------|----------------------------|--|
| R3[3] | FREQ_INC_DEC_EN | Enables/Disables DCO mode |
| R3[4] | FREQ_INC_DEC_REG_MODE | Selects DCO trigger through GPIOs or Serial Interface. |
| R3[6:5] | FREQ_DEC_REG, FREQ_INC_REG | Generates FREQ_INC/FREQ_DEC signal through serial Interface |
| R43[15:0] | FREQ_INC_DEC_DELTA | Frequency Increment/Decrement step size |

表 9-8. Computing Divider Settings in DCO Mode

| PARAMETERS | VALUE (EXAMPLE) | DESCRIPTION |
|---|-----------------|---|
| Input PFD Frequency (F_{PFD}) | 25 MHz | Set according to F_{PFD} . |
| Expected VCO Frequency (F_{VCO}) | 2457.6 MHz | F_{VCO} is set within the operating VCO range of 2335 MHz - 2625 MHz. F_{VCO} is selected such that $PSA/PSB/Output\ Divider$ is Integer. |
| Expected Output Frequency (F_{OUT}) | 24.576 MHz | $PSA = 4$, $IOD = 25$. $F_{VCO} = PSA \times IOD \times F_{OUT}$. |
| Expected step size (in ppm) (F_{step}) | 0.1 | Every rising edge of FREQ_INC/FREQ_DEC would change the output by this step size. |
| N-divider Value (N) | 98 | $INT(F_{VCO}/F_{PFD})$ |
| Minimum Numerator value to meet 0ppb accuracy (Num) | 76 | These values are computed to meet accuracy requirement at output. Should be less than 2^{24} . |
| Minimum Denominator to meet 0ppb accuracy (Den) | 250 | |
| Minimum Denominator value to meet ppm step size ($F_{DEN,min}$) | 101725.26 | $1/(F_{step} \times 1e6) / (F_{VCO}/F_{PFD})$ |
| Final Denominator value ($F_{DEN,final}$) | 500000 | $F_{DEN,final}$ should be greater than $F_{DEN,min}$ and less than 2^{24} . $F_{DEN,final}$ and $F_{NUM,final}$ should be integer multiple of Den and Num respectively. $F_{DEN,final}/Den = F_{NUM,final}/Num$ |
| Final Numerator value ($F_{NUM,final}$) | 152000 | |
| Increment/ Decrement step size | 5 | This value should be less than $2^{16}-1$. $F_{DEN,final}$ should be closest integer multiple of $F_{DEN,min}$. |

9.3.3 Clock Distribution

The VCO output connects to two individually configurable pre-scalar dividers sourcing the on-chip clock distribution - PSA and PSB. PSA and PSB can be configured as division value of /4, /5 or /6 independently.

The clock distribution consists of four output channels. Each output channel contains an integer divider (IOD) with glitchless switching and synchronization capabilities.

IOD can be sourced from either the PSA, the PSB, or the Reference Clock. IOD can be bypassed to provide a Reference clock at the output.

There are five output channels - OUT0, OUT1, OUT2, OUT3, and OUT4.

The OUT0 is a slew-rate controllable LVCMOS output. Either the reference clock or PFD clock can be routed to this output through the clock distribution network.

The OUT1 and OUT4 are identical output channels. The output buffers in this channel are compatible with various signaling standards - LVCMOS, LP-HCSL, and LVDS-like.

The OUT2 and OUT3 are identical output channels. The output buffers in this channel are compatible with various signaling standards - LP-HCSL and LVDS-like.

- The LP-HCSL output buffer can be directly connected to the receiver without any termination resistor to GND. The output impedance of LP-HCSL is trimmed to 50 Ω ± 10%. A series resistor can be used to adapt to the trace impedance.
- The LVDS-like requires a differential termination connected between the positive and negative polarity output pins. The termination can be connected directly or through an AC-coupling capacitor. For a 50-Ω system, a 100-Ω differential termination is appropriate.
- LVCMOS outputs are designed for capacitive loads only. The polarity of the positive and negative output pins can be configured individually.

The differential buffers support wide range of output frequencies up to 328.125 MHz. LVCMOS supports up to 200 MHz.

表 9-9. Configuring Input Reference/PFD/PLL Clock to Output ⁷

| REGISTER BIT ADDRESS | REGISTER BIT FIELD NAME | DESCRIPTION |
|----------------------|---|--|
| R25[10] | IP_BYP_OUT0_EN | Enables Reference Clock/PFD Clock to OUT0. |
| R25[9] | REF_CH_MUX | Selects between PFD Clock or Input Reference Clock |
| R25[14:11] | IP_REF_TO_OUT4_EN, IP_REF_TO_OUT3_EN, IP_REF_TO_OUT2_EN, IP_REF_TO_OUT1_EN | Selects reference clock to OUT1-OUT4 |
| R56[15:14] | CH1_MUX | Clock selection MUX control for OUT1 |
| R62[15:14] | CH2_MUX | Clock selection MUX control for OUT2 |
| R67[15:14] | CH3_MUX | Clock selection MUX control for OUT3 |
| R72[15:14] | CH4_MUX | Clock selection MUX control for OUT4 |

表 9-10. Configuring Clock Distribution Network

| REGISTER BIT ADDRESS | REGISTER BIT FIELD NAME | DESCRIPTION |
|----------------------|-------------------------|-------------------------------------|
| R47[6:5] | PLL_PSB | Programmable Pre-scalar divider PSB |
| R47[4:3] | PLL_PSA | Programmable Pre-scalar divider PSA |
| R56[13:0] | CH1_DIV | OUT1 Integer Divider value |
| R62[13:0] | CH2_DIV | OUT2 Integer Divider value |
| R67[13:0] | CH3_DIV | OUT3 Integer Divider value |

⁷ It is recommended to disable any clock when not in use to reduce crosstalk

表 9-10. Configuring Clock Distribution Network (continued)

| REGISTER BIT ADDRESS | REGISTER BIT FIELD NAME | DESCRIPTION |
|----------------------|-------------------------|----------------------------|
| R72[13:0] | CH4_DIV | OUT4 Integer Divider value |

表 9-11. Configuring LVCMOS Output Buffer ^{8 9}

| REGISTER BIT ADDRESS | REGISTER BIT FIELD NAME | DESCRIPTION |
|----------------------|--|--|
| R78[12] | CH0_EN | Enables OUT0 LVCMOS Buffer |
| R79[3:0] | CH0_CMOS_SLEW_RATE_CTRL | Controls output slew rate of OUT0 LVCMOS Buffer |
| R59[14], R75[14] | CH1_CMOSN_EN, CH4_CMOSP_EN | Enables OUT1N/OUT4P LVCMOS Buffer |
| R59[13], R75[13] | CH1_CMOSP_EN, CH4_CMOSN_EN | Enables OUT1P/OUT4N LVCMOS Buffer |
| R59[12], R75[12] | CH1_CMOSN_POL, CH4_CMOSP_POL | Sets output polarity of OUT1N/OUT4P LVCMOS Buffer |
| R59[11], R75[11] | CH1_CMOSP_POL, CH4_CMOSN_POL | Sets output polarity of OUT1P/OUT4N LVCMOS Buffer |
| R60[3:0], R76[3:0] | CH1_CMOS_SLEW_RATE_CTRL, CH4_CMOS_SLEW_RATE_CTRL | Controls output slew rate of OUT1/OUT4 LVCMOS Buffer |

表 9-12. Configuring LP-HCSL Output Buffer ^{10 11 12}

| REGISTER BIT ADDRESS | REGISTER BIT FIELD NAME | DESCRIPTION |
|------------------------------------|--|---|
| R57[14], R63[13], R68[13], R73[13] | CH1_HCSL_EN, CH2_HCSL_EN, CH3_HCSL_EN, CH4_HCSL_EN | Enables LP-HCSL buffer on OUT1/OUT2/OUT3/OUT4 |

表 9-13. Configuring LVDS-Like Output Buffer ^{13 14 15}

| REGISTER BIT ADDRESS | REGISTER BIT FIELD NAME | DESCRIPTION |
|---|--|---|
| R59[15], R65[11], R70[11], R75[15] | CH1_LVDS_EN, CH2_LVDS_EN, CH3_LVDS_EN, CH4_LVDS_EN | Enables LVDS-like buffer on OUT1/OUT2/OUT3/OUT4 |
| R60[15:12], R66[3:0], R71[3:0], R76[9:6] | CH1_DIFFBUF_IBIAS_TRIM, CH2_DIFFBUF_IBIAS_TRIM, CH3_DIFFBUF_IBIAS_TRIM, CH4_DIFFBUF_IBIAS_TRIM | Sets the output swing and output common mode of OUT1/OUT2/OUT3/OUT4 |
| R60[11:10], R66[5:4], R71[5:4], R76[5:4] | CH1_LVDS_CMTRIM_INC, CH2_LVDS_CMTRIM_INC, CH3_LVDS_CMTRIM_INC, CH4_LVDS_CMTRIM_INC | Increases the output common mode of OUT1/OUT2/OUT3/OUT4. 2.5 V/3.3 V mode only. |
| R60[5:4], R65[14:13], R71[10:9], R77[1:0] | CH1_LVDS_CMTRIM_DEC, CH2_LVDS_CMTRIM_DEC, CH3_LVDS_CMTRIM_DEC, CH4_LVDS_CMTRIM_DEC | Decreases the output common mode of OUT1/OUT2/OUT3/OUT4. 2.5 V/3.3 V mode only. |

9.3.3.1 Glitchless Operation

The bit fields `ch{x}_glitchless_en` can be used to enable glitchless output divider update. This feature ensures that the high pulse of a clock period is not cut off by the output divider update process. It also ensures that setup

⁸ Multiple output buffers should not be enabled at the same time

⁹ Based on the VDDO levels, `ch1_1p8vdet`, `ch2_1p8vdet`, `ch3_1p8vdet`, `ch4_1p8vdet` should be set accordingly. When setting for 1.8V, `safety_1p8v_mode` should be set.

¹⁰ Multiple output buffers should not be enabled at the same time

¹¹ External termination not needed. Voltage mode driver.

¹² Based on the VDDO levels, `ch1_1p8vdet`, `ch2_1p8vdet`, `ch3_1p8vdet`, `ch4_1p8vdet` should be set accordingly. When setting for 1.8V, `safety_1p8v_mode` should be set.

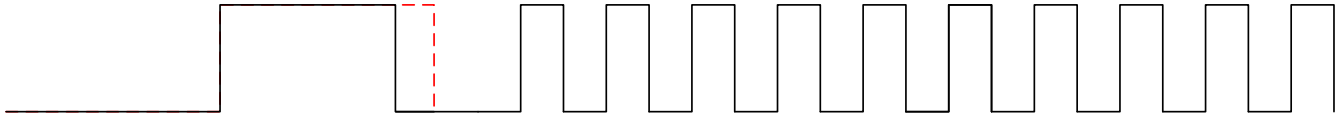
¹³ Multiple output buffers should not be enabled at the same time.

¹⁴ 100 Ω differential termination needed in DC-coupled mode. 50 Ω single ended or 100 Ω differential termination needed in AC-coupled mode

¹⁵ Based on the VDDO levels, `ch1_1p8vdet`, `ch2_1p8vdet`, `ch3_1p8vdet`, `ch4_1p8vdet` should be set accordingly. When setting for 1.8V, `safety_1p8v_mode` should be set.

and hold time of a receiver is not violated. The low pulse in the transition from earlier period to the new period is extended accordingly.

Glitch-Less Divider Disabled:



Glitch-Less Divider Enabled:

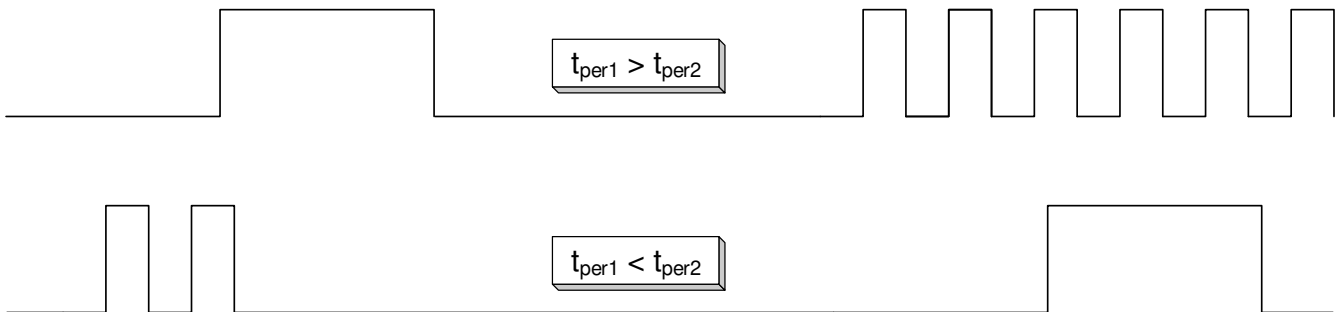


图 9-8. Glitchless Divider Update

9.3.3.2 Divider Synchronization

The output dividers can be reset in a deterministic way. This can be achieved using the sync bit or PDN pin. The level of the pin is qualified internally using the reference frequency at the PFD input. A low level on the SYNCN pin or sync bit will mute the outputs. A high level will synchronously release all output dividers to operation, so that all outputs share a common rising edge. The first rising edge can be individually delayed in steps of the respective pre-scalar period, up to 32 cycles using `ch{x}_sync_delay`. This allows the user to compensate external delays like routing mismatch, cables, or inherent delays introduced by logic gates in an FPGA design. Each channel can be included or excluded from the SYNC process. Divider synchronization can be enabled individually by `ch{x}_sync_en`.

For a deterministic behavior over power-cycles seen from input to output the reference divider must be set to 1. It should not divide the reference clock nor should the reference doubler be used.

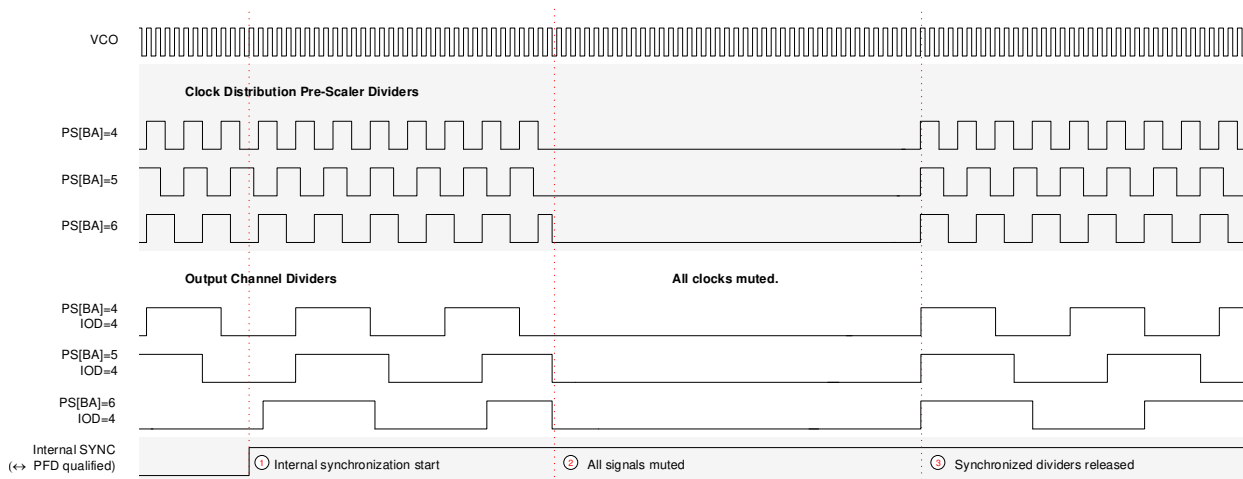


图 9-9. Output Divider Synchronization

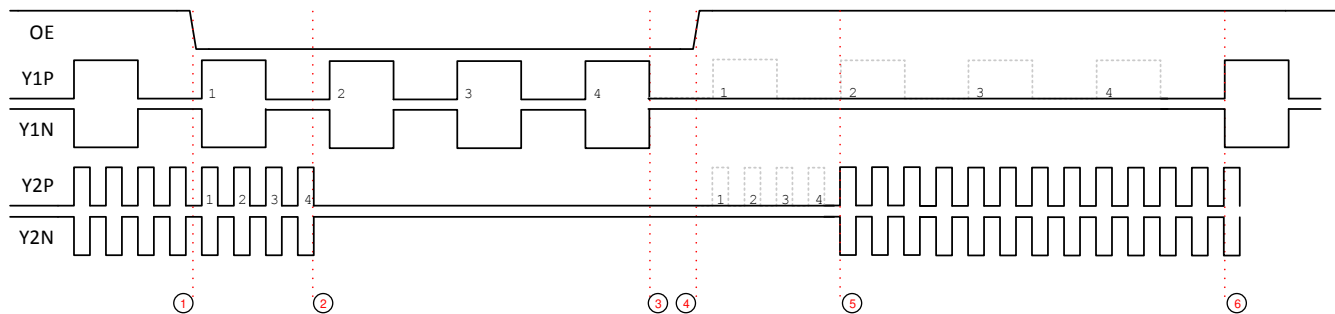
9.3.3.3 Global and Individual Output Enable

The output enable functionality allows the user to enable or disable all or a specific output buffer. The bypass copy on OUT0 is excluded from the global output enable signal. When an output is disabled, it drives a configurable mute-state. When the serial interface is deactivated one can use all individual output enable signals at the same time. The individual output enable signal controls the respective output channel integer divider to gate the clock, therefore each integer divider must be active.

The individual output enable signal enables and disables the respective output in a deterministic way. Therefore the high and low level of the signal is qualified by counting four cycles of the respective output clock.

1. The OE falling edge disables the output. The output is enabled for 4 cycles after asserting the Output Enable of a channel. This will enable any further operation in the system after OE is asserted.
2. The OE rising edge enables the output. Outputs starts toggling after 4 internal clock cycles.

MUTE_SEL= Logic Low



MUTE_SEL= Logic High

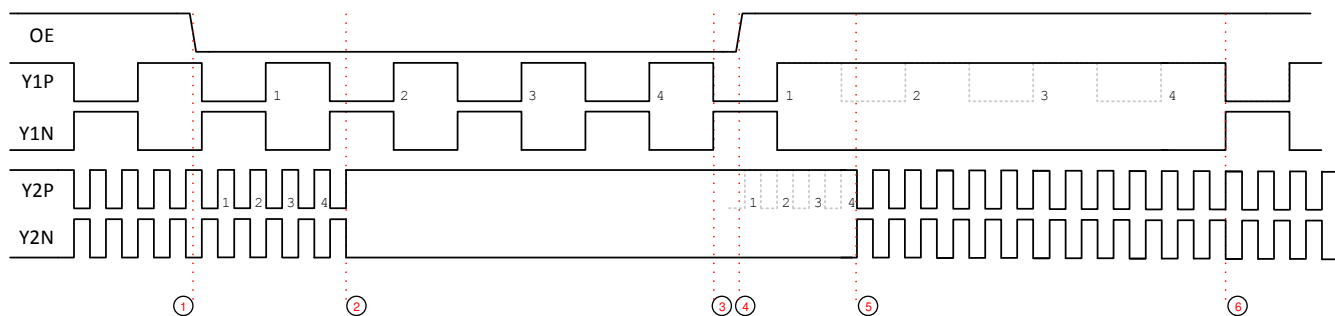


图 9-10. Individual Output Enable and Disable

表 9-14. Glitch-less Operation, Divider Synchronization and Global/Individual OE Settings

| REGISTER BIT ADDRESS | REGISTER BIT FIELD NAME | DESCRIPTION |
|--------------------------------|---|---|
| R0[14] | PDN_INPUT_SEL | Configures PDN pin as PDN or SYNCN |
| R0[5] | SYNC | Generates SYNC signal through serial interface |
| R57[9], R63[9], R68[9], R73[9] | CH1_GLITCHLESS_EN, CH2_GLITCHLESS_EN, CH3_GLITCHLESS_EN, CH4_GLITCHLESS_EN | Enables Glitch-less switching for OUT1/ OUT2/OUT3/OUT4 |
| R57[3], R63[3], R68[3], R73[3] | CH1_SYNC_EN, CH2_SYNC_EN, CH3_SYNC_EN, CH4_SYNC_EN | Enables SYNC for OUT1/OUT2/OUT3/OUT4 |
| R57[1], R63[1], R68[1], R73[1] | CH1_MUTESEL, CH2_MUTESEL, CH3_MUTESEL, CH4_MUTESEL | Sets Output level when mute on OUT1/ OUT2/OUT3/OUT4 |
| R57[0], R63[0], R68[0], R73[0] | CH1_MUTE, CH2_MUTE, CH3_MUTE, CH4_MUTE | Mutes output on OUT1/OUT2/OUT3/OUT4 |

9.3.4 Power Supplies and Power Management

The CDCE6214-Q1 provides multiple power supply pins. Each of the power supplies supports 1.8 V, 2.5 V, or 3.3 V individually. Internal low-dropout regulators (LDO) source the internal blocks and allow each pin to be supplied with its individual supply voltage. The VDDREF pin supplies the control pins and the serial interface, therefore any pullup resistors shall be connected to the same domain as VDDREF.

The device is very flexible with respect to internal power management. Each block offers a power-down bit and can be disabled to save power when the block is not required. The available bits are illustrated in [表 9-15](#). The bypass output Y0 is connected to the pdn_ch4 bit. Each output channel has a bit which should be adapted to the applied supply voltage, ch[4:1]_1p8vdet.

表 9-15. Power Management

| VDDREF | VDDVCO | VDDO_12 | VDDO_34 |
|-------------------|----------------------------|-------------------|-------------------|
| R0[1] - POWERDOWN | R0[1] - POWERDOWN | R0[1] - POWERDOWN | R0[1] - POWERDOWN |
| | R5[8] - PLL_VCOBUFF_LDO_PD | R4[4] - CH1_PD | R4[6] - CH3_PD |
| | R5[7] - PLL_VCO_LDO_PD | R4[5] - CH2_PD | R4[7] - CH4_PD |
| | R5[6] - PLL_VCO_BUFF_PD | | |
| | R5[5] - PLL_CP_LDO_PD | | |
| | R5[4] - PLL_LOCKDET_PD | | |
| | R5[3] - PLL_PSB_PD | | |
| | R5[2] - PLL_PSA_PD | | |
| | R5[1] - PLL_PFD_PD | | |
| | R53[6] - PLL_NCTR_EN | | |
| | R53[3] - PLL_CP_EN | | |

9.3.5 Control Pins

The ultra-low power clock generator is controlled by multiple LVCMOS input pins.

HW_SW_CTRL pin acts as EEPROM page select. The CDCE6214-Q1 clock generator contains two pages of configuration settings. The level of this pin is sampled after device power up. A low level selects page zero. A high level selects page one. The HW_SW_CTRL pin is a tri-level input pin. This third voltage level is automatically applied by an internal voltage divider. The mid-level is used to select an internal default where the serial interface is enabled.

PDN/SYNCRN (pin 8) , SCL (pin 12), and SDA (pin 19) have a secondary functionality and can act as general-purpose inputs and outputs (GPIO). This means that either the serial interface or the GPIO functionality can be active.

PDN/SYNCRN resets the internal circuitry and is used in the initial power-up sequence. The pin can be reconfigured to act as synchronization input. The differential outputs are kept in mute while SYNCRN is low. When SYNCRN is high, outputs are active.

表 9-16. Control and GPIO Pins

| PIN NO. | NAME | TYPE | 2-LEVEL INPUT | 3-LEVEL INPUT | OUTPUT | TERMINATION |
|---------|------------|--------------|---------------|---------------|--------|---|
| 23 | HW_SW_CTRL | Input | - | Yes | - | PUPD |
| 20 | GPIO1 | Input/Output | Yes | - | Yes | PU (when Input) |
| 19 | GPIO2 | Input/Output | Yes | - | Yes | Open-Drain I/O in I ² C mode, CMOS (Input) |
| 12 | GPIO3 | Input | Yes | - | - | - |
| 11 | GPIO4 | Input/Output | Yes | - | Yes | PU (when Input) |
| 8 | PDN | Input | Yes | - | - | PU (when Input) |
| 4 | REFSEL | Input | - | Yes | - | PUPD |

表 9-17. GPIO Input/Output Signal List

| ABBREVIATION | TYPE | DESCRIPTION |
|--------------|--------|---|
| FREQ_INC | Input | Frequency Increment; Increments the MASH numerator |
| FREQ_DEC | Input | Frequency Decrement; Decrements the MASH numerator |
| OE (global) | Input | Enables or disables all differential outputs Y[4:1] (bypass not affected) |
| SSC_EN | Input | Enables or disables SSC. |
| OE1 | Input | Enables or disables OUT1 |
| OE2 | Input | Enables or disables OUT2 |
| OE3 | Input | Enables or disables OUT3 |
| OE4 | Input | Enables or disables OUT4 |
| PLL_LOCK | Output | PLL Lock Status. 0 = PLL out of lock; 1 = indicates PLL in lock |

9.4 Device Functional Modes

9.4.1 Operation Modes

The operating modes listed in 表 9-18 can be set, and the GPIOs configured. An operating mode change only becomes effective when it is loaded from the EEPROM after a power cycle.

表 9-18. Modes of Operations

| DESCRIPTION | MODE | REFSEL | HW_SW_CTRL | GPIO1 | GPIO2 | GPIO3 | GPIO4 |
|-------------------------|-----------------------|--------|------------|-------|-------|-------|-------|
| I ² C + GPIO | Fall-back | M | M | I/O | SDA | SCL | I/O |
| OE | Pin Mode | L/H | L/H | OE1 | OE2 | OE3 | OE4 |
| I ² C + GPIO | Serial Interface Mode | L/H | L/H | I/O | SDA | SCL | I/O |

9.4.1.1 Fall-Back Mode

As the programming interface can be intentionally deactivated using the EEPROM, an accidental disabling of the I²C blocks further access to the device. The serial interface can be forced using the fall-back mode. To enter this mode, the user leaves pin 4 and pin 23 floating while the supply voltage is applied to VDDREF. In this mode, EEPROM Read at power up is bypassed and device boots in default mode. In this mode, pin 11 is pre-configured as an input and pin 20 is configured as an output. After powering up in fall-back mode, the device can be re-programmed through serial interface and be re-configured for normal operation. EEPROM can also be re-programmed. The PLL would not be auto-calibrated, however, and the I²C interface would be active. This mode would allow the user to fully configure the device before re-locking the PLL.

9.4.1.2 Pin Mode

In pin mode, the pins 12 and 19 are input pins which act as individual output enable pins. Together with pins 11 and 20, this allows for one output enable pin per output channel.

9.4.1.3 Serial Interface Mode

In serial interface mode, pins 12 and 19 are configured as an I²C interface.

9.5 Programming

9.5.1 I²C Serial Interface

The CDCE6214-Q1 ultra-low power clock generator provides an I²C-compatible serial interface for register and EEPROM access. The device is compatible to standard-mode I²C at 100 kHz and the fast-mode I²C at 400-kHz clock frequency.

1. In fall-back mode, I²C slave address = 67h.
2. In other modes, I²C slave address = 68h (Default).

3. The LSB bit of the device can be programmed in the EEPROM. For example, if I2C_A0 is programmed H in Page 0 of EEPROM, setting HW_SW_CTRL=0 would set I²C address as 69h.
4. Two devices with EEPROM + 1 device in fall-back mode can be used on the same I²C bus with addresses 67h, 68h and 69h.

表 9-19. I²C-Compatible Serial Interface, Slave Address Byte ^{16 17}

| | | | | | | | |
|---------------------|----------|----------|----------|----------|----------|----------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Slave Address [6:0] | | | | | | | R/W# Bit |

表 9-20. I²C-Compatible Serial Interface, Programmable Slave Address ^{18 19}

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | HW_SW_SEL | DESCRIPTION |
|----|----|----|----|----|----|--------|-----------|----------------|
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | MID | Fall-back Mode |
| 1 | 1 | 0 | 1 | 0 | 0 | I2C_A0 | LOW | EEPROM Page 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | I2C_A0 | HIGH | EEPROM Page 1 |

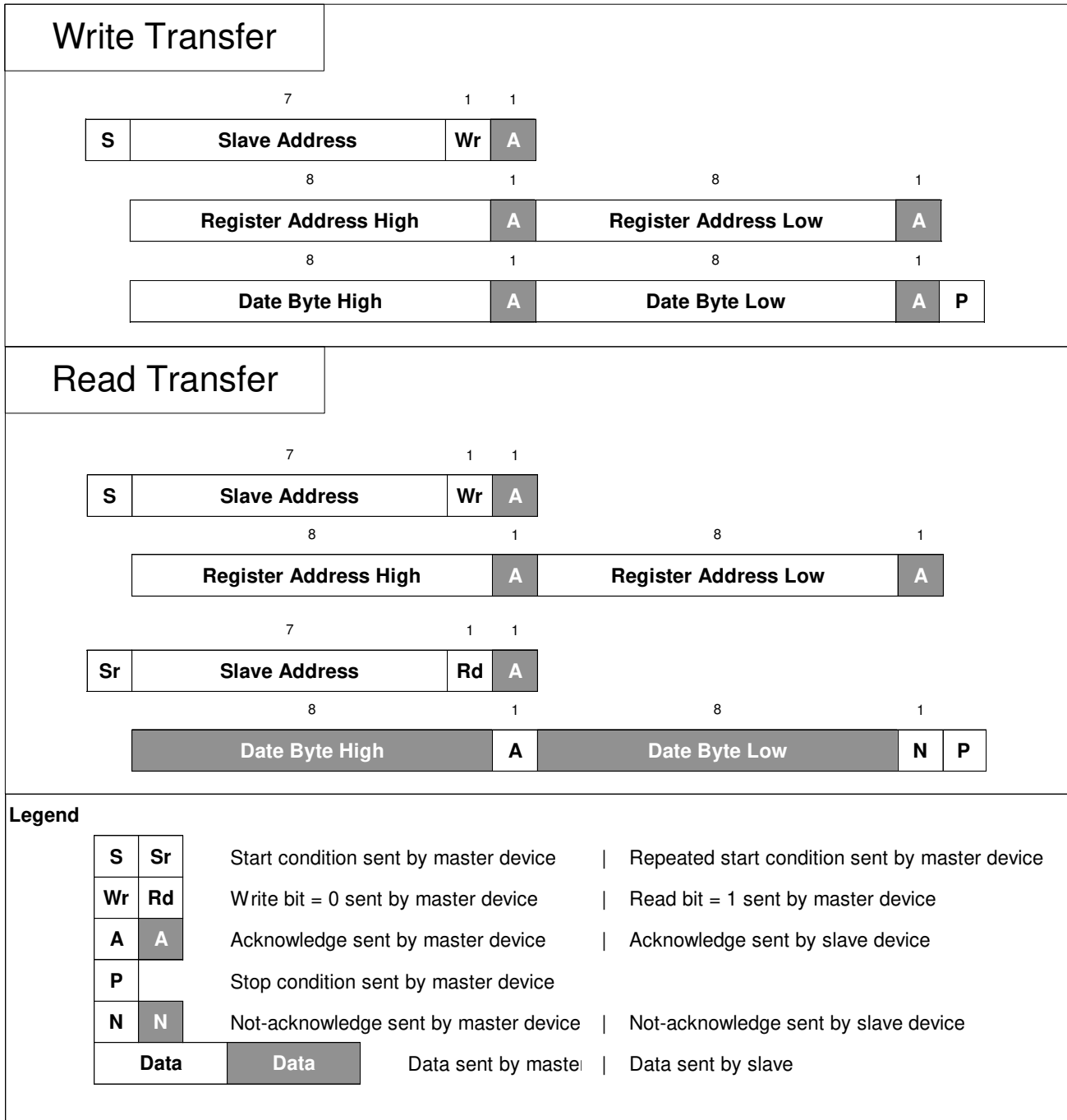
The serial interface uses the following protocol as shown in [图 9-11](#). The slave address is followed by a word-wide register offset and a word-wide register value.

¹⁶ The slave address consists of two sections. The hardwired MSBs A[6:1] and the software-selectable LSBs A[0].

¹⁷ The R/W# bit indicates a read (1) or a write (0) transfer.

¹⁸ In EEPROM Page 0, Serial Interface is not available. Device configured in Pin Mode

¹⁹ In EEPROM Page 1, I2C_A0 is programmed as 0, Expected Slave Address is 68h



Legend

| | | | |
|------|------|---------------------------------------|--|
| S | Sr | Start condition sent by master device | Repeated start condition sent by master device |
| Wr | Rd | Write bit = 0 sent by master device | Read bit = 1 sent by master device |
| A | A | Acknowledge sent by master device | Acknowledged sent by slave device |
| P | | Stop condition sent by master device | |
| N | N | Not-acknowledge sent by master device | Not-acknowledge sent by slave device |
| Data | Data | Data sent by master | Data sent by slave |

图 9-11. I²C-Compatible Serial Interface, Supported Protocol

9.5.2 EEPROM

9.5.2.1 EEPROM - Cyclic Redundancy Check

The device contains a cyclic redundancy check (CRC) function for reads from the EEPROM to the device registers. At start-up, the EEPROM will be read internally and a CRC value calculated. One of the EEPROM words contains an earlier stored CRC value. The stored and the actual CRC value are compared and the result transferred to register. The CRC calculation can be triggered again by writing a 1 to the update_crc bit. A mismatch between stored and calculated CRC value is informational only and non-blocking to the device

operation. Just reading back the CRC status bit and the live CRC value can speed up in-system EEPROM programming and avoid reading back each word of the EEPROM for known configurations.

The polynomial used is CCITT-CRC16: $x^{16} + x^{12} + x^5 + 1$.

9.5.2.2 Recommended Programming Procedure

TI recommends programming the registers of the device in the following way:

1. Read-back factory default EEPROM page configuration. Each device will have different EEPROM base page configuration.
2. Modify register bits.
3. Ensure that ee_lock is set to 5h (unlock) when overwriting the EEPROM.
4. Program register addresses in descending order from 0x53 to 0x00 including all register addresses with reserved values.

9.5.2.3 EEPROM Access

Note

The EEPROM word write access time is typically 8 ms.

There are two methods to write into the internal EEPROM

1. Register Commit method.
2. EEPROM Direct Access Method

Use the following steps to bring the device into a good known configuration.

1. Power down all the supplies.
2. Apply PDN = LOW.
3. REFSEL and HW_SW_CTRL pins can be High, Low or High-Z. For factory programmed device, I²C interface is not available when HW_SW_CTRL is LOW.
4. Apply power supplies to all VDD pins. When device operation is not required, apply power supply to VDDREF.
5. Apply PDN = HIGH.
6. Use the I²C interface to configure the device.

9.5.2.3.1 Register Commit Flow

In the Register Commit flow, all bits from the device registers are copied into the EEPROM. The recommended flow is:

1. Pre-configure the device as desired, except the serial interface using mode.
2. Write 1 to RECAL to calibrate the VCO in this operation mode.
3. Select the EEPROM page, to copy the register settings into, using REGCOMMIT_PAGE.
4. Unlock the EEPROM for write access with EE_LOCK = x5.
5. Start the register commit operation by writing 1 to REGCOMMIT.
6. Force a CRC update by writing a 1 to UPDATE_CRC.
7. Read back the calculated CRC in NVMLCRC.
8. Store the read CRC value in the EEPROM by writing 0x3F to NVM_WR_ADDR and then the CRC value to NVM_WR_DATA.

9.5.2.3.2 Direct Access Flow

In the EEPROM direct access flow, the EEPROM words are directly accessed using the address and the data bit-fields. The recommended flow is:

1. Prepare an EEPROM image consisting of 64 words of 16 bits each.
2. Unlock the EEPROM for write access with EE_LOCK = 0x5.
3. Write the initial address offset to the address bit-field. Write a 0x00 to NVM_WR_ADDR.

4. Loop through the EEPROM image from address 0 to 63 by writing each word from the image to NVM_WR_DATA. The EEPROM word address is automatically incremented by every write access to NVM_WR_DATA.

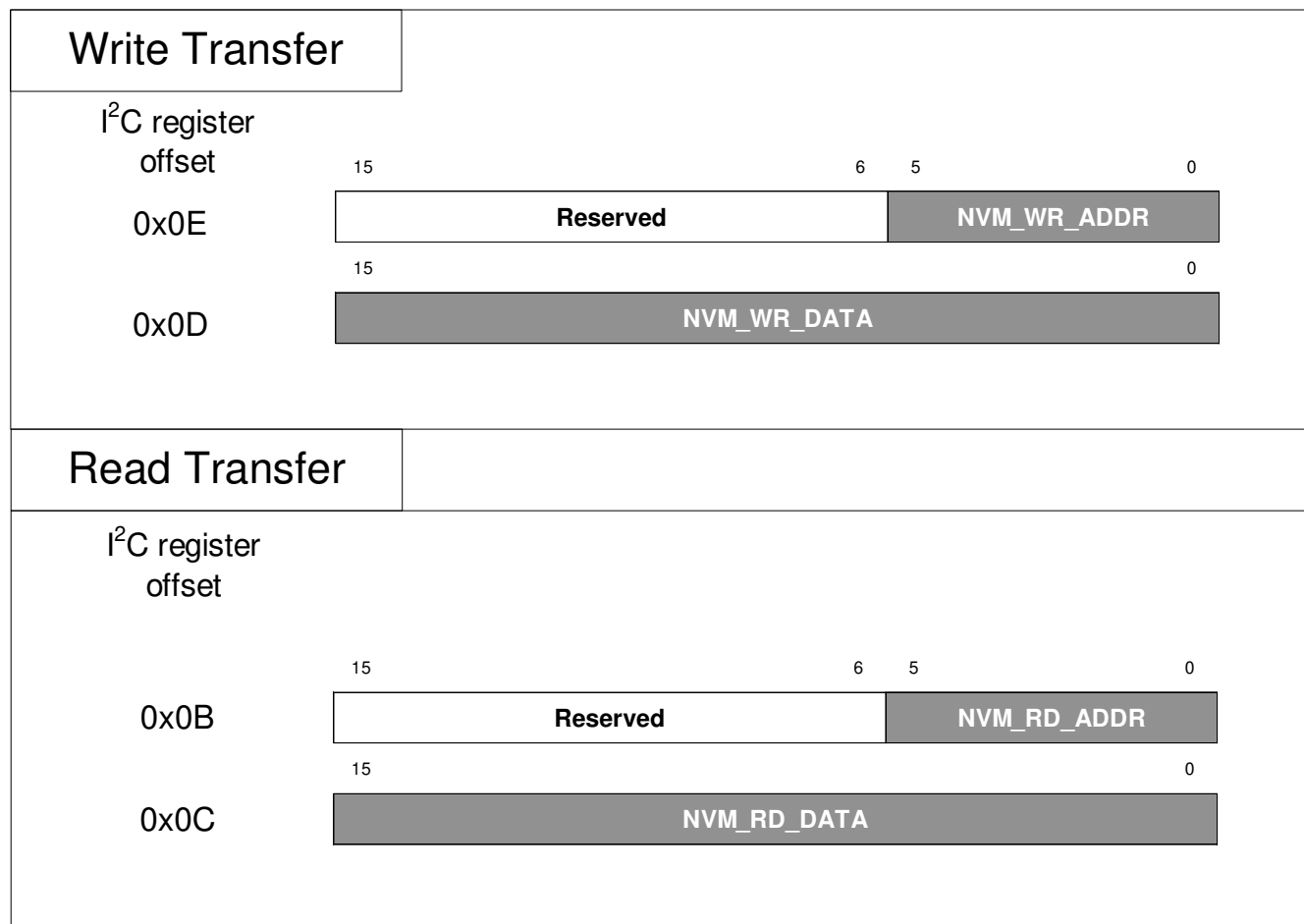


图 9-12. EEPROM Direct Access Using I²C

9.5.2.4 Register Bits to EEPROM Mapping

Register bits settings are mapped into EEPROM. EEPROM is divided into three segments:

- EEPROM Base Page: Selectable by connecting HW_SW_CTRL pin either to Logic 0 to Logic 1.
- EEPROM Page 0: Selectable by connecting HW_SW_CTRL pin to Logic 0.
- EEPROM Page 1: Selectable by connecting HW_SW_CTRL pin to Logic 1.

表 9-21. EEPROM Mapping ^{20 21 22 23}

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|--------|--------|--------|--------|--------|----------|----------|----------|--------|--------|--------|-------|-------|-------|--------|-------|
| 0 | 0 | 1 | 1 | 1 | R5[8] | R5[7] | R5[6] | R5[5] | R5[4] | R5[1] | R4[3] | R4[2] | R4[1] | R4[0] | R3[9] | R0[3] |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | R15[5] | 1 |
| 2 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4 | R48[4] | R48[3] | R48[2] | R48[1] | R48[0] | R47[1 2] | R47[1 1] | R47[1 0] | R47[9] | R47[8] | R47[7] | 0 | 0 | 0 | 0 | 0 |

²⁰ Address Locations 0-15: EEPROM Base Page

²¹ Address Locations 16-39: EEPROM Page 0

²² Address Locations 40-63: EEPROM Page 1

²³ Bit locations marked in Red may vary from device to device

表 9-21. EEPROM Mapping ^{20 21 22 23} (continued)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 5 | 0 | R49[4] | R49[3] | R49[2] | R49[1] | R49[0] | R48[1 4] | R48[1 3] | R48[1 2] | R48[1 1] | R48[1 0] | R48[9] | R48[8] | R48[7] | R48[6] | R48[5] |
| 6 | 0 | 0 | 0 | R50[1 0] | R50[9] | R50[8] | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7 | R55[6] | R53[6] | 1 | R53[2] | R53[1] | R53[0] | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | R58[4] | R58[3] | R58[2] | R58[1] | R58[0] | 0 | R55[9] | R55[8] | R55[7] |
| 9 | 0 | 1 | R60[1 5] | R60[1 4] | R60[1 3] | R60[1 2] | R60[3] | R60[2] | R60[1] | R60[0] | R59[9] | R59[8] | R59[7] | R59[6] | R59[5] | R59[4] |
| 10 | R65[8] | R65[7] | R65[6] | R65[5] | R65[4] | 1 | 0 | 0 | 0 | 0 | R64[9] | R64[8] | R64[7] | R64[6] | R64[5] | 0 |
| 11 | 0 | 0 | 0 | R69[9] | R69[8] | R69[7] | R69[6] | R69[5] | 0 | 0 | 1 | R66[3] | R66[2] | R66[1] | R66[0] | R65[9] |
| 12 | R74[5] | 0 | 0 | 1 | R71[3] | R71[2] | R71[1] | R71[0] | R70[9] | R70[8] | R70[7] | R70[6] | R70[5] | R70[4] | 1 | 0 |
| 13 | R76[0] | R75[9] | R75[8] | R75[7] | R75[6] | R75[5] | R75[4] | 1 | 0 | 0 | 0 | 0 | R74[9] | R74[8] | R74[7] | R74[6] |
| 14 | 0 | 0 | 0 | 0 | 0 | R79[3] | R79[2] | R79[1] | R79[0] | R76[9] | R76[8] | R76[7] | R76[6] | R76[3] | R76[2] | R76[1] |
| 15 | 0 | 0 | 0 | 0 | 0 | 0 | R81[3] | 1 | 0 | 0 | 0 | 0 | 0 | 0 | R80[3] | 0 |
| 16 | R1[6] | R1[5] | R1[4] | R1[3] | R1[2] | R1[1] | R1[0] | R0[15] | R0[14] | R0[13] | R0[12] | 0 | R0[10] | 0 | R0[8] | R0[0] |
| 17 | R2[6] | R2[5] | R2[4] | R2[3] | R2[2] | R2[1] | R2[0] | R1[15] | R1[14] | R1[13] | R1[12] | R1[11] | R1[10] | R1[9] | R1[8] | R1[7] |
| 18 | 0 | R5[3] | R5[2] | R4[7] | R4[6] | R4[5] | R4[4] | R3[4] | R3[3] | R2[13] | R2[12] | R2[11] | R2[10] | R2[9] | R2[8] | R2[7] |
| 19 | R24[1 5] | R24[1 2] | R24[1 1] | R24[1 0] | R24[9] | R24[8] | 0 | 0 | R24[5] | R24[4] | R24[3] | R24[2] | R24[1] | R24[0] | 0 | 0 |
| 20 | R27[0] | 0 | R25[1 4] | R25[1 3] | R25[1 2] | R25[1 1] | R25[1 0] | R25[9] | R25[7] | R25[6] | R25[5] | R25[4] | R25[3] | R25[2] | R25[1] | R25[0] |
| 21 | R30[1 4] | R30[1 3] | R30[1 2] | R30[1 1] | R30[1 0] | R30[9] | R30[8] | R30[7] | R30[6] | R30[5] | R30[4] | R30[3] | R30[2] | R30[1] | R30[0] | R27[1] |
| 22 | R31[1 5] | R31[1 4] | R31[1 3] | R31[1 2] | R31[1 1] | R31[1 0] | R31[9] | R31[8] | R31[7] | R31[6] | R31[5] | R31[4] | R31[3] | R31[2] | R31[1] | R31[0] |
| 23 | R33[7] | R33[6] | R33[5] | R33[4] | R33[3] | R33[2] | R33[1] | R33[0] | R32[7] | R32[6] | R32[5] | R32[4] | R32[3] | R32[2] | R32[1] | R32[0] |
| 24 | R34[7] | R34[6] | R34[5] | R34[4] | R34[3] | R34[2] | R34[1] | R34[0] | R33[1 5] | R33[1 4] | R33[1 3] | R33[1 2] | R33[1 1] | R33[1 0] | R33[9] | R33[8] |
| 25 | R43[1 0] | R43[9] | R43[8] | R43[7] | R43[6] | R43[5] | R43[4] | R43[3] | R43[2] | R43[1] | R43[0] | R42[5] | R42[3] | R42[2] | R42[1] | R41[1 5] |
| 26 | R51[1 0] | 0 | 0 | 1 | R51[6] | 0 | 0 | R47[6] | R47[5] | R47[4] | R47[3] | R43[1 5] | R43[1 4] | R43[1 3] | R43[1 2] | R43[1 1] |
| 27 | R56[1 0] | R56[9] | R56[8] | R56[7] | R56[6] | R56[5] | R56[4] | R56[3] | R56[2] | R56[1] | R56[0] | R53[3] | 1 | 0 | 0 | 0 |
| 28 | R57[1 4] | R57[1 2] | R57[9] | R57[8] | R57[7] | R57[6] | R57[5] | R57[4] | R57[3] | R57[1] | R57[0] | R56[1 5] | R56[1 4] | R56[1 3] | R56[1 2] | R56[1 1] |
| 29 | R62[6] | R62[5] | R62[4] | R62[3] | R62[2] | R62[1] | R62[0] | R60[1 1] | R60[1 0] | R60[5] | R60[4] | R59[1 5] | R59[1 4] | R59[1 3] | R59[1 2] | R59[1 1] |
| 30 | R63[7] | R63[6] | R63[5] | R63[4] | R63[3] | R63[1] | R63[0] | R62[1 5] | R62[1 4] | R62[1 3] | R62[1 2] | R62[1 1] | R62[1 0] | R62[9] | R62[8] | R62[7] |
| 31 | R67[6] | R67[5] | R67[4] | R67[3] | R67[2] | R67[1] | R67[0] | R66[5] | R66[4] | R65[1 4] | R65[1 3] | R65[1 1] | R63[1 3] | R63[1 2] | R63[9] | R63[8] |
| 32 | R68[7] | R68[6] | R68[5] | R68[4] | R68[3] | R68[1] | R68[0] | R67[1 5] | R67[1 4] | R67[1 3] | R67[1 2] | R67[1 1] | R67[1 0] | R67[9] | R67[8] | R67[7] |
| 33 | R72[6] | R72[5] | R72[4] | R72[3] | R72[2] | R72[1] | R72[0] | R71[1 0] | R71[9] | R71[5] | R71[4] | R70[1 1] | R68[1 3] | R68[1 2] | R68[9] | R68[8] |

²⁰ Address Locations 0-15: EEPROM Base Page
²¹ Address Locations 16-39: EEPROM Page 0
²² Address Locations 40-63: EEPROM Page 1
²³ Bit locations marked in Red may vary from device to device

表 9-21. EEPROM Mapping ^{20 21 22 23} (continued)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| 34 | R73[7] | R73[6] | R73[5] | R73[4] | R73[3] | R73[1] | R73[0] | R72[1 5] | R72[1 4] | R72[1 3] | R72[1 2] | R72[1 1] | R72[1 0] | R72[9] | R72[8] | R72[7] |
| 35 | 0 | 0 | 0 | R77[1] | R77[0] | R76[5] | R76[4] | R75[1 5] | R75[1 4] | R75[1 3] | R75[1 2] | R75[1 1] | R73[1 3] | R73[1 2] | R73[9] | R73[8] |
| 36 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | R79[9] | R78[1 2] | 0 | 0 | 0 | 0 | 0 |
| 37 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 38 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 39 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 40 | R1[6] | R1[5] | R1[4] | R1[3] | R1[2] | R1[1] | R1[0] | R0[15] | R0[14] | R0[13] | R0[12] | 0 | R0[10] | 0 | R0[8] | R0[0] |
| 41 | R2[6] | R2[5] | R2[4] | R2[3] | R2[2] | R2[1] | R2[0] | R1[15] | R1[14] | R1[13] | R1[12] | R1[11] | R1[10] | R1[9] | R1[8] | R1[7] |
| 42 | 0 | R5[3] | R5[2] | R4[7] | R4[6] | R4[5] | R4[4] | R3[4] | R3[3] | R2[13] | R2[12] | R2[11] | R2[10] | R2[9] | R2[8] | R2[7] |
| 43 | R24[1 5] | R24[1 2] | R24[1 1] | R24[1 0] | R24[9] | R24[8] | 0 | 0 | R24[5] | R24[4] | R24[3] | R24[2] | R24[1] | R24[0] | 0 | 0 |
| 44 | R27[0] | 0 | R25[1 4] | R25[1 3] | R25[1 2] | R25[1 1] | R25[1 0] | R25[9] | R25[7] | R25[6] | R25[5] | R25[4] | R25[3] | R25[2] | R25[1] | R25[0] |
| 45 | R30[1 4] | R30[1 3] | R30[1 2] | R30[1 1] | R30[1 0] | R30[9] | R30[8] | R30[7] | R30[6] | R30[5] | R30[4] | R30[3] | R30[2] | R30[1] | R30[0] | R27[1] |
| 46 | R31[1 5] | R31[1 4] | R31[1 3] | R31[1 2] | R31[1 1] | R31[1 0] | R31[9] | R31[8] | R31[7] | R31[6] | R31[5] | R31[4] | R31[3] | R31[2] | R31[1] | R31[0] |
| 47 | R33[7] | R33[6] | R33[5] | R33[4] | R33[3] | R33[2] | R33[1] | R33[0] | R32[7] | R32[6] | R32[5] | R32[4] | R32[3] | R32[2] | R32[1] | R32[0] |
| 48 | R34[7] | R34[6] | R34[5] | R34[4] | R34[3] | R34[2] | R34[1] | R34[0] | R33[1 5] | R33[1 4] | R33[1 3] | R33[1 2] | R33[1 1] | R33[1 0] | R33[9] | R33[8] |
| 49 | R43[1 0] | R43[9] | R43[8] | R43[7] | R43[6] | R43[5] | R43[4] | R43[3] | R43[2] | R43[1] | R43[0] | R42[5] | R42[3] | R42[2] | R42[1] | R41[1 5] |
| 50 | R51[1 0] | 0 | 0 | 1 | R51[6] | 0 | 0 | R47[6] | R47[5] | R47[4] | R47[3] | R43[1 5] | R43[1 4] | R43[1 3] | R43[1 2] | R43[1 1] |
| 51 | R56[1 0] | R56[9] | R56[8] | R56[7] | R56[6] | R56[5] | R56[4] | R56[3] | R56[2] | R56[1] | R56[0] | R53[3] | 1 | 0 | 0 | 0 |
| 52 | R57[1 4] | R57[1 2] | R57[9] | R57[8] | R57[7] | R57[6] | R57[5] | R57[4] | R57[3] | R57[1] | R57[0] | R56[1 5] | R56[1 4] | R56[1 3] | R56[1 2] | R56[1 1] |
| 53 | R62[6] | R62[5] | R62[4] | R62[3] | R62[2] | R62[1] | R62[0] | R60[1 1] | R60[1 0] | R60[5] | R60[4] | R59[1 5] | R59[1 4] | R59[1 3] | R59[1 2] | R59[1 1] |
| 54 | R63[7] | R63[6] | R63[5] | R63[4] | R63[3] | R63[1] | R63[0] | R62[1 5] | R62[1 4] | R62[1 3] | R62[1 2] | R62[1 1] | R62[1 0] | R62[9] | R62[8] | R62[7] |
| 55 | R67[6] | R67[5] | R67[4] | R67[3] | R67[2] | R67[1] | R67[0] | R66[5] | R66[4] | R65[1 4] | R65[1 3] | R65[1 1] | R63[1 3] | R63[1 2] | R63[9] | R63[8] |
| 56 | R68[7] | R68[6] | R68[5] | R68[4] | R68[3] | R68[1] | R68[0] | R67[1 5] | R67[1 4] | R67[1 3] | R67[1 2] | R67[1 1] | R67[1 0] | R67[9] | R67[8] | R67[7] |
| 57 | R72[6] | R72[5] | R72[4] | R72[3] | R72[2] | R72[1] | R72[0] | R71[1 0] | R71[9] | R71[5] | R71[4] | R70[1 1] | R68[1 3] | R68[1 2] | R68[9] | R68[8] |
| 58 | R73[7] | R73[6] | R73[5] | R73[4] | R73[3] | R73[1] | R73[0] | R72[1 5] | R72[1 4] | R72[1 3] | R72[1 2] | R72[1 1] | R72[1 0] | R72[9] | R72[8] | R72[7] |
| 59 | 0 | 0 | 0 | R77[1] | R77[0] | R76[5] | R76[4] | R75[1 5] | R75[1 4] | R75[1 3] | R75[1 2] | R75[1 1] | R73[1 3] | R73[1 2] | R73[9] | R73[8] |
| 60 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | R79[9] | R78[1 2] | 0 | 0 | 0 | 0 | 0 |
| 61 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

²⁰ Address Locations 0-15: EEPROM Base Page
²¹ Address Locations 16-39: EEPROM Page 0
²² Address Locations 40-63: EEPROM Page 1
²³ Bit locations marked in Red may vary from device to device

表 9-21. EEPROM Mapping ^{20 21 22 23} (continued)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 62 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 63 | SCRC[15] | SCRC[14] | SCRC[13] | SCRC[12] | SCRC[11] | SCRC[10] | SCRC[9] | SCRC[8] | SCRC[7] | SCRC[6] | SCRC[5] | SCRC[4] | SCRC[3] | SCRC[2] | SCRC[1] | SCRC[0] |

表 9-22. Register Defaults in Fall-Back Mode and EEPROM Mode

| REGISTER ADDRESSES | FALL-BACK MODE | HW_SW_CTRL = 0 | HW_SW_CTRL = 1 | REGISTER ADDRESSES | FALL-BACK MODE | HW_SW_CTRL = 0 | HW_SW_CTRL = 1 |
|--------------------|----------------|----------------|----------------|--------------------|----------------|----------------|----------------|
| R85 | x0000 | x0000 | x0000 | R42 | x0002 | x0002 | x0002 |
| R84 | x0000 | x0000 | x0000 | R41 | x0000 | x0000 | x0000 |
| R83 | x0000 | xFF00 | xFF00 | R40 | x0000 | x0000 | x0000 |
| R82 | x0000 | x01C0 | x01C0 | R39 | x0000 | x0000 | x0000 |
| R81 | x0004 | x0004 | x0004 | R38 | x0000 | x0000 | x0000 |
| R80 | x0000 | x0008 | x0008 | R37 | x0000 | x0000 | x0000 |
| R79 | x0008 | x0008 | x0008 | R36 | x0000 | x0000 | x0000 |
| R78 | x1000 | x0000 | x0000 | R35 | x0000 | x0028 | x0028 |
| R77 | x0000 | x0002 | x0002 | R34 | x0000 | x0000 | x0000 |
| R76 | x0008 | x0188 | x0188 | R33 | x0000 | x0000 | x0000 |
| R75 | x0008 | x0008 | x8008 | R32 | x0000 | x0000 | x0000 |
| R74 | xA181 | xA181 | xA181 | R31 | x0000 | x0000 | x0000 |
| R73 | x2000 | x2000 | x0000 | R30 | x0030 | x0030 | x0030 |
| R72 | x0006 | x0006 | x0006 | R29 | x0000 | x0000 | x0000 |
| R71 | x0000 | x0406 | x0406 | R28 | x0000 | x0000 | x0000 |
| R70 | x0008 | x0008 | x0808 | R27 | x0005 | x0004 | x0004 |
| R69 | xA181 | xA181 | xA181 | R26 | x0000 | x0000 | x0000 |
| R68 | x2000 | x2000 | x0000 | R25 | x0400 | x0400 | x0400 |
| R67 | x0006 | x0006 | x0006 | R24 | x0718 | x091C | x091C |
| R66 | x0000 | x0006 | x0006 | R23 | x0000 | x2406 | x2406 |
| R65 | x0008 | x4008 | x4808 | R22 | x06A2 | x06A2 | x06A2 |
| R64 | xA181 | xA181 | xA181 | R21 | x0000 | x0590 | x0513 |
| R63 | x2000 | x2000 | x0000 | R20 | x0000 | x0000 | x0000 |
| R62 | x0006 | x0006 | x0006 | R19 | x0000 | x0000 | x0000 |
| R61 | x0000 | x0000 | x0000 | R18 | x0000 | x0000 | x0000 |
| R60 | x0008 | x0008 | x6028 | R17 | x26C4 | x26C4 | x26C4 |
| R59 | x0008 | x0008 | x8008 | R16 | x921F | x921F | x921F |
| R58 | x502C | x502C | x502C | R15 | xA037 | xA037 | xA037 |
| R57 | x4000 | x4000 | x0000 | R14 | x0000 | x0000 | x0000 |
| R56 | x0006 | x0006 | x0006 | R13 | x0000 | x0000 | x0000 |
| R55 | x001E | x001E | x001E | R12 | x0000 | x0000 | x7002 |
| R54 | x3400 | x3400 | x3400 | R11 | x0000 | x0000 | x003F |
| R53 | x0069 | x0069 | x0069 | R10 | x0000 | xA777 | xA777 |
| R52 | x5000 | x5000 | x5000 | R9 | x0000 | x7BFA | xA777 |
| R51 | x40C0 | x40C0 | x40C0 | R8 | x0000 | x0001 | x0001 |
| R50 | x01C0 | x01C0 | x01C0 | R7 | x0000 | x0C2D | x0C0D |
| R49 | x0013 | x0013 | x0013 | R6 | x0000 | x0E6C | x0E6C |
| R48 | x1A14 | x1A05 | x1A05 | R5 | x0008 | x0008 | x0008 |
| R47 | x0A00 | x0280 | x0280 | R4 | x0000 | x0000 | x0000 |

²⁰ Address Locations 0-15: EEPROM Base Page
²¹ Address Locations 16-39: EEPROM Page 0
²² Address Locations 40-63: EEPROM Page 1
²³ Bit locations marked in Red may vary from device to device

表 9-22. Register Defaults in Fall-Back Mode and EEPROM Mode (continued)

| REGISTER ADDRESSES | FALL-BACK MODE | HW_SW_CTRL = 0 | HW_SW_CTRL = 1 | REGISTER ADDRESSES | FALL-BACK MODE | HW_SW_CTRL = 0 | HW_SW_CTRL = 1 |
|--------------------|----------------|----------------|----------------|--------------------|----------------|----------------|----------------|
| R46 | x0000 | x0000 | x0000 | R3 | x0000 | x0200 | x0200 |
| R45 | x4F80 | x4F80 | x4F80 | R2 | x0000 | x0000 | x0000 |
| R44 | x0318 | x0318 | x0318 | R1 | x2310 | x7654 | x7652 |
| R43 | x0051 | x0051 | x0051 | R0 | x0000 | x0001 | x2000 |

10 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

A typical application using the I²C interface and a 25-MHz crystal input is shown in 图 10-1. The two ends of 25-MHz XTAL are connected to pin 1 and 2. The REFSEL pin is pulled down to select a secondary input. The HW_SW_CTRL can be pulled either low or high if EEPROM is used, or kept floating if EEPROM is unused. 1.8 V, 2.5 V, or 3.3 V can be supplied to the VDD_REF and VDD_VCO pins, as well as VDDO_12 and VDDO_34 pins with filtering. Data and clock lines of I2C must be pulled to VDD_REF using pullup resistors. The PDN can be connected to the MCU if a hardware reset is required, otherwise it can be left floating. The GPIO1 and 4 pins can be connected to the MCU if needed, otherwise they can be left floating. Unused outputs can be left floating.

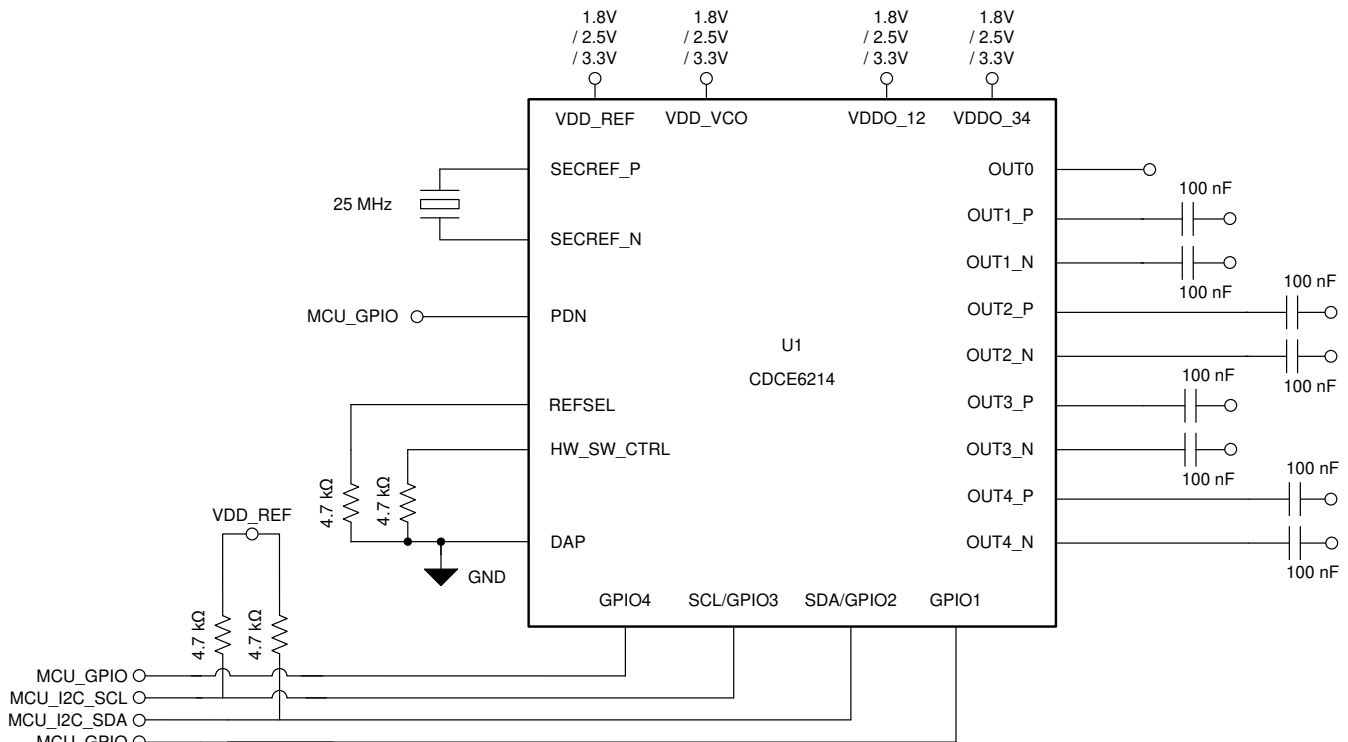


图 10-1. Typical Application Schematic With I²C Interface

10.2 Typical Application

图 10-2 图 10-2 shows typical block diagram for eAVB system using CDCE6214-Q1.

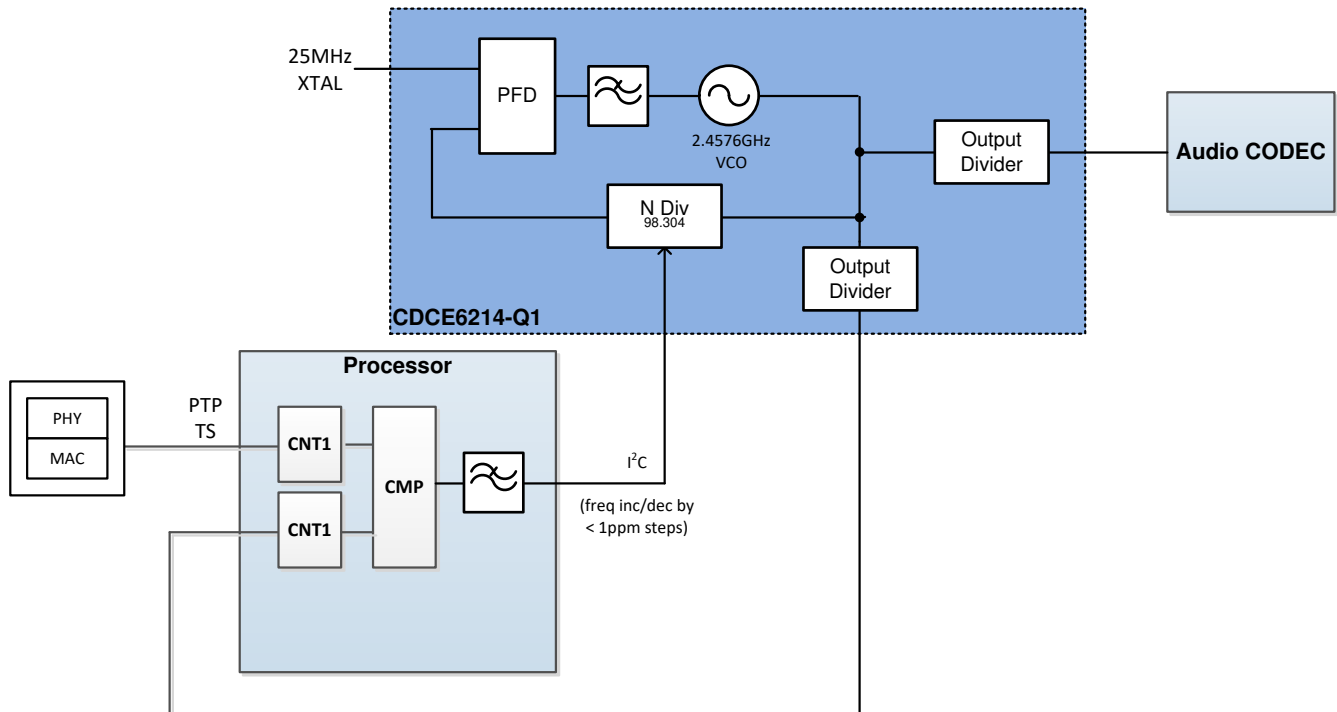


图 10-2. eAVB System Block Diagram Using CDCE6214-Q1

10.2.1 Design Requirements

For designs with the CDCE6214-Q1, the designer must select:

- a primary or secondary input
- an input type
- an input frequency
- a device communication mode (I^2C and/or EEPROM)
- the required device operation modes to configure the connections of GPIO pins
- a supply voltage (1.8 V, 2.5 V, or 3.3 V)
- a digital reference (1.8 V, 2.5 V, or 3.3 V)
- an output reference (1.8 V, 2.5 V, or 3.3 V)
- an output format

10.2.2 Detailed Design Procedure

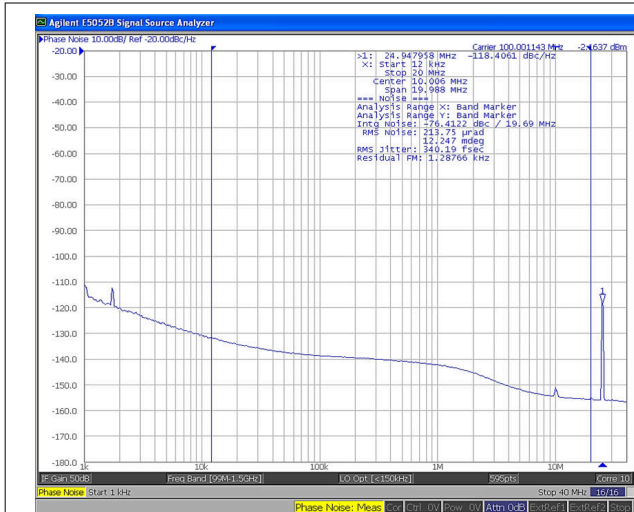
The CDCE6214-Q1 is designed for ease-of-use. To power up the device:

1. Either tie the power supply pin (VDD_REF, VDD_VCO, VDDO_12 and VDDO_34) together or independently connect them to the 1.8-V, 2.5-V, or 3.3-V power supply.
2. Solder the GND Pin (DAP) to the PCB Plane.
3. Ensure that the REFSEL, HW_SW_CTRL, and PDN configuration pins are appropriately connected:
 - a. Internally connect the PDN pin to VDD_REF through a pullup resistor. When floating, the PDN pin would automatically release device from PDN.
 - b. If PDN pin is low, the device will not respond to I2C commands.
 - c. REFSEL and HW_SW_CTRL are tri-level pins. If left floating, the device will start in fall-back mode.

The device is factory-configured to provide:

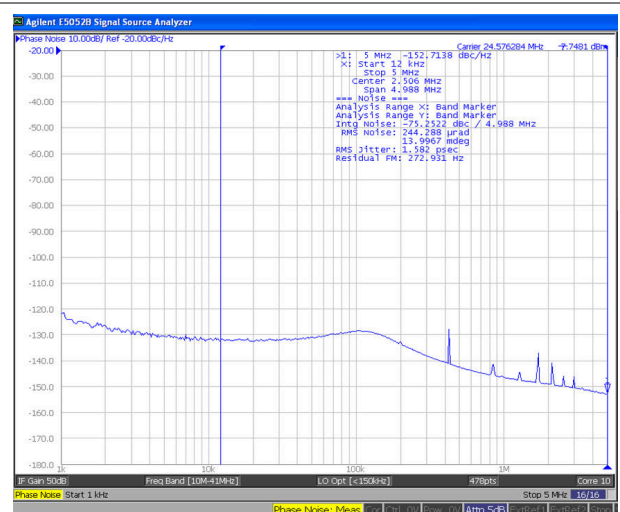
- 100-MHz LVDS with 25-MHz XTAL when HW_SW_CTRL=L. The 25-MHz output on OUT0 is enabled.
- 100-MHz LP-HCSL with 25-MHz XTAL and HW_SW_CTRL = H. The 25-MHz output on OUT0 is enabled.

10.2.3 Application Curves



Reference: Crystal Closed-Loop Phase 100-MHz LP-HCSL
Input 25 MHz Noise from 2.4-GHz VCO

图 10-3. 100-MHz LP-HCSL Output for PCIe Application



Reference: Crystal Closed-Loop Phase 24.576-MHz
Input 25 MHz Noise from 2.4576-GHz VCO LVCMOS

图 10-4. 24.576MHz LVCMOS Output for Audio Clocking

11 Power Supply Recommendations

The CDCE6214-Q1 provides multiple power supply pins. Each power supply supports 1.8 V, 2.5 V, or 3.3 V. Internal low-dropout regulators (LDO) source the internal blocks and allow each pin to be supplied with its individual supply voltage. The VDD_REF pin supplies the control pins and the serial interface. Therefore, any pullup resistors shall be connected to the same domain as VDD_REF. VDD_VCO powers all PLL blocks. VDDO_12 powers outputs OUT1 and OUT2. VDDO_34 powers OUT0, OUT3, and OUT4.

VDD_REF and VDDO_34 can be used for level translation operation on OUT0.

11.1 Power-Up Sequence

There are no restrictions from the device for applying power to the supply pins. From an application perspective, TI recommends to either apply all the VDDs at the same time or apply the VDDREF first. The digital core is connected to VDDREF and thus the settings of the EEPROM are applied automatically.

11.2 Decoupling

TI recommends isolating all power supplies using a ferrite bead and provide decoupling for each of the supplies. TI also recommends optimizing the decoupling for the respective layout, and consider the power supply impedance to optimize for the individual frequency plan.

An example for a decoupling per supply pin: 1x 4.7 μ F, 1x 470 nF, and 1x 100 nF.

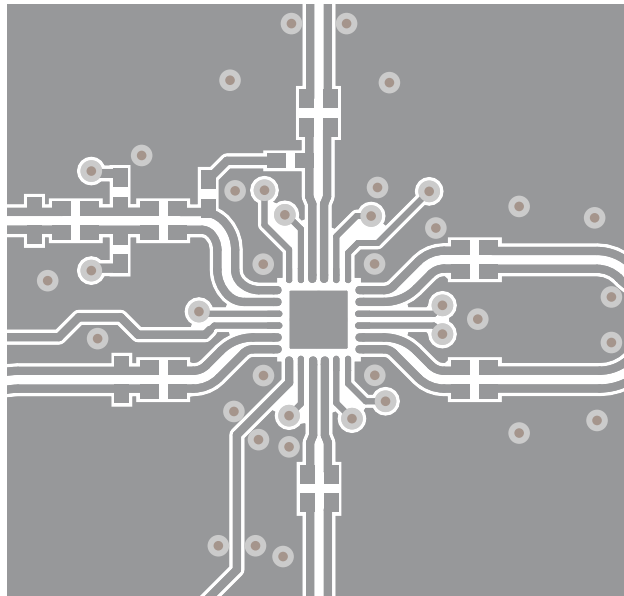
12 Layout

12.1 Layout Guidelines

For this example, follow these guidelines:

- Isolate inputs and outputs using a GND shield. **BROKEN_LINK** routes all inputs and outputs as differential pairs.
- Isolate outputs to adjacent outputs when generating multiple frequencies.
- Isolate the crystal area, connect the GND pads of the crystal package and flood the adjacent area. [图 12-2](#) shows a foot print which supports multiple crystal sizes.
- Try to avoid impedance jumps in the fan-in and fan-out areas when possible.
- Use five VIAs to connect the thermal pad to a solid GND plane. Full-through VIAs are preferred.
- Place decoupling capacitors with small capacitance values very close to the supply pins. Try to place them very close on the same layer or directly on the backside layer. Larger values can be placed more far away. [图 12-2](#) shows three decoupling capacitors close to the device. Ferrite beads are recommended to isolate the different frequency domains and the VDD_VCO domain.
- Preferably use multiple VIAs to connect wide supply traces to the respective power planes.

12.2 Layout Examples



[图 12-1](#). Layout Example, Top Layer

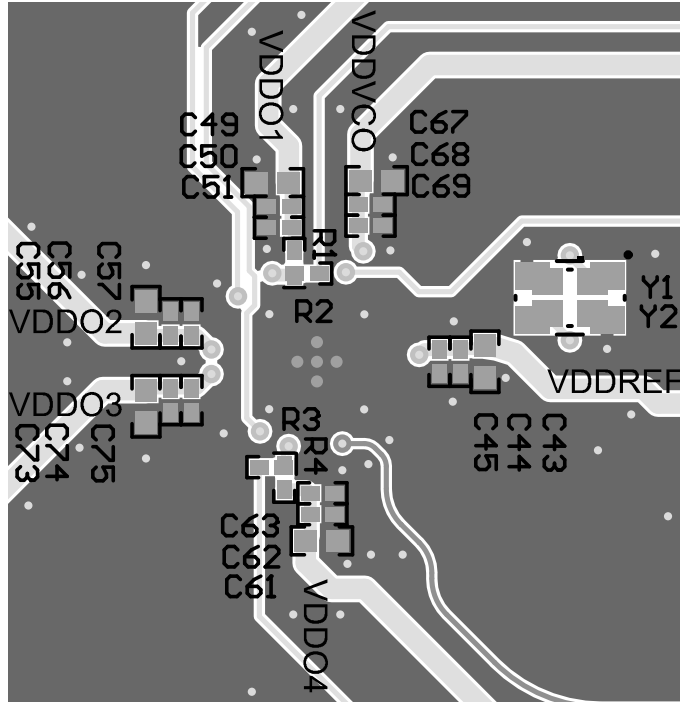


图 12-2. Layout Example, Bottom Layer

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

Contact your TI representative for more information.

13.1.2 Device Nomenclature

CDCE6214-Q1 - 62= clock generator 1= 1x PLL 4=4x outputs E = EEPROM, integer and fractional output dividers

13.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

13.4 Trademarks

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13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

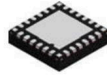
13.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

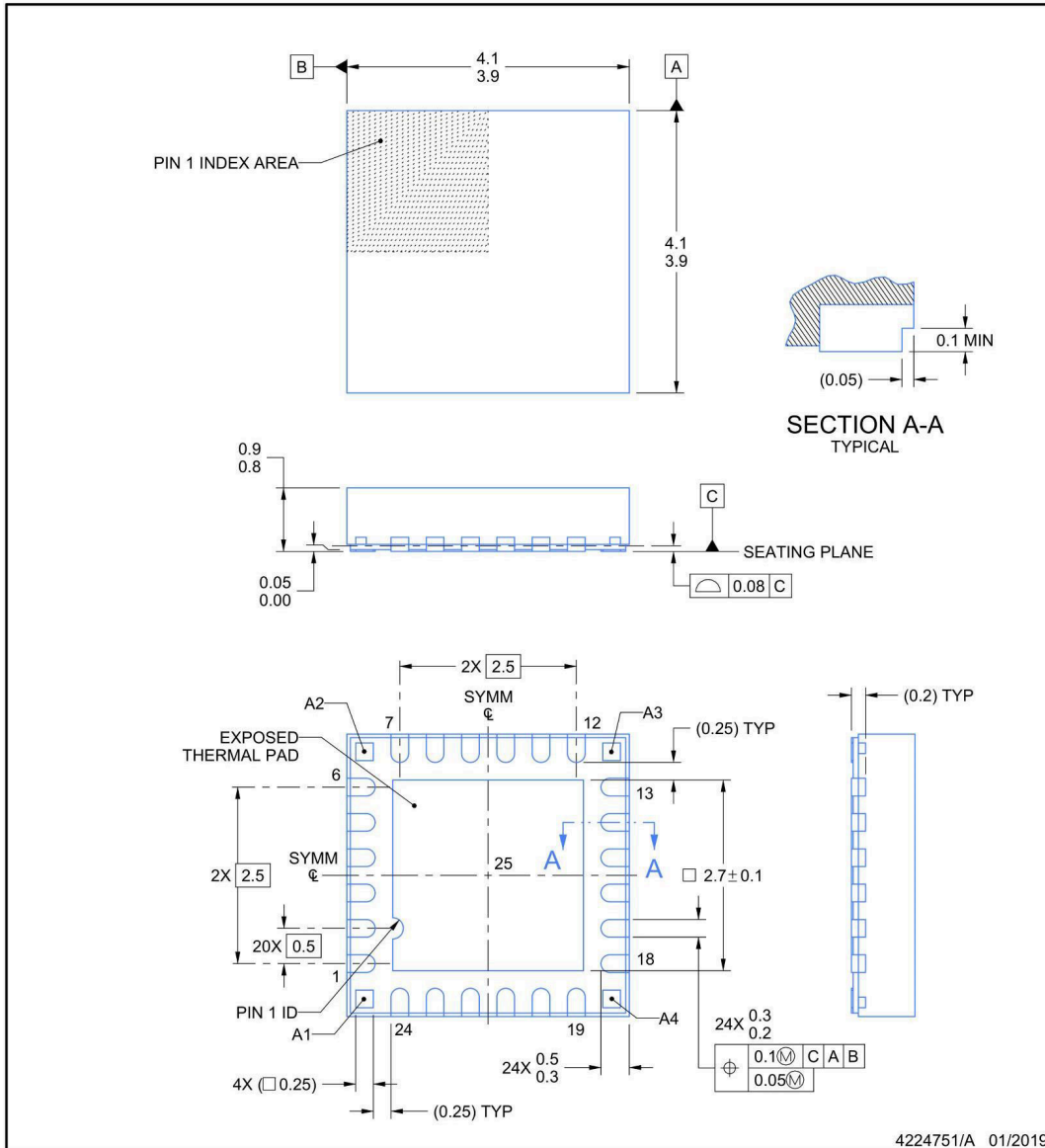
RGE0024P



PACKAGE OUTLINE

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

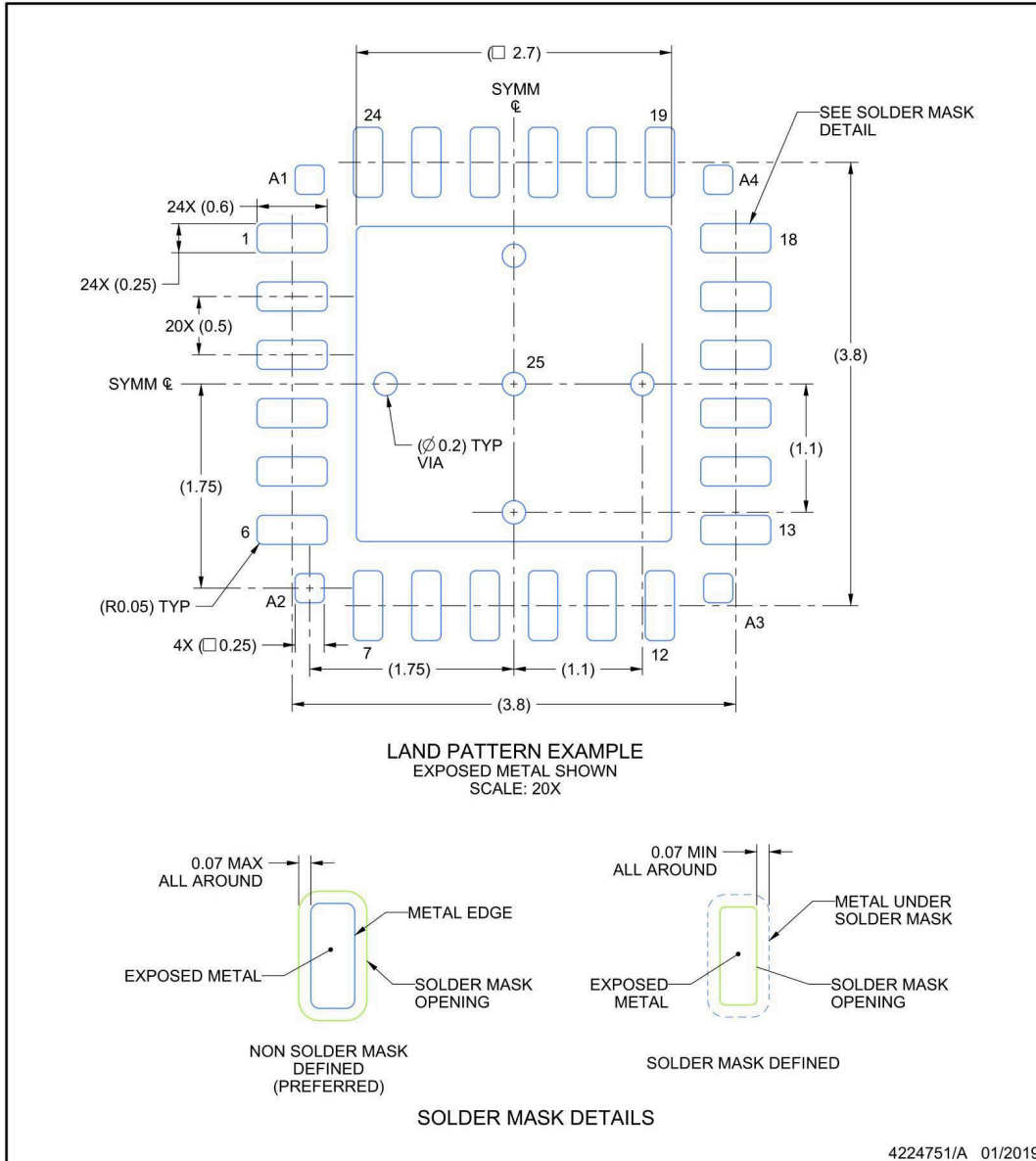
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGE0024P

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

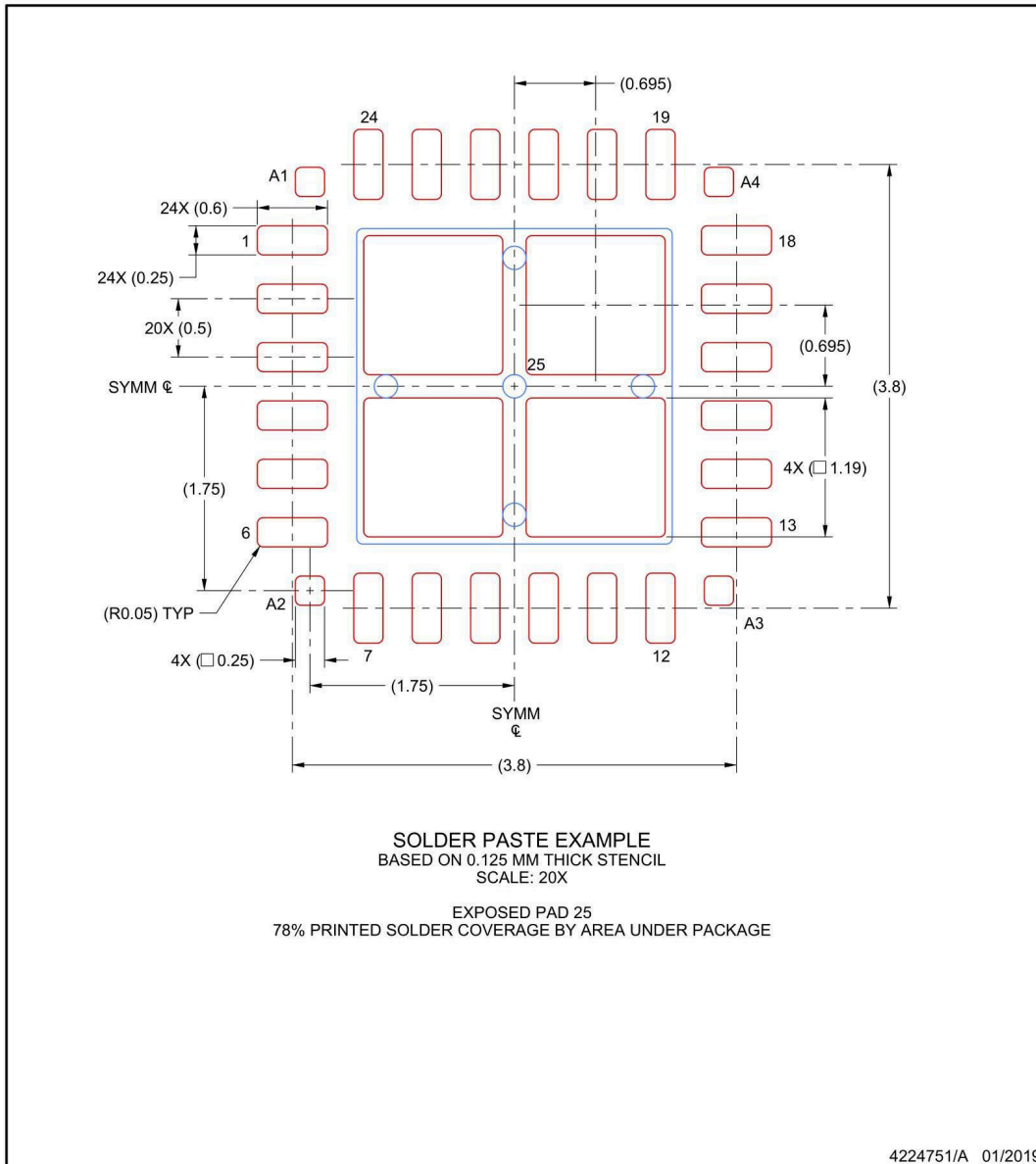
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024P

VQFN - 0.9 mm max height



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| CDCE6214TWRGERQ1 | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 105 | 6214Q1 A2Z |  |
| CDCE6214TWRGETQ1 | ACTIVE | VQFN | RGE | 24 | 250 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 105 | 6214Q1 A2Z |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CDCE6214-Q1 :

- Catalog : [CDCE6214](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCE6214TWRGERQ1 | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CDCE6214TWRGETQ1 | VQFN | RGE | 24 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCE6214TWRGERQ1 | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| CDCE6214TWRGETQ1 | VQFN | RGE | 24 | 250 | 210.0 | 185.0 | 35.0 |

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