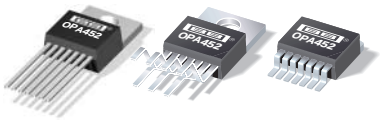
OPA452
OPA453



SBOS127C – JULY 2000 – REVISED NOVEMBER 2003

80V, 50mA OPERATIONAL AMPLIFIERS

FEATURES

- **WIDE POWER-SUPPLY RANGE: ±10V to ±40V**
- **HIGH OUTPUT LOAD DRIVE: 50mA Continuous**
- **WIDE OUTPUT VOLTAGE SWING: 1V to Rail**
- **FULLY PROTECTED: Thermal Shutdown Output Current-Limited**
- **WIDE OPERATING TEMPERATURE RANGE: –40°C TO +125°C**
- **PACKAGE OPTIONS: TO220-7 DDPACK-7 Surface-Mount**

APPLICATIONS

- **PIEZOELECTRIC CELLS**
- **TEST EQUIPMENT**
- **AUDIO AMPLIFIERS**
- **TRANSDUCER DRIVERS**
- **SERVO DRIVERS**

DESCRIPTION

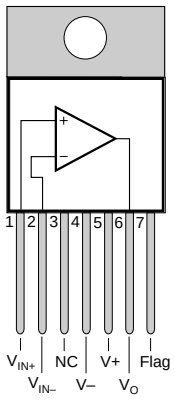
The OPA452 and OPA453 are low-cost operational amplifiers with high-voltage (80V) and high-current capabilities (50mA). The OPA452 is unity-gain stable and has a gain bandwidth product of 1.8MHz, whereas the OPA453 is optimized for gains greater than 5 and has a 7.5MHz bandwidth.

The OPA452 and OPA453 are internally protected against over-temperature conditions and current overloads. Power supplies in the range of ±10V to ±40V can be used. Unlike most other power op amps, the OPA452 and OPA453 have ensured specifications over the entire power-supply range.

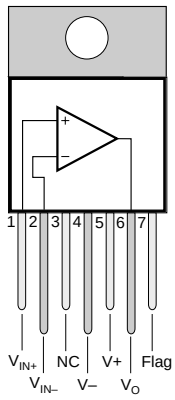
These laser-trimmed, monolithic integrated circuits provide excellent low-level accuracy along with wide output swing. Special design considerations assure that the product is easy to use and free from phase inversion problems often found in other amplifiers.

The OPA452 and OPA453 are available in TO220-7 and DDPAK-7 options. They are specified for a junction temperature range of –40°C to +125°C.

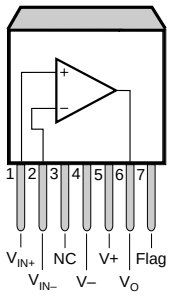
7-Lead Straight-Formed TO-220 (TA)



7-Lead Stagger-Formed TO-220 (TA-1)



7-Lead DDPAK (FA) Surface-Mount



NOTE: Tabs are electrically connected to V– supply.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	80V
Signal Input Terminals, Voltage[2]	(V–) – 0.5V to (V+) + 0.5V
Current[2]	5mA
Output Short-Circuit	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering 10s, TO-220)	300°C
(soldering 3s, DDPAK)	240°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 5mA or less.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS: OPA452; V_S = ±10V to ±40V

Boldface limits apply over the specified junction temperature range, **T_J = –40°C to +125°C.**

At T_J = +25°C, R_L = 3.8kΩ connected to ground, and V_{OUT} = 0V, unless otherwise noted.

PARAMETER		CONDITION	OPA452TA, FA MIN	OPA452TA, FA TYP	OPA452TA, FA MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±40V, V_{CM} = 0V, I_O = 0V		±1	±3	mV
over Temperature					**±6**	**mV**
Drift	**dV_{OS}/dT**			**±5**		**µV/°C**
vs Power Supply	PSRR	V_S = ±10V to ±40V, V_{CM} = 0V		5	30	µV/V
over Temperature					**45**	**µV/V**
INPUT BIAS CURRENT(1)						
Input Bias Current	I_B	V_S = ±40V, V_{CM} = 0V		±7	±100	pA
Input Offset Current	I_{OS}	V_S = ±40V, V_{CM} = 0V		±1	±100	pA
NOISE						
Input Voltage Noise Density	e_n	f = 1kHz		21		nV/√Hz
Current Noise Density	i_n	f = 1kHz		9		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) + 5		(V+) – 0.5	V
Common-Mode Rejection Ratio	CMRR	V_S = ±40V, –35V < V_{CM} < 39.5V	86	94		dB
over Temperature		**V_S = ±40V, –35V < V_{CM} < 39.5V**	**76**			**dB**
INPUT IMPEDANCE						
Differential				10^{13} || 2		Ω || pF
Common-Mode		V_S = ±40V, –35V < V_{CM} < 39.5V		10^{13} || 6		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	I_O = 10mA, $–V_S$ + 2V < V_O < $+V_S$ – 2V	105	110		dB
over Temperature		**I_O = 10mA, $–V_S$ + 2V < V_O < $+V_S$ – 2V**		**107**		**dB**
		I_O = 50mA, $–V_S$ + 4V < V_O < $+V_S$ – 4V	96	110		dB
over Temperature		**I_O = 50mA, $–V_S$ + 5V < V_O < $+V_S$ – 5.5V**		**105**		**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	V_S = ±40V		1.8		MHz
Slew Rate	SR	V_S = ±40V		+7.2/–10		V/µs
Settling Time: 0.1%		V_S = ±40V, G = +1, 10V Step, C_L = 100pF		2		µs
0.01%		V_S = ±40V, G = +1, 10V Step, C_L = 100pF		5		µs
Overload Recovery Time		V_{IN} • Gain = V_S		1		µs
Total Harmonic Distortion + Noise	THD+N	V_S = ±40V, V_O = 30Vp-p, G = 5 f = 1kHz, R_L = 2kΩ		0.0008		%
OUTPUT						
Voltage Output	V_{OUT}	I_O = 50mA	(V–) + 4.0		(V+) – 4	V
over Temperature		**I_O = 50mA**	**(V–) + 5**		**(V+) – 5.5**	**V**
Voltage Output		I_O = 10mA	(V–) + 2		(V+) – 2	V
over Temperature		**I_O = 10mA**	**(V–) + 2**		**(V+) – 2**	**V**
Output Current			±50			mA
Short-Circuit Current	I_{SC}			±125		mA
Capacitive Load Drive	C_{LOAD}			See Typical Characteristic		
SHUTDOWN FLAG						
Thermal Shutdown Status Output						
Normal Operation		V_S = ±40V		0.1	1.0	µA
Thermally Shutdown		V_S = ±40V	100	140	165	µA
Junction Temperature						
Shutdown				+160		°C
Reset from Shutdown				+145		°C
POWER SUPPLY						
Supply Voltage Range	V_S		±10		±40	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		±5.5	±6.5	mA
over Temperature					**±7.5**	**mA**
TEMPERATURE RANGE						
Specified Range (junction)	T_J		–40		+125	°C
Operating Range (junction)	T_J		–55		+125	°C
Storage Range (ambient)	T_A		–65		+150	°C
Thermal Resistance	θ_{JC}					
TO200-7				3		°C/W
DDPAK-7				3		°C/W

NOTE: (1) All tests are high-speed tested at +25°C ambient temperature. Effective junction temperature is +25°C, unless otherwise noted.

ELECTRICAL CHARACTERISTICS: OPA453; V_S = ±10V to ±40V

Boldface limits apply over the specified junction temperature range, **T_J = –40°C to +125°C.**

At T_J = +25°C, R_L = 3.8kΩ connected to ground, and V_{OUT} = 0V, unless otherwise noted.

PARAMETER		CONDITION	OPA453TA, FA MIN	OPA453TA, FA TYP	OPA453TA, FA MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±40V, V_{CM} = 0V, I_O = 0V		±1	±3	mV
over Temperature					**±6**	**mV**
Drift	**dV_{OS}/dT**			**±5**		**µV/°C**
vs Power Supply	PSRR	V_S = ±10V to ±40V, V_{CM} = 0V		5	30	µV/V
over Temperature					**45**	**µV/V**
INPUT BIAS CURRENT(1)						
Input Bias Current	I_B	V_S = ±40V, V_{CM} = 0V		±7	±100	pA
Input Offset Current	I_{OS}	V_S = ±40V, V_{CM} = 0V		±1	±100	pA
NOISE						
Input Voltage Noise Density	e_n	f = 1kHz		21		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 1kHz		9		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) + 5		(V+) – 0.5	V
Common-Mode Rejection Ratio	CMRR	V_S = ±40V, –35V < V_{CM} < 39.5V	86	94		dB
over Temperature		**V_S = ±40V, –35V < V_{CM} < 39.5V**	**76**			**dB**
INPUT IMPEDANCE						
Differential				10^{13} || 2		Ω || pF
Common-Mode		V_S = ±40V, –35V < V_{CM} < 39.5V		10^{13} || 6		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	I_O = 10mA, $–V_S$ + 2V < V_O < $+V_S$ – 2V	105	110		dB
over Temperature		**I_O = 10mA, $–V_S$ + 2V < V_O < $+V_S$ – 2V**		**107**		**dB**
		I_O = 50mA, $–V_S$ + 4V < V_O < $+V_S$ – 4V	96	110		dB
over Temperature		**I_O = 50mA, $–V_S$ + 5V < V_O < $+V_S$ – 5.5V**		**105**		**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	V_S = ±40V		7.5		MHz
Slew Rate	SR	V_S = ±40V		+23/–38		V/µs
Settling Time: 0.1%		V_S = ±40V, G = +5, 10V Step, C_L = 100pF		1		µs
0.01%		V_S = ±40V, G = +5, 10V Step, C_L = 100pF		1.5		µs
Overload Recovery Time		V_{IN} • Gain = V_S		1		µs
Total Harmonic Distortion + Noise	THD+N	V_S = ±40V, V_O = 30Vp-p, G = 5 f = 1kHz, R_L = 2kΩ		0.0008		%
OUTPUT						
Voltage Output	V_{OUT}	I_O = 50mA	(V–) + 4.0		(V+) – 4	V
over Temperature		**I_O = 50mA**	**(V–) + 5**		**(V+) – 5.5**	**V**
Voltage Output		I_O = 10mA	(V–) + 2		(V+) – 2	V
over Temperature		**I_O = 10mA**	**(V–) + 2**		**(V+) – 2**	**V**
Output Current			±50			mA
Short-Circuit Current	I_{SC}			±125		mA
Capacitive Load Drive	C_{LOAD}			See Typical Characteristic		
SHUTDOWN FLAG						
Thermal Shutdown Status Output						
Normal Operation		V_S = ±40V		0.1	1.0	µA
Thermally Shutdown		V_S = ±40V	100	140	165	µA
Junction Temperature						
Shutdown				+160		°C
Reset from Shutdown				+145		°C
POWER SUPPLY						
Supply Voltage Range	V_S		±10		±40	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		±5.5	±6.5	mA
over Temperature					**±7.5**	**mA**
TEMPERATURE RANGE	T_J					
Specified Range (junction)	T_J		–40		+125	°C
Operating Range (junction)	T_A		–55		+125	°C
Storage Range (ambient)			–65		+150	°C
Thermal Resistance	θ_{JC}					
TO200-7				3		°C/W
DDPAK-7				3		°C/W

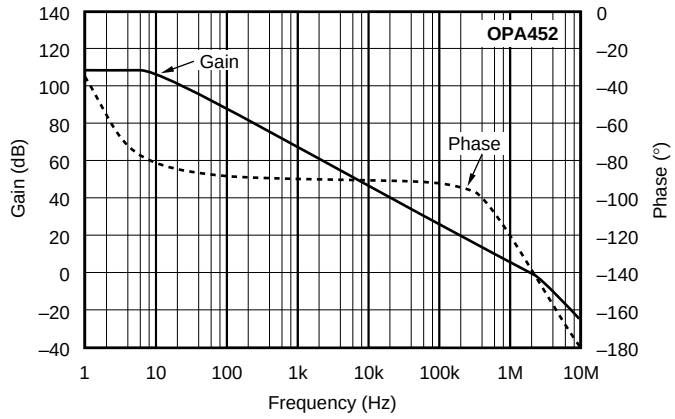
NOTE: (1) All tests are high-speed tested at +25°C ambient temperature. Effective junction temperature is +25°C, unless otherwise noted.

TYPICAL CHARACTERISTICS

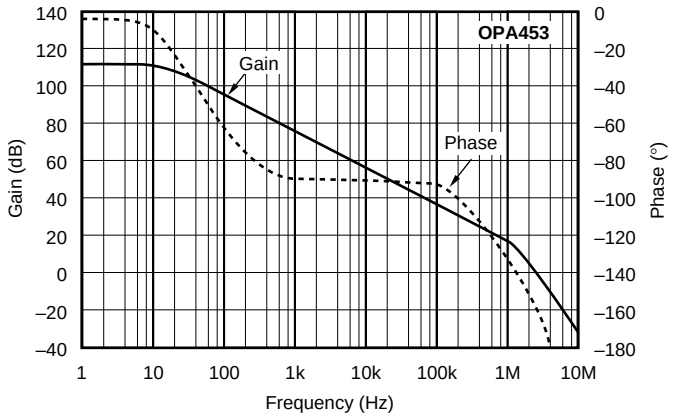
At T_J = +25°C, V_S = ±40V, and R_L = 3.8kΩ, unless otherwise noted.

All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.

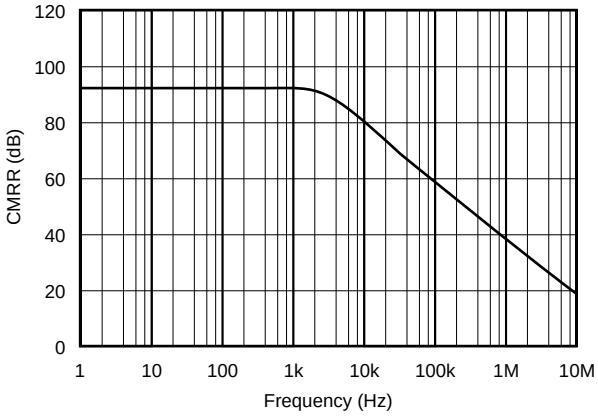
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



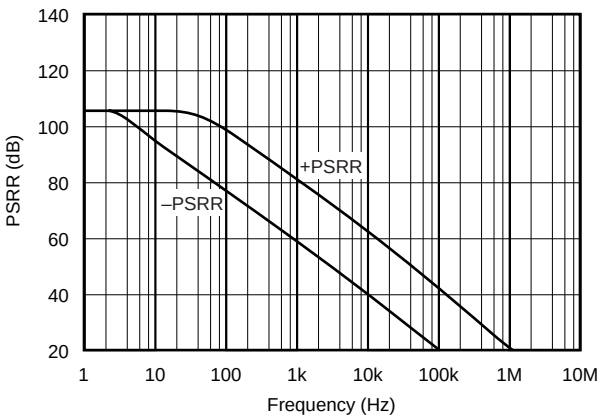
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



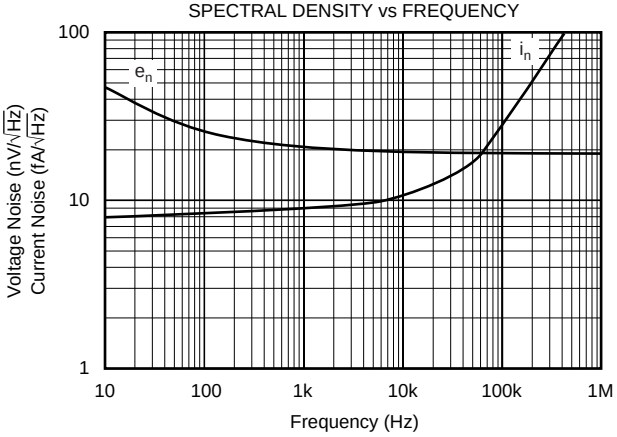
COMMON-MODE REJECTION RATIO vs FREQUENCY



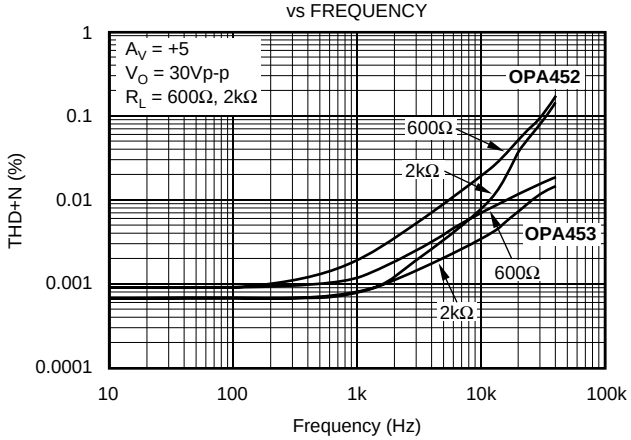
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

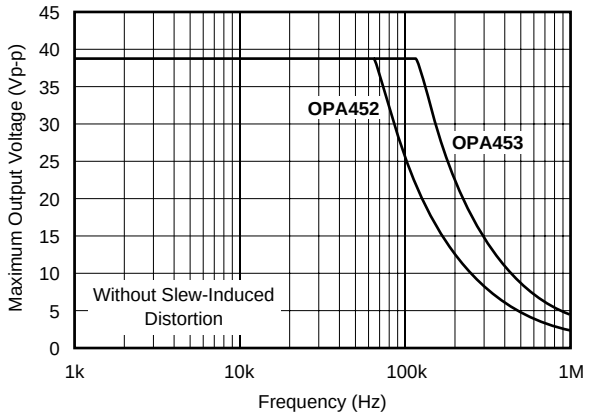


TYPICAL CHARACTERISTICS (Cont.)

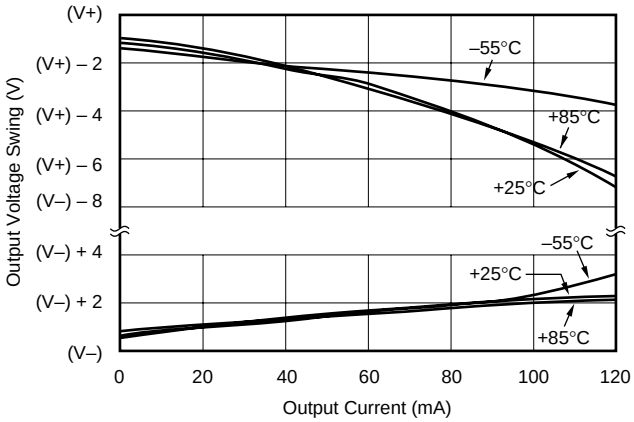
At T_J = +25°C, V_S = ±40V, and R_L = 3.8kΩ, unless otherwise noted.

All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.

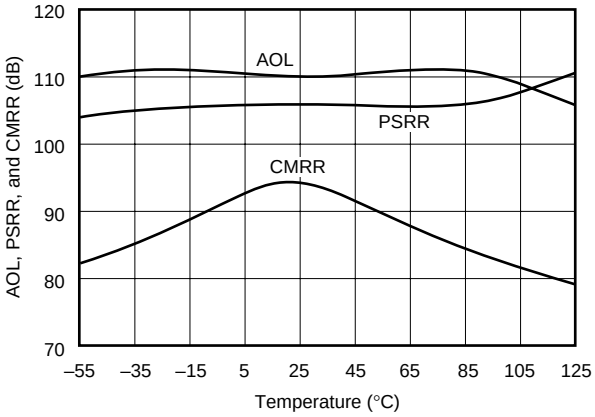
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



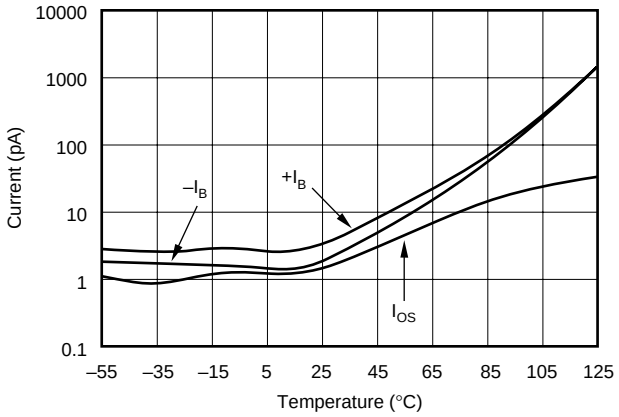
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



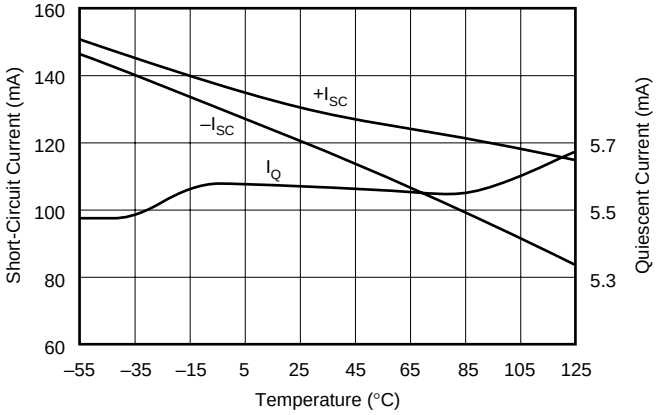
OPEN-LOOP GAIN, POWER-SUPPLY REJECTION RATIO, AND COMMON-MODE REJECTION RATIO vs TEMPERATURE



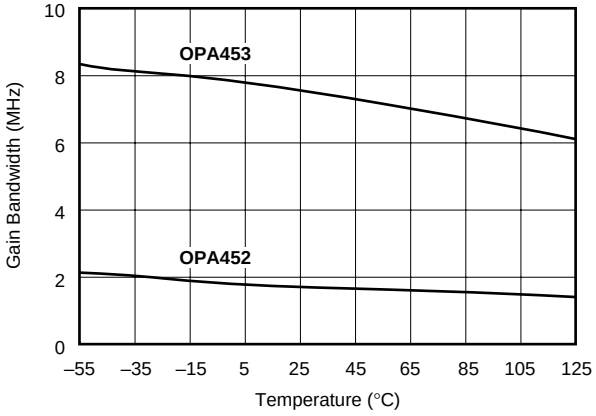
INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE



QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



GAIN BANDWIDTH PRODUCT vs TEMPERATURE

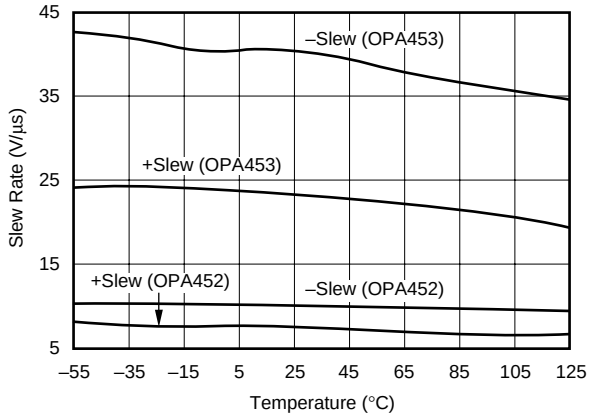


TYPICAL CHARACTERISTICS (Cont.)

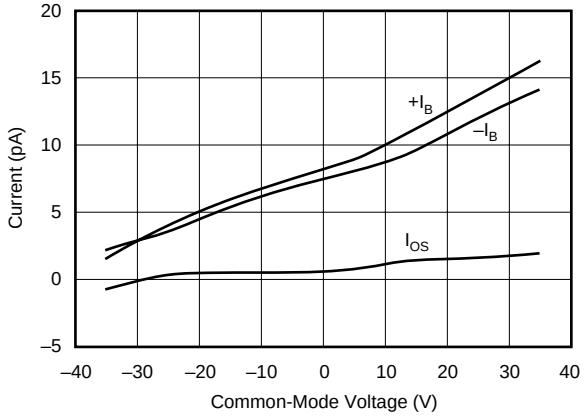
At T_J = +25°C, V_S = ±40V, and R_L = 3.8kΩ, unless otherwise noted.

All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.

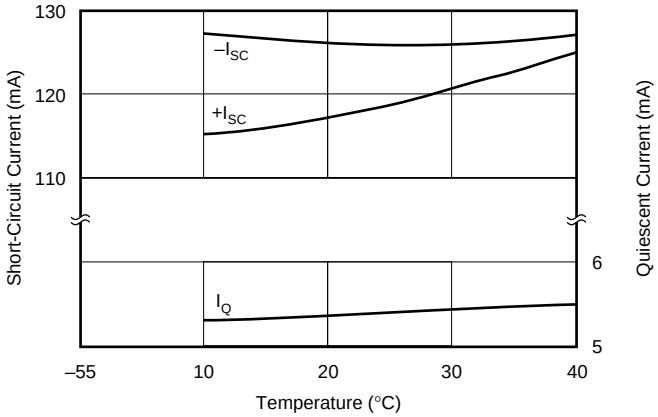
SLEW RATE vs TEMPERATURE



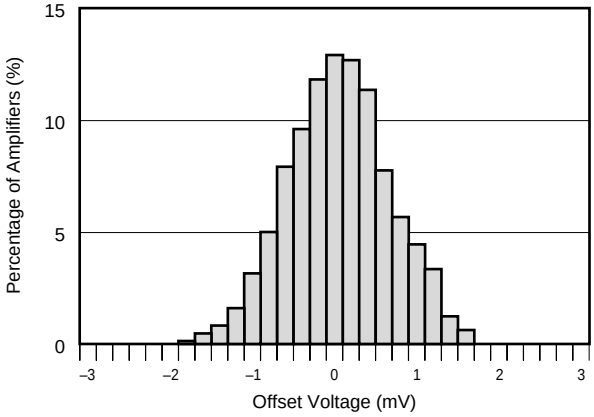
INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs COMMON-MODE VOLTAGE



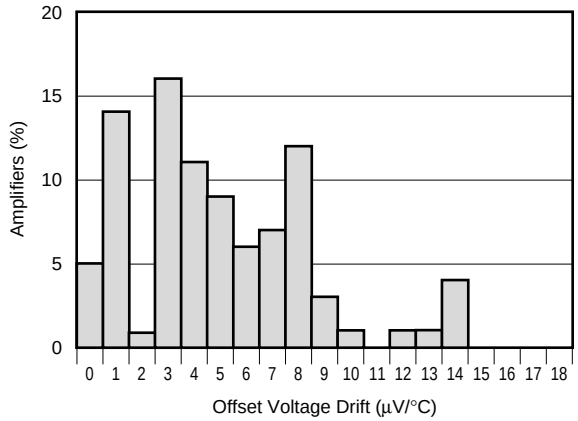
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



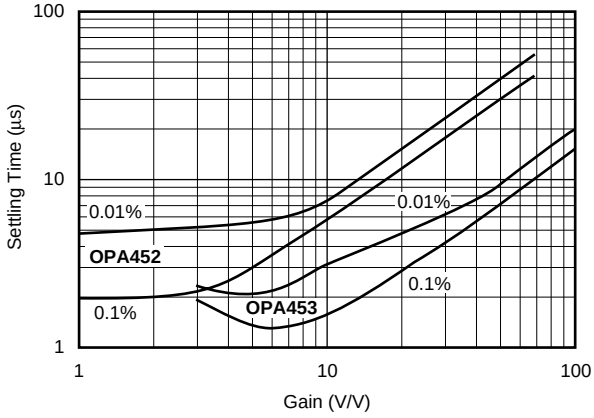
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT DISTRIBUTION



SETTLING TIME vs CLOSED-LOOP GAIN

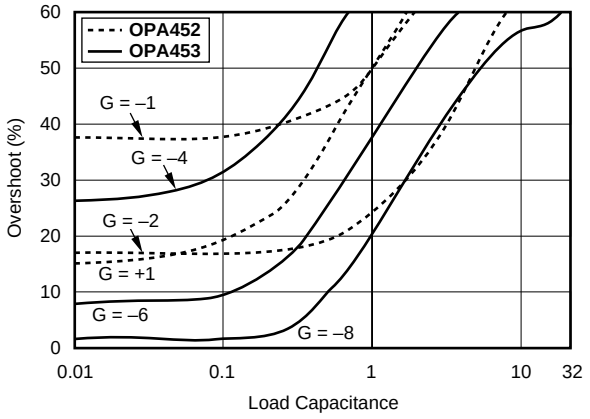


TYPICAL CHARACTERISTICS (Cont.)

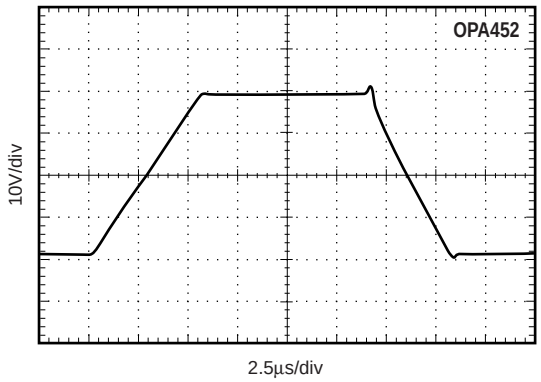
At T_J = +25°C, V_S = ±40V, and R_L = 3.8kΩ, unless otherwise noted.

All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.

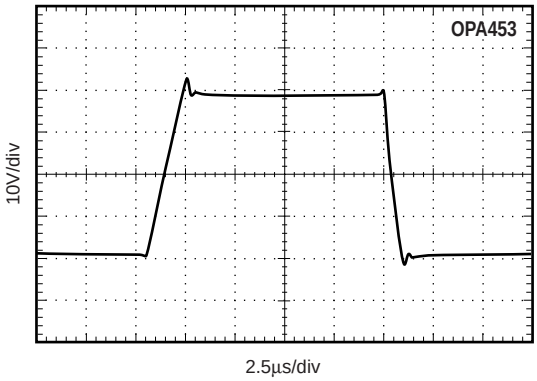
SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



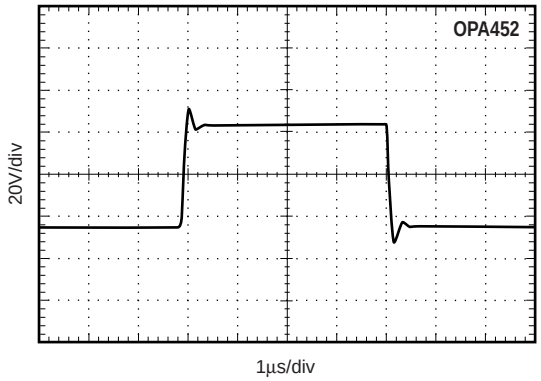
LARGE-SIGNAL STEP RESPONSE
(G = 1, C_L = 100pF)



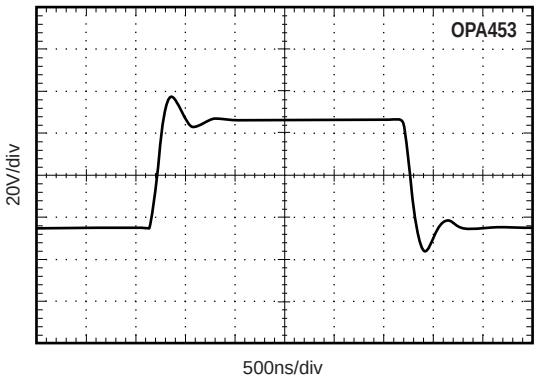
LARGE-SIGNAL STEP RESPONSE
(G = 5, C_L = 100pF)



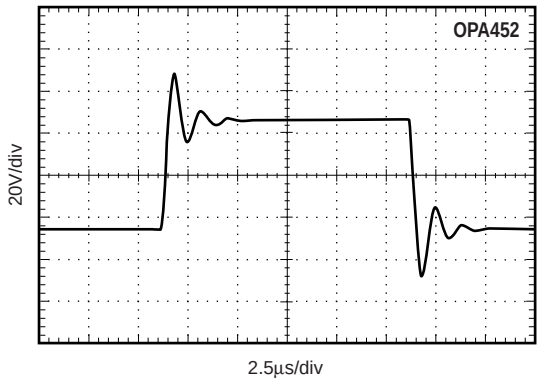
SMALL-SIGNAL STEP RESPONSE
(G = 1, C_L = 100pF)



SMALL-SIGNAL STEP RESPONSE
(G = 5, C_L = 100pF)



SMALL-SIGNAL STEP RESPONSE
(G = –1, C_L = 1000pF)



APPLICATIONS INFORMATION

Figure 1 shows the OPA452 connected as a basic noninverting amplifier. The OPA452 can be used in virtually any op amp configuration. The OPA453 is designed for use in configurations with gains of 5 or greater. Power-supply terminals should be bypassed with 0.1µF capacitors, or greater, near the power-supply pins. Be sure that the capacitors are appropriately rated for the power-supply voltage used. The OPA452 and OPA453 can supply output currents up to 50mA with excellent performance.

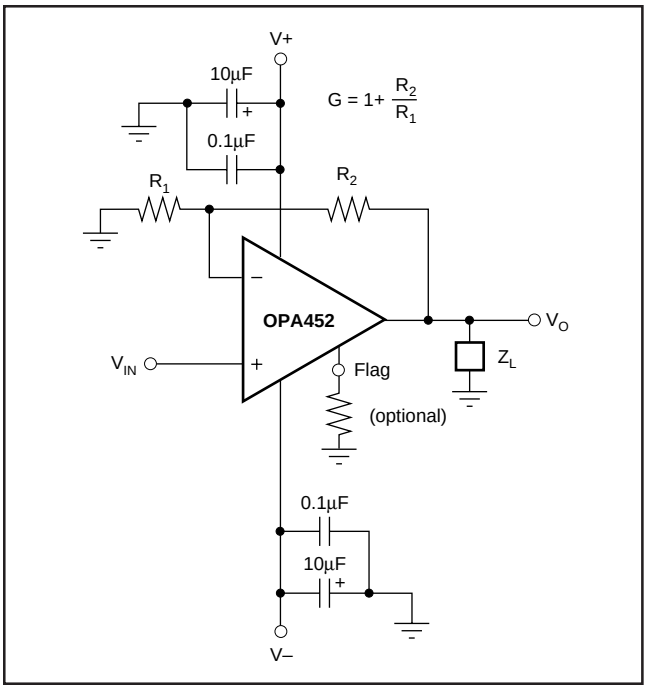


FIGURE 1. Basic Circuit Connections.

CURRENT LIMIT

The OPA452 and OPA453 are designed with internal current-limiting circuitry that limits the output current to approximately 125mA. The current limit varies slightly with increasing junction temperature and supply voltage, as shown in the Typical Characteristics. Current limit, in combination with the thermal protection circuitry, provides protection from most types of overload conditions including short-circuit to ground.

THERMAL PROTECTION

The OPA452 and OPA453 have thermal shutdown circuitry that protects the amplifier from damage caused by overload conditions. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is automatically re-enabled.

The thermal shutdown function is not intended to replace proper heat sinking. Activation of the thermal shutdown circuitry is an indication of excessive power dissipation or an inadequate heat sink. Continuously running the amplifier into thermal shutdown can degrade reliability.

The Thermal Shutdown Indicator (Flag) pin can be monitored to determine if shutdown is occurring. During normal operation, the current output from the flag pin is typically 50nA. During shutdown, the current output from the flag pin increases to 140µA (typical). This current output allows for easy interfacing to external logic. Figure 2 shows two examples implementing this function.

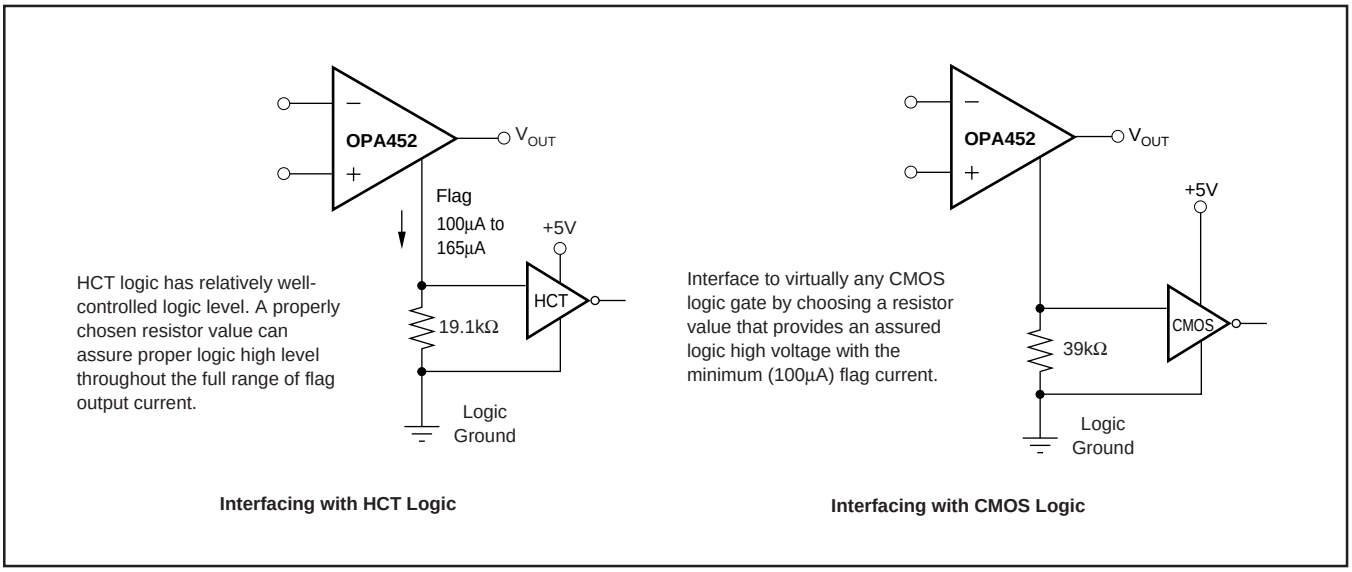


FIGURE 2. Thermal Shutdown Indicator.

POWER SUPPLIES

The OPA452 and OPA453 may be operated from power supplies of ±10V to ±40V, or a total of 80V with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the Typical Characteristics.

For applications that do not require symmetrical output voltage swing, power-supply voltages do not need to be equal. The OPA452 and OPA453 can operate with as little as 20V between the supplies or with up to 80V between the supplies. For example, the positive supply could be set to 70V with the negative supply at –10V or vice-versa.

The tabs of the DDPAK-7 and TO220 packages are electrically connected to the negative supply (V–), however, these connections should not be used to carry current. For best thermal performance, the tab should be soldered directly to the circuit board copper area (see Heat Sinking section).

POWER DISSIPATION

Internal power dissipation of these op amps can be quite large. All of the specifications for the OPA452 and OPA453 may change with junction temperature. If the device is not subjected to internal self-heating, the junction temperature will be the same as the ambient. However, in practical applications, the device will self-heat and the junction temperature will be significantly higher than ambient. The following calculation can be performed to establish junction temperature as a function of ambient temperature and the conditions of the application.

Consider the OPA452 in a circuit configuration where the load is 600Ω and the output voltage is 20V. The supplies are at ±40V and the ambient temperature (T_A) is 40°C. The θ_{JA} for the package plus heat sink is 30°C/W.

First, the quiescent heating of the op amp is as follows:

$$P_{D(internal)} = I_Q \bullet V_S = 6mA \bullet 80V = 480mW$$

The output current (I_O) can be calculated:

$$I_O = V_O/R_L = 20V/600\Omega = 33.33mA$$

The power being dissipated (P_D) in the output transistor of the amplifier can be calculated:

$$P_{D(output\ stage)} = I_O \bullet (V_S - V_O) = 33.3mA \bullet (40 - 20) = 667mW$$

$$P_{D(total)} = P_{D(internal)} + P_{D(output\ stage)} = 480mW + 667mW = 1147mW$$

The resulting junction temperature can be calculated:

$$T_J = T_A + P_D\ \theta_{JA}$$

$$T_J = 40°C + 1147mW \bullet 30°C/W = 74.4°C$$

Where,

V_O = output voltage

V_S = supply voltage

I_O = output current

R_L = load resistance

T_J = junction temperature (°C)

T_A = ambient temperature (°C)

θ_{JA} = junction-to-air thermal resistance (°C/W)

To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection should trigger more than +35°C above the maximum expected ambient condition of your application. This ensures a maximum junction temperature of +125°C at the maximum expected ambient condition.

Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation because a larger voltage can be impressed across the conducting output transistor. Consult Application Bulletin SBOA022 at www.ti.com for further information on how to calculate or measure power dissipation.

Power dissipation can be minimized by using the lowest possible supply voltage. For example, with a 50mA load, the output will swing to within 5.0V of the power-supply rails. Power supplies set to no more than 5.0V above the maximum output voltage swing required by the application will minimize the power dissipation.

SAFE OPERATING AREA

The Safe Operating Area (SOA curves, Figure 3) shows the permissible range of voltage and current. The safe output current decreases as the voltage across the output transistor ($V_S - V_O$) increases. For further insight on SOA, consult Application Report SBOA022.

Output short circuits are a very demanding case for SOA. A short-circuit to ground forces the full power-supply voltage (V+ or V–) across the conducting transistor and produces a

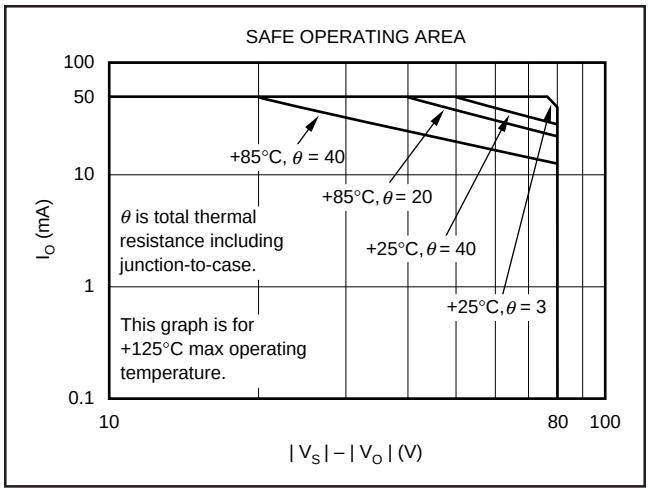


FIGURE 3. DDPAK-7 and TO220-7 Safe Operating Area.

typical output current of 125mA. With ±40V power supplies, this creates an internal dissipation of 10W. This far exceeds practical heat sinking and is not recommended. If operation in this region is unavoidable, use the part with a heat sink.

HEAT SINKING

Power dissipated in the OPA452 or OPA453 will cause the junction temperature to rise. For reliable operation, the junction temperature should be limited to +125°C. Many applications will require a heat sink to assure that the maximum operating junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions.

For heat sinking purposes, the tab of the DDPAK is typically soldered directly to a circuit board copper area. Increasing the copper area improves heat dissipation. Figure 4 shows typical thermal resistance from junction-to-ambient as a function of copper area.

Depending on conditions, additional heat sinking may be required. Aavid Thermal Products Inc. manufactures surface-mountable heat sinks designed specifically for use with these packages. Further information is available on Aavid's web site, www.aavid.com.

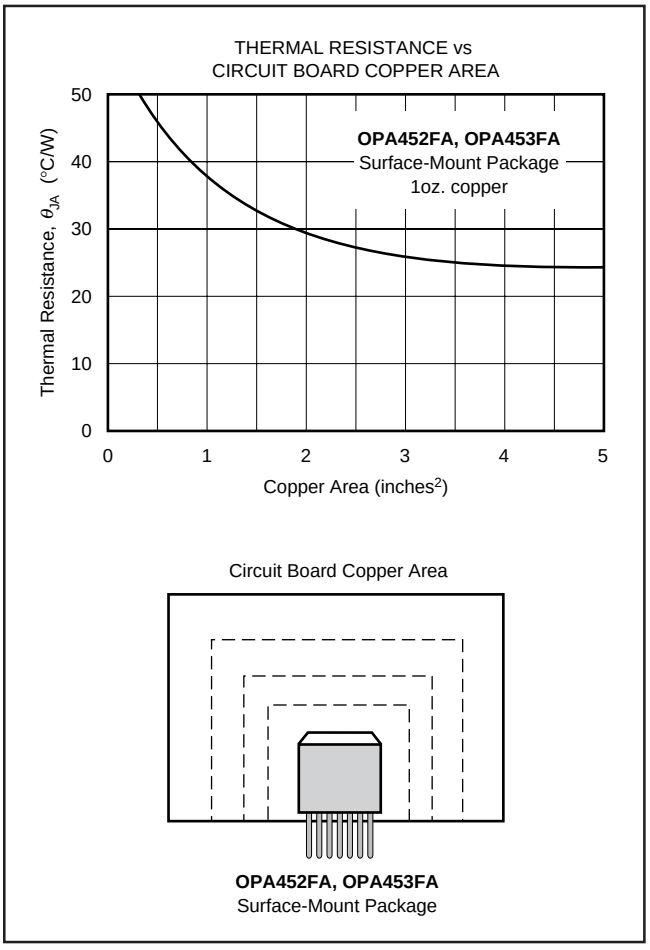


FIGURE 4. DDPAK Thermal Resistance versus Circuit Board Copper Area.

CAPACITIVE LOADS

The dynamic characteristics of the OPA452 and OPA453 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Figure 5 shows a circuit that preserves phase margin with capacitive load. Figure 6 shows the small-signal step response for the circuit in Figure 5. Consult Application Bulletin SBOA015, at www.ti.com, for more information.

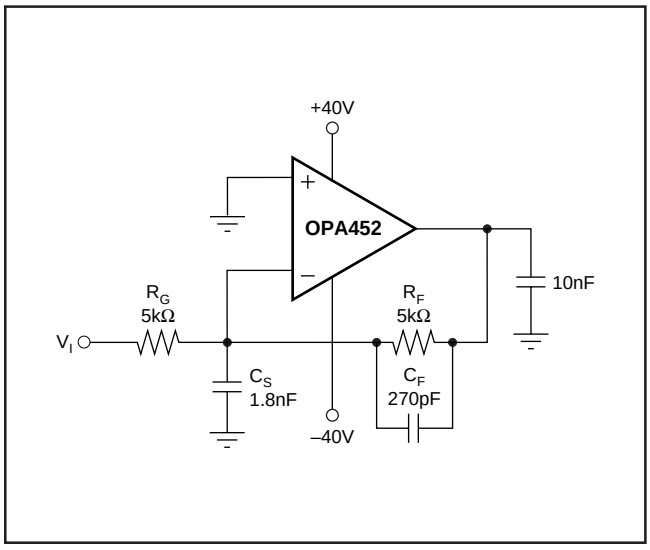


FIGURE 5. Driving Large Capacitive Loads.

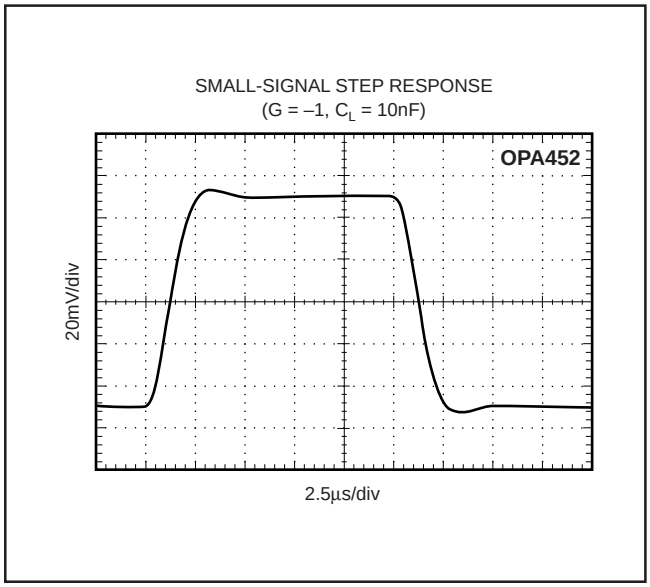


FIGURE 6. Small-Signal Step Response for Figure 5.

INCREASING OUTPUT CURRENT

In those applications where the 50mA of output current is not sufficient to drive the desired load, output current can be increased by connecting two or more OPA452s or OPA453s in parallel, as shown in Figure 7. Amplifier A1 is the master amplifier and may be configured in virtually any op amp circuit. Amplifier A2, the slave, is configured as a unity gain buffer. Alternatively, external output transistors can be used to boost output current. The circuit in Figure 8 is capable of supplying output currents up to 1A. Alternatively, the OPA547, OPA548, and OPA549 series power op amps should be considered for high output current drive, along with programmable current limit and output disable capability.

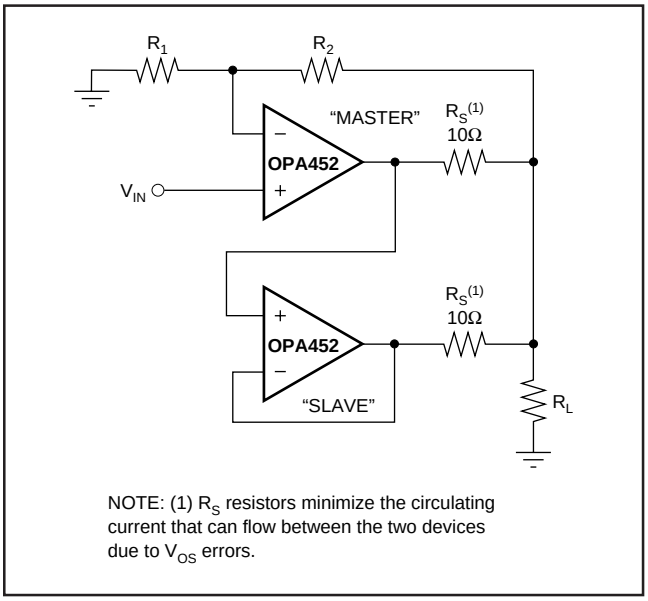


FIGURE 7. Parallel Amplifiers Increase Output Current Capability.

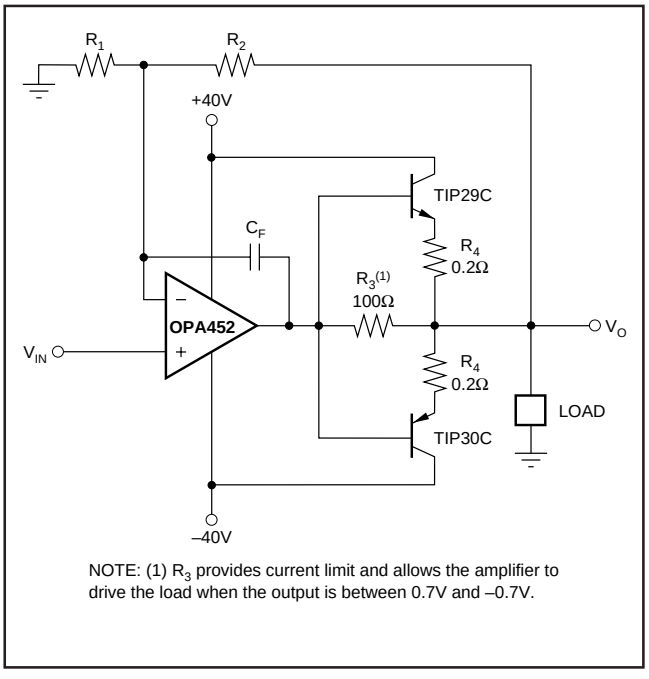


FIGURE 8. External Output Transistors Boost Output Current Up to 1 Amp.

INPUT PROTECTION

The OPA452 and OPA453 feature internal clamp diodes to protect the inputs when voltages beyond the supply rails are encountered. However, input current should be limited to 5mA. In some cases, an external series resistor may be required. Many input signals are inherently current-limited, therefore, a limiting resistor may not be required. Please consider that a large series resistor, in conjunction with the input capacitance, can affect stability.

USING THE OPA453 IN LOW GAINS

The OPA453 is intended for applications with signal gains of 5 or greater, but it is possible to take advantage of its high slew rate in lower gains using an external compensation technique in an inverting configuration. This technique maintains low noise characteristics of the OPA453 architecture at low frequencies. Depending on the application, a small increase in high-frequency noise may result. This technique shapes the loop gain for good stability while giving an easily controlled 2nd-order low-pass frequency response.

Considering only the noise gain (noninverting signal gain) for the circuit of Figure 9, the low-frequency noise gain (NG_1) will be set by the resistor ratios, whereas the high-frequency noise gain (NG_2) will be set by the capacitor ratios. The capacitor values set both the transition frequencies and the high-frequency noise gain. If this noise gain, determined by $NG_2 = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp and the noise gain pole, set by $1/R_FC_F$, is placed correctly, a very well controlled, 2nd-order low-pass frequency response will result.

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. First, the target for the high-frequency noise gain (NG_2) should be greater than the minimum stable gain for the OPA453. In the circuit in Figure 9, a target NG_2 of 10 is used. Second, the signal gain of –1 in Figure 10 sets the low-frequency noise gain to $NG_1 = 1 + R_F/R_G$ (= 2 in this example). Using these two gains, knowing the Gain Bandwidth Product (GBP) for the OPA453 (7.5MHz), and targeting a maximally flat 2nd-order, low-pass Butterworth frequency response (Q = 0.707), the key frequency in the compensation can be found.

For the values in Figure 9, the $f_{–3dB}$ will be approximately 180kHz. This is less than that predicted by simply dividing the GBP by NG_1. The compensation network controls the bandwidth to a lower value while providing good slew rate at the output and an exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \bullet Z_0$. The capacitor values in Figure 10 are calculated for $NG_1 = 2$ and $NG_2 = 10$ with no adjustment for parasitics.

Actual circuit values can be optimized by checking the small-signal step response with actual load conditions. See Figure 9 for the small-signal step response of this OPA453, G = –1 circuit with a 1000pF load. It is well-behaved with no tendency to oscillate. If C_S and C_F were removed, the circuit would be unstable.

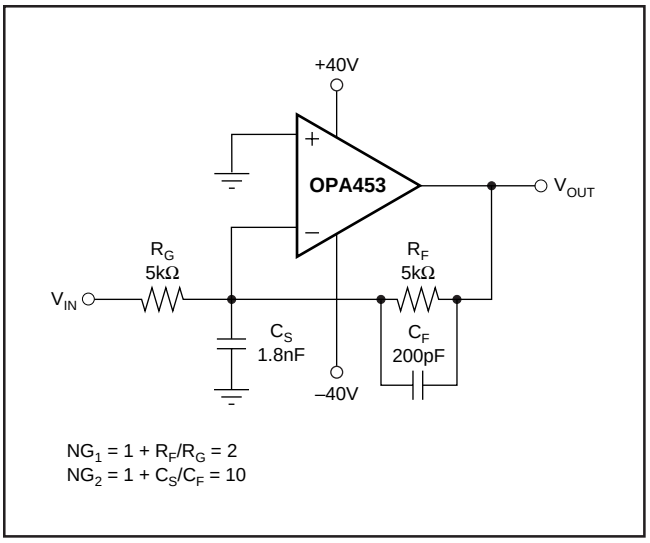


FIGURE 9. Compensation of the OPA453 for G = –1.

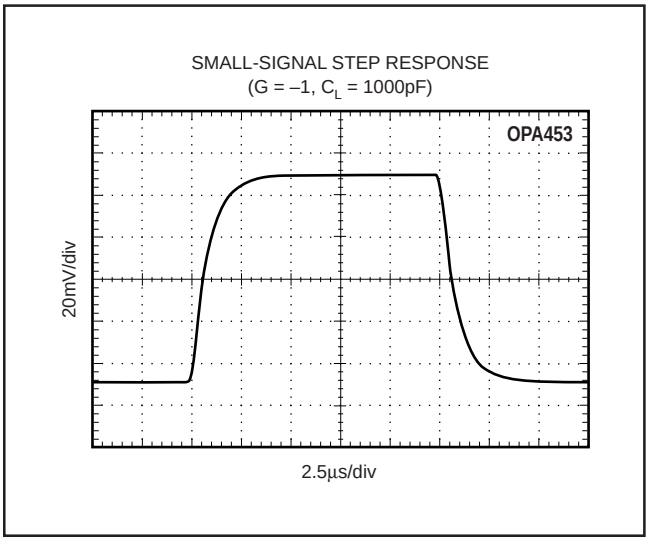


FIGURE 10. Small-Signal Step Response for Figure 9.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA452FA/500	ACTIVE	DDPAK/ TO-263	KTW	7	500	RoHS & Green	Call TI | SN	Level-3-245C-168 HR	-40 to 125	OPA452F	Samples
OPA452FAKTWT	ACTIVE	DDPAK/ TO-263	KTW	7	250	RoHS & Green	Call TI | SN	Level-3-245C-168 HR	-40 to 125	OPA452F	Samples
OPA452FAKTWTG3	ACTIVE	DDPAK/ TO-263	KTW	7	250	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	OPA452F	Samples
OPA453FAKTWT	ACTIVE	DDPAK/ TO-263	KTW	7	250	RoHS & Green	Call TI | SN	Level-3-245C-168 HR	-40 to 125	OPA453F	Samples
OPA453TA	ACTIVE	TO-220	KC	7	50	RoHS & Green	Call TI | SN	N / A for Pkg Type	-40 to 125	OPA453T	Samples
OPA453TA-1	ACTIVE	TO-220	KVT	7	50	RoHS & Green	Call TI | SN	N / A for Pkg Type	-40 to 125	OPA453T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

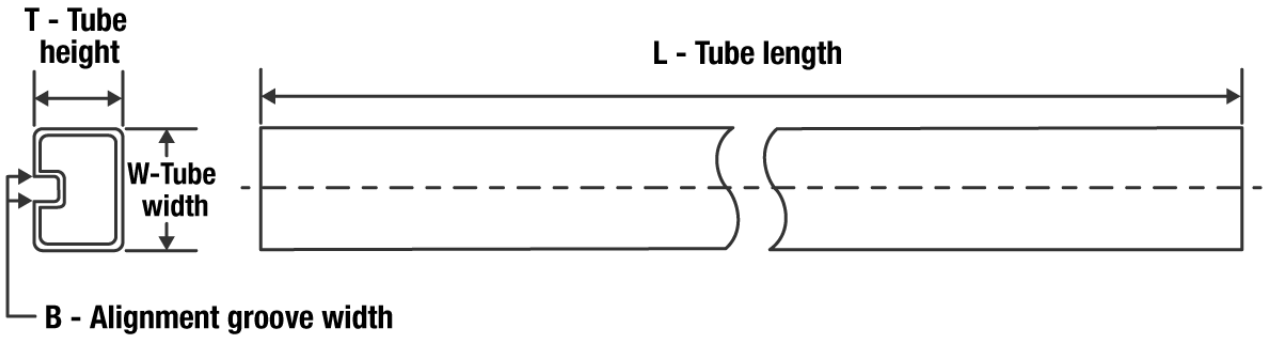
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE

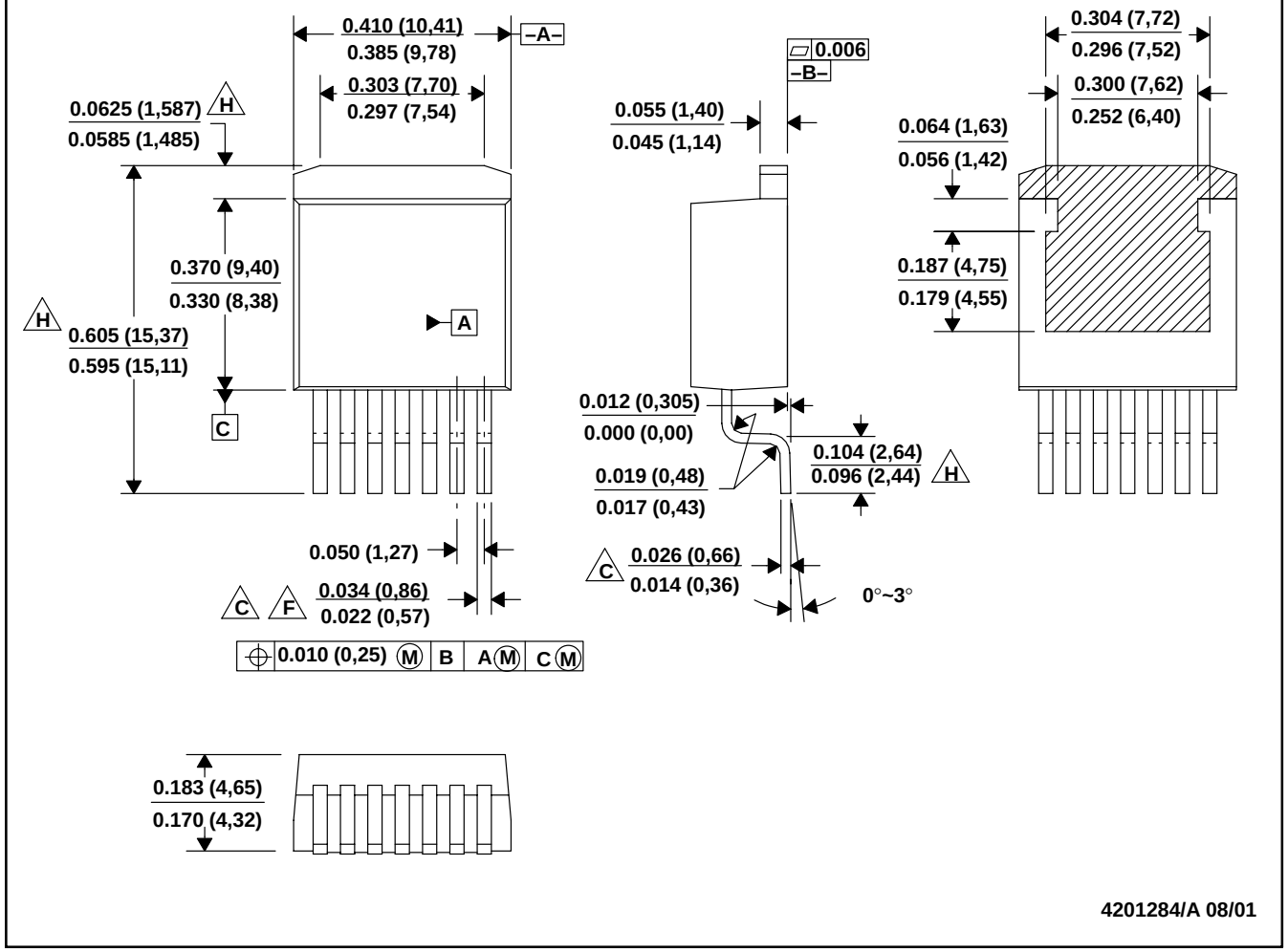


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA453TA	KC	TO-220	7	50	532.13	34.54	13340	NA
OPA453TA-1	KVT	TO-220	7	50	532.13	34.54	13340	NA

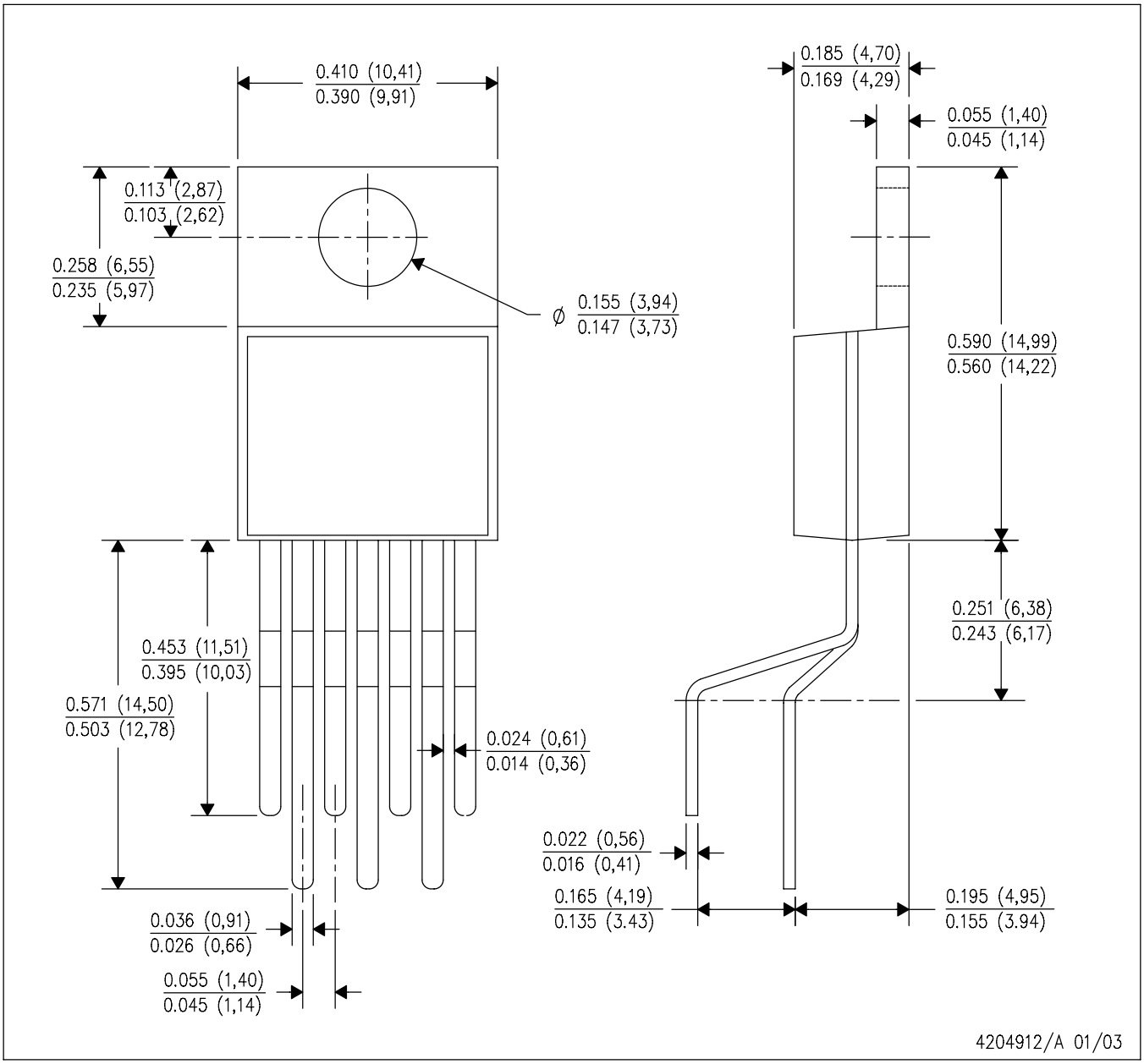
MPSF015 – AUGUST 2001

KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



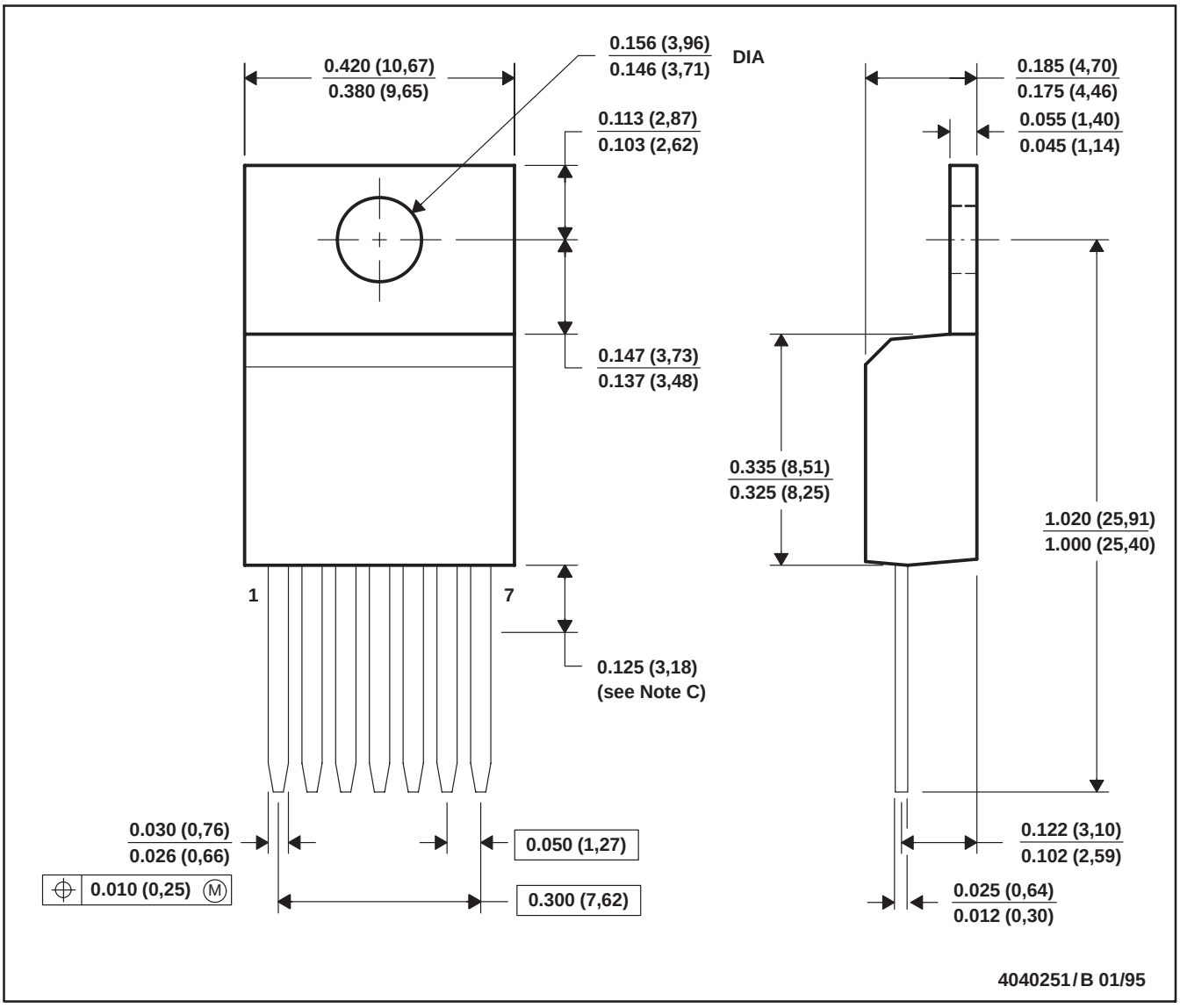
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

KVT (R–PZFM–T7) PLASTIC FLANGE MOUNT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

KC (R-PSFM-T7) **PLASTIC FLANGE-MOUNT PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.

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