TPS65279 具有电流均流功能的 4.5V 至 18V 输入、5A/5A 双路同步降压转换器

1 特性

- 4.5V 至 18V 宽输入电压范围
- 针对输出电压转换的可编程转换率控制
- 降压转换器 1 和降压转换器 2 中高达 5A 最大持续输出电流
- 可将降压转换器 1 和降压转换器 2 并联以传送高达 10A 的电流
- 脉冲跳跃模式，可实现轻负载条件下的高效率
- 可调开关频率为 200kHz 至 1.6MHz（由外部电阻设置）
- 针对每个降压转换器的专用使能和软启动
- 具有简单补偿电路的峰值电流模式控制
- 逐周期过流保护
- 180° 相移运行可减少输入电容量和电源引入感应噪声
- 过热保护
- 可提供 32 引脚耐热增强型带散热片薄型小外形尺寸封装 (HTSSOP) (DAP) 以及 36 引脚超薄四方扁平无引线 (VQFN) 6mm × 6mm (RHH) 封装

2 应用范围

- 数字电视 (DTV)
- 电信和网络
- 负载点
- 机顶盒
- 平板电脑

3 说明

TPS65279 是一款具有 4.5V 至 18V 宽工作输入电压范围的单片双路同步降压转换器，它的电压范围曾包括大多数中间总线关闭电压为 5V，9V，12V 或 15V 的电源总线或电池。 这个具有恒定频率峰值电流模式控制的转换器被设计用来简化它的应用，与此同时，能够使设计人员根据目标应用来优化他们的使用方法。

通过使用电流均流模式，将 ISHARE 引脚接至高电平，可将 TPS65279 中的两个降压转换器并联，以传送高达 10A 负载电流。 采用电流均流的两相位运行减少了系统滤波电容和电感，减轻了电磁干扰 (EMI) 并改进了输出电压纹波和噪声。

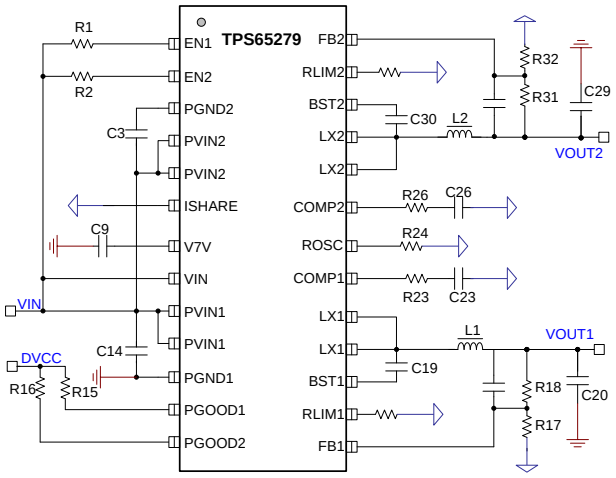
TPS65279 特有一个专用使能引脚。 一个独立软启动引脚提供加电可编程性中的灵活性。 恒定频率峰值电流模式简化了补偿并提供快速瞬态响应。 逐周期过流保护和断续模式操作可在出现短路或过载故障条件时限制 MOSFET 功耗。

器件信息(1)

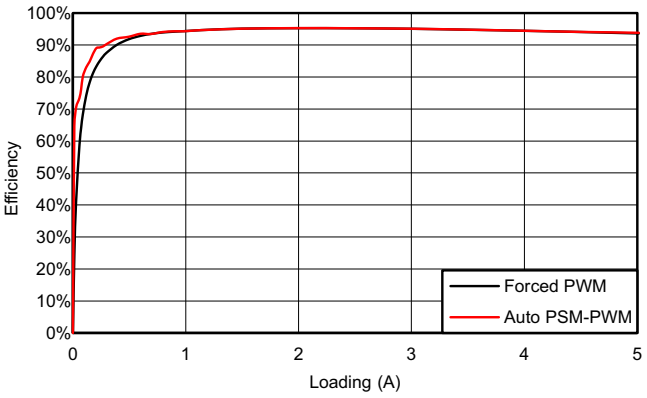
部件号	封装	封装尺寸（标称值）
TPS65279	HTSSOP (32)	6.20mm × 11.00mm
	VQFN (36)	6.00mm x 6.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



效率与负载间的关系



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4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2013) to Revision C **Page**

- 已添加 *ESD 额定值表，特性描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分* ... 1
- Updated conditions for *Electrical Characteristics* from T_J = 25°C to T_J = –40°C to 125°C ... 6
- Updated UVLO minimum for falling V_{IN} to 3.4 from 3.5 ... 6
- Updated enable threshold rising maximum to 1.3 and falling minimum to 1.0, from 1.26 and 1.10, respectively ... 6

Changes from Revision A (December 2013) to Revision B **Page**

- Changed I_{LIMIT2} test conditions ... 6
- Changed *Functional Block Diagram* ... 12
- Changed *Current Sharing Operation* section ... 15
- Changed Loop Compensation section ... 20

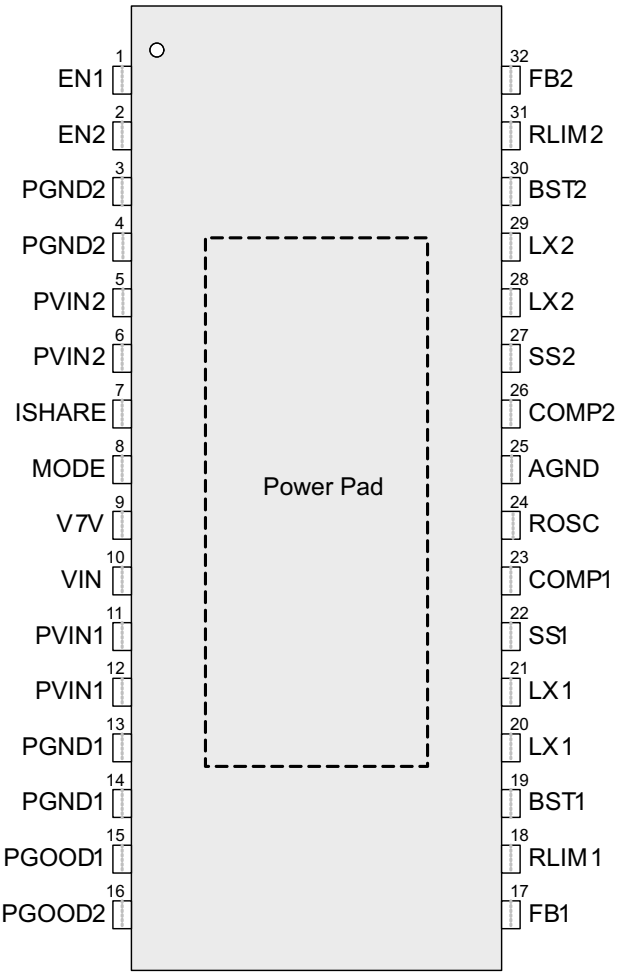
5 说明（续）

低侧反向过流保护还能够防止过多灌电流损坏转换器。 TPS65279 还特有一个由 MODE 引脚配置控制的轻负载脉冲跳跃模式 (PSM)。

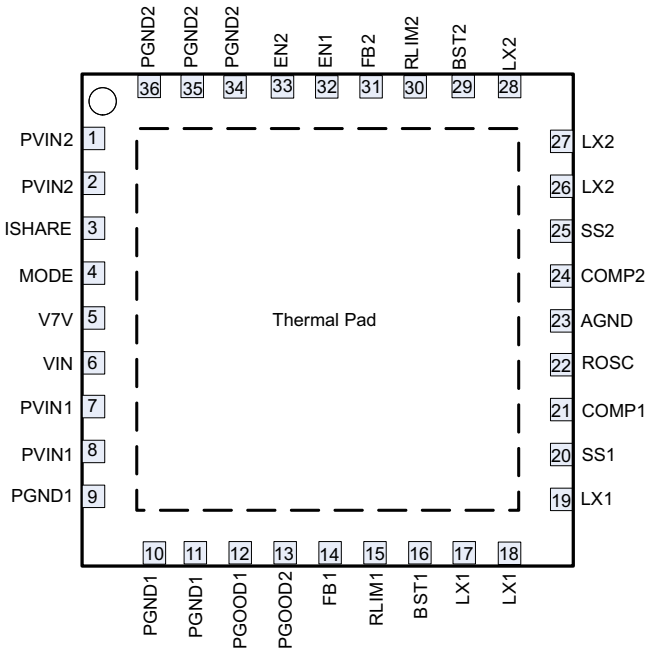
TPS65279 采用 32 引脚耐热增强型 HTSSOP (DAP) 封装和 36 引脚 6mm × 6mm VQFN (RHH) 封装。

6 Pin Configuration and Functions

DAP Package
32-Pin HTSSOP
Top View



RHH Package
36-Pin VQFN
Top View



Pin Functions

PIN			DESCRIPTION
NAME	HTSSOP	VQFN	
EN1, EN2	1, 2	32, 33	Enable pin. Adjust the input under-voltage lockout with two resistors.
PGND2	3, 4	34, 35, 36	Power ground of buck2, place the input capacitor's ground pin as close as possible to this pin.
PVIN2	5, 6	1, 2	Power input. Input power supply to the power switches of the power converter 2.
ISHARE	7	3	Logic pin to configure current sharing mode, tie to high to parallel two buck converters, in current sharing mode, buck1 will be used; tie to low to run in separate mode.
MODE	8	4	Connecting this pin to ground, the buck converter forces a continuous current mode (CCM) operation. Connecting this pin to V7V, the buck converter automatically operates in pulse skipping mode (PSM) at light load condition to save the power.
V7V	9	5	Internal low-drop linear regulator (LDO) output to power internal driver and control circuits. Decouple this pin to power ground with a minimum 1-µF ceramic capacitor. Output regulates to typical 6.3 V for optimal conduction on-resistances of internal power MOSFETs. In PCB design, the power ground and analog ground should have one-point common connection at the (-) terminal of V7V bypass capacitor. If VIN is lower than 6.3 V, V7V will be slightly lower than VIN.
VIN	10	6	Power supply of the internal LDO and controllers
PVIN1	11, 12	7, 8	Power input. Input power supply to the power switches of the power converter 1.
PGND1	13, 14	9, 10, 11	Power ground of buck1, place the input capacitor's ground pin as close as possible to this pin.
PGOOD1	15	12	Power Good pin for buck1, open drain output, when output is within range, output high impedance, a 100-kΩ resistor is recommended to connect to this pin.
PGOOD2	16	13	Power Good pin for buck2, open drain output, when output is within range, output high impedance, a 100-kΩ resistor is recommended to connect to this pin.
FB1	17	14	Feedback sensing pin for buck1 output voltage. Connect this pin to the resistor divider of buck1 output. The feedback reference voltage is 0.6 V ±1%.
RLIM1	18	15	Current limit threshold set pin for buck1, connect a resistor between this pin to GND to set the OCP.
BST1	19	16	Add a bootstrap capacitor between BST1 and LX1. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET.
LX1	20, 21	17, 18, 19	Switching node of buck1
SS1	22, 27	20, 25	Soft-start and voltage tracking in buck1. An external capacitor connected to this pin sets the internal voltage reference rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing. In current sharing application, this pin serves as the soft-start pin.
COMP1	23	21	Error amplifier output and loop compensation pin for buck1. Connect frequency compensation to this pin; In current sharing application, this pin serves as the compensation pin.
ROSC	24	22	Oscillator frequency programmable pin. Connect an external resistor to set the switching frequency. When connected to an external clock, the internal oscillator synchronizes to the external clock.
AGND	25	23	Analog ground of the controllers
COMP2	26	24	Error amplifier output and loop compensation pin for buck2. Connect frequency compensation to this pin. In current sharing application, float this pin.
SS2	27	25	Soft-start and voltage tracking in buck2. An external capacitor connected to this pin sets the internal voltage reference rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and power sequencing. In current sharing application, float this pin.
LX2	28, 29	26, 27, 28	Switching nodes
BST2	30	29	Add a bootstrap capacitor between BST2 and LX2. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET of buck2.
RLIM2	31	30	Current limit threshold set pin for buck2, connect a resistor between this pin to GND to set the OCP.
FB2	32	31	Feedback sensing pin for buck2 output voltage. Connect this pin to the resistor divider of buck2 output. The feedback reference voltage is 0.6 V ±1%. In current sharing mode, connect this pin to ground.
Exposed Thermal Pad	33	37	Exposed thermal pad of the package. Connect to the power ground. Always solder thermal pad to the board, and have as many vias as possible on the PCB to enhance power dissipation. There is no electric signal down bonded to the thermal pad inside the IC package.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Voltage at VIN, PVIN1, PVIN2	–0.3	20	V
	Voltage at LX1, LX2 (maximum withstand voltage transient < 20 ns)	–4.5	23	V
	Voltage at BST1, BST2, referenced to LX1, LX2 pin	–0.3	7	V
	Voltage at V7V, EN1, EN2, RLIM1, RLIM2, PGOOD1, PGOOD2, MODE, ISHARE, ROSC	–0.3	7	V
	Voltage at SS1, SS2, FB1, FB2, COMP1, COMP2	–0.3	3.6	V
	Voltage at AGND, PGND1, PGND2	–0.3	0.3	V
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM)	2000	V
		Charge device model (CDM)	1000	

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply input voltage range	4.5	18	V
I_{OUT1}, I_{OUT2}	Load current	0	5	A
V_{out}	Output voltage	0.6	9	V
EN	Enable voltage	0	6	V
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS65279		UNIT
		DAP (HTSSOP)	RHH (VQFN)	
		32 PINS	36 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	30.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.7	18.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19	6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.9	6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range	VIN1 and VIN2	4.5		18	V
IDD_{SDN}	Shutdown supply current	EN1 = EN2 = low		10		µA
IDD_{Q_NSW}	Switching quiescent current with no load at DCDC output	EN1 = EN2 = 3.3 V With power skip mode, without bucks switching		1.2		mA
IDD_{Q_SW}	Switching quiescent current with no load at DCDC output, Buck switching	EN1 = EN2 = 3.3 V With bucks switching		10		mA
UVLO	V_{IN} undervoltage lockout	Rising V_{IN}		4.25	4.50	V
		Falling V_{IN}	3.4	3.75		
		Hysteresis		0.5		
V_{7V}	6.3 V LDO	V_{7V} load current = 0 A	6.10	6.3	6.5	V
I_{OCP_V7V}	Current limit of V7V LDO			200		mA
ENABLE						
V_{ENR}	Enable threshold	Rising		1.21	1.3	V
V_{ENF}	Enable threshold	Falling	1.0	1.17		V
I_{ENR}	Enable Input current	EN = 1 V		3		µA
I_{ENF}	Enable hysteresis current	EN = 1.5 V		3		µA
OSCILLATOR						
F_{SW}	Switching frequency		200		1600	kHz
		R_{OSC} = 100 kΩ (1%)	340	400	460	
t_{SYNC_w}	Clock sync minimum pulse width			20		ns
V_{SYNC_HI}	Clock sync high threshold				2	V
V_{SYNC_LO}	Clock sync low threshold		0.8			V
V_{SYNC_D}	Clock falling edge to LX rising edge delay			66		ns
F_{SYNC}	Clock sync frequency range		200		1600	kHz
BUCK 1, BUCK 2 CONVERTERS						
$V_{ref(min)}$	Voltage reference	0 A < I_{OUT1} < 6 A, 0 A < I_{OUT2} < 3.5 A	0.594	0.6	0.606	V
$V_{LINEREG}$	Line regulation-DC	I_{OUT} = 2 A		0.5		%/V
$V_{LOADREG}$	Load regulation-DC	I_{OUT} = (10-90%) x I_{OUT_max}		0.5		%/A
G_{m_EA}	Error amplifier trans-conductance	-2 µA < I_{COMP} < 2 µA		1350		µS
G_{m_SRC}	COMP voltage to inductor current Gm	I_{LX} = 0.5 A		10		A/V
I_{SSx}	Soft-start pin charging current			6		µA
I_{LIMIT1}	Buck 1 peak inductor current limit	R_{LIM1} = 60.4 kΩ		7.3		A
I_{LIMIT2}	Buck 2 peak inductor current limit	R_{LIM2} = 60.4 kΩ		7.3		A
$I_{LIMITLSx}$	Low side sinking current limit			-2.6		A
R_{dsonx_HS}	On resistance of high side FET	V7V = 6.3 V		31		mΩ
R_{dsonx_LS}	On resistance of low side FET	V_{IN} = 12 V		23		mΩ
T_{minon}	Minimum on time			94		ns
V_{bootUV}	Boot-LX UVLO			2.1	3	V
$T_{hiccupwait}$	Hiccup wait time			512		cycles
T_{hiccup_re}	Hiccup time before re-start			16384		cycles

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD						
V_{PGOOD}	PGOOD trip levels	FB rising to PGOOD high		94%		
		FB falling to PGOOD low		92.5%		
		FB rising to PGOOD low		107.5%		
		FB falliong to PGOOD high		105.5%		
THERMAL SHUTDOWN						
T_{TRIP}	Thermal protection trip point	Rising temperature		160		°C
T_{HYST}	Thermal protection hysteresis			20		°C

7.6 Typical Characteristics

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

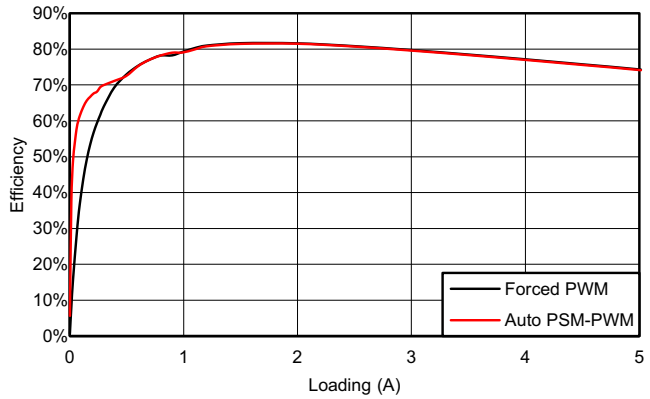


Figure 1. 0.8-V Efficiency
V_{IN} = 12 V, V_{OUT} = 0.8 V

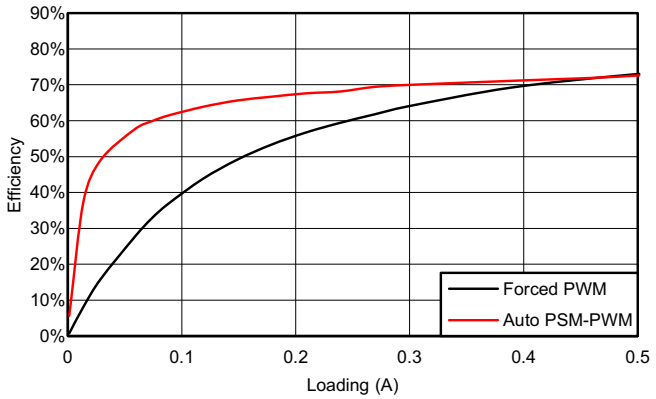


Figure 2. 0.8-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 0.8 V

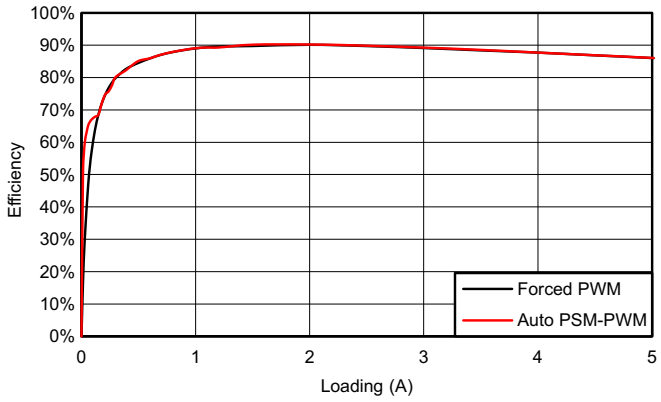


Figure 3. 1.8-V Efficiency
V_{IN} = 12 V, V_{OUT} = 1.8 V

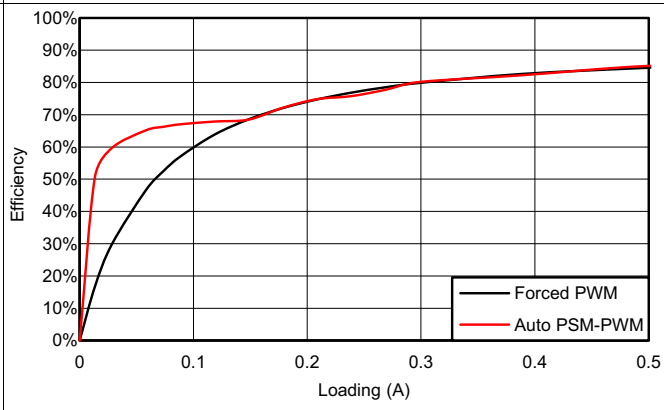


Figure 4. 1.8-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 1.8 V

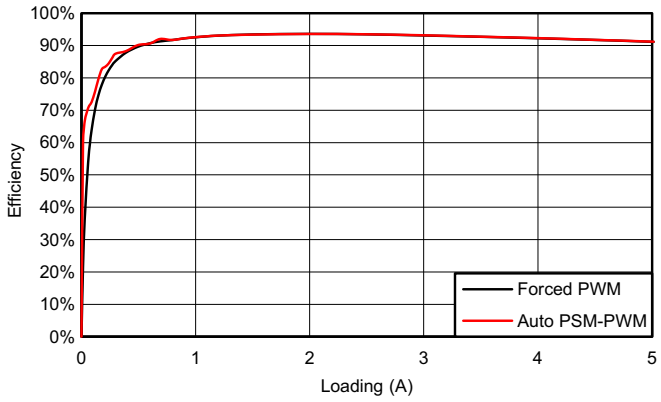


Figure 5. 3.3-V Efficiency
V_{IN} = 12 V, V_{OUT} = 3.3 V

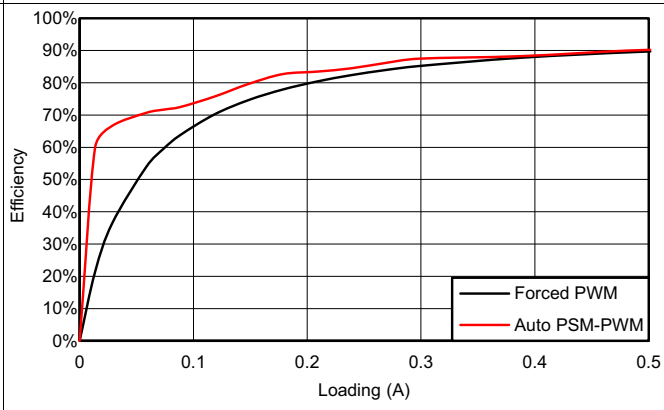


Figure 6. 3.3-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 3.3 V

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

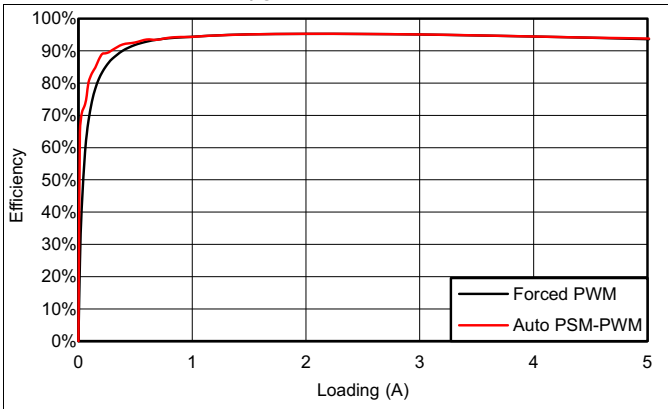


Figure 7. 5-V Efficiency
V_{IN} = 12 V, V_{OUT} = 5 V

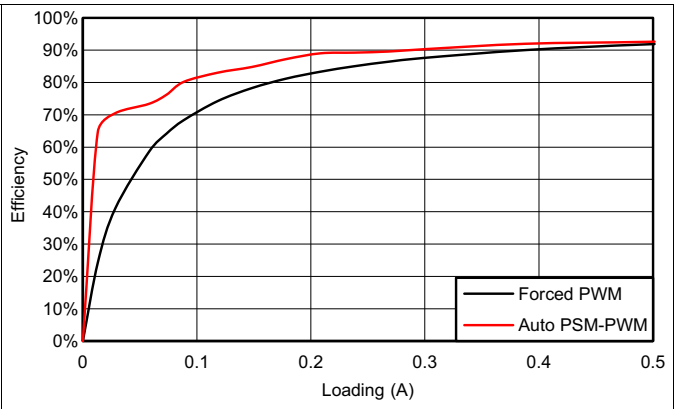


Figure 8. 5-V Efficiency, Light Load
V_{IN} = 12 V, V_{OUT} = 5 V

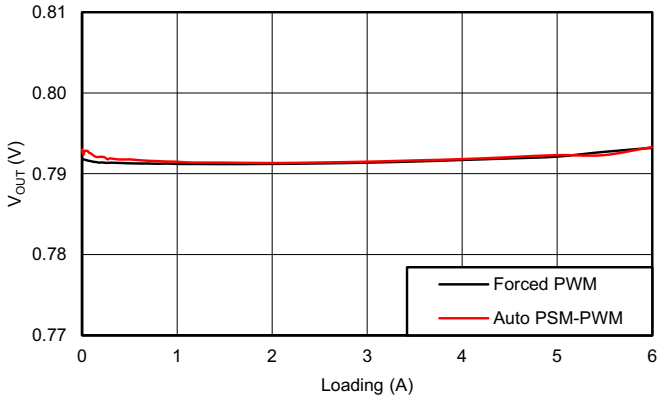


Figure 9. 0.8-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 0.8 V

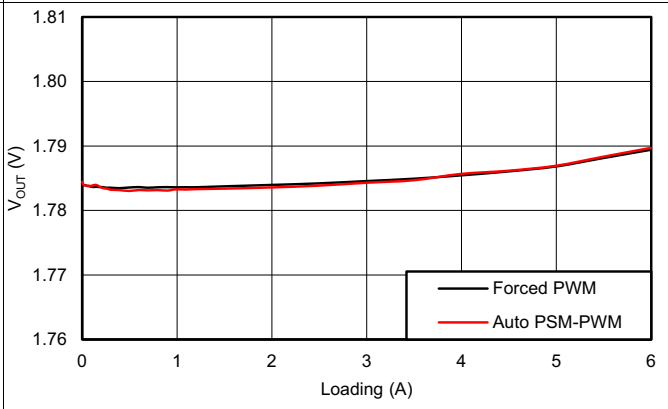


Figure 10. 1.8-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 1.8 V

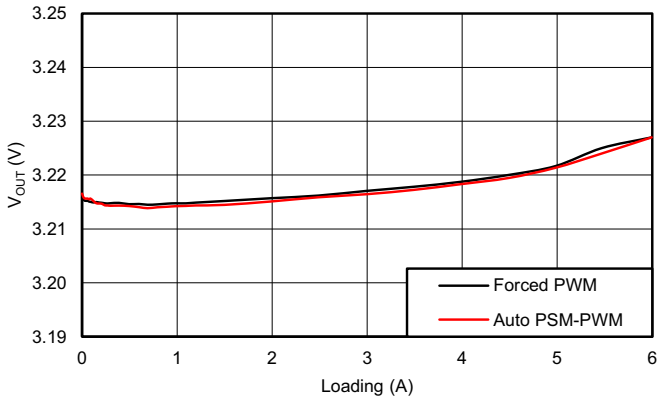


Figure 11. 3.3-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 3.3 V

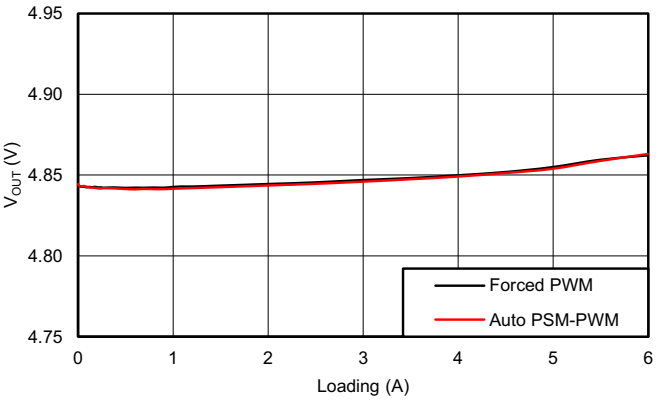


Figure 12. 5-V Load Regulation
V_{IN} = 12 V, V_{OUT} = 5 V

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 625 kHz (unless otherwise noted)

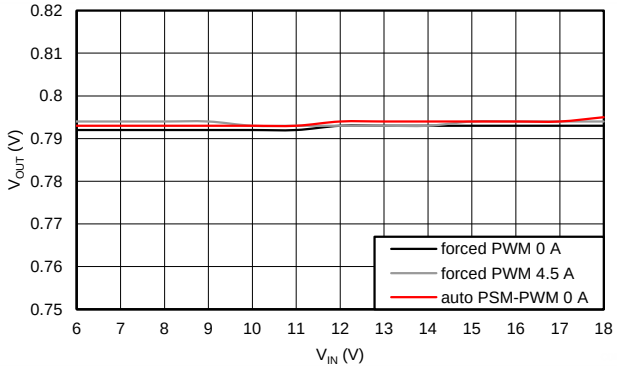


Figure 13. 0.8-V Line Regulation
V_{OUT} = 0.8 V

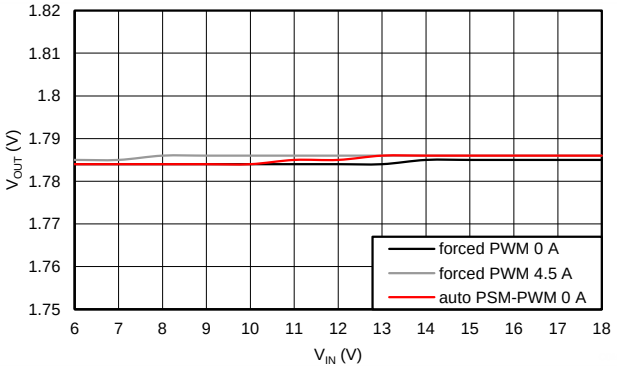


Figure 14. 1.8-V Line Regulation
V_{OUT} = 1.8 V

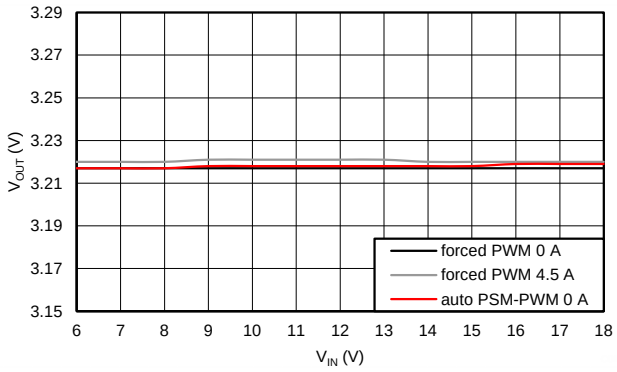


Figure 15. 3.3-V Line Regulation
V_{OUT} = 3.3 V

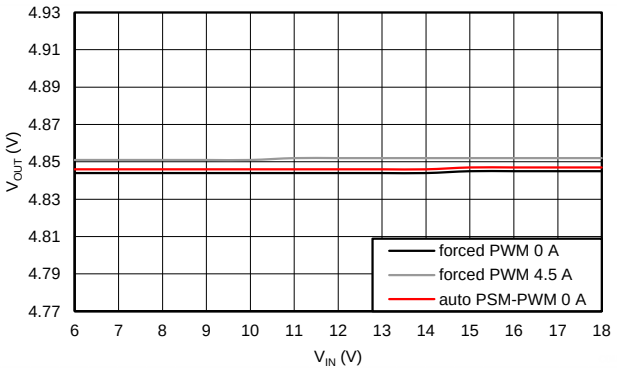


Figure 16. 5-V Line Regulation
V_{OUT} = 5 V

8 Detailed Description

8.1 Overview

TPS65279 is a dual 5-A/5-A output current, synchronous step-down (buck) converter with integrated N-channel MOSFETs. A wide 4.5-V to 18-V input supply range to buck encompasses most intermediate bus voltages operating off 9-V, 12-V or 15-V power bus.

TPS65279 implements a constant frequency, peak current mode control which simplifies external frequency compensation. The wide switching frequency of 200 kHz to 1600 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency can be adjusted with an external resistor to ground on the ROSC pin. The TPS65279 also has an internal phase lock loop (PLL) controlled by the ROSC pin that can be used to synchronize the switching cycle to the falling edge of an external system clock. 180° out-of-phase operation between two channels reduces input filter and power supply induced noise.

TPS65279 has been designed for safe monotonic startup into prebiased loads. The default start up is typically 4.5 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for automatically starting up the TPS65279 with the internal pullup current.

The integrated MOSFETs of each channel allow for high efficiency power supply designs with continuous output currents up to 5 A. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The TPS65279 reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and LX pins. The boot capacitor voltage is monitored by a BOOT to LX UVLO (BOOT-LX UVLO) circuit allowing LX pin to be pulled low to recharge the boot capacitor. The TPS65279 can operate at 100% duty cycle as long as the boot capacitor voltage is higher than the preset BOOT-LX UVLO threshold which is typically 2.1 V.

The TPS65279 has a power good comparator with hysteresis which monitors the output voltage through internal feedback voltage.

The SS (soft start/tracking) pin is used to minimize inrush current or provide power supply sequencing during power up. A small value capacitor or resistor divider should be coupled to the pin for soft start or critical power supply sequencing requirements.

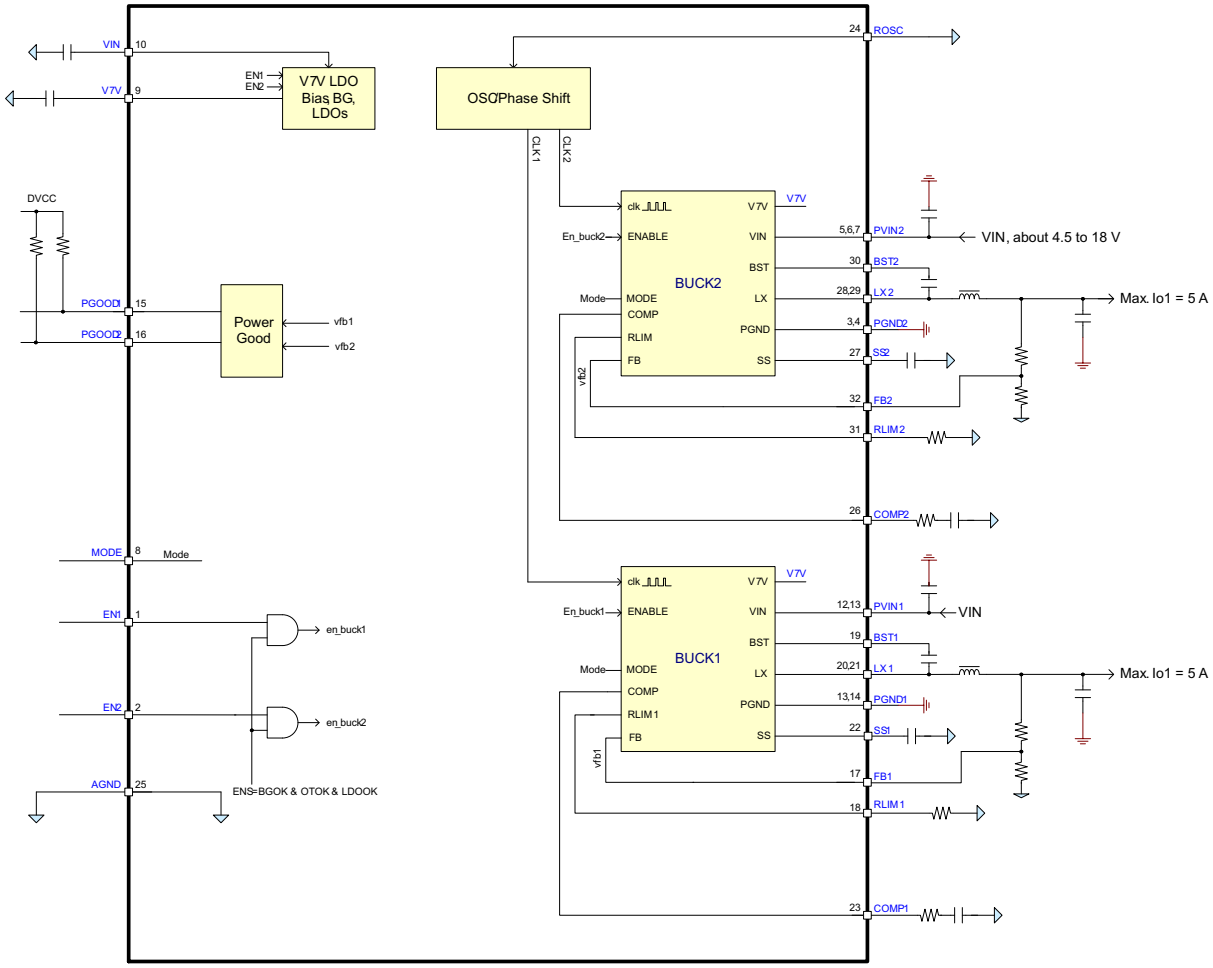
The TPS65279 is protected from output overvoltage, overload, and thermal fault conditions. The TPS65279 minimizes excessive output overvoltage transients by taking advantage of the power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the internal feedback voltage is lower than 107.5% of the 0.6-V reference voltage. The TPS65279 implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. If the over current condition has lasted for more than the hiccup wait time, the TPS65279 will shut down and re-start after the hiccup time. The TPS65279 also shuts down if the junction temperature is higher than thermal shutdown trip point. When the junction temperature drops 20°C typically below the thermal shutdown trip point, the built-in thermal shutdown hiccup timer is triggered. The TPS65279 will be restarted under control of the soft start circuit automatically after the thermal shutdown hiccup time is over.

Furthermore, if the over-current condition has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the TPS65279 will shut down itself and restart after the hiccup time which is set for 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe over-current conditions.

The TPS65279 operates at any load conditions unless the COMP pin voltage drops below the COMP pin start switching threshold which is typically 0.25 V.

When PSM mode operation is enabled, the TPS65279 monitors the peak switch current of the high-side MOSFET. Once the peak switch current is lower than typically 1 A, the device stops switching to boost the efficiency until the peak switch current is higher than typically 1 A again.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable and Adjusting Undervoltage Lockout (UVLO)

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 500 mV.

8.3.2 Adjustable Switching Frequency and Synchronization

The ROSC pin can be used to set the switching frequency of the device in two mode. The resistor mode is to connect a resistor between ROSC pin and GND. The switching frequency of the device is adjustable from 200 kHz to 1600 kHz. The other mode called synchronization mode is to connect an external clock signal directly to the ROSC pin. The device is synchronized to the external clock frequency with PLL.

Synchronization mode overrides the resistor mode. The device is able to detect the proper mode automatically and switch from synchronization mode to resistor mode.

Feature Description (continued)

8.3.2.1 Synchronization

An internal phase locked loop (PLL) has been implemented to allow synchronization between 200 kHz and 1600 kHz, and to easily switch from Resistor mode to Synchronization mode.

To implement the synchronization feature, connect a square wave clock signal to the ROSC pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2 V. The start of the switching cycle is synchronized to the falling edge of ROSC pin.

In applications where both Resistor mode and Synchronization mode are needed, the device can be configured as shown in Figure 17. Before the external clock is present, the device works in Resistor mode and the switching frequency is set by ROSC resistor. When the external clock is present, the Synchronization mode overrides the Resistor mode. The first time the ROSC pin is pulled above the ROSC high threshold (2 V), the device switches from the Resistor mode to the Synchronization mode and the ROSC pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from the Synchronization mode back to the Resistor mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by ROSC resistor.

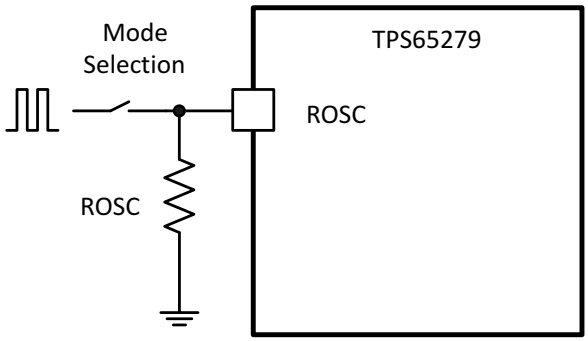


Figure 17. Resistor Mode and Synchronization Mode

8.3.3 Soft-Start Time

The start-up of buck output is controlled by the voltage on the respective SS pin. When the voltage on the SS pin is less than the internal 0.6-V reference, the TPS65279 regulates the internal feedback voltage to the voltage on the SS pin instead of 0.6 V. The SS pin can be used to program an external soft-start function or to allow output of buck to track another supply during start-up. The device has an internal pullup current source of 6 µA that charges an external soft-start capacitor to provide a linear ramping voltage at SS pin. The TPS65279 regulates the internal feedback voltage according to the voltage on the SS pin, allowing VOUT to rise smoothly from 0 V to its final regulated voltage. The total soft-start time will be calculated approximately:

$$t_{SS}(ms) = Css(nF) \times \left(\frac{0.6\ V}{6\ \mu A} \right) \quad (1)$$

8.3.4 Out-of-Phase Operation

In order to reduce input ripple current, Buck 1 and Buck 2 operate 180° out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

8.3.5 Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications

Feature Description (continued)

with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

8.3.6 Bootstrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and LX pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-LX voltage is below regulation. The value of this ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT to LX pin voltage is greater than the BOOT-LX UVLO threshold which is typically 2.1 V. When the voltage between BOOT and LX drops below the BOOT-LX UVLO threshold the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split input voltage rails, 100% duty cycle operation can be achieved as long as (VIN – PVIN) > 4 V.

8.3.7 Overcurrent Protection

The device is protected from over current conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

8.3.7.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle by cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off.

TPS65279 features adjustable overcurrent protection trip point. The peak current limit can be set by external resistors connected between pin RLIM1/2 to ground. By setting lower current limit, lower current rating inductor can be used to reduce system cost.

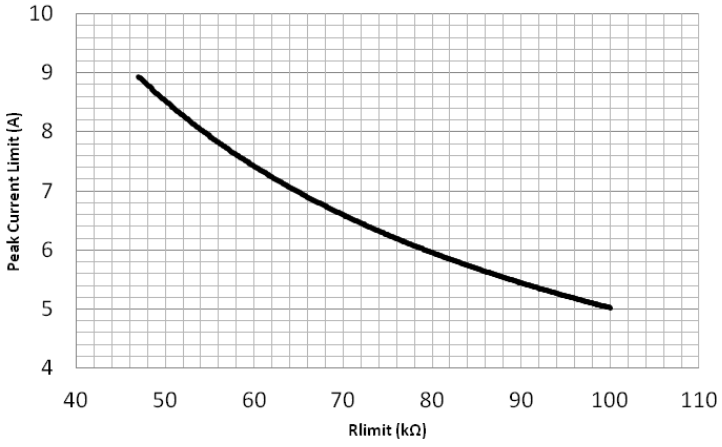


Figure 18. Peak Current Limit vs R_{limit}

$$Ilim\ (A) = 168.98 \times Rlimit\ (k\Omega)^{-0.763} \quad (2)$$

Feature Description (continued)

8.3.7.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the device will shut down itself and restart after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions. When one channel is in OCP, the other channel is not impacted and remains independent.

8.3.8 Current Sharing Operation

As TPS65279 uses peak current mode control method, the two buck converters can be paralleled together to provide large current. Paralleling two bucks provides some advantages over single buck operation, such as smaller input and output ripple, faster response in load transient, and so forth. The converters will work in current sharing mode by connecting the iShare pin to high. Once in current mode, signal pins in Buck 2 are not active, for example, FB2, COMP2, SS2, these pins will be neglected. Connecting FB2 to GND and floating COMP2, SS2, PGOOD2 are recommended.

8.3.9 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. Once the junction temperature drops below 140°C typically, the internal thermal hiccup timer will start to count. The device reinitiates the power up sequence after the built-in thermal shutdown hiccup time (16384 cycles) is over.

8.4 Device Functional Modes

8.4.1 CCM Operation Mode

When the VIN/PVINx are above UVLO threshold and ENx are above the threshold, two switchers operate in continuous current mode(CCM) when MODE pin connects to GND. In CCM, the converters work in peak current mode for easy loop compensation and cycle-by-cycle high side MOSFET current limit.

8.4.2 PSM Operation Mode

When connect MODE pin to V7V, PSM mode is enabled. The devices are designed to operate in high-efficiency PSM under light load conditions. Pulse skipping is initiated when the switch current falls to 0 A. During pulse skipping, the low-side FET is turned off when the switch current falls to 0 A. The switching node (LX) waveform takes on the characteristics of DCM operation and the apparent switching frequency decreases.

8.4.3 Current Sharing Mode

When ISHARE pin connects to high, SW1/SW2 pair output are shared, the responding pairs current sharing mode is enabled and the two buck converters are paralleled together to provide large current. For the detail configuration, see current sharing application schematics.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The devices are step-down DC-DC converters. They are typically used to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 5/5 A. The following design procedure can be used to select component values for the TPS65279. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

9.2 Typical Applications

9.2.1 Dual Buck Operation Mode Application

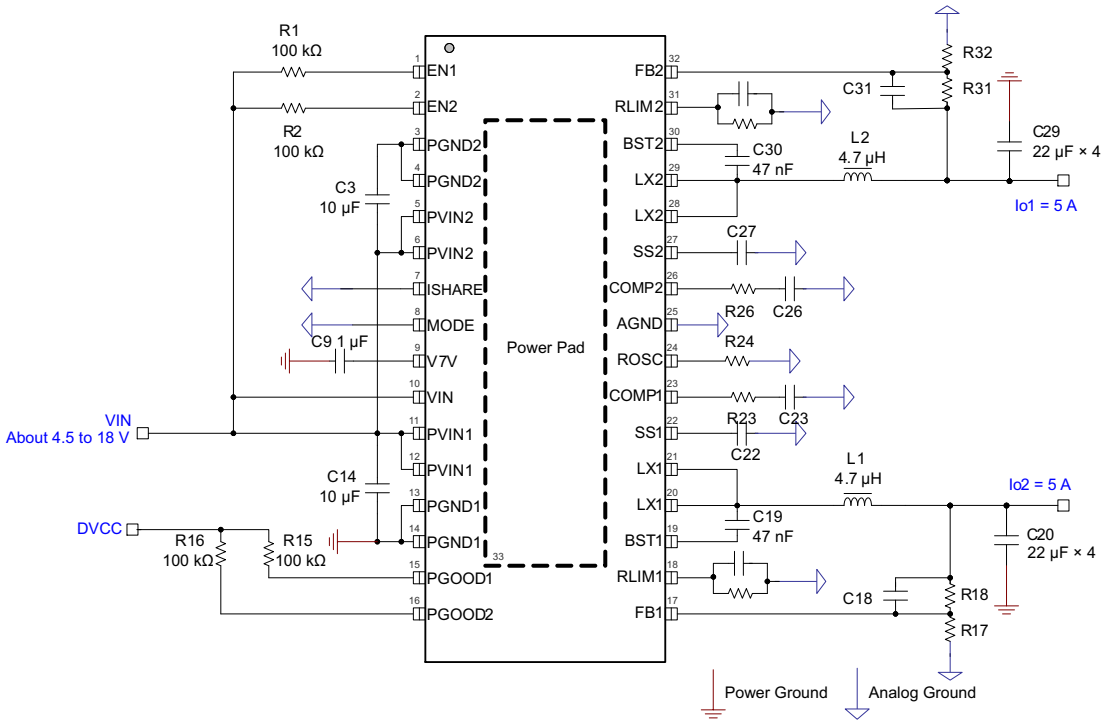


Figure 19. Dual Mode Operation to Deliver 5 A at Buck1 and 5 A at Buck2

Typical Applications (continued)

9.2.1.1 Design Requirements

For this design example, use the following in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 18 V
Output voltage	1.2 V/1.8 V
Transient response, 1.5-A load step	ΔVout = ±5%
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	5 A
Operating frequency	600 kHz

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node (VOUT) to the FB pin. TI recommends to use 1% tolerance or better divider resistors.

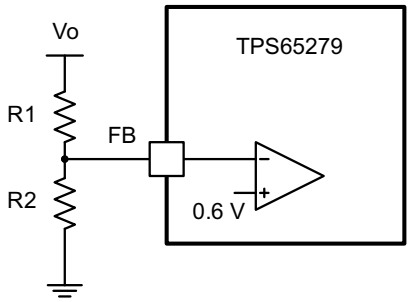


Figure 20. Voltage Divider Circuit

$$R2 = R1 \times \left(\frac{0.6\ V}{V_{OUT} - 0.6\ V} \right) \quad (3)$$

Start with a 40.2-kΩ for R1 and use Equation 3 to calculate R2. To improve efficiency at light loads consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

The minimum output voltage and maximum output voltage can be limited by the minimum on time of the high-side MOSFET and bootstrap voltage (BOOT-LX voltage) respectively. See *Bootstrap Voltage (BOOT) and Low Dropout Operation* for more information.

9.2.1.2.2 Adjusting UVLO

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN, in split rail applications, then the EN pin can be configured as shown in Figure 21.

When using the external UVLO function, TI recommends to set the hysteresis to >500 mV.

The EN pin has a small pullup current I_P which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function since it increases by Ih once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 4 and Equation 5.

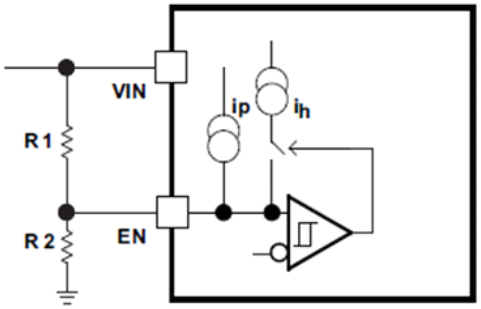


Figure 21. Adjustable VIN UVLO

$$R_1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (4)$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1(I_h + I_p)}$$

where

- I_h = 3 µA
- I_P = 3 µA
- $V_{ENRISING}$ = 1.21 V
- $V_{ENFALLING}$ = 1.17 V (5)

9.2.1.2.3 Adjustable Switching Frequency (Resistor Mode)

To determine the ROSC resistance for a given switching frequency, use Equation 6 or the curve in Figure 22. To reduce the solution size one would set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on time should be considered.

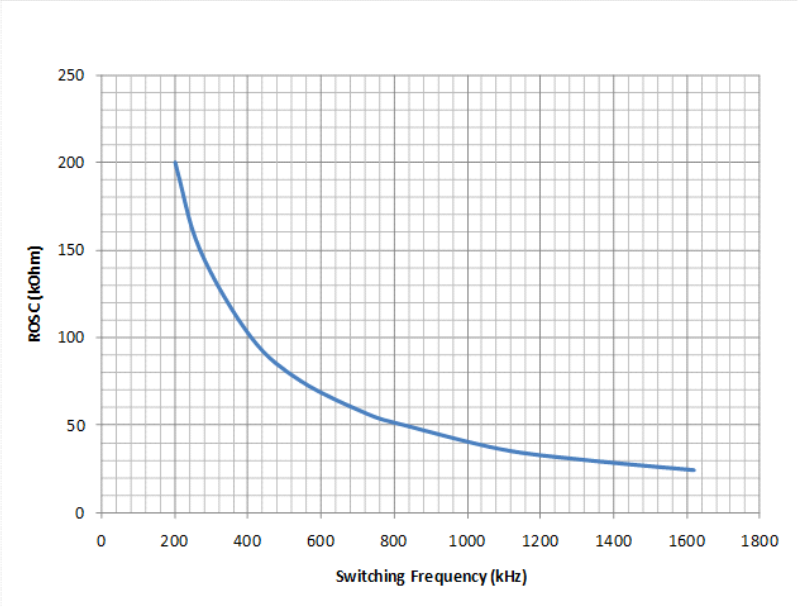


Figure 22. ROSC vs Switching Frequency

$$R_{osc}(k\Omega) = 45580 \times f_{sw}^{-1.019}(kHz) \quad (6)$$

9.2.1.2.4 Output Inductor Selection

To calculate the value of the output inductor, use Equation 7. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{inmax} - V_{out}}{I_o \times LIR} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \quad (7)$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 9 and Equation 10.

$$I_{ripple} = \frac{V_{inmax} - V_{out}}{L} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \quad (8)$$

$$I_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{out} \times (V_{inmax} - V_{out})}{V_{inmax} \times L \times f_{SW}}\right)^2}{12}} \quad (9)$$

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2} \quad (10)$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

9.2.1.2.5 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 11 shows the minimum output capacitance necessary to accomplish this.

$$C_o = \frac{2 \times \Delta I_{out}}{f_{sw} \times \Delta V_{out}} \quad (11)$$

where

- ΔI_{OUT} is the change in output current.
- f_{SW} is the regulators switching frequency.
- ΔV_{OUT} is the allowable change in the output voltage.

For this example, the transient load response is specified as a 5% change in V_{OUT} for a load step of 3 A. For this example, ΔI_{OUT} = 3 A and ΔV_{OUT} = 0.05 x 3.3 = 0.165 V. Using these numbers gives a minimum capacitance of 75.8 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 12 calculates the minimum output capacitance needed to meet the output voltage ripple specification.

$$C_o > \frac{1}{8 \times f_{sw}} \times \frac{1}{\frac{V_{oripple}}{I_{oripple}}}$$

where

- f_{sw} is the switching frequency.
- $V_{oripple}$ is the maximum allowable output voltage ripple.
- $I_{oripple}$ is the inductor ripple current. (12)

Equation 13 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{oripple}}{I_{oripple}} \quad (13)$$

Additional capacitance deratings for aging, temperature, and DC bias should be factored in which increases this minimum value.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 14 can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{corms} = \frac{V_{out} \times (V_{inmax} - V_{out})}{\sqrt{12} \times V_{inmax} \times L \times f_{sw}} \quad (14)$$

9.2.1.2.6 Input Capacitor Selection

The TPS65279 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10-µF of effective capacitance on the PVIN input voltage pins. In some applications additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS65279. The input ripple current can be calculated using Equation 15.

$$I_{inrms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{inmin}} \times \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \quad (15)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. TPS65279 may operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 16.

$$\Delta V_{in} = \frac{I_{outmax} \times 0.25}{C_{in} \times f_{sw}} \quad (16)$$

9.2.1.2.7 Loop Compensation

Integrated buck DC/DC converter in TPS65279 incorporates a peak current mode control scheme. The error amplifier is a transconductance amplifier with a gain of 1350 µA/V. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. C_b adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow the following steps.

1. Select switching frequency f_{sw} that is appropriate for application depending on L and C sizes, output ripple, EMI, and etc. Switching frequency between 500 kHz to 1 MHz gives best trade off between performance and cost. To optimize efficiency, lower switching frequency is desired.

2. Set up cross over frequency, f_c, which is typically between 1/5 and 1/20 of f_{sw}.
3. R_C can be determined by:

$$R_C = \frac{2\pi \times f_c \times V_O \times C_O}{g_M \times Vref \times gm_{ps}}$$

where

- g_M is the error amplifier gain (1350 µA/V).
- gm_{ps} is the power stage voltage to current conversion gain (10 A/V).

4. Calculate C_C by placing a compensation zero at or before the dominant pole:

$$(f_P = \frac{1}{C_O \times R_L \times 2\pi}) \quad (17)$$

$$C_C = \frac{R_L \times Co}{R_C} \quad (18)$$

5. Optional C_b can be used to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{R_{ESR} \times Co}{R_C} \quad (19)$$

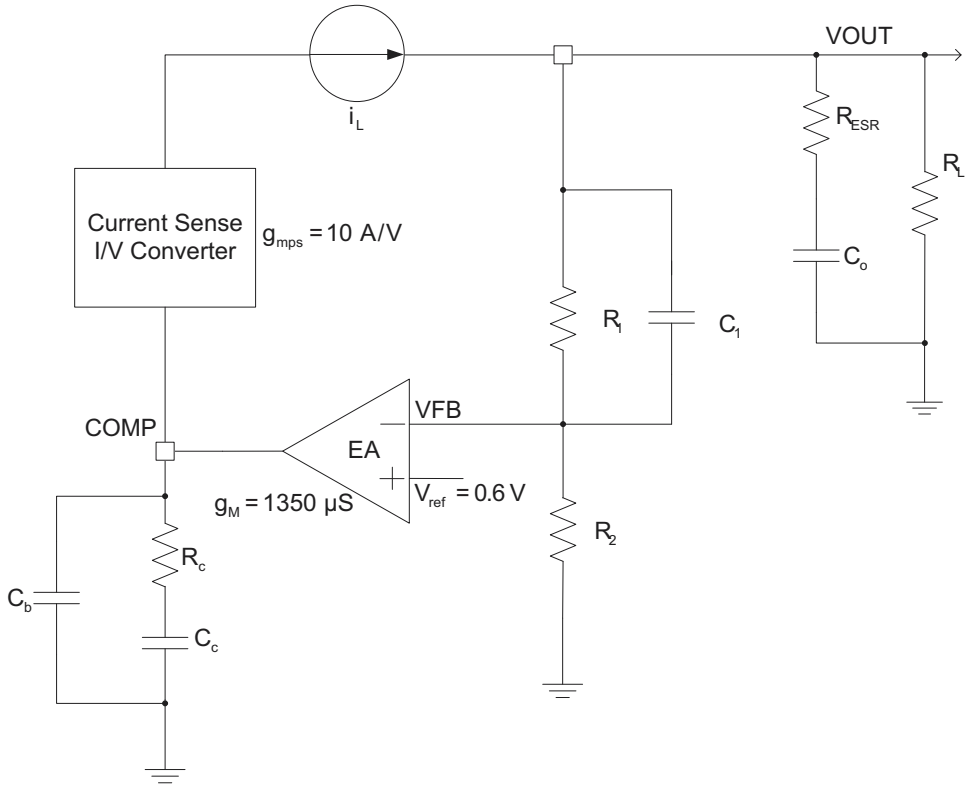


Figure 23. DC/DC Loop Compensation

9.2.1.3 Application Curves

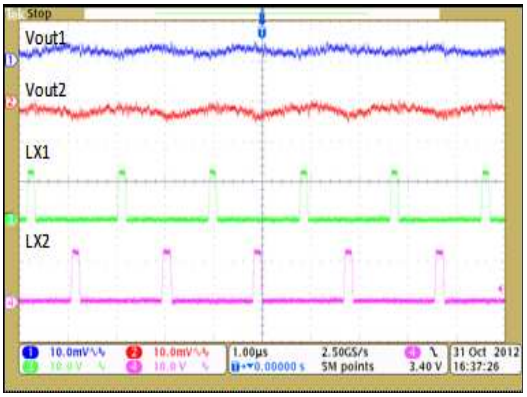


Figure 24. Output Ripple at 0 A, Forced PWM

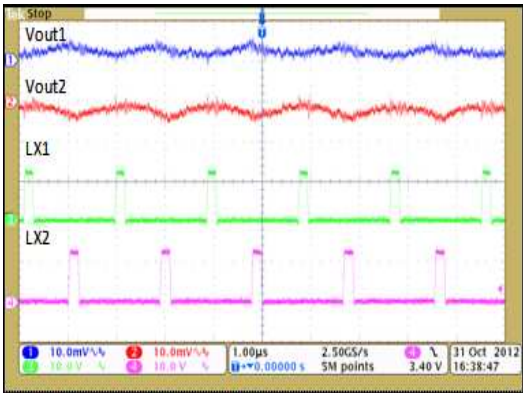


Figure 25. Output Ripple at 3.5 A, Forced PWM

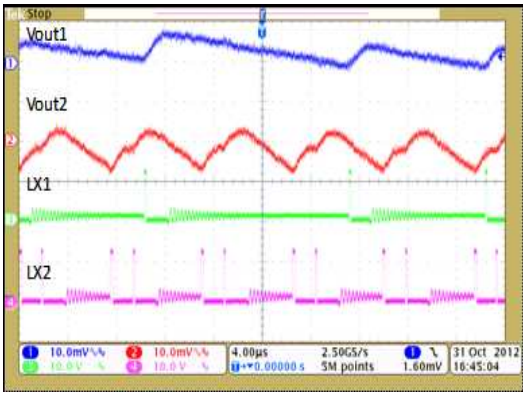


Figure 26. Output Ripple, Buck1 at 0.05 A, Buck2 at 0.2 A Auto PSM-PWM Mode

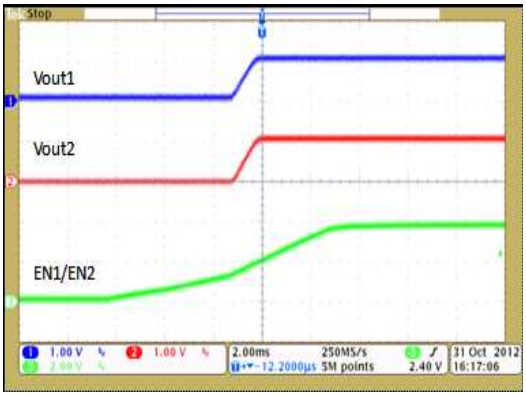


Figure 27. Startup With Enable

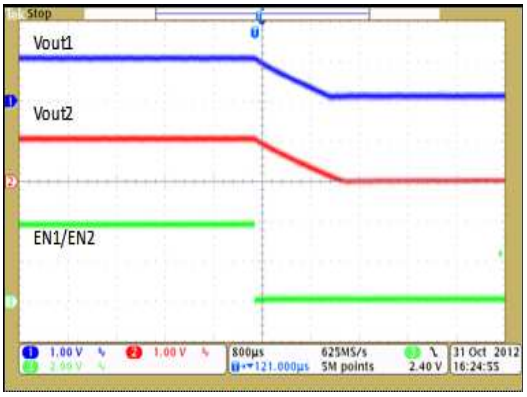


Figure 28. Shutdown With Enable

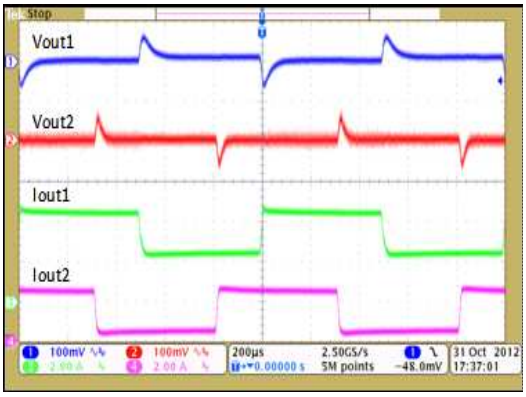


Figure 29. Load Transient, Buck1 2.5 A - 4.5 A, Buck2 0.5 A - 2.5 A

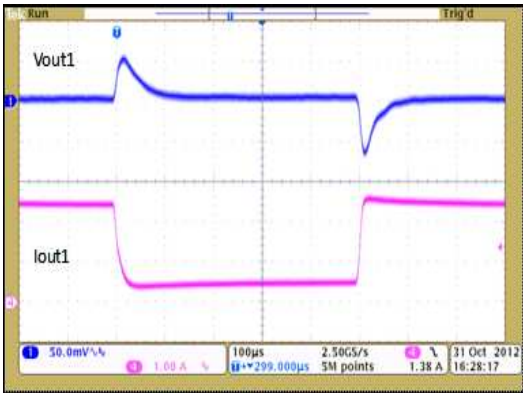


Figure 30. Load Transient, Buck1 (0.5 A - 2.5 A)

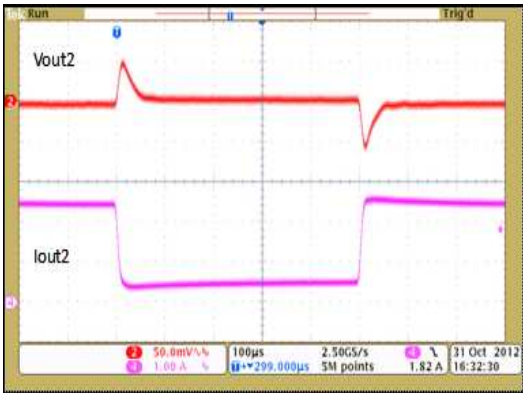


Figure 31. Load Transient, Buck2 (0.5 A - 2.5 A)

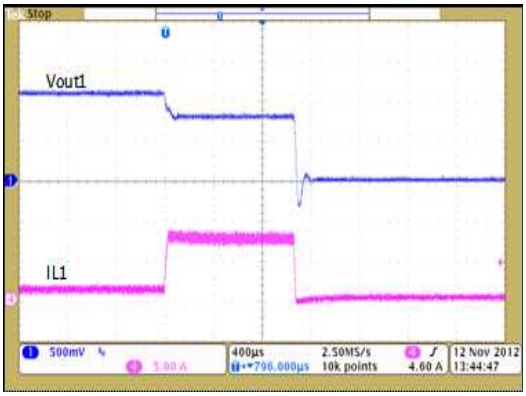


Figure 32. Overcurrent Protection Buck1

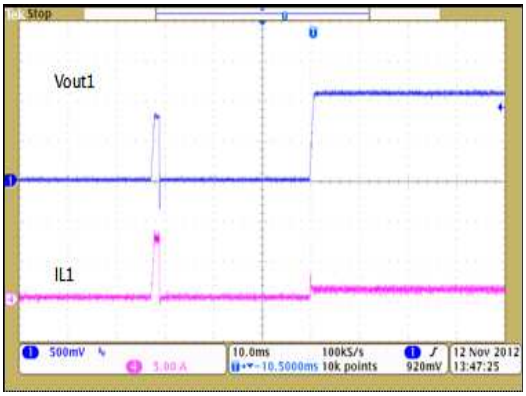


Figure 33. Hiccup Recover, Buck1

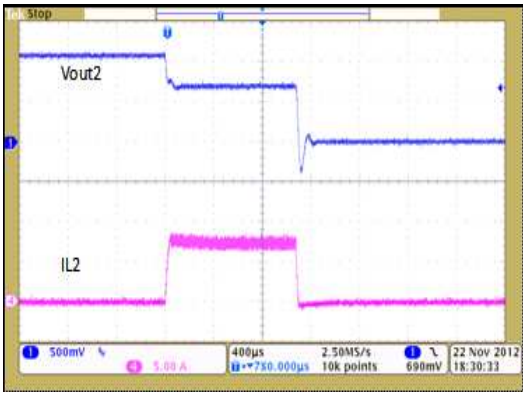


Figure 34. Overcurrent Protection, Buck2

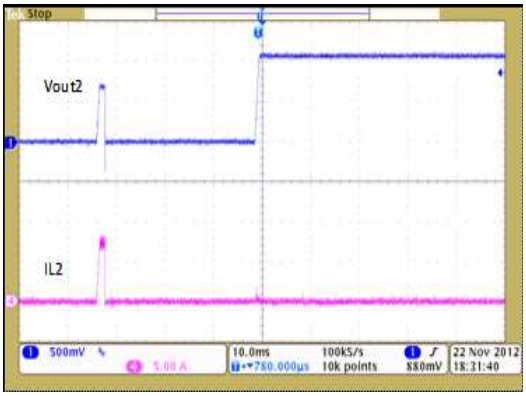


Figure 35. Hiccup Recover, Buck2

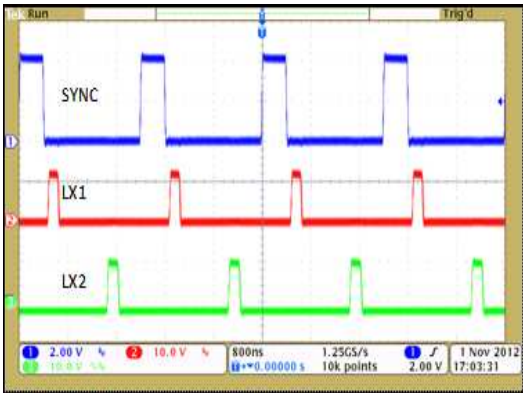


Figure 36. Synchronization at 500 kHz

9.2.2 Current Sharing Mode Operation Application

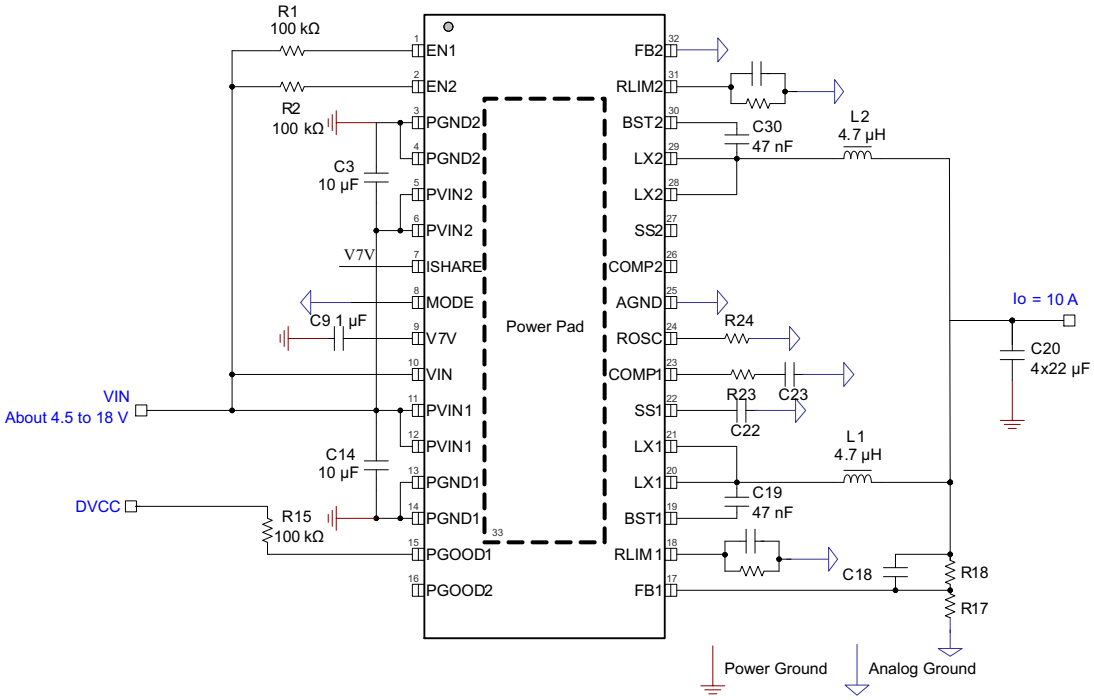


Figure 37. Share Mode Operation to Deliver 10 A

9.2.2.1 Design Requirements

See previous *Design Requirements*.

9.2.2.2 Detailed Design Procedure

As TPS65279 utilizes peak current mode control method, the two buck converters can be paralleled together to provide large current. The converters will work in current sharing mode by connecting the iShare pin to high. Once in current mode, signal pins in Buck 2 are not active, for example, FB2, COMP2, SS2, these pins will be neglected. Connecting FB2 to GND and floating COMP2, SS2, PGOOD2 are recommended.

For other component selection, refer to previous *Detailed Design Procedure*.

9.2.2.3 Application Curves

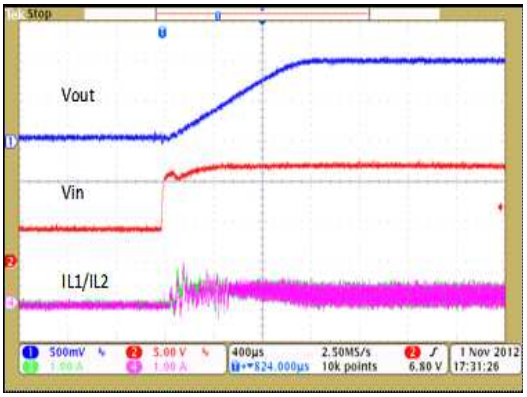


Figure 38. Current Share Mode Startup

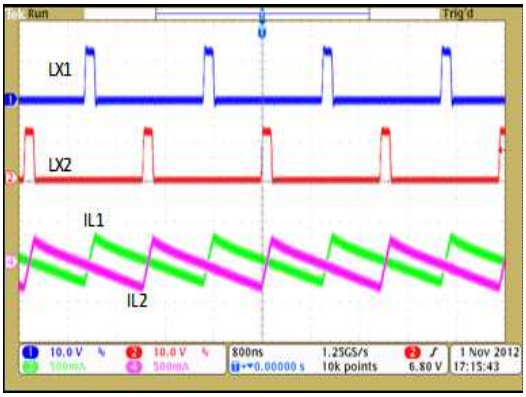


Figure 39. Steady State of Current Share Mode Operation (I_O = 0 A)

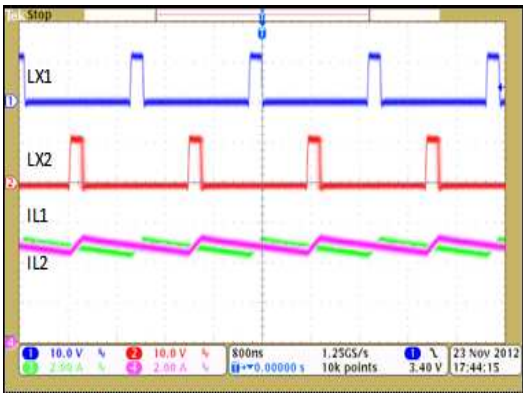


Figure 40. Steady State of Current Share Mode Operation (I_O = 10 A)

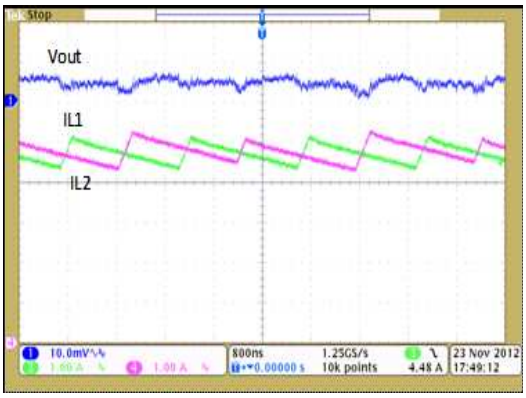


Figure 41. Output Ripple, Current Share Mode Operation (I_O = 10 A)

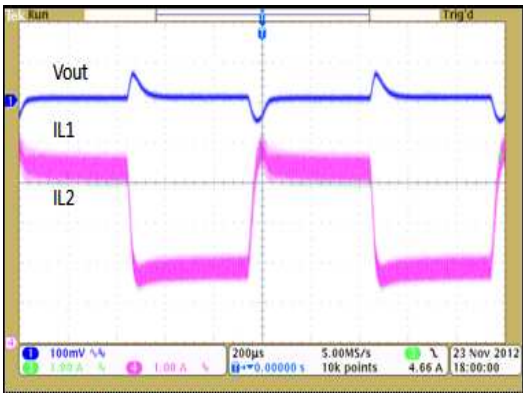


Figure 42. Load Transient, Current Share Mode Operation (I_O = 4 A - 9 A)

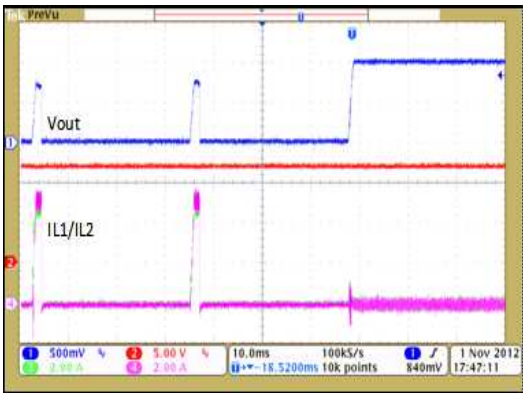


Figure 43. Hiccup Recover, Current Share Mode

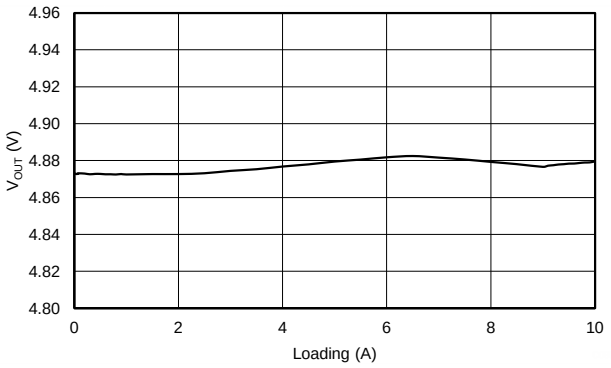


Figure 44. Current Share Mode, 5-V Load Regulation

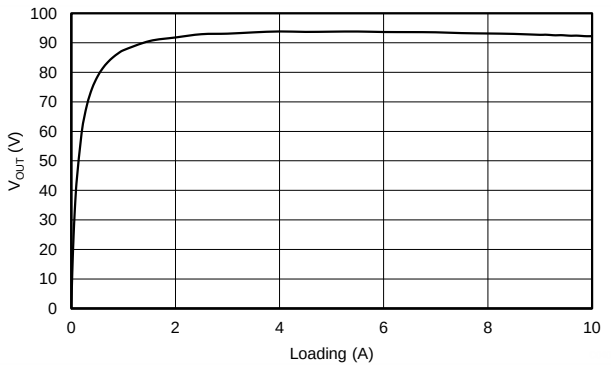


Figure 45. Current Share Mode, 5-V Load Efficiency

10 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 4.5 and 18 V. This input power supply should be well regulated. If the input supply is located more than a few inches from the TPS65400 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 22 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

The designer can layout the TPS65279 on a 2-layer PCB as shown in Figure 46.

Layout is a critical portion of good power supply design. See Figure 46 for a PCB layout example. The top layer contains the main power traces for VIN, VOUT, and VLX. Also on the top layer are connections for the remaining pins of the TPS65279 and a large top side area filled with ground. The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65279 device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as ground plane connecting analog ground and power ground.

The GND pin should be tied directly to the power pad under the IC and the power pad. For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.

The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.

Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The additional external components can be placed approximately as shown.

11.2 Layout Example

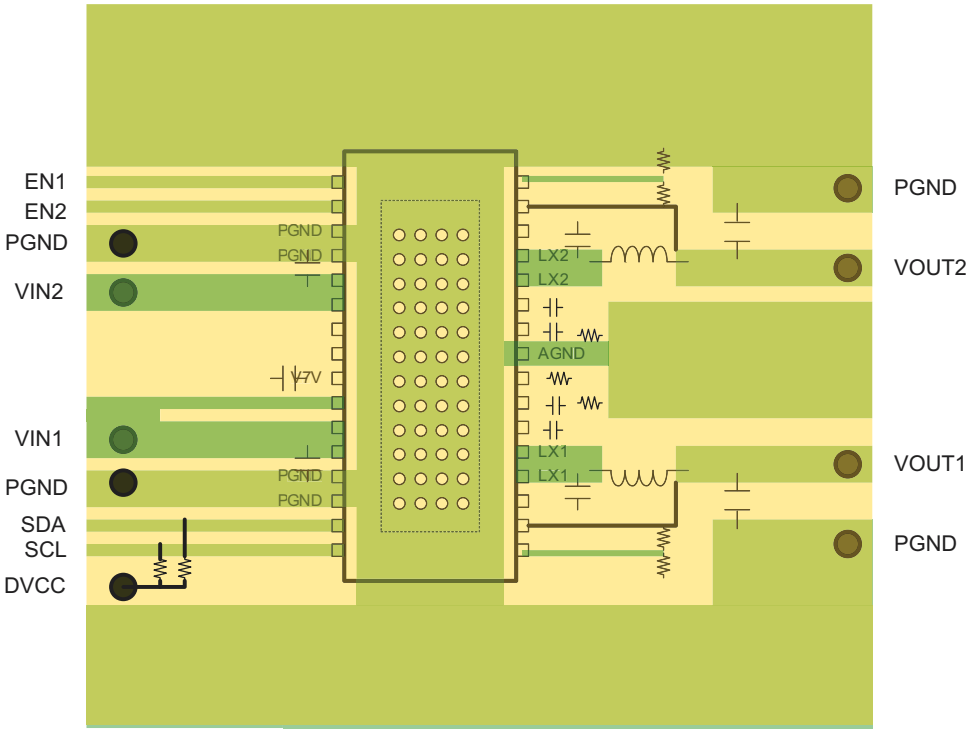


Figure 46. TPS65279 Layout on 2-Layer PCB

12 器件和文档支持

12.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65279DAP	ACTIVE	HTSSOP	DAP	32	46	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		TPS65279	Samples
TPS65279DAPR	ACTIVE	HTSSOP	DAP	32	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS65279	Samples
TPS65279RHHR	ACTIVE	VQFN	RHH	36	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65279	Samples
TPS65279RHHT	ACTIVE	VQFN	RHH	36	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 65279	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

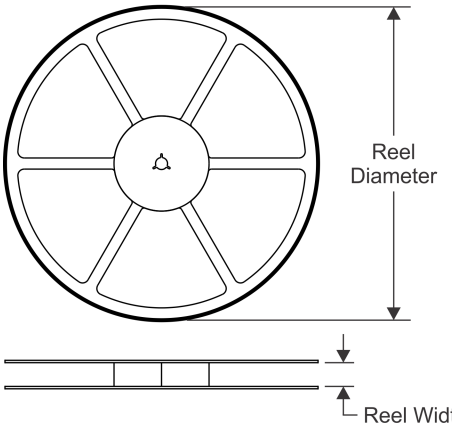
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

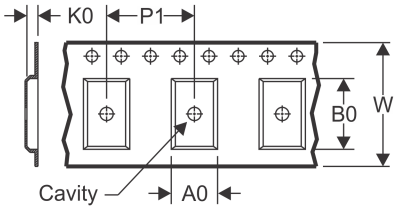
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

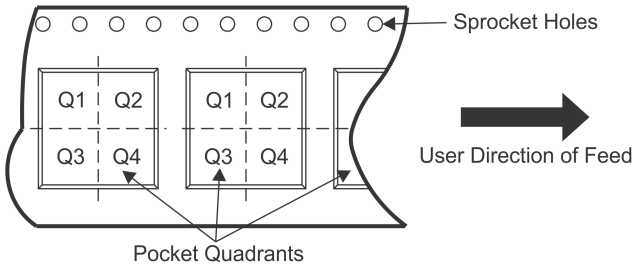


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

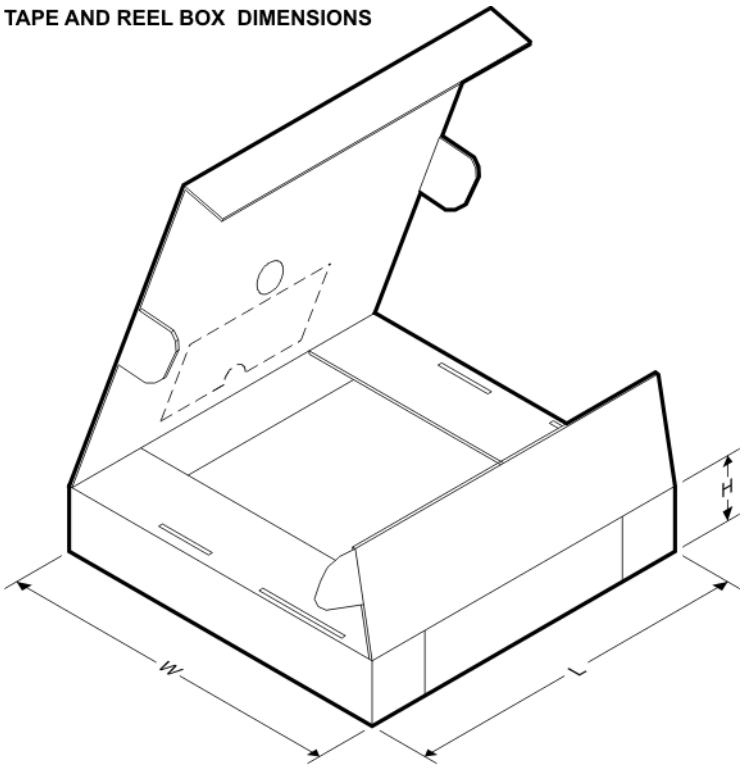
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65279DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TPS65279RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65279RHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

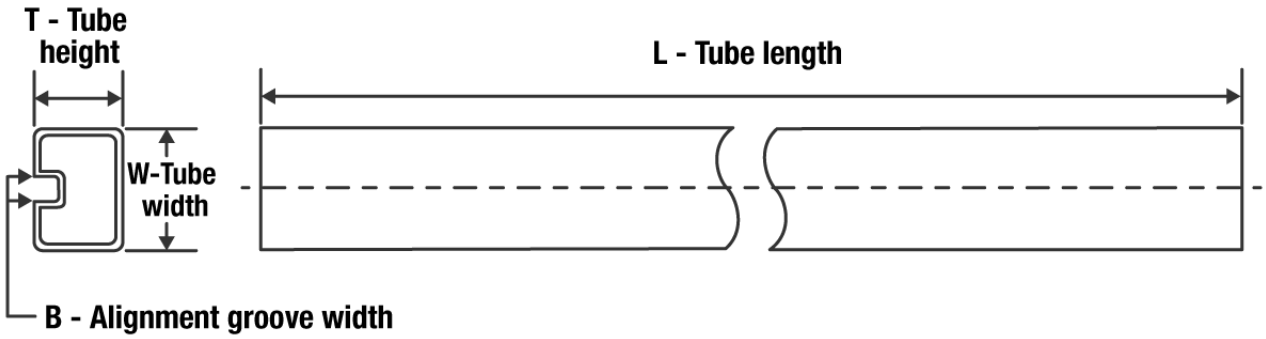
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65279DAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0
TPS65279RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
TPS65279RHHT	VQFN	RHH	36	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS65279DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

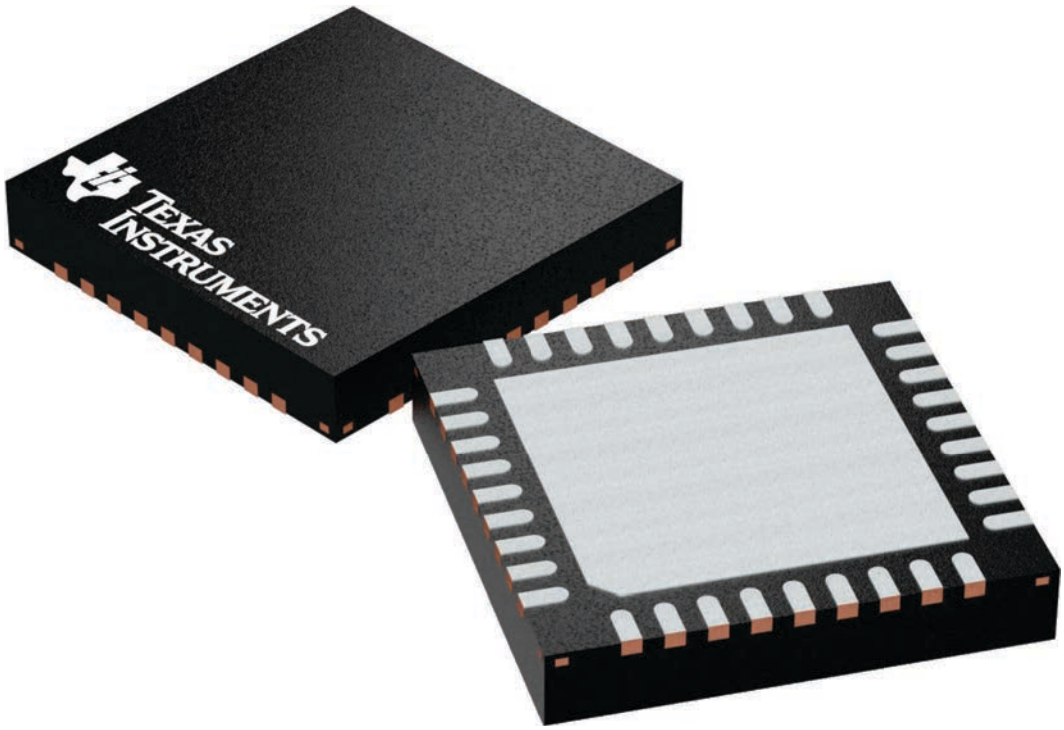
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



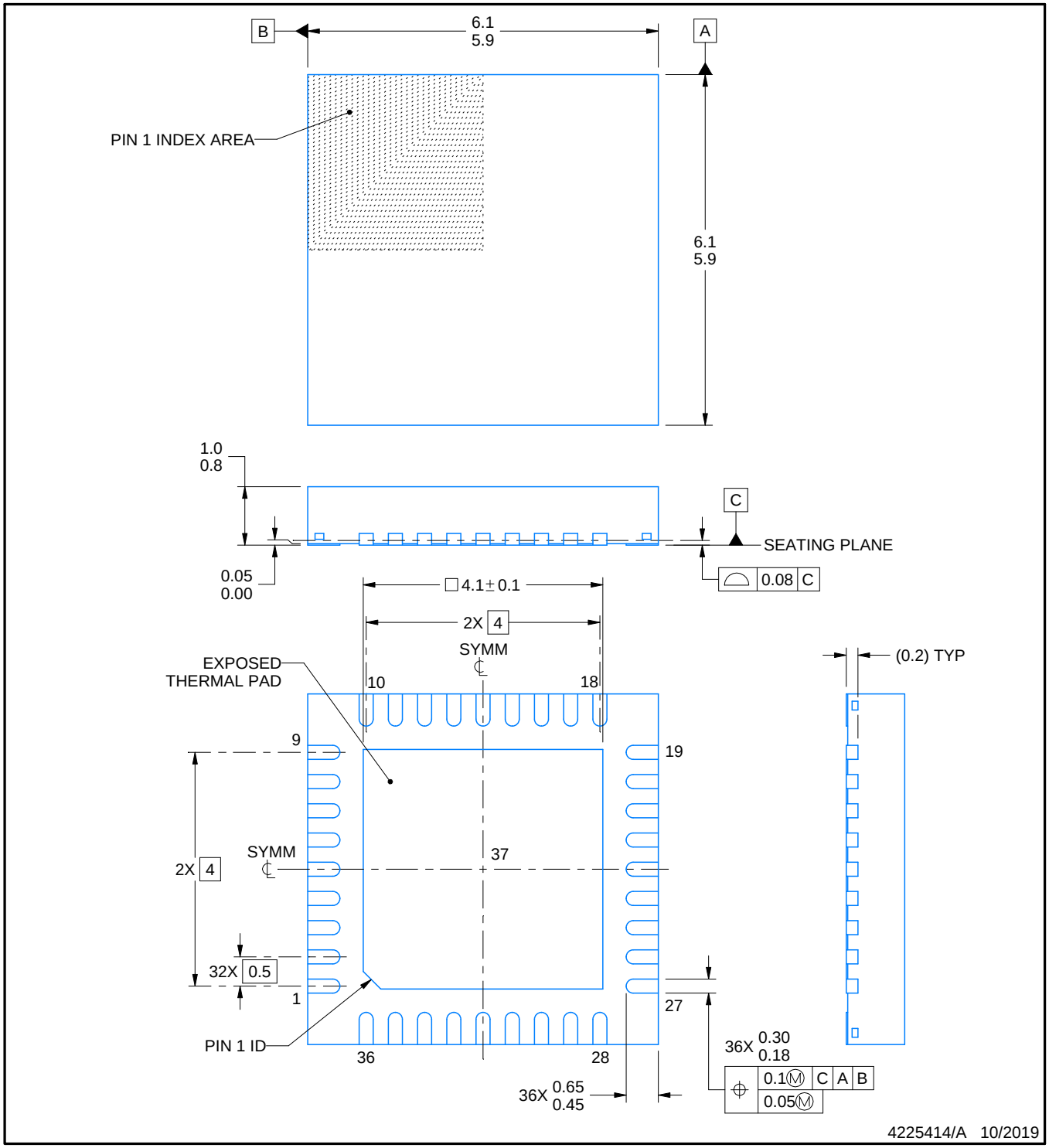
4225440/A

RHH0036B

PACKAGE OUTLINE

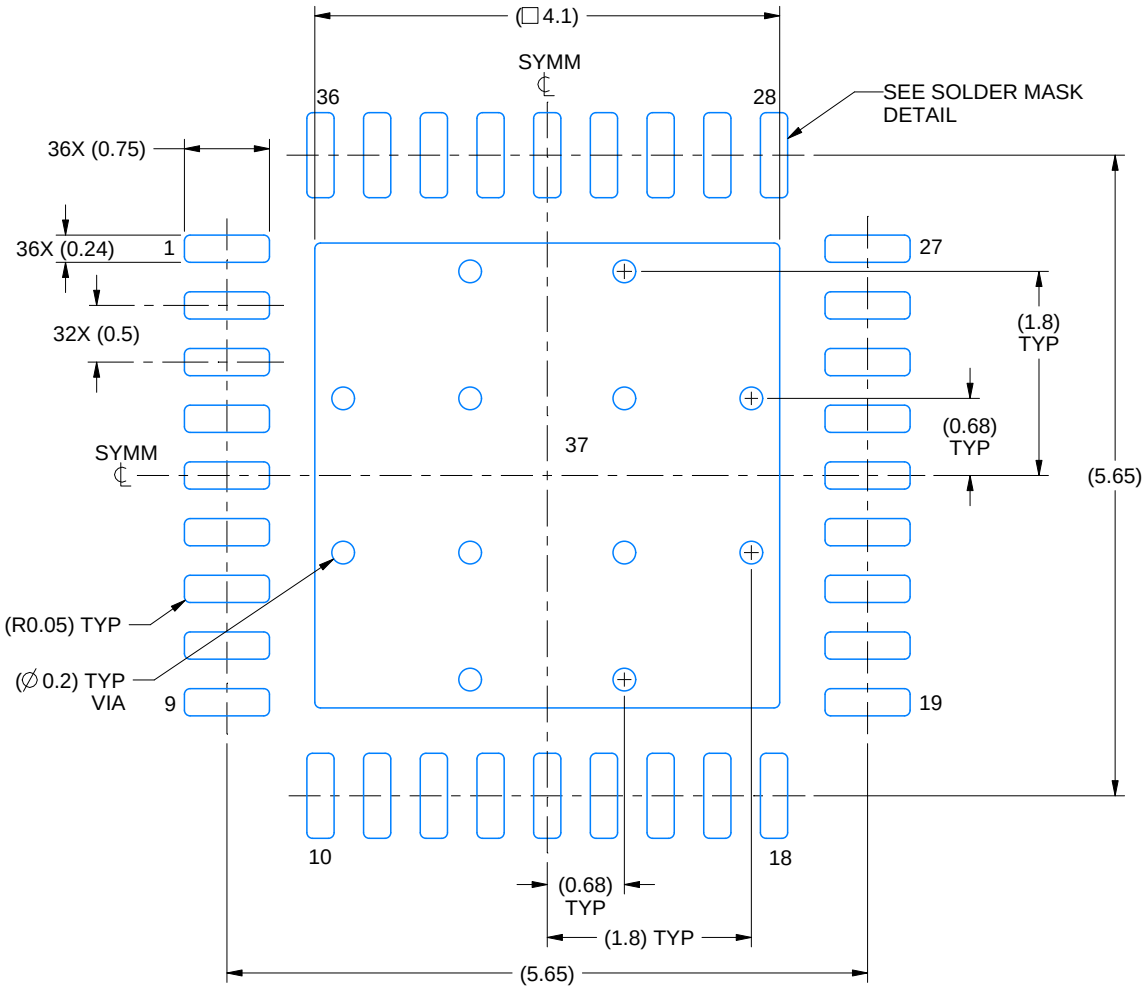
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

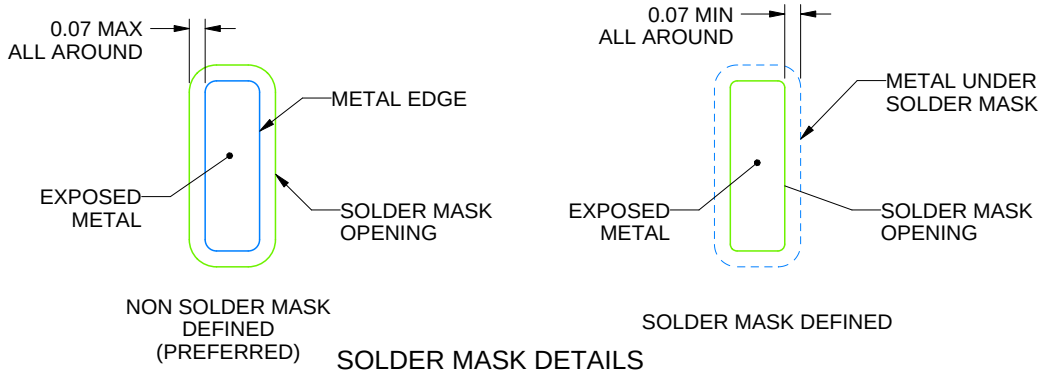


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

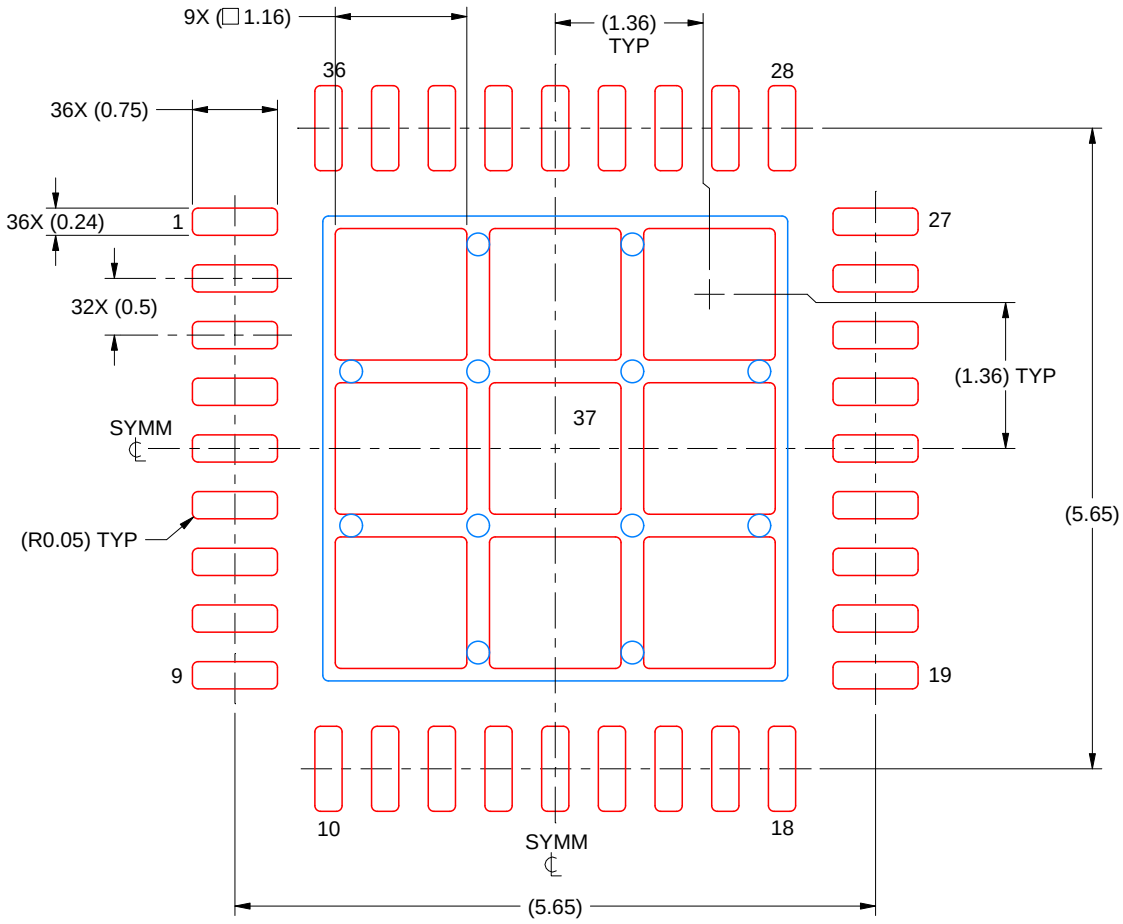


SOLDER MASK DETAILS

4225414/A 10/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225414/A 10/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

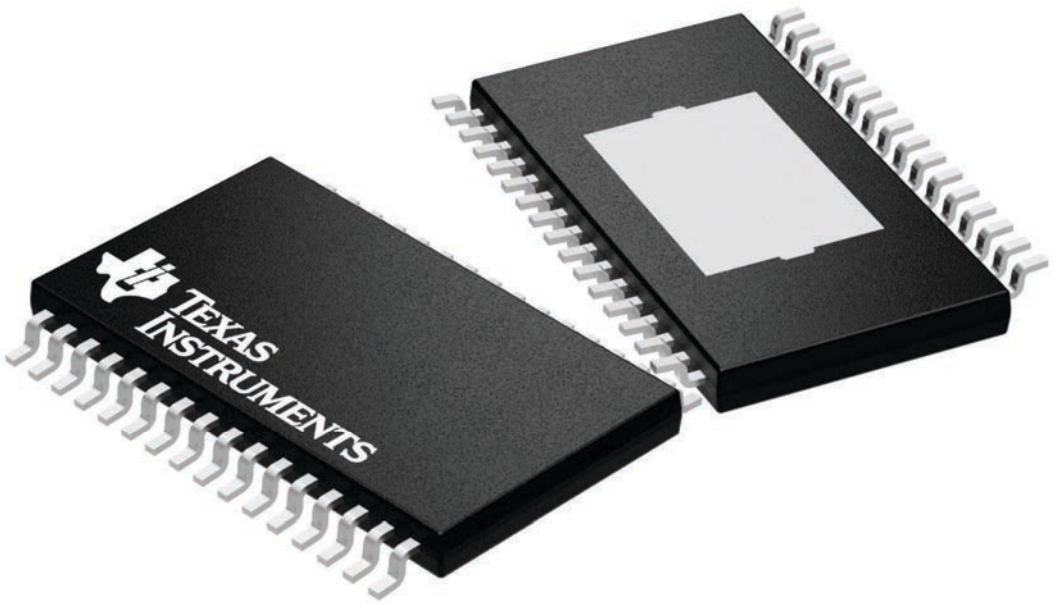
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

8.1 x 11, 0.65 mm pitch

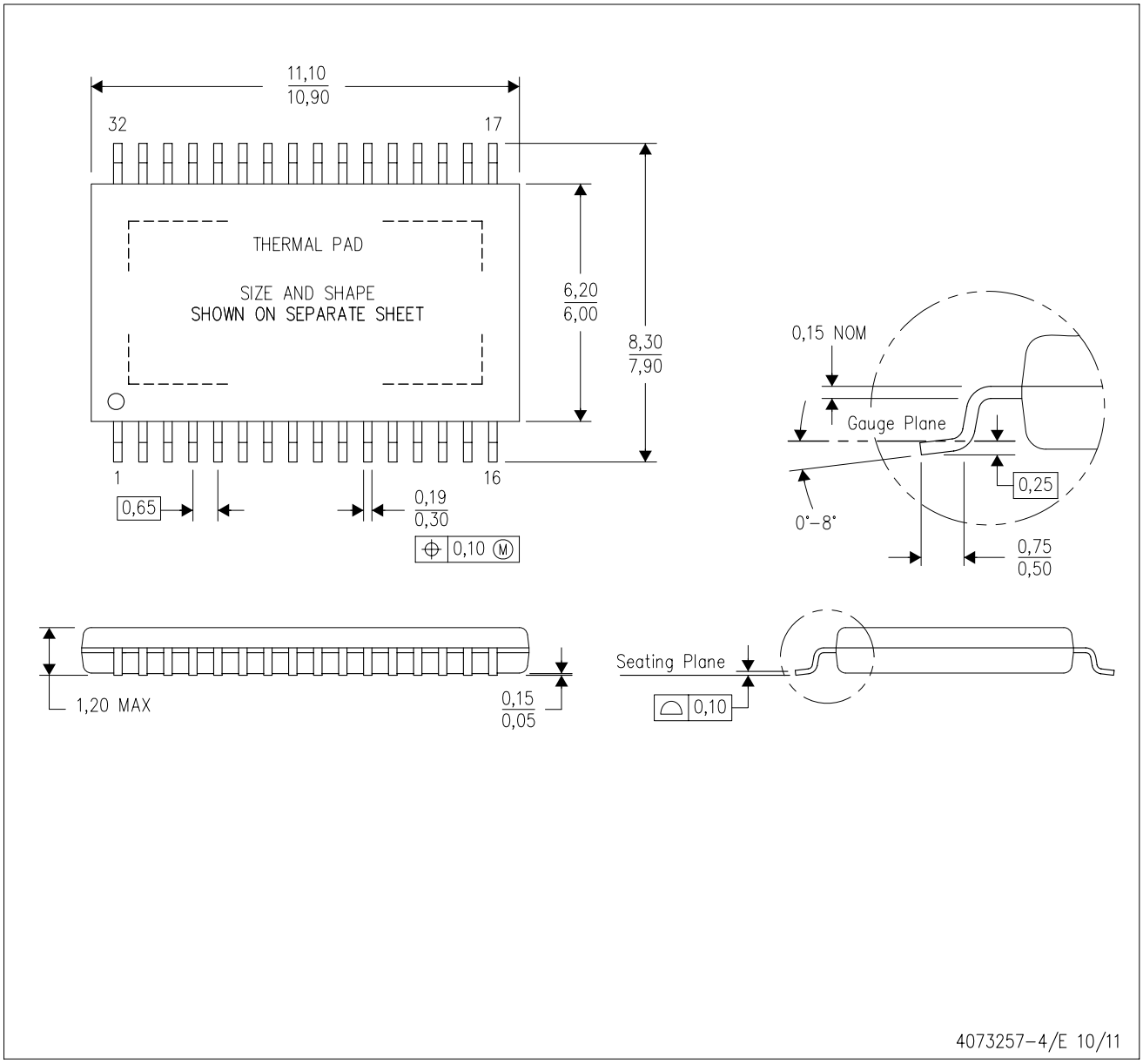
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

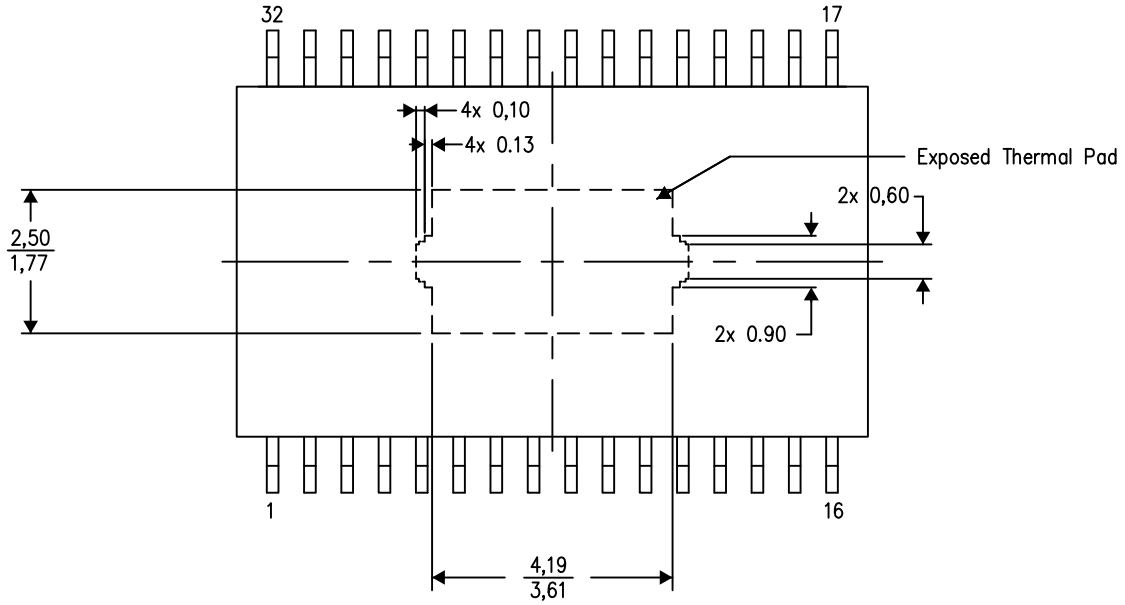
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206319–10/M 09/13

NOTE: All linear dimensions are in millimeters

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265