TLC555 LinCMOS™ 计时器

1 特性

- 极低功耗：
  - V_{DD} = 5V 时为 1mW（典型值）
- 能够在非稳态模式下正常工作
- 支持轨到轨摆动的 CMOS 输出
- 高输出电流能力
  - 灌电流：100mA（典型值）
  - 拉电流：10mA（典型值）
- 输出与 CMOS、TTL 和 MOS 完全兼容
- 低电源电流在输出转换期间降低了尖峰
- 2V 至 15V 单电源运行
- 在功能上可与 NE555 互换；具有相同的引脚
- ESD 保护超过 MIL-STD-883C 方法 3015.2 规定的 2000V
- 可用于 Q 级温度汽车
  - 高可靠性汽车 应用
  - 配置控制和打印支持
  - 通过汽车标准认证

2 应用

- 精确计时
- 脉冲发生
- 顺序计时
- 延时时间生成
- 脉宽调制
- 脉冲位置调制
- 线性斜坡发生器

3 说明

TLC555 是一款采用 TI LinCMOS™工艺制造的单片计时电路。该计时器与 CMOS、TTL 和 MOS 逻辑器件完全兼容，可在高达 2MHz 的频率下正常工作。由于输入阻抗较高，此器件可支持比 NE555 或 LM555 所支持的计时电容器更小的计时电容器。因此，可实现更加准确的延时时间和振荡。在整个电源电压范围内可保持较低功耗。

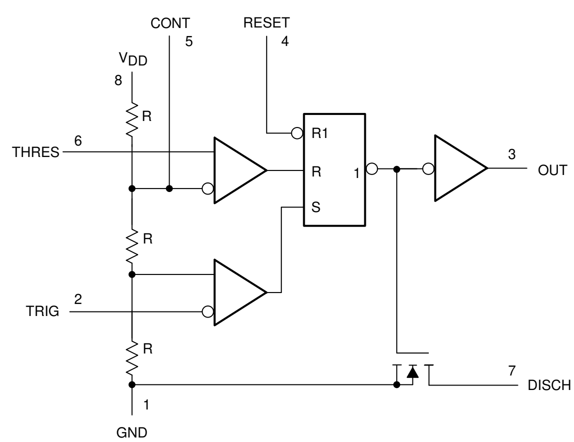
与 NE555 类似，TLC555 有一个约等于电源电压三分之一的触发电平以及一个约等于电源电压三分之二的阈值电平。可使用控制电压端子 (CONT) 来改变这些电平。当触发输入 (TRIG) 下降至低于触发电平的时候，触发器被设定并且输出变为高电平。如果 TRIG 高于触发电平并且阈值输入 (THRES) 在阈值电平之上的话，触发器被复位并且输出为低电平。复位输入 (RESET) 的优先级高于所有其它输入并且可被用来启动一个新的定时周期。如果 RESET 为低电平，触发器被复位并且输出为低电平。只要当输出为低电平，在放电端子 (DISCH) 和接地 (GND) 之间提供一个低阻抗路径。所有未用输入端必须接入合适的逻辑电平以免发生误触发。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLC555C	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.38mm
	SOP (8)	6.20mm × 5.30mm
	TSSOP (14)	5.00mm × 4.40mm
TLC555I	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.38mm
TLC555M	LCCC (20)	8.89mm x 8.89mm
	CDIP (8)	9.60mm × 6.67mm
TLC555Q	SOIC (8)	4.90mm × 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

Changes from Revision H (August 2016) to Revision I **Page**

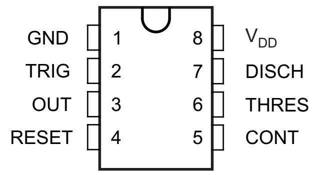
- Added MIN value for input voltage in *Absolute Maximum Ratings* 6
- Added discharge pin in *Absolute Maximum Ratings* 6
- Changed MIN supply voltage based on part number in *Recommended Operating Conditions* 6
- Added power dissipation capacitance TYP value in *Electrical Characteristics: V_{DD} = 2 V for TLC555C, V_{DD} = 3 V for TLC555I* 7
- Added trigger, threshold capacitance TYP value in *Electrical Characteristics: V_{DD} = 5 V* 8
- Changed V_{OH} test condition current to –1 mA in *Electrical Characteristics: V_{DD} = 5 V* 8
- Added power dissipation capacitance TYP value in *Electrical Characteristics: V_{DD} = 5 V* 9
- Added trigger, threshold capacitance TYP value in *Electrical Characteristics: V_{DD} = 15 V* 9
- Added power dissipation capacitance TYP value in *Electrical Characteristics: V_{DD} = 15 V* 10
- Added *Operating Characteristics* to the *Specifications* section 11
- Added Supply Current vs Supply Voltage chart to the *Typical Characteristics* section 12
- Added Control Impedance vs Temperature chart to the *Typical Characteristics* section 12
- Added Output Low Resistance vs Temperature chart to the *Typical Characteristics* section 12
- Added Output High Resistance vs Temperature chart to the *Typical Characteristics* section 12
- Added Propagation Delay vs Control Voltage chart, V_{DD} = 2 V to the *Typical Characteristics* section 12
- Added Propagation Delay vs Control Voltage chart, V_{DD} = 5 V to the *Typical Characteristics* section 12
- Changed trigger high hold time to 1 µs in the *Monostable Operation* section 15
- Changed minimum monostable pulse width to 1 µs in the *Monostable Operation* section 15
- Changed Output Pulse Duration vs Capacitance chart scale down to 0.001 ms in the *Monostable Operation* section 15
- Added more astable frequency formulas to the *Astable Operation* section 17
- Changed scale on Free-Running Frequency vs Timing Capacitance chart up to 2 MHz in the *Astable Operation* section 18
- Added CONT pin table note to the Function Table in the *Device Functional Modes* section 19
- Changed the application curve chart in the *Pulse-Width Modulation* section 22
- Changed the application curve charts in the *Pulse-Position Modulation* section 23
- Added clamping diodes to Sequential Timer Circuit in the *Sequential Timer* section 24
- Added *Designing for Improved ESD Performance* section to the *Application Information* section 25

修订历史记录 (接下页)

Changes from Revision G (November 2008) to Revision H	Page
• 已添加 *特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• Changed values in the *Thermal Information* table to align with JEDEC standards	6
• Deleted *Dissipation Ratings* table	6

5 Pin Configuration and Functions

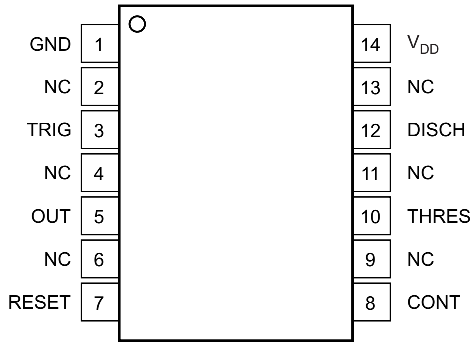
D, P, PS, and JG Packages
8-Pin SOIC, PDIP, SOP, CDIP
Top View



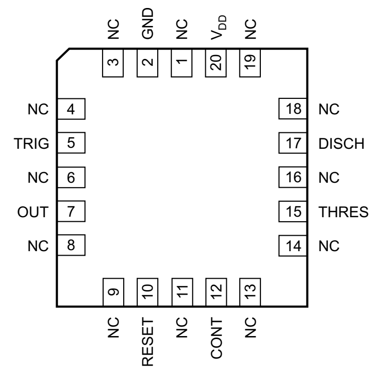
Pin Functions: D, P, PS, and JG Packages

PIN		I/O	DESCRIPTION
NAME	SOIC, PDIP, SOP, CDIP		
CONT	5	I	Controls comparator thresholds. Outputs 2/3 V_{DD} and allows bypass capacitor connection.
DISCH	7	O	Open collector output to discharge timing capacitor.
GND	1	—	Ground.
NC	—	—	No internal connection.
OUT	3	O	High current timer output signal.
RESET	4	I	Active low reset input forces output and discharge low.
THRES	6	I	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	2	I	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
V_{DD}	8	—	Power-supply voltage.

PW Package
14-Pin TSSOP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions: PW and FK

PIN			I/O	DESCRIPTION
NAME	TSSOP	LCCC		
CONT	8	12	I	Controls comparator thresholds. Outputs 2/3 V_{DD} and allows bypass capacitor connection.
DISCH	12	17	O	Open-collector output to discharge timing capacitor.
GND	1	2	—	Ground.
NC	2, 4, 6, 9, 11, 13	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	No internal connection.
OUT	5	7	O	High current timer output signal.
RESET	7	10	I	Active low reset input forces output and discharge low.
THRES	10	15	I	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	3	5	I	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
V_{DD}	14	20	—	Power-supply voltage.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)*Continuous total power dissipation* and *lead temperature* parameters from *Absolute Maximum Ratings*

			MIN	MAX	UNIT
Voltage	Supply, V_{DD} (2)		–0.3	18	V
	Input, any input		–0.3	V_{DD}	
	Discharge		–0.3	18	
Current	Sink, discharge or output			150	mA
	Source, output, I_O			15	
Temperature	Operating, T_A	C-suffix	0	70	°C
		I-suffix	–40	85	
		Q-suffix	–40	125	
		M-suffix	–55	125	
	Case, for 60 seconds	FK package	–65	150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD}	TLC555C	2	15	V
	TLC555I	3	15	
	TLC555M	5	15	
	TLC555Q	5	15	
Operating free-air temperature, T_A	TLC555C	0	70	°C
	TLC555I	–40	85	
	TLC555M	–55	125	
	TLC555Q	–40	125	

6.3 Thermal Information

THERMAL METRIC(1)		TLC555						UNIT
		D (SOIC)	FK (LCCC)	JG (CDIP)	P (PDIP)	PS (SOP)	PW (TSSOP)	
		8 PINS	20 PINS	8 PINS	8 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113	n/a	120	58	120	135	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58	37	81	48	72	61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55	36	110	35	69	77	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11	n/a	45	26	32	12	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54	n/a	103	35	68	77	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	4.3	31	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.4 Electrical Characteristics: V_{DD} = 2 V for TLC555C, V_{DD} = 3 V for TLC555I

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C	TLC555C	0.95	1.33	1.65	V
			TLC555I	1.6		2.4	
		Full range	TLC555C	0.85		1.75	
			TLC555I	1.5		2.5	
I_{IT}	Threshold current	25°C	TLC555C		10		pA
			TLC555I		10		
		Max	TLC555C		75		
			TLC555I		150		
$V_{I(TRIG)}$	Trigger voltage	25°C	TLC555C	0.4	0.67	0.95	V
			TLC555I	0.71	1	1.29	
		Full range	TLC555C	0.3		1.05	
			TLC555I	0.61		1.39	
$I_{I(TRIG)}$	Trigger current	25°C	TLC555C		10		pA
			TLC555I		10		
		Max	TLC555C		75		
			TLC555I		150		
$V_{I(RESET)}$	Reset voltage	25°C	TLC555C	0.4	1.1	1.5	V
			TLC555I	0.4	1.1	1.5	
		Full range	TLC555C	0.3		2	
			TLC555I	0.3		1.8	
	Control voltage (open-circuit) as a percentage of supply voltage	Max	TLC555C		66.7%		
			TLC555I		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 1 mA, 25°C	TLC555C		0.03	0.2	V
			TLC555I		0.03	0.2	
		I_{OL} = 1 mA, Full range	TLC555C			0.25	
			TLC555I			0.375	
	Discharge switch off-stage current	25°C	TLC555C		0.1		nA
			TLC555I		0.1		
		Max	TLC555C		0.5		
			TLC555I		120		
V_{OH}	High-level output voltage	I_{OH} = –300 µA, 25°C	TLC555C	1.5	1.9		V
			TLC555I	2.5	2.85		
		I_{OH} = –300 µA, Full range	TLC555C	1.5			
			TLC555I	2.5			
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, 25°C	TLC555C		0.07	0.3	V
			TLC555I		0.07	0.3	
		I_{OL} = 1 mA, Full range	TLC555C			0.35	
			TLC555I			0.4	
I_{DD}	Supply current(2)	25°C	TLC555C			250	µA
			TLC555I			250	
		Full range	TLC555C			400	
			TLC555I			500	
C_{PD}	Power dissipation capacitance(3)(4)	25°C	TLC555C		80		pF
			TLC555I		90		

(1) Full range is 0°C to 70°C the for TLC555C, and –40°C to 85°C for the TLC555I. For conditions shown as ***Max***, use the appropriate value specified in the *Recommended Operating Conditions* table.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.
(3) C_{PD} is used to determine the dynamic power consumption.
(4) $P_D = V_{DD}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage

6.5 Electrical Characteristics: V_{DD} = 5 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[(1)]		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	2.8	3.3	3.8	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	2.7		3.9	
I_{IT}	Threshold current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
$V_{I(TRIG)}$	Trigger voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	1.36	1.66	1.96	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	1.26		2.06	
$I_{I(TRIG)}$	Trigger current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
C_I	Trigger, threshold capacitance (each pin)	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		2.1		pF
$V_{I(RESET)}$	Reset voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	0.4	1.1	1.5	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	0.3		1.8	
$I_{I(RESET)}$	Reset current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
	Control voltage (open circuit) as a percentage of supply voltage	Max	TLC555C, TLC555I, TLC555M, TLC555Q		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 10 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.14	0.5	V
		I_{OL} = 10 mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q			0.6	
	Discharge switch off-stage current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.1		nA
		Max	TLC555C		0.5		
			TLC555I		120		
			TLC555M, TLC555Q		120		
V_{OH}	High-level output voltage	I_{OH} = –1 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q	4.1	4.8		V
		I_{OH} = –1 mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q	4.1			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.21	0.4	V
		I_{OL} = 8 mA, Full range	TLC555C			0.5	
			TLC555I			0.5	
			TLC555M, TLC555Q			0.6	

(1) Full range is 0°C to 70°C the for TLC555C, –40°C to 85°C for the TLC555I, –40°C to 125°C for the TLC555Q, and –55°C to 125°C for the TLC555M. For conditions shown as ***Max***, use the appropriate value specified in the *Recommended Operating Conditions* table.

Electrical Characteristics: V_{DD} = 5 V (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 5 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.13	0.3	V
		I_{OL} = 5 mA, Full range	TLC555C			0.4	
			TLC555I			0.4	
			TLC555M, TLC555Q			0.45	
		I_{OL} = 3.2 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.08	0.3	
		I_{OL} = 3.2 mA, Full range	TLC555C			0.35	
			TLC555I			0.35	
			TLC555M, TLC555Q			0.4	
I_{DD}	Supply current[2]	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		170	350	µA
		Full range	TLC555C			500	
			TLC555I			600	
			TLC555M, TLC555Q			700	
C_{PD}	Power dissipation capacitance[3][4]	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		115		pF

(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.
(3) C_{PD} is used to determine the dynamic power consumption.
(4) $P_D = V_{DD}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage

6.6 Electrical Characteristics: V_{DD} = 15 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	9.45	10	10.55	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	9.35		10.65	
I_{IT}	Threshold current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
$V_{I(TRIG)}$	Trigger voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	4.65	5	5.35	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	4.55		5.45	
$I_{I(TRIG)}$	Trigger current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		
C_I	Trigger, threshold capacitance (each pin)	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		1.8		pF
$V_{I(RESET)}$	Reset voltage	25°C	TLC555C, TLC555I, TLC555M, TLC555Q	0.4	1.1	1.5	V
		Full range	TLC555C, TLC555I, TLC555M, TLC555Q	0.3		1.8	
$I_{I(RESET)}$	Reset current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		10		pA
		Max	TLC555C		75		
			TLC555I		150		
			TLC555M, TLC555Q		5000		

(1) Full range is 0°C to 70°C for TLC555C, –40°C to 85°C for TLC555I, –40°C to 125°C for the TLC555Q, and –55°C to 125°C for TLC555M. For conditions shown as ***Max***, use the appropriate value specified in the *Recommended Operating Conditions* table.

Electrical Characteristics: V_{DD} = 15 V (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
	Control voltage (open circuit) as a percentage of supply voltage	Max	TLC555C, TLC555I, TLC555M, TLC555Q		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 100 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.77	1.7	V
		I_{OL} = 100 mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q			1.8	
	Discharge switch off-stage current	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.1		nA
		Max	TLC555C		0.5		
			TLC555I		120		
			TLC555M, TLC555Q		120		
V_{OH}	High-level output voltage	I_{OH} = –10 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q	12.5	14.2		V
		I_{OH} = –10 mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q	12.5			
		I_{OH} = –5 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q	13.5	14.6		
		I_{OH} = –5 mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q	13.5			
		I_{OH} = –1 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q	14.2	14.9		
		I_{OH} = –1 mA, Full range	TLC555C, TLC555I, TLC555M, TLC555Q	14.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		1.28	3.2	V
		I_{OL} = 100 mA, Full range	TLC555C			3.6	
			TLC555I			3.7	
			TLC555M, TLC555Q			3.8	
		I_{OL} = 50 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.63	1	
		I_{OL} = 50 mA, Full range	TLC555C			1.3	
			TLC555I			1.4	
			TLC555M, TLC555Q			1.5	
		I_{OL} = 10 mA, 25°C	TLC555C, TLC555I, TLC555M, TLC555Q		0.12	0.3	
		I_{OL} = 10 mA, Full range	TLC555C			0.4	
			TLC555I			0.4	
			TLC555M, TLC555Q			0.45	
I_{DD}	Supply current[2]	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		360	600	µA
		Full range	TLC555C			800	
			TLC555I			900	
			TLC555M, TLC555Q			1000	
C_{PD}	Power dissipation capacitance[3][4]	25°C	TLC555C, TLC555I, TLC555M, TLC555Q		140		pF

(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.
(3) C_{PD} is used to determine the dynamic power consumption.
(4) $P_D = V_{DD}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage

6.7 Operating Characteristics

V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Initial error of timing interval[1]	V_{DD} = 5 V to 15 V, C_T = 0.1 μF R_A = R_B = 1 kΩ to 100 kΩ [2]		1%	3%	
	Supply voltage sensitivity of timing interval	V_{DD} = 5 V to 15 V, C_T = 0.1 μF R_A = R_B = 1 kΩ to 100 kΩ [2]		0.1	0.5	%/V
t_r	Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
t_f	Output pulse fall time	R_L = 10 MΩ, C_L = 10 pF		15	60	ns
f_{max}	Maximum frequency in a-stable mode	R_A = 470 Ω, C_T = 200 pF R_B = 200 Ω [2]	1.2	2.1		MHz

(1) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
(2) R_A, R_B, and C_T are as defined in Figure 12.

6.8 Typical Characteristics

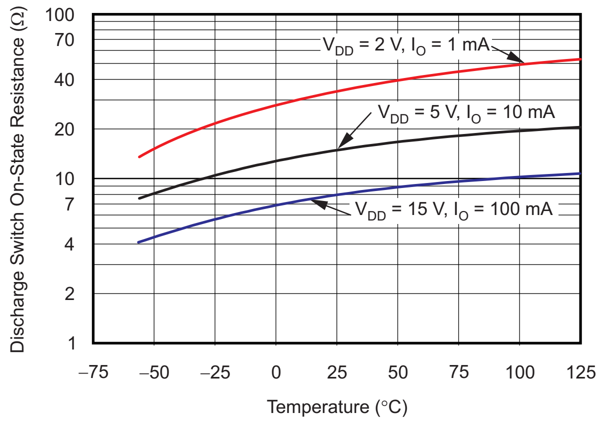
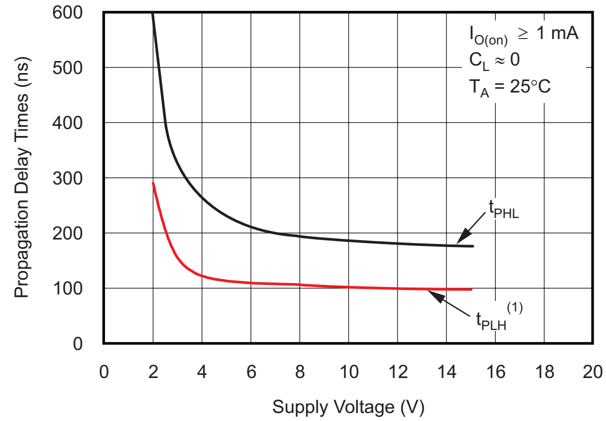


Figure 1. Discharge Switch On-State Resistance vs Free-Air Temperature



(1) The effects of the load resistance on these values must be taken into account separately.

Figure 2. Propagation Delay Times to Discharge Output From Trigger and Threshold Shorted Together vs Supply Voltage

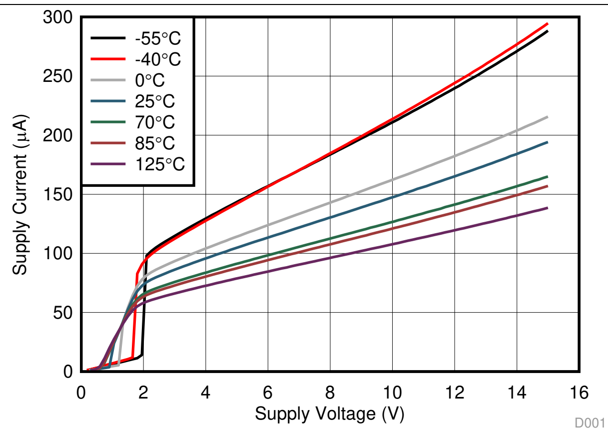


Figure 3. Supply Current vs Supply Voltage

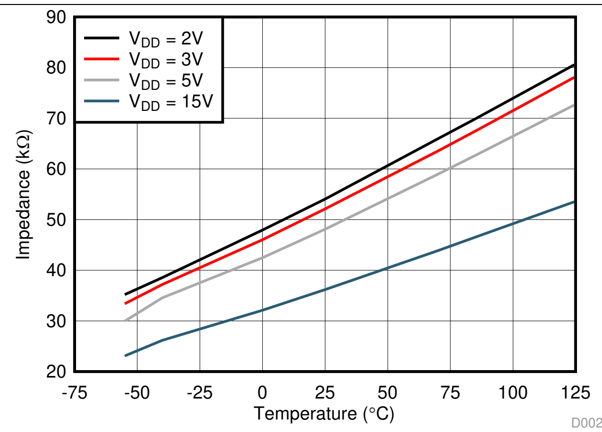


Figure 4. Control Impedance vs Temperature

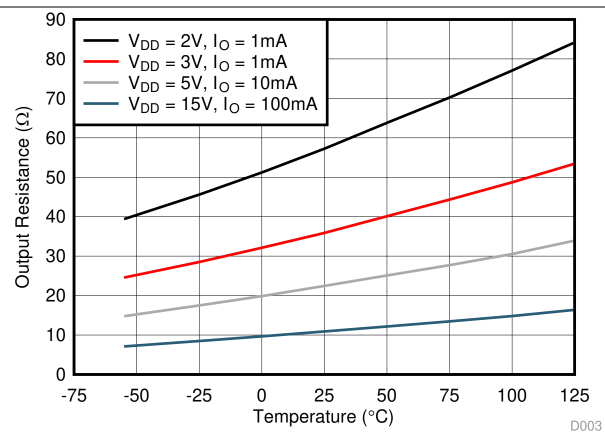


Figure 5. Output Low Resistance vs Temperature

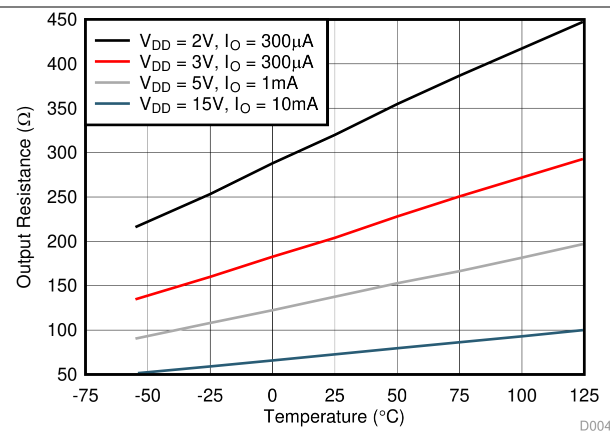


Figure 6. Output High Resistance vs Temperature

Typical Characteristics (continued)

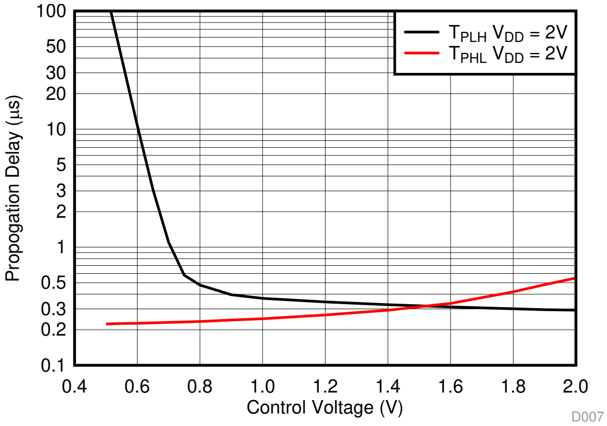


Figure 7. Propagation Delay vs Control Voltage V_{DD} = 2 V

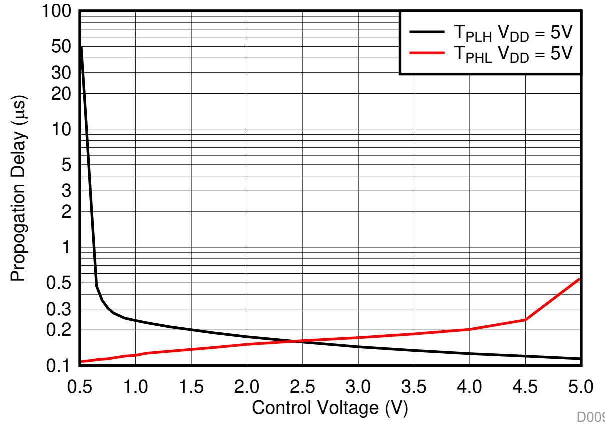


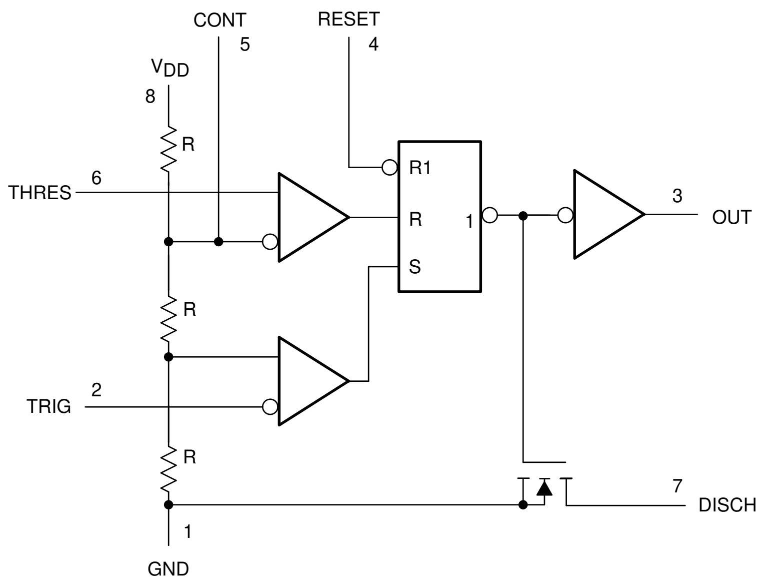
Figure 8. Propagation Delay vs Control Voltage V_{DD} = 5 V

7 Detailed Description

7.1 Overview

The TLC555 is a precision timing device used for general-purpose timing applications up to 2.1 MHz. All inputs are level sensitive not edge triggered inputs.

7.2 Functional Block Diagram



Pin numbers are for all packages except the PW and FK package. RESET can override TRIG, which can override THRES (when CONT pin is 2/3 V_{DD}).

The resistance of “R" resistors vary with V_{DD} and temperature. The resistors match each other very well across V_{DD} and temperature for a temperature stable control voltage ratio.

7.3 Feature Description

7.3.1 Monostable Operation

For monostable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the internal latch; the output goes high, and discharge pin (DISCH) becomes open drain. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the internal latch, the output goes low, the discharge pin goes low which quickly discharges capacitor C.

Feature Description (continued)

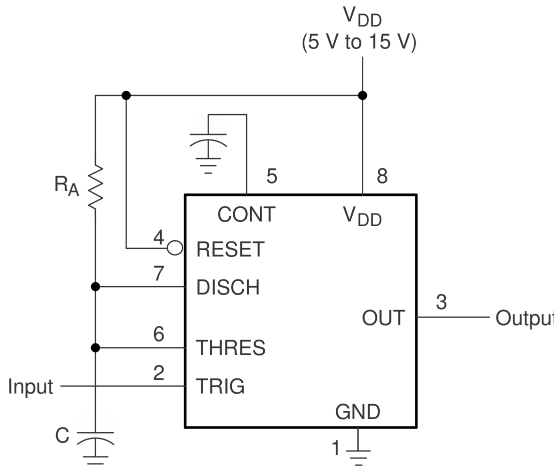


Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least 1 µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 1 µs, which limits the minimum monostable pulse width to 1 µs. The output pulse duration is approximately $t_w = 1.1 \times R_A C$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{DD}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges capacitor C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used it must be connected to V_{DD}.

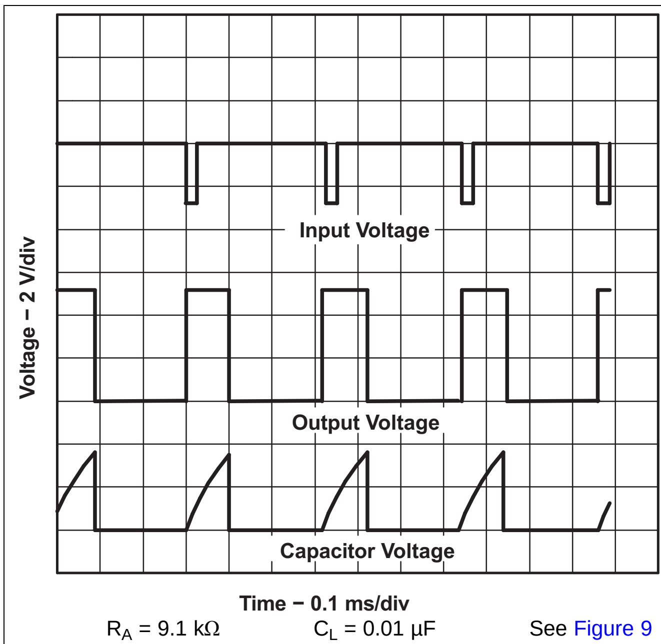


Figure 10. Typical Monostable Waveforms

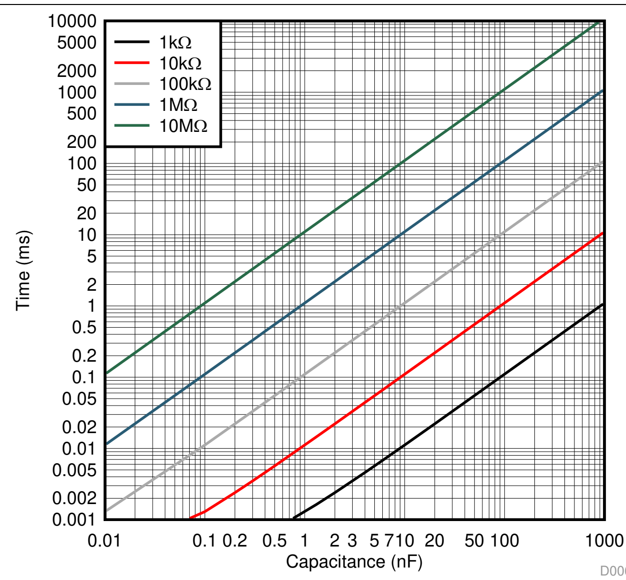


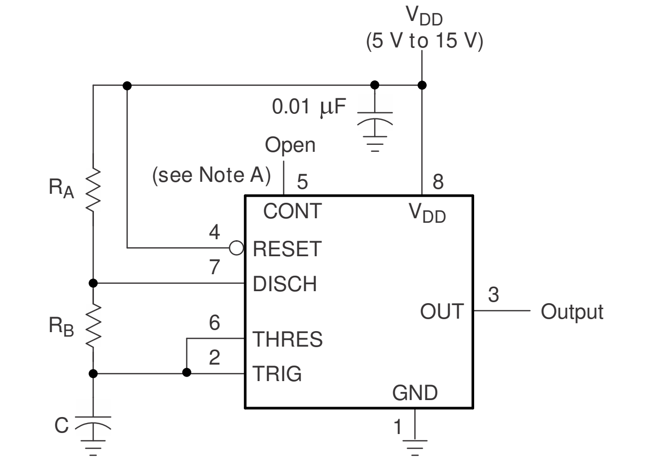
Figure 11. Output Pulse Duration vs Capacitance

Feature Description (continued)

7.3.2 Astable Operation

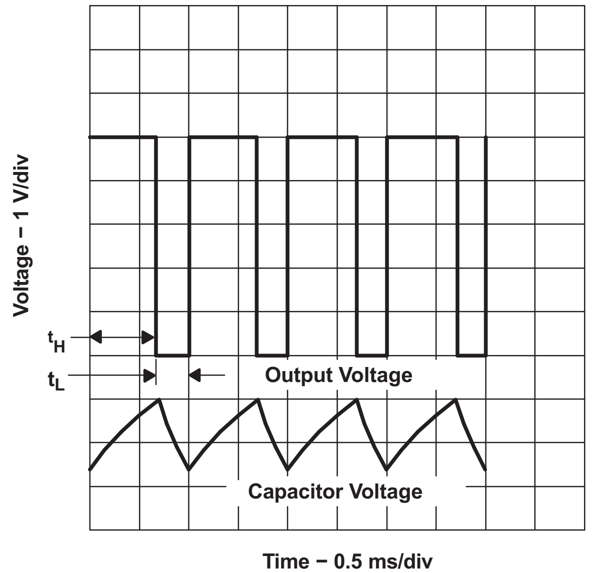
As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level (≈ 0.67 × V_{CC}) and the trigger-voltage level (≈ 0.33 × V_{CC}). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation



R_A = 5 kΩ R_B = 3 kΩ C = 0.15 µF
See Figure 12

Figure 13. Typical Astable Waveforms

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L for frequencies below 100 kHz can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

Feature Description (continued)

The formulas (1-7) do not account for any propagation delay times from the TRIG and THRES inputs to DISCH output. These delay times add directly to the period and overcharge the capacitor which creates differences between calculated and actual values that increase with frequency. In addition, the internal on-state resistance r_{on} during discharge adds to R_B to provide another source of timing error in the calculation when R_B is very low. The equations below provide better agreement with measured values. The formulas Equation 8 represent the actual low and high times when used at higher frequencies because propagation delay and discharge on resistance is added to the formulas. Because the formulas are complex, a calculation tool, TLC555 Design Calculator can be used to calculate the component values.

$$t_{c(H)} = C_T\ (R_A + R_B)\ln\left[3 - \exp\left(\frac{-t_{PLH}}{C_T(R_B + r_{on})}\right)\right] + t_{PHL}$$

$$t_{c(L)} = C_T\ (R_B + r_{on})\ln\left[3 - \exp\left(\frac{-t_{PHL}}{C_T(R_A + R_B)}\right)\right] + t_{PLH} \quad (8)$$

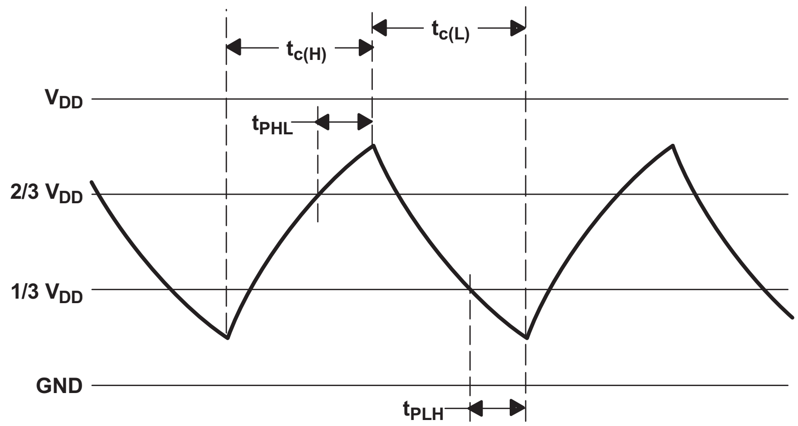


Figure 14. Trigger and Threshold Voltage Waveform

Feature Description (continued)

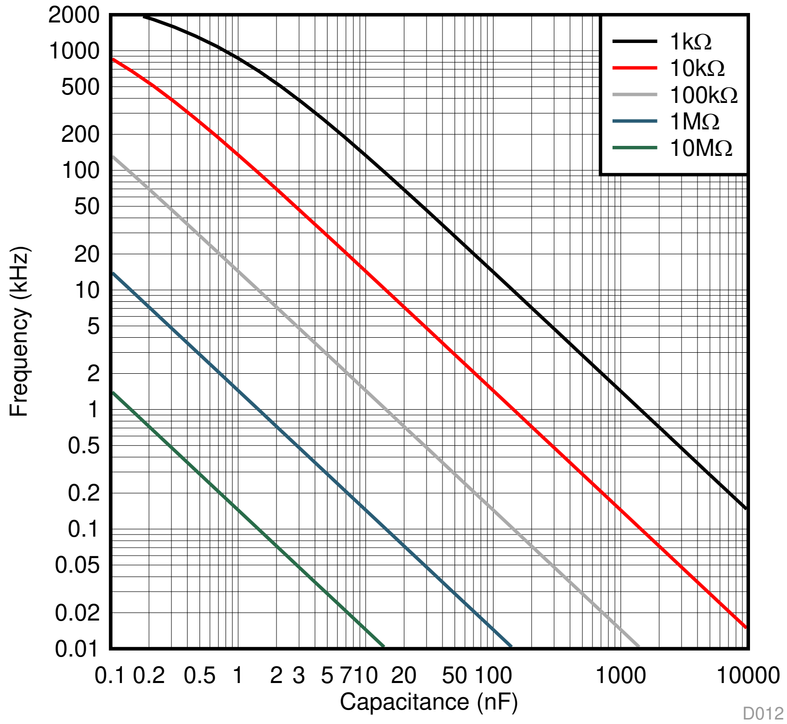
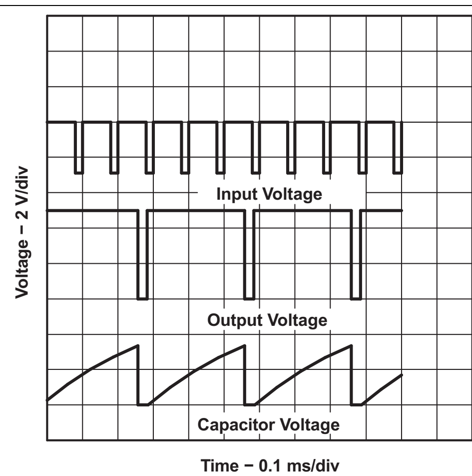


Figure 15. Free-Running Frequency vs Timing Capacitance
Resistance = $R_A + 2 \times R_B$

7.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 16 shows a divide-by-three circuit that makes use of the fact that re-triggering cannot occur during the timing cycle.



V_{CC} = 5 V R_A = 1250 Ω C = 0.02 µF
See Figure 9

Figure 16. Divide-by-Three Circuit Waveforms

7.4 Device Functional Modes

Table 1 shows the device truth table.

Table 1. Function Table

RESET VOLTAGE(1)	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	L	On
>MAX	<MIN	Irrelevant(2)	H	Off
>MAX	>MAX	>MAX	L	On
>MAX	>MAX	<MIN	As previously established	

(1) For conditions shown as MIN or MAX, use the appropriate value specified under *Electrical Characteristics: V_{DD} = 5 V*.
(2) CONT pin open or 2/3 V_{DD}.

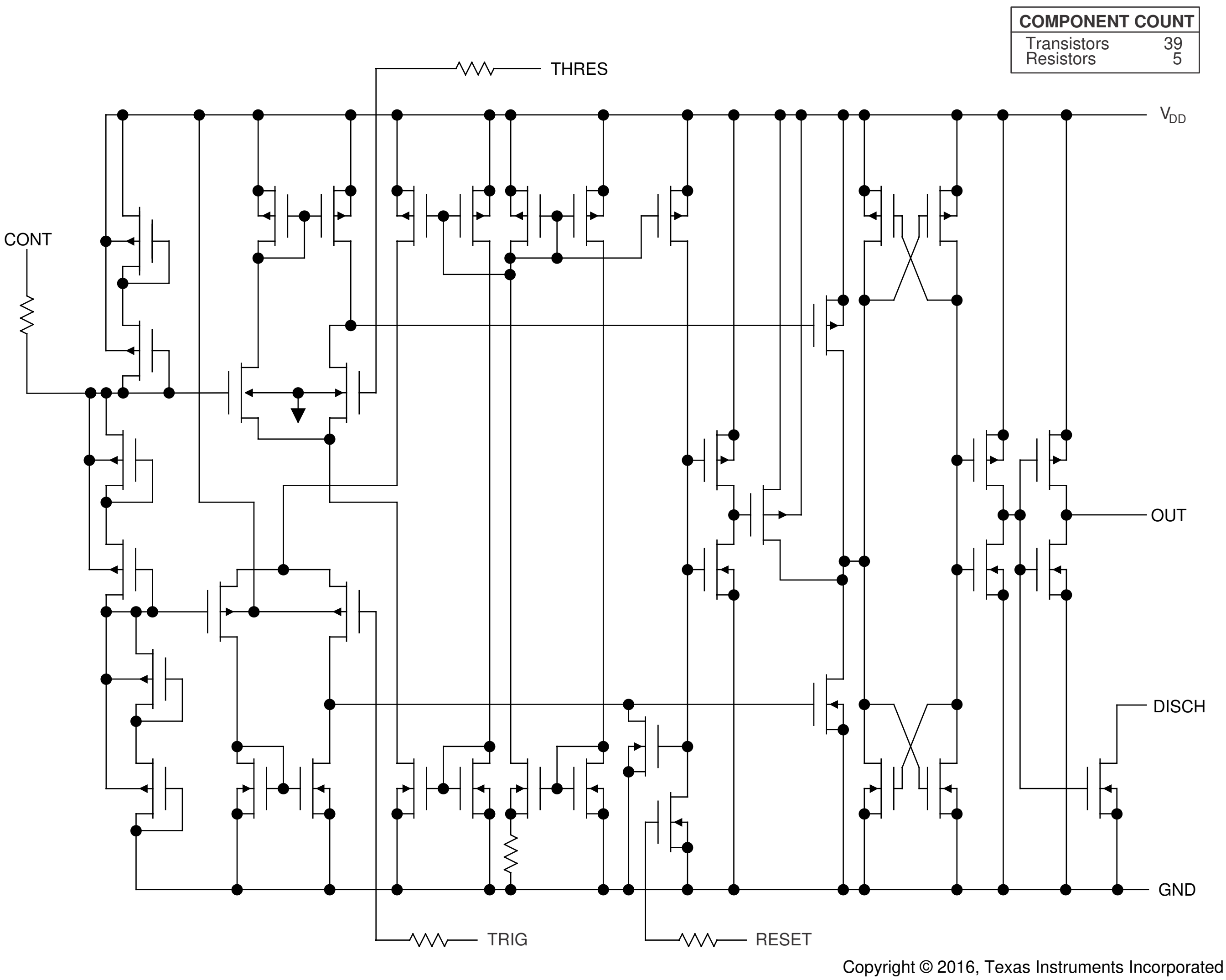


Figure 17. Equivalent Schematic

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLC555 timer device uses resistor and capacitor charging delay to provide a programmable time delay or operating frequency. The *Typical Applications* section presents a simplified discussion of the design process. Reset mode forces output and discharge low and provides a small reduction in supply current.

8.2 Typical Applications

8.2.1 Missing-Pulse Detector

The circuit shown in Figure 18 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 19.

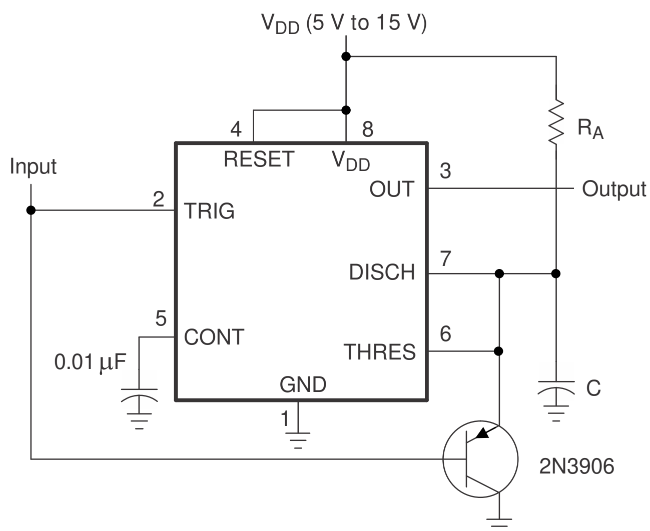


Figure 18. Circuit for Missing-Pulse Detector

8.2.1.1 Design Requirements

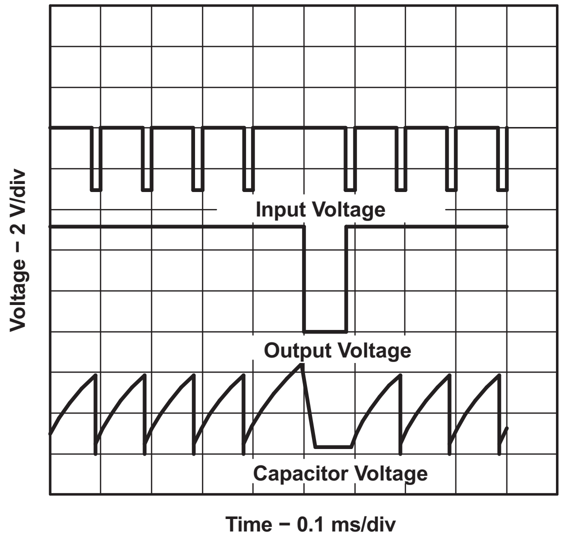
Input fault (missing pulses) must be input high. An input stuck low cannot be detected because the timing capacitor (C) remains discharged.

8.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C$ > [maximum normal input high time].

Typical Applications (continued)

8.2.1.3 Application Curve

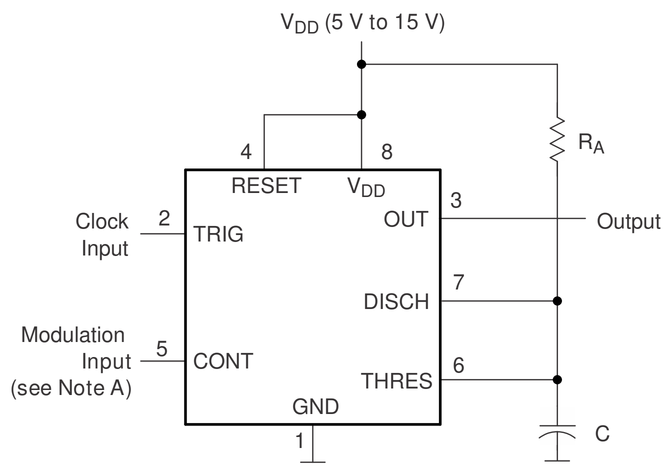


V_{DD} = 5 V R_A = 1 kΩ   C = 0.1 µF
See Figure 18

Figure 19. Timing Waveforms for Missing-Pulse Detector

8.2.2 Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 20 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 21 shows the resulting duty cycle versus control voltage transfer function. Attempting to run under 10% duty cycle could result in inconsistent output pulses. Attempting to run close to 100% duty cycle will result in frequency division by 2, then 3, then 4.



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

Figure 20. Circuit for Pulse-Width Modulation

Typical Applications (continued)

8.2.2.1 Design Requirements

The clock input must have V_{OL} and V_{OH} levels that are less than and greater than 1/3 V_{DD}, respectively. Clock input V_{OL} time must be less than minimum output high time, therefore a high (positive) duty cycle clock is recommended. Minimum recommended modulation voltage is 1 V. Lower CONT voltage can greatly increase threshold comparator's propagation delay and storage time. The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is RC based with an negative exponential curve.

8.2.2.2 Detailed Design Procedure

Choose R_A and C so that R_A × C is same or less than clock input period. Figure 21 shows the non linear relationship between control voltage and output duty cycle. Duty cycle is function of control voltage and clock period relative to RC time constant.

8.2.2.3 Application Curve

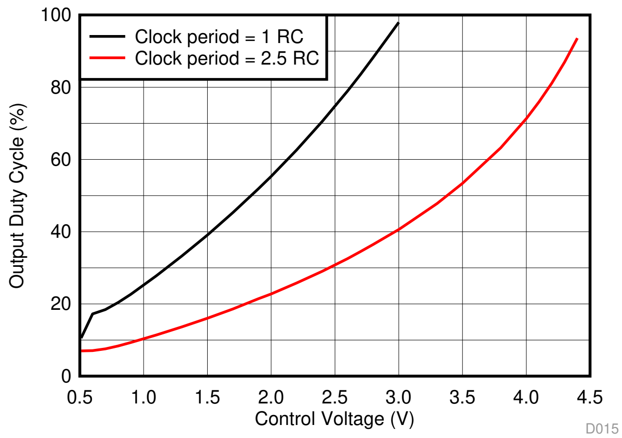
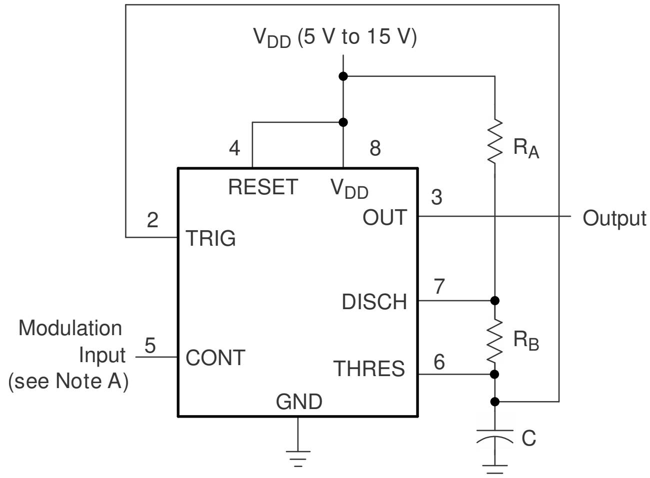


Figure 21. Pulse-Width-Modulation vs Control Voltage Clock Duty Cycle 98%, V_{DD} = 5 V

8.2.3 Pulse-Position Modulation

As shown in Figure 22, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and thereby the time delay of a free-running oscillator. Figure 23 and Figure 24 shows the output frequency and duty cycle versus control voltage.

Typical Applications (continued)



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

$R_A = 3\ k\Omega$ $R_B = 309\ k\Omega$ $C = 1\ nF$

Figure 22. Circuit for Pulse-Position Modulation

8.2.3.1 Design Requirements

Both DC- and AC-coupled modulation input changes the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle vary with the modulation voltage. Control voltage below 1 V could result in output glitches instead of a steady output pulse stream

8.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle for control voltage set to 2/3 of V_{DD} can be determined using formulas in *Astable Operation* section.

8.2.3.3 Application Curves

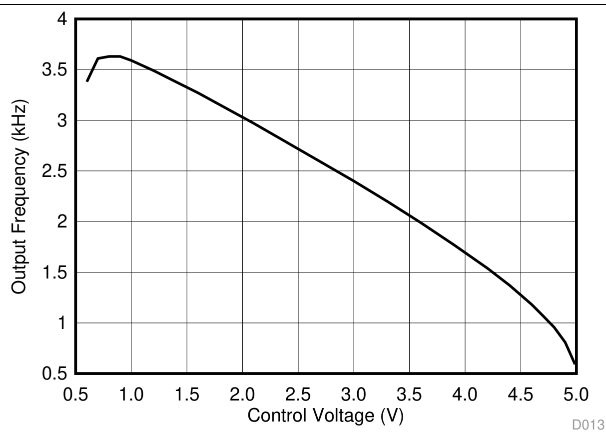


Figure 23. Pulse-Position-Modulation Frequency vs Control Voltage, V_{DD} = 5 V

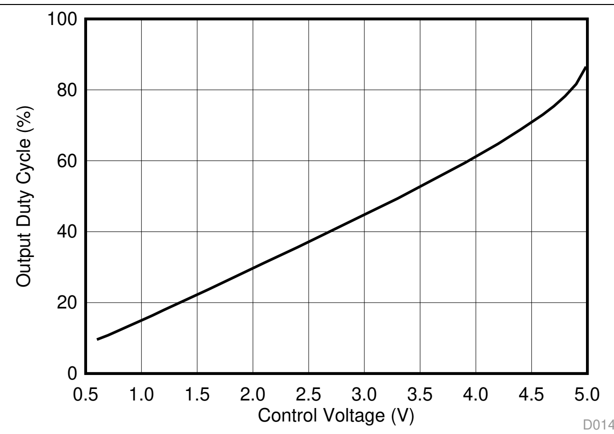
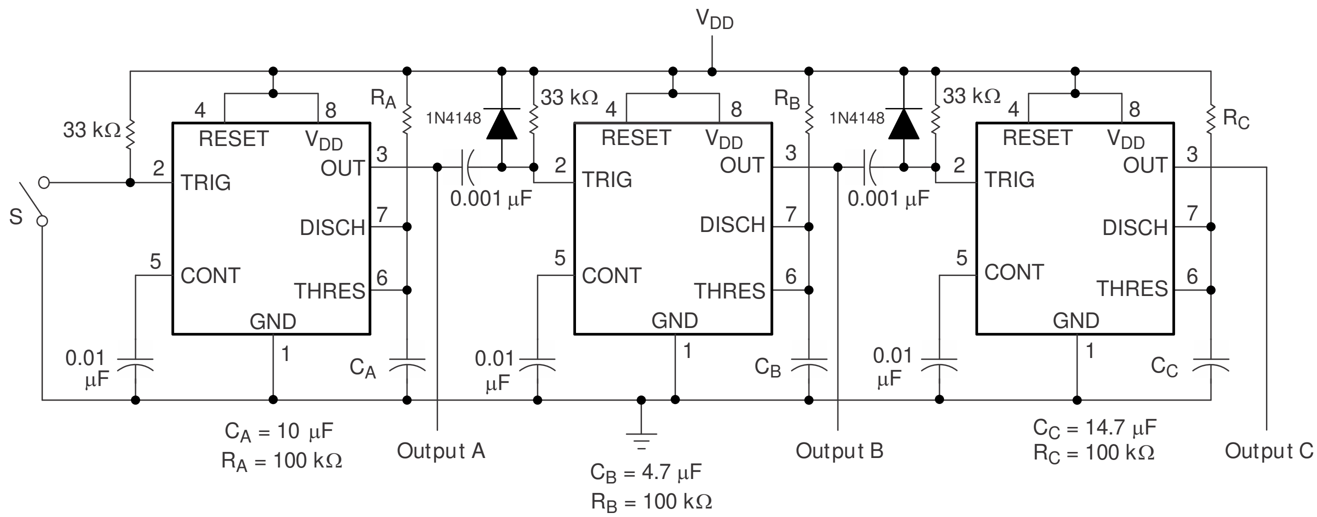


Figure 24. Pulse-Position-Modulation Duty Cycle vs Control Voltage, V_{DD} = 5 V

Typical Applications (continued)

8.2.4 Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 25 shows a sequencer circuit with possible applications in many systems, and Figure 26 shows the output waveforms.



NOTE: S closes momentarily at t = 0.

Figure 25. Sequential Timer Circuit

8.2.4.1 Design Requirements

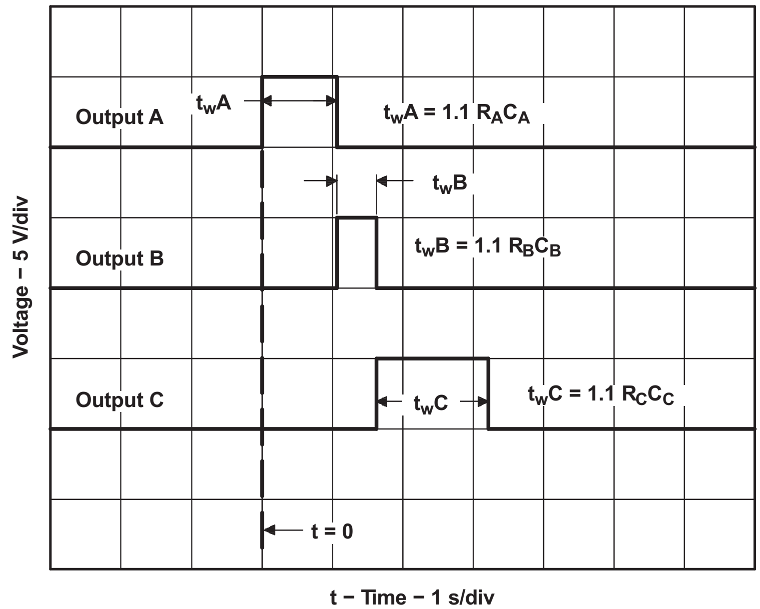
The sequential timer application chains together multiple monostable timers. The joining components are the 33-kΩ resistors and 0.001-µF capacitors. The output high to low edge passes a 10-µs start pulse to the next monostable. A diode is needed to prevent over voltage on the trigger input when on the previous output's low to high edge.

8.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula: $t_w = 1.1 \times R \times C$.

Typical Applications (continued)

8.2.4.3 Application Curve



See Figure 25

Figure 26. Sequential Timer Waveforms

8.2.5 Designing for Improved ESD Performance

The TLC555 internal HBM and CDM protection allows for safe assembly in ESD controlled environments. In applications that may expose pins of the TLC555 to ESD, additional protection is highly recommended. The test board schematic below has bypass capacitors, current-limiting resistors, and voltage clamping TVS diodes to provide additional protection for commonly exposed pins [Reset, Trig, and Output] against ESD.

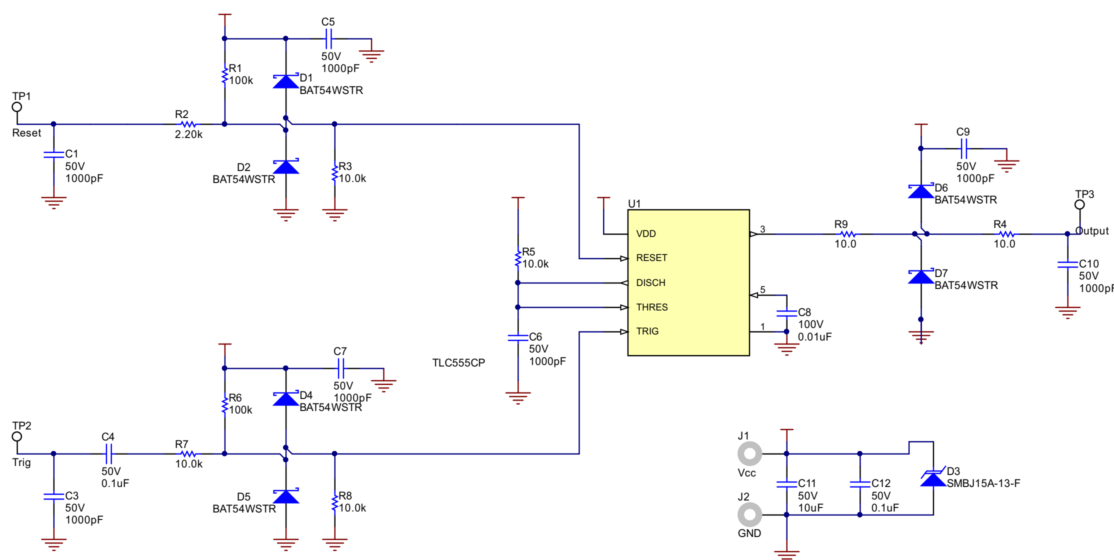


Figure 27. ESD Test Schematic

Typical Applications (continued)

The table below gives the ESD protection levels recorded for different supply voltages and external components populated. Using only passive components to protect the TLC555 with a single 15-V supply is not recommended because the higher voltage allows for an unacceptable amount of current to flow through the device.

Table 2. ESD test result table

Supply Voltage	Just passive components populated. D1..D7 not populated (1)	All components populated (1)
5 V	8 kV	12 kV
15 V	Not recommended	12 kV

(1) Sample results. Results may vary with populated components, board layout, and samples used.

9 Power Supply Recommendations

The TLC555 requires a voltage supply greater than or equal to 2 V, 3 V, or 5 V based the coldest ambient temperature supported and a supply voltage less than or equal to 15 V. Adequate power supply bypassing is necessary to protect associated circuitry and provide stable output pulses. Minimum recommended is 0.1-µF ceramic in parallel with 1-µF electrolytic. Place the bypass capacitors as close as possible to the TLC555 and minimize the trace length.

10 Layout

10.1 Layout Guidelines

Standard PCB rules apply to routing the TLC555. The 0.1-µF ceramic capacitor in parallel with a 1-µF electrolytic capacitor must be as close as possible to the TLC555. The capacitor used for the time delay must also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

Figure 28 is the basic layout for various applications.

- C1—based on time delay calculations
- C2—0.01-µF bypass capacitor for control voltage pin
- C3—0.1-µF bypass ceramic capacitor
- C4—1-µF electrolytic bypass capacitor
- R1—based on time-delay calculations

10.2 Layout Example

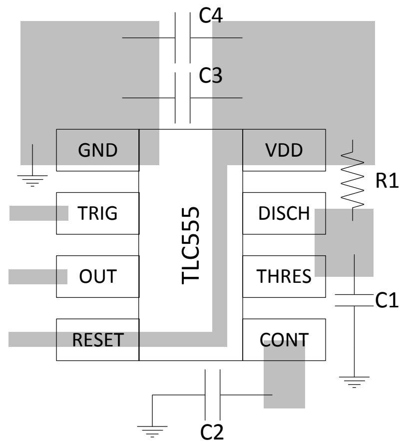


Figure 28. Layout Example

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC555CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL555C	Samples
TLC555CDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL555C	Samples
TLC555CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL555C	Samples
TLC555CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL555C	Samples
TLC555CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC555CP	Samples
TLC555CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC555CP	Samples
TLC555CPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555	Samples
TLC555CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555	Samples
TLC555CPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555	Samples
TLC555CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555	Samples
TLC555CPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	P555	Samples
TLC555ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL555I	Samples
TLC555IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL555I	Samples
TLC555IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL555I	Samples
TLC555IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL555I	Samples
TLC555IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC555IP	Samples
TLC555IPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLC555IP	Samples
TLC555QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL555Q	Samples
TLC555QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TL555Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLC555 :

- Automotive : TLC555-Q1
- Military : TLC555M

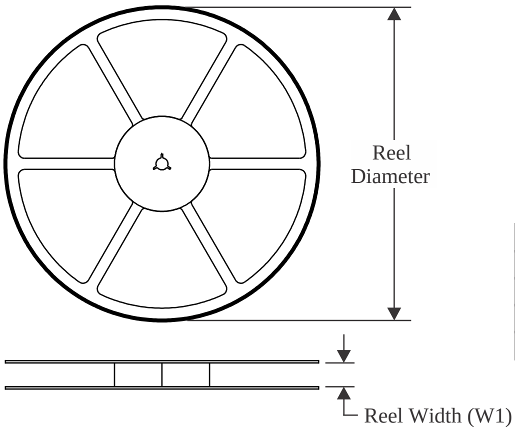
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

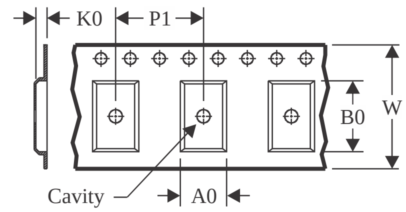
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

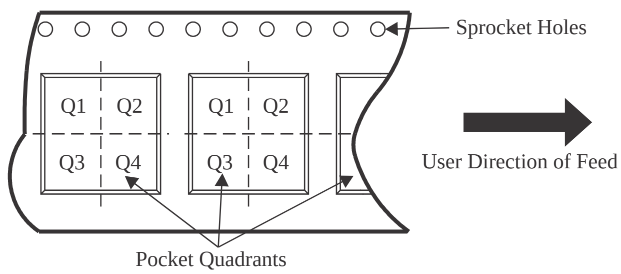


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

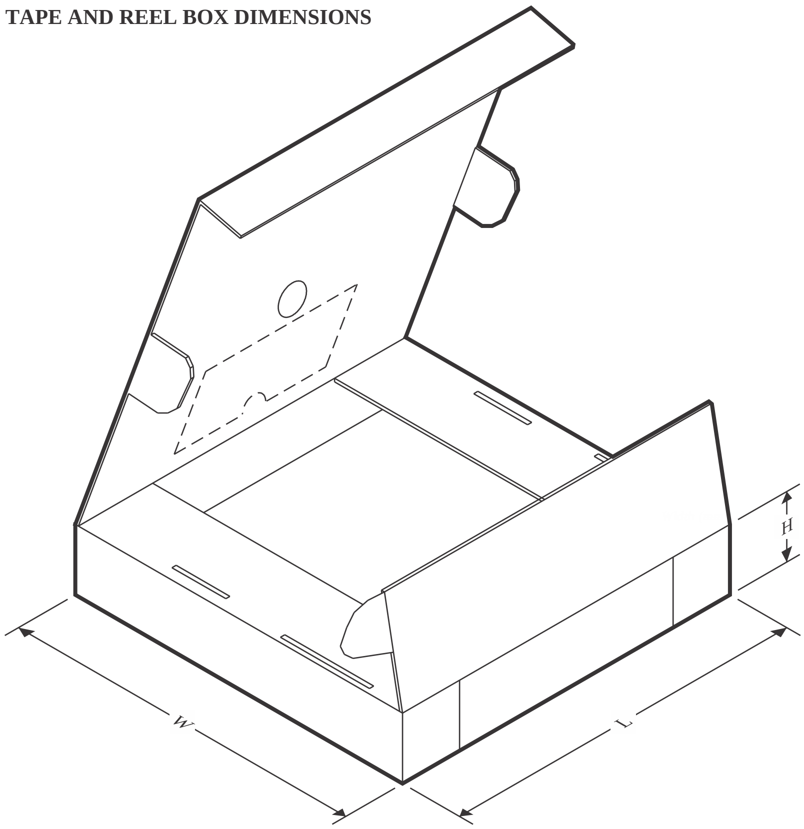
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC555CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1
TLC555CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC555IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC555QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

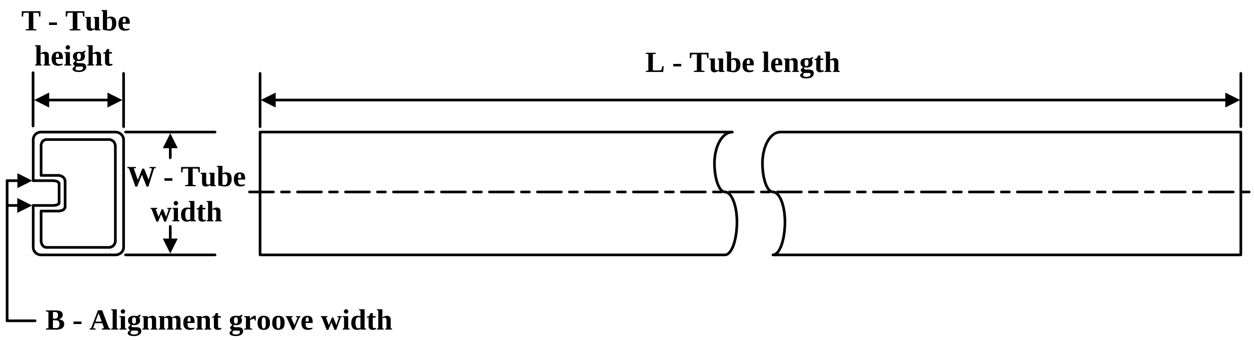
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC555CDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC555CPSR	SO	PS	8	2000	367.0	367.0	38.0
TLC555CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLC555IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLC555QDR	SOIC	D	8	2500	350.0	350.0	43.0
TLC555QDRG4	SOIC	D	8	2500	350.0	350.0	43.0

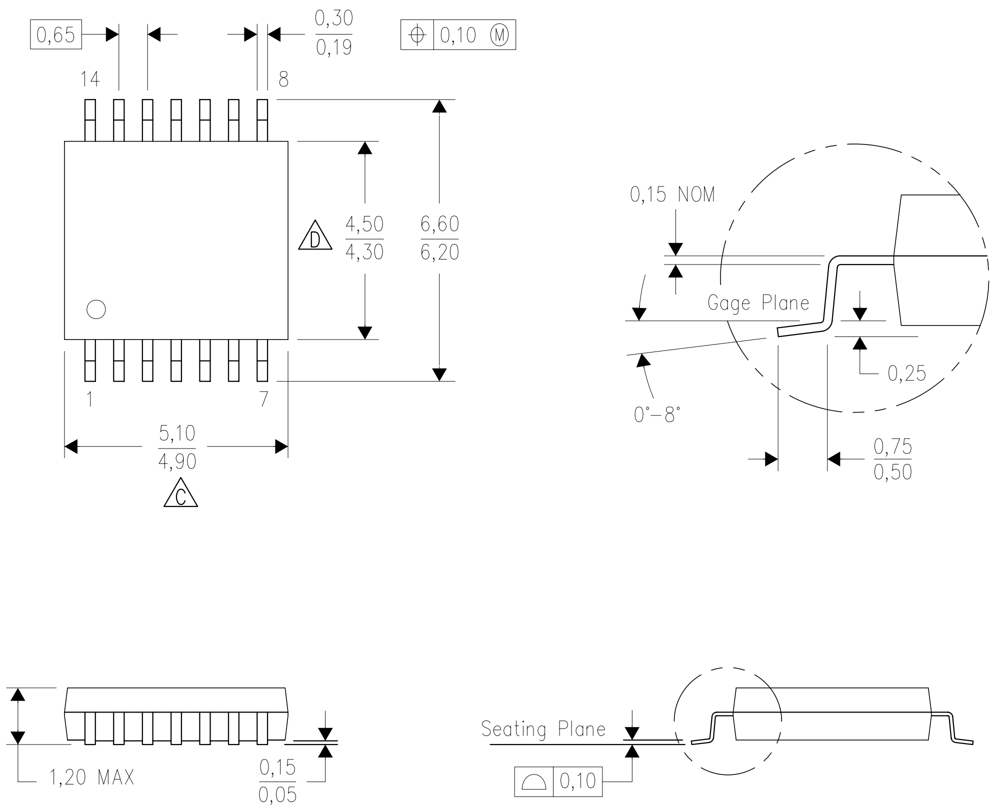
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC555CD	D	SOIC	8	75	507	8	3940	4.32
TLC555CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC555CDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC555CDG4	D	SOIC	8	75	507	8	3940	4.32
TLC555CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC555CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLC555CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC555CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC555ID	D	SOIC	8	75	507	8	3940	4.32
TLC555ID	D	SOIC	8	75	505.46	6.76	3810	4
TLC555IDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC555IDG4	D	SOIC	8	75	507	8	3940	4.32
TLC555IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC555IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC555IPE4	P	PDIP	8	50	506	13.97	11230	4.32
TLC555IPE4	P	PDIP	8	50	506	13.97	11230	4.32

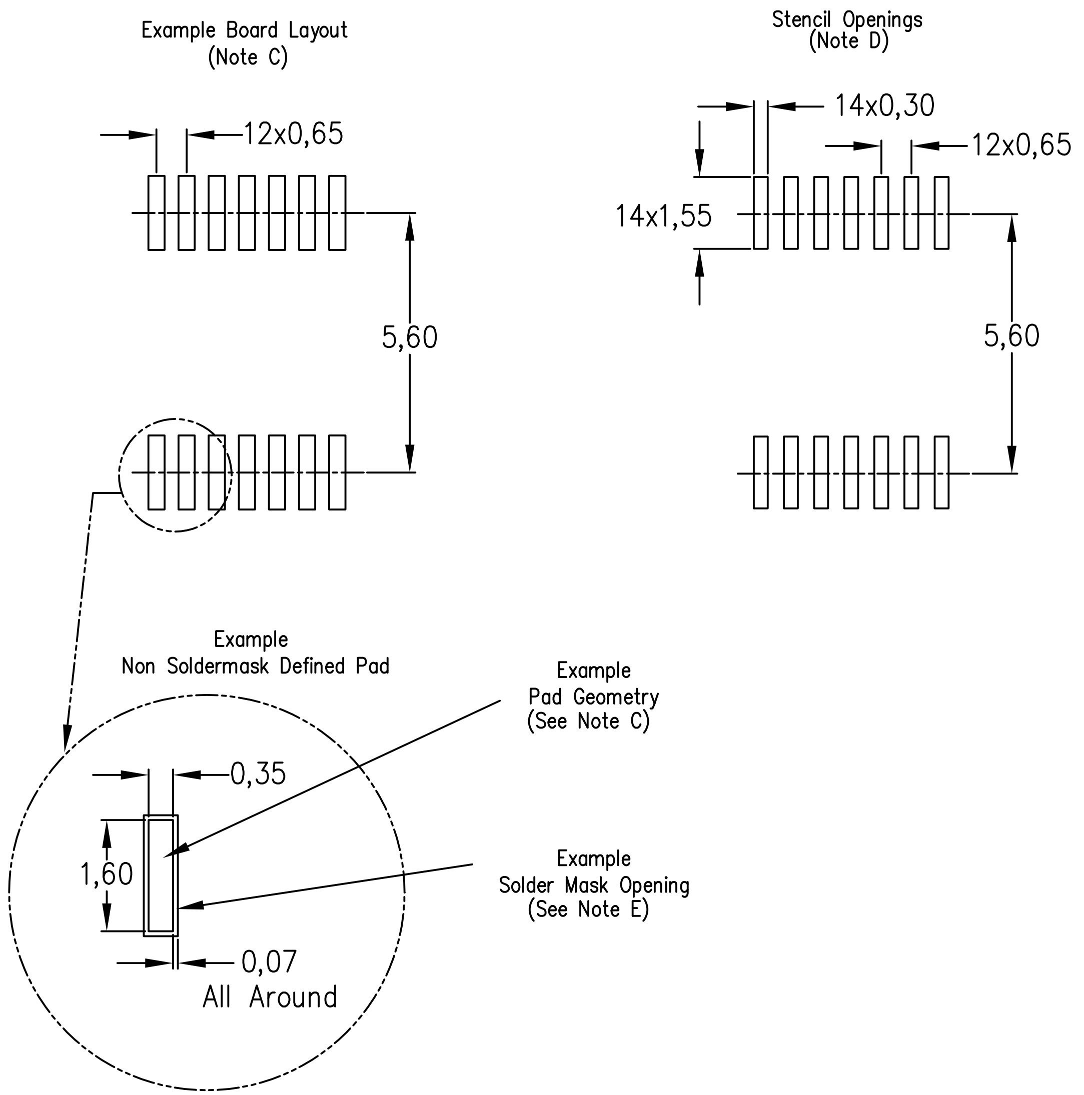
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

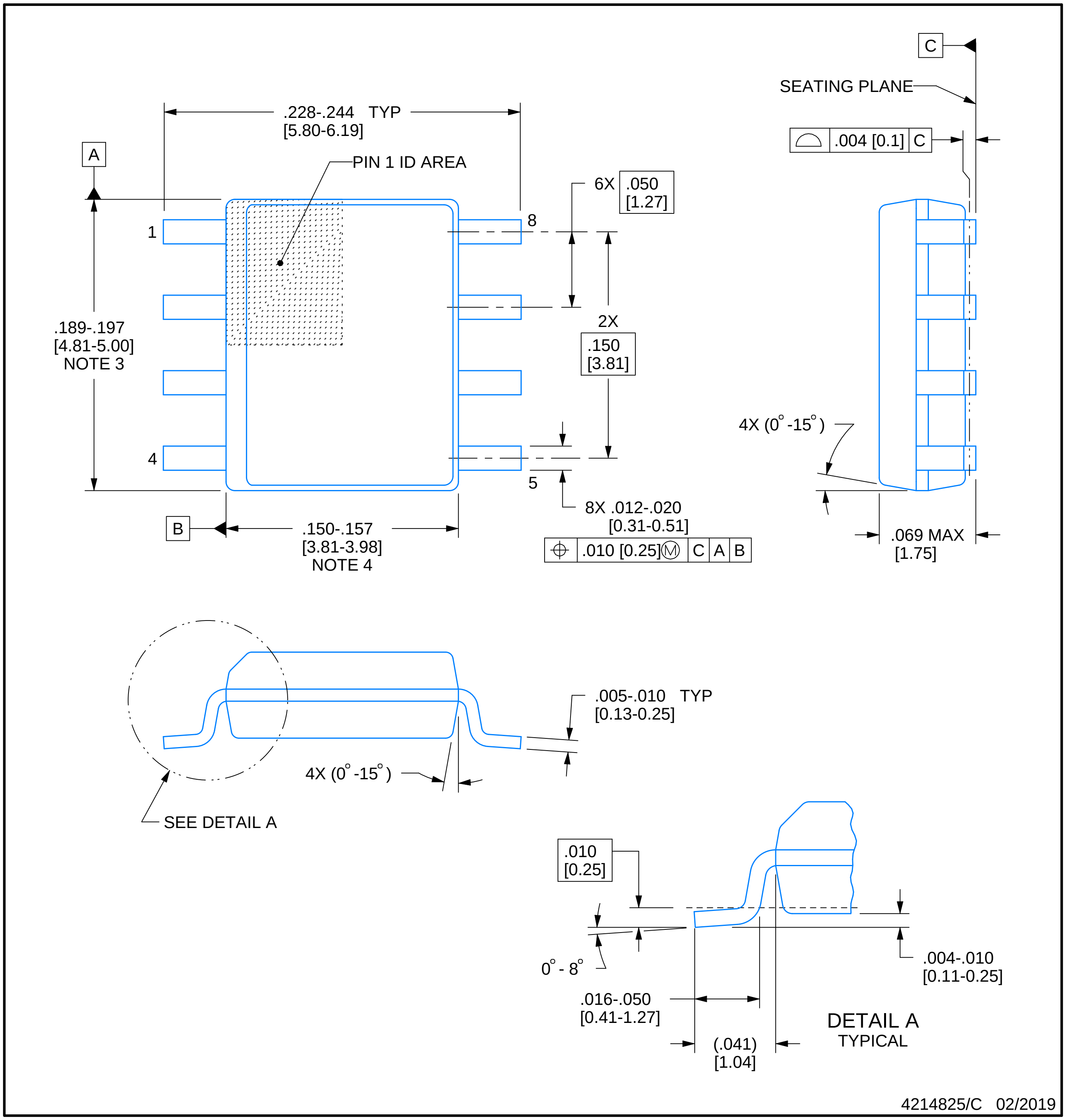
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



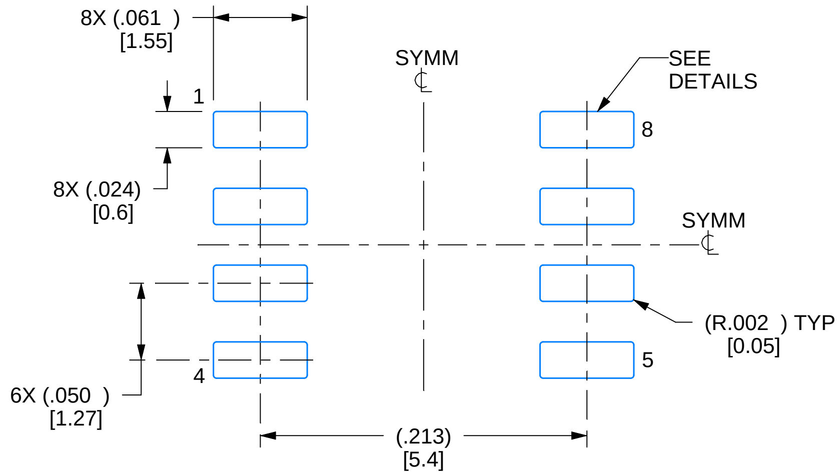
4211284-2/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

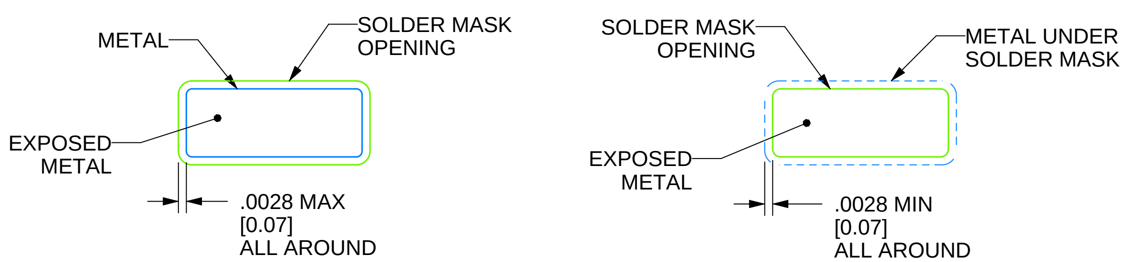


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

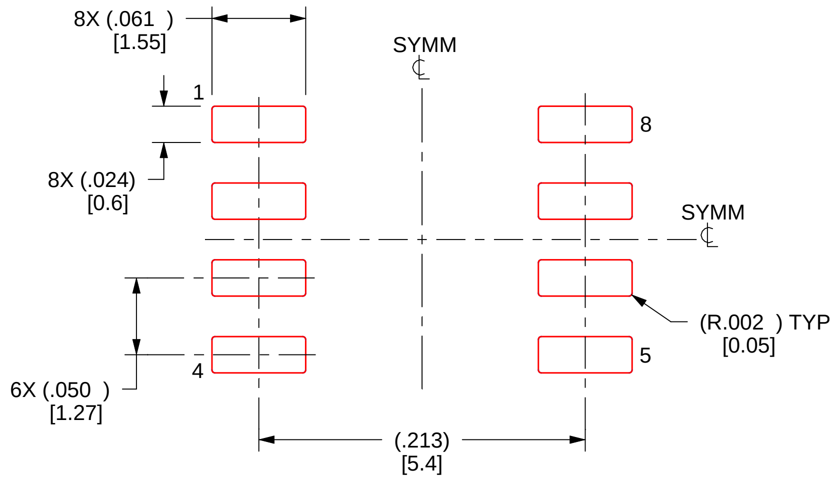
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



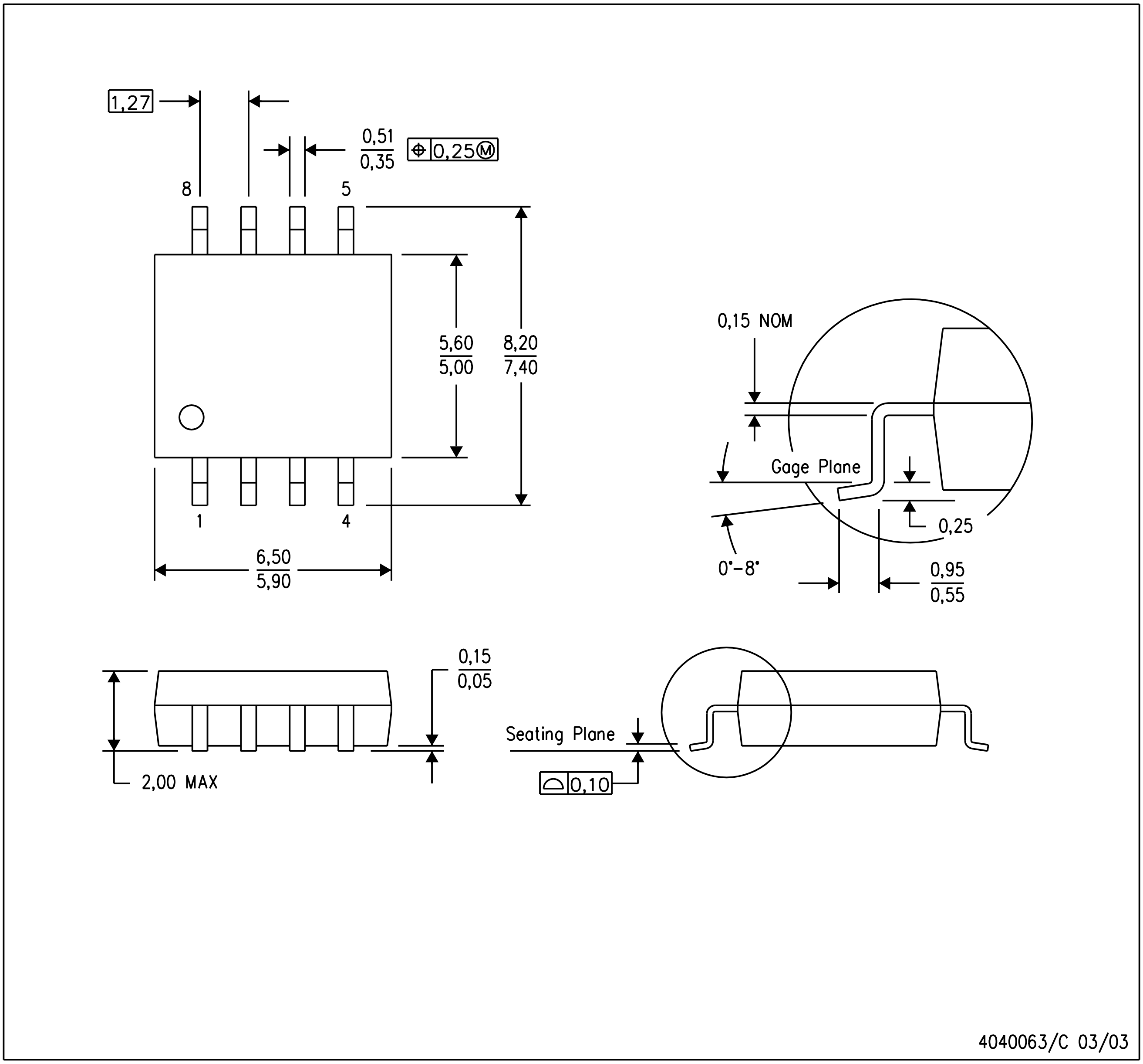
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

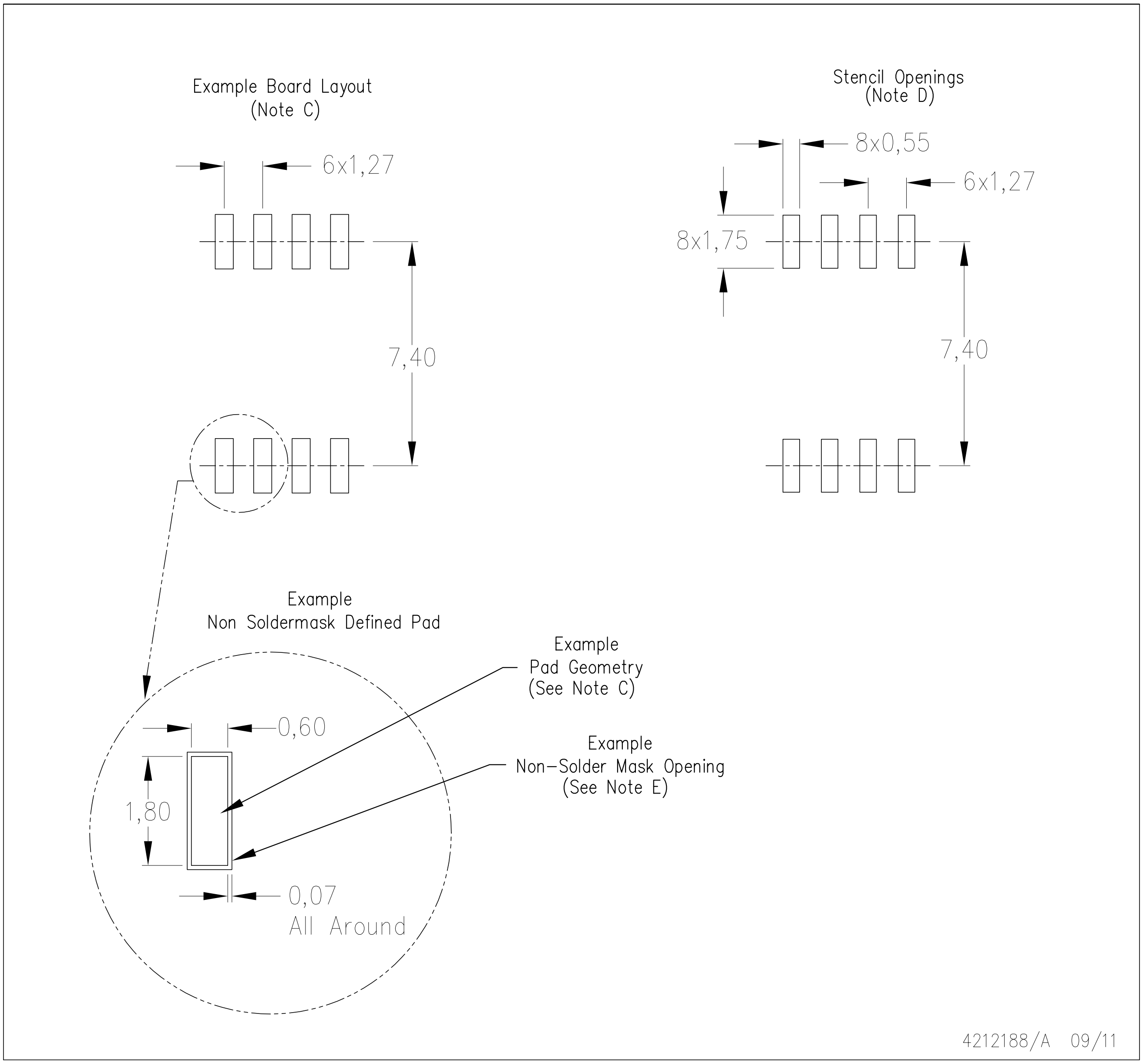
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



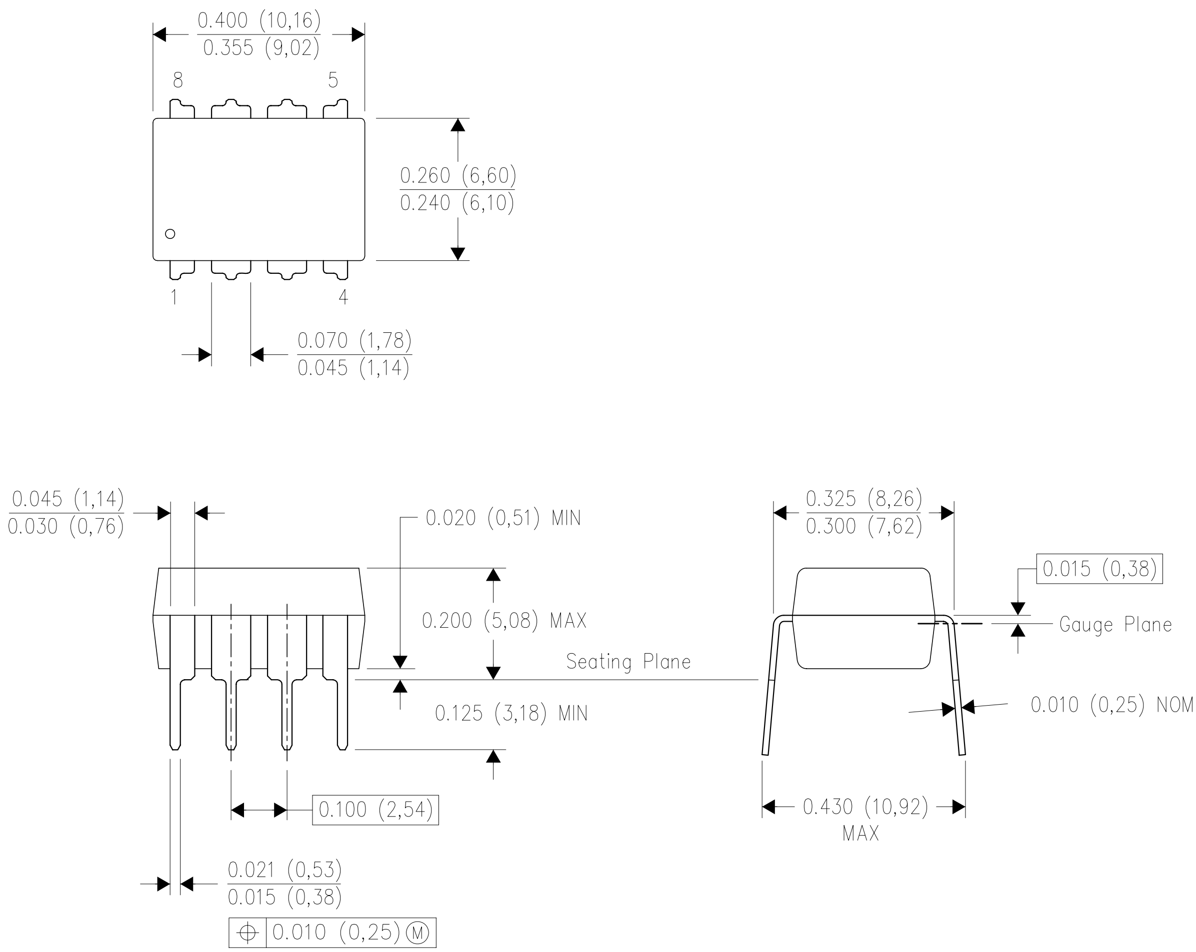
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

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