AFE5818 具有 140mW/通道功耗、0.75nV/√Hz 噪声、14 位 65MSPS 或 12 位 80MSPS ADC 以及 CW 无源混频器的 16 通道超声波模拟前端

1 特性

- 16 通道全套模拟前端：
  - LNA、VCAT、PGA、LPF、ADC和 CW 混频器
- LNA 具有可编程增益：
  - 增益：24dB、18dB 以及 12dB
  - 线性输入范围：$0.25V_{PP}$、$0.5V_{PP}$ 以及 $1V_{PP}$
  - 输入引入噪声：0.63nV/√Hz、0.7nV/√Hz 以及 0.9nV/√Hz
  - 可编程有源终端
- 压控衰减器 (VCAT)：40dB
- 可编程增益放大器 (PGA)：24dB 和 30dB
- 总信号链增益：54dB（最大值）
- 三阶线性相位 LPF：
  - 10MHz、15MHz、20MHz、30MHz、35MHz 以及 50MHz
- 模数转换器 (ADC)：
  - 14 位 ADC：65MSPS 时 75dBFS SNR
  - 12 位 ADC：80MSPS 时 72dBFS SNR
- 低压差分信令 (LVDS) 接口最大速度达 1Gbps
- 噪声和功率优化（全通道）：
  - 0.75nV/√Hz、65MSPS 时每通道 140mW
  - 1.1nV/√Hz、40MSPS 时每通道 91.5mW
  - CW 模式下每通道 80mW
- 出色的器件间增益匹配:
  - ±0.5dB（典型值）和 ±1.1dB（最大值）
- 低谐波失真
- 快速且持续的过载恢复
- CWD 无源混频器：
  - 低近端相位噪声：在偏离 2.5MHz 载波信号 1KHz 时为 –156dBc/Hz
  - 相位分辨率：λ/16
  - 支持 16X、8X、4X 和 1X CW 时钟
  - 三阶和五阶谐波 12dB 抑制
  - CWD 高通滤波器会抑制不良低频信号 < 1kHz
- 小型封装：15mm × 15mm NFBGA-289

2 应用

- 医疗超声波成像
- 无损检测设备
- 声纳成像设备
- 多通道高速数据采集

3 说明

AFE5818 是一套高度集成的模拟前端 (AFE) 解决方案，专用于要求高性能和小尺寸的超声波系统。该器件集成了完整的时间增益控制 (TGC) 成像路径和连续波多普勒 (CWD) 路径。该器件还允许选择多种功率和噪声组合，从而优化系统性能。因此，AFE5818 是一套适合高端便携式系统的超声波 AFE 解决方案。

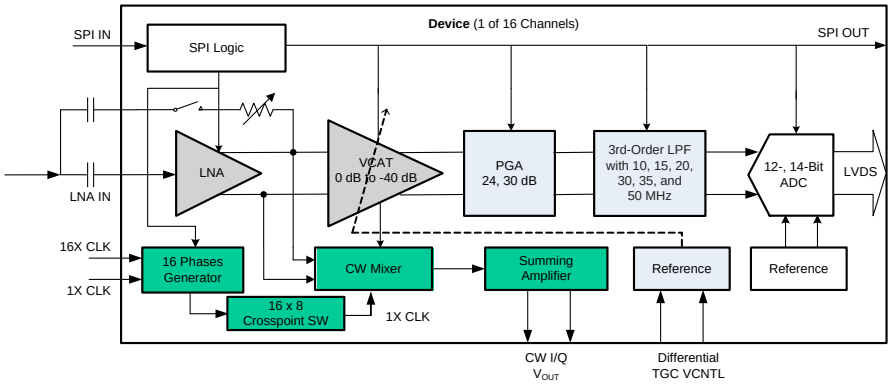
中）

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AFE5818	NFBGA (289)	15.00mm x 15.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

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- 已更改文献编号以将完整版文档发布至 Web ... 1
- Added *Device Comparison Table* ... 5
- Changed the common-mode voltage value from *1.5 V* to *2.5 V* in the descriptions of the CLKM_1X , CLKP_1X, CLKM_16X , and CLKP_16X, rows in the *Pin Functions* table ... 7
- Changed the pulldown resistor value from 100 kΩ to 20-kΩ in the description of the TX_TRIG pin in the *Pin Functions* table ... 10
- Changed *Absolute Maximum Ratings* table: deleted *Voltage at digital inputs* row and added *Voltage at all digital inputs except CW clocks* and *Voltage at CW clock input pins* rows ... 11
- Changed the typical specifications of last four rows of TGC Full-Signal Channel, *Channel-to-channel noise correlation factor* parameter in the *Electrical Characteristics* table ... 14
- Changed test conditions of second row in Power Dissipation, *CW mode* parameter in the *Electrical Characteristics* table ... 18
- Changed SDATA to SDIN in title of *CMOS Digital Inputs* section in the *Digital Characteristics* table ... 19
- Changed typical specification from *25* to *50* in z_0 parameter of *Digital Characteristics* table ... 19
- Changed typical specifications of ADC Timing, C_d parameter in *Output Interface Timing* table ... 20
- Changed Figure 1 ... 21
- Changed Figure 56 and Figure 57 ... 31
- Changed input to *Serial Interface* block from *SDATA* to *SDIN* in *Functional Block Diagram* ... 34
- Changed Figure 84: changed values of t_setup and t_hold ... 55
- Deleted *Setup and Hold Time Constraints for a Hardware RESET* figure and associated description because this data was determined to be misleading ... 55
- Changed input to *Serial Interface* block from *SDATA* to *SDIN* in Figure 98 ... 68
- Changed input to *Serial Interface* block from *SDATA* to *SDIN* in Figure 99 ... 69

修订历史记录 **(**接下页**)**

- Changed *Test Patterns* section to improve clarity 72
- Changed AFE8 to AFE4 in Figure 103 78
- Added footnote to Figure 104 79
- Changed Figure 108 85
- Changed SDATA to SDIN in list of SPI control signals in first paragraph of *Serial Register Map* section 91
- Changed bit type from R/W to W in Register 0 92
- Changed CUSTOM_PATTERN[13:0] to CUSTOM_PATTERN[15:0] in register address 5 of *Table 14* 93
- Changed Register 5 in the *ADC Register Map* section 99

Changes from Original (February 2015) to Revision A **Page**

- 已从文档中删除 AFE58JD18 1
- 已添加 AFE58JD18 至文档 1
- 已更改*压控衰减器 (VCAT)*、*LVDS 接口*最大速度和*噪声和功率优化*（*全通道*） 特性 要点 1
- 已删除*无源混频器*的第二个分项至最后一个分项（ 特性 部分） 1
- 已添加 AFE58JD18 特定的 特性 要点 1
- 已更改*输出接口*和*数字 I/Q 解调器*列的标题（在*器件信息表* 1

5 说明 （续）

AFE5818 共有 16 通道，每通道有一个压控放大器 (VCA)，一个同步采样 14 位和 12 位模数转换器 (ADC) 以及一个连续波 (CW) 混频器。每个 VAC 包含一个低噪声放大器 (LNA)、一个电压控制器衰减器 (VCAT)、一个可编程增益放大器 (PGA) 和一个低通滤波器 (LPF)。LNA 增益可编程，并且支持 250mV$_{PP}$ 至 1V$_{PP}$ 输入信号和可编程有源终端。超低噪声 VCAT 提供 40dB 衰减控制范围并且可改善整体低增益 SNR，这由于有谐波和近场成像。PGA 提供 24dB 和 30dB 增益选项。在 ADC 前，可配置 10MHz、15MHz、20MHz、30MHz、35 MHz 或 50MHz 低通滤波器 (LPF) 来支持不同频率的 各种 超声波应用。

AFE5818 还集成了一个低功耗混频器和一个低噪声混合放大器，用以生成一个片载 CWD 波束形成器。可将 16 个可选相位延迟应用于每个模拟输入信号。此外，器件采用独特的三阶和五阶谐波抑制滤波器来增强 CW 灵敏度。

高性能 14 位 ADC 可实现 75dBFS SNR。该 ADC 可确保在低信号链增益时仍具有出色的 SNR。该器件的最高运行速度为 65MSPS 和 80MSPS，分别提供 14 位和 12 位输出。

ADC 低压差分信令 (LVDS) 输出可实现灵活的系统集成，非常适用于微型系统。

AFE5818 还允许选择多种功率和噪声组合，从而优化系统性能。因此，AFE5818 对于高端系统及便携式系统都是非常理想的超声波 AFE 解决方案。

AFE5818 采用 15mm × 15mm NFBGA-289 封装（ZBV 封装，S-PBGA-N289），额定工作温度范围为 –40°C 至 85°C。这些器件还与 AFE5816 系列器件引脚兼容。

6 Device Comparison Table

DEVICE	DESCRIPTION	PACKAGE	BODY SIZE (NOM)
AFE5816	16-channel, ultrasound, analog front-end (AFE) with 90-mW/channel, 1-nV/√Hz noise, 14-bit, 65-MSPS or 12-bit, 80-MSPS ADC and passive CW mixer	NFBGA (289)	15.00 mm × 15.00 mm
AFE5812	Fully integrated, 8-channel ultrasound AFE with passive CW mixer, and digital I/Q demodulator, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 180 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5809	8-channel ultrasound AFE with passive CW mixer, and digital I/Q demodulator, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 158 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5808A	8-channel ultrasound AFE with passive CW mixer, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 158 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5807	8-channel ultrasound AFE with passive CW mixer, 1.05 nV/√Hz, 12 bits, 80 MSPS, 117 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5803	8-channel ultrasound AFE, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 158 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5805	8-channel ultrasound AFE, 0.85 nV/√Hz, 12 bits, 50 MSPS, 122 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5804	8-channel ultrasound AFE, 1.23 nV/√Hz, 12 bits, 50 MSPS, 101 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5801	8-channel variable-gain amplifier (VGA) with octal high-speed ADC, 5.5 nV/√Hz, 12 bits, 65 MSPS, 65 mW/ch	VQFN (64)	9.00 mm × 9.00 mm
AFE5851	16-channel VGA with high-speed ADC, 5.5 nV/√Hz, 12 bits, 32.5 MSPS, 39 mW/ch	VQFN (64)	9.00 mm × 9.00 mm
VCA5807	8-channel voltage-controlled amplifier for ultrasound with passive CW mixer, 0.75 nV/√Hz, 99 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
VCA8500	8-channel, ultralow-power VGA with low-noise pre-amp, 0.8 nV/√Hz, 65 mW/ch	VQFN (64)	9.00 mm × 9.00 mm
ADS5294	Octal-channel, 14-bit, 80-MSPS ADC, 75-dBFS SNR, 77 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
ADS5292	Octal-channel, 12-bit, 80-MSPS ADC, 70-dBFS SNR, 66 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
ADS5295	Octal-channel, 12-bit, 100-MSPS ADC, 70.6-dBFS SNR, 80 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
ADS5296A	10-bit, 200-MSPS, 4-channel, 61-dBFS SNR, 150-mW/ch and 12-bit, 80-MSPS, 8-channel, 70-dBFS SNR, 65-mW/ch ADC	VQFN (64)	9.00 mm × 9.00 mm

7 Pin Configuration and Functions

ZBV Package
NFBGA-289
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	INP16	INP15	INP14	INP13	INP12	INP11	INP10	INP9	NC	INP8	INP7	INP6	INP5	INP4	INP3	INP2	INP1
B	ACT16	ACT15	ACT14	ACT13	ACT12	ACT11	ACT10	ACT9	NC	ACT8	ACT7	ACT6	ACT5	ACT4	ACT3	ACT2	ACT1
C	INM16	INM15	INM14	INM13	INM12	INM11	INM10	INM9	NC	INM8	INM7	INM6	INM5	INM4	INM3	INM2	INM1
D	CW_DC_INM_IP	CW_DC_INP_IP	CW_IP_AMPINM	CW_IP_AMPINP	CM_BYP1	AVDD_5V	AVDD_5V	AVDD_5V	AVDD_5V	AVDD_5V	AVDD_5V	AVDD_5V	NC	NC	AVSS	AVSS	AVSS
E	CW_DC_OUTP_IP	CW_DC_OUTM_IP	CW_IP_OUTP	CW_IP_OUTM	CM_BYP2	AVDD_3P3	AVDD_3P3	AVSS	AVSS	AVSS	AVDD_3P3	AVDD_3P3	AVDD_3P3	AVDD_3P3	AVSS	CLKP_16X	CLKM_16X
F	CW_DC_OUTP_QP	CW_DC_OUTM_QP	CW_QP_OUTP	CW_QP_OUTM	VHIGH1	AVDD_3P3	AVDD_3P3	AVSS	AVSS	AVSS	AVDD_3P3	AVDD_3P3	AVDD_3P3	AVDD_3P3	AVSS	AVSS	AVSS
G	CW_DC_INM_QP	CW_DC_INP_QP	CW_QP_AMPINM	CW_QP_AMPINP	VHIGH2	AVDD_3P3	AVDD_3P3	AVSS	AVSS	AVSS	AVDD_3P3	AVDD_3P3	NC	NC	AVSS	CLKM_1X	CLKP_1X
H	AVSS	AVSS	AVSS	VCNTLP	NC	AVDD_3P3	AVDD_3P3	AVSS	AVSS	AVSS	AVDD_3P3	AVDD_3P3	NC	NC	NC	SDOUT	NC
J	ADC_CLKP	ADC_CLKM	AVSS	VCNTLM	NC	AVDD_3P3	AVDD_3P3	AVSS	AVSS	AVSS	AVDD_3P3	AVDD_3P3	NC	NC	NC	NC	SCLK
K	AVSS	AVSS	AVSS	NC	NC	AVDD_3P3	AVDD_3P3	AVSS	AVSS	AVSS	AVDD_3P3	AVDD_3P3	NC	NC	NC	NC	SEN
L	NC	NC	DVDD_1P2	NC	AVDD_1P8	AVDD_1P8	AVDD_1P8	AVSS	AVSS	AVSS	AVDD_1P8	AVDD_1P8	AVDD_1P8	NC	NC	SDIN	RESET
M	NC	NC	DVSS	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD_1P2	DVDD_1P2	DVDD_1P2	TX_TRIG	PDN_GBL	PDN_FAST
N	NC	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVDD_1P2	DVDD_1P2	NC
P	NC	DVDD_1P2	DVDD_1P2	DVDD_1P8	DVDD_1P8	DVDD_1P8	DVDD_1P8	DVSS	DVSS	DVSS	DVDD_1P8	DVDD_1P8	DVDD_1P8	DVDD_1P8	DVDD_1P2	DVDD_1P2	NC
R	NC	DOUTP16	DOUTP15	DOUTP14	NC	DOUTM11	DOUTP11	FCLKM	NC	FCLKP	DOUTM6	DOUTP6	NC	DOUTP3	DOUTP2	DOUTP1	NC
T	NC	DOUTM16	DOUTM15	DOUTM14	DOUTP13	DOUTP12	DOUTP10	DOUTP9	DCLKP	DOUTP8	DOUTP7	DOUTP5	DOUTP4	DOUTM3	DOUTM2	DOUTM1	NC
U	NC	NC	NC	NC	DOUTM13	DOUTM12	DOUTM10	DOUTM9	DCLKM	DOUTM8	DOUTM7	DOUTM5	DOUTM4	NC	NC	NC	NC

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ACT16	B1	I	Active-termination input pins for channels 1 to 16. 1-µF capacitors are recommended. Bias voltage = 1.5 V.
ACT15	B2		
ACT14	B3		
ACT13	B4		
ACT12	B5		
ACT11	B6		
ACT10	B7		
ACT9	B8		
ACT8	B10		
ACT7	B11		
ACT6	B12		
ACT5	B13		
ACT4	B14		
ACT3	B15		
ACT2	B16		
ACT1	B17		
ADC_CLKM(1)	J2	I	Differential clock input pin, negative. A single-ended clock is also supported. Connect ADC_CLKM to dc ground when using a single-ended clock. (Common-mode voltage = 0.7 V.)
ADC_CLKP	J1	I	Differential clock input pin, positive. A single-ended clock is also supported. Connect the ADC clock to the ADC_CLKP pin in a single-ended clock. (Common-mode voltage = 0.7 V.)
AVDD_1P8	L5-L7, L11-L13	I	1.8-V analog supply pins for the ADC
AVDD_3P3	E6, E7, E11-E14, F6, F7, F11-F14, G6, G7, G11, G12, H6, H7, H11, H12, J6, J7, J11, J12, K6, K7, K11, K12	I	3.3-V analog supply pins for the low-noise amplifier (LNA), voltage-controlled attenuator (VCAT), programmable gain amplifier (PGA), low-pass filter (LPF), and continuous wave (CW) blocks
AVDD_5V	D6-D12	I	5-V analog supply pins for the LNA, VCAT, PGA, LPF, and CW blocks
AVSS	D15-D17, E8-E10, E15, F8-F10, F15-F17, G8-G10, G15, H1-H3, H8-H10, J3, J8-J10, K1-K3, K8-K10, L8-L10	I	Analog ground pins
CLKM_1X	G16	I	Differential clock inputs for the 1X CW clock, negative. In differential mode, the device forces a 2.5-V common-mode voltage on this pin. A single-ended clock is also supported. In single-ended clock mode, the CLKM_1X pin is internally pulled to ground. In 1X clock mode, this pin is the quadrate-phase 1X CLKM for the CW mixer. When CW mode is not used, this pin can be left floated.
CLKP_1X	G17	I	Differential clock inputs for the 1X CW clock, positive. In differential mode, the device forces a 2.5-V common-mode voltage on this pin. A single-ended clock is also supported. Connect the 1X CW clock to the CLKP_1X pin in a single-ended clock. In 1X clock mode, this pin is the quadrate-phase 1X CLKP for the CW mixer. When CW mode is not used, this pin can be left floated.
CLKM_16X	E17	I	Differential clock inputs for the 32X, 16X, 8X, and 4X CW clocks, negative. In differential mode, the device forces a 2.5-V common-mode voltage on this pin. A single-ended clock is also supported. In single-ended clock mode, the CLKM_16X pin is internally pulled to ground. In 1X CW clock mode, this pin becomes the in-phase 1X CLKM for the CW mixer. When CW mode is not used, this pin can be floated.
CLKP_16X	E16	I	Differential clock inputs for the 32X, 16X, 8X, and 4X CW clocks, positive. A single-ended clock is also supported. Connect the 16X CW clock to the CLKP_16X pin in a single-ended clock. In 1X CW clock mode, this pin becomes the in-phase 1X CLKP for the CW mixer. In differential mode, the device forces a 2.5-V common-mode voltage on this pin. When CW mode is not used, this pin can be floated.
CM_BYP1	D5	O	Bypass to ground with a ≥ 1-µF capacitor. To suppress ultra low-frequency noise, a 10-µF capacitor can be used. Bias voltage = 1.5 V.
CM_BYP2	E5		

(1) M = negative, P = positive.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
CW_DC_INM_IP	D1	I	In-phase CW high-pass filter differential inputs. An external capacitor must be connected between CW_DC_INM_IP, CW_DC_OUTP_IP and CW_DC_INP_IP, CW_DC_OUTM_IP. When CW high-pass filter (HPF) mode is not used, these pins can be floated. Bias voltage = 1.5 V.
CW_DC_INP_IP	D2		
CW_DC_INM_QP	G1	I	Quadrature-phase CW high-pass filter differential inputs. An external capacitor must be connected between CW_DC_INM_QP, CW_DC_OUTP_QP and CW_DC_INP_QP, CW_DC_OUTM_QP. When CW HPF mode is not used, these pins can be floated. Bias voltage = 1.5 V.
CW_DC_INP_QP	G2		
CW_DC_OUTM_IP	E2	O	In-phase CW high-pass filter differential outputs. An external capacitor must be connected between CW_DC_INM_IP, CW_DC_OUTP_IP and CW_DC_INP_IP, CW_DC_OUTM_IP. When CW HPF mode is not used, these pins can be floated. Bias voltage = 1.5 V.
CW_DC_OUTP_IP	E1		
CW_DC_OUTM_QP	F2	O	Quadrature-phase CW high-pass filter differential outputs. An external capacitor must be connected between CW_DC_INM_QP, CW_DC_OUTP_QP and CW_DC_INP_QP, CW_DC_OUTM_QP. When CW HPF mode is not used, these pins can be floated. Bias voltage = 1.5 V.
CW_DC_OUTP_QP	F1		
CW_IP_AMPINM	D3	I	In-phase CW summing amplifier differential inputs. An external capacitor must be connected between CW_IP_AMPINM, CW_IP_OUTP and CW_IP_AMPINP, CW_IP_OUTM. When CW HPF mode is not used, these pins can be floated. Bias voltage = 1.5 V.
CW_IP_AMPINP	D4		
CW_IP_OUTM	E4	O	In-phase CW summing amplifier differential outputs. An external capacitor must be connected between CW_IP_AMPINM, CW_IP_OUTP and CW_IP_AMPINP, CW_IP_OUTM. When CW HPF mode is not used, these pins can be floated. Bias voltage = 1.5 V.
CW_IP_OUTP	E3		
CW_QP_AMPINM	G3	I	Quadrature-phase CW summing amplifier differential inputs. An external capacitor must be connected between CW_QP_AMPINM, CW_QP_OUTP and CW_QP_AMPINP, CW_QP_OUTM. When CW mode is not used, these pins can be floated. Bias voltage = 1.5 V.
CW_QP_AMPINP	G4		
CW_QP_OUTM	F4	O	Quadrature-phase CW summing amplifier differential outputs. An external capacitor must be connected between CW_QP_AMPINM, CW_QP_OUTP and CW_QP_AMPINP, CW_QP_OUTM. When CW mode is not used, these pins can be floated. Bias voltage = 1.5 V.
CW_QP_OUTP	F3		
DCLKM	U9	O	Low-voltage differential signaling (LVDS) serialized data clock outputs (receiver bit alignment)
DCLKP	T9		
DOUTM1	T16	O	LVDS serialized differential data outputs for channel 1
DOUTP1	R16		
DOUTM2	T15	O	LVDS serialized differential data outputs for channel 2
DOUTP2	R15		
DOUTM3	T14	O	LVDS serialized differential data outputs for channel 3
DOUTP3	R14		
DOUTM4	U13	O	LVDS serialized differential data outputs for channel 4
DOUTP4	T13		
DOUTM5	U12	O	LVDS serialized differential data outputs for channel 5
DOUTP5	T12		
DOUTM6	R11	O	LVDS serialized differential data outputs for channel 6
DOUTP6	R12		
DOUTM7	U11	O	LVDS serialized differential data outputs for channel 7
DOUTP7	T11		
DOUTM8	U10	O	LVDS serialized differential data outputs for channel 8
DOUTP8	T10		
DOUTM9	U8	O	LVDS serialized differential data outputs for channel 9
DOUTP9	T8		
DOUTM10	U7	O	LVDS serialized differential data outputs for channel 10
DOUTP10	T7		
DOUTM11	R6	O	LVDS serialized differential data outputs for channel 11
DOUTP11	R7		
DOUTM12	U6	O	LVDS serialized differential data outputs for channel 12
DOUTP12	T6		

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DOUTM13	U5	O	LVDS serialized differential data outputs for channel 13
DOUTP13	T5		
DOUTM14	T4	O	LVDS serialized differential data outputs for channel 14
DOUTP14	R4		
DOUTM15	T3	O	LVDS serialized differential data outputs for channel 15
DOUTP15	R3		
DOUTM16	T2	O	LVDS serialized differential data outputs for channel 16
DOUTP16	R2		
DVDD_1P2	L3, M4-M6, M12-M14, N2-N6, N12-N16, P2, P3, P15, P16	I	1.2-V digital supply pins for the ADC digital block
DVDD_1P8	P4-P7, P11-P14	I	1.8-V digital supply pins for the ADC digital, digital I/Os, phase-locked loop (PLL), and LVDS interface blocks
DVSS	M3, M7-M11, N7-N11, P8-P10	I	ADC digital ground
FCLKM	R8	O	LVDS serialized frame clock outputs (receiver word alignment)
FCLKP	R10		
INM1	C17	I	Complimentary analog inputs for channel 1. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP1	A17	I	Analog inputs for channel 1. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM2	C16	I	Complimentary analog inputs for channel 2. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP2	A16	I	Analog inputs for channel 2. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM3	C15	I	Complimentary analog inputs for channel 3. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP3	A15	I	Analog inputs for channel 3. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM4	C14	I	Complimentary analog inputs for channel 4. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP4	A14	I	Analog inputs for channel 4. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM5	C13	I	Complimentary analog inputs for channel 5. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP5	A13	I	Analog inputs for channel 5. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM6	C12	I	Complimentary analog inputs for channel 6. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP6	A12	I	Analog inputs for channel 6. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM7	C11	I	Complimentary analog inputs for channel 7. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP7	A11	I	Analog inputs for channel 7. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM8	C10	I	Complimentary analog inputs for channel 8. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP8	A10	I	Analog inputs for channel 8. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM9	C8	I	Complimentary analog inputs for channel 9. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
INP9	A8	I	Analog inputs for channel 9. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM10	C7	I	Complimentary analog inputs for channel 10. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP10	A7	I	Analog inputs for channel 10. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM11	C6	I	Complimentary analog inputs for channel 11. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP11	A6	I	Analog inputs for channel 11. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM12	C5	I	Complimentary analog inputs for channel 12. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP12	A5	I	Analog inputs for channel 12. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM13	C4	I	Complimentary analog inputs for channel 13. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP13	A4	I	Analog inputs for channel 13. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM14	C3	I	Complimentary analog inputs for channel 14. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP14	A3	I	Analog inputs for channel 14. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM15	C2	I	Complimentary analog inputs for channel 15. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP15	A2	I	Analog inputs for channel 15. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
INM16	C1	I	Complimentary analog inputs for channel 16. Place a ≥ 15-nF capacitor to ground. The HPF response of the LNA depends on the capacitors. Bias voltage = 2.2 V.
INP16	A1	I	Analog inputs for channel 16. AC-couple to inputs with 0.1-µF capacitors. Bias voltage = 2.2 V.
NC	A9, B9, C9, D13, D14, G13, G14, H5, H13-H15, H17, J5, J13-J16, K4, K5, K13-K16, L1, L2, L4, L14, L15, M1, M2, N1, N17, P1, P17, R1, R5, R9, R13, R17, T1, T17, U1-U4,U14-U17	—	Unused pins. Do not connect.
PDN_FAST	M17	I	Partial power-down control pin for the entire device with an internal 16-kΩ pulldown resistor; active high. Note that a 1.8-V logic level is recommended.
PDN_GBL	M16	I	Global (complete) power-down control pin for the entire device with an internal 16-kΩ pulldown resistor; active high. Note that a 1.8-V logic level is required.
RESET	L17	I	Hardware reset pin with an internal 16-kΩ pulldown resistor; active high. Note that a 1.8-V logic level is required.
SCLK	J17	I	Serial interface clock pin with an internal 16-kΩ pulldown resistor. Note that a 1.8-V logic level is required.
SDIN	L16	I	Serial interface data pin with an internal 16-kΩ pulldown resistor. Note that a 1.8-V logic level is required.
SDOUT	H16	O	Serial interface readout pin for channels 1 to 16. This pin is in tri-state by default. Note that a 1.8-V logic level is required.
SEN	K17	I	Serial interface enable, active low. This pin has a 16-kΩ pullup resistor. Note that a 1.8-V logic level is required.
TX_TRIG	M15	I	This pin synchronizes test patterns across devices. This pin has a 20-kΩ pulldown resistor. Note that a 1.8-V logic level is required.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VCNTLM	J4	I	Differential attenuation control pins
VCNTLP	H4		
VHIGH1	F5	O	Bypass to ground with a ≥ 1-µF capacitor. Bias voltage = 1 V.
VHIGH2	G5		

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage	AVDD_1P8	–0.3	2.2	V
	AVDD_3P3	–0.3	3.9	
	AVDD_5V	–0.3	6	
	DVDD_1P2	–0.3	1.35	
	DVDD_1P8	–0.3	2.2	
Voltage at analog inputs		–0.3	minimum [3.6, AVDD_3P3 + 0.3]	V
Voltage at all digital inputs except CW clocks		–0.3	minimum [2.2, DVDD_1P8 + 0.3]	V
Voltage at CW clock input pins		–0.3	minimum [6, AVDD_5V + 0.3]	V
Temperature	Peak solder temperature(2)		260	°C
	Maximum junction temperature (T_J), any condition		105	
	Operating, T_A	–40	85	
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device complies with JSTD-020D.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT
AVDD_1P8 voltage	1.7	1.9	V
AVDD_3P3 voltage	3.15	3.6	V
AVDD_5V voltage	4.75	5.25	V
DVDD_1P2 voltage	1.15	1.25	V
DVDD_1P8 voltage	1.7	1.9	V
VCNTLP – VCNTLM	0	1.5	V
Sample rate	5	80(1)	MHz
Ambient temperature, T_A	–40	85	°C

(1) The maximum speed supported is a function of ADC resolution. The number specified is for 12-bit mode.

8.4 Thermal Information

THERMAL METRIC(1)		AFE5818 ZBV (NFBGA) 289 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
TGC FULL-SIGNAL CHANNEL (VGA + LPF + ADC)							
en (RTI)	Input voltage noise over LNA gain	Low-noise mode, R_S = 0 Ω, f = 2 MHz, PGA = 24 dB	LNA = 24 dB		0.76		nV/√Hz
			LNA = 18 dB		0.87		
			LNA = 12 dB		1.19		
		Low-noise mode, R_S = 0 Ω, f = 2 MHz, PGA = 30 dB	LNA = 24 dB		0.75		
			LNA = 18 dB		0.84		
			LNA = 12 dB		1.15		
		Low-power mode, R_S = 0 Ω, f = 2 MHz, PGA = 24 dB	LNA = 24 dB		1.1		
			LNA = 18 dB		1.2		
			LNA = 12 dB		1.7		
		Low-power mode, R_S = 0 Ω, f = 2 MHz, PGA = 30 dB	LNA = 24 dB		1.1		
			LNA = 18 dB		1.2		
			LNA = 12 dB		1.6		
		Medium-power mode, R_S = 0 Ω, f = 2 MHz, PGA = 24 dB	LNA = 24 dB		1		
			LNA = 18 dB		1.1		
			LNA = 12 dB		1.3		
		Medium-power mode, R_S = 0 Ω, f = 2 MHz, PGA = 30 dB	LNA = 24 dB		0.95		
			LNA = 18 dB		1		
			LNA = 12 dB		1.25		
	Input-referred current noise	Low-noise mode			3.2		pA/√Hz
		Medium-power mode			2.7		
		Low-power mode			2.3		
NF	Noise figure	LNA = 18 dB, R_S = 50 Ω, no active termination	Low-noise mode		2.4		dB
			Medium-power mode		3.2		
			Low-power mode		3.7		
			Low-noise figure mode		3.4		
		LNA = 18 dB, R_S = 400 Ω, no active termination	Low-noise mode		1.2		
			Medium-power mode		1.2		
			Low-power mode		1.2		
			Low-noise figure mode		0.83		
VMAX	Maximum linear input voltage	LNA gain = 24 dB			250		mV_{PP}
		LNA gain = 18 dB			500		
		LNA gain = 12 dB			1000		
	Input clamp voltage in auto clamp mode	LNA gain = 24 dB			350		mV_{PP}
		LNA gain = 18 dB			600		
		LNA gain = 12 dB			1150		
	PGA gain	Low-noise mode			24		dB
					30		
		Medium-power and low-power modes			24		
					27.5		
	Total gain	LNA = 24 dB, PGA = 30 dB, low-noise mode			54		dB
		LNA = 24 dB, PGA = 30 dB, medium-power mode			51.5		
		LNA = 24 dB, PGA = 30 dB, low-power mode			51.5		

Electrical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
TGC FULL-SIGNAL CHANNEL (continued)							
	Channel-to-channel noise correlation factor(1)	Without a signal			–20		dB
		With a signal, full band	VCNTLP = 0 V		–10		
			VCNTLP = 0.8 V		–10		
		With a signal, 1-MHz band over carrier	VCNTLP = 0 V		–10		
			VCNTLP = 0.8 V		–3.75		
SNR	Signal-to-noise ratio	VCNTLP = 0.6 V (22-dB total channel gain)		65.7	68.5		dBFS
		VCNTLP = 0 V, LNA = 18 dB, PGA = 24 dB		59.3	62.5		
		VCNTLP = 0 V, LNA = 24 dB, PGA = 24 dB			58		
	Narrow-band SNR	SNR over 2-MHz band around carrier at VCNTLP = 0.6 V (22-dB total gain)		73.8	77		dBFS
	Input common-mode voltage	At INP and INM pins			2.2		V
	Input resistance	At dc			8		kΩ
		Preset active termination enabled(2), across GBL_ACTIVE_TERM (register 196, bits 7-6) register settings; see Table 74			50		Ω
					100		
					200		
					400		
	Input capacitance				20		pF
	Input control voltage	VCNTLP – VCNTLM		0		1.5	V
	Common-mode voltage	VCNTLP and VCNTLM			0.75		V
	Tolerable noise at VCNTLP – VCNTLM	For summation of 16 channels; see Figure 69			6		nV/√Hz
		For summation of 64 channels; see Figure 69			3		
	Gain range				–40		dB
	Gain slope	VCNTLP = 0.1 V to 0.9 V			35		dB/V
	Input resistance	Between VCNTLP and VCNTLM			200		kΩ
	Input capacitance	Between VCNTLP and VCNTLM			1		pF
	TGC response time	VCNTLP = 0-V to 1.5-V step function			1.5		µs
	3rd-order, low-pass filter	–1-dB cutoff frequency across LPF_RPOG (register 195, bits 3-0) register settings; see Table 72			10		MHz
					15		
					20		
					30		
					35		
					50		
	Settling time	For change in LNA gain			14		µs
		For change in active termination setting			10		

(1) The noise-correlation factor is defined as $10 \times \log_{10}[Nc / (Nu + Nc)]$, where Nc is the correlated noise power in a single channel and Nu is the uncorrelated noise power in a single channel. The noise-correlation factor measurement is described by the equation:
Nc / (Nu + Nc) = N_16CH / N_1CH / 240 – 1 / 15,
where N_16CH is the noise power of the summed 16 channels and N_1CH is the noise power of one channel.
(2) Total device input impedance is given by the parallel combination of the mentioned active termination resistance and a passive resistance of 15 kΩ.

Electrical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
AC ACCURACY							
	LPF bandwidth tolerance				±5%		
	Channel-to-channel group delay variation	2 MHz to 15 MHz			2		ns
	Channel-to-channel phase variation	15-MHz signal			11		Degrees
	Gain matching	0 V < VCNTLP < 0.1 V (device-to-device)			±0.5		dB
		0.1 V < VCNTLP < 1.1 V (device-to-device)		–1.1	±0.5	1.1	
		1.1 V < VCNTLP < 1.5 V (device-to-device)			±0.5		
	Output offset			–120		120	LSB
AC PERFORMANCE							
HD2	Second-harmonic distortion	Input frequency = 2 MHz, output amplitude = –1 dBFS			–60		dBc
		Input frequency = 5 MHz, output amplitude = –1 dBFS			–60		
		Input frequency = 5 MHz, output amplitude = –1 dBFS, input amplitude = 500 mV_{PP}, LNA = 18 dB, VCNTLP = 0.88 V			–55		
		Input frequency = 5 MHz, output amplitude = –1 dBFS, input amplitude = 250 mV_{PP}, LNA = 24 dB, VCNTLP = 0.88 V			–55		
HD3	Third-harmonic distortion	Input frequency = 2 MHz, output amplitude = –1 dBFS			–55		dBc
		Input frequency = 5 MHz, output amplitude = –1 dBFS			–55		
		Input frequency = 5 MHz, output amplitude = –1 dBFS, input amplitude = 500 mV_{PP}, LNA = 18 dB, VCNTLP = 0.88 V			–55		
		Input frequency = 5 MHz, output amplitude = –1 dBFS, input amplitude = 250 mV_{PP}, LNA = 24 dB, VCNTLP = 0.88 V			–55		
THD	Total harmonic distortion	Input frequency = 2 MHz, output amplitude = –1 dBFS			–55		dBc
		Input frequency = 5 MHz, output amplitude = –1 dBFS			–55		
IMD3	Intermodulation distortion	Input frequency 1 = 5 MHz at –1 dBFS, input frequency 2 = 5.01 MHz at –27 dBFS			–60		dBc
	Fundamental crosstalk	Signal applied to single channel			-60		dBFS
	Phase noise	1 kHz off 5-MHz carrier (VCNTLP = 0 V)			–132		dBc/√Hz
LOW-NOISE AMPLIFIER (LNA)							
HPF	High-pass filter	–3-dB cutoff frequency for INMx capacitor = 15 nF, across LNA_HPF_PROG (register 203, bits 3-2) and RED_LNA_HPF_3X (register 205, bit 8) register settings; see Table 89 and Table 91			16		kHz
					50		
					100		
					150		
					200		
	Input-referred voltage noise	R_S = 0 Ω, f = 2 MHz, R_{IN} = high-Z	LNA gain = 24 dB		0.63		nV/√Hz
			LNA gain = 18 dB		0.70		
			LNA gain = 12 dB		0.9		
	LNA linear output				4		V_{PP}
VCAT + PGA							
	VCAT input noise	0-dB attenuation			2		nV/√Hz
		–40-dB attenuation			10.5		
	PGA input noise	24-dB and 30-dB attenuation			1.75		nV/√Hz
	–3-dB HPF cutoff frequency				80		kHz

Electrical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
CW DOPPLER							
en (RTI)	Input voltage noise (CW)	1 channel mixer, LNA = 24 dB, 500-Ω external feedback resistor			0.98		nV/√Hz
		16 channel mixers, LNA = 24 dB, 32-Ω external feedback resistor			0.31		
		1 channel mixer, LNA = 18 dB, 500-Ω external feedback resistor			1.31		
		16 channel mixers, LNA = 18 dB, 32-Ω external feedback resistor			0.5		
en (RTO)	Output voltage noise (CW)	1 channel mixer, LNA = 24 dB, 500-Ω external feedback resistor			13.3		nV/√Hz
		16 channel mixers, LNA = 24 dB, 32-Ω external feedback resistor			3.56		
		1 channel mixer, LNA = 18 dB, 500-Ω external feedback resistor			8.85		
		16 channel mixers, LNA = 18 dB, 32-Ω external feedback resistor			2.86		
NF	Noise figure	R_S = 100 Ω, R_{IN} = high-Z, f_{IN} = 2 MHz, 1 channel, LNA = 18 dB			3.18		dB
		R_S = 100 Ω, R_{IN} = high-Z, f_{IN} = 2 MHz, 16 channels, LNA = 18 dB			6.15		
	CW operating range	CW signal carrier frequency			8		MHz
CWCLK	CW clock frequency	CLKP_1X, CLKM_1X (16X mode)				8	MHz
		CLKP_16X, CLKM_16X (16X mode)				128	
		CLKP_16X, CLKM_16X (4X mode)			32		
	Clock amplitude (ac-coupled)	CLKM_1X, CLKP_1X and CLKM_16X, CLKP_16X		0.2	0.35		V_{PP}
	CLK duty cycle	1X and 16X CLKs		35%		65%	
	Common-mode voltage	Internally provided			2.5		V
	V_{CMOS} CMOS input clock amplitude			4		5	V
	CW mixer conversion loss				4		dB
	CW mixer phase noise	1 kHz off 2-MHz carrier (16X mode, 1 channel)			156		dBc/Hz
		1 kHz off 2-MHz carrier (16X mode, 16 channel)			161		
DR	Input dynamic range	Input frequency = 2.5 MHz	LNA = 24 dB		159.1		dBFS/Hz
			LNA = 18 dB		162.6		
			LNA = 12 dB		164.4		
IMD3	Intermodulation distortion	f_1 = 5 MHz, f_2 = 5.01 MHz, both tones at –16-dBm amplitude, 16 channels summed up in-phase, CW feedback resistor = 32 Ω			–50		dBc
		f_1 = 5 MHz, f_2 = 5.01 MHz, both tones at –16-dBm amplitude, single channel summed up in-phase, CW feedback resistor = 500 Ω			–60		
	I/Q channel gain matching	16X mode			±0.04		dB
		4X mode			±0.04		
	I/Q channel phase matching	16X mode			±0.01		Degrees
		4X mode			±0.01		
	Image rejection ratio				–50		dBc

Electrical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
CW SUMMING AMPLIFIER							
	Output common-mode voltage	Internally provided			1.5		V
	Summing amplifier output				4		V_{PP}
	Input-referred voltage noise	At 100 Hz			1.6		nV/√Hz
		At 1 kHz			0.9		
		At 2 kHz to 100 MHz			0.8		
	Input-referred current noise				3.75		pA/√Hz
	Unity-gain bandwidth				150		MHz
	Maximum output current				50		mA_{PP}
ADC SPECIFICATIONS (Clock Input)							
	Sample rate	14-bit rate		5		65	MSPS
		12-bit rate		5		80	
	Input clock amplitude differential (ADC_CLKP – ADC_CLKM)	Sine-wave, ac-coupled			1.5		V_{PP}
		LVPECL, ac-coupled			1.6		
		LVDS, ac-coupled		0.3			
	Input clock CMOS amplitude single-ended (ADC_CLKP)	High-level input voltage (V_{IH})		1.5			V
		Low-level input voltage (V_{IL})				0.3	
	Input clock duty cycle			35%	50%	65%	
ADC SPECIFICATIONS (Signal-to-Noise Ratio)							
SNR	Signal-to-noise ratio	14-bit ratio	Without signal		75		dBFS
			With full-scale signal		72.5		
		12-bit ratio	Without signal		72		
			With full-scale signal		69.5		
ADC SPECIFICATIONS (Analog Input)							
	ADC input full-scale range				2		V_{PP}
	LVDS rate					1000	Mbps
POWER DISSIPATION							
	AVDD_1P8 voltage			1.7	1.8	1.9	V
	AVDD_3P3 voltage			3.15	3.3	3.6	V
	AVDD_5V voltage			4.75	5	5.25	V
	DVDD_1P2 voltage			1.15	1.2	1.25	V
	DVDD_1P8 voltage			1.7	1.8	1.9	V

Electrical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.

PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
POWER DISSIPATION (continued)						
TGC mode (Total power dissipation per channel)	TGC low-noise mode, no signal	ADC in 12-bit resolution, 80 MSPS		143	170	mW/Ch
		ADC in 14-bit resolution, 65 MSPS		140		
		ADC in 14-bit resolution, 50 MSPS		136		
		ADC in 14-bit resolution, 40 MSPS		134		
	TGC low-noise mode, 500-mV_{PP} input,1% duty cycle			139.5		
	TGC medium-power mode			104.4		
	TGC medium-power mode, 500-mV_{PP} input, 1% duty cycle			107.4		
	TGC low-power mode			93.5		
	TGC low-power, 500-mV_{PP} input, 1% duty cycle			96		
CW mode (Total power dissipation per channel with ADC and PGA in power-down state)	CW mode, no signal, ADC shutdown CW mode	16X clock = 32 MHz		80		mW/Ch
		16X clock = 80 MHz		95	112	
	CW mode, 16X clock = 80 MHz, CW summing amplifier external feedback resistance = 33 Ω, 500-mV_{PP} input to all 16 channels, ADC shutdown			203		
AVDD_3P3 current	TGC low-noise mode, no signal			414	467	mA
	TGC medium-power mode, no signal			260		
	TGC low-power mode, no signal			207		
	CW mode, no signal	16X clock = 32 MHz		285		
		16X clock = 80 MHz		285	337	
	TGC low-noise mode, 500-mV_{PP} input, 1% duty cycle			430		
	TGC medium-power mode, 500-mV_{PP} input, 1% duty cycle			274		
	TGC low-power mode, 500-mV_{PP} input, 1% duty cycle			219		
	CW mode, 16X clock = 80 MHz, 500-mV_{PP} input to all 16 channels			740		
AVDD_5V current	TGC low-noise, medium-power, or low-power mode, no signal			57	80	mA
	CW mode, no signal	16X clock = 32 MHz		64		
		16X clock = 80 MHz		115	136	
	TGC, low-noise, medium-power, or low-power mode, 500-mV_{PP} input, 1% duty cycle			57		
	CW mode, 16X clock = 80 MHz, 500-mV_{PP} input to all 16 channels			160		
AVDD_1P8 current	12-bit mode	80 MSPS		170	197	mA
		20 MSPS		120		
	14-bit mode	65 MSPS		160		
		20 MSPS		120		
DVDD_1P2 current	12-bit mode	80 MSPS		110	160	mA
		20 MSPS		50		
	14-bit mode	65 MSPS		95		
		20 MSPS		52		
DVDD_1P8 current	12-bit mode	80 MSPS		100	132	mA
		20 MSPS		85		
	14-bit mode	65 MSPS		95		
		20 MSPS		85		

Electrical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
POWER-DOWN							
	Power dissipation in power-down mode	Partial power-down when PDN_FAST = high (1.8 V)			28		mW/Ch
		Complete power-down when PDN_GBL = high (1.8 V)			2.2		
	Power-down response time				1		µs
	Power-up response time	Partial power-down when PDN_FAST= high (1.8 V) and the device in partial power-down time for < 500 µs			3		µs
		Complete power-down when PDN_GBL = high (1.8 V)			2.7		ms
PSMR	Power-supply modulation ratio	f_{IN} = 5 MHz, supply tone of 100 mV_{PP} at 1-kHz frequency	AVDD_3P3		–65		dBc
			AVDD_5V		–63		
PSRR	Power-supply rejection ratio(3)	Supply tone of 100 mV_{PP} at 1-kHz frequency	AVDD_3P3		–70		dBc
			AVDD_5V		–70		

(3) The PSRR value in dBc is measured with respect to the supply tone amplitude applied at the device supply (that is, 100 mV_{PP}).

8.6 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. Typical values are at T_A = 25°C, minimum and maximum values are across the full temperature range of T_{MIN} = -40°C to T_{MAX} = 85°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, external differential load resistance between the LVDS output pair, and R_{LOAD} = 100 Ω, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOAD RESISTANCE						
	External differential load resistance	Between LVDS output pair		100		Ω
CMOS DIGITAL INPUTS (PDN_GBL, PDN_FAST, RESET, SCLK, SDIN, SEN)						
V_{IH}	High-level input voltage		1.4		2.1	V
V_{IL}	Low-level input voltage		0		0.3	V
I_{IH}	High-level input current			100		µA
I_{IL}	Low-level input current			100		µA
C_i	Input capacitance			4		pF
LVDS DIGITAL OUTPUTS (DOUTPx, DOUTMx)(1)						
$\|V_{OD}\|$	Output differential voltage			420		mV
V_{OS}	Output offset voltage	Common-mode voltage of DOUTPx and DOUTMx		1.03		V
CMOS DIGITAL OUTPUT (SDOUT)						
V_{OH}	High-level output voltage		1.4		DVDD_1P8	V
V_{OL}	Low-level output voltage		DVSS		0.3	V
z_o	Output impedance			50		Ω

(1) All LVDS specifications are characterized but are not tested at production.

8.7 Output Interface Timing

Typical values are at T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, differential ADC clock, LVDS load C_{LOAD} = 5 pF, R_{LOAD} = 100 Ω, 14-bit ADC resolution, and sample rate = 65 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C.

			MIN	TYP	MAX	UNIT
GENERAL						
t_{AP}	Aperture delay(1)			1.6		ns
δt_{AP}	Aperture delay variation from device to device (at same temperature and supply)			±0.5		ns
t_{APJ}	Aperture jitter with LVPECL clock as input clock			0.5		ps
	Wake-up time	Time to valid data after exiting standby mode (units are in number of ADC_CLKP, ADC_CLKM cycles)		15		Cycles
		Time to valid data after exiting PDN_GBL mode		1		ms
		Time to valid data after stopping and restarting the input clock		100		µs
ADC TIMING						
C_d	ADC latency	Default after reset(1)		8.5		ADC clocks
		Low-latency mode		4.5		
LVDS TIMING(2)						
f_F	Frame clock frequency(1)			f_{CLKIN}		MHz
D_{FRAME}	Frame clock duty cycle			50%		
N_{SER}	Number of bits serialization of each ADC word		12		16	Bits
f_D	Output rate of serialized data	1X output data rate mode		$N_{SER} \times f_{CLKIN}$	1000	Mbps
		2X output data rate mode		$2 \times N_{SER} \times f_{CLKIN}$	1000	
f_B	Bit clock frequency			f_D / 2	500	MHz
D_{BIT}	Bit clock duty cycle			50%		
t_D	Data bit duration(1)		1	1000 / f_D		ns
t_{PDI}	Clock propagation delay(1)			6 × t_D + 5		ns
δt_{PROP}	Clock propagation delay variation from device to device (at same temperature and supply)			±2		ns
t_{ORF}	DOUT, DCLK, FCLK rise and fall time, transition time between –100 mV and +100 mV			0.2		ns
t_{OSU}	Minimum serial data, serial clock setup time(1)			t_D / 2 – 0.4		ns
t_{OH}	Minimum serial data, serial clock hold time(1)			t_D / 2 – 0.4		ns
t_{DV}	Minimum data valid window(3)(1)			t_D – 0.65		ns
TX_TRIG TIMING						
$t_{TX\_TRIG\_DEL}$	Delay between TX_TRIG and TX_TRIGD(4)		0.5		0.4 × t_{CLKIN}(5)	ns
$t_{SU\_TX\_TRIGD}$	Setup time related to latching TX_TRIGD relative to the rising edge of the system clock			0.6		ns
$t_{H\_TX\_TRIGD}$	Hold time related to latching TX_TRIGD relative to the rising edge of the system clock			0.4		ns

(1) See Figure 1.
(2) All LVDS specifications are characterized but are not tested at production.
(3) The specification for the minimum data valid window is larger than the sum of the minimum setup and hold times because there can be a skew between the ideal transitions of the serial output data with respect to the transition of the bit clock. This skew can vary across channels and across devices. A mechanism to correct this skew can therefore improve the setup and hold timing margins. For example, the LVDS_DCLK_DELAY_PROG control can be used to shift the relative timing of the bit clock with respect to the data.
(4) TX_TRIGD is the internally delayed version of TX_TRIG that gets latched on the rising edge of the ADC clock.
(5) t_{CLKIN} is the ADC clock period in nanoseconds (ns).

8.8 Serial Interface Timing Characteristics

Typical values are at T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, and DVDD_1P8 = 1.8 V, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = 85°C.

		MIN	TYP	MAX	UNIT
t_{SCLK}	SCLK period	50			ns
t_{SCLK_H}	SCLK high time	20			ns
t_{SCLK_L}	SCLK low time	20			ns
t_{DSU}	Data setup time	5			ns
t_{DHO}	Data hold time	5			ns
t_{SEN_SU}	SEN falling edge to SCLK rising edge	8			ns
t_{SEN_HO}	Time between last SCLK rising edge to SEN rising edge	8			ns
t_{OUT_DV}	SDOUT delay	12	20	28	ns

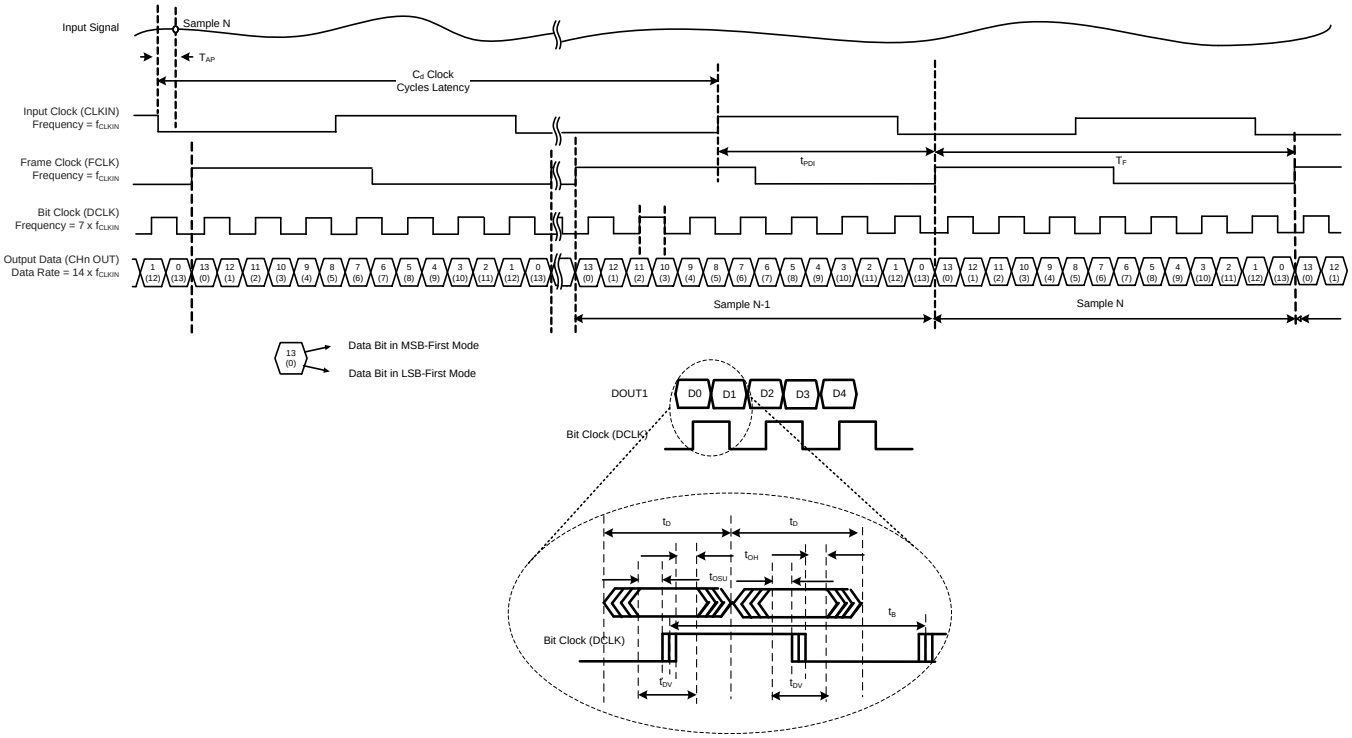
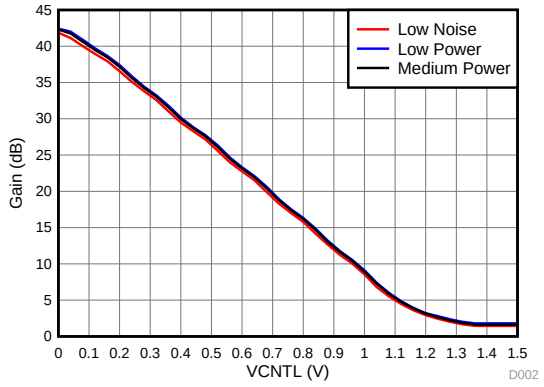


Figure 1. Output Timing Specification

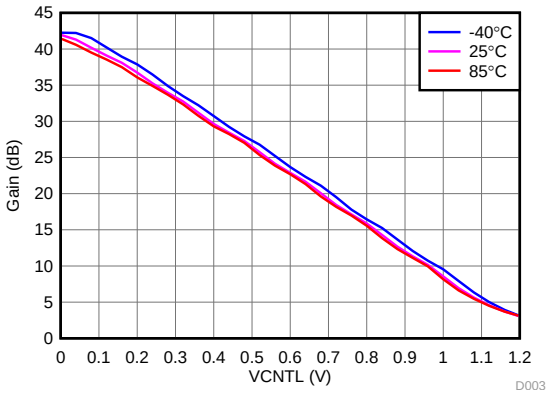
8.9 Typical Characteristics

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.



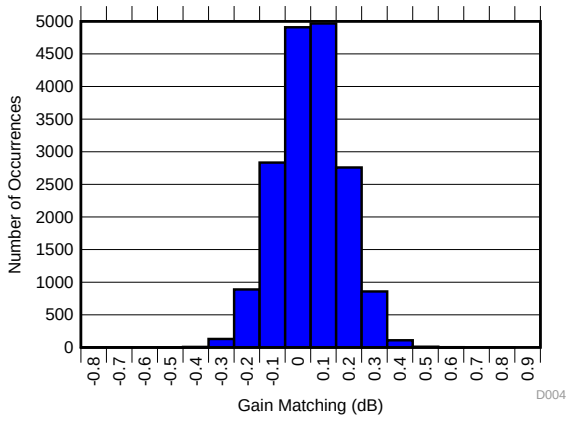
Across power modes

Figure 2. Gain vs VCNTL



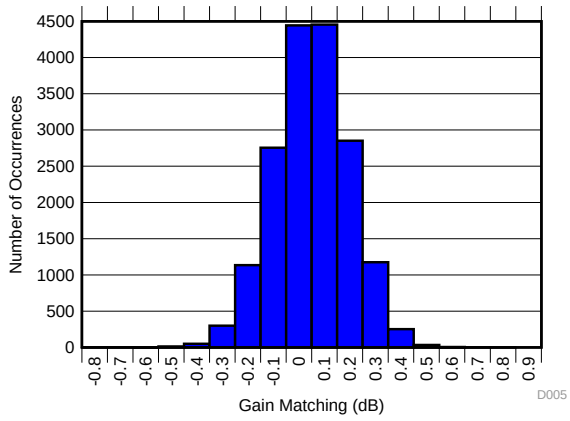
Across temperature

Figure 3. Gain vs VCNTL



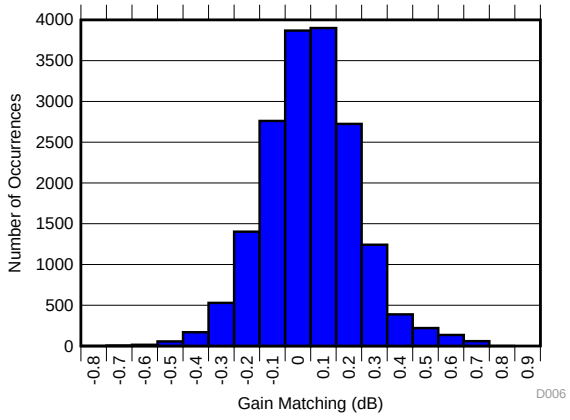
VCNTL = 0.3 V

Figure 4. Gain Matching Histogram (17472 Channels)



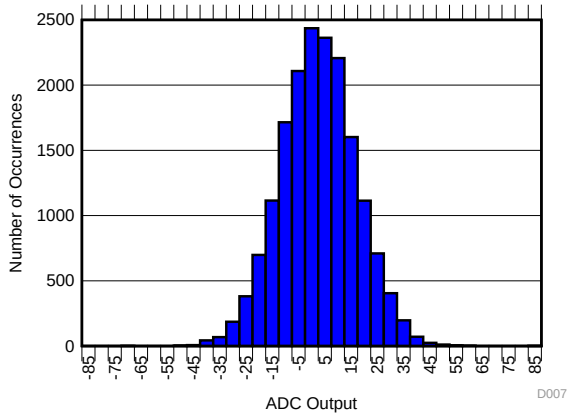
VCNTL = 0.6 V

Figure 5. Gain Matching Histogram (17472 Channels)



VCNTL = 0.9 V

Figure 6. Gain Matching Histogram (17472 Channels)

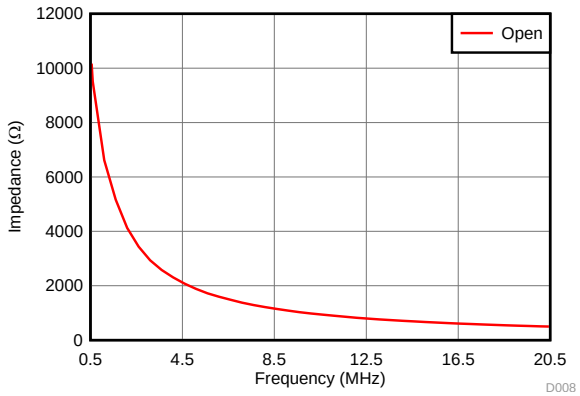


VCNTL = 0 V

Figure 7. Output Offset Histogram (17472 Channels)

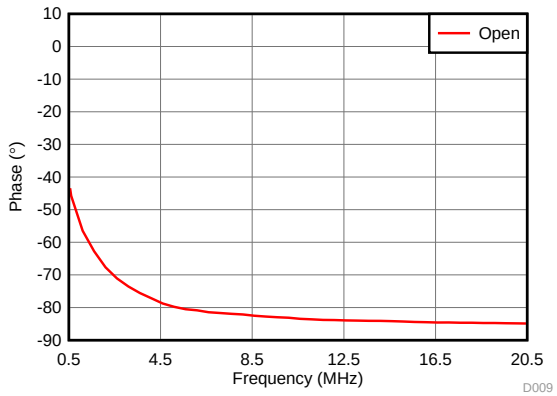
Typical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.



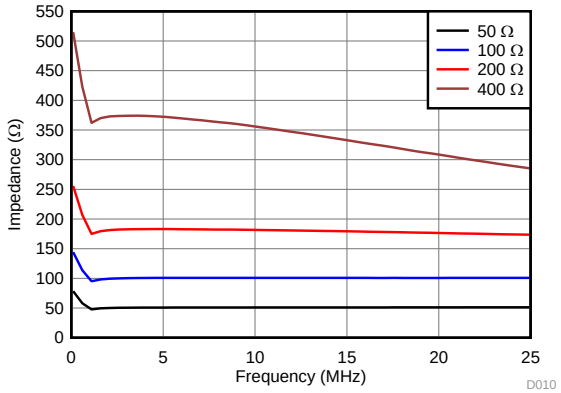
Without active termination

Figure 8. Input Impedance Magnitude vs Frequency



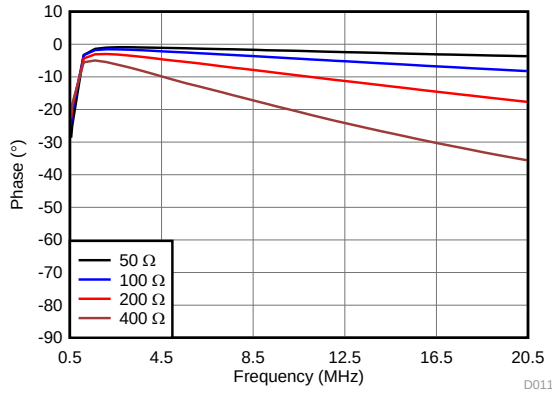
Without active termination

Figure 9. Input Impedance Phase vs Frequency



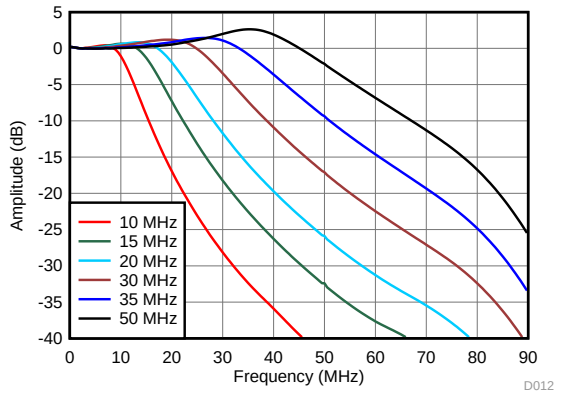
Across active termination

Figure 10. Input Impedance Magnitude vs Frequency



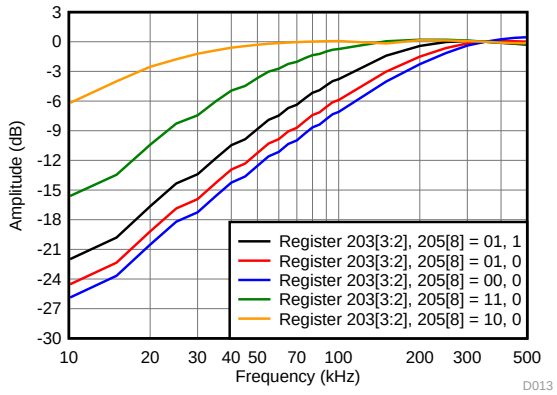
Across active termination

Figure 11. Input Impedance Phase vs Frequency



Across LPF corner settings

Figure 12. Full-Channel Amplitude Response vs Frequency



Across LNA_HPF_PROG (register 203, bits 3-2) and RED_LNA_HPF_3X (register 205, bit 8)

Figure 13. LNA High-Pass Filter Amplitude Response vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.

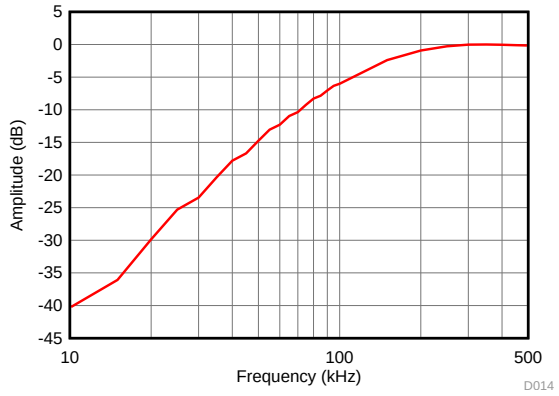
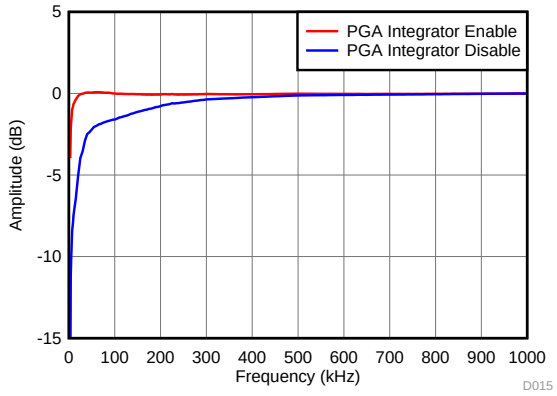
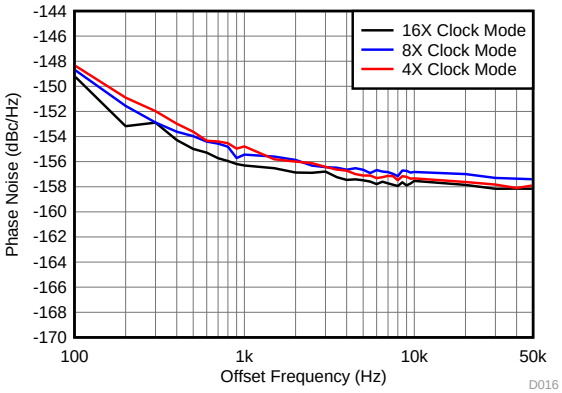


Figure 14. Full-Channel High-Pass Filter Amplitude Response vs Frequency



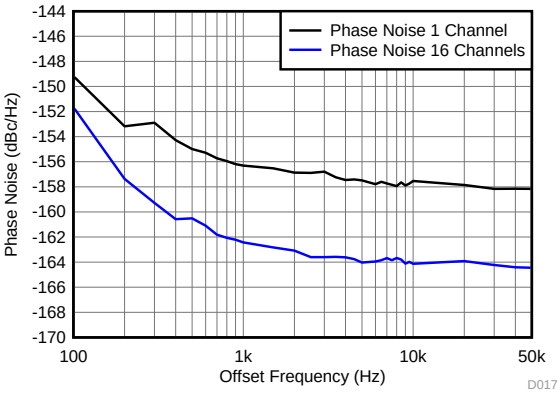
With INM capacitor = 1 µF

Figure 15. Full-Channel Low Frequency Amplitude Response vs Frequency



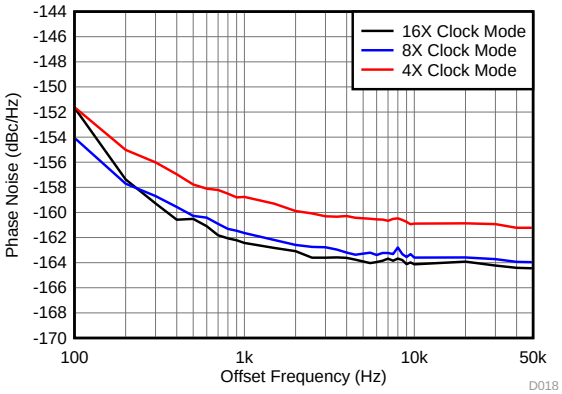
f_{IN} = 2 MHz, one channel across CW clock modes

Figure 16. CW Phase Noise vs Offset Frequency



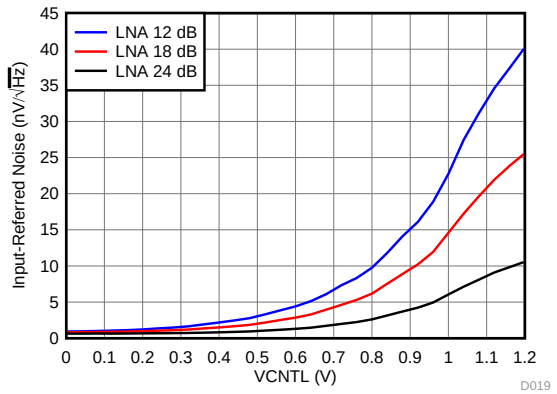
f_{IN} = 2 MHz, across one channel and 16 channels

Figure 17. CW Phase Noise vs Offset Frequency



f_{IN} = 2 MHz, 16 channels across CW clock modes

Figure 18. CW Phase Noise vs Offset Frequency

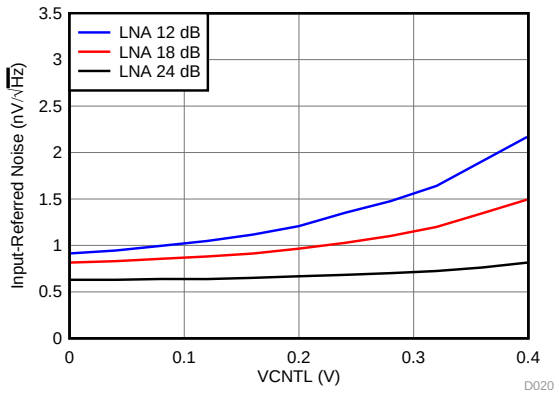


Across LNA gain for low-noise mode

Figure 19. Input-Referred Noise vs VCNTL

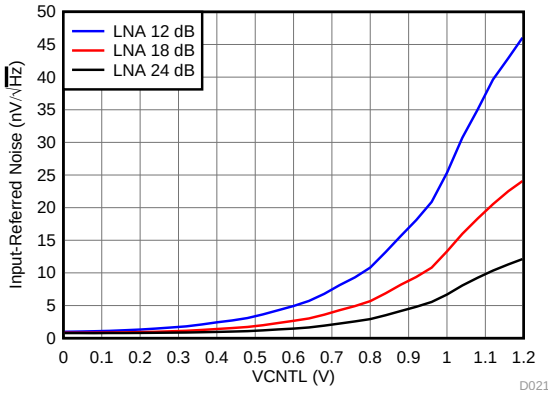
Typical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.



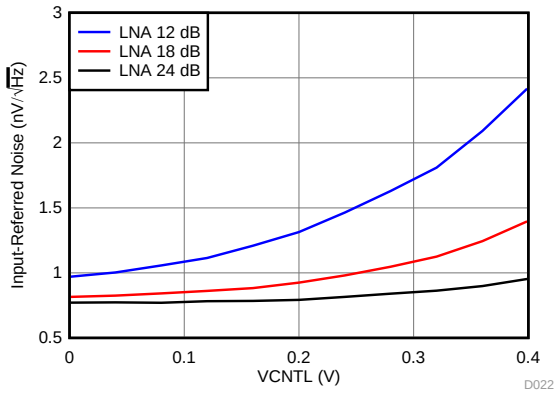
Across LNA gain for low-noise mode

Figure 20. Input-Referred Noise vs VCNTL (Zoomed)



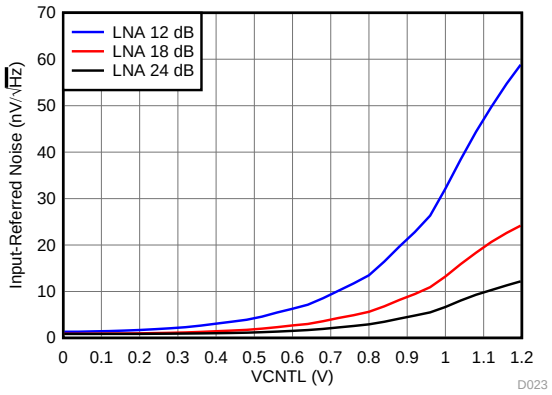
Across LNA gain for medium-power mode

Figure 21. Input-Referred Noise vs VCNTL



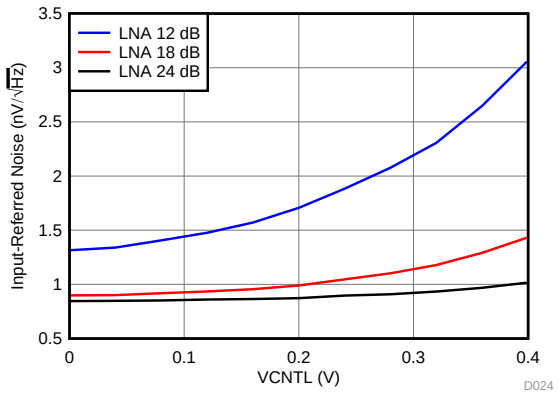
Across LNA gain for medium-power mode

Figure 22. Input-Referred Noise vs VCNTL (Zoomed)



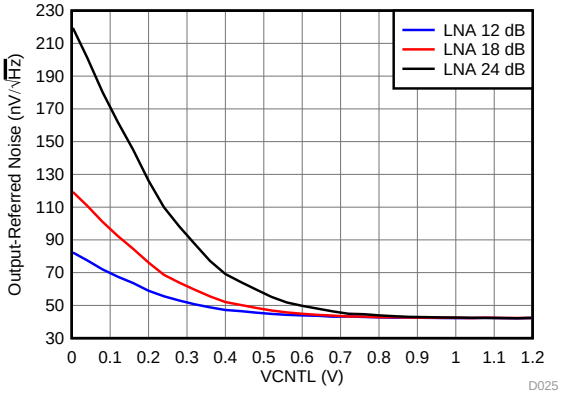
Across LNA gain for low-power mode

Figure 23. Input-Referred Noise vs VCNTL



Across LNA gain for low-power mode

Figure 24. Input-Referred Noise vs VCNTL (Zoomed)

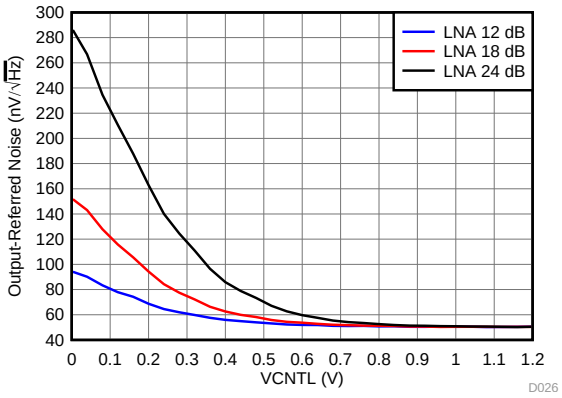


Across LNA gain for low-noise mode

Figure 25. Output-Referred Noise vs VCNTL

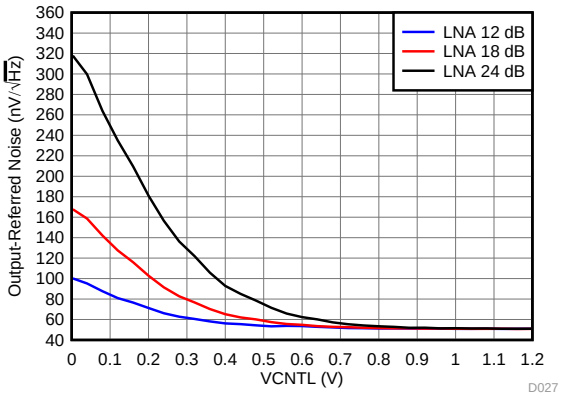
Typical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.



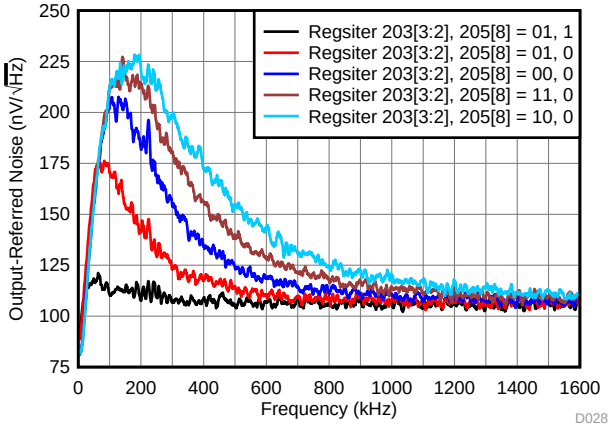
Across LNA gain for medium-power mode

Figure 26. Output-Referred Noise vs VCNTL



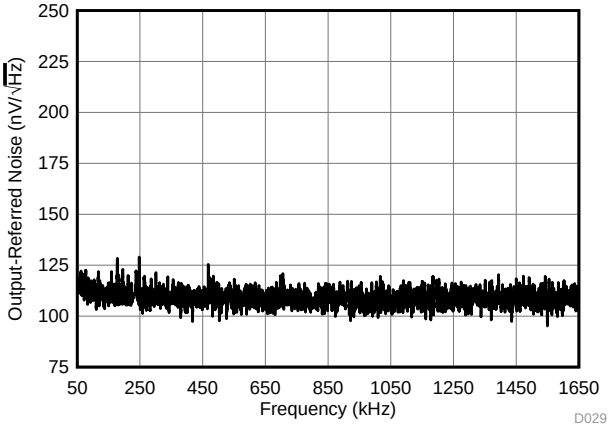
Across LNA gain for low-power mode

Figure 27. Output-Referred Noise vs VCNTL



Across LNA_HPF_PROG (register 203, bits 3-2) and RED_LNA_HPF_3X (register 205, bit 8)

Figure 28. Low-Frequency Output-Referred Noise vs Frequency



INMx capacitor = 1 µF, PGA_HPF_DIS (register 195, bit 4) = 1

Figure 29. Low-Frequency Output-Referred Noise vs Frequency

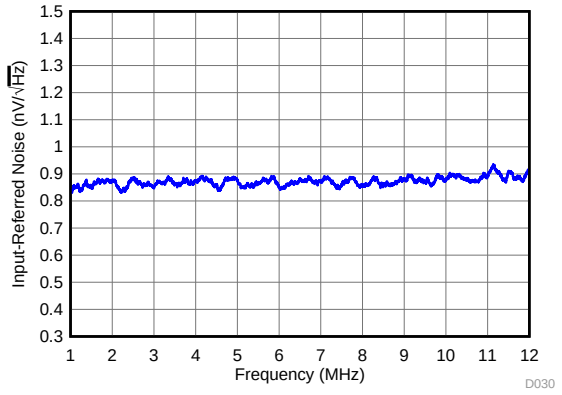


Figure 30. Input-Referred Noise vs Frequency

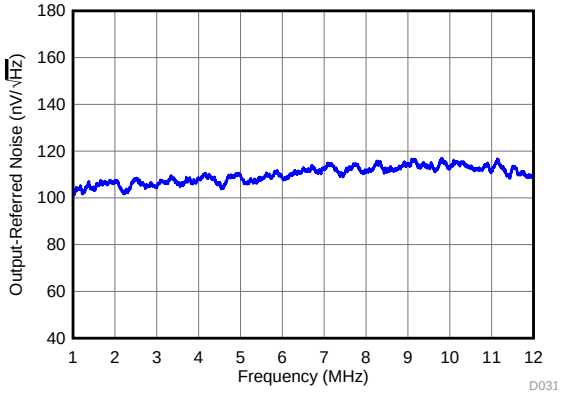
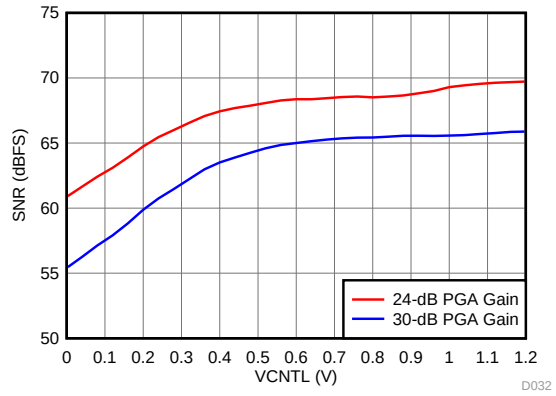


Figure 31. Output-Referred Noise vs Frequency

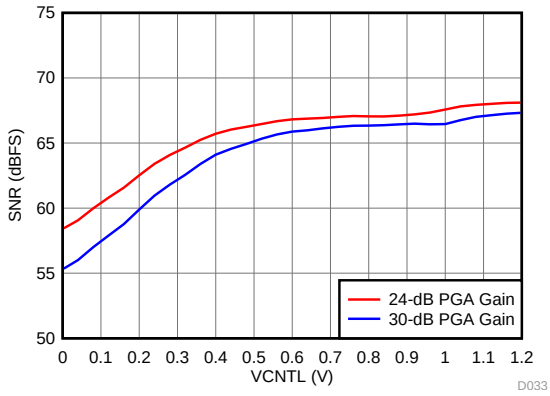
Typical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.



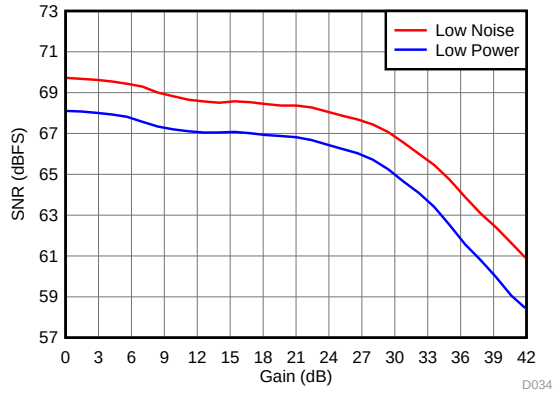
Low-noise mode across PGA gain

Figure 32. Signal-to-Noise Ratio vs VCNTL



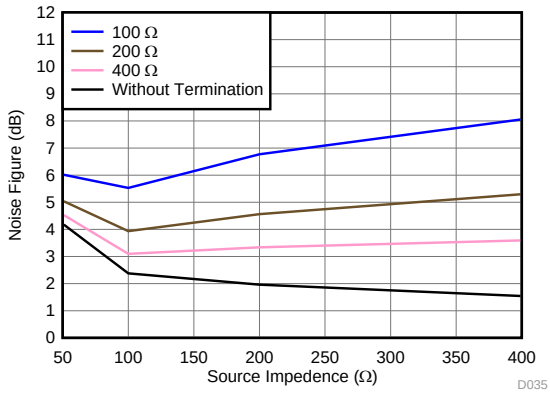
Low-power mode across PGA gain

Figure 33. Signal-to-Noise Ratio vs VCNTL



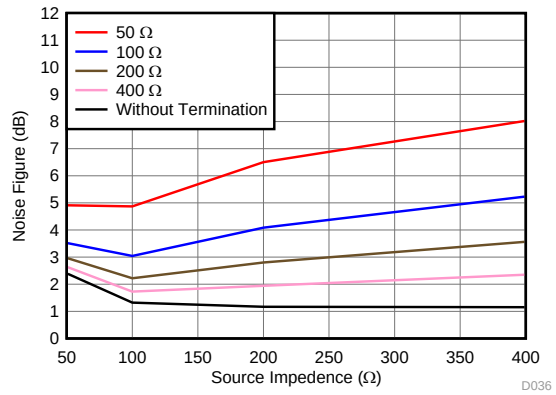
Across power modes

Figure 34. Signal-to-Noise Ratio vs Gain



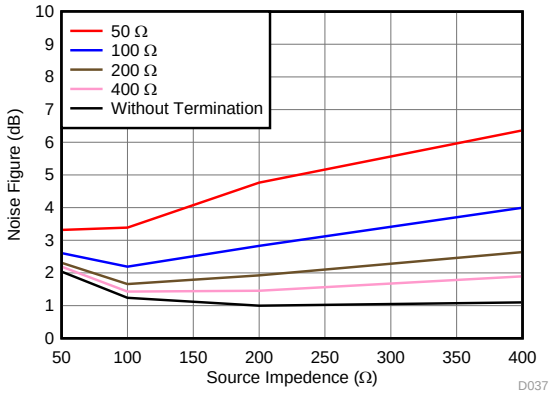
LNA = 12 dB, low-noise mode across active termination

Figure 35. Noise Figure vs Source Impedance



LNA = 18 dB, low-noise mode across active termination

Figure 36. Noise Figure vs Source Impedance

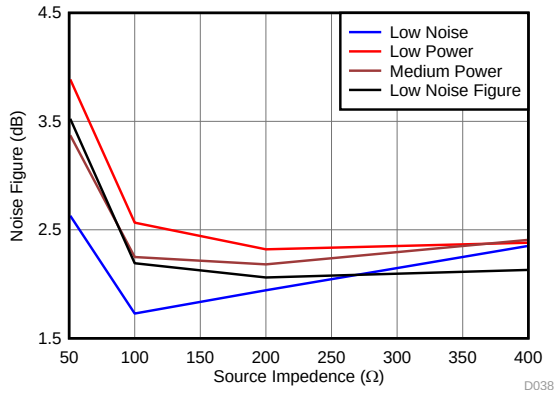


LNA = 24 dB, low-noise mode across active termination

Figure 37. Noise Figure vs Source Impedance

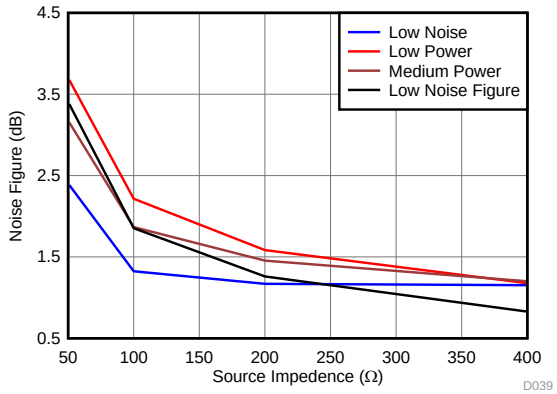
Typical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.



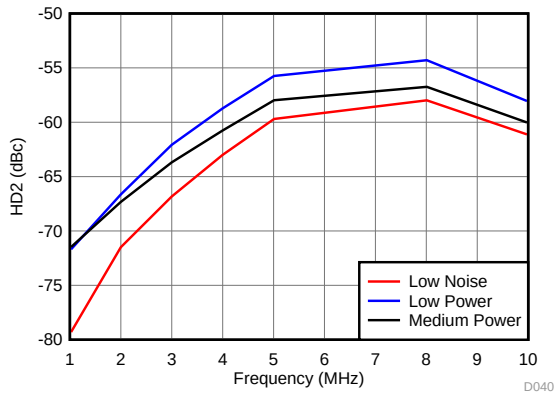
Active termination = 400-Ω across power modes

Figure 38. Noise Figure vs Source Impedance



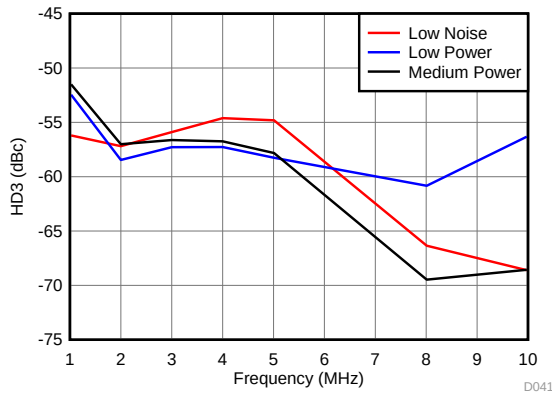
Without active termination across power modes

Figure 39. Noise Figure vs Source Impedance



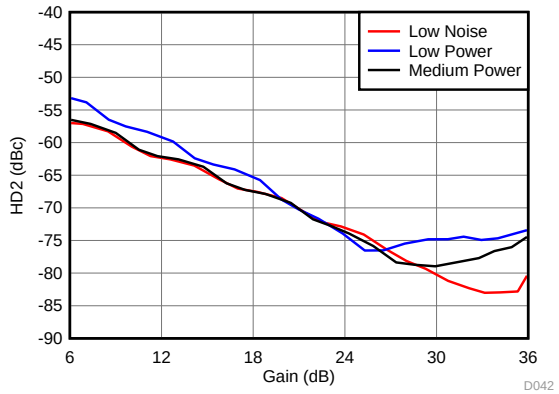
V_{IN} = 500 mV_{PP}, V_{OUT} = –1 dBFS across power modes

Figure 40. Second-Order Harmonic Distortion vs Frequency



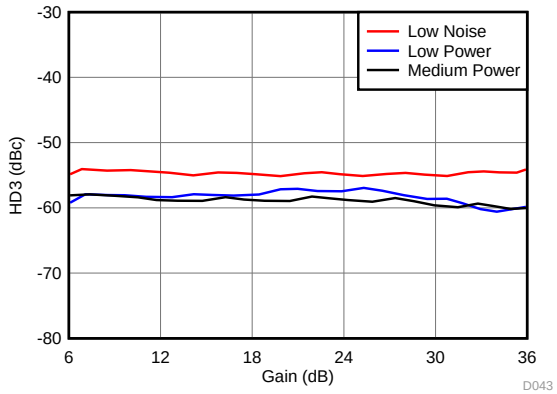
V_{IN} = 500 mV_{PP}, V_{OUT} = –1 dBFS across power modes

Figure 41. Third-Order Harmonic Distortion vs Frequency



LNA = 12 dB, V_{OUT} = –1 dBFS across power modes

Figure 42. Second-Order Harmonic Distortion vs Gain

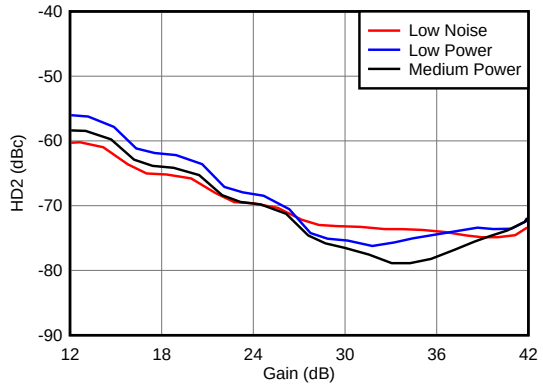


LNA = 12 dB, V_{OUT} = –1 dBFS across power modes

Figure 43. Third-Order Harmonic Distortion vs Gain

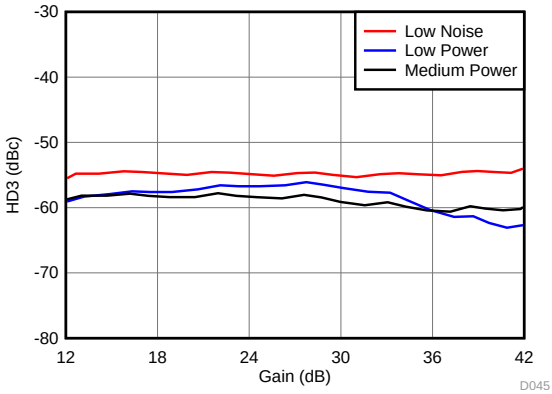
Typical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.



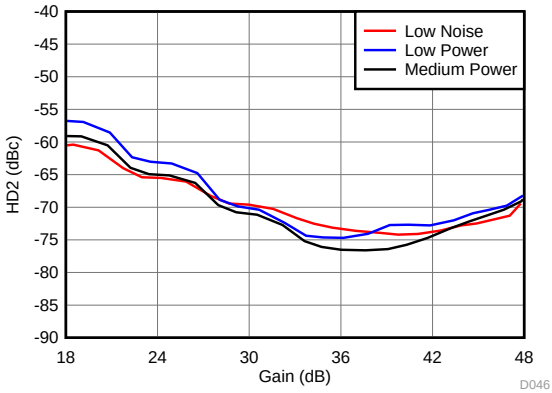
LNA = 18 dB, V_{OUT} = –1 dBFS across power modes

Figure 44. Second-Order Harmonic Distortion vs Gain



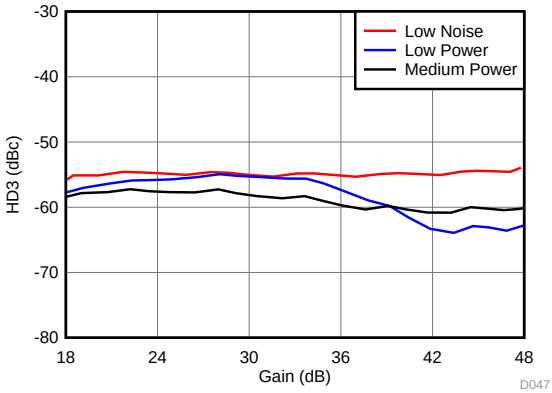
LNA = 18 dB, V_{OUT} = –1 dBFS, across power modes

Figure 45. Third-Order Harmonic Distortion vs Gain



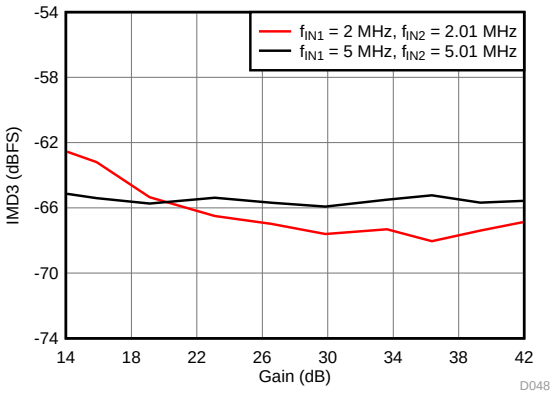
LNA = 24 dB, V_{OUT} = –1 dBFS across power modes

Figure 46. Second-Order Harmonic Distortion vs Gain



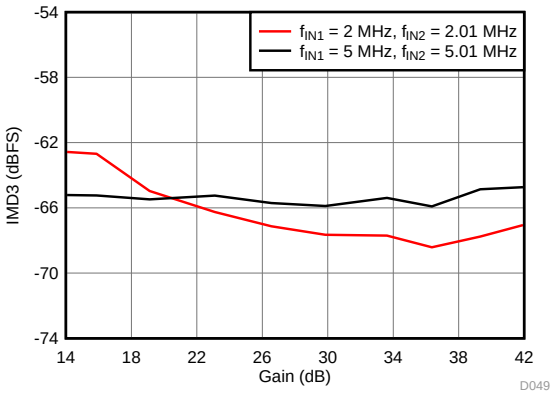
LNA = 24 dB, V_{OUT} = –1 dBFS across power modes

Figure 47. Third-Order Harmonic Distortion vs Gain



f_{OUT1} = –1 dBFS, f_{OUT2} = –21 dBFS

Figure 48. IMD3 vs Gain



f_{OUT1} = –7 dBFS, f_{OUT2} = –7 dBFS

Figure 49. IMD3 vs Gain

Typical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.

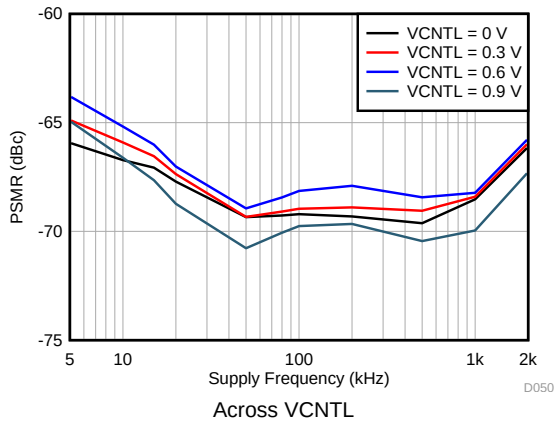


Figure 50. AVDD Power-Supply Modulation Ratio vs 100-mV_{PP} Supply Noise Frequencies

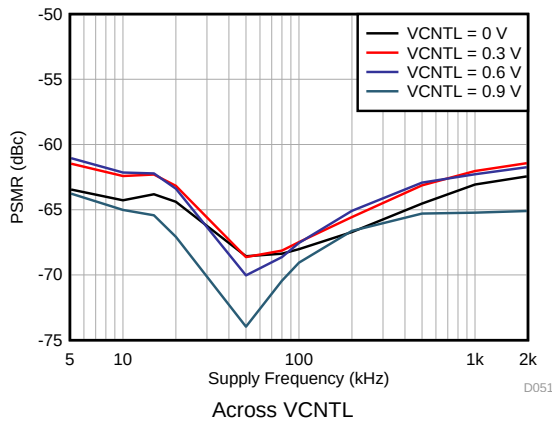


Figure 51. AVDD_5V Power-Supply Modulation Ratio vs 100-mV_{PP} Supply Noise Frequencies

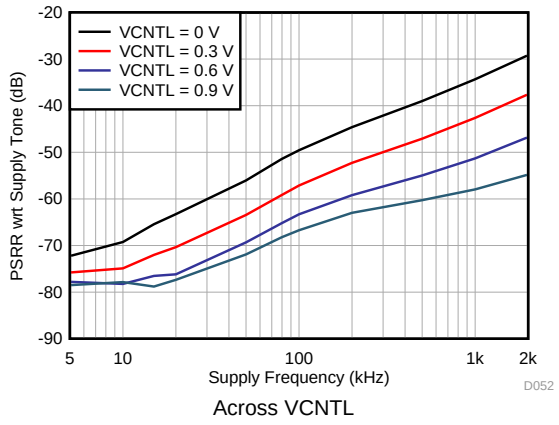


Figure 52. AVDD Power-Supply Rejection Ratio vs 100-mV_{PP} Supply Noise Frequencies

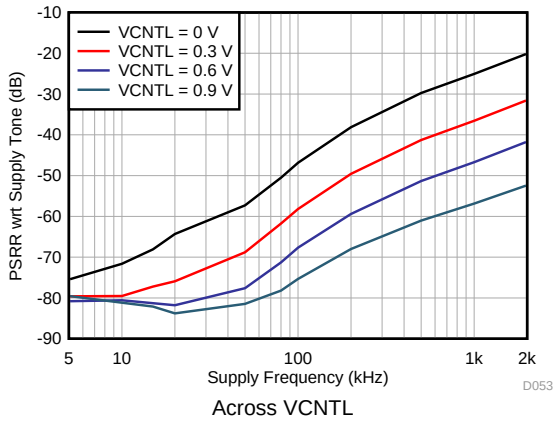


Figure 53. AVDD_5V Power-Supply Rejection Ratio vs 100-mV_{PP} Supply Noise Frequencies

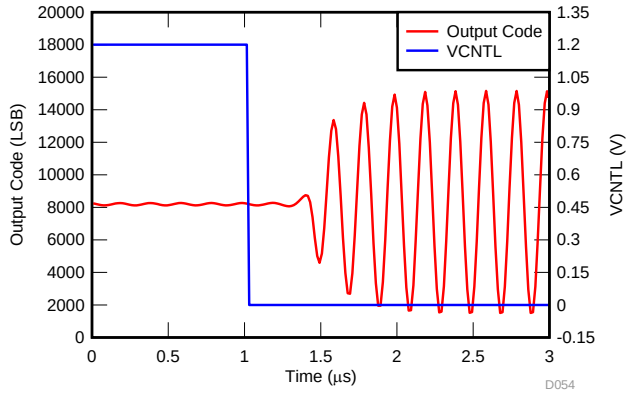


Figure 54. VCNTL Response vs Time

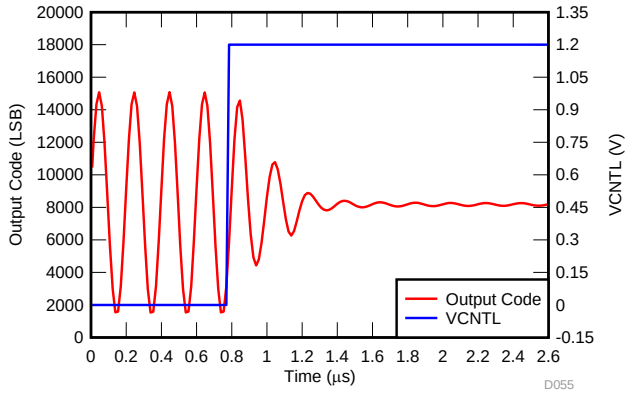


Figure 55. VCNTL Response vs Time

Typical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.

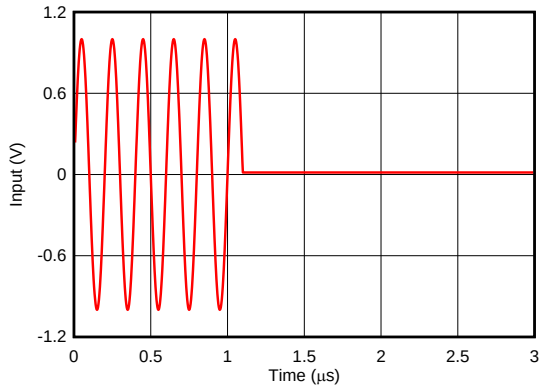


Figure 56. Pulse Inversion Asymmetrical Positive Input

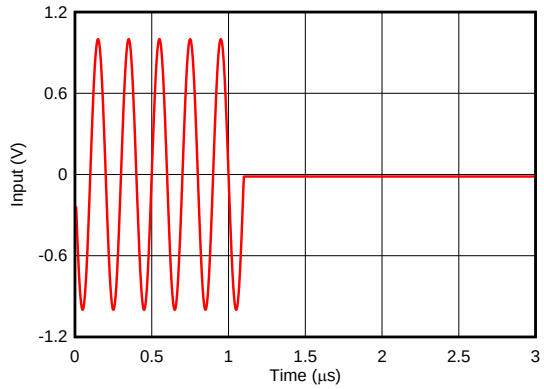
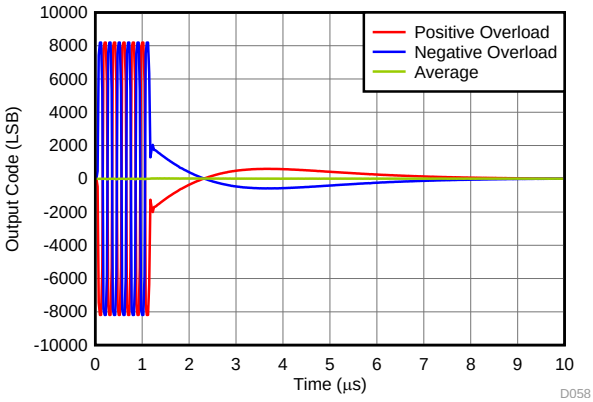
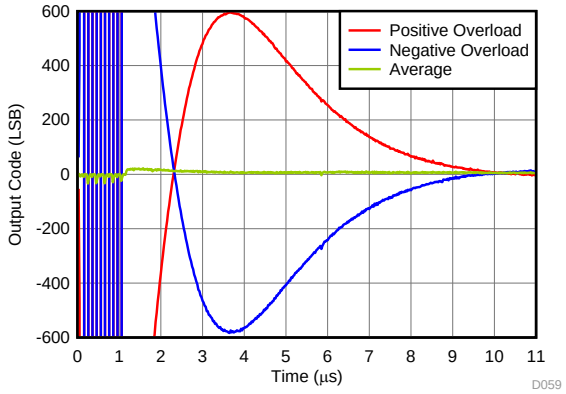


Figure 57. Pulse Inversion Asymmetrical Negative Input



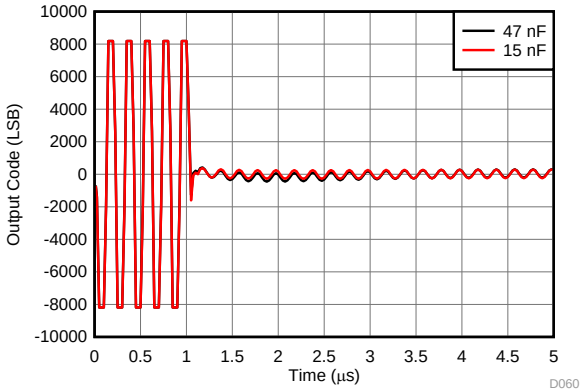
V_{IN} = 2 V_{PP}, PRF = 1 kHz, gain = 21 dB, across pulse inversion asymmetrical positive and negative input

Figure 58. Device Pulse Inversion Output vs Time



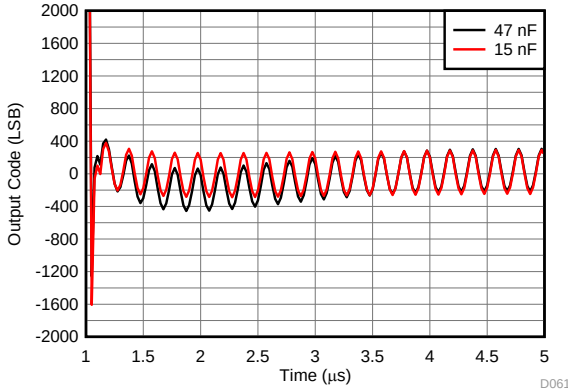
V_{IN} = 2 V_{PP}, PRF = 1 kHz, gain = 21 dB

Figure 59. Device Pulse Inversion Output vs Time (Zoomed)



V_{IN} = large amplitude (50 mV_{PP}) followed by small amplitude (500 μV_{PP}), across INM capacitor

Figure 60. Overload Recovery Output vs Time

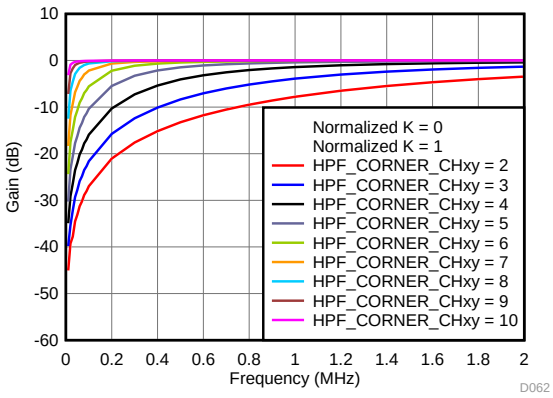


V_{IN} = large amplitude (50 mV_{PP}) followed by small amplitude (500 μV_{PP}), across INM capacitor

Figure 61. Overload Recovery Output vs Time (Zoomed)

Typical Characteristics (continued)

At T_A = 25°C, AVDD_1P8 = 1.8 V, AVDD_3P3 = 3.3 V, AVDD_5V = 5 V, DVDD_1P2 = 1.2 V, DVDD_1P8 = 1.8 V, ac-coupled with a 0.1-µF capacitor at INP, 15-nF capacitor to ground at INM, no active termination, VCNTLP = VCNTLM = 0 V, LNA = 18 dB, PGA = 24 dB, LPF filter = 15 MHz, low-noise mode, internal 500-Ω CW feedback resistor, 14-bit ADC resolution, ADC_CLKP and ADC_CLKM = 50-MHz differential, LVDS mode to capture ADC data, input signal frequency f_{IN} = 5 MHz, and output amplitude V_{OUT} = –1 dBFS, unless otherwise noted. Minimum and maximum values are specified across the full temperature range.



Across various HPF corner settings

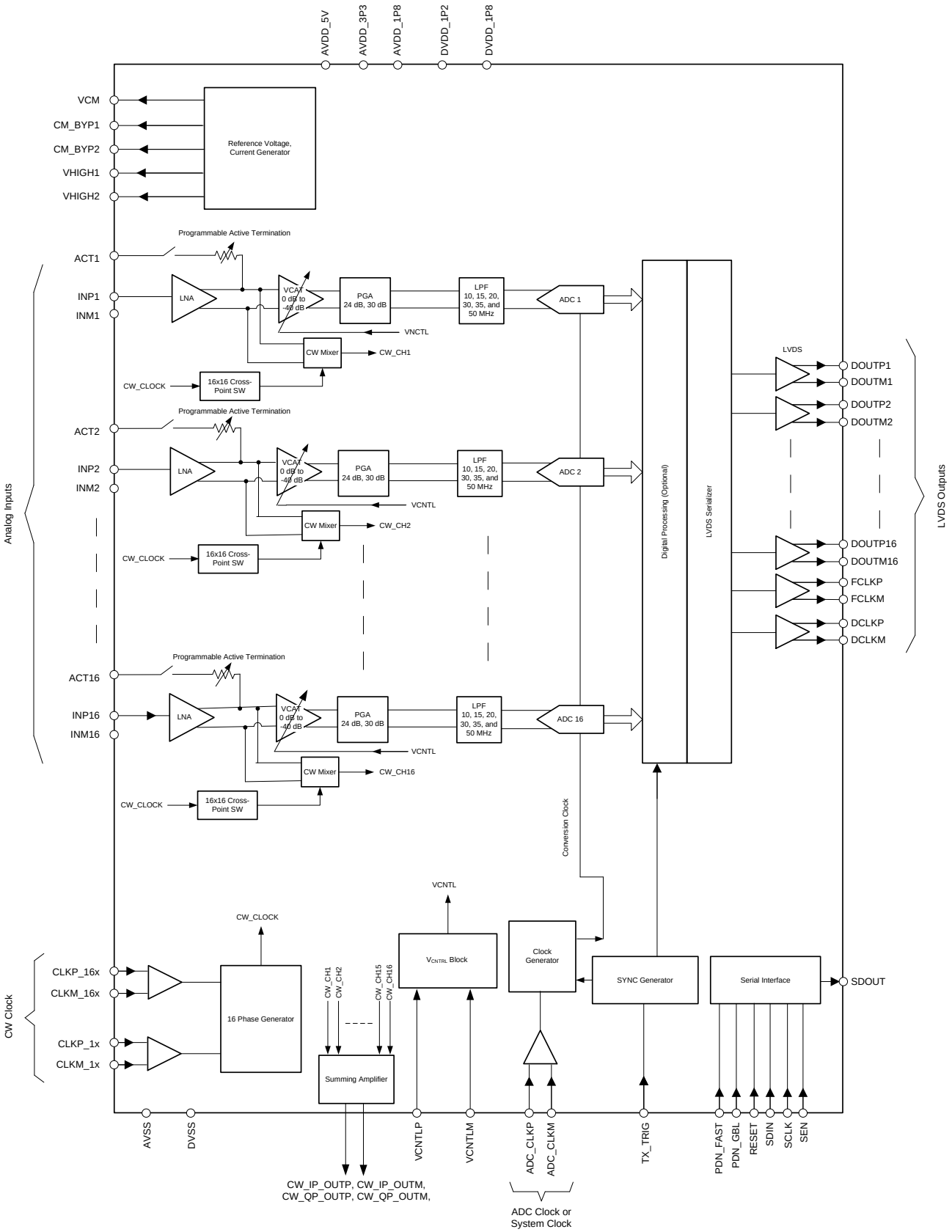
Figure 62. Digital High-Pass Filter Gain Response vs Frequency

9 Detailed Description

9.1 Overview

The AFE5818 is a highly-integrated, analog front-end (AFE) solution specifically designed for ultrasound systems in which high performance and higher integration are required. The device integrates a complete time-gain-control (TGC) imaging path and a continuous wave Doppler (CWD) path. The device also enables users to select from a variety of power and noise combinations to optimize system performance. The device contains 16 dedicated channels, each comprising a low-noise amplifier (LNA), voltage-controlled attenuator (VCAT), programmable gain amplifier (PGA), low-pass filter (LPF), and either a 14-bit or 12-bit analog-to-digital converter (ADC). At the output of the 16 ADCs is a low-voltage differential signaling (LVDS) serializer to transfer digital data. In addition, the device also contains a continuous wave (CW) mixer. Multiple features in the device are suitable for ultrasound applications (such as active termination, individual channel control, fast power-up and power-down response, programmable clamp voltage control, fast and consistent overload recovery, and digital processing). Therefore, this device brings premium image quality to ultra-portable, handheld systems all the way up to high-end ultrasound systems. In addition, the signal chain of the device can handle signal frequencies as low as 10 kHz and as high as 50 MHz. This broad analog frequency range enables the device to be used in both sonar and medical applications. See the *Functional Block Diagram* section for a simplified function block diagram.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Low-Noise Amplifier

In many high-gain systems, a low-noise amplifier is critical to achieve overall performance. The device uses new proprietary architecture and a bipolar junction transistor (BJT) input transistor to achieve exceptional low-noise performance when operating on a low-quiescent current.

9.3.1.1 Input Signal Support

The LNA takes a single-ended input signal and converts it to a differential output signal that is configurable for programmable gains of 24 dB, 18 dB, and 12 dB. The differential output signal has an input-referred noise of 0.63 nV/√Hz, 0.70 nV/√Hz, and 0.9 nV/√Hz, respectively, across the different gain modes. The LNA supports a maximum linear differential output swing of 4 V_{PP} across all gain settings. Therefore, depending on the LNA gain, the maximum linear input swing support changes from 250 mV_{PP}, 500 mV_{PP}, and 1 V_{PP}, for LNA gains of 24 dB, 18 dB, and 12 dB, respectively.

9.3.1.2 Input Circuit

The LNA input pin (INPx) is internally biased at approximately 2.2 V. AC couple the input signal to the INPx pin with an adequately-sized capacitor, C_{IN}. TI recommends using a 0.1-µF capacitor for C_{IN}. Similarly, the active termination pin is internally biased at 1.5 V. TI recommends connecting a 1-µF capacitor (C_{ACT}) from the active termination pin (ACTx) to the INP capacitor, as shown in Figure 63.

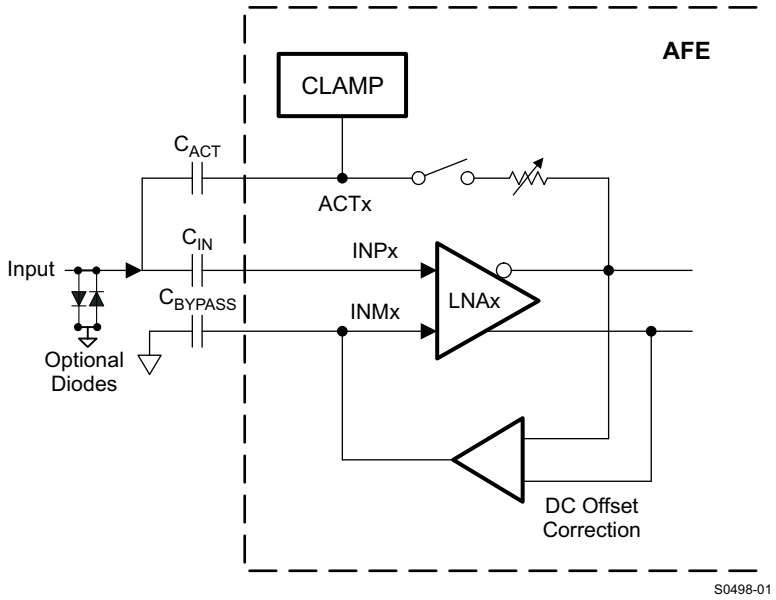


Figure 63. Device Input Circuit

9.3.1.3 LNA High-Pass Filter

To reject an unwanted low-frequency leakage signal from the transducer and to achieve low dc offset drift from the device, the AFE5818 incorporates a dc offset correction circuit for each amplifier stage; see Figure 63. This circuit extracts the low-frequency component from the LNA output, which is then fed back to the LNA complementary input for low-frequency signal rejection. Afterwards, this feedback circuit functions as a high-pass filter (HPF). The effective corner frequency of the HPF is determined by the C_{BYPASS} capacitor connected at the INMx pin of the device. The corner frequency is lower with larger C_{BYPASS} capacitors. A large capacitor (such as 1 µF) can be used for setting the low corner frequency (< 2 kHz) of the LNA dc offset correction circuit. For stable operation, the minimum value of the C_{BYPASS} capacitor that is supported by device is 15 nF. To disable this HPF, set the LNA_HPF_DIS register bit to 1. Note that disabling this HPF results in a large dc offset at the device output. Also, for a given INMx capacitor, the corner frequency of the HPF can be programmed using the LNA_HPF_PROG bit. Table 1 lists the HPF corner frequency for any arbitrary C_{BYPASS} capacitor connected at the INMx pin across various LNA_HPF_PROG bit settings.

Feature Description (continued)

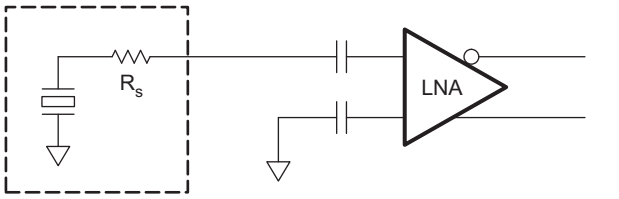
Table 1. LNA HPF Corner Frequency

LNA_HPF_PROG (Register 203, Bits 3-2)	HPF CORNER WITH 15-nF CAPACITOR CONNECTED AT INMx PIN	HPF CORNER WITH C_{BYPASS} CAPACITOR CONNECTED AT INMx PIN
00	100 kHz	100 kHz × (15 nF / C_{BYPASS})
01	50 kHz	50 kHz × (15 nF / C_{BYPASS})
10	200 kHz	200 kHz × (15 nF / C_{BYPASS})
11	150 kHz	150 kHz × (15 nF / C_{BYPASS})

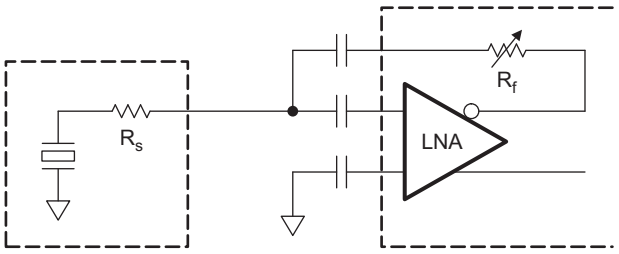
The LNA HPF corner frequency can be reduced by 3X by setting the RED_LNA_HPF_3X (register 205, bit 8) bit to 1. For instance, if the INMx capacitor is 15 nF, the LNA_HPF_PROG bits are set to 01, and RED_LNA_HPF_3X is set to 1, then the LNA HPF corner frequency is given by 50 kHz / 3 = 16.6 kHz. Figure 28 and Figure 29 illustrate the low-frequency noise for various LNA_HPF_PROG, RED_LNA_HPF_3X, and INM capacitor combinations.

9.3.1.4 LNA Input Impedance

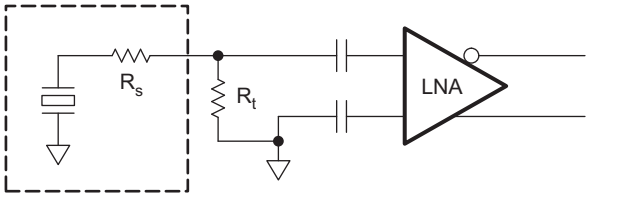
In ultrasound applications, signal reflection exists as a result of long cables between the transducer and system. This reflection results in extra ringing added to echo signals in PW mode. This ringing effect can degrade the axial resolution, which depends on the echo signal length. Therefore, either passive termination or active termination is preferred if good axial resolution is desired. Figure 64 shows three termination configurations: no termination, active termination, and passive termination.



(a) No Termination



(b) Active Termination



(c) Passive Termination

S0499-01

Figure 64. Termination Configurations

Under the no termination configuration, the input impedance of the device is approximately 6 kΩ (8 KΩ // 20 pF) at 1 MHz. Passive termination requires an external termination resistor (R_t), which contributes to additional thermal noise. The LNA supports active termination with programmable values, as shown in Figure 65.

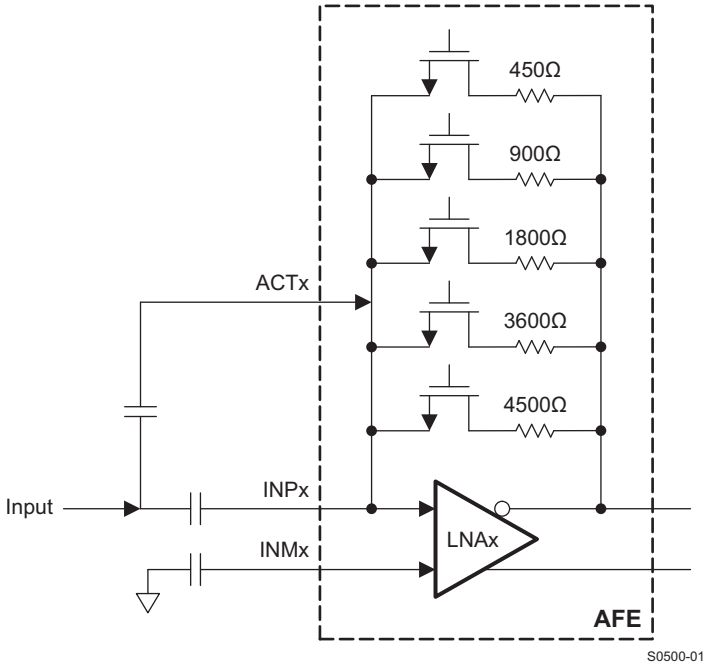


Figure 65. Active Termination Implementation

The device has four pre-settings: 50 Ω, 100 Ω, 200 Ω, and 400 Ω, which are configurable through the registers. Other termination values can be realized by setting the termination switches shown in Figure 65. The ACT_TERM_IND_RES register (register 196, bits 4-0) is used to enable these switches. The input impedance of the LNA under the active termination configuration approximately follows Equation 1:

$$Z_{IN} = \frac{R_f}{1 + \frac{Av_{LNA}}{2}} // C_{IN} // R_{IN} \quad (1)$$

where:

- R_{IN} (8 kΩ) and C_{IN} (20 pF) are the input resistance and capacitance of the LNA, respectively.

Table 75 lists the LNA R_{IN}s under different LNA gains. System designers can achieve fine tuning for different probes. Therefore, Z_{IN} is frequency dependent and decreases as frequency increases; see Figure 9. This rolling-off effect does not greatly affect system performance because 2 MHz to 10 MHz is the most commonly-used frequency range in medical ultrasound applications. Active termination can be applied to both CW and TGC modes; however, resulting from NF concerns, CW mode can use no termination mode. The flexibility of the impedance configuration is of great benefit because each ultrasound system includes multiple transducers with different impedances.

Figure 36, Figure 37, Figure 38, Figure 39, and Figure 40 illustrate the noise frequency (NF) under different termination configurations. All these NF plots indicate that no termination achieves the best noise figure. However, active termination adds less noise than passive termination. Thus, termination topology must be carefully selected based on each scenario in an ultrasound application.

9.3.1.5 LNA Gain Switch Response

The LNA gain is programmable through the LNA_GAIN_GBL (register 196, bits 14-13) SPI registers. The gain switching time depends on the SPI speed as well as the LNA gain response time. During switching, glitches can occur and sometimes appear as artifacts in images. In addition, the signal chain requires approximately 14 µs to settle after the LNA gain change. Thus, the LNA gain switching may not be preferred when switching time or settling time for the signal chain is limited. Note that a gain switch also changes the voltage level of clamping diodes; therefore, the setting time of the clamp circuit must be considered.

9.3.1.6 LNA Noise Contribution

The noise specification is critical for the LNA and determines the dynamic range of the entire system. The device LNA achieves low power, an exceptionally low-noise voltage of 0.63 nV/√Hz, and a low-current noise of 2.7 pA/√Hz.

Typical ultrasonic transducer impedance (R_S) varies from tens of ohms to several hundreds of ohms. Voltage noise is the dominant noise in most cases; however, the LNA current noise flowing through the source impedance (R_S) generates additional voltage noise. Total LNA noise can be computed with Equation 2.

$$LNA\_Noise_{total} = \sqrt{V^2_{LNAnoise} + R^2_s \times I^2_{LNAnoise}} \quad (2)$$

The device achieves a low noise figure (NF) over a wide range of source resistances; see Figure 36, Figure 37, Figure 38, Figure 39, and Figure 40.

9.3.1.7 LNA Overload Recovery

To avoid any image artifacts in an ultrasound system, the device must offer consistent and fast overload recovery response. In order to achieve this response, a clamping circuit is used on the active termination path; see Figure 63 to create a low-impedance path when an overload signal is detected by the device. The clamp circuit limits large input signals at the LNA inputs and improves the overload recovery performance. The clamp level can be automatically set to 350 mV_{PP}, 600 mV_{PP}, or 1.15 V_{PP}, depending on the LNA gain settings when the INPUT_CLAMP_LVL register (register 196, bits 10-9) is set to 00. Other clamp voltages (such as 1.15 V_{PP}, 0.6 V_{PP}, and 1.5 V_{PP}) are also achievable by setting different combinations of the INPUT_CLAMP_LVL bits. This clamping circuit is also designed to obtain good pulse inversion performance and reduce the affect of asymmetrical inputs. For very large overload signals (> 6 dB of the linear input signal range), TI recommends using back-to-back Schottky clamping diodes at the input to limit the amplitude of the input signal.

9.3.2 Voltage-Controlled Attenuator

The voltage-controlled attenuator is designed to have a linear-in-dB attenuation characteristic (that is, the average attenuation in dB; see Figure 3) that is constant for each equal increment of the control voltage (VCNTL = VCNTLP – VCNTLM). In the device, a differential control structure is used to reduce common-mode noise. However, a single-ended control voltage is also supported. A simplified attenuator structure is illustrated in Figure 66 and Figure 67 for analog and digital structures, respectively.

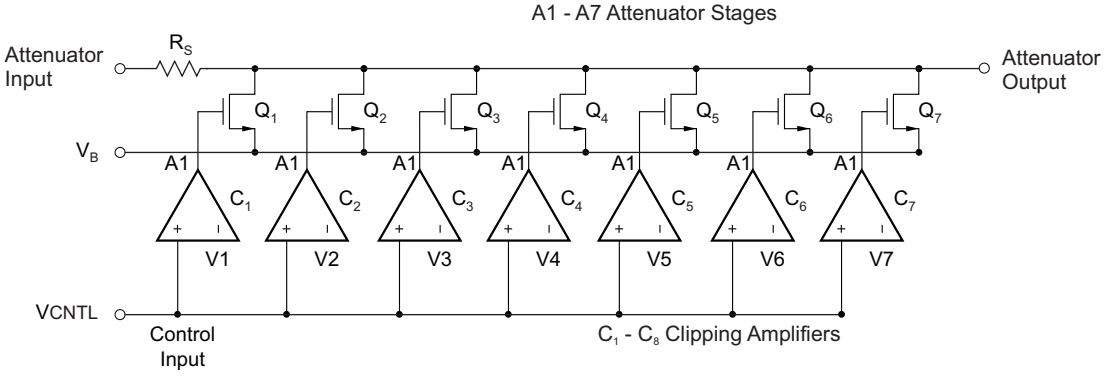


Figure 66. Simplified Voltage-Controlled Attenuator (Analog Structure)

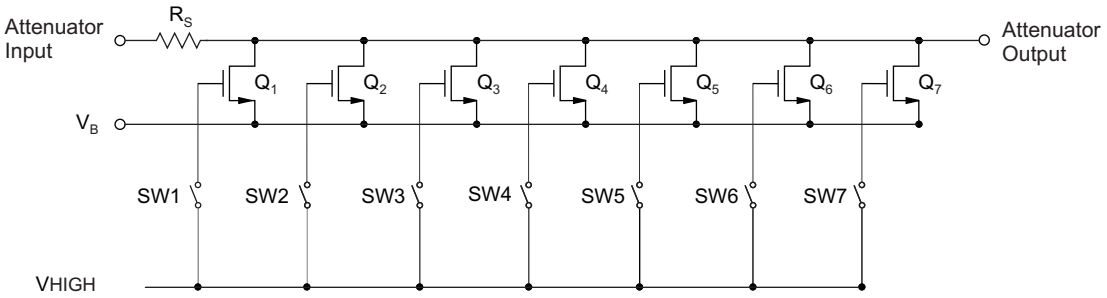


Figure 67. Simplified Voltage-Controlled Attenuator (Digital Structure)

The attenuator is essentially a variable voltage divider that consists of the series input resistor (R_S) and seven shunt field-effect transistors (FETs) placed in parallel and controlled by sequentially activated clipping amplifiers (A1 through A7). VCNTL is the effective difference between VCNTLP and VCNTLM. Each clipping amplifier can be understood as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltage. Reference voltages V1 through V7 are equally spaced over the 0-V to 1.5-V control voltage range. As control voltage increases through the input range of each clipping amplifier, the amplifier output rises from a voltage where the FET is nearly off to VHIGH where the FET is completely on. As each FET approaches its on-state and the control voltage continues to rise, the next clipping amplifier and FET combination takes over for the next portion of the piecewise linear attenuation characteristic. Thus, low control voltages have most of the FETs turned off, producing minimum signal attenuation. Similarly, high control voltages turn the FETs on, leading to a maximum signal attenuation. Therefore, each FET functions to decrease the shunt resistance of the voltage divider formed by R_S and the parallel FET network. Even though splitting the control voltage into seven segments achieves the full attenuation through different setoff transistors, the gain curve across the VCNTL voltage slightly deviates from the ideal dB-linear curve. The typical ripple is in the order of ±0.5 dB.

The typical gain range for this VCAT is approximately 40 dB, and this gain range is independent of the LNA and PGA gain settings. The TGC gain curve is inversely proportional to the voltage difference between VCNTLP and VCNTLM. The maximum attenuation (minimum channel gain) of the TGC gain curve appears at VCNTLP – VCNTLM = 1.5 V, and minimum attenuation (maximum channel gain) of the TGC gain curve occurs at VCNTLP – VCNTLM = 0 V.

The total channel gain for an 18-dB LNA gain and a 24-dB PGA gain setting, for different VCNTL values, is illustrated in Figure 2.

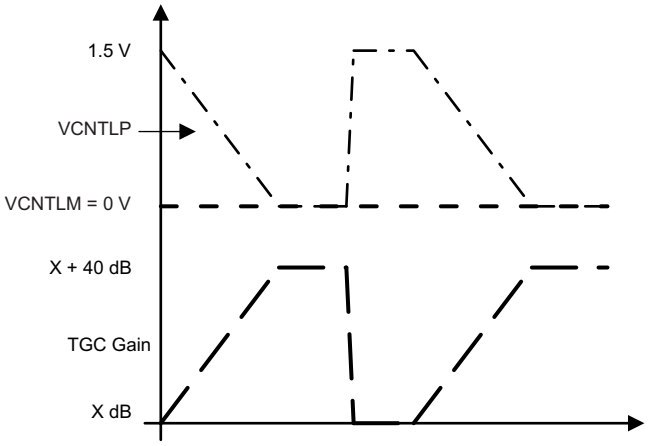
When the device operates in CW mode, the attenuator stage remains connected to the LNA outputs. Therefore, powering down the VCA is recommended using the PDWN_VCA_PGA (register 197, bit 12) register bit. In this case, the VCNTLP and VCNTLM voltage does not matter.

9.3.2.1 Digital TGC

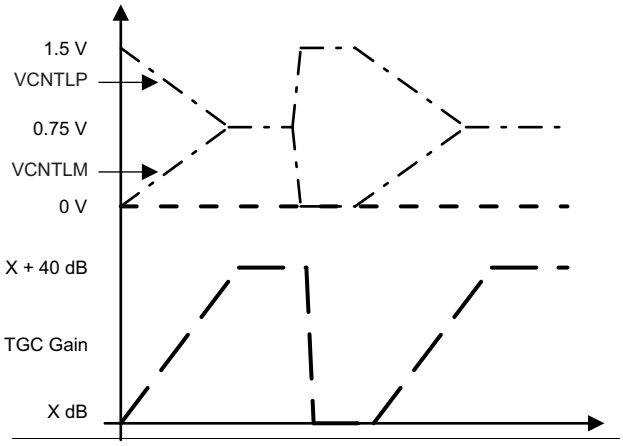
Additionally, a digitally-controlled TGC mode is implemented to achieve better phase-noise performance in the device. The attenuator can be controlled digitally instead of by the analog control voltage, VCNTL. This mode can be set by the EN_DIG_TGC (register 203, bit 7) register bit. The variable voltage divider is implemented as a fixed series resistance and a FET is implemented as the shunt resistance. Each FET can be turned on by connecting the SW[7:1] switches. Turning on each of these switches provides approximately 6 dB of attenuation. This attenuation can be controlled by the DIG_TGC_ATTENUATION (register 203, bits 6-4) register bits. This digital control feature can eliminate the noise from the VCNTL circuit and provide better SNR and phase noise for the TGC path. This digital TGC can be used for PW Doppler or color Doppler modes to achieve better performance than analog TGC.

9.3.2.2 Control Voltage Input

As previously mentioned, VCNTLP and VCNTLM can be driven by either a differential or a single-ended signal. For single-ended operation, VCNTLM can be grounded and VCNTLP can be swept from 0 V to 1.5 V. The TGC gain profile for the single-ended VCNTL is as shown in Figure 68a. For differentially driving VCNTL, VCNTLP must always be kept higher than VCNTLM with a typical common-mode of 0.75 V, as shown in Figure 68b.



(a) Single-Ended Input at VCNTLP



(b) Differential Inputs at VCNTLP and VCNTLM

Figure 68. VCNTLP and VCNTLM Configurations

The VCNTL pins are high-impedance pins, and the VCNTL pins of multiple devices can be connected in parallel with no significant loading effect. When the voltage level (VCNTLP, VCNTLM) is above 1.5 V or below 0 V, the attenuator continues to operate at its maximum attenuation level or minimum attenuation level, respectively. Limiting the voltage from –0.3 V to 2 V is recommended.

The VCNTL inputs have an approximate bandwidth of 800 kHz. This wide bandwidth, although useful in many applications (such as fast VCNTL response), can also allow high-frequency noise to modulate the gain control input and finally affect the Doppler performance. In practice, this modulation can be avoided by additional external filtering (R_{VCNTL} and C_{VCNTL}) at the VCNTLM and VCNTLP, pins as Figure 104 illustrates. However, the external filter cutoff frequency cannot be kept too low, which results in a low gain response time. Without an external filter on the VCNTLP, VCNTLM pins, the gain control response time typically requires less than 1 µs, as indicated in Figure 54.

Noise at the VCNTL pins must be low enough to obtain good system performance because this noise is correlated across channels. Figure 69 shows the allowed noise on the VCNTL pins for different channel systems.

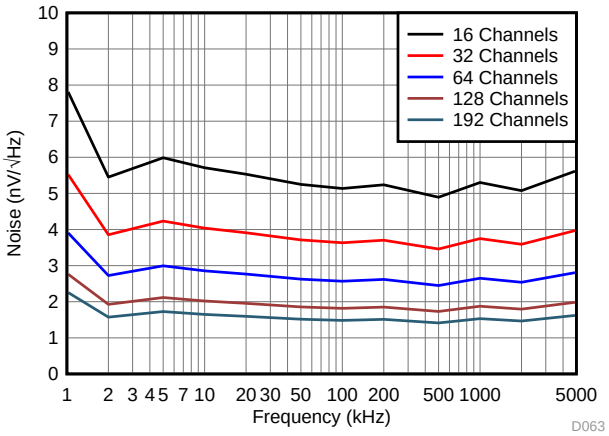


Figure 69. Allowed Noise on the VCNTL Signal Across Frequency and Different Channels

Typical VCNTLM and VCNTLP signals are generated by an 8-bit to 12-bit, 10-MSPS, digital-to-analog converter (DAC) and a differential operation amplifier. TI's DACs, such as the TLV5626, DAC7821. Differential amplifiers with output common-mode voltage control (that is, the THS4130 and OPA1632) can connect the DAC to the VCNTLM and VCNTLP pins. The buffer amplifier can also be configured as an active filter to suppress low frequency noise. The VCNTLM and VCNTLP circuit achieve low noise in order to prevent the VCNTLM and VCNTLP noise from being modulated to RF signals. VCNTLM and VCNTLP noise is recommended to be below 25 nV/√Hz at 1 kHz and 5 nV/√Hz at 50 kHz. For more information, see the THS413x data sheet and application report *Design for a Wideband Differential Transimpedance DAC Output* (SBAA150).

9.3.2.3 Voltage Attenuator Noise

The voltage-controlled attenuator noise follows a monotonic relationship to the attenuation coefficient. At higher attenuation the input-referred noise is higher, and vice-versa. The attenuator noise is then amplified by the PGA and becomes the noise floor at the ADC input. In the high attenuation operating range of the attenuator (that is, when VCNTL is high), the attenuator input noise can exceed the LNA output noise. The attenuator then becomes the dominant noise source for the following PGA stage and ADC. Therefore, minimize the attenuator noise compared to the LNA output noise. The device attenuator is designed for achieving very low noise even at high attenuation (low channel gain) and realizing better SNR of near-field imaging in ultrasound systems. The input-referred noise for different attenuations are listed in Table 2.

Table 2. Voltage-Controlled Attenuator Noise vs Attenuation

ATTENUATION (dB)	ATTENUATOR INPUT-REFERRED NOISE (nV/√Hz)
–40	10.5
–36	10
–30	9
–24	8.5
–18	6
–12	4
–6	3
0	2

9.3.3 Programmable Gain Amplifier (PGA)

After the voltage-controlled attenuator, a programmable gain amplifier can be configured as 24 dB or 30 dB with a constant input-referred noise of 1.75 nV/√Hz. The PGA structure consists of a differential voltage-to-current (V2I) converter with programmable gain, clamping circuits, a transimpedance amplifier (I2V) with a programmable third-order low-pass filter, and a dc offset correction circuit. The simplified PGA block diagram is shown in Figure 70.

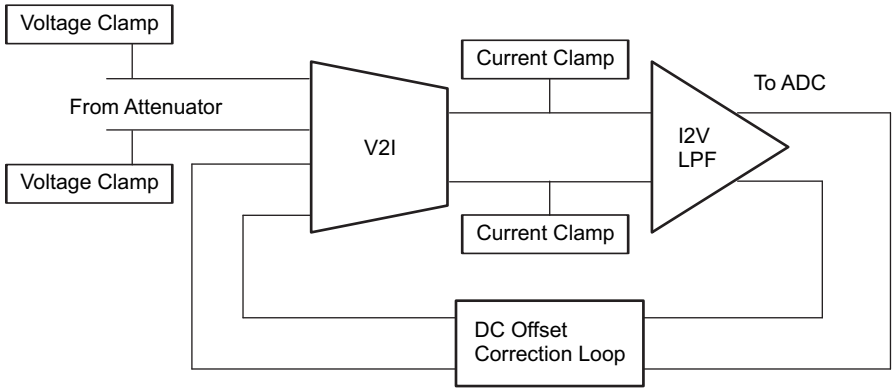


Figure 70. Simplified Block Diagram of the PGA

9.3.3.1 PGA Clamp

The PGA consists of two clamp circuits, positioned as shown in Figure 70. These clamps limit the amplitude of the overloaded signal and therefore provide better overload recovery performance.

An input-to-voltage (I2V) block in the PGA supports a maximum output swing of 2 V_{PP}, which means that the maximum allowed signal amplitude supported at the voltage-to-input (V2I) block input is 125 mV_{PP} (for a PGA gain = 24 dB) or 62.5 mV_{PP} (for a PGA gain = 30 dB). If the input signal amplitude of the V2I bock is much higher than the allowable range, then the V2I input can be clamped using a voltage clamp as shown in Figure 70. This voltage clamp is disabled by default and can be enabled by using the V2I_CLAMP (register 205, bit 13) register bit.

A current clamp is at the output of the V2I block, as shown in Figure 70, to further limit the overload signal amplitude. This current clamp can be programmed through the PGA_CLAMP_DIS (register 195, bit 7) and PGA_CLAMP_LVL (register 195, bit 6) register bits. Note that in low-power and medium-power modes, the current clamp is disabled for power savings if PGA_CLAMP_DIS (register 195, bit 7) = 0. This current clamp helps obtain a better overload recovery response. Without enabling this current clamp, at a 0.5-V VCNTL, the device shows a standard deviation of 4 LSBs at the output signal immediately after the overload. However, with the current clamp enabled, the standard deviation approaches 3.2 LSBs, meaning that the device requires less time to reach stable output. Also note that when the PGA output levels are greater than –2 dBFS and the current clamp is enabled, there is a degradation of approximately 3 dB to 5 dB in HD3 performance.

If the V2I block input is massively overloaded, the output of the I2V block can become saturated even if the voltage and current clamp described previously is enabled. When the I2V block becomes saturated, higher-order harmonics are generated that are aliased back to signal bandwidth after sampling. To avoid this undesirable V2I output saturation, a current clamp can be programmed to –6 dBFs, using the PGA_CLAMP_HALF bit (register 205, bit 15).

9.3.3.2 Low-Pass Filter (LPF)

The current from the V2I is fed to a programmable transimpedance amplifier, which also functions as a low-pass filter (LPF). The LPF is designed as a differential, active, third-order filter with Butterworth characteristics and a typical 18-dB per octave roll-off. Programmable through the serial interface, the –1-dB frequency corner can be set to 10 MHz, 15 MHz, 20 MHz, 30 MHz, 35 MHz, or 50 MHz. The filter bandwidth is set for all channels simultaneously. When very low bandwidth is desired (usually when suppressing higher order harmonics to a very low value), a 5-MHz filtering mode can be enabled using the SUPRESS_HIGHER_HARMONICS (register 205, bit 14) bit. However, enabling this mode can cause higher gain variation across devices when compared to other filter corner modes.

9.3.3.3 High-Pass Filter (HPF)

A selectable dc offset correction circuit is implemented in the PGA as well. This correction circuit is similar to the one used in the LNA. This circuit extracts the dc component of the PGA outputs, which are fed back to the PGA complimentary inputs for dc offset correction. This dc offset correction circuit also has a high-pass response with a cutoff frequency of 80 kHz. This HPF is enabled by default and can be disabled by using the PGA_HPF_DIS (register 195, bit 4) bit.

9.3.3.4 Noise

Low input noise is always preferred in a PGA and its noise contribution must not degrade the ADC SNR too much after the attenuator. The PGA is designed as a 24-dB or 30-dB gain with a constant input-referred noise of 1.75 nV/$\sqrt{\text{Hz}}$. The LNA noise dominates at minimum attenuation (used for small input signals), and the PGA and ADC noise dominate at maximum attenuation (large input signals). Thus, a 24-dB PGA gain achieves better SNR as long as the amplified signals can exceed the noise floor of the ADC.

9.3.4 Analog-to-Digital Converter (ADC)

The device supports a high-performance, 14-bit ADC that achieves 72-dBFS SNR. This ADC ensures excellent SNR at low-chain gain. The ADC can operate at maximum speeds of 65 MSPS and 80 MSPS, providing a 14-bit and a 12-bit output, respectively. The low-voltage differential signaling (LVDS) outputs of the ADC enable a flexible system integration that is desirable for miniaturized systems. In the following sections, full description of all inputs and outputs of the ADC with different configurations are provided along with suitable examples.

9.3.4.1 System Clock Input

The 16 channels on the device operate from a single clock input. To ensure that the aperture delay and jitter are the same for all channels, the device uses a clock tree network to generate individual sampling clocks for each channel. The clock lines for all channels are matched from the source point to the sampling circuit for each of the 16 internal ADCs. The delay variation is described by the aperture delay parameter of the *Output Interface Timing Characteristics* table. Variation over time is described by the aperture jitter parameter of the *Output Interface Timing Characteristics* table.

This system clock input can be driven differentially (sine wave, LVPECL, or LVDS) or single-ended (LVCMOS). The device clock input has an internal buffer and clock amplifier (see Figure 71) which is enabled or disabled automatically, depending on the type of clock provided (auto-detect feature).

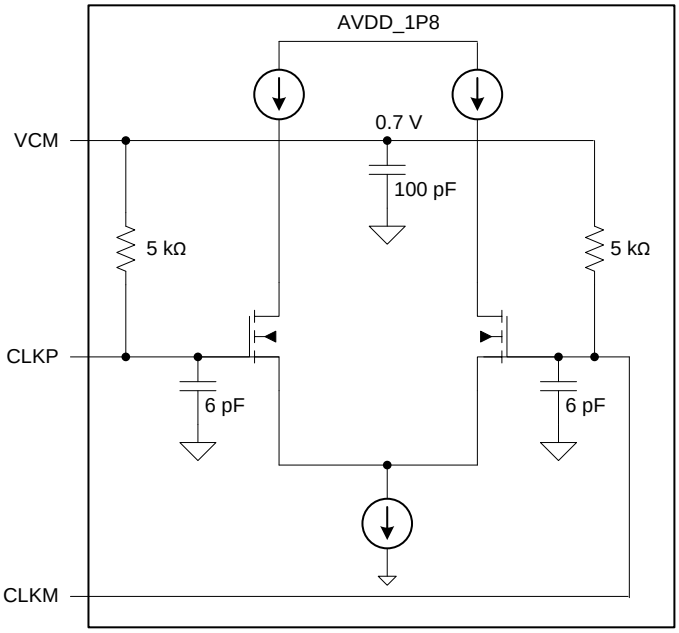


Figure 71. Internal Clock Buffer for Differential Clock Mode

If the preferred clocking scheme for the device is single-ended, connect the CLKM pin to ground (in other words, short CLKM directly to AVSS, as shown in Figure 72). In this case, the auto-detect feature shuts down the internal clock buffer and the device automatically goes into a single-ended clock input. Connect the single-ended clock source directly (without decoupling) to the CLKP pin, which is the only device clock input available because CLKM is connected to ground. Therefore, TI recommends using low-jitter, square signals (LVCMOS levels, 1.8-V amplitude) to drive the ADC (see technical brief, *Clocking High-Speed Data Converters,* SLYT075 for further details).

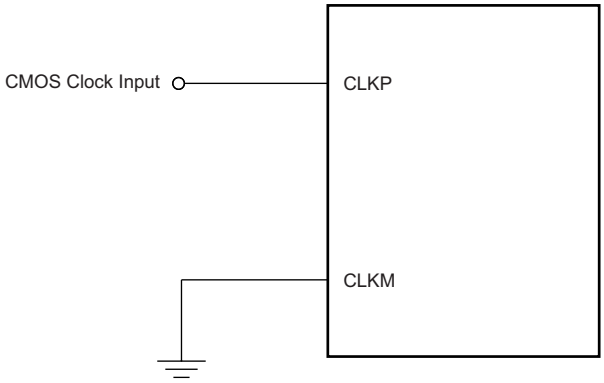


Figure 72. Single-Ended Clock Driving Circuit

For single-ended sinusoidal clocks, or for differential clocks (such as differential sine wave, LVPECL, LVDS, and so forth), enable the clock amplifier with the connection scheme shown in Figure 73. The 10-nF capacitor used to couple the clock input is as shown in Figure 73. This same scheme applies when the clock is single-ended but the clock amplitude is either small or its edges are not sharp (for instance, with a sinusoidal single-ended clock). In this case, the input clock signal can be connected with a capacitor to CLKP (as in Figure 73) and connect CLKM to ground through a capacitor (that is, ac-coupled to AVSS).

If a transformer is used with the secondary coil floating (for instance, to convert from single-ended to differential), the transformer can be connected directly to the clock inputs without requiring the 10-nF series capacitors.

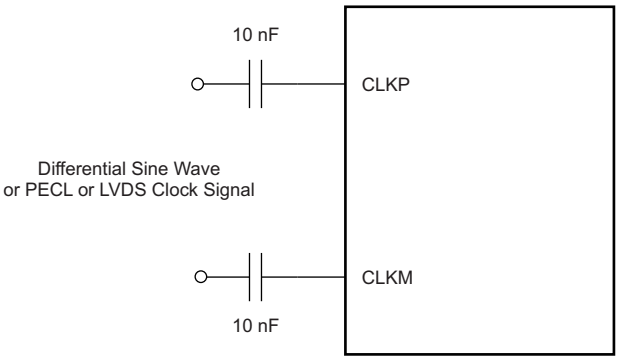


Figure 73. Differential Clock Driving Circuit

9.3.4.2 System Clock Configuration for Multiple Devices

To ensure that the aperture delay and jitter are the same for all channels, the device uses a clock tree network to generate individual sampling clocks for each channel. For all channels, the clock is matched from the source point to the sampling circuit of each of the eight internal devices. The variation on this delay is described in the *Aperture Delay* parameter of the *Output Interface Timing Characteristics* table. Variation is described by the aperture jitter parameter of the *Output Interface Timing Characteristics* table.

The system clock input can be driven by differential clocks (sine wave, LVPECL, or LVDS) or single-ended clocks (LVCMOS). In the single-ended case, TI recommends the use of low-jitter square signals (LVCMOS levels, 1.8-V amplitude). See technical brief, *Clocking High-Speed Data Converters,* SLYT075 for further details on the theory.

The jitter cleaners CDCM7005, CDCE72010, or LMK048X series are suitable to generate the system clock and ensure high performance for the 14-bit device resolution. Figure 74 shows a clock distribution network.

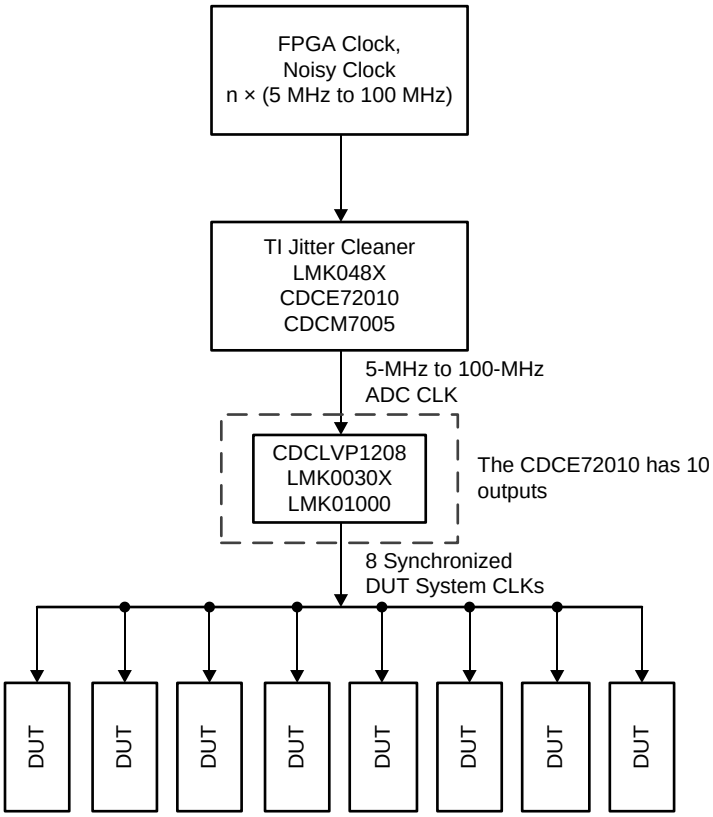


Figure 74. System Clock Distribution Network

9.3.4.3 LVDS Interface

The device supports an LVDS output interface in order to transfer device digital data serially to an FPGA. The device has a total of 18 LVDS output lines. One of these pairs is a serial data clock, another pair is a data framing clock, and the remaining 16 pairs are dedicated for data transfer. A graphical representation of the LVDS output is shown in Figure 75.

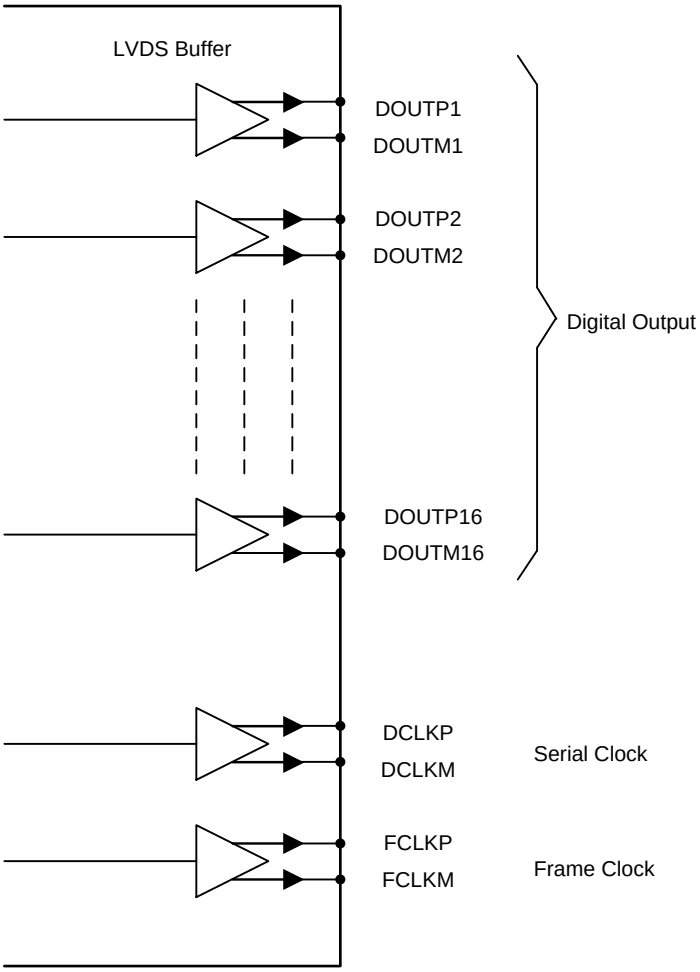


Figure 75. LVDS Output

9.3.4.3.1 LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 76. The buffer is designed for an output impedance of 100 Ω (R_{OUT}). The differential outputs can be terminated at the receiver end by a 100-Ω termination. The buffer output impedance functions like a source-side series termination. By absorbing reflections from the receiver end, the buffer output impedance helps improve signal integrity. Note that this internal termination can neither be disabled nor its value changed.

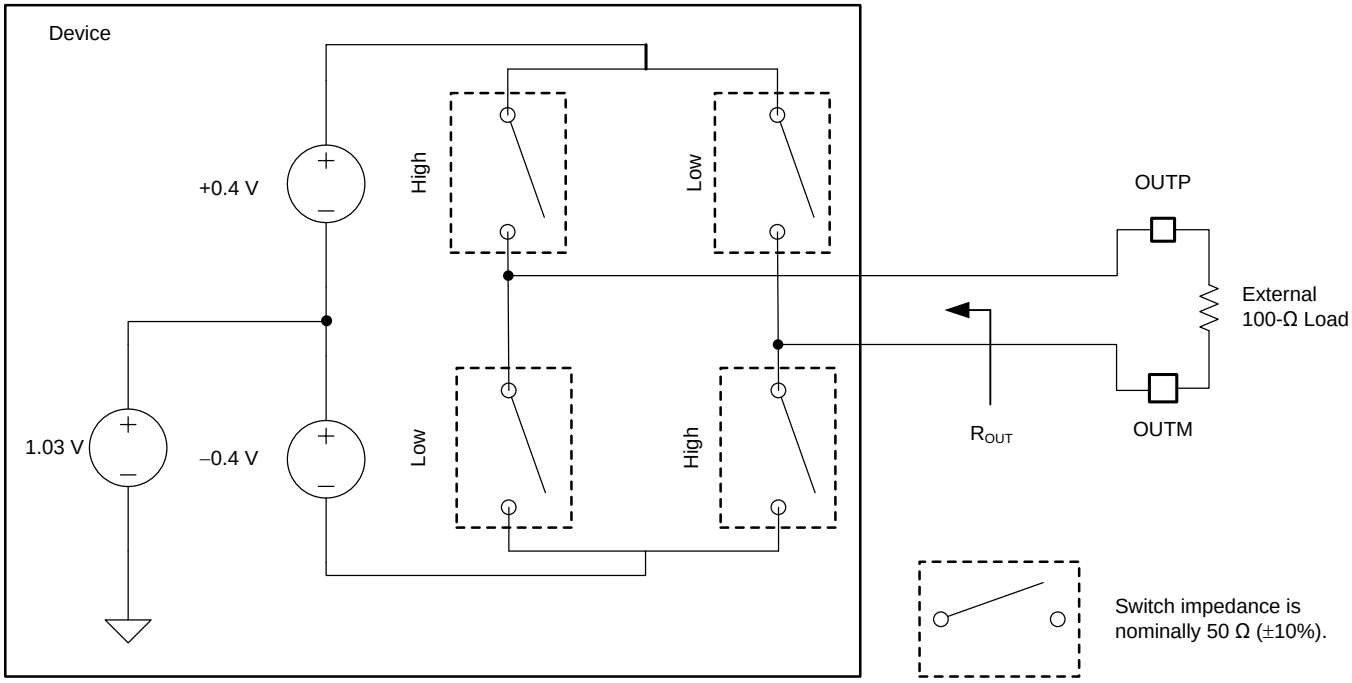


Figure 76. LVDS Output Circuit

9.3.4.3.2 LVDS Data Rate Modes

The LVDS interface supports two data rate modes, as described in this section. Figure 77 shows the Nomenclatures used in LVDS timing diagrams

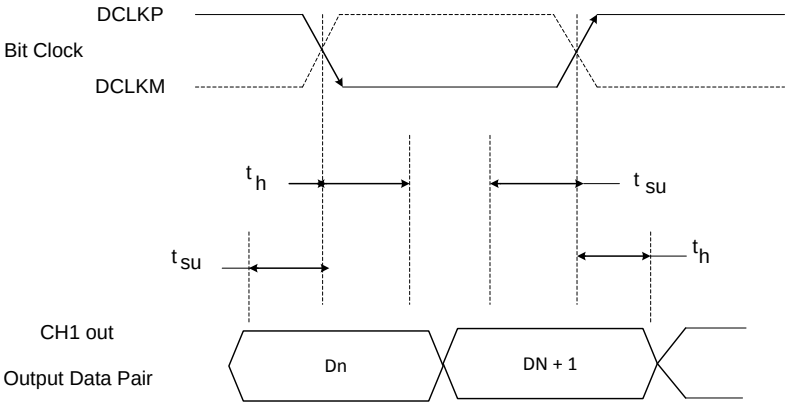
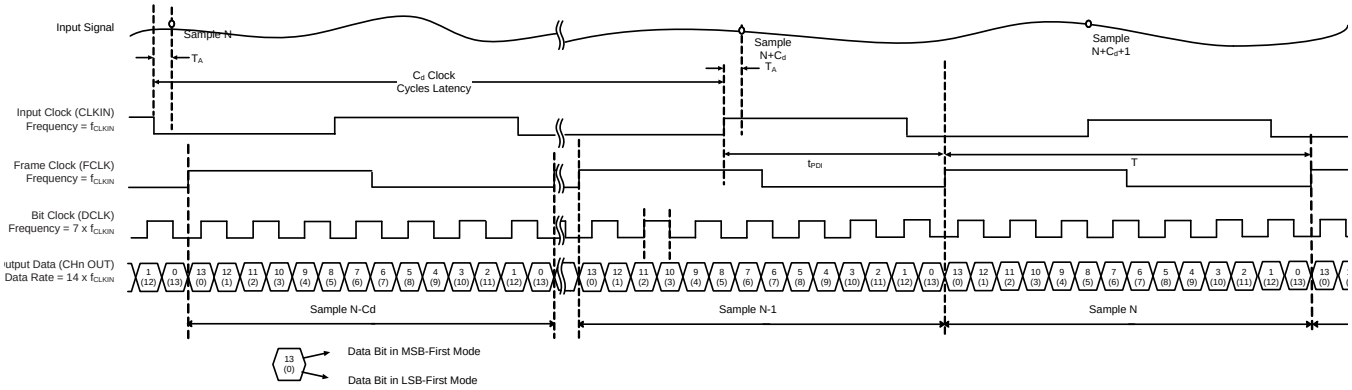


Figure 77. LVDS Timing Nomenclature

9.3.4.3.2.1 1X Data Rate Mode

In 1X data rate mode, each LVDS output carries data from a single ADC. Figure 78 and Figure 79 show the output data, serial clock, and frame clock LVDS lines for the 14-bit and 12-bit 1X mode, respectively.



(1) K = ADC resolution.

Figure 78. 14-Bit, 1X Data Rate Output Timing Specification

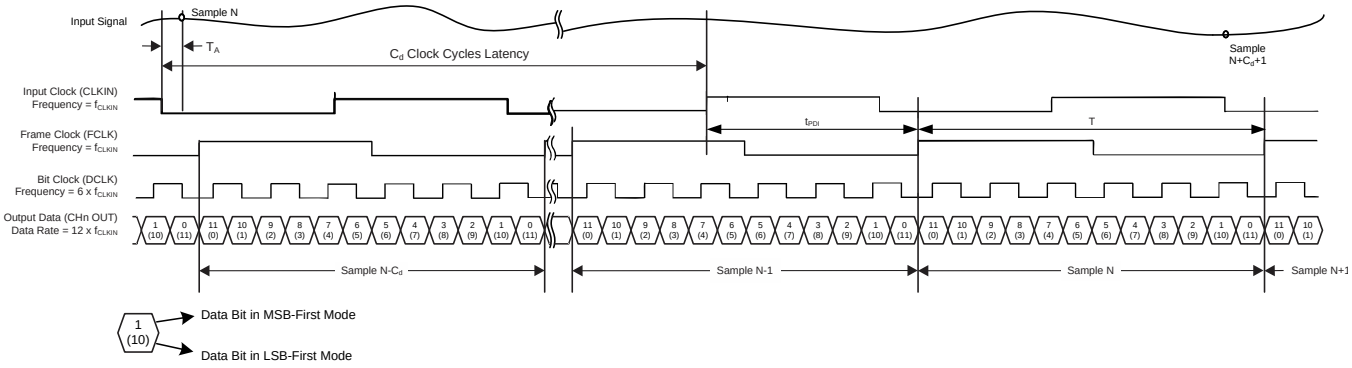


Figure 79. 12-Bit, 1X Data Rate Output Timing Specification

9.3.4.3.2.2 2X Data Rate Mode

In 2X data rate mode, only half of the LVDS lines are used to transfer data. Thus, this mode is useful for saving power when lower sampling frequency ranges permit. This mode is enabled with the LVDS_RATE_2X register bit (register 1, bit 14). After enabling this mode, the digital data from two ADCs are transmitted with a single LVDS lane. When compared to the 1X data rate mode, the 2X data rate mode serial clock frequency is doubled, but the frame clock frequency remains the same (for the same serialization factor and ADC resolution).

When the frame clock is high, data on DOUT1 corresponds to channel 1, DOUT2 corresponds to channel 3, and so forth. When the frame clock is low, DOUT1 transmits channel 2 data, DOUT2 transmits channel 4 data, and so forth.

Figure 80 and Figure 81 show a timing diagram for the 14-bit and 12-bit 2X mode, respectively. Channel and LVDS data line mapping for this mode are listed in Table 3. Note that idle LVDS lines are not powered down by default. To save power, these lines can be powered down using the corresponding power-down bits (PDN_LVDSx).

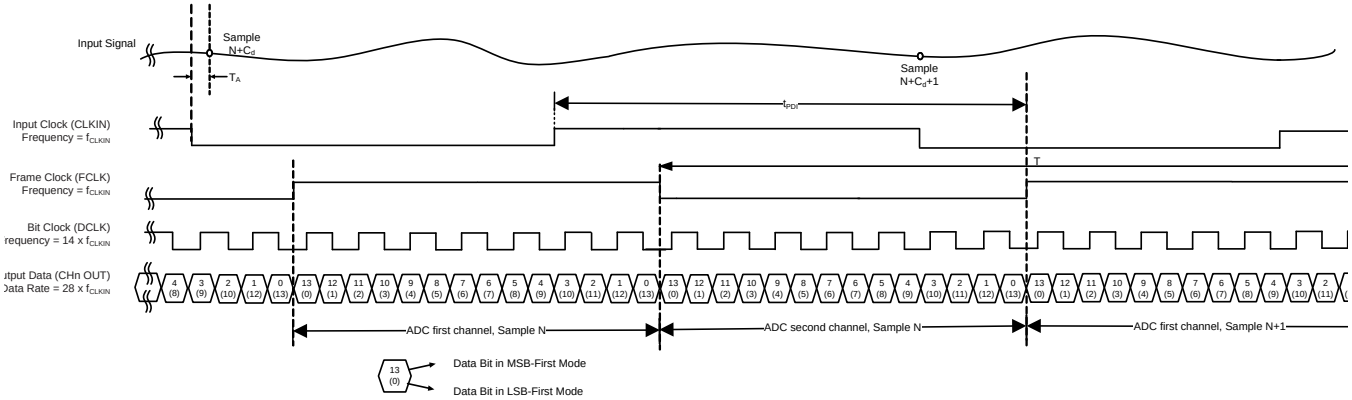


Figure 80. 14-Bit, 2X Data Rate Output Timing Specification

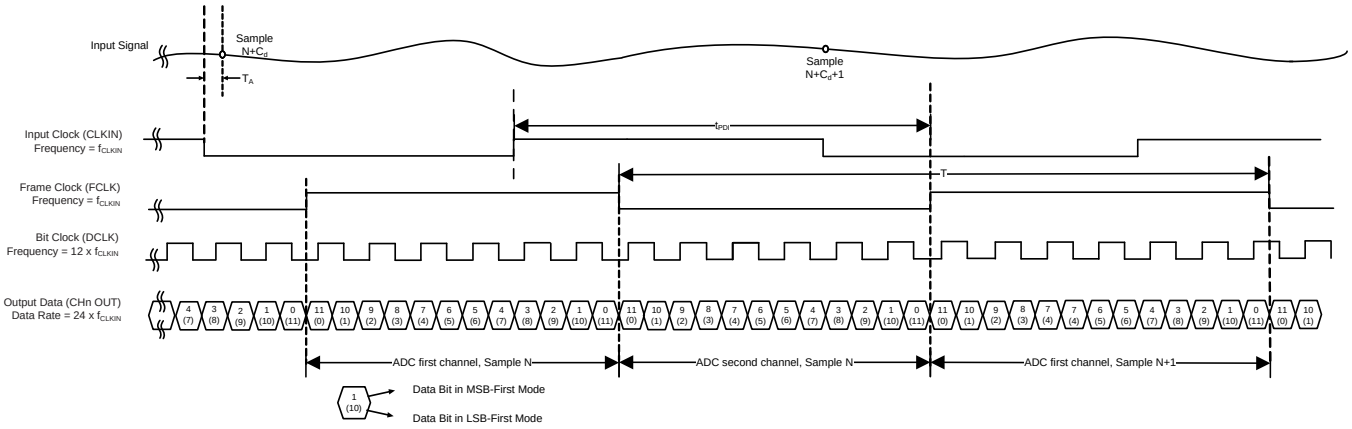


Figure 81. 12-Bit, 2X Data Rate Output Timing Specification

Table 3. Channel and ADC Data Line Mapping (2X Rate)

CHANNELS	MAPPING
DOUT1	ADC data for channels 1 and 2
DOUT2	ADC data for channels 3 and 4
DOUT3	ADC data for channels 5 and 6
DOUT4	ADC data for channels 7 and 8
DOUT5	Idle
DOUT6	Idle
DOUT7	Idle
DOUT8	Idle
DOUT9	ADC data for channels 9 and 10
DOUT10	ADC data for channels 11 and 12
DOUT11	ADC data for channels 13 and 14
DOUT12	ADC data for channels 15 and 16
DOUT13	Idle
DOUT14	Idle
DOUT15	Idle
DOUT16	Idle

9.3.4.4 ADC Register, Digital Processing Description

The ADC has extensive digital processing functionalities that can be used to enhance ADC output performance. The digital processing blocks are arranged as shown in Figure 82.

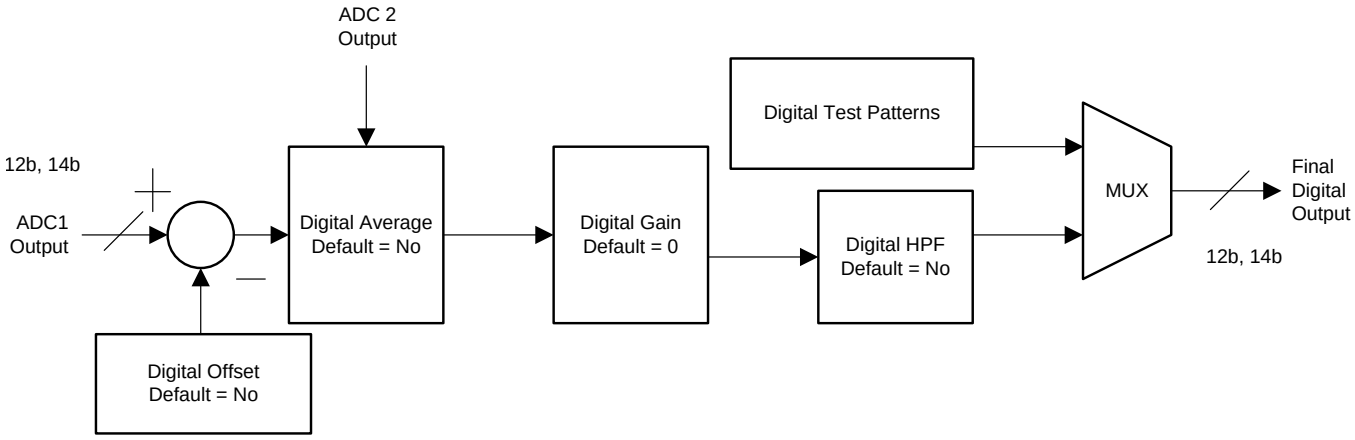


Figure 82. ADC Digital Block Diagram

9.3.4.4.1 Digital Offset

Digital functionality provides for channel offset correction. Setting the DIG_OFFSET_EN bit to 1 enables the subtraction of the offset value from the ADC output. There are two offset correction modes, as shown in Figure 83.

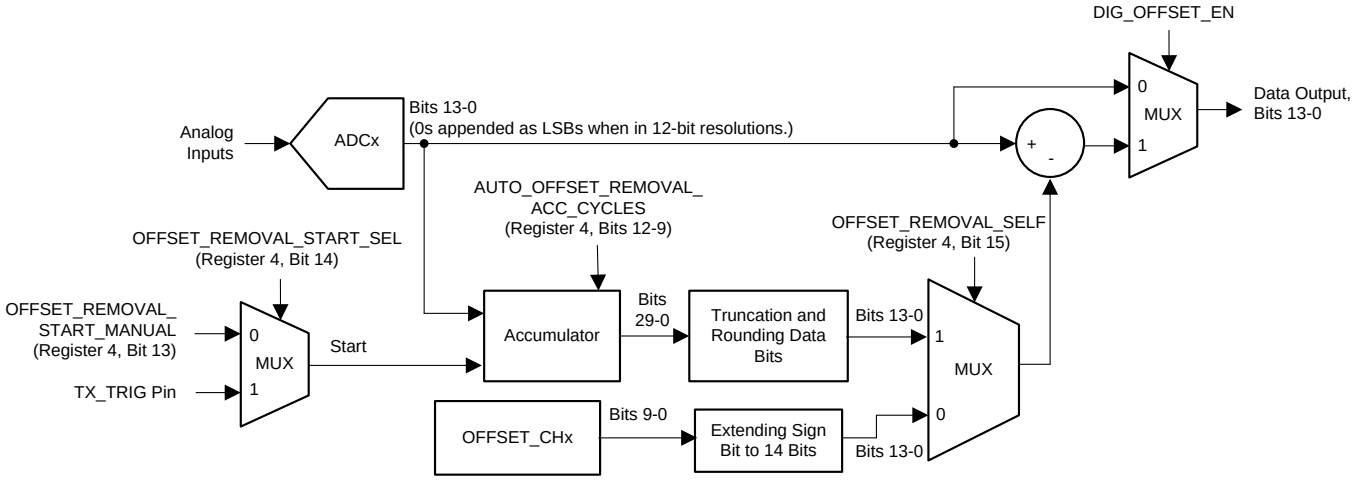


Figure 83. Digital Offset Correction Block Diagram

9.3.4.4.1.1 Manual Offset Correction

If the channel offset is known, the appropriate value can be written in the OFFSET_CHx register (bits 13-0, offset for channel x). The offset value programmed in the OFFSET_CHx register (bits 13-0) subtracts out from the ADC output. The offset of each of the 16 ADC output channels can be independently programmed. The same offset value must be programmed into two adjacent offset registers. For instance, when programming the channel 1 offset value 0000011101, write the same offset value of 0000011101 in registers 13 (bits 9-0) and 14 (bits 9-0).

9.3.4.4.1.2 Auto Offset Correction Mode (Offset Correction using a Built-In Offset Calculation Function)

The auto offset calculation module can be used to calculate the channel offset that is then subtracted from the ADC output. To enable the auto offset correction mode, set the OFFSET_REMOVAL_SELF bit to 1.

In auto offset correction mode the dc component of the ADC output (assumed to be the channel offset) is estimated using a digital accumulator. The ADC output sample set used by the accumulator is determined by a start time or first sample and number of samples to be used. Figure 83 illustrates the options available to determine the accumulator sample set. A high pulse on the TX_TRIG pin or setting the OFFSET_REMOVAL_START_MANUAL register can be used to determine the accumulator first sample. To set the number of samples, the AUTO_OFFSET_REMOVAL_ACC_CYCLES register (bits 12-9) must be programmed according to Table 4.

If a pulse on the TX_TRIG pin is used to set the first sample, additional flexibility in setting the first sample is provided. A programmable delay between the TX_TRIG pulse and first sample can be set by writing to the OFFSET_CORR_DELAY_FROM_TX_TRIG register.

The determined offset value can be read out channel wise. Set the channel number in the AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL register and read the offset value for the corresponding channel in the AUTO_OFFSET_REMOVAL_VAL_RD register.

Table 4. Auto Offset Removal Accumulator Cycles

AUTO_OFFSET_REMOVAL_ACC_CYCLES (Bits 3-0)	NUMBER OF SAMPLES USED FOR OFFSET VALUE EVALUATION
0	2047
1	127
2	255
3	511
4	1023
5	2045
6	4095
7	8191
8	16383
9	32767
10 to 15	65535

9.3.4.4.2 Digital Average

The signal-to-noise ratio (SNR) of the signal chain can be further improved by averaging two channels with the AVG_EN register bit (register 2, bit 11). The way data are transmitted on the digital output lines in this mode is described in Table 5.

Table 5. Channel and ADC Data Line Mapping (Averaging Enabled)

CHANNELS	MAPPING
DOUT1	Average of channels 1 and 2
DOUT2	Average of channels 3 and 4
DOUT3	Average of channels 5 and 6
DOUT4	Average of channels 7 and 8
DOUT5	Idle
DOUT6	Idle
DOUT7	Idle
DOUT8	Idle
DOUT9	Average of channels 9 and 10
DOUT10	Average of channels 11 and 12
DOUT11	Average of channels 13 and 14
DOUT12	Average of channels 15 and 16
DOUT13	Idle
DOUT14	Idle
DOUT15	Idle
DOUT16	Idle

NOTE

Idle LVDS lines are not powered down by default. To save power, these lines can be powered down using corresponding power-down bits (PDN_LVDSx).

The serialization factor must be greater than the ADC resolution to obtain SNR improvement after averaging in 12b resolution.

9.3.4.4.3 Digital Gain

To enable the digital gain block, set DIG_GAIN_EN (register 3, bit 12) to 1. When enabled, the gain value for channel x (where x is from 1 to 16) can be set with the register bits for the corresponding channel (GAIN_CHx, bits 15-11). Gain is given as [0 dB + 0.2 dB × GAIN CHx (bits 15-11)]. For instance, if GAIN_CH5 (bits 15-11) = 3, then channel 5 is increased by 0.6-dB gain. GAIN_CHx (bits 15-11) = 31 produces the same effect as GAIN_CHx (bits 15-11) = 30, which sets the gain of channel x to 6 dB.

9.3.4.4.4 Digital HPF

To enable the digital high-pass filter (HPF) of channel 1 to 8 and 9 to 16, set the DIG_HPF_EN_CH1-8 (register 21, bit 0) and DIG_HPF_EN_CH9-16 (register 45, bit 0) register bits to 1, respectively.

The HPF_CORNER_CHxy register bits (where xy are 1-4, 5-8, 9-12, or 13-16) control the characteristics of a digital high-pass transfer function applied to the output data, based on Equation 3. These bits correspond to bits 4-1 in registers 21, 33, 45, and 57, respectively (these register settings describe the value of K). The valid values of K are 2 to 10. The digital HPF can be used to suppress low-frequency noise. Table 6 shows the cutoff frequency versus K.

$$Y(n) = \frac{2^k}{2^k + 1} [x(n) - x(n-1) + y(n-1)] \quad (3)$$

Table 6. Digital HPF, –1-dB Corner Frequency versus K and f_S

CORNER FREQUENCY (k) (HPF_CORNER_CHxy Register)	CORNER FREQUENCY (kHz)		
	f_S = 40 MSPS	f_S = 50 MSPS	f_S = 65 MSPS
2	2780	3480	4520
3	1490	1860	2420
4	738	230	1200
5	369	461	600
6	185	230	300
7	111	138	180
8	49	61	80
9	25	30	40
10	12.	15	20

HPF output is mapped to ADC resolution bits either by truncation or a round-off operation. By default, the HPF output is truncated to map to the ADC resolution. To enable the rounding operation to map the HPF output to the ADC resolution, set the HPF_ROUND_ENABLE register bit (register 21, bit 5) to 1.

9.3.5 LVDS Synchronization Operation

Different test patterns can be synchronized on the LVDS serialized output lines to help set and program the FPGA timing that receives the LVDS serial output. Of these test patterns, the ramp, toggle, and pseudo-random sequence (PRBS) test patterns can be reset or synchronized by providing a synchronization pulse on the TX_TRIG pin or by setting and resetting a specific register bit. The synchronization pulse on the TX_TRIG pin must meet the setup and hold time constraints with respect to the system clock, as shown in Figure 84.

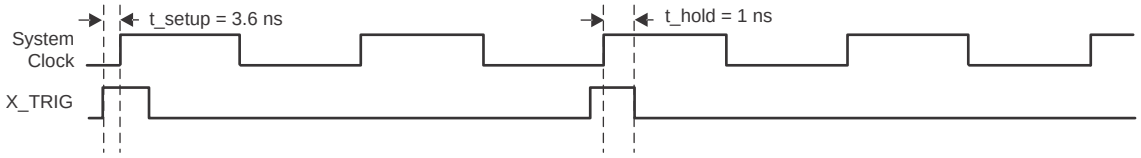


Figure 84. Setup and Hold Time Constraint for the TX_TRIG Signal

The PRBS_SYNC register bit (register 4, bit 7) can be used to synchronize the PRBS sequence. SCLK must be synchronous with the system clock and must meet the setup and hold time constraints with respect to the system clock, as shown in Figure 85.

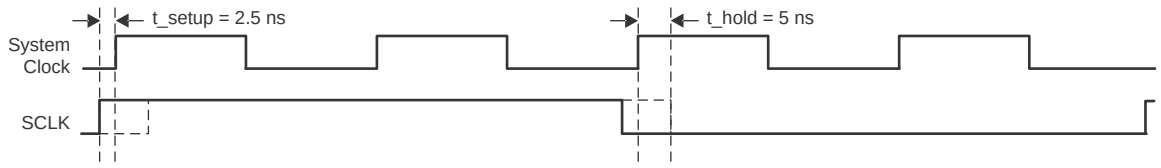


Figure 85. Setup and Hold Time Constraints on SCLK for Using Software, SOFTWARE_RESET, and RESET Functions

9.3.6 Continuous-Wave (CW) Beamformer

The continuous-wave Doppler is a key function in mid-end to high-end ultrasound systems. Compared to the TGC mode, the CW path must handle high dynamic range along with strict phase noise performance. CW beamforming is often implemented in the analog domain because of the strict requirements. Multiple beamforming methods are implemented in ultrasound systems, including a passive delay line, active mixer, and passive mixer. Among these approaches, the passive mixer achieves optimized power and noise. This mixer satisfies the CW processing requirements (such as wide dynamic range, low phase noise, and accurate gain and phase matching).

A simplified CW path block diagram and an in-phase or quadrature (I/Q) channel block diagram are illustrated in Figure 86 and Figure 87, respectively. Each CW channel includes an LNA, a voltage-to-current converter, a switch-based mixer, a shared summing amplifier with a low-pass filter, and clocking circuits.

NOTE

The local oscillator inputs of the passive mixer are cos (ωt) for the I channel and sin (ωt) for the Q channel, respectively. Depending on the application-specific CW Doppler complex FFT processing, swapping the I and Q channels in either the field-programmable gate array (FPGA) or digital signal processor (DSP) can be required in order to obtain correct blood flow direction.

All blocks include well-matched, in-phase, quadrature channels to achieve good image frequency rejection as well as beamforming accuracy. As a result, the image rejection ratio from an I/Q channel is better than –46 dBc, which is desired in ultrasound systems.

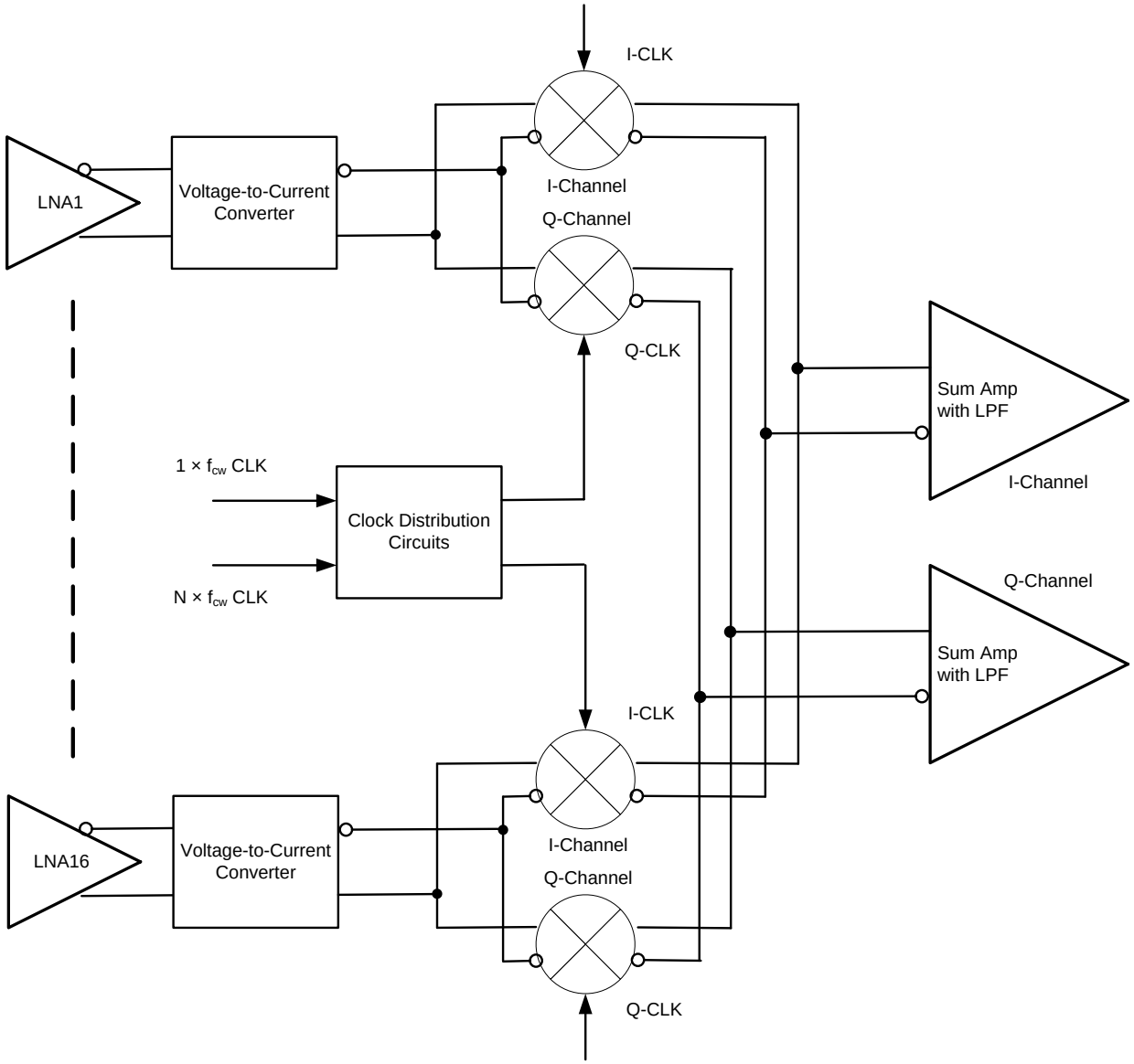
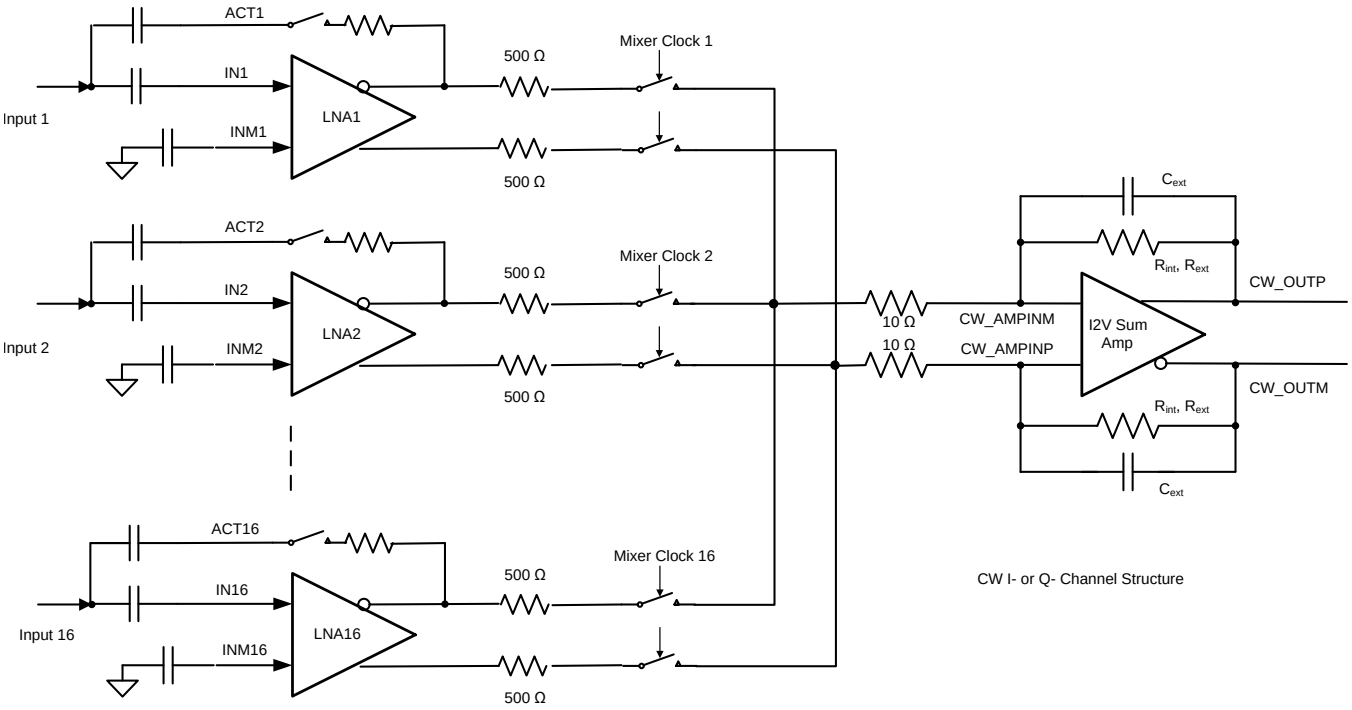


Figure 86. Simplified Block Diagram of the CW Path



NOTE: The 10-Ω to 15-Ω resistors at CW_AMPINM and CW_AMPINP result from the internal device routing and can create slight attenuation.

Figure 87. A Complete In-Phase or Quadrature-Phase Channel

The CW mixer in the device is passive and switch based; the passive mixer adds less noise than active mixers. The CW mixer achieves good performance at low power. Figure 88 and the calculations of Equation 4 describe the principles of the mixer operation. The LO(t) is square-wave based and includes odd harmonic components.

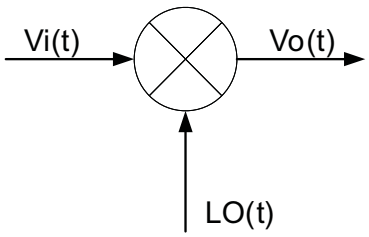


Figure 88. Mixer Operation Block Diagram

$$Vi(t) = \sin(\omega_0 t + \omega_d t + \varphi)$$

$$LO(t) = \frac{4}{\pi}\left[\sin(\omega_0 t) + \frac{1}{3}\sin(3\omega_0 t) + \frac{1}{5}\sin(5\omega_0 t) \ldots\right] - Fourier\ series\ of\ square\ wave$$

$$Vo(t) = \frac{2}{\pi}[\cos(\omega_d t + \varphi) - \cos(2\omega_0 t + \omega_d t + \varphi) + \ldots] \quad (4)$$

where:

- Vi(t), Vo(t), and LO(t) are the input, output, and local oscillator (LO) signals for a mixer, respectively.

From Equation 4, the third- and fifth-order harmonics from the LO can interface with the third- and fifth-order harmonic signals in the Vi(t) or the noise around the third- and fifth-order harmonics in the Vi(t). Therefore. the mixer performance is degraded. In order to eliminate this side effect resulting from the square-wave demodulation, a proprietary harmonic suppression circuit is implemented in the device. The third- and fifth-order harmonic components from the LO can be suppressed by over 12 dB. Thus, the LNA output noise around the third- and fifth-order harmonic bands are not down-converted to base band. Hence, a better noise figure is achieved. The conversion loss of the mixer is approximately –4 dB, which is derived from $20\log_{10} 2 / \pi$.

The mixed current outputs of the 16 channels are summed together internally. An internal low-noise operational amplifier is used to convert the summed current to a voltage output. The internal summing amplifier is designed to accomplish low power consumption, low noise, and ease of use. CW outputs from multiple devices can be further combined on the system board to implement a CW beamformer with more than 16 channels.

Multiple clock options are supported in the device CW path. Two CW clock inputs are required: an N × f_{cw} clock and a 1 × f_{cw} clock, where f_{cw} is the CW transmitting frequency and N can be 16, 8, 4, or 1. The most convenient system clock solution can be selected for the device. In the 16 × f_{cw} and 8 × f_{cw} modes, the third- and fifth-order harmonic suppression feature can be supported. Thus, the 16 × f_{cw} and 8 × f_{cw} modes achieve better performance than the 4 × f_{cw} and 1 × f_{cw} modes.

9.3.6.1 16 × f_{cw} Mode

The 16 × f_{cw} mode achieves the best phase accuracy compared to other modes. This mode is the default mode for CW operation. In this mode, 16 × f_{cw} and 1 × f_{cw} clocks are required. 16 × f_{cw} generates LO signals with 16 accurate phases. Multiple devices can be synchronized by the 1 × f_{cw} (that is, LO signals in multiple AFEs can have the same starting phase). The phase noise spec is critical only for 16X clock. 1X clock is for synchronization only and doesn't require low phase noise. Please see the phase noise requirement in the section of application information.

The top-level clock distribution diagram is shown in Figure 89. Each mixer clock is distributed through a 16 × 16 cross-point switch. The inputs of the cross-point switch are 16 different phases of the 1X clock. TI recommends aligning the 1 × f_{cw} and 16 × f_{cw} clocks; see Figure 90.

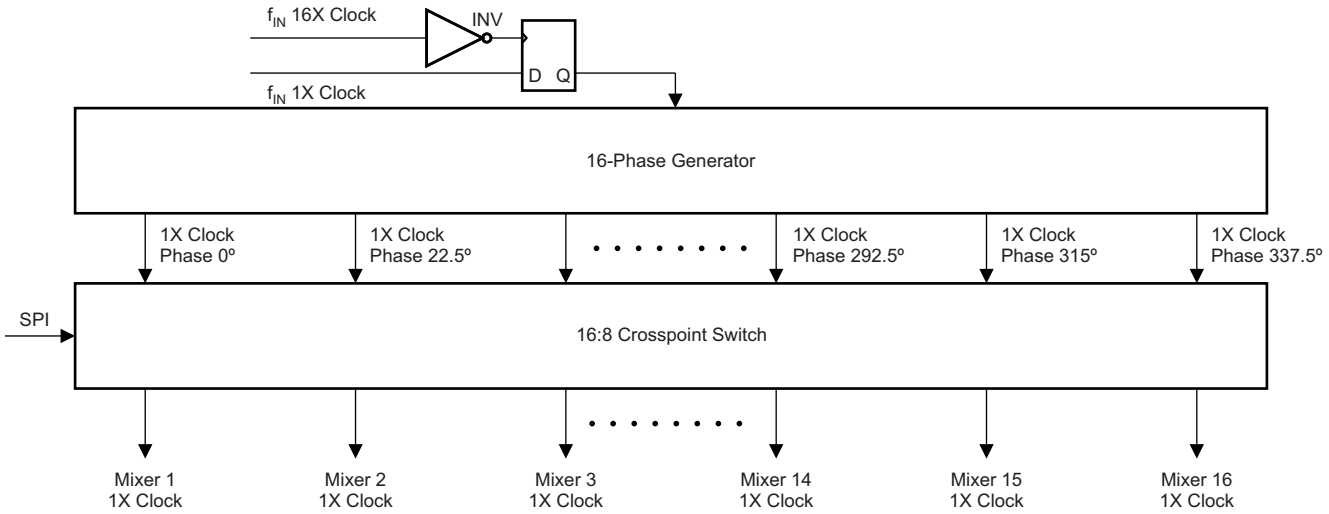


Figure 89. CW Clock Distribution Scheme

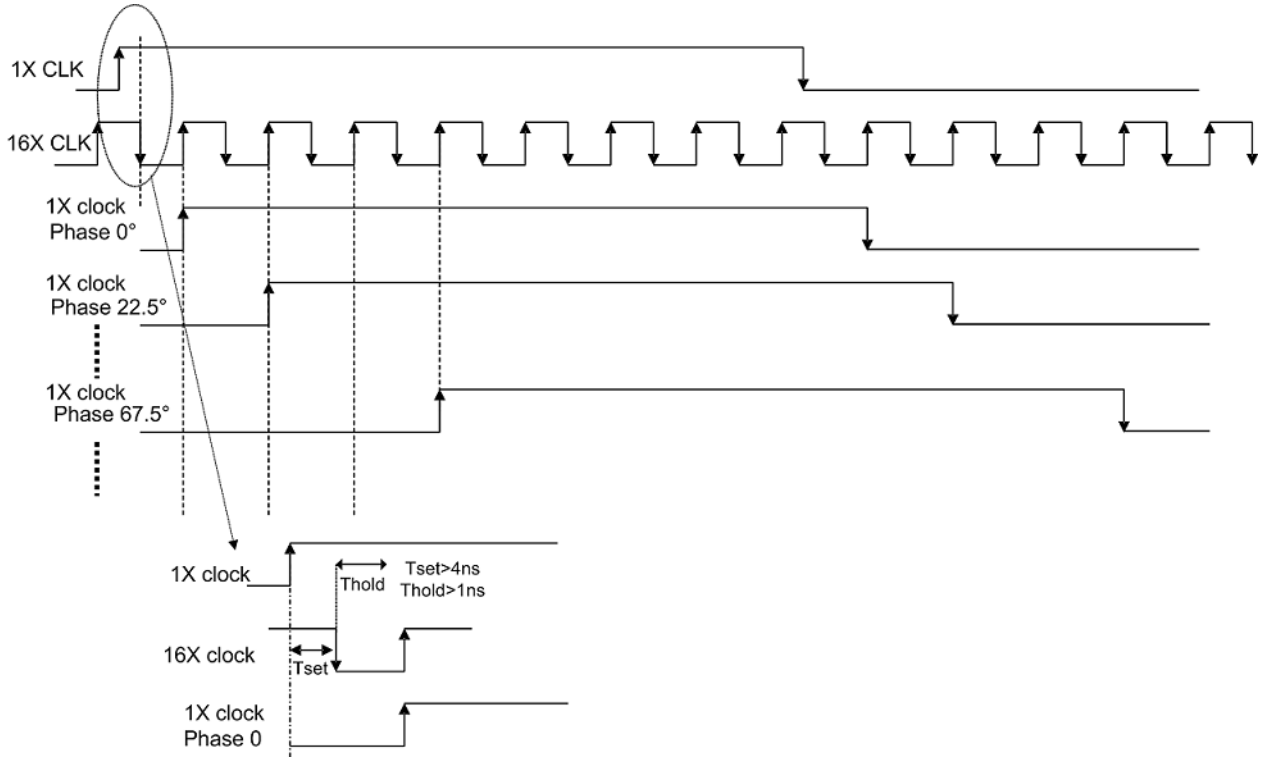


Figure 90. 1X and 16X CW Clock Timing Diagram

The cross-point switch distributes the clocks with an appropriate phase delay to each mixer. For example, Vi(t) is a received signal with a delay of (1 / 16) T. Apply a delayed LO(t) to the mixer in order to compensate for the (1 / 16) T delay. Thus, a 22.5º delayed clock, that is 2π / 16 is selected for this channel. The mathematic calculation is expressed in Equation 5.

$$Vi(t) = \sin\left[\omega_0\left(t + \frac{1}{16f_0}\right) + \omega_d t\right] = \sin\left[\omega_0 t + 22.5° + \omega_d t\right]$$

$$LO(t) = \frac{4}{\pi}\sin\left[\omega_0\left(t + \frac{1}{16f_0}\right)\right] = \frac{4}{\pi}\sin\left[\omega_0 t + 22.5°\right]$$

$$Vo(t) = \frac{2}{\pi}\cos\left(\omega_d t\right) + f\left(\omega_n t\right) \quad (5)$$

Vo(t) represents the demodulated Doppler signal of each channel. When the Doppler signals from N channels are summed, the signal-to-noise ratio improves. ω_d is the Doppler frequency, ω_o is the local oscillator frequency, and ω_n represents the high-frequency components that are filtered out.

9.3.6.2 8 × f_{cw} and 4 × f_{cw} Modes

The 8 × f_{cw} and 4 × f_{cw} modes are alternative modes when a higher frequency clock solution (that is, a 16 × f_{cw} clock) is not available in the system. The block diagram of these two modes is shown in Figure 91.

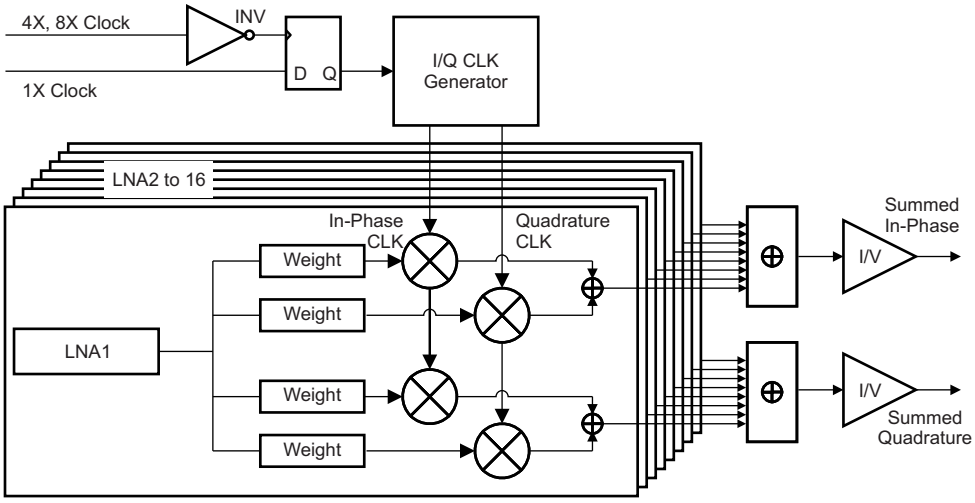


Figure 91. 8 × f_{cw} and 4 × f_{cw} Block Diagram

Good phase accuracy and matching are also maintained. The quadrature clock generator is used to create in-phase and quadrature clocks with exactly a 90° phase difference. The only difference between the 8 × f_{cw} and 4 × f_{cw} modes is the accessibility of the third- and fifth-order harmonic suppression filter. In the 8 × f_{cw} mode, the suppression filter can be supported. In both modes, a (1 / 16) T phase delay resolution is achieved by weighting the in-phase and quadrature paths correspondingly. For example, if a delay of (1 / 16) T or 22.5° is targeted, the weighting coefficients must follow Equation 6, assuming I_{in} and Q_{in} are sin ($\omega_0 t$) and cos ($\omega_0 t$), respectively.

$$I_{delayed}(t) = I_{in}\cos\left(\frac{2\pi}{16}\right) + Q_{in}\sin\left(\frac{2\pi}{16}\right) = I_{in}\left(t + \frac{1}{16 f_0}\right)$$
$$Q_{delayed}(t) = Q_{in}\cos\left(\frac{2\pi}{16}\right) - I_{in}\sin\left(\frac{2\pi}{16}\right) = Q_{in}\left(t + \frac{1}{16 f_0}\right) \quad (6)$$

Therefore, after the I/Q mixers, phase delay in the received signals is compensated. The mixer outputs from all channels are aligned and added linearly to improve the signal-to-noise ratio. TI recommends meeting the timing between the 1 × f_{cw} clock and 4 × f_{cw} or 8 × f_{cw} clock; see Figure 92.

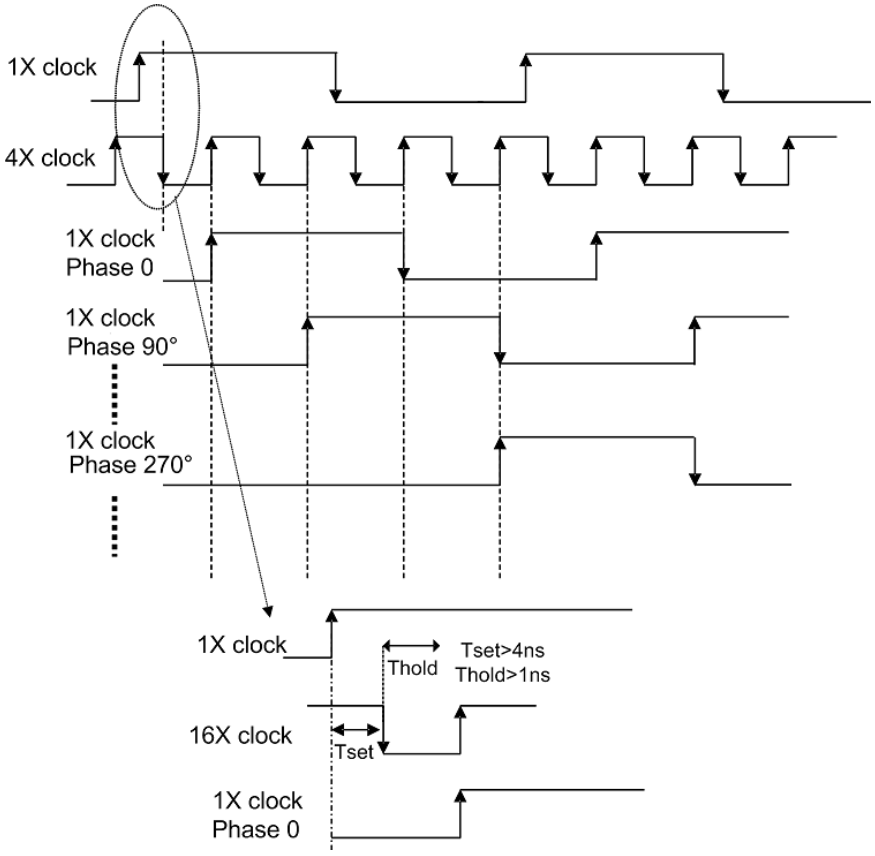


Figure 92. 8 × f_{cw} and 4 × f_{cw} Timing Diagram

9.3.6.3 1 × f_{cw} Mode

The 1 × f_{cw} mode requires in-phase and quadrature clocks with low phase noise specifications. A block diagram for this mode is shown in Figure 93. The (1 / 16) T phase delay resolution is also achieved by weighting the in-phase and quadrature signals, as described in the *8 × f_{cw} and 4 × f_{cw} Modes* section.

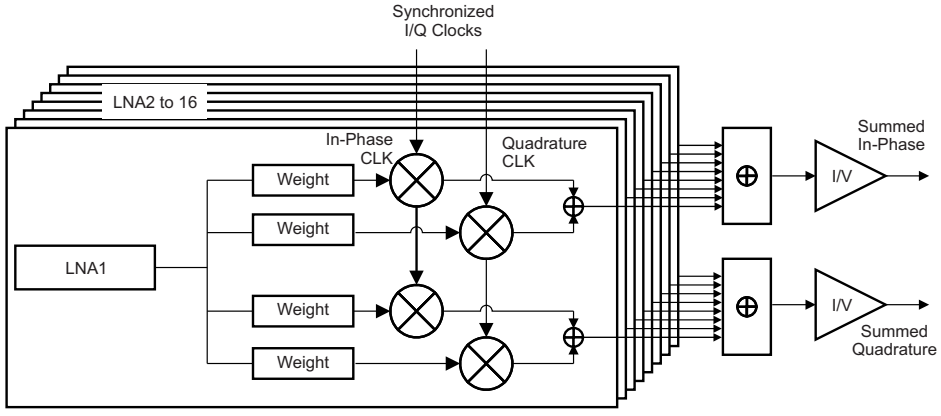


Figure 93. 1 × f_{cw} Mode Block Diagram

9.3.6.4 CW High-Pass Filter

The summing amplifier is implemented in the device to sum and convert 16-channel mixer current outputs to a differential voltage output. This summing amplifier has five internal gain adjustment resistors that can provide 32 different gain settings; see Table 80. System designers can easily adjust the CW path gain, depending on signal strength and transducer sensitivity. For any other gain values an external resistor option is supported. The gain of the summation amplifier is determined by the ratio between the 2000 Ω resistors after the LNA and internal or external resistor network (R_S). Thus, the matching between these resistors plays a more important role than the absolute resistor values. Better than 1% matching is achieved on-chip. The absolute resistor tolerance can be higher, depending on the process variation. If external resistors are used, the gain error between the I/Q channels or among multiple AFEs can increase. TI recommends using internal resistors to set the gain in order to achieve better gain matching (across channels and multiple AFEs).

The device provides an extra feature to suppress undesired low-frequency signal presents at the CW output, which is achieved by implementing an HPF at the CW output using the scheme shown in Figure 94.

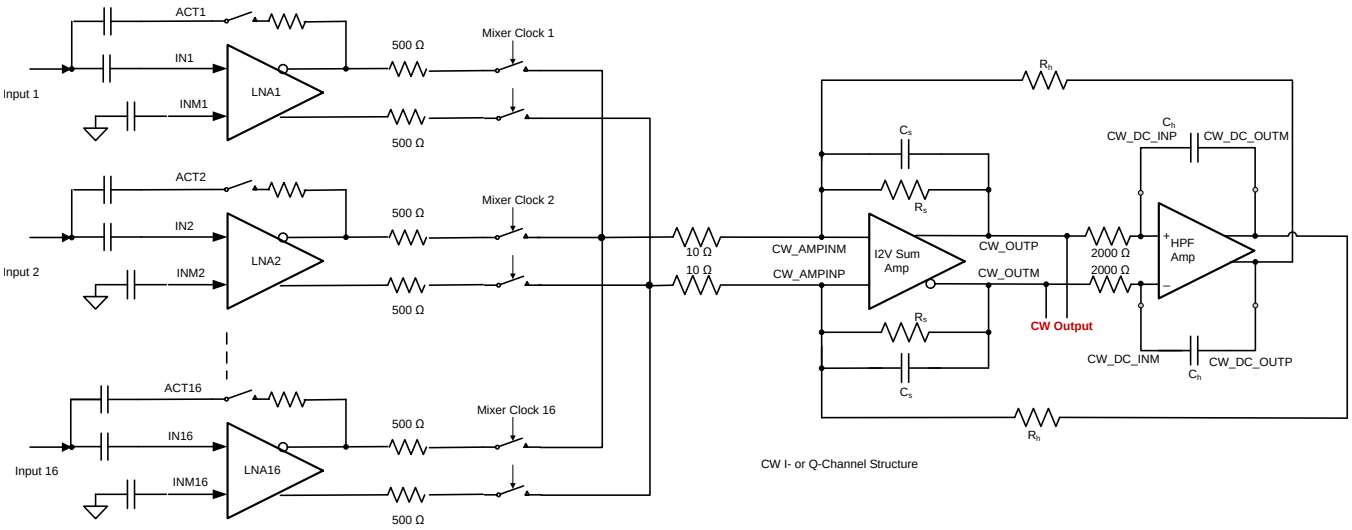


Figure 94. CW Summing Amplifier and High-Pass Filter Implementation

When this feature is enabled, the overall transfer function of the CW summing amplifier across frequency is as shown in Figure 95.

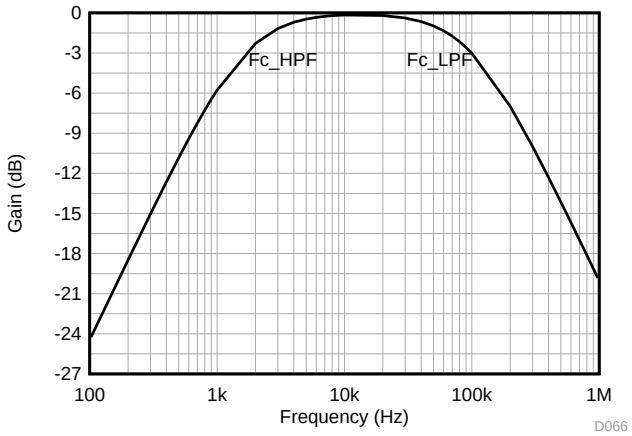


Figure 95. CW Summing Amplifier Transfer Function

The high-pass corner and low-pass corner shown in Figure 95 is given by Equation 7 and Equation 8, respectively:

$$Fc\_hpf = R_s / (2 \times \pi \times R_h \times C_h \times 2000\ \Omega) \quad (7)$$

$$Fc\_lpf = 1 / (2 \times \pi \times R_s \times C_s) \quad (8)$$

The following rules can be used to calculate the value of different components:

1. R_s is the resistor value determined by how much signal gain is needed.
2. C_s is selected depending upon the value of Fc_lpf.
3. R_h is determined by the amplitude of the undesired low-frequency signal required to be rejected. For instance, suppose that without enabling the CW HPF feature, the peak-to-peak amplitude of the low-frequency signal at the CW summing amplifier output is given by V_{opp}. Then the value of R_h has the relationship shown in Equation 9. The previous constraint occurs because the CW HPF amplifier output can only swing up to 4 V_{pp}.

$$R_h < 4 \times R_s / V_{opp} \quad (9)$$

NOTE

Higher resistance values of R_h provide better noise performance.

4. C_h is the selected value of this capacitor depending upon the value of Fc_hpf.

An alternative current-summing circuit is shown in Figure 96. However, this circuit only achieves good performance when a lower noise operational amplifier is available compared to the device internal summing differential amplifier. This current output mode requires the internal summing amplifier to be powered down (register 198, bit 9) and R_s set to 0 Ω.

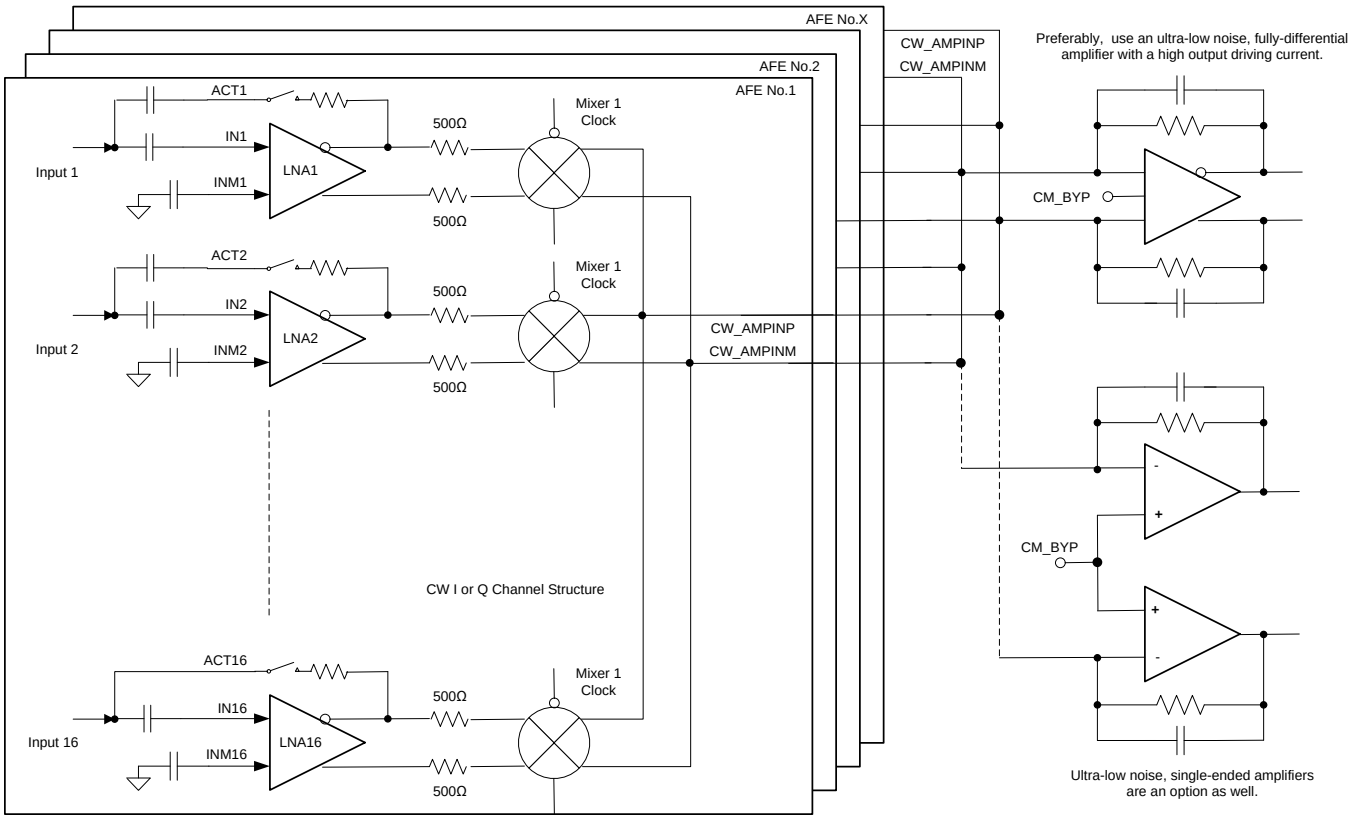


Figure 96. CW Circuit With Multiple Devices (Current Output Mode, CM_BYP = 1.5 V)

The CW I/Q channels are well matched internally to suppress image frequency components in the Doppler spectrum. Use low tolerance components and precise operational amplifiers for achieving good matching in the external circuits as well.

NOTE

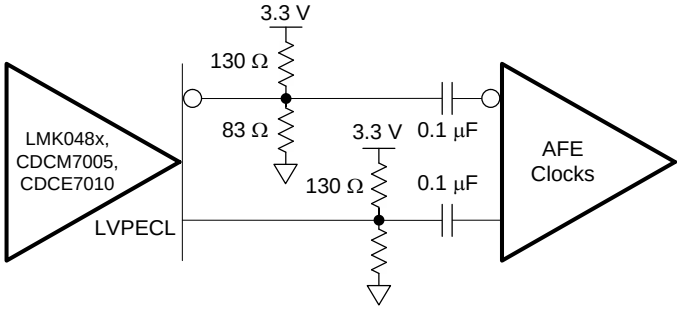
The local oscillator inputs of the passive mixer are cos (ω_t) for the I channel and sin (ω_t) for the Q channel, respectively. Depending on the application-specific CW Doppler complex FFT processing, swapping I/Q channels in the FPGA or DSP may be needed in order to obtain correct blood flow directions.

9.3.6.5 CW Clock Selection

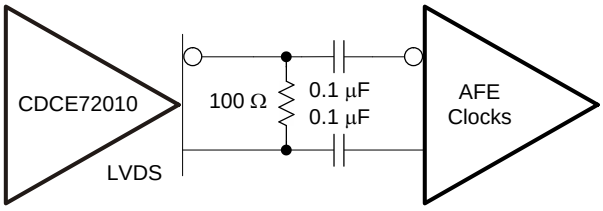
The device can accept differential LVDS, LVPECL, and other differential clock inputs as well as a single-ended CMOS clock. An internally-generated V_{CM} of 2.5 V is applied to CW clock inputs (that is, CLKP_16X, CLKM_16X and CLKP_1X, CLKM_1X). Because this 2.5-V V_{CM} is different from the one used in standard LVDS or LVPECL clocks, ac coupling is required between clock drivers and the device CW clock inputs. When the CMOS clock is used, tie CLKM_1X and CLKM_16X to ground. Common clock configurations are shown in Figure 97. Appropriate termination is recommended to achieve good signal integrity.

NOTE

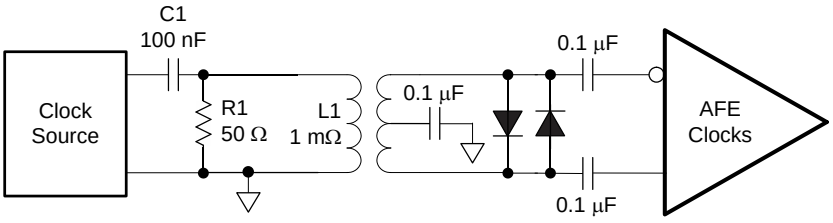
The configurations shown in Figure 97 can also be used as a reference for the ADC clock input.



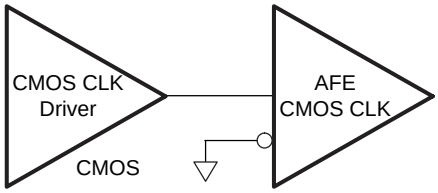
(a) LVPECL Configuration



(b) LVDS Configuration



(c) Transformer-Based Configuration



(d) CMOS Configuration

Figure 97. Clock Configurations

The combination of the clock noise and the CW path noise can degrade CW performance. The internal clocking circuit is designed for achieving excellent phase noise required by CW operation. The phase noise of the device CW path is better than 160 dBc/Hz at a 1-kHz offset. Consequently, the phase noise of the mixer clock inputs must be better than 160 dBc/Hz.

In the 16, 8, and 4 × f_{cw} operations modes, a low-phase noise clock is required for the 16, 8, and 4 × f_{cw} clocks (that is, the CLKP_16X and CLKM_16X pins) in order to maintain good CW phase noise performance. The 1 × f_{cw} clock (that is, the CLKP_1X and CLKM_1X pins) is only used to synchronize the multiple device chips and is not used for demodulation. Thus, the 1 × f_{cw} clock phase noise is not a concern. However, in the 1 × f_{cw} operation mode, low-phase noise clocks are required for both the CLKP_16X, CLKM_16X and CLKP_1X, CLKM_1X pins because both are used for mixer demodulation. In general, a higher slew rate clock has lower phase noise. Thus, clocks with high amplitude and fast slew rate are preferred in CW operation. In the CMOS clock mode, a 5-V CMOS clock can achieve the highest slew rate.

Clock phase noise can be improved by a divider as long as the divider phase noise is lower than the target phase noise. The phase noise of a divided clock can be improved approximately by a factor of $20\log_N$ dB, where N is the dividing factor of 16, 8, or 4. If the target phase noise of the mixer LO clock 1 × f_{cw} is 160 dBc/Hz at a 1-kHz off the carrier, the 16 × f_{cw} clock phase noise must be better than 160 – 20log16 = 136 dBc/Hz. TI's jitter cleaners LMK048x, CDCM7005, and CDCE72010 exceed this requirement and can be selected to work with the device. In the 4X and 1X modes, higher quality input clocks are expected to achieve the same performance because N is smaller. Thus, the 16X mode is a preferred mode because this mode reduces the phase noise requirement for the system clock design. In addition, the phase delay accuracy is specified by the internal clock divider and distribution circuit.

Note that in the 16X operation mode, the CW operation range is limited to 8 MHz as a result of the 16X clock. The maximum clock frequency for the 16X clock is 128 MHz. In the 8X, 4X, and 1X modes, higher CW signal frequencies up to 15 MHz can be supported with a small degradation in performance. For example, the phase noise is degraded by 9 dB at 15 MHz, compared to 2 MHz.

As the channel number in a system increases, clock distribution becomes more complex. Using one clock driver output is not preferred to drive multiple AFEs because the clock buffer load capacitance increases by a factor of N. The section can be used as a reference for the system clock configuration. When clock phase noise is not a concern (for example, the 1 × f_{cw} clock in the 16, 8, and 4 × f_{cw} operation modes), one clock driver output can excite more than one device. Nevertheless, special considerations must be applied for such a clock distribution network design. Preferably, all clocks are generated from the same clock source in typical ultrasound systems (such as 16 × f_{cw} , 1 × f_{cw} clocks, audio ADC clocks, RF ADC clock, pulse repetition frequency signal, frame clock, and so on). By using the same clock source, interference resulting from clock asynchronization can be minimized.

9.3.6.6 CW Supporting Circuits

As a general practice in the CW circuit design, in-phase and quadrature channels must be strictly symmetrical by using well-matched layout and high-accuracy components. In systems, additional high-pass wall filters (20 Hz to 500 Hz) and low-pass audio filters (10 kHz to 100 kHz) with multiple poles are usually needed. Because the CW Doppler signal ranges from 20 Hz to 20 kHz, noise under this range is critical. Consequently, low-noise audio operational amplifiers are suitable to build these active filters for CW post-processing (that is, the OPA1632, OPA2211, or THS4131). More filter design techniques can be found at www.ti.com. The TI active filter design tool is the WEBENCH® Filter Designer. The filtered audio CW I/Q signals are sampled by audio ADCs and processed by the DSP or PC. Although CW signal frequency is from 20 Hz to 20 KHz, higher sampling rate ADCs are still preferred for further decimation and SNR enhancement. Because of the large dynamic range of CW signals, high-resolution ADCs (≥ 16 bits) are required [such as the ADS8413 (2 MSPS, 16 bits, 92-dBFS SNR) and the ADS8472 (1 MSPS, 16 bits, 95-dBFS SNR)]. ADCs for in-phase and quadrature-phase channels must be strictly matched, not only for amplitude matching but also for phase matching in order to achieve the best I/Q matching. In addition, the in-phase and quadrature ADC channels must be sampled simultaneously.

9.3.6.7 Power Management

Power management plays a critical role to extend battery life and to ensure a long operation time. The device has a fast and flexible power-up and power-down control that can maximize battery life. The device can be powered down or up through external pins or internal registers.

This section describes the functionality of different power-down pins and register bits available in the device. The device can be divided in two major blocks, the VCA and ADC; see Figure 98 and Figure 99.

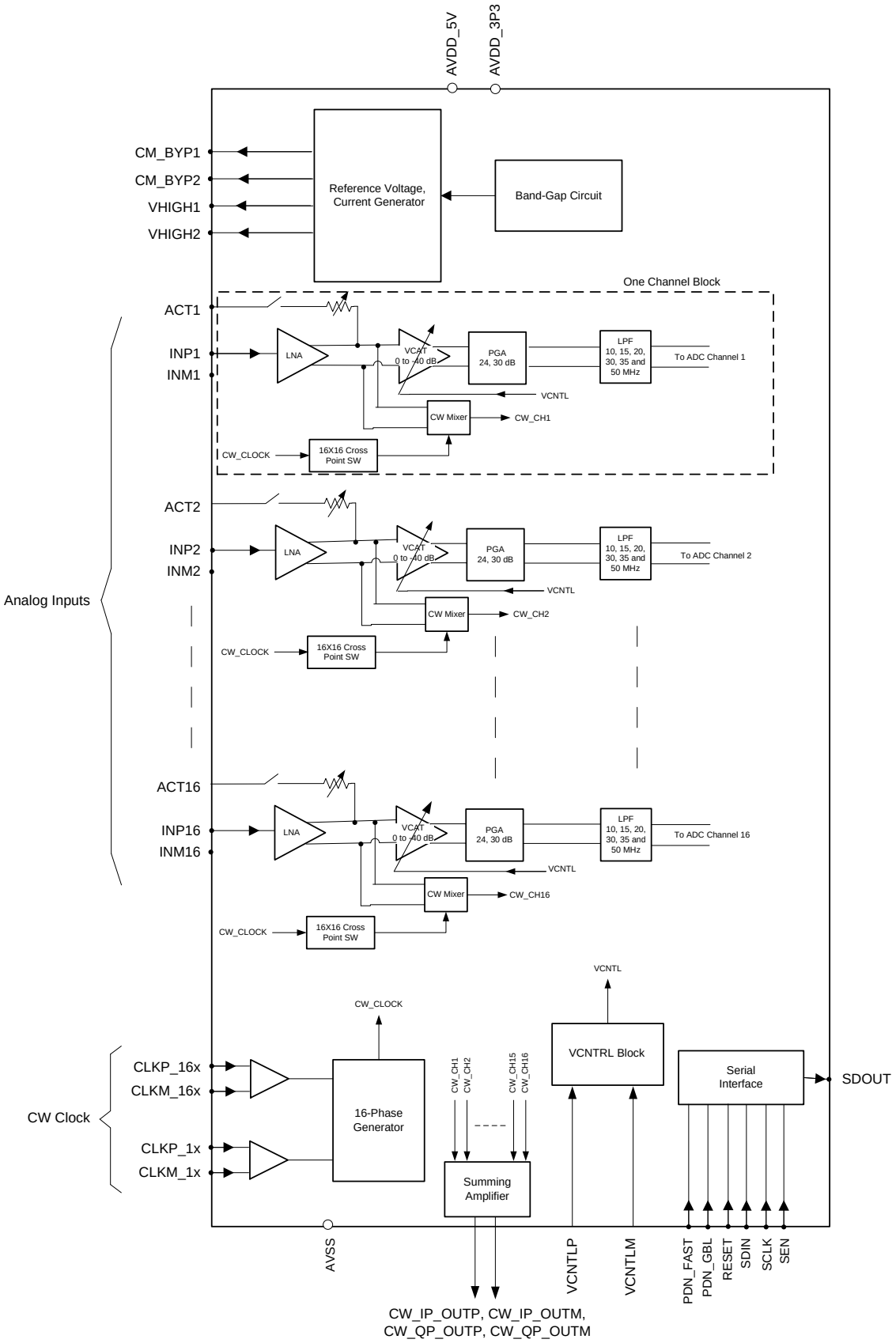


Figure 98. VCA Block Diagram

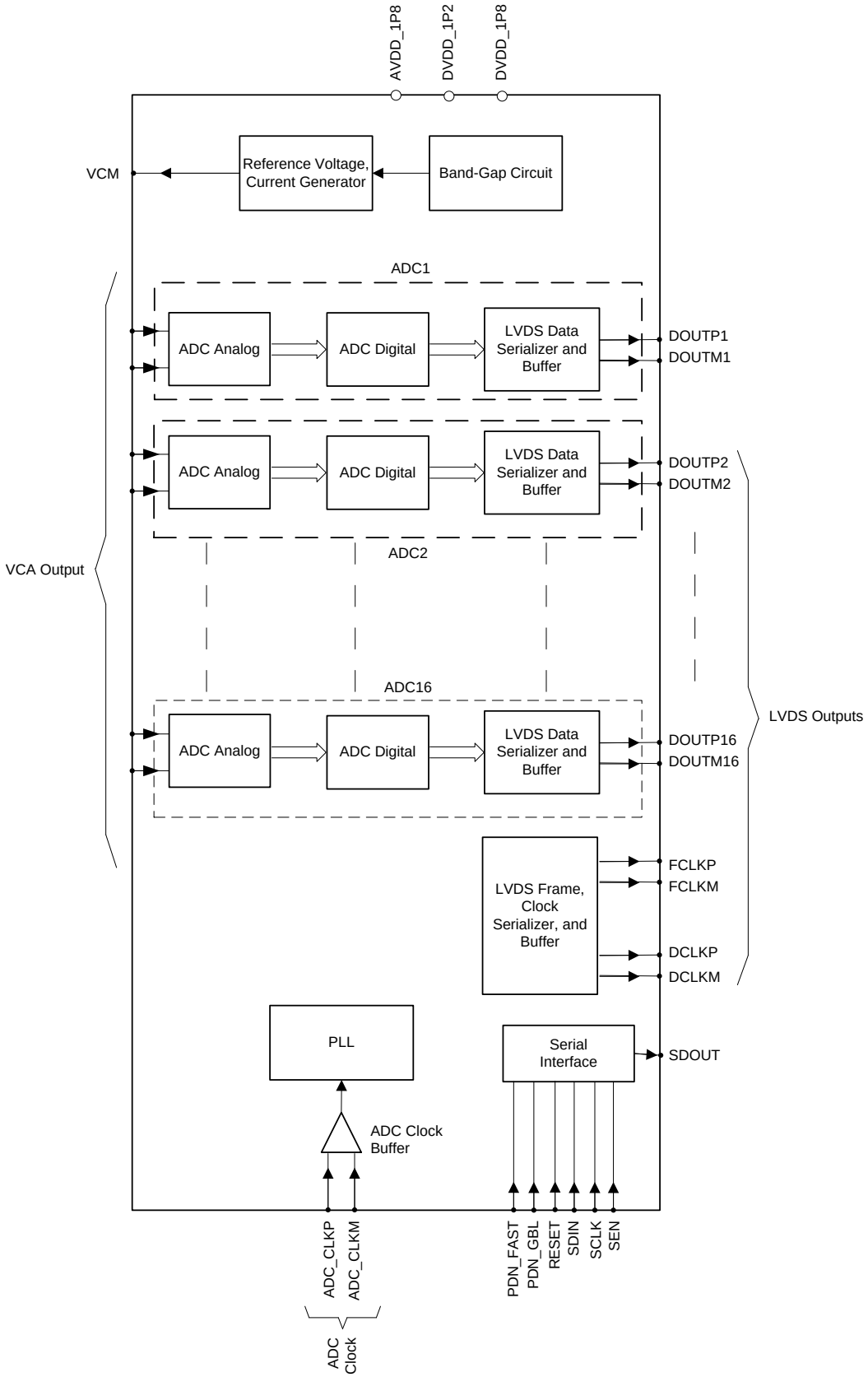


Figure 99. ADC Block Diagram

9.3.6.7.1 VCA

The VCA consists of the following blocks:

- Band-gap circuit,
- Serial interface,
- Reference voltage and current generator,
- A total of 16 channel blocks (each channel block includes an LNA, VCAT, PGA, LPF, CW mixer, and a 16X16 cross-point switch),
- VCNTRL block,
- Phase generator for CW mode, and
- CW summing amplifier.

Of these VCA blocks, only the band gap and serial interface block cannot be powered down by using power-down pins or bits. Table 7 lists all the VCA blocks that are powered down using various pin and bit settings.

Table 7. VCA Power-Down Mode Descriptions

NAME	TYPE (Pin or Register)	LNA	VCAT + PGA + LPF	CW MIXER	16X16 CROSS-POINT SWITCH	REFERENCE	VCNTRL BLOCK	CW SUMMING AMPLIFIER + PHASE GENERATOR	CHANNEL
PDN_GBL	Pin	Yes(1)	Yes	Yes	Yes	Yes	Yes	Yes	All(2)
GBL_PDWN	Register 197, bit 15	Yes	Yes	Yes	Yes	Yes	Yes	Yes	All
PDN_FAST	Pin	Yes	Yes	Yes	Yes	No	No	Yes	All
FAST_PDWN	Register 197, bit 14	Yes	Yes	Yes	Yes	No	No	Yes	All
PDNCHxx	Register 197, bits 7-0, register 213, bits 7-0	Yes	Yes	Yes	Yes	No	No	No	Individual
PDWN_LNA	Register 197, bit 13	Yes	No	No	No	No	No	No	All
PDWN_VCA_PGA	Register 197, bit 12	No	Yes	No	No	No	No	No	All

(1) Yes = powered down. No = active.
(2) All = all channels are powered down. Individual = only a single channel is powered down, depending upon the corresponding bit.

If more than one bit is simultaneously enabled, then all blocks listed as *Yes* for each bit setting is powered down.

9.3.6.7.2 ADC

The ADC consists of the following blocks:

- Band-gap circuit,
- Serial interface,
- Reference voltage and current generator,
- ADC analog block that performs a sampling and conversion,
- ADC digital block that includes all the digital post processing blocks (such as the offset, gain, digital HPF, and so forth),
- LVDS data serializer and buffer that converts the ADC parallel data to a serial stream.
- LVDS frame and clock serializer and buffer,
- PLL (phase-locked loop) that generates a high-frequency clock for both the ADC and serializer.

Of all these blocks, only the band gap and serial interface block cannot be power down using power-down pins or bits. Table 8 lists which blocks in the ADC are powered down using different pins and bits.

Table 8. Power-Down Modes Description for the ADC

NAME	TYPE (Pin or Register)	ADC ANALOG	ADC DIGITAL	LVDS DATA SERIALIZER, BUFFER	LVDS FRAME AND CLOCK SERIALIZER, BUFFER	REFERENCE + ADC CLOCK BUFFER	PLL	CHANNEL
PDN_GBL	Pin	Yes(1)	Yes	Yes	Yes	Yes	Yes	All(2)
GLOBAL_PDN	Register 1, bit 0	Yes	Yes	Yes	Yes	Yes	Yes	All
PDN_FAST	Pin	Yes	Yes	Yes	No	No	No	All
DIS_LVDS	Register 1, bit 5	No	No	Yes	Yes	No	No	All
PDN_ANA_CHx	Registers 24 (bits 7-4), 36 (bits 7-4), 48 (bits 7-4), and 60 (bits 7-4)	Yes	No	No	No	No	No	Individual
PDN_DIG_CHx	Registers 4 (bits 15-12), 36 (bits 15-12), 48 (bits 15-12), and 60 (bits 15-12)	No	Yes	No	No	No	No	Individual
PDN_LVDSx	Register 24 (bits 11-8), 36 (bits 11-8), 48 (bits 11-8), and 60 (bits 11-8)	No	No	Yes	No	No	No	Individual

(1) Yes = powered down. No = active.
(2) All = all channels are powered down. Individual = only a single channel is powered down, depending upon the corresponding bit.

9.4 Device Functional Modes

9.4.1 ADC Test Pattern Mode

9.4.1.1 Test Patterns

9.4.1.1.1 LVDS Test Pattern Mode

The ADC data coming out of the LVDS outputs can be replaced by different kinds of test patterns. The different test patterns are described in Table 9.

Table 9. Description of LVDS Test Patterns

TEST PATTERN MODE	PROGRAMMING THE MODE		TEST PATTERNS REPLACE(1)
	THE SAME PATTERN MUST BE COMMON TO ALL DATA LINES (DOUT)	THE PATTERN IS SELECTIVELY REQUIRED ON ONE OR MORE DATA LINE (DOUT)	
All 0s	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0].	Zeros in all bits (00000000000000)
All 1s	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0].	Ones in all bits (11111111111111)
Deskew	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0].	The ADC data are replaced by alternate 0s and 1s (01010101010101)
Sync	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0].	ADC data are replaced by half 1s and half 0s (11111110000000)
Custom	Set the mode using PAT_MODES[2:0]. Set the desired custom pattern using the CUSTOM_PATTERN register control.	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0].	The word written in the CUSTOM_PATTERN control (taken from the MSB side) replaces ADC data. (For instance, CUSTOM_PATTERN = 1100101101011100 and ADC data = 11001011010111 when the serialization factor is 14.)
Ramp	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0].	The ADC data are replaced by a word that increments by 1 LSB every conversion clock starting at negative full-scale, increments until positive full-scale, and wraps back to negative full-scale. The step size of the ramp pattern is function of ADC resolution (N) and serialization factor (S) and is given by $2^{(S-N)}$.
Toggle	Set the mode using PAT_MODES[2:0]	Set PAT_SELECT_IND = 1. To output the pattern on the DOUTx line, select PAT_LVDSx[2:0].	The ADC data alternate between two words that are all 1s and all 0s. At each setting of the toggle pattern, the start word can either be all 0s or all 1s. (Alternate between 11111111111111 and 00000000000000.)
PRBS	Set SEL_PRBS_PAT_GBL = 1. Select either custom or ramp pattern with PAT_MODES[2:0]. Enable PRBS mode using PRBS_EN. Select the desired PRBS mode using PRBS_MODE. Reset the PRBS generator with PRBS_SYNC.	Set PAT_SELECT_IND = 1. Select either custom or ramp pattern with PAT_LVDSx[2:0]. Enable PRBS mode on DOUTx with the PAT_PRBS_LVDSx control. Select the desired PRBS mode using PRBS_MODE. Reset the PRBS generator with PRBS_SYNC.	A 16-bit pattern is generated by a 23-bit (or 9-bit) PRBS pattern generator (taken from the MSB side) and replaces the ADC data.

(1) Shown for a serialization factor of 14.

All patterns listed in Table 9 (except the PRBS pattern) can also be forced on the frame clock output line by using PAT_MODES_FCLK[2:0]. To force a PRBS pattern on the frame clock, use the SEL_PRBS_PAT_FCLK, PRBS_EN, and PAT_MODES_FCLK register controls.

The ramp, toggle, and pseudo-random sequence (PRBS) test patterns can be reset or synchronized by providing a synchronization pulse on the TX_TRIG pin or by setting and resetting a specific register bit.

Figure 100 depicts a block diagram representation of this scheme.

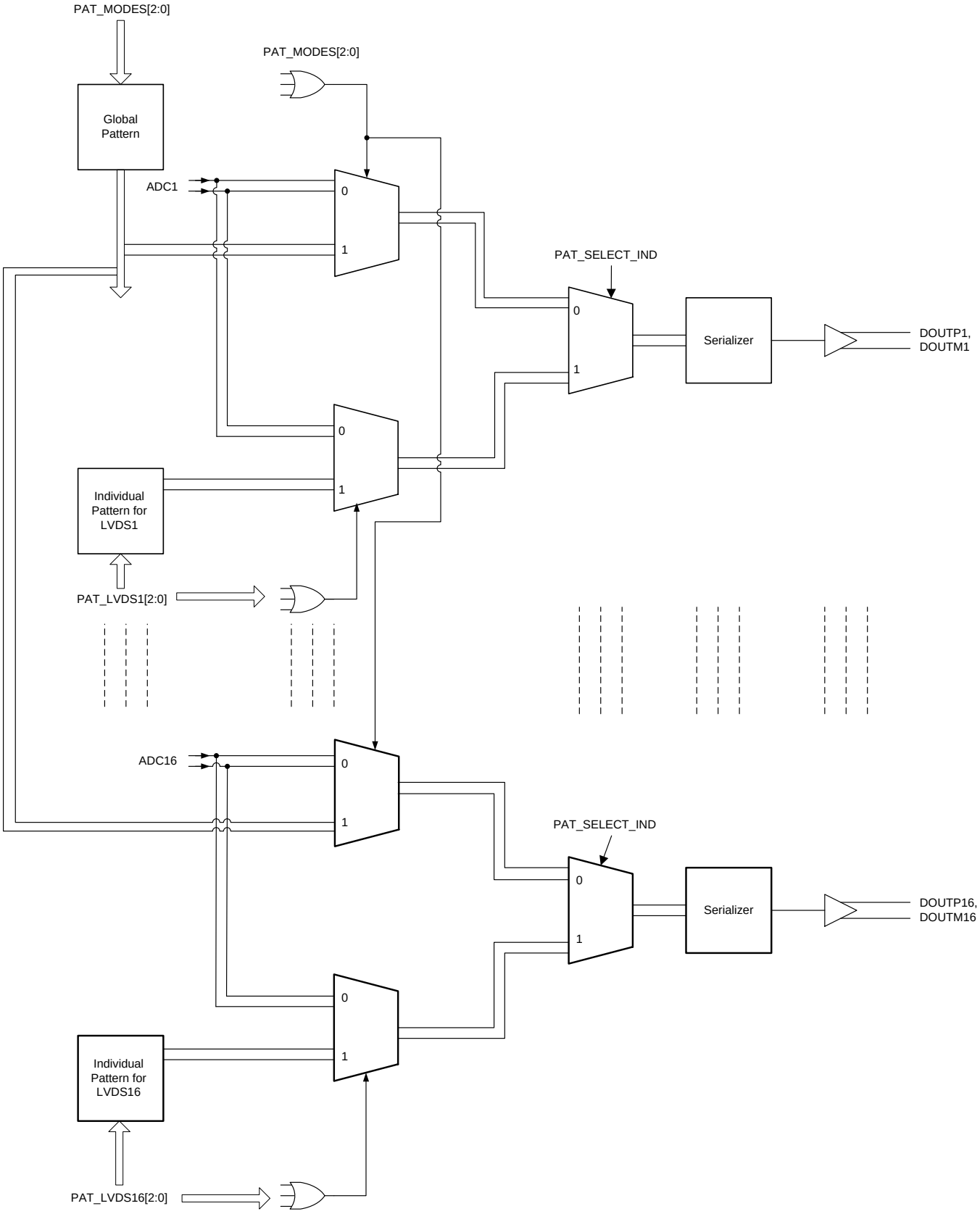


Figure 100. Test Pattern Block Diagram

9.4.2 Partial Power-Up and Power-Down Mode

The partial power-up and power-down mode is also called *fast power-up and power-down mode*. The VCA can be programmed in partial power-down mode either by setting the PDN_FAST pin high or setting the FAST_PDWN (register 197, bit 14) register bit to 1. Similarly, the ADC can be programmed in this mode by setting the PDN_FAST pin high. In this mode, most amplifiers in the signal path are powered down and the internal reference circuits remain active as well as all the data and frame and clock LVDS serializer and buffer. The partial power-down function allows the device to quickly wake-up from a low-power state. This configuration ensures that the external capacitors are discharged slowly; thus, a minimum wake-up time is required as long as the charges on these capacitors are restored. The VCA wake-up response is typically approximately 2 µs or 1% of the power-down duration, whichever is larger. The longest wake-up time depends on the capacitors connected at INP and INM, because the wake-up time is the time required to recharge the capacitors to the desired operating voltages. For instance, 0.1 µF at INP and 15 nF at INM provides a wake-up time of 2.5 ms. For larger capacitors, this time is longer. The ADC wake-up time is approximately 1 µs. Thus, the device wake-up time is more dependent on the VCA wake-up time with the assumption that the ADC clock is running for at least 50 µs before the normal operating mode resumes. The power-down time is instantaneous, less than 1 µs. This fast wake-up response is desired for portable ultrasound applications in which power savings is critical. The pulse repetition frequency of an ultrasound system can vary from 50 kHz to 500 Hz, and the imaging depth (that is, the active period for a receive path) varies from tens of µs to hundreds of µs. The power savings can be quite significant when a system PRF is low. In some cases, only the VCA is powered down when the ADC runs normally to ensure minimal interference to the FPGAs; see the *Electrical Characteristics* table to determine device power dissipation in partial power-down mode.

9.4.3 Global Power-Down Mode

To achieve the lowest power dissipation, the device can be placed into a complete power-down mode. This mode is controlled through the GBL_PDWN (for the VCA) or GLOBAL_PDN (for the ADC) registers or the PDN_GBL pin (for both the VCA and ADC). In complete power-down mode, all circuits (including reference circuits within the device) are powered down and the capacitors connected to the device are discharged. The wake-up time depends on the time that the device spends in shutdown mode. 0.1 µF at INP and 15 nF at INM provide a wake-up time of approximately 2.5 ms.

9.4.4 TGC Configuration

By default, after reset the VCA is configured in TGC mode. Depending upon the system requirements, the device can be programmed in a suitable power mode using the POW_MODES (register 197, bits 11-10) register bits.

9.4.5 CW Configuration

To configure the device in CW mode, set the CW_TGC_SEL (register 198, bit 9) register bit to 1. To save power, the voltage-controlled attenuator and programmable gain amplifier in the TGC path can be disabled by setting the PDWN_VCA_PGA bit (register 197, bit 12) to 1. Also, the ADC can be powered down completely using the GLOBAL_PDN bit (register 1, bit 0). Usually only half the number of channels in a system are active in the CW mode. Thus, the individual channel control can power-down unused channels and save power; see Table 7 and Table 8.

9.4.6 TGC + CW Mode

In systems that require fast switching between the TGC and CW modes, both TGC and CW mode can remain active simply by setting the CW_TGC_SEL (register 198, bit 9) register bit to 1.

9.5 Programming

9.5.1 Serial Peripheral Interface (SPI) Operation

Several different device modes can be programmed with the serial peripheral interface (SPI). This interface is formed by the SEN (serial interface enable), SCLK (serial interface clock), SDIN (serial interface data), and RESET pins. Inside the device, the SCLK and SDIN pins have a 16-kΩ, pulldown resistor to ground and the SEN pin has a 16-kΩ, pullup resistor to the DVDD_1P8 supply. Serially shifting bits into the device is enabled when SEN is low. SDIN serial data are latched at every SCLK rising edge when SEN is active (low). SDIN serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse (an internal counter counts the number of 24 clock groups after the SEN falling edge). The interface can function with SCLK frequencies from 20 MHz down to low speeds (of a few hertz) and also with a non-50% SCLK duty cycle. Data are divided into two main portions: the register address (8 bits) and data (16 bits). These portions are loaded on the addressed register. When writing to a register with unused bits, set these bits to 0. Figure 101 shows this process.

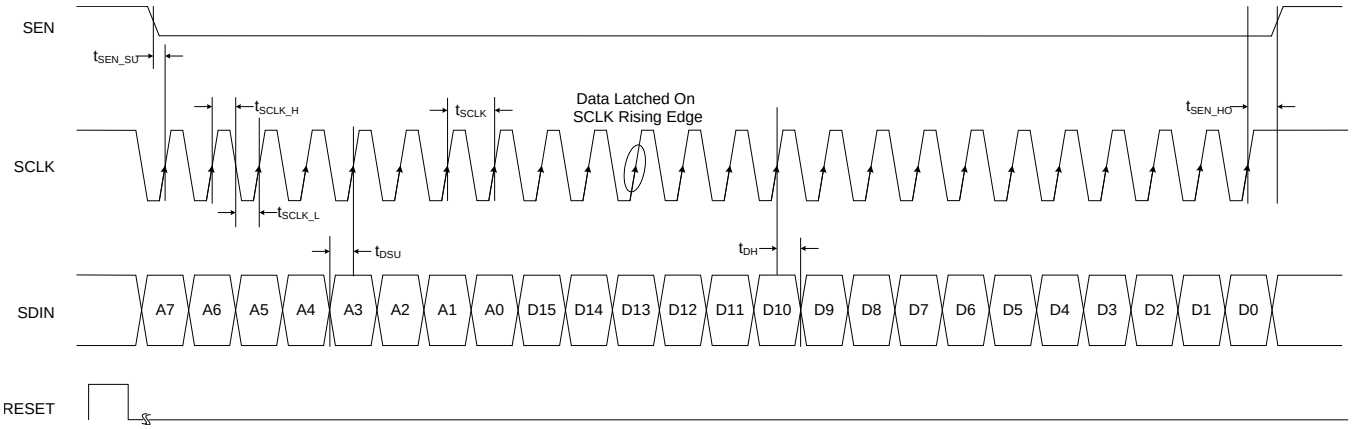


Figure 101. Serial Interface Timing Diagram

Programming (continued)

9.5.1.1 Register Readout

The device includes an option where the contents of the internal registers can be read back. This readback feature can be useful as a diagnostic test to verify the serial interface communication between the external controller and the AFE. First, the REG_READ_EN bit (register 0, bit 1) must be set to 1. Then, initiate a serial interface cycle specifying the address of the register (A[7:0]) whose content must be read. The data bits are *don't care*. The device outputs the contents (bits 15-0) of the selected register on the SDOUT pin. SDOUT has a typical 20-ns delay (t_{OUT_DV}) from the SCLK falling edge. For lower-speed SCLKs, SDOUT can be latched on the SCLK rising edge. For higher-speed SCLKs (for example, if the SCLK period is less than 60 ns), latching SDOUT at the next SCLK falling edge is preferable. The read operation timing diagram is shown in Figure 102 (see the *Serial Interface Timing Characteristics* table). In readout mode, the REG_READ_EN bit can be accessed with SDIN, SCLK, and SEN. To enable serial register writes, set the REG_READ_EN bit back to 0.

The device SDOUT buffer is 3-stated and is only enabled when the REG_READ_EN bit (register 0, bit 1) is enabled. SDOUT pins from multiple devices can be tied together without any pullup resistors. The SN74AUP1T04 level shifter can be used to convert 1.8-V logic to 2.5-V or 3.3-V logic, if necessary.

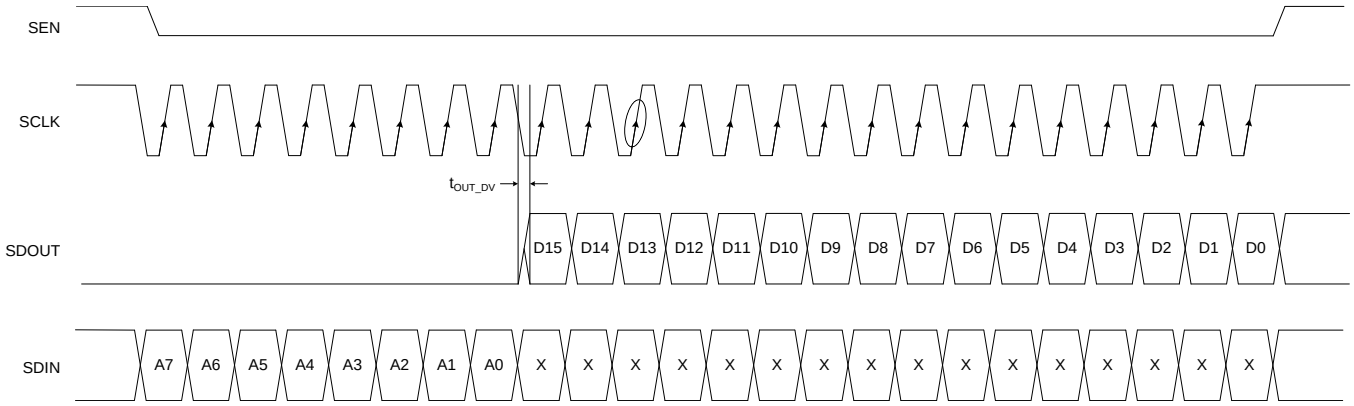


Figure 102. Serial Interface Register, Read Operation

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The device supports a wide-frequency bandwidth signal in the range of several kHz to several MHz. The device is a highly-integrated solution that includes a low-noise amplifier (LNA), a voltage-controlled attenuator (VCAT), a programmable gain amplifier (PGA), an antialiasing filter, an analog-to-digital converter (ADC), and a continuous wave (CW) mixer. As a result of the device functionality, the device can be used in various applications (such as in medical ultrasound imaging systems, sonar imaging equipment, radar, and other systems that require a very large dynamic range).

10.2 Typical Application

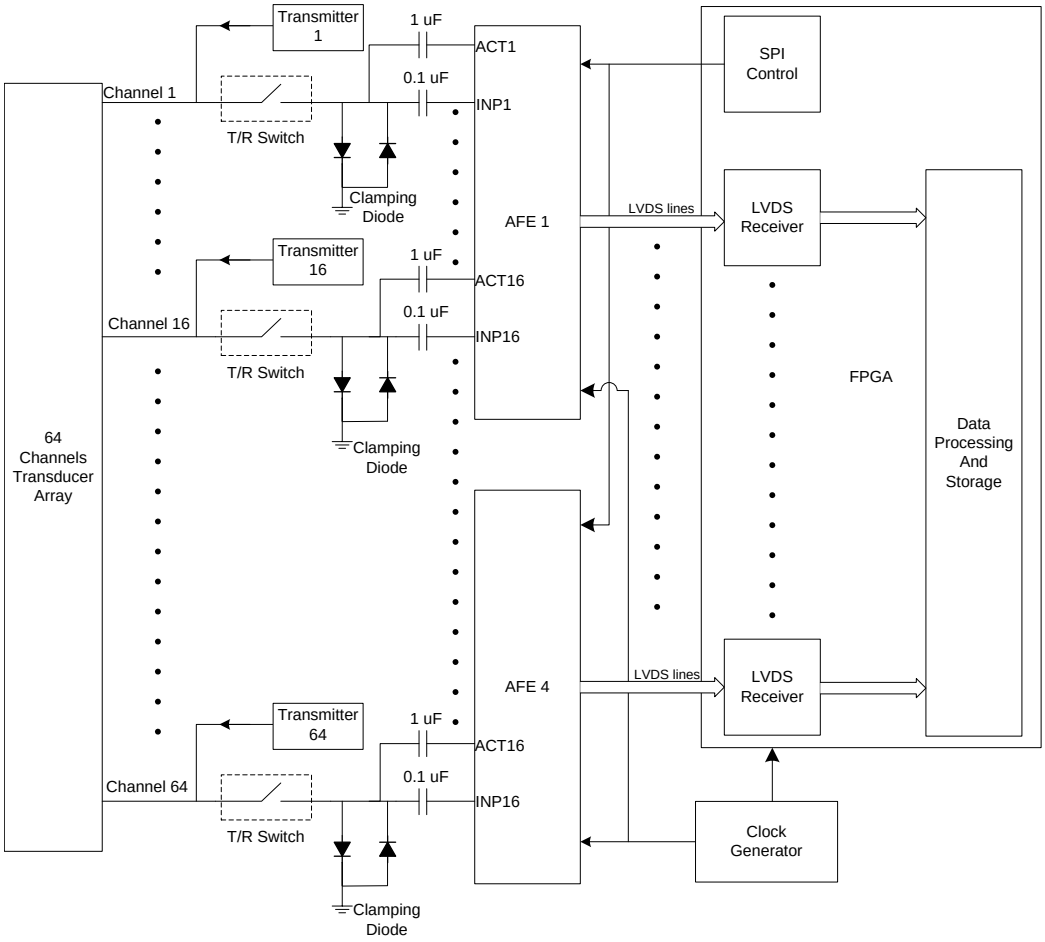
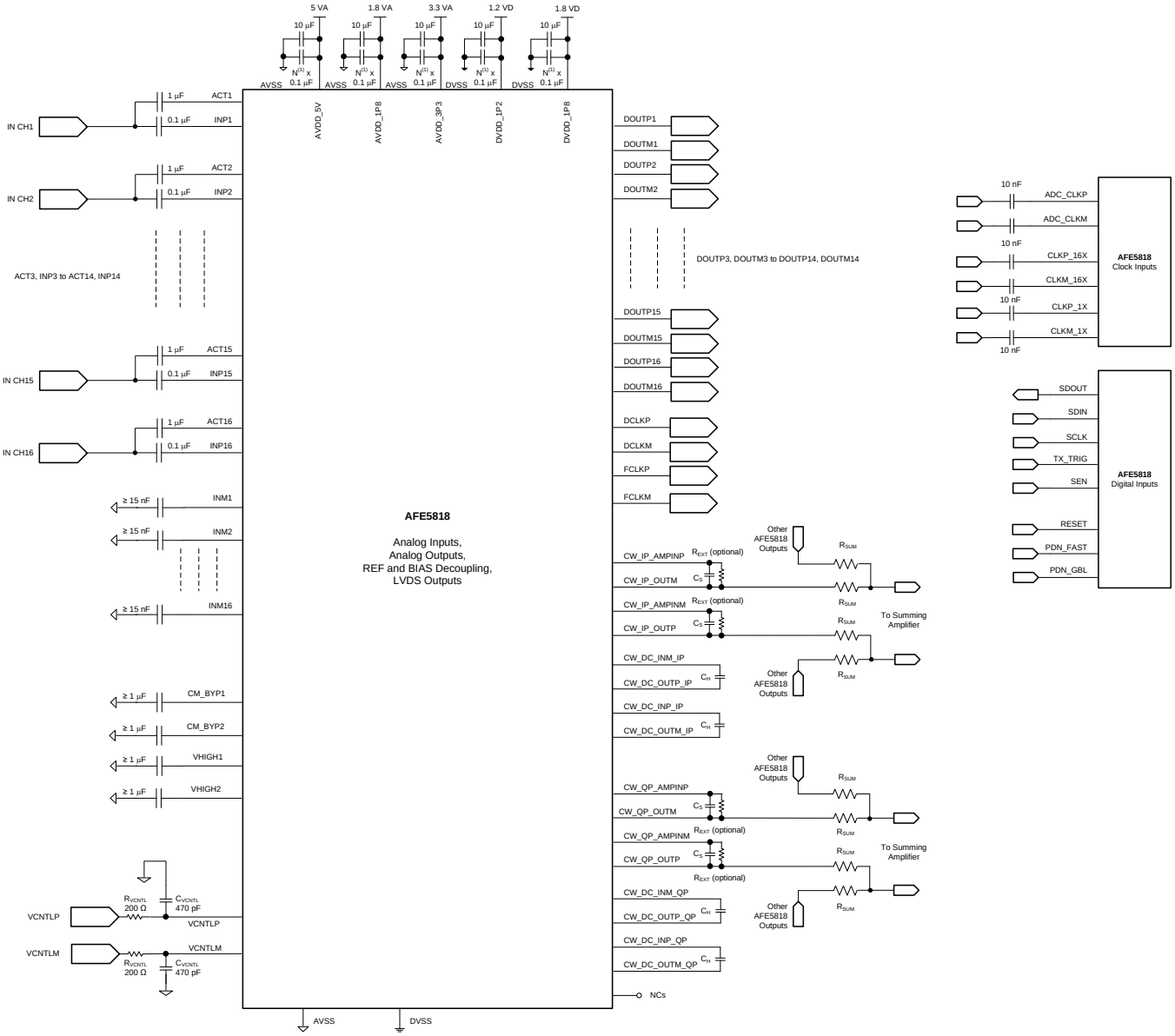


Figure 103. Simplified Schematic

Typical Application (continued)



(1) N represents the number of capacitors connected to the supply. Placing at least one capacitor for every three supply pins is recommended.

Figure 104. Application Circuit

Typical Application (continued)

10.2.0.2 Design Requirements

Typical requirements for a medical ultrasound imaging system are listed in Table 10.

Table 10. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Signal center frequency	5 MHz
Signal bandwidth	2 MHz
Maximum overloaded signal	1 V_{PP}
Maximum input signal amplitude	100 mV_{PP}
Transducer noise level	1 nV/$\sqrt{Hz}$
Dynamic range	151 dBc/Hz
Time gain compensation range	40 dB
Total harmonic distortion	40 dBc

10.2.0.3 Detailed Design Procedure

Medical ultrasound imaging is a widely-used diagnostic technique that enables visualization of internal organs, their size, structure, and blood flow estimation. An ultrasound system uses a focal imaging technique that involves time shifting, scaling, and intelligently summing the echo energy using an array of transducers to achieve high imaging performance. The concept of focal imaging provides the ability to focus on a single point in the scan region. By subsequently focusing at different points, an image is assembled.

See Figure 103 for a simplified schematic of a 64-channel ultrasound imaging system. When initiating an imaging, a pulse is generated and transmitted from each of the 64 transducer elements. The pulse, now in the form of mechanical energy, propagates through the body as sound waves, typically in the frequency range of 1 MHz to 15 MHz.

The sound waves weaken rapidly as they travel through the objects being imaged, falling off as the square of the distance traveled. As the signal travels, portions of the wave front energy are reflected. Signals that are reflected immediately after transmission are very strong because they are from reflections close to the surface; reflections that occur long after the transmit pulse are very weak because they are reflecting from deep in the body. As a result of the limitations on the amount of energy that can be put into the imaging object, the industry developed extremely sensitive receive electronics. Receive echoes from focal points close to the surface require little, if any, amplification. This region is referred to as the *near field*. However, receive echoes from focal points deep in the body are extremely weak and must be amplified by a factor of 100 or more. This region is referred to as the *far field*. In the high-gain (far field) mode, the limit of performance is the sum of all noise sources in the receive chain.

In high-gain (far field) mode, system performance is defined by its overall noise level, which is limited by the noise level of the transducer assembly and the receive low-noise amplifier (LNA). However in the low-gain (near field) mode, system performance is defined by the maximum amplitude of the input signal that the system can handle. The ratio between noise levels in high-gain mode and the signal amplitude level in low-gain mode is defined as the dynamic range of the system.

The high integration and high dynamic range of the device make it ideally suited for ultrasound imaging applications. The device includes an integrated LNA and VCAT (which use the gain that can be changed with enough time to handle both near- and far-field systems), a low-pass antialiasing filter to limit the noise bandwidth, an ADC with high SNR performance, and a CW mixer. Figure 104 illustrates an application circuit of the device.

Use the following steps to design medical ultrasound imaging systems:

1. Use the signal center frequency and signal bandwidth to select an appropriate ADC sampling frequency.
2. Use the time gain compensation range to select the range of the VCNTL signal.
3. Use the transducer noise level and maximum input signal amplitude to select the appropriate LNA gain. The device input-referred noise level reduces with higher LNA gain. However, higher LNA gain leads to lower input signal swing support.
4. See Figure 104 to select different passive components for different device pins.
5. See the *LNA Input Impedance* section to select the appropriate input termination configuration.
6. See the *CW Clock Selection* section to select the clock configuration for the ADC and CW clocks.

10.2.0.4 Application Curves

Figure 105 and Figure 106 show the FFT of a device output for VCNTL = 0 V and VCNTL = 0.9 V, respectively, with an input signal at 5 MHz captured at a sample rate of 50 MHz. Figure 105 shows the spectrum for a far field imaging scenario with the full Nyquist band, default device settings, and VCNTL = 0 V.Figure 106 shows the spectrum for a near field imaging scenario for the full Nyquist band with default device settings and VCNTL = 0.9 V.

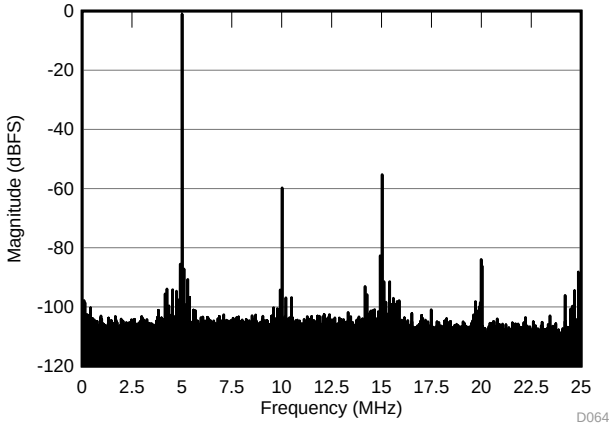


Figure 105. FFT for VCNTL = 0 V

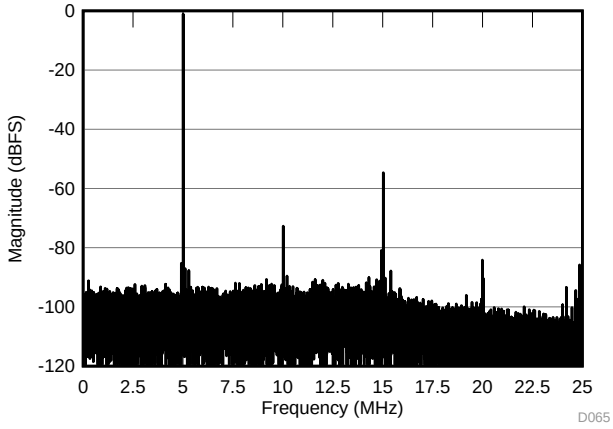


Figure 106. FFT for VCNTL = 0.9 V

10.3 Do's and Don'ts

Driving the inputs (analog or digital) beyond the power-supply rails. For device reliability, an input must not go more than 300 mV below the ground pins or 300 mV above the supply pins as suggested in the *Absolute Maximum Ratings* table. Exceeding these limits, even on a transient basis, can cause faulty or erratic operation and can impair device reliability.

Driving the device signal input with an excessively high level signal. The device offers consistent and fast overload recovery with a 6-dB overloaded signal. For very large overload signals (> 6 dB of the linear input signal range), TI recommends back-to-back Schottky clamping diodes at the input to limit the amplitude of the input signal; see the *LNA Overload Recovery* section for more details.

Driving the VCNTL signal with an excessive noise source. Noise on the VCNTL signal gets directly modulated with the input signal and causes higher output noise and reduction in SNR performance. Maintain a noise level for the VCNTL signal as discussed in the *Control Voltage Input* section.

Using a clock source with excessive jitter, an excessively long input clock signal trace, or having other signals coupled to the ADC or CW clock signal trace. These situations cause the sampling interval to vary, causing an excessive output noise and a reduction in SNR performance. For a system with multiple devices, the clock tree scheme must be used to apply an ADC or CW clock; see the *CW Clock Selection* section for clock mismatch between devices, which can lead to latency mismatch and reduction in SNR performance.

LVDS routing length mismatch. The routing length of all LVDS lines routing to the FPGA must be matched to avoid any timing related issue. For systems with multiple devices, the LVDS serialized data clock (DCLKP, DCLKM) and the frame clock (FCLKP, FCLKM) of each individual device must be used to deserialize the corresponding LDVS serialized data (DOUTP, DOUTM).

Failure to provide adequate heat removal. Use the appropriate thermal parameter listed in the *Thermal Information* table and an ambient, board, or case temperature in order to calculate device junction temperature. A suitable heat removal technique must be used to keep the device junction temperature below the maximum limit of 105°C.

Incorrect register programming. After resetting the device, write register 1, bit 2 = 1 and register 1, bit 4 = 1. If these bits are not set as specified, the device will not function properly. Furthermore, ADD_OFFSET (register 0, bit 2) must be used carefully; see the *VCA Register Map* section.

10.4 Initialization Set Up

After bringing up all the supplies, use the following steps to initialize the device:

1. Apply a hardware reset pulse on the RESET pin with a minimum pulse duration of 100 ns. Note that after powering up the device, a hardware reset is required.
2. After applying a hardware reset pulse, wait for a minimum time of 100 ns.
3. Set register 1, bits 2 and 4 to 1 using SPI signals.
4. Write any other register settings as required.

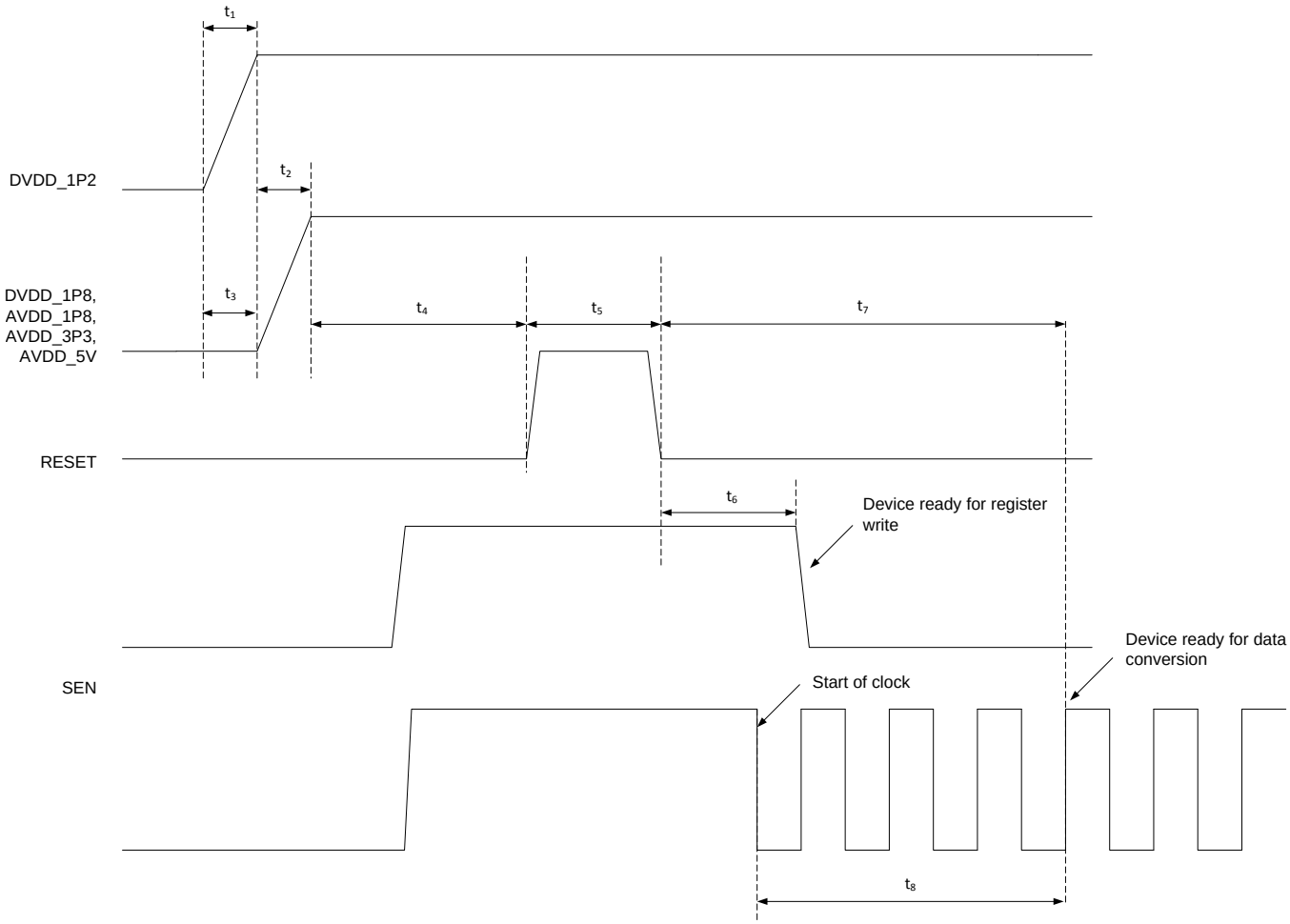
11 Power Supply Recommendations

The device requires a total of five supplies in order to operate properly. These supplies are: AVDD_5V, AVDD_3P3, AVDD_1P8, DVDD_1P8, and DVDD_1P2. For detailed information regarding the operating voltage minimum and maximum specifications of different supplies, see the *Recommended Operating Conditions* table.

11.1 Power Sequencing and Initialization

11.1.1 Power Sequencing

Figure 107 shows the suggested power-up sequencing and reset timing for the device. Note that the DVDD_1P2 supply must rise before the AVDD_1P8 supply. If the AVDD_1P8 supply rises before the DVDD_1P2 supply, the AVDD_1P8 supply current is eight to 12 times larger than the normal current until the DVDD_1P2 supply reaches a 1.2-V level.



NOTE: 10 µs < t_1 < 50 ms, 10 µs < t_2 < 50 ms, t_3 > t_1, t_4 > 10 ms, t_5 > 100 ns, t_6 > 100 ns, t_7 > 4 ADC clock cycles, and t_8 > 100 µs.

Figure 107. Recommended Power-Up Sequencing and Reset Timing Diagram

12 Layout

12.1 Layout Guidelines

12.1.1 Power Supply, Grounding, and Bypassing

In a mixed-signal system design, the power-supply and grounding design plays a significant role. The device distinguishes between two different grounds: AVSS (analog ground) and DVSS (digital ground). In most cases laying out the printed circuit board (PCB) to use a single ground plane is adequate, but in high-frequency or high-performance systems, care must be taken so that this ground plane is properly partitioned between various sections within the system to minimize interactions between analog and digital circuitry. Alternatively, the digital supply set consisting of the DVDD_1P8, DVDD_1P2, and DVSS pins can be placed on separate power and ground planes. For this configuration, tie the AVSS and DVSS grounds together at the power connector in a star layout. In addition, optical or digital isolators (such as the ISO7240) can completely separate the analog portion from the digital portion. Consequently, such isolators prevent digital noise from contaminating the analog portion. Table 11 lists the related circuit blocks for each power supply.

Table 11. Supply versus Circuit Blocks

POWER SUPPLY	GROUND	CIRCUIT BLOCKS(1)
AVDD_5V	AVSS	Reference voltage and current generator, LNA, VCNTRL block, CW mixer, CW clock buffer, 16x16 cross-point switch, 16-phase generator
AVDD_3P3	AVSS	Band-gap circuit, reference voltage and current generator, LNA, VCAT, PGA, LPF, CW summing amplifier, VCA SPI
AVDD_1P8	AVSS	ADC analog, reference voltage and current generator, band-gap circuit, ADC clock buffer
DVDD_1P8	DVSS	LVDS serializer and buffer, PLL
DVDD_1P2	DVSS	ADC digital, serial interface

(1) See Figure 98 and Figure 99 for further details.

Reference all bypassing and power supplies for the device to their corresponding ground planes. Bypass all supply pins with 0.1-µF ceramic chip capacitors (size 0603 or smaller). In order to minimize the lead and trace inductance, the capacitors must be located as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition, larger bipolar decoupling capacitors (2.2 µF to 10 µF, effective at lower frequencies) can also be used on the main supply pins. These components can be placed on the PCB in close proximity (< 0.5 inch or 12.7 mm) to the device itself.

The device has a number of reference supplies that must be bypassed, such as CM_BYP1, CM_BYP2 and VHIGH1, VHIGH2. Bypass these pins with at least a 1-µF capacitor; higher value capacitors can be used for better low-frequency noise suppression. For best results, choose low-inductance ceramic chip capacitors (size 0402, > 1 µF) and placed as close as possible to the device pins.

12.1.2 Board Layout

High-speed, mixed-signal devices are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffer and drivers. For the device, care must be taken to ensure that the interaction between the analog and digital supplies within the device is kept to a minimal amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each of the supply and ground connections. Smaller effective inductances of the supply and ground pins result in better noise suppression. For this reason, multiple pins are used to connect each supply and ground sets. Low inductance properties must be maintained throughout the design of the PCB layout by use of proper planes and layer thickness.

To avoid noise coupling through supply pins, TI recommends to keep sensitive input pins (such as INM, INP, and ACT pins) away from the AVDD_3P3 and AVDD_5V planes. For example, do not route the traces or vias connected to these pins across the AVDD_3P3 and AVDD_5V planes. That is, avoid the power planes under the INM, INP, and ACT pins.

In order to maintain proper LVDS timing, all LVDS traces must follow a controlled impedance design. In addition, all LVDS trace lengths must be equal and symmetrical; TI recommends keeping trace length variations less than 150 mil (0.150 inch or 3.81 mm).

In addition, appropriate delay matching must be considered for the CW clock path, especially in systems with a high channel count. For example, if the clock delay is half of the 16X clock period, a phase error of 22.5°C can exist. Thus, the timing delay difference among channels contributes to the beamformer accuracy.

Additional details on the NFBGA PCB layout techniques can be found in the Texas Instruments application report, *MicroStar BGA Packaging Reference Guide* (SSYZ015), which can be downloaded from www.ti.com.

12.2 Layout Example

Figure 108 and Figure 109 illustrate example layouts for the top and bottom layers, respectively.

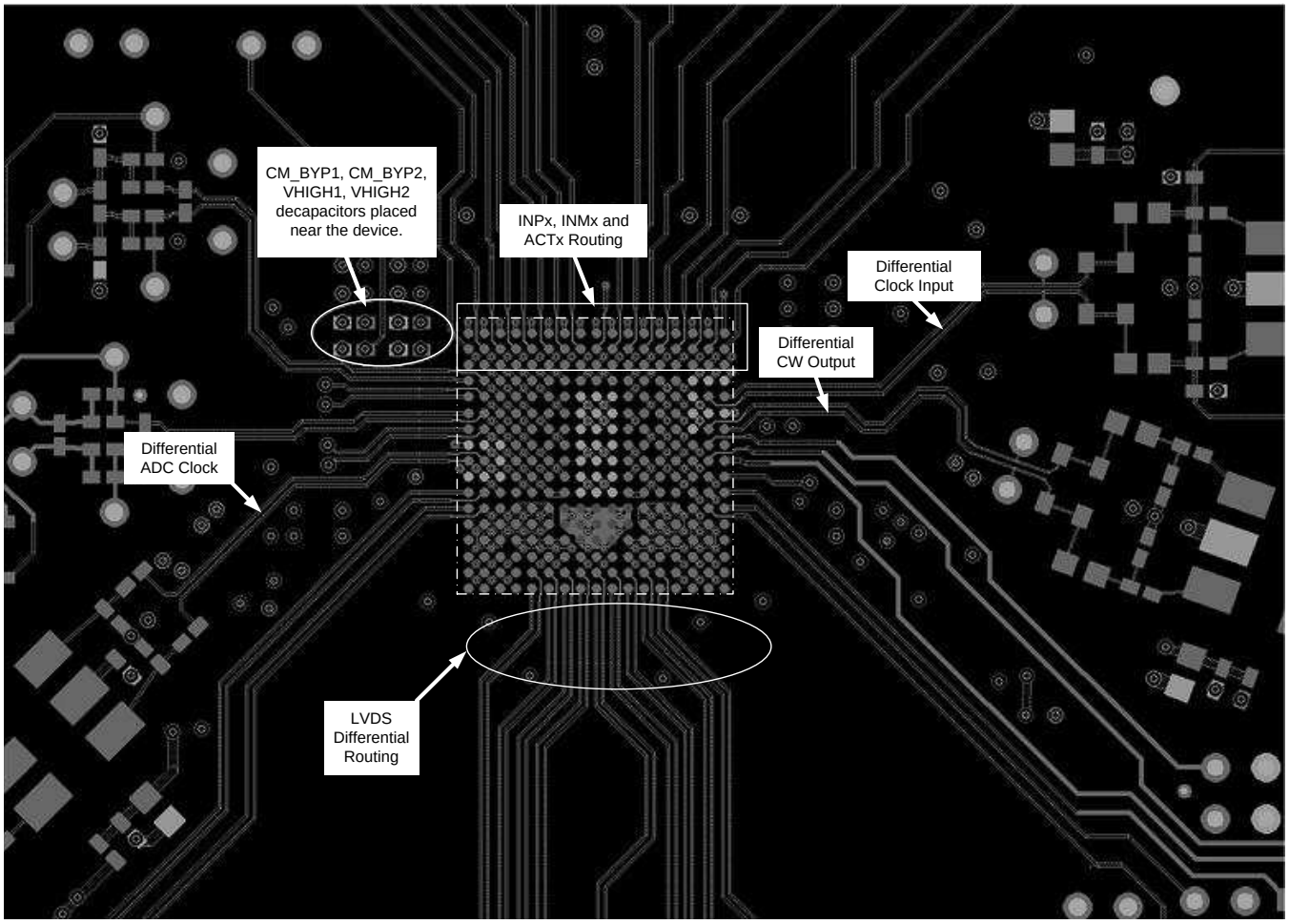


Figure 108. Top Layer

Layout Example (continued)

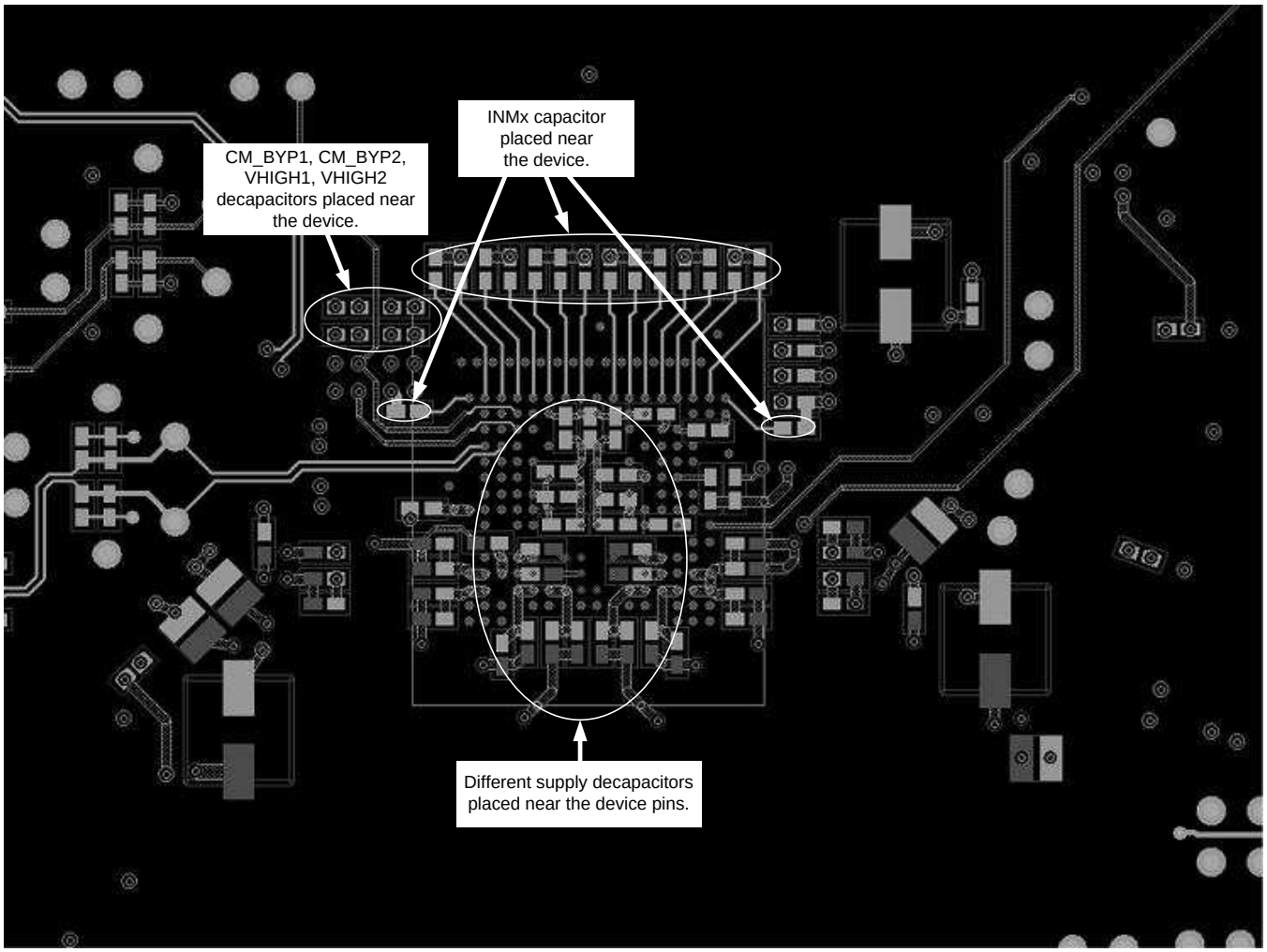


Figure 109. Bottom Layer

Layout Example (continued)

Figure 110 shows a routing example for the ground planes.

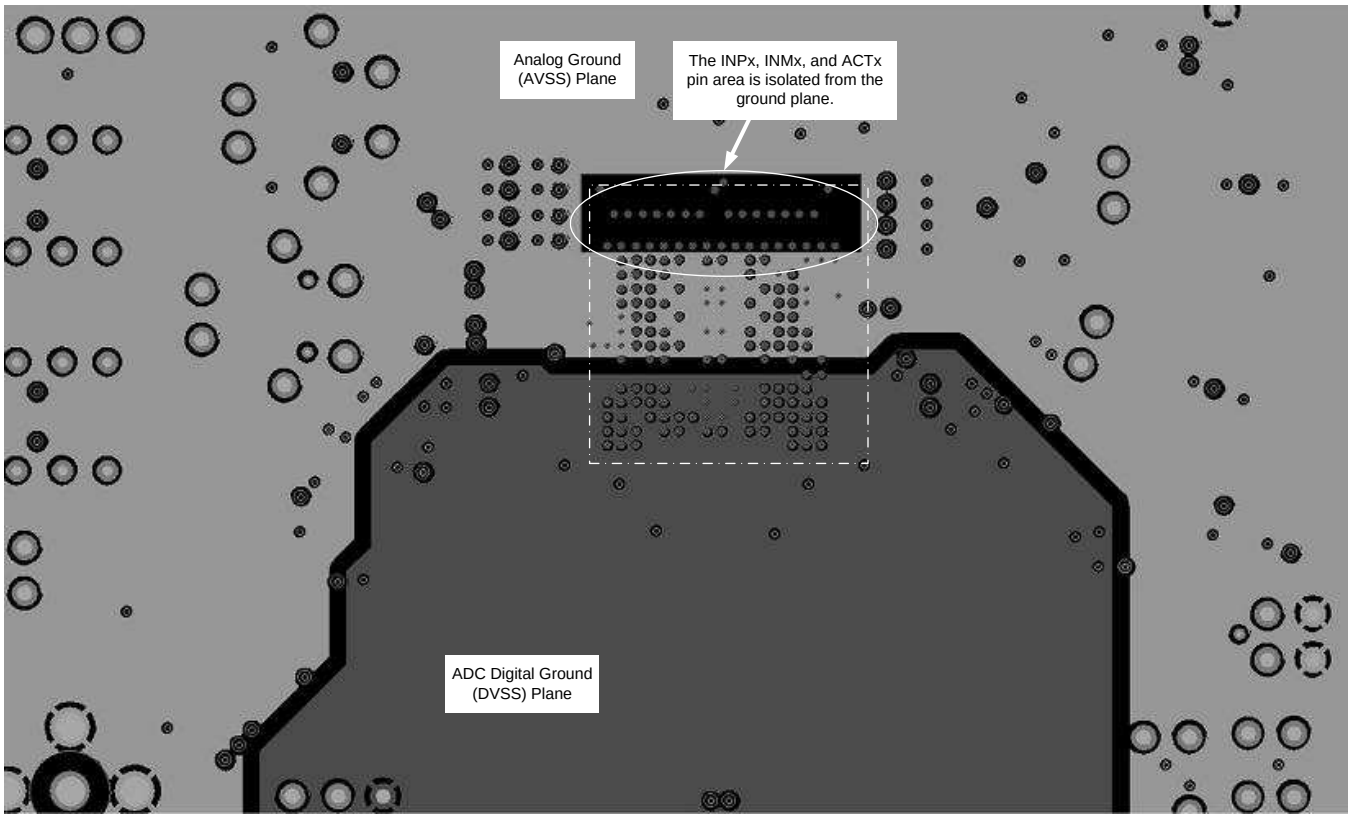


Figure 110. Ground Plane

Layout Example (continued)

Figure 111, Figure 112, and Figure 113 illustrate routing examples for different power planes.

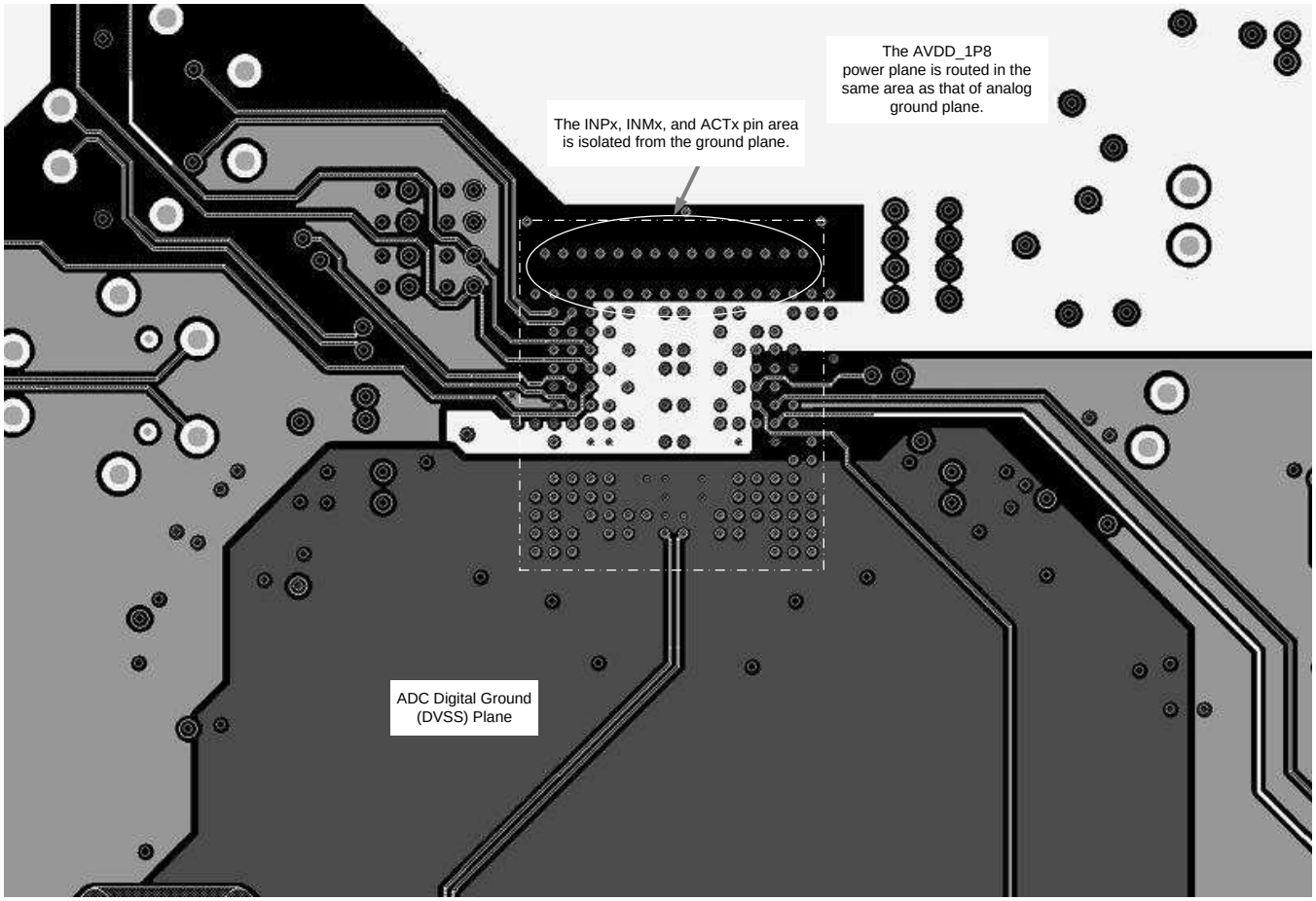


Figure 111. AVDD_1P8 Power Plane

Layout Example (continued)

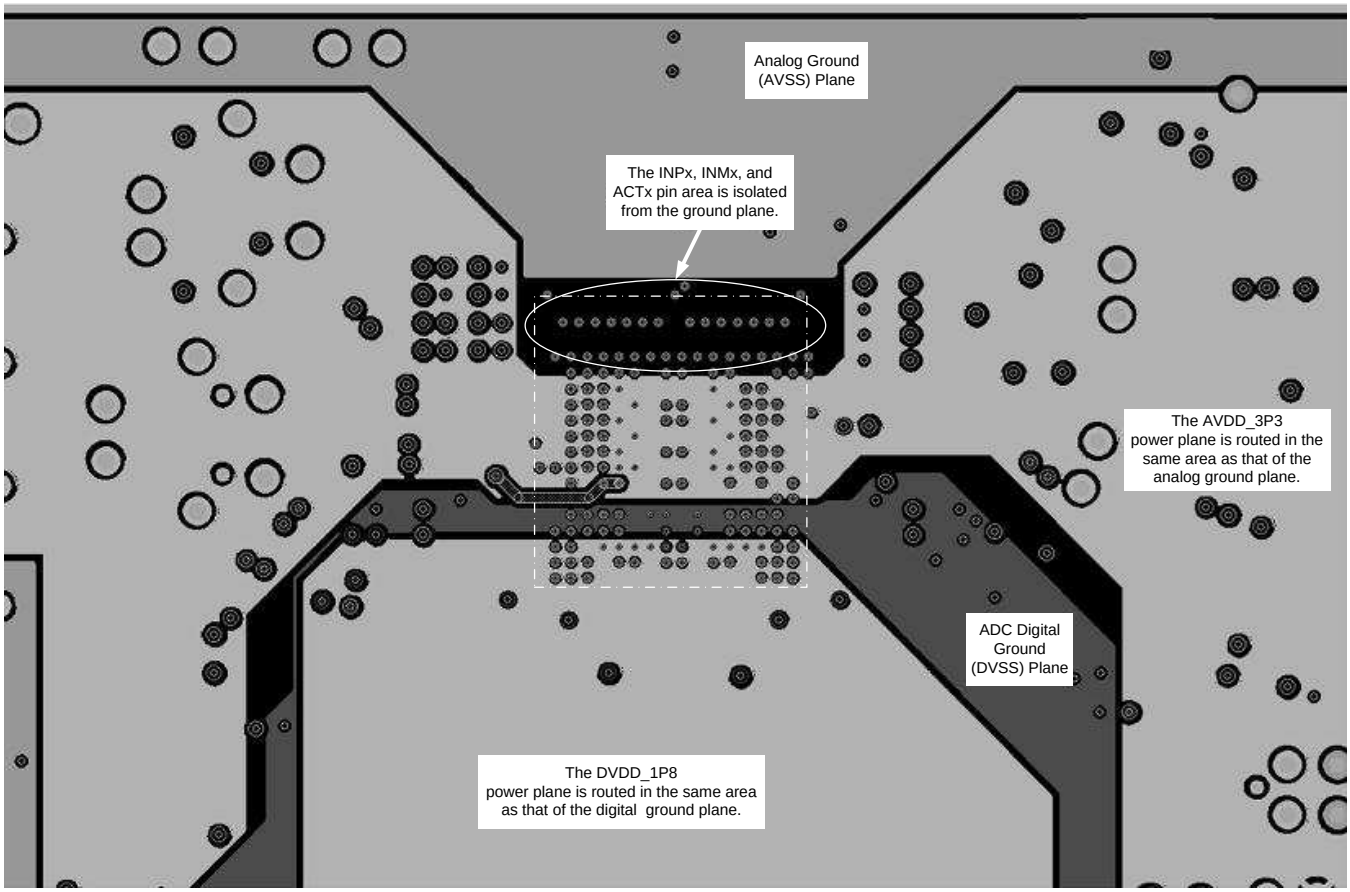


Figure 112. AVDD_3P3, DVDD_1P8 Power Planes

Layout Example (continued)

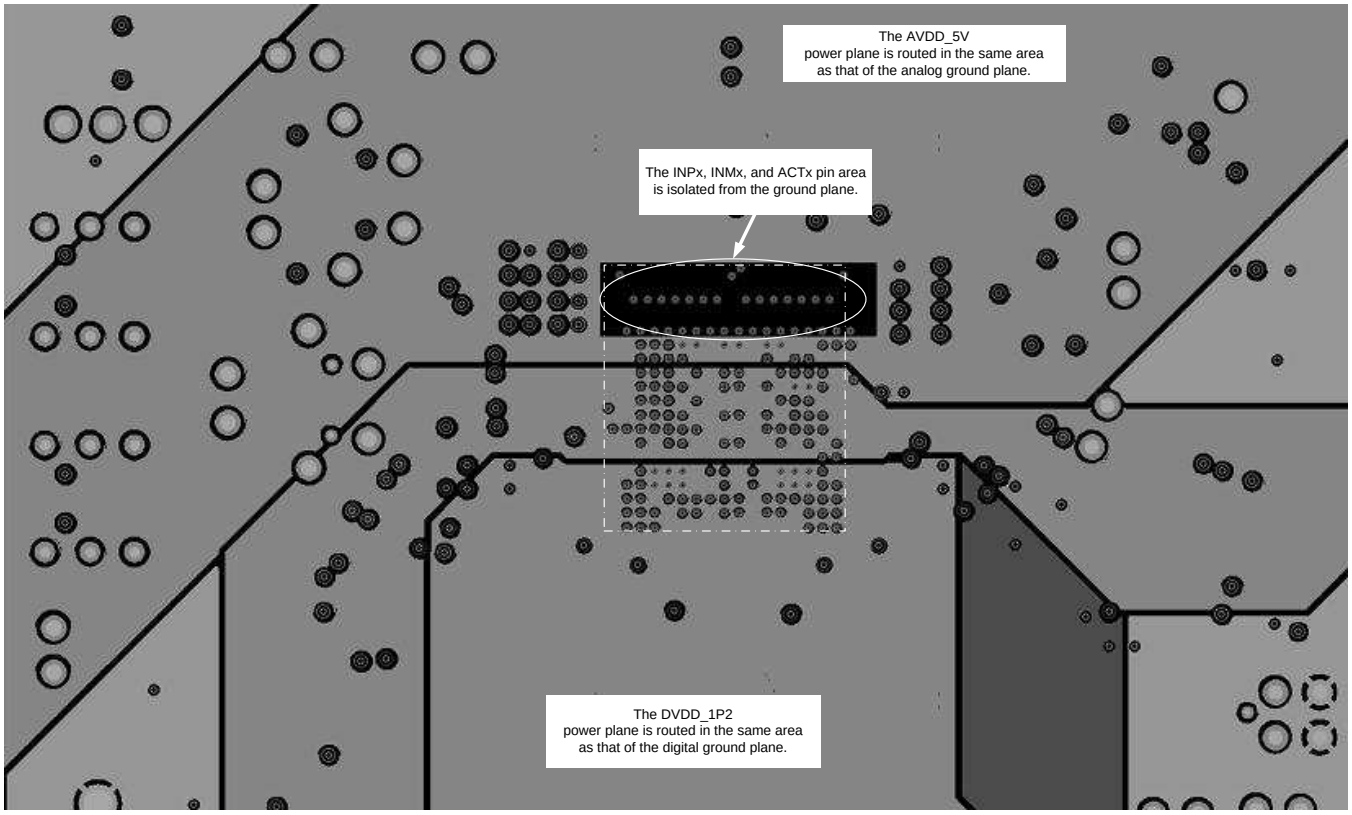


Figure 113. AVDD_5V, DVDD_1P2 Power Planes

13 Register Maps

13.1 Serial Register Map

The device has two voltage-controlled amplifier (VCA) dies and one analog-to-digital converter (ADC) die, as shown in Figure 114. Figure 114 also describes the channel mapping of VCA dies to the input pins. All dies share the same SPI control signals (SCLK, SDIN, and SEN). The address space of the programmable registers for the ADC die is from register 1 to register 60. By default, the address space of the programmable registers for the VCA dies are shared (that is, both VCA dies have an address space from register 192 to register 205). Therefore, the ADC and VCA dies can be programmed independently. Because the VCA dies share the same address space, these dies are programmed together. To program VCA die 1 and VCA die 2 independently, the address space for these dies must be separated by enabling the ADD_OFFSET bit (register 0, bit 2). All programmable bits and addresses are listed in this section.

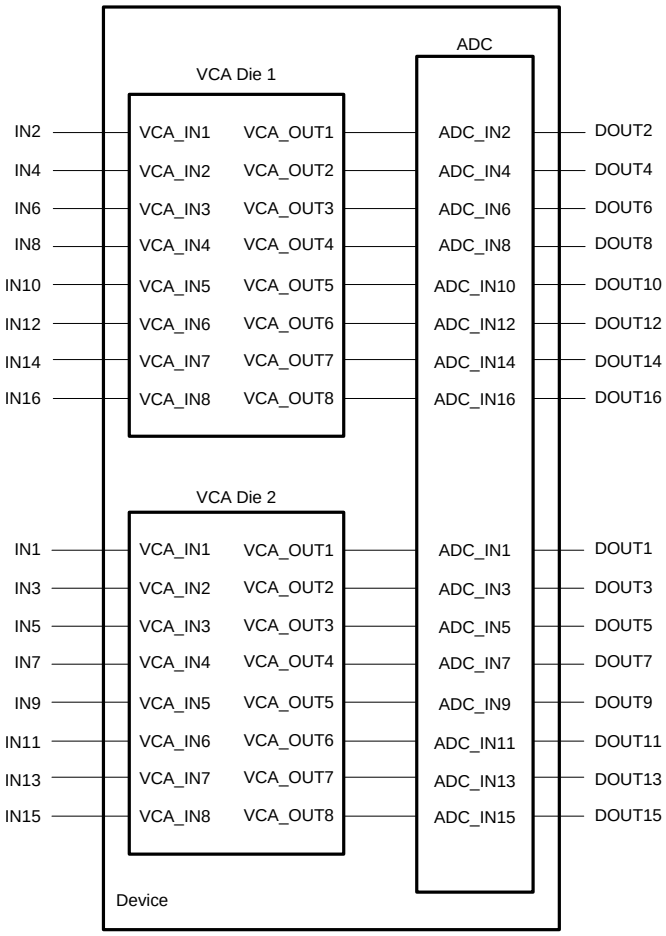


Figure 114. Channel Mapping: VCA Dies

A reset process is required at the device initialization stage.

NOTE

Initialization can be accomplished with a hardware reset by applying a positive pulse to the RESET pin. After reset, all ADC and VCA registers are set to 0 (default). Note that during register programming, all unlisted register bits must be set to 0.

The *Global Register* is comprised of register 0 and controls both the VCA and ADC die. The *ADC Registers* include registers that control the ADC die. The *VCA Registers* include registers that control the VCA dies (that is, VCA die 1 and VCA die 2).

Serial Register Map (continued)

13.1.1 Global Register Map

This section discusses the global register. A register map is available in Table 12.

Table 12. Global Register Map

REGISTER ADDRESS		REGISTER DATA(1)															
DECIMAL	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADD_ OFFSET	REG_READ_ EN	SOFTWARE_ RESET

(1) The default value of all registers is 0.

13.1.1.1 Description of Global Register

13.1.1.1.1 Register 0 (address = 0h)

Figure 115. Register 0

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	ADD_OFFSET	REG_READ_ EN	SOFTWARE_ RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value

Table 13. Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
15-3	0	W	0h	Must write 0
2	ADD_OFFSET	W	0h	0 = Normal operation 1 = Separates the SPI address space of the VCA die 1 and VCA die 2. Set this bit to 1 to write register addresses 213, 215, 216, and 217. Otherwise set this bit to 0.
1	REG_READ_EN	W	0h	0 = Register readout mode disabled 1 = Register readout mode enabled; see the *Register Readout* section for further details
0	SOFTWARE_RESET	W	0h	0 = Disabled 1 = Enabled (this setting returns the device to a reset state). This bit is a self-clearing register bit.

13.1.2 ADC Register Map

This section discusses the ADC and LVDS registers. A register map is available in Table 14.

Table 14. ADC Register Map

REGISTER ADDRESS		REGISTER DATA[1]															
DECIMAL	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	LVDS_RATE_2X	0	0	0	0	0	0	0	0	DIS_LVDS	1	0	1	0	GLOBAL_PDN
2	2	PAT_MODES_FCLK[2:0]			LOW_LATENCY_EN	AVG_EN	SEL_PRBS_PAT_FCLK	PAT_MODES[2:0]			SEL_PRBS_PAT_GBL	OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0]					
3	3	SER_DATA_RATE			DIG_GAIN_EN	0	OFFSET_CORR_DELAY_FROM_TX_TRIG[7:6]		DIG_OFFSET_EN	0	0	0	0	0	0	0	0
4	4	OFFSET_REMOVAL_SELF	OFFSET_REMOVAL_START_SEL	OFFEST_REMOVAL_START_MANUAL	AUTO_OFFSET_REMOVAL_ACC_CYCLES[3:0]				PAT_SELECT_IND	PRBS_SYNC	PRBS_MODE	PRBS_EN	MSB_FIRST	0	0	ADC_RES	
5	5	CUSTOM_PATTERN[15:0]															
7	7	AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL[4:0]					0	0	0	0	0	0	0	0	0	0	CHOPPER_EN
8	8	0	0	AUTO_OFFSET_REMOVAL_VAL_RD[13:0]													
11	B	0	0	0	0	EN_DITHER	0	0	0	0	0	0	0	0	0	0	0
13	D	GAIN_CH1					0	OFFSET_CH1									
14	E	0					0	OFFSET_CH1									
15	F	GAIN_CH2					0	OFFSET_CH2									
16	10	0					0	OFFSET_CH2									
17	11	GAIN_CH3					0	OFFSET_CH3									
18	12	0					0	OFFSET_CH3									
19	13	GAIN_CH4					0	OFFSET_CH4									
20	14	0					0	OFFSET_CH4									
21	15	PAT_PRBS_LVDS1	PAT_PRBS_LVDS2	PAT_PRBS_LVDS3	PAT_PRBS_LVDS4	PAT_LVDS1[2:0]			PAT_LVDS2[2:0]			HPF_ROUND_EN	HPF_CORNER_CH1-4[3:0]				DIG_HPF_EN_CH1-4
23	17	0	0	0	0	0	0	0	0	PAT_LVDS3[2:0]			PAT_LVDS4[2:0]			0	0
24	18	PDN_DIG_CH4	PDN_DIG_CH3	PDN_DIG_CH2	PDN_DIG_CH1	PDN_LVDS4	PDN_LVDS3	PDN_LVDS2	PDN_LVDS1	PDN_ANA_CH4	PDN_ANA_CH3	PDN_ANA_CH2	PDN_ANA_CH1	INVERT_LVDS4	INVERT_LVDS3	INVERT_LVDS2	INVERT_LVDS1
25	19	GAIN_CH5					0	OFFSET_CH5									
26	1A	0					0	OFFSET_CH5									
27	1B	GAIN_CH6					0	OFFSET_CH6									
28	1C	0					0	OFFSET_CH6									
29	1D	GAIN_CH7					0	OFFSET_CH7									
30	1E	0					0	OFFSET_CH7									
31	1F	GAIN_CH8					0	OFFSET_CH8									
32	20	0					0	OFFSET_CH8									

(1) Default value of all registers is 0.

Table 14. ADC Register Map (continued)

REGISTER ADDRESS		REGISTER DATA[1]															
DECIMAL	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
33	21	PAT_PRBS_LVDS5	PAT_PRBS_LVDS6	PAT_PRBS_LVDS7	PAT_PRBS_LVDS8	PAT_LVDS5[2:0]			PAT_LVDS6[2:0]			0	HPF_CORNER_CH5-8[3:0]				DIG_HPF_EN_CH5-8
35	23	0	0	0	0	0	0	0	0	PAT_LVDS7[2:0]			PAT_LVDS8[2:0]			0	0
36	24	PDN_DIG_CH8	PDN_DIG_CH7	PDN_DIG_CH6	PDN_DIG_CH5	PDN_LVDS8	PDN_LVDS7	PDN_LVDS6	PDN_LVDS5	PDN_ANA_CH8	PDN_ANA_CH7	PDN_ANA_CH6	PDN_ANA_CH5	INVERT_CH8	INVERT_CH7	INVERT_CH6	INVERT_CH5
37	25	GAIN_CH9					0	OFFSET_CH9									
38	26	0					0	OFFSET_CH9									
39	27	GAIN_CH10					0	OFFSET_CH10									
40	28	0					0	OFFSET_CH10									
41	29	GAIN_CH11					0	OFFSET_CH11									
42	2A	0					0	OFFSET_CH11									
43	2B	GAIN_CH12					0	OFFSET_CH12									
44	2C	0					0	OFFSET_CH12									
45	2D	PAT_PRBS_LVDS9	PAT_PRBS_LVDS10	PAT_PRBS_LVDS11	PAT_PRBS_LVDS12	PAT_LVDS9[2:0]			PAT_LVDS10[2:0]			0	HPF_CORNER_CH9-12[3:0]				DIG_HPF_EN_CH9-12
47	2F	0	0	0	0	0	0	0	0	PAT_LVDS11[2:0]			PAT_LVDS12[2:0]			0	0
48	30	PDN_DIG_CH12	PDN_DIG_CH11	PDN_DIG_CH10	PDN_DIG_CH9	PDN_LVDS12	PDN_LVDS11	PDN_LVDS10	PDN_LVDS9	PDN_ANA_CH12	PDN_ANA_CH11	PDN_ANA_CH10	PDN_ANA_CH9	INVERT_CH12	INVERT_CH11	INVERT_CH10	INVERT_CH9
49	31	GAIN_CH13					0	OFFSET_CH13									
50	32	0					0	OFFSET_CH13									
51	33	GAIN_CH14					0	OFFSET_CH14									
52	34	0					0	OFFSET_CH14									
53	35	GAIN_CH15					0	OFFSET_CH15									
54	36	0					0	OFFSET_CH15									
55	37	GAIN_CH16					0	OFFSET_CH16									
56	38	0					0	OFFSET_CH16									
57	39	PAT_PRBS_LVDS13	PAT_PRBS_LVDS14	PAT_PRBS_LVDS15	PAT_PRBS_LVDS16	PAT_LVDS13[2:0]			PAT_LVDS14[2:0]			0	HPF_CORNER_CH13-16[3:0]				DIG_HPF_EN_CH13-16
59	3B	0	0	0	0	0	0	0	0	PIN_PAT_LVDS15[2:0]			PAT_LVDS16[2:0]			0	0
60	3C	PDN_DIG_CH16	PDN_DIG_CH15	PDN_DIG_CH14	PDN_DIG_CH13	PDN_LVDS16	PDN_LVDS15	PDN_LVDS14	PDN_LVDS13	PDN_ANA_CH16	PDN_ANA_CH15	PDN_ANA_CH14	PDN_ANA_CH13	INVERT_CH16	INVERT_CH15	INVERT_CH14	INVERT_CH13
67	43	0	0	0	0	0	0	0	0	0	0	0	LVDS_DCLK_DELAY_PROG[3:0]				0

13.1.2.1 Description of ADC Registers

13.1.2.1.1 Register 1 (address = 1h)

Figure 116. Register 1

15	14	13	12	11	10	9	8
0	LVDS_RATE_2X	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	DIS_LVDS	1	0	1	0	GLOBAL_PDN
R/W-0h	R/W-0h	R/W-0h	W-1h	R/W-0h	W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 15. Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
15	0	R/W	0h	Must write 0
14	LVDS_RATE_2X	R/W	0h	0 = 1x rate; normal operation (default) 1 = 2x rate. This setting combines the data of two LVDS pairs into a single LVDS pair. This feature can be used when the ADC clock rate is low; see the *LVDS Interface* section for further details.
13-6	0	R/W	0h	Must write 0
5	DIS_LVDS	R/W	0h	0 = LVDS interface is enabled (default) 1 = LVDS interface is disabled
4	1	R/W	0h	Must write 1
3	0	R/W	0h	Must write 0
2	1	R/W	0h	Must write 1
1	0	R/W	0h	Must write 0
0	GLOBAL_PDN	R/W	0h	0 = Device operates in normal mode (default) 1 = ADC enters in complete power-down mode

13.1.2.1.2 Register 2 (address = 2h)

Figure 117. Register 2

15	14	13	12	11	10	9	8
PAT_MODES_FCLK[2:0]			LOW_ LATENCY_EN	AVG_EN	SEL_PRBS_ PAT_FCLK	PAT_MODES[2:0]	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
PAT_ MODES[2:0]	SEL_PRBS_ PAT_GBL	OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0]					
R/W-0h	R/W-0h	R/W-0h					

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 16. Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	PAT_MODES_FCLK[2:0]	R/W	0h	These bits enable different test patterns on the frame clock line; see Table 17 for bit descriptions and to the *Test Patterns* section for further details.
12	LOW_LATENCY_EN	R/W	0h	0 = Default latency with digital features supported 1 = Low-latency with digital features bypassed
11	AVG_EN	R/W	0h	0 = No averaging 1 = Enables averaging of two channels to improve signal-to-noise ratio (SNR); see the *LVDS Interface* section for further details.
10	SEL_PRBS_PAT_FCLK	R/W	0h	0 = Normal operation 1 = Enables the PRBS pattern to be generated on f_{CLK}; see the *Test Patterns* section for further details.
9-7	PAT_MODES[2:0]	R/W	0h	These bits enable different test patterns on the LVDS data lines; see Table 17 for bit descriptions and to the *Test Patterns* section for further details.
6	SEL_PRBS_PAT_GBL	R/W	0h	0 = Normal operation 1 = Enables the PRBS pattern to be generated; see the *Test Patterns* section for further details.
5-0	OFFSET_CORR_DELAY_FROM_ TX_TRIG[5:0]	R/W	0h	8-bit register to initiate offset correction after the TX_TRIG input pulse (each step is equivalent to one sample delay); the remaining two MSB bits are the OFFSET_CORR_DELAY_FROM_TX_TRIG[7:6] bits (bits 10-9) in register 3.

Table 17. Pattern Mode Bit Description

PAT_MODES[2:0]	DESCRIPTION
000	Normal operation
001	Sync (half frame 0, half frame 1)
010	Alternate 0s and 1s
011	Custom pattern
100	All 1s
101	Toggle mode
110	All 0s
111	Ramp pattern

13.1.2.1.3 Register 3 (address = 3h)

Figure 118. Register 3

15	14	13	12	11	10	9	8
SER_DATA_RATE			DIG_GAIN_EN	0	OFFSET_CORR_DELAY_FROM _TX_TRIG[7:6]		DIG_ OFFSET_EN
R/W-0h			R/W-0h	R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 18. Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
15-13	SER_DATA_RATE	R/W	0h	These bits control the LVDS serialization rate. 000 = 12x 001 = 14x 100 = 16x 101, 110, 111, 010, 011 = Unused
12	DIG_GAIN_EN	R/W	0h	0 = Digital gain disabled 1 = Digital gain enabled
11	0	R/W	0h	Must write 0
10-9	OFFSET_CORR_DELAY_FROM_ TX_TRIG[7:6]	R/W	0h	8-bit register to initiate offset correction after the TX_TRIG input pulse (each step is equivalent to one sample delay); the remaining six LSB bits are the OFFSET_CORR_DELAY_FROM_TX_TRIG[5:0] bits (bits 5-0) in register 2.
8	DIG_OFFSET_EN	R/W	0h	0 = Digital offset subtraction disabled 1 = Digital offset subtraction enabled
7-0	0	R/W	0h	Must write 0

13.1.2.1.4 Register 4 (address = 4h)

Figure 119. Register 4

15	14	13	12	11	10	9	8
OFFSET_ REMOVAL_ SELF	0	0	0	0	0	0	PAT_ SELECT_IND
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PRBS_ SYNC	PRBS_ MODE	PRBS_EN	MSB_FIRST	0	0	ADC_RES	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 19. Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
15	OFFSET_REMOVAL_SELF	R/W	0h	Auto offset removal mode is enabled when this bit is set to 1
14	OFFSET_REMOVAL_START_SEL	R/W	0h	Enable this bit to initiate offset correction with a pulse at the TX_TRIG pin, otherwise offset correction is initiated when the OFFSET_REMOVAL_START_MANUAL bit (bit 13) in register 4 is enabled.
13	OFFSET_REMOVAL_START_ MANUAL	R/W	0h	This bit initiates offset correction manually instead of with a TX_TRIG pulse
12-9	AUTO_OFFSET_REMOVAL_ACC_ CYCLES	R/W	0h	These bits define the number of samples required to generate an offset in auto offset correction mode
8	PAT_SELECT_IND	R/W	0h	0 = All LVDS output lines have the same pattern, as determined by the PAT_MODES[2:0] bits (register 2, bits 9-7) 1 = Different test patterns can be sent on different LVDS lines, depending upon the channel and register; see the *Test Patterns* section for further details.
7	PRBS_SYNC	R/W	0h	0 = Normal operation 1 = PRBS generator is in a reset state
6	PRBS_MODE	R/W	0h	0 = 23-bit PRBS generator 1 = 9-bit PRBS generator
5	PRBS_EN	R/W	0h	0 = PRBS sequence generation block disabled 1 = PRBS sequence generation block enabled; see the *Test Patterns* section for further details.
4	MSB_FIRST	R/W	0h	0 = The LSB is transmitted first on serialized output data 1 = The MSB is transmitted first on serialized output data
3	0	R/W	0h	Must write 0
2	0	R/W	0h	Must write 0
1-0	ADC_RES	R/W	0h	These bits control the ADC resolution. 00 = 12-bit resolution 01 = 14-bit resolution 10, 11 = Unused

13.1.2.1.5 Register 5 (address = 5h)

Figure 120. Register 5

15	14	13	12	11	10	9	8
CUSTOM_PATTERN[15:0]							
R/W-0h							
7	6	5	4	3	2	1	0
CUSTOM_PATTERN[15:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 20. Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CUSTOM_PATTERN[15:0]	R/W	0h	If the pattern mode is programmed to a custom pattern mode, then the custom pattern value can be provided by programming these bits; see the *Test Patterns* section for further details.

13.1.2.1.6 Register 7 (address = 7h)

Figure 121. Register 7

15	14	13	12	11	10	9	8
AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL					0	0	0
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	CHOPPER_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 21. Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	AUTO_OFFSET_REMOVAL_VAL_RD_CH_SEL	R/W	0h	Write the channel number to read the offset value in auto offset correction mode for a corresponding channel number (read the offset value in register 8, bits 13-0)
10-1	0	R/W	0h	Must write 0
0	CHOPPER_EN	R/W	0h	The chopper can be used to move low-frequency, 1 / f noise to an f_S / 2 frequency. 0 = Chopper disabled 1 = Chopper enabled

13.1.2.1.7 Register 8 (address = 8h)

Figure 122. Register 8

15	14	13	12	11	10	9	8
0	0	AUTO_OFFSET_REMOVAL_VAL_RD[13:0]					
R/W-0h	R/W-0h	R/W-0h					
7	6	5	4	3	2	1	0
AUTO_OFFSET_REMOVAL_VAL_RD[13:0]							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 22. Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
15-14	0	R/W	0h	Must write 0
13-0	AUTO_OFFSET_REMOVAL_VAL_RD	R/W	0h	Read the offset value applied in auto offset correction mode for a specific channel number as defined in register 7, bits 15-11

13.1.2.1.8 Register 11 (address = Bh)

Figure 123. Register 11

15	14	13	12	11	10	9	8
0	0	0	0	EN_DITHER	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 23. Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	0	R/W	0h	Must write 0
11	EN_DITHER	R/W	0h	Dither can be used to remove higher-order harmonics. 0 = Dither disabled 1 = Dither enable Note: Enabling the dither converts higher-order harmonics power in noise. Thus, enabling this mode removes harmonics but degrades SNR.
10-0	0	R/W	0h	Must write 0

13.1.2.1.9 Register 13 (address = Dh)

Figure 124. Register 13

15	14	13	12	11	10	9	8
GAIN_CH1					0	OFFSET_CH1	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH1							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 24. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH1	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 1 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH1	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 1 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 14, bits 9-0.

13.1.2.1.10 Register 14 (address = Eh)

Figure 125. Register 14

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH1	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH1							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 25. Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH1	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 1 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 13, bits 9-0.

13.1.2.1.11 Register 15 (address = Fh)

Figure 126. Register 15

15	14	13	12	11	10	9	8
GAIN_CH2					0	OFFSET_CH2	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 26. Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH2	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 2 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH2	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 2 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 16, bits 9-0.

13.1.2.1.12 Register 16 (address = 10h)

Figure 127. Register 16

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH2	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 27. Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH2	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 2 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 15, bits 9-0.

13.1.2.1.13 Register 17 (address = 11h)

Figure 128. Register 17

15	14	13	12	11	10	9	8
GAIN_CH3					0	OFFSET_CH3	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH3							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 28. Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH3	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 3 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH3	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 3 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 18, bits 9-0.

13.1.2.1.14 Register 18 (address = 12h)

Figure 129. Register 18

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH3	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH3							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 29. Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH3	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 3 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 19, bits 9-0.

13.1.2.1.15 Register 19 (address = 13h)

Figure 130. Register 19

15	14	13	12	11	10	9	8
GAIN_CH4					0	OFFSET_CH4	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH4							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 30. Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH4	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 4 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH4	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 4 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 20, bits 9-0.

13.1.2.1.16 Register 20 (address = 14h)

Figure 131. Register 20

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH4	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH4							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 31. Register 20 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH4	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 4 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 19, bits 9-0.

13.1.2.1.17 Register 21 (address = 15h)

Figure 132. Register 21

15	14	13	12	11	10	9	8
PAT_PRBS_LVDS1	PAT_PRBS_LVDS2	PAT_PRBS_LVDS3	PAT_PRBS_LVDS4	PAT_LVDS1[2:0]			PAT_LVDS2[2:0]
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS2[2:0]		HPF_ROUND_EN	HPF_CORNER_CH1-4[3:0]				DIG_HPF_EN_CH1-4
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 32. Register 21 Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS1	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 1 can be enabled with this bit; see the *Test Patterns* section for further details.
14	PAT_PRBS_LVDS2	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 2 can be enabled with this bit; see the *Test Patterns* section for further details.
13	PAT_PRBS_LVDS3	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 3 can be enabled with this bit; see the *Test Patterns* section for further details.
12	PAT_PRBS_LVDS4	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 4 can be enabled with this bit; see the *Test Patterns* section for further details.
11-9	PAT_LVDS1[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 1 can be programmed with these bits; see Table 33 for bit descriptions.
8-6	PAT_LVDS2[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 2 can be programmed with these bits; see Table 33 for bit descriptions.
5	HPF_ROUND_EN	R/W	0h	0 = Rounding in the ADC HPF is disabled. HPF output is truncated to be mapped to the ADC resolution bits. 1 = HPF output is mapped to the ADC resolution bits by the round-off operation.
4-1	HPF_CORNER_CH1-4[3:0]	R/W	0h	When the DIG_HPF_EN_CH1-4 bit is set to 1, then the digital HPF characteristic for the corresponding channels can be programmed by setting the value of k with these bits. Characteristics of a digital high-pass transfer function applied to the output data for a given value of k is defined by: $Y(n) = \frac{2^k}{2^k + 1} [x(n) - x(n-1) + y(n-1)]$ Note that the value of k can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_CH1-4	R/W	0h	0 = Digital HPF disabled for channels 1 to 4 (default) 1 = Enables digital HPF for channels 1 to 4

Table 33. Pattern Mode Bit Description

PAT_MODES[2:0]	DESCRIPTION
000	Normal operation
001	Sync (half frame 0, half frame 1)
010	Alternate 0s and 1s
011	Custom pattern
100	All 1s
101	Toggle mode
110	All 0s
111	Ramp pattern

13.1.2.1.18 Register 23 (address = 17h)

Figure 133. Register 23

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS3[2:0]			PAT_LVDS4[2:0]			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 34. Register 23 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	0	R/W	0h	Must write 0
7-5	PAT_LVDS3[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 3 can be programmed with these bits; see Table 33 for bit descriptions.
4-2	PAT_LVDS4[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 4 can be programmed with these bits; see Table 33 for bit descriptions.
1-0	0	R/W	0h	Must write 0

13.1.2.1.19 Register 24 (address = 18h)

Figure 134. Register 24

15	14	13	12	11	10	9	8
PDN_DIG_CH4	PDN_DIG_CH3	PDN_DIG_CH2	PDN_DIG_CH1	PDN_LVDS4	PDN_LVDS3	PDN_LVDS2	PDN_LVDS1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_ANA_CH4	PDN_ANA_CH3	PDN_ANA_CH2	PDN_ANA_CH1	INVERT_LVDS4	INVERT_LVDS3	INVERT_LVDS2	INVERT_LVDS1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 35. Register 24 Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_CH4	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 4
14	PDN_DIG_CH3	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 3
13	PDN_DIG_CH2	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel2
12	PDN_DIG_CH1	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 1
11	PDN_LVDS4	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 4
10	PDN_LVDS3	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 3
9	PDN_LVDS2	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 2
8	PDN_LVDS1	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 1
7	PDN_ANA_CH4	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 4
6	PDN_ANA_CH3	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 3
5	PDN_ANA_CH2	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 2
4	PDN_ANA_CH1	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 1
3	INVERT_LVDS4	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 4
2	INVERT_LVDS3	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 3
1	INVERT_LVDS2	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 2
0	INVERT_LVDS1	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 1

13.1.2.1.20 Register 25 (address = 19h)

Figure 135. Register 25

15	14	13	12	11	10	9	8
GAIN_CH5					0	OFFSET_CH5	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH5							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 36. Register 25 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH5	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 5 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH5	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 5 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 26, bits 9-0.

13.1.2.1.21 Register 26 (address = 1Ah)

Figure 136. Register 26

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH5	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH5							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 37. Register 26 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH5	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 5 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 25, bits 9-0.

13.1.2.1.22 Register 27 (address = 1Bh)

Figure 137. Register 27

15	14	13	12	11	10	9	8
GAIN_CH6					0	OFFSET_CH6	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH6							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 38. Register 27 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH6	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 6 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH6	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 6 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 28, bits 9-0.

13.1.2.1.23 Register 28 (address = 1Ch)

Figure 138. Register 28

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH6	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH6							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 39. Register 28 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH6	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 6 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 27, bits 9-0.

13.1.2.1.24 Register 29 (address = 1Dh)

Figure 139. Register 29

15	14	13	12	11	10	9	8
GAIN_CH7					0	OFFSET_CH7	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH7							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 40. Register 29 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH7	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 7 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH7	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 7 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 30, bits 9-0.

13.1.2.1.25 Register 30 (address = 1Eh)

Figure 140. Register 30

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH7	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH7							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 41. Register 30 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH7	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 7 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 29, bits 9-0.

13.1.2.1.26 Register 31 (address = 1Fh)

Figure 141. Register 31

15	14	13	12	11	10	9	8
GAIN_CH8					0	OFFSET_CH8	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH8							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 42. Register 31 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH8	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 8 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH8	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 8 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 32, bits 9-0.

13.1.2.1.27 Register 32 (address = 20h)

Figure 142. Register 32

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH8	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH8							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 43. Register 32 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH8	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 16 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 31, bits 9-0.

13.1.2.1.28 Register 33 (address = 21h)

Figure 143. Register 33

15	14	13	12	11	10	9	8
PAT_PRBS_LVDS5	PAT_PRBS_LVDS6	PAT_PRBS_LVDS7	PAT_PRBS_LVDS8	PAT_LVDS5[2:0]			PAT_LVDS6[2:0]
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS6[2:0]		0	HPF_CORNER_CH5-8[3:0]				DIG_HPF_EN_CH5-8
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 44. Register 33 Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS5	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 5 can be enabled with this bit; see the *Test Patterns* section for further details.
14	PAT_PRBS_LVDS6	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 6 can be enabled with this bit; see the *Test Patterns* section for further details.
13	PAT_PRBS_LVDS7	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 7 can be enabled with this bit; see the *Test Patterns* section for further details.
12	PAT_PRBS_LVDS8	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 8 can be enabled with this bit; see the *Test Patterns* section for further details.
11-9	PAT_LVDS5[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 5 can be programmed with these bits; see Table 33 for bit descriptions.
8-6	PAT_LVDS6[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 6 can be programmed with these bits; see Table 33 for bit descriptions.
5	0	R/W	0h	Must write 0
4-1	HPF_CORNER_CH5-8[3:0]	R/W	0h	When the DIG_HPF_EN_CH5-8 bit is set to 1, then the digital HPF characteristic for the corresponding channels can be programmed by setting the value of k with these bits. Characteristics of a digital high-pass transfer function applied to the output data for a given value of k is defined by: $Y(n) = \frac{2^k}{2^k + 1} [x(n) - x(n-1) + y(n-1)]$ Note that the value of k can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_CH5-8	R/W	0h	0 = Digital HPF disabled for channels 5 to 8 (default) 1 = Enables digital HPF for channels 5 to 8

13.1.2.1.29 Register 35 (address = 23h)

Figure 144. Register 35

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS7[2:0]			PAT_LVDS8[2:0]			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 45. Register 35 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	0	R/W	0h	Must write 0
7-5	PAT_LVDS7[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 7 can be programmed with these bits; see Table 33 for bit descriptions.
4-2	PAT_LVDS8[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 8 can be programmed with these bits; see Table 33 for bit descriptions.
1-0	0	R/W	0h	Must write 0

13.1.2.1.30 Register 36 (address = 24h)

Figure 145. Register 36

15	14	13	12	11	10	9	8
PDN_DIG_CH8	PDN_DIG_CH7	PDN_DIG_CH6	PDN_DIG_CH5	PDN_LVDS8	PDN_LVDS7	PDN_LVDS6	PDN_LVDS5
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_ANA_CH8	PDN_ANA_CH7	PDN_ANA_CH6	PDN_ANA_CH5	INVERT_CH8	INVERT_CH7	INVERT_CH6	INVERT_CH5
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 46. Register 36 Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_CH8	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 8
14	PDN_DIG_CH7	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 7
13	PDN_DIG_CH6	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 6
12	PDN_DIG_CH5	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 5
11	PDN_LVDS8	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 8
10	PDN_LVDS7	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 7
9	PDN_LVDS6	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 6
8	PDN_LVDS5	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 5
7	PDN_ANA_CH8	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 8
6	PDN_ANA_CH7	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 7
5	PDN_ANA_CH6	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 6
4	PDN_ANA_CH5	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 5
3	INVERT_CH8	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 8
2	INVERT_CH7	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 7
1	INVERT_CH6	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 6
0	INVERT_CH5	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 5

13.1.2.1.31 Register 37 (address = 25h)

Figure 146. Register 37

15	14	13	12	11	10	9	8
GAIN_CH9					0	OFFSET_CH9	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH9							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 47. Register 37 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH9	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 9 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH9	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 9 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 38, bits 9-0.

13.1.2.1.32 Register 38 (address = 26h)

Figure 147. Register 38

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH9	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH9							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 48. Register 38 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH9	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 9 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 37, bits 9-0.

13.1.2.1.33 Register 39 (address = 27h)

Figure 148. Register 39

15	14	13	12	11	10	9	8
GAIN_CH10					0	OFFSET_CH10	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH10							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 49. Register 39 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH10	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 10 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH10	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 10 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 40, bits 9-0.

13.1.2.1.34 Register 40 (address = 28h)

Figure 149. Register 40

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH10	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH10							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 50. Register 40 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH10	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 10 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 39, bits 9-0.

13.1.2.1.35 Register 41 (address = 29h)

Figure 150. Register 41

15	14	13	12	11	10	9	8
GAIN_CH11					0	OFFSET_CH11	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH11							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 51. Register 41 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH11	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 11 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH11	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 11 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 42, bits 9-0.

13.1.2.1.36 Register 42 (address = 2Ah)

Figure 151. Register 42

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH11	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH11							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 52. Register 42 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH11	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 11 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 41, bits 9-0.

13.1.2.1.37 Register 43 (address = 2Bh)

Figure 152. Register 43

15	14	13	12	11	10	9	8
GAIN_CH12					0	OFFSET_CH12	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH12							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 53. Register 43 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH12	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 12 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH12	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 12 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 44, bits 9-0.

13.1.2.1.38 Register 44 (address = 2Ch)

Figure 153. Register 44

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH12	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH12							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 54. Register 44 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH12	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 12 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 43, bits 9-0.

13.1.2.1.39 Register 45 (address = 2Dh)

Figure 154. Register 45

15	14	13	12	11	10	9	8
PAT_PRBS_LVDS9	PAT_PRBS_LVDS10	PAT_PRBS_LVDS11	PAT_PRBS_LVDS12	PAT_LVDS9[2:0]			PAT_LVDS10[2:0]
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS10[2:0]		0	HPF_CORNER_CH9-12[3:0]				DIG_HPF_EN_CH9-12
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 55. Register 45 Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS9	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 9 can be enabled with this bit; see the *Test Patterns* section for further details.
14	PAT_PRBS_LVDS10	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 10 can be enabled with this bit; see the *Test Patterns* section for further details.
13	PAT_PRBS_LVDS11	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 11 can be enabled with this bit; see the *Test Patterns* section for further details.
12	PAT_PRBS_LVDS12	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 12 can be enabled with this bit; see the *Test Patterns* section for further details.
11-9	PAT_LVDS9[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 9 can be programmed with these bits; see Table 33 for bit descriptions.
8-6	PAT_LVDS10[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 10 can be programmed with these bits; see Table 33 for bit descriptions.
5	0	R/W	0h	Must write 0
4-1	HPF_CORNER_CH9-12[3:0]	R/W	0h	When the DIG_HPF_EN_CH9-12 bit is set to 1, then the digital HPF characteristic for the corresponding channels can be programmed by setting the value of k with these bits. Characteristics of a digital high-pass transfer function applied to the output data for a given value of k is defined by: $Y(n) = \frac{2^k}{2^k + 1} [x(n) - x(n-1) + y(n-1)]$ Note that the value of k can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_CH9-12	R/W	0h	0 = Digital HPF disabled for channels 9 to 12 (default) 1 = Enables digital HPF for channels 9 to 12

13.1.2.1.40 Register 47 (address = 2Fh)

Figure 155. Register 47

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS11[2:0]			PAT_LVDS12[2:0]			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 56. Register 47 Field Descriptions

Bit	Field	Type	Reset	Description
15-18	0	R/W	0h	Must write 0
7-5	PAT_LVDS11[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 11 can be programmed with these bits; see Table 33 for bit descriptions.
4-2	PAT_LVDS12[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 12 can be programmed with these bits; see Table 33 for bit descriptions.
1-0	0	R/W	0h	Must write 0

13.1.2.1.41 Register 48 (address = 30h)

Figure 156. Register 48

15	14	13	12	11	10	9	8
PDN_DIG_CH12	PDN_DIG_CH11	PDN_DIG_CH10	PDN_DIG_CH9	PDN_LVDS12	PDN_LVDS11	PDN_LVDS10	PDN_LVDS9
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_ANA_CH12	PDN_ANA_CH11	PDN_ANA_CH10	PDN_ANA_CH9	INVERT_CH12	INVERT_CH11	INVERT_CH10	INVERT_CH9
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 57. Register 48 Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_CH12	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 12
14	PDN_DIG_CH11	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 11
13	PDN_DIG_CH10	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 10
12	PDN_DIG_CH9	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 9
11	PDN_LVDS12	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 12
10	PDN_LVDS11	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 11
9	PDN_LVDS10	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 10
8	PDN_LVDS9	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 9
7	PDN_ANA_CH12	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 12
6	PDN_ANA_CH11	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 11
5	PDN_ANA_CH10	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 10
4	PDN_ANA_CH9	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 9
3	INVERT_CH12	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 12
2	INVERT_CH11	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 11
1	INVERT_CH10	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 10
0	INVERT_CH9	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 9

13.1.2.1.42 Register 49 (address = 31h)

Figure 157. Register 49

15	14	13	12	11	10	9	8
GAIN_CH13					0	OFFSET_CH13	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH13							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 58. Register 49 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH13	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 13 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH13	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 13 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 50, bits 9-0.

13.1.2.1.43 Register 50 (address = 32h)

Figure 158. Register 50

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH13	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH13							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 59. Register 50 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH13	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 13 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 49, bits 9-0.

13.1.2.1.44 Register 51 (address = 33h)

Figure 159. Register 51

15	14	13	12	11	10	9	8
GAIN_CH14					0	OFFSET_CH14	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH14							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 60. Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH14	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 14 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH14	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 14 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 52, bits 9-0.

13.1.2.1.45 Register 52 (address = 34h)

Figure 160. Register 52

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH14	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH14							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 61. Register 52 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH14	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 14 can be obtained with this 10-bit register. The offset value is in twos complement format. Write the same offset value in register 51, bits 9-0.

13.1.2.1.46 Register 53 (address = 35h)

Figure 161. Register 53

15	14	13	12	11	10	9	8
GAIN_CH15					0	OFFSET_CH15	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH15							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 62. Register 53 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH15	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 15 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH15	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 15 can be obtained with this 10-bit register. the offset value is in twos complement format. Write the same offset value in register 54, bits 9-0.

13.1.2.1.47 Register 54 (address = 36h)

Figure 162. Register 54

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH15	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH15							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 63. Register 54 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH15	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 15 can be obtained with this 10-bit register. the offset value is in twos complement format. Write the same offset value in register 53, bits 9-0.

13.1.2.1.48 Register 55 (address = 37h)

Figure 163. Register 55

15	14	13	12	11	10	9	8
GAIN_CH16					0	OFFSET_CH16	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH16							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 64. Register 55 Field Descriptions

Bit	Field	Type	Reset	Description
15-11	GAIN_CH16	R/W	0h	When the DIG_GAIN_EN bit (register 3, bit 12) is set to 1, then the digital gain value for channel 16 can be obtained with this register. For an *N* value (decimal equivalent of binary) written to these bits, set the digital gain to N × 0.2 dB.
10	0	R/W	0h	Must write 0
9-0	OFFSET_CH16	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 16 can be obtained with this 10-bit register. the offset value is in twos complement format. Write the same offset value in register 56, bits 9-0.

13.1.2.1.49 Register 56 (address = 38h)

Figure 164. Register 56

15	14	13	12	11	10	9	8
0	0	0	0	0	0	OFFSET_CH16	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
OFFSET_CH16							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 65. Register 56 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	0	R/W	0h	Must write 0
9-0	OFFSET_CH16	R/W	0h	When the DIG_OFFSET_EN bit (register 3, bit 8) is set to 1, then the offset value for channel 16 can be obtained with this 10-bit register. the offset value is in twos complement format. Write the same offset value in register 55, bits 9-0.

13.1.2.1.50 Register 57 (address = 39h)

Figure 165. Register 57

15	14	13	12	11	10	9	8
PAT_PRBS_LVDS13	PAT_PRBS_LVDS14	PAT_PRBS_LVDS15	PAT_PRBS_LVDS16	PAT_LVDS13[2:0]			PAT_LVDS14[2:0]
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
PAT_LVDS14[2:0]		0	HPF_CORNER_CH25-32[3:0]				DIG_HPF_EN_CH25-32
R/W-0h		R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 66. Register 57 Field Descriptions

Bit	Field	Type	Reset	Description
15	PAT_PRBS_LVDS13	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 13 can be enabled with this bit; see the *Test Patterns* section for further details.
14	PAT_PRBS_LVDS14	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 14 can be enabled with this bit; see the *Test Patterns* section for further details.
13	PAT_PRBS_LVDS15	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 15 can be enabled with this bit; see the *Test Patterns* section for further details.
12	PAT_PRBS_LVDS16	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the PRBS pattern on LVDS output 16 can be enabled with this bit; see the *Test Patterns* section for further details.
11-9	PAT_LVDS13[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 13 can be programmed with these bits; see Table 33 for bit descriptions.
8-6	PAT_LVDS14[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 14 can be programmed with these bits; see Table 33 for bit descriptions.
5	0	R/W	0h	Must write 0
4-1	HPF_CORNER_CH13-16[3:0]	R/W	0h	When the DIG_HPF_EN_CH13-16 bit is set to 1, then the digital HPF characteristic for the corresponding channels can be programmed by setting the value of k with these bits. Characteristics of a digital high-pass transfer function applied to the output data for a given value of k is defined by: $Y(n) = \frac{2^k}{2^k + 1} [x(n) - x(n-1) + y(n-1)]$ Note that the value of k can be from 2 to 10 (0010b to 1010b); see the *Digital HPF* section for further details.
0	DIG_HPF_EN_CH13-16	R/W	0h	0 = Digital HPF disabled for channels 13 to 16 (default) 1 = Enables digital HPF for channels 13 to 16

13.1.2.1.51 Register 59 (address = 3Bh)

Figure 166. Register 59

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PIN_PAT_LVDS15[2:0]			PAT_LVDS16[2:0]			0	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 67. Register 59 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	0	R/W	0h	Must write 0
7-5	PAT_LVDS15[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the differentpattern on LVDS output 15 can be programmed with these bits; see Table 33 for bit descriptions.
4-2	PAT_LVDS16[2:0]	R/W	0h	When the PAT_SELECT_IND bit (register 4, bit 8) is set to 1, then the different pattern on LVDS output 16 can be programmed with these bits; see Table 33 for bit descriptions.
1-0	0	R/W	0h	Must write 0

13.1.2.1.52 Register 60 (address = 3Ch)

Figure 167. Register 60

15	14	13	12	11	10	9	8
PDN_DIG_CH16	PDN_DIG_CH15	PDN_DIG_CH14	PDN_DIG_CH13	PDN_LVDS16	PDN_LVDS15	PDN_LVDS14	PDN_LVDS13
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDN_ANA_CH16	PDN_ANA_CH15	PDN_ANA_CH14	PDN_ANA_CH13	INVERT_CH16	INVERT_CH15	INVERT_CH14	INVERT_CH13
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 68. Register 60 Field Descriptions

Bit	Field	Type	Reset	Description
15	PDN_DIG_CH16	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 16
14	PDN_DIG_CH15	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 15
13	PDN_DIG_CH14	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 14
12	PDN_DIG_CH13	R/W	0h	0 = Normal operation (default) 1 = Powers down the digital block for channel 13
11	PDN_LVDS16	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 16
10	PDN_LVDS15	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 15
9	PDN_LVDS14	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 14
8	PDN_LVDS13	R/W	0h	0 = Normal operation (default) 1 = Powers down LVDS output line 13
7	PDN_ANA_CH16	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 16
6	PDN_ANA_CH15	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 15
5	PDN_ANA_CH14	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 14
4	PDN_ANA_CH13	R/W	0h	0 = Normal operation (default) 1 = Powers down the analog block for channel 13
3	INVERT_CH15	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 16
2	INVERT_CH16	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 15
1	INVERT_CH14	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 14
0	INVERT_CH13	R/W	0h	0 = Normal operation (default) 1 = Inverts digital output data sent on LVDS output line 13

13.1.2.1.53 Register 67 (address = 43h)

Figure 168. Register 67

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	LVDS_DCLK_DELAY_PROG[3:0]				0
R/W-0h	R/W-0h	R/W-0h	R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 69. Register 67 Field Descriptions

Bit	Field	Type	Reset	Description
15-5	0	R/W	0h	Must write 0
4-1	LVDS_DCLK_DELAY_PROG[3:0]	R/W	0h	The LVDS DCLK output delay is programmable with 110-ps steps. Delay values are in twos complement format. Increasing the positive delay increases setup time and reduces hold time, and vice-versa for the negative delay. 0000 = No delay 0001 = 110 ps 0010 = 220 ps … 1110 = –220 ps 1111 = –110ps …
0	0	R/W	0h	Must write 0

13.1.3 VCA Register Map

This section discusses the VCA registers. A register map is available in Table 70.

Table 70. VCA Register Map

REGISTER ADDRESS		REGISTER DATA(1)															
DECIMAL	HEX	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
195	C3	0	0	PGA_GAIN	0	0	0	0	0	PGA_CLAMP_DIS	PGA_CLAMP_LVL	0	PGA_HPF_DIS	LPF_PROG			
196	C4	LNA_GAIN_IND_EN	LNA_GAIN_GBL		LNA_HPF_DIS	0	INPUT_CLAMP_LVL		ACT_TERM_EN	GBL_ACTIVE_TERM		ACT_TERM_IND_RES_EN	ACT_TERM_IND_RES				
197	C5	GBL_PDWN	FAST_PDWN	PDWN_LNA	PDWN_VCA_PGA	POW_MODES		LOW_NF	0	PDCH 15/16	PDCH 13/14	PDCH 11/12	PDCH9/10	PDCH7/8	PDCH5/6	PDCH3/4	PDCH1/2
198	C6	0	CW_HPF_EN	CW_HPF_FB_RES		CW_CLK_MODE		DIS_CW_AMP	CW_TGC_SEL	0	1X_CLK_BUF_MODE	16X_CLK_BUF_MODE	CW_SUM_AMP_GAIN				
199	C7	CW_MIX_PH_CH7/8				CW_MIX_PH_CH5/6				CW_MIX_PH_CH3/4				CW_MIX_PH_CH1/2			
200	C8	CW_MIX_PH_CH15/16				CW_MIX_PH_CH13/14				CW_MIX_PH_CH11/12				CW_MIX_PH_CH9/10			
201	C9	LNA_GAIN_CH15/16		LNA_GAIN_CH13/14		LNA_GAIN_CH11/12		LNA_GAIN_CH9/10		LNA_GAIN_CH7/8		LNA_GAIN_CH5/6		LNA_GAIN_CH3/4		LNA_GAIN_CH1/2	
203	CB	0	0	0	0	0	0	0	0	EN_DIG_TGC	DIG_TGC_ATTENUATION			LNA_HPF_PROG		0	0
205	CD	PGA_CLAMP_HALF	SUPRESS_HIGHER_HARMONICS	V2I_CLAMP	0	0	0	0	RED_LNA_HPF_3X	0	0	0	0	0	0	0	0
213	D5	GBL_PDWN_DIE2	FAST_PDWN_DIE2	PDWN_LNA_DIE2	PDWN_VCA_PGA_DIE2	POW_MODES_DIE2		LOW_NF_DIE2	0	PDCH15	PDCH13	PDCH11	PDCH9	PDCH7	PDCH5	PDCH3	PDCH1
215	D7	CW_MIX_PH_CH7				CW_MIX_PH_CH5				CW_MIX_PH_CH3				CW_MIX_PH_CH1			
216	D8	CW_MIX_PH_CH15				CW_MIX_PH_CH13				CW_MIX_PH_CH11				CW_MIX_PH_CH9			
217	D9	LNA_GAIN_CH15		LNA_GAIN_CH13		LNA_GAIN_CH11		LNA_GAIN_CH9		LNA_GAIN_CH7		LNA_GAIN_CH5		LNA_GAIN_CH3		LNA_GAIN_CH1	

(1) The default value of all registers is 0.

13.1.3.1 Description of VCA Registers

13.1.3.1.1 Register 195 (address = C3h)

Table 71. Register 195

15	14	13	12	11	10	9	8
0	0	PGA_GAIN	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PGA_CLAMP_DIS	PGA_CLAMP_LVL	0	PGA_HPF_DIS	LPF_PROG			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 72. Register 195 Field Descriptions

Bit	Field	Type	Reset	Description
15-14	0	R/W	0h	Must write 0
13	PGA_GAIN	R/W	0h	0 = PGA gain set to 24 dB 1 = PGA gain set to 30 dB
12-8	0	R/W	0h	Must write 0
7	PGA_CLAMP_DIS	R/W	0h	When POW_MODES (register 197, bits 11-10) is 01 or 10: 0 = Disables the PGA current clamp circuit 1 = Enables the PGA current clamp circuit before the PGA outputs When POW_MODES (register 197, bits 11-10) is 00: 0 = Enables the PGA current clamp circuit 1 = Disables the PGA current clamp circuit before the PGA outputs PGA_CLAMP_LVL (register 195, bit 6) determines the current clamp level.
6	PGA_CLAMP_LVL	R/W	0h	0 = –2 dBFS 1 = 0 dBFS Note that the current clamp circuit ensures that the PGA output is in the linear range. For example, at a 0-dBFS setting, the PGA output HD3 worsens by 3 dB at a –2-dBFS ADC input. In normal operation, the current clamp function can be set as 0 dBFS.
5	0	R/W	0h	Must write 0
4	PGA_HPF_DIS	R/W	0h	0 = PGA high-pass filter enabled 1 = PGA high-pass filter disabled
3-0	LPF_PROG	R/W	0h	These bits program the cutoff frequency of the antialiasing low-pass filter. 0000 = 15 MHz 0100 = 20 MHz 0101 = 35 MHz 0110 = 30 MHz 0111 = 50 MHz 1000 = 10 MHz All other bit combinations are not applicable

13.1.3.1.2 Register 196 (address = C4h)

Table 73. Register 196

15	14	13	12	11	10	9	8
LNA_GAIN_IND_EN	LNA_GAIN_GBL		LNA_HPF_DIS	0	INPUT_CLAMP_LVL		ACT_TERM_EN
R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
GBL_ACTIVE_TERM		ACT_TERM_IND_RES_EN	ACT_TERM_IND_RES				
R/W-0h		R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 74. Register 196 Field Descriptions

Bit	Field	Type	Reset	Description
15	LNA_GAIN_IND_EN	R/W	0h	0 = Disabled 1 = LNA individual channel control enabled See register 201 and register 217 for details.
14-13	LNA_GAIN_GBL	R/W	0h	00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Reserved
12	LNA_HPF_DIS	R/W	0h	0 = LNA high-pass filter enabled 1 = LNA high-pass filter disabled
11	0	R/W	0h	Must write 0
10-9	INPUT_CLAMP_LVL	R/W	0h	00 = Auto setting 01 = 1.5 V_{PP} 10 = 1.15 V_{PP} 11 = 0.6 V_{PP}
8	ACT_TERM_EN	R/W	0h	0 = Active termination disabled 1 = Active termination enabled
7-6	GBL_ACTIVE_TERM	R/W	0h	00 = 50 Ω 01 = 100 Ω 10 = 200 Ω 11 = 400 Ω Note that the device adjusts resistor mapping (register 196, bits 4-0) automatically. 50-Ω active termination is not supported in the 12-dB LNA setting. Instead, 00 represents high-impedance mode when LNA gain is 12 dB.
5	ACT_TERM_IND_RES_EN	R/W	0h	0 = Disabled 1 = Internal active termination individual resistor control enabled
4-0	ACT_TERM_IND_RES	R/W	0h	To enable this bit, ensure that ACT_TERM_IND_RES_EN (register 196, bit 5) is 1. For further details, see Table 75.

Table 75. ACT_TERM_IND_RES(1) (Register 196, Bits 4-0) versus LNA Input Impedances

BIT SETTINGS	ACT_TERM_IND_RES (Register 196, Bits 4-0)		
	LNA = 12 dB	LNA = 18 dB	LNA = 24 dB
00000	High-Z	High-Z	High-Z
00001	150 Ω	90 Ω	50 Ω
00010	300 Ω	180 Ω	100 Ω
00011	100 Ω	60 Ω	33 Ω
00100	600 Ω	360 Ω	200 Ω
00101	120 Ω	72 Ω	40 Ω
00110	200 Ω	120 Ω	66.67 Ω
00111	86 Ω	51 Ω	29 Ω
01000	1200 Ω	720 Ω	400 Ω
01001	133 Ω	80 Ω	44 Ω
01010	240 Ω	144 Ω	80 Ω
01011	92 Ω	55 Ω	31 Ω
01100	400 Ω	240 Ω	133 Ω
01101	109 Ω	65 Ω	36 Ω
01110	171 Ω	103 Ω	57 Ω
01111	80 Ω	48 Ω	27 Ω
10000	1500 Ω	900 Ω	500 Ω
10001	136 Ω	82 Ω	45 Ω
10010	250 Ω	150 Ω	83 Ω
10011	94 Ω	56 Ω	31 Ω
10100	429 Ω	257 Ω	143 Ω
10101	111 Ω	67 Ω	37 Ω
10110	176 Ω	106 Ω	59 Ω
10111	81 Ω	49 Ω	27 Ω
11000	667 Ω	400 Ω	222 Ω
11001	122 Ω	73 Ω	41 Ω
11010	207 Ω	124 Ω	69 Ω
11011	87 Ω	52 Ω	29 Ω
11100	316 Ω	189 Ω	105 Ω
11101	102 Ω	61 Ω	34 Ω
11110	154 Ω	92 Ω	51 Ω
11111	76 Ω	46 Ω	25 Ω

(1) Total device input impedance is given by the parallel combination of the mentioned active termination resistance and a passive resistance of 15 kΩ.

13.1.3.1.3 Register 197 (address = C5h)

Table 76. Register 197

15	14	13	12	11	10	9	8
GBL_PDWN	FAST_PDWN	PDWN_LNA	PDWN_VCA_PGA	POW_MODES		LOW_NF	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDCH15/16	PDCH13/14	PDCH11/12	PDCH9/10	PDCH7/8	PDCH5/6	PDCH3/4	PDCH1/2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 77. Register 197 Field Descriptions

Bit	Field	Type	Reset	Description
15	GBL_PDWN	R/W	0h	0 = Normal operation 1 = When ADD_OFFSET is set to 0, the LNA, VCAT, and PGA are completely powered down (slow wake response) for both VCA dies 1 and 2 When ADD_OFFSET is set to 1, the LNA, VCAT, and PGA are completely powered down (slow wake response) for only VCA die 1. This bit can overwrite FAST PDWN (register 197, bit 14). Note that enabling this bit does not power-down the ADC. This bit only powers down the VCA dies.
14	FAST_PDWN	R/W	0h	0 = Normal operation 1 = When ADD_OFFSET set to 0, the LNA, VCAT, and PGA are partially powered down (fast wake response) for both VCA dies 1 and 2 When ADD_OFFSET set to 1, the LNA, VCAT, and PGA are partially powered down (fast wake response) for only VCA die 1. Note that enabling this bit does not power-down the ADC. This bit only powers down the VCA dies.
13	PDWN_LNA	R/W	0h	0 = Normal operation 1 = When ADD_OFFSET is set to 0, only the LNA is powered down for both VCA dies 1 and 2 When ADD_OFFSET is set to 1, only the LNA is powered down for VCA die 1.
12	PDWN_VCA_PGA	R/W	0h	0 = Normal operation 1 = When ADD_OFFSET is set to 0, the VCAT and PGA are powered down for both VCA dies 1 and 2 When ADD_OFFSET set to 1, the VCAT and PGA are powered down for only VCA die 1.
11-10	POW_MODES	R/W	0h	00 = Low-noise mode 01 = Set to low-power mode; at 30-dB PGA the total chain gain can slightly change 10 = Set to medium-power mode; at 30-dB PGA the total chain gain can slightly change 11 = Reserved When ADD_OFFSET is set to 0, the device performs an operation as this POW_MODES section describes on both VCA dies 1 and 2. When ADD_OFFSET is set to 1, the device performs an operation as this POW_MODES section describes only on VCA die 1.
9	LOW_NF	R/W	0h	This mode can be used to improve the noise figure for high-impedance probes. To write to this register, ensure that POW MODES (register 197, bits 11-10) = 00. 0 = Disable low-noise figure mode 1 = When ADD_OFFSET is set to 0, the low-noise figure mode is enabled on both VCA dies 1 and 2 When ADD_OFFSET set to 1, the low-noise figure mode is enabled only on VCA die 1.
8	0	R/W	0h	Must write 0
7	PDCH15/16	R/W	0h	0 = Default 1 = When ADD_OFFSET is 0, channels 15 and 16 are powered down; when ADD_OFFSET is 1, only channel 16 is powered down This bit only powers down the channel of the VCA die (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.

Table 77. Register 197 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PDCH13/14	R/W	0h	0 = Default 1 = When ADD_OFFSET is 0, channels 13 and 14 are powered down; when ADD_OFFSET is 1, only channel 14 is powered down This bit only powers down the channel of the VCA die (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
5	PDCH11/12	R/W	0h	0 = Default 1 = When ADD_OFFSET is 0, channels 11 and 12 are powered down; when ADD_OFFSET is 1, only channel 12 is powered down This bit only powers down the channel of the VCA die (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
4	PDCH9/10	R/W	0h	0 = Default 1 = When ADD_OFFSET is 0, channels 9 and 10 are powered down; when ADD_OFFSET is 1, only channel 10 is powered down This bit only powers down the channel of the VCA die (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
3	PDCH7/8	R/W	0h	0 = Default 1 = When ADD_OFFSET is 0, channels 7 and 8 are powered down; when ADD_OFFSET is 1, only channel 8 is powered down This bit only powers down the channel of the VCA die (that is, LNA + VCA + PGA). This bit doesn't have any impact on ADC channel.
2	PDCH5/6	R/W	0h	0 = Default 1 = When ADD_OFFSET is 0, channels 5 and 6 are powered down; when ADD_OFFSET is 1, only channel 6 is powered down This bit only powers down the channel of the VCA die (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
1	PDCH3/4	R/W	0h	0 = Default 1 = When ADD_OFFSET is 0, channels 3 and 4 are powered down; when ADD_OFFSET is 1, only channel 4 is powered down This bit only powers down the channel of the VCA die (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
0	PDCH1/2	R/W	0h	0 = Default 1 = When ADD_OFFSET is 0, channels 1 and 2 are powered down; when ADD_OFFSET is 1, only channel 2 is powered down This bit only powers down the channel of the VCA die (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.

13.1.3.1.4 Register 198 (address = C6h)

Table 78. Register 198

15	14	13	12	11	10	9	8
0	CW_HPF_EN	CW_HPF_FB_RES		CW_CLK_MODE		DIS_CW_AMP	CW_TGC_SEL
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	1X_CLK_BUF_MODE	16X_CLK_BUF_MODE	CW_SUM_AMP_GAIN				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 79. Register 198 Field Descriptions

Bit	Field	Type	Reset	Description
15	0	R/W	0h	Must write 0
14	CW_HPF_EN	R/W	0h	0 = Normal operation 1 = Enables CW output high-pass filter
13-12	CW_HPF_FB_RES	R/W	0h	If CW_HPF_EN = 1 then the value of the CW high-pass filter feedback resistor is given by: 00 = 400 Ω 01 = 133 Ω 10 = 80 Ω 11 = 57 Ω If CW_HPF_EN = 0 then these bits are ignored and the feedback path remains open.
11-10	CW_CLK_MODE	R/W	0h	00 = 16X mode 01 = 8X mode 10 = 4X mode 11 = 1X mode
9	DIS_CW_AMP	R/W	0h	0 = CW summing amplifier enabled 1 = CW summing amplifier disabled Note that this bit is only effective in CW mode.
8	CW_TGC_SEL	R/W	0h	0 = TGC mode 1 = CW mode Note that the VCAT and PGA still function in CW mode. Power-down the VCAT and PGA separately with PDWN_VCA_PGA (register 197, bit 12).
7	0	R/W	0h	Must write 0
6	1X_CLK_BUF_MODE	R/W	0h	0 = Accepts CMOS clock 1 = Accepts differential clock
5	16X_CLK_BUF_MODE	R/W	0h	0 = Accepts differential clock 1 = Accepts CMOS clock
4-0	CW_SUM_AMP_GAIN	R/W	0h	These bits select the feedback resistor for the CW amplifier, as per Table 75.

Table 80. CW Summing Amplifier Feedback Resistor

REGISTER 198 (Bits 4-0)	FEEDBACK RESISTOR	REGISTER 198 (Bits 4-0)	FEEDBACK RESISTOR	REGISTER 198 (Bits 4-0)	FEEDBACK RESISTOR
00000	Open	01011	111 Ω	10110	153 Ω
00001	250 Ω	01100	333 Ω	10111	95 Ω
00010	250 Ω	01101	142 Ω	11000	666 Ω
00011	125 Ω	01110	142 Ω	11001	181 Ω
00100	500 Ω	01111	90 Ω	11010	181 Ω
00101	166 Ω	10000	2000 Ω	11011	105 Ω
00110	166 Ω	10001	222 Ω	11100	285 Ω
00111	100 Ω	10010	222 Ω	11101	133 Ω
01000	1000 Ω	10011	117 Ω	11110	133 Ω
01001	200 Ω	10100	400 Ω	11111	87 Ω
01010	200 Ω	10101	153 Ω		

13.1.3.1.5 Register 199 (address = C7h)

Table 81. Register 199

15	14	13	12	11	10	9	8
CW_MIX_PH_CH[7/8]				CW_MIX_PH_CH[5/6]			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
CW_MIX_PH_CH[3/4]				CW_MIX_PH_CH[1/2]			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 82. Register 199 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	CW_MIX_PH_CH[7/8]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. The functionality of these bits depends upon the value of the ADD_OFFSET bit. When the ADD_OFFSET bit is set to 0, setting bits 15-12 programs the CW phase of channels 7 and 8. When the ADD_OFFSET bit is set to 1, setting bits 15-12 programs the CW phase of only channel 8.
11-8	CW_MIX_PH_CH[5/6]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. The functionality of these bits depends upon the value of the ADD_OFFSET bit. When the ADD_OFFSET bit is set to 0, setting bits 11-8 programs the CW phase of channels 5 and 6. When the ADD_OFFSET bit is set to 1, setting bits 11-8 programs the CW phase of only channel 6.
7-4	CW_MIX_PH_CH[3/4]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. The functionality of these bits depends upon the value of the ADD_OFFSET bit. When the ADD_OFFSET bit is set to 0, setting bits 7-4 programs the CW phase of channels 3 and 4. When the ADD_OFFSET bit is set to 1, setting bits 7-4 programs the CW phase of only channel 4.
3-0	CW_MIX_PH_CH[1/2]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. The functionality of these bits depends upon the value of the ADD_OFFSET bit. When the ADD_OFFSET bit is set to 0, setting bits 3-0 programs the CW phase of channels 1 and 2. When the ADD_OFFSET bit is set to 1, setting bits 3-0 programs the CW phase of only channel 2.

Table 83. CW Mixer Phase Delay versus Register Settings

BIT SETTINGS	CW_MIX_PH_CHX, CW_MIX_PH_CHY PHASE SHIFT
0000	0
0001	22.5°
0010	45°
0011	67.5°
0100	90°
0101	112.5°
0110	135°
0111	157.5°
1000	180°
1001	202.5°
1010	225°
1011	247.5°
1100	270°
1101	292.5°
1110	315°
1111	337.5°

13.1.3.1.6 Register 200 (address = C8h)

Table 84. Register 200

15	14	13	12	11	10	9	8
CW_MIX_PH_CH[15/16]				CW_MIX_PH_CH[13/14]			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
CW_MIX_PH_CH[11/12]				CW_MIX_PH_CH[9/10]			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 85. Register 200 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	CW_MIX_PH_CH[15/16]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. The functionality of these bits depends upon the value of the ADD_OFFSET bit. When the ADD_OFFSET bit is set to 0, setting bits 15-12 programs the CW phase of channels 15 and 16. When the ADD_OFFSET bit is set to 1, setting bits 15-12 programs the CW phase of only channel 16.
11-8	CW_MIX_PH_CH[13/14]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. The functionality of these bits depends upon the value of the ADD_OFFSET bit. When the ADD_OFFSET bit is set to 0, setting bits 11-8 programs the CW phase of channels 13 and 14. When the ADD_OFFSET bit is set to 1, setting bits 11-8 programs the CW phase of only channel 14.
7-4	CW_MIX_PH_CH[11/12]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. The functionality of these bits depends upon the value of the ADD_OFFSET bit. When the ADD_OFFSET bit is set to 0, setting bits 7-4 programs the CW phase of channels 11 and 12. When the ADD_OFFSET bit is set to 1, setting bits 7-4 programs the CW phase of only channel 12.
3-0	CW_MIX_PH_CH[9/10]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. The functionality of these bits depends upon the value of the ADD_OFFSET bit. When the ADD_OFFSET bit is set to 0, setting bits 3-0 programs the CW phase of channels 9 and 10. When the ADD_OFFSET bit is set to 1, setting bits 3-0 programs the CW phase of only channel 10.

13.1.3.1.7 Register 201 (address = C9h)

Table 86. Register 201

15	14	13	12	11	10	9	8
LNA_GAIN_CH[15/16]		LNA_GAIN_CH[13/14]		LNA_GAIN_CH[11/12]		LNA_GAIN_CH[9/10]	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
LNA_GAIN_CH[7/8]		LNA_GAIN_CH[5/6]		LNA_GAIN_CH[3/4]		LNA_GAIN_CH[1/2]	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 87. Register 201 Field Descriptions

Bit	Field	Type	Reset	Description
15-14	LNA_GAIN_CH[15/16]	R/W	0h	To enable this bit, ensure that LNA_GAIN_IND_EN (register 196, bit 15) is 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use The functionality of this bit depends on the ADD_OFFSET bit. When ADD_OFFSET is 0, the gain of channels 15 and 16 are programmed; when ADD_OFFSET is 1, only the gain of channel 16 is programmed.
13-12	LNA_GAIN_CH[13/14]	R/W	0h	To enable this bit, ensure that LNA_GAIN_IND_EN (register 196, bit 15) is 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use The functionality of this bit depends on the ADD_OFFSET bit. When ADD_OFFSET is 0, the gain of channels 13 and 14 are programmed; when ADD_OFFSET is 1, only the gain of channel 14 is programmed.
11-10	LNA_GAIN_CH[11/12]	R/W	0h	To enable this bit, ensure that LNA_GAIN_IND_EN (register 196, bit 15) is 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use The functionality of this bit depends on the ADD_OFFSET bit. When ADD_OFFSET is 0, the gain of channels 11 and 12 are programmed; when ADD_OFFSET is 1, only the gain of channel 12 is programmed.
9-8	LNA_GAIN_CH[9/10]	R/W	0h	To enable this bit, ensure that LNA_GAIN_IND_EN (register 196, bit 15) is 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use The functionality of this bit depends on the ADD_OFFSET bit. When ADD_OFFSET is 0, the gain of channels 9 and 10 are programmed; when ADD_OFFSET is 1, only the gain of channel 10 is programmed.

Table 87. Register 201 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	LNA_GAIN_CH[7/8]	R/W	0h	To enable this bit, ensure that LNA_GAIN_IND_EN (register 196, bit 15) is 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use The functionality of this bit depends on the ADD_OFFSET bit. When ADD_OFFSET is 0, the gain of channels 7 and 8 are programmed; when ADD_OFFSET is 1, only the gain of channel 8 is programmed.
5-4	LNA_GAIN_CH[5/6]	R/W	0h	To enable this bit, ensure that LNA_GAIN_IND_EN (register 196, bit 15) is 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use The functionality of this bit depends on the ADD_OFFSET bit. When ADD_OFFSET is 0, the gain of channels 5 and 6 are programmed; when ADD_OFFSET is 1, only the gain of channel 6 is programmed.
3-2	LNA_GAIN_CH[3/4]	R/W	0h	To enable this bit, ensure that LNA_GAIN_IND_EN (register 196, bit 15) is 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use The functionality of this bit depends on the ADD_OFFSET bit. When ADD_OFFSET is 0, the gain of channels 3 and 4 are programmed; when ADD_OFFSET is 1, only the gain of channel 4 is programmed.
1-0	LNA_GAIN_CH[1/2]	R/W	0h	To enable this bit, ensure that LNA_GAIN_IND_EN (register 196, bit 15) is 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use The functionality of this bit depends on the ADD_OFFSET bit. When ADD_OFFSET is 0, the gain of channels 1 and 2 are programmed; when ADD_OFFSET is 1, only the gain of channel 2 is programmed.

13.1.3.1.8 Register 203 (address = CBh)

Table 88. Register 203

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EN_DIG_TGC	DIG_TGC_ATTENUATION			LNA_HPF_PROG		0	0
R/W-0h	R/W-0h			R/W-0h		R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 89. Register 203 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	0	R/W	0h	Must write 0
7	EN_DIG_TGC	R/W	0h	0 = Disable digital TGC attenuator 1 = Enable digital TGC attenuator
6-4	DIG_TGC_ATTENUATION	R/W	0h	When EN_DIG_TGC (register 203, bit 7) is set to 1, then the digital attenuation in the TGC path is programmed as follows: 000 = 0-dB attenuation 001 = 6-dB attenuation 010 = 12-dB attenuation 011 = 18-dB attenuation 100 = 24-dB attenuation. 101 = 30-dB attenuation 110 = 36-dB attenuation 111 = 42-dB attenuation
3-2	LNA_HPF_PROG	R/W	0h	00 = 100 kHz 01 = 50 kHz 10 = 200 kHz 11 = 150 kHz with 0.015 µF on INMx
1-0	0	R/W	0h	Must write 0

13.1.3.1.9 Register 205 (address = CDh)

Table 90. Register 205

15	14	13	12	11	10	9	8
PGA_CLAMP_HALF	SUPRESS_HIGHER_HARMONICS	V2I_CLAMP	0	0	0	0	RED_LNA_HPF_3X
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 91. Register 205 Field Descriptions

Bit	Field	Type	Reset	Description
15	PGA_CLAMP_HALF	R/W	0h	0 = Disables –6-dB PGA clamp 1 = Enables a –6-dB PGA clamp setting (that is, the PGA output HD3 worsens by 3 dB at a –6-dBFS ADC input). The actual PGA output is reduced to approximately 1.5 V_{PP}. As a result, the device low-pass filter (LPF) is not saturated and can suppress harmonic signals better at the PGA output. Resulting from the reduction of the PGA output, the ADC output dynamic range is affected.
14	SUPRESS_HIGHER_HARMONICS	R/W	0h	0 = Disables a 1st-order, 5-MHz LPF filter 1 = Enables a 1st-order, 5-MHz LPF filter to suppress signals > 5 MHz or high-order harmonics
13	V2I_CLAMP	R/W	0h	0 = Disables V2I clamp in the PGA 1 = Enables V2I clamp in the PGA
12-9	0	R/W	0h	Must write 0
8	RED_LNA_HPF_3X	R/W	0h	0 = The LNA HPF corner frequency is given as per the LNA_HPF_PROG bit description 1 = The LNA HPF corner frequency reduces by 3x as per the LNA_HPF_PROG bit description. For example, if LNA_HPF_PROG = 01 and RED_LNA_HPF_3X = 1, then the LNA HPF corner is given by the equation 50 kHz / 3 = 16.6 kHz.
7-0	0	R/W	0h	Must write 0

13.1.3.1.10 Register 213 (address = D5h)

Table 92. Register 213

15	14	13	12	11	10	9	8
GBL_PDWN_DIE2	FAST_PDWN_DIE2	PDWN_LNA_DIE2	PDWN_VCA_PGA_DIE2	POW_MODES_DIE2		LOW_NF_DIE2	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PDCH15	PDCH13	PDCH11	PDCH9	PDCH7	PDCH5	PDCH3	PDCH1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 93. Register 213 Field Descriptions

Bit	Field	Type	Reset	Description
15	GBL_PDWN_DIE2	R/W	0h	0 = Normal operation 1 = When ADD_OFFSET is set to 1, the LNA, VCAT, and PGA are completely powered down (slow wake response) for only VCA die 2. Note that enabling this bit does not power-down the ADC. This bit only powers down VCA dies.
14	FAST_PDWN_DIE2	R/W	0h	0 = Normal operation 1 = When ADD_OFFSET set to 1, the LNA, VCAT, and PGA partially powered down (fast wake response) for only VCA die 2. Note that enabling this bit does not power-down the ADC. This bit only powers down VCA dies.
13	PDWN_LNA_DIE2	R/W	0h	0 = Normal operation 1 = When ADD_OFFSET is set to 1, only the LNA is powered down for VCA die 2.
12	PDWN_VCA_PGA_DIE2	R/W	0h	0 = Normal operation 1 = When ADD_OFFSET set to 1, the VCAT and PGA are powered down for only VCA die 2.
11-10	POW_MODES_DIE2	R/W	0h	00 = Low-noise mode 01 = Set to low-power mode. At 30-dB PGA, the total chain gain may slightly change. 10 = Set to medium-power mode. At 30-dB PGA, the total chain gain may slightly change. 11 = Reserved When ADD_OFFSET set to 1, the device performs an operation as described in this POW_MODES_DIE2 section only on die 2.
9	LOW_NF_DIE2	R/W	0h	This mode can be used to improve the noise figure for high-impedance probes. To write to this register, set POW MODES_DIE2 (register 213, bits 11-10) = 00. 0 = Disable the low-noise figure mode 1 = When ADD_OFFSET set to 1, the low-noise figure mode is enabled on only on VCA die 2.
8	0	R/W	0h	Must write 0
7	PDNCH15	R/W	0h	0 = Default 1 = When ADD_OFFSET is 1, channel 15 is powered down This bit powers down the channel of the VCA die only (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
6	PDNCH13	R/W	0h	0 = Default 1 = When ADD_OFFSET is 1, channel 13 is powered down This bit powers down the channel of the VCA die only (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
5	PDNCH11	R/W	0h	0 = Default 1 = When ADD_OFFSET is 1, channel 11 is powered down This bit powers down the channel of the VCA die only (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
4	PDNCH9	R/W	0h	0 = Default 1 = When ADD_OFFSET is 1, channel 9 is powered down This bit powers down the channel of the VCA die only (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.

Table 93. Register 213 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PDNCH7	R/W	0h	0 = Default 1 = When ADD_OFFSET is 1, channel 7 is powered down This bit powers down the channel of the VCA die only (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
2	PDNCH5	R/W	0h	0 = Default 1 = When ADD_OFFSET is 1, channel 5 is powered down This bit powers down the channel of the VCA die only (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
1	PDNCH3	R/W	0h	0 = Default 1 = When ADD_OFFSET is 1, channel 3 is powered down This bit powers down the channel of the VCA die only (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.
0	PDNCH1	R/W	0h	0 = Default 1 = When ADD_OFFSET is 1, channel 1 is powered down This bit powers down the channel of the VCA die only (that is, LNA + VCA + PGA). This bit does not affect the ADC channel.

13.1.3.1.11 Register 215 (address = D7h)

Table 94. Register 215

15	14	13	12	11	10	9	8
CW_MIX_PH_CH7				CW_MIX_PH_CH5			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
CW_MIX_PH_CH3				CW_MIX_PH_CH1			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 95. Register 215 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	CW_MIX_PH_CH[7]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. When the ADD_OFFSET bit is set to 1, setting bits 15-12 programs the CW phase of channel 7.
11-8	CW_MIX_PH_CH[5]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. When the ADD_OFFSET bit is set to 1, setting bits 11-8 programs the CW phase of channel 5.
7-4	CW_MIX_PH_CH[3]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. When the ADD_OFFSET bit is set to 1, setting bits 7-4 programs the CW phase of channel 3.
3-0	CW_MIX_PH_CH[1]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. When the ADD_OFFSET bit is set to 1, setting bits 3-0 programs the CW phase of channel 1.

13.1.3.1.12 Register 216 (address = D8h)

Table 96. Register 216

15	14	13	12	11	10	9	8
CW_MIX_PH_CH15				CW_MIX_PH_CH13			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
CW_MIX_PH_CH11				CW_MIX_PH_CH9			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 97. Register 216 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	CW_MIX_PH_CH[15]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. When the ADD_OFFSET bit is set to 1, setting bits 15-12 programs the CW phase of channel 15.
11-8	CW_MIX_PH_CH[13]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. When the ADD_OFFSET bit is set to 1, setting bits 11-8 programs the CW phase of channel 13.
7-4	CW_MIX_PH_CH[11]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. When the ADD_OFFSET bit is set to 1, setting bits 7-4 programs the CW phase of channel 11.
3-0	CW_MIX_PH_CH[9]	R/W	0h	These bits control the CW mixer phase. Writing *N* to these bits sets the corresponding channel phase to N × 22.5°. Where, N = 0 to 15; see Table 83 for further details. When the ADD_OFFSET bit is set to 1, setting bits 3-0 programs the CW phase of channel 9.

13.1.3.1.13 Register 217 (address = D9h)

Table 98. Register 217

15	14	13	12	11	10	9	8
LNA_GAIN_CH15		LNA_GAIN_CH13		LNA_GAIN_CH11		LNA_GAIN_CH9	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
LNA_GAIN_CH7		LNA_GAIN_CH5		LNA_GAIN_CH3		LNA_GAIN_CH1	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value

Table 99. Register 217 Field Descriptions

Bit	Field	Type	Reset	Description
15-14	LNA_GAIN_CH[15]	R/W	0h	To enable this bit, set LNA_GAIN_IND_EN (register 196, bit D15) to 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use When ADD_OFFSET is 1, the gain of channel 15 is programmed.
13-12	LNA_GAIN_CH[13]	R/W	0h	To enable this bit, set LNA_GAIN_IND_EN (register 196, bit D15) to 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use When ADD_OFFSET is 1, the gain of channel 13 is programmed.
11-10	LNA_GAIN_CH[11]	R/W	0h	To enable this bit, set LNA_GAIN_IND_EN (register 196, bit D15) to 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use When ADD_OFFSET is 1, the gain of channel 11 is programmed.
9-8	LNA_GAIN_CH[9]	R/W	0h	To enable this bit, set LNA_GAIN_IND_EN (register 196, bit D15) to 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use When ADD_OFFSET is 1, the gain of channel 9 is programmed.
7-6	LNA_GAIN_CH[7]	R/W	0h	To enable this bit, set LNA_GAIN_IND_EN (register 196, bit D15) to 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use When ADD_OFFSET is 1, the gain of channel 7 is programmed.
5-4	LNA_GAIN_CH[5]	R/W	0h	To enable this bit, set LNA_GAIN_IND_EN (register 196, bit D15) to 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use When ADD_OFFSET is 1, the gain of channel 5 is programmed.
3-2	LNA_GAIN_CH[3]	R/W	0h	To enable this bit, set LNA_GAIN_IND_EN (register 196, bit D15) to 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use When ADD_OFFSET is 1, the gain of channel 3 is programmed.
1-0	LNA_GAIN_CH[1]	R/W	0h	To enable this bit, set LNA_GAIN_IND_EN (register 196, bit D15) to 1. 00 = 18 dB 01 = 24 dB 10 = 12 dB 11 = Do not use When ADD_OFFSET is 1, the gain of channel 1 is programmed.

14 器件和文档支持

14.1 文档支持

14.1.1 相关文档

《AFE5816 数据表》，SBAS688

《*MicroStar BGA 封装参考指南*》，SSYZ015

《*高速时钟数据转换器*》，SLYT075

《*宽带差分互阻抗 DAC 输出设计*》，SBAA150

TI 有源滤波器设计工具，WEBENCH® Filter Designer

《CDCM7005 数据表》，SCAS793

《CDCE72010 数据表》，SCAS858

《TLV5626 数据表》，SLAS236

《DAC7821 数据表》，SBAS365

《THS413x 数据表》，SLOS318

《OPA1632 数据表》，SBOS286

《LMK048x 数据表》，SNAS489

《OPA2211 数据表》，SBOS377

《ADS8413 数据表》，SLAS490

《ADS8472 数据表》，SLAS514

《ADS8881 数据表》，SBAS547

《SN74AUP1T04 数据表》，SCES800

《UCC28250 数据表》，SLUSA29

《ISO7240 数据表》，SLLS868

14.2 商标

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14.3 静电放电警告

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14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

15.1 托盘信息

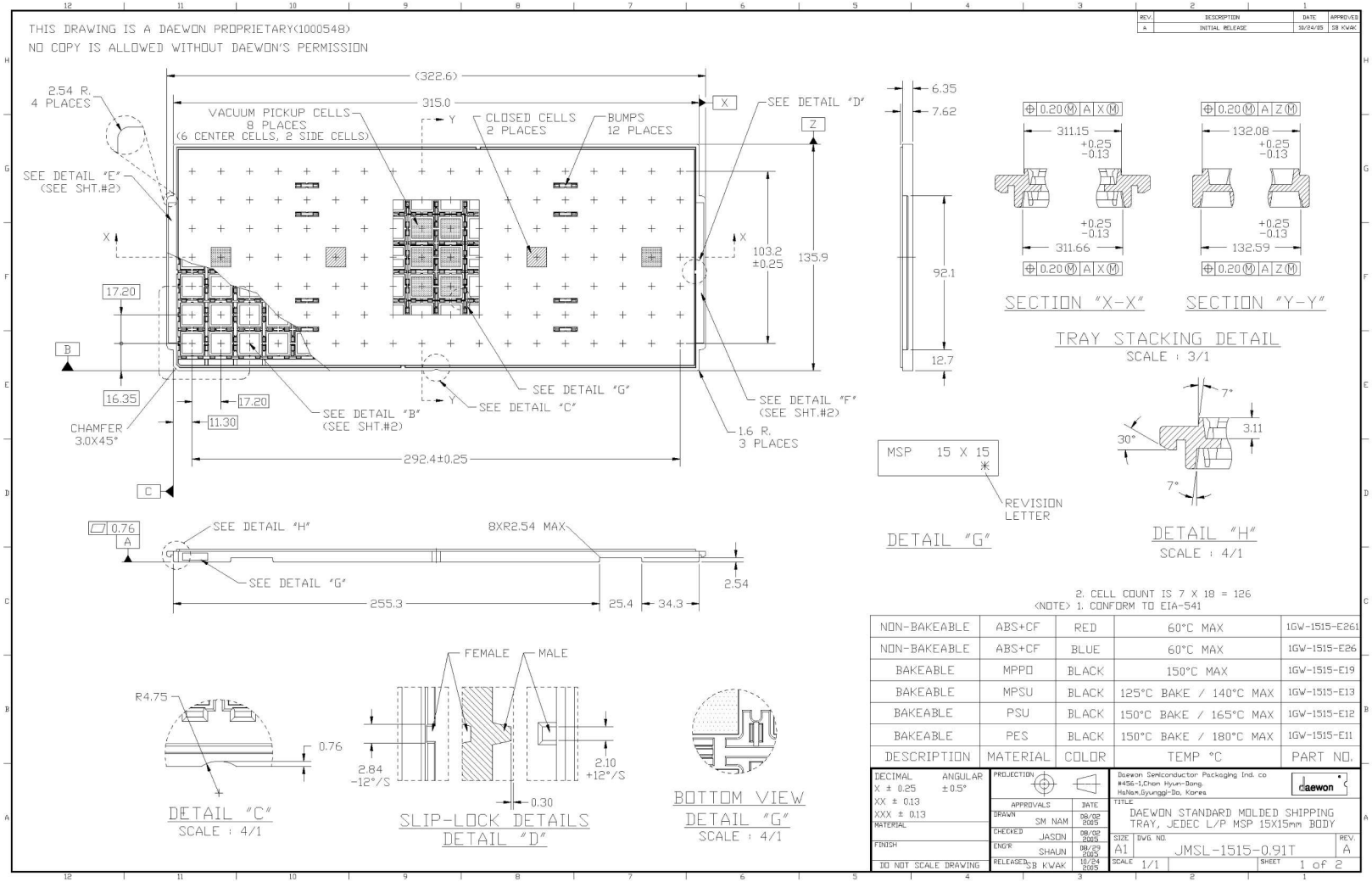


图 **169.** 托盘图，第 **1** 节

托盘信息 **(**接下页**)**

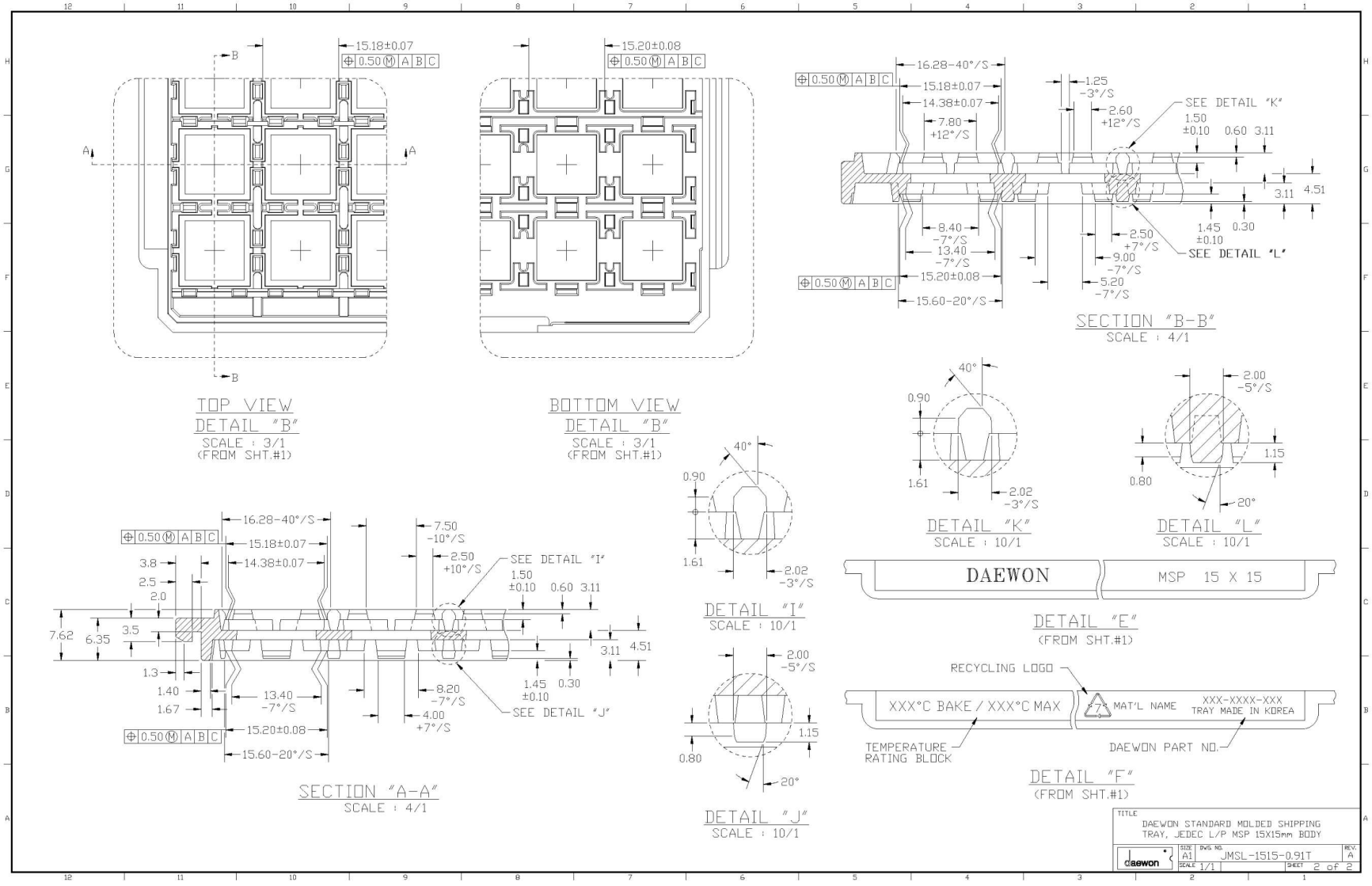


图 **170.** 托盘图，第 **2** 节

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE5818ZBV	ACTIVE	NFBGA	ZBV	289	126	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE5818	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

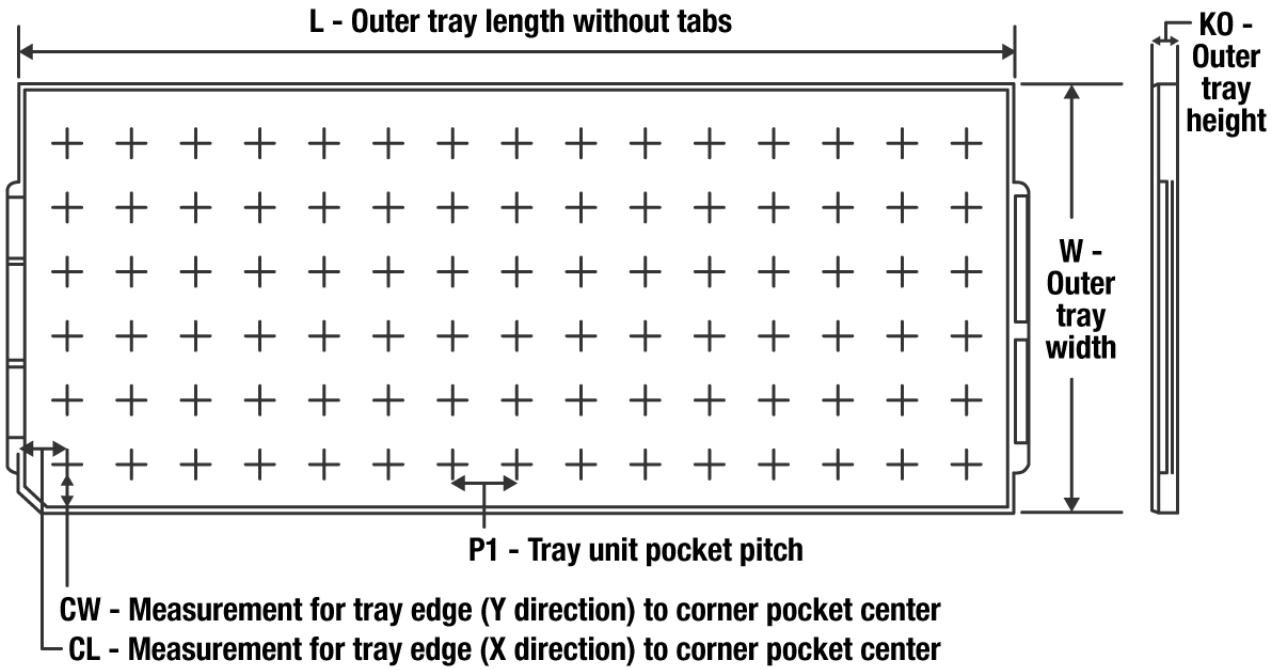
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY

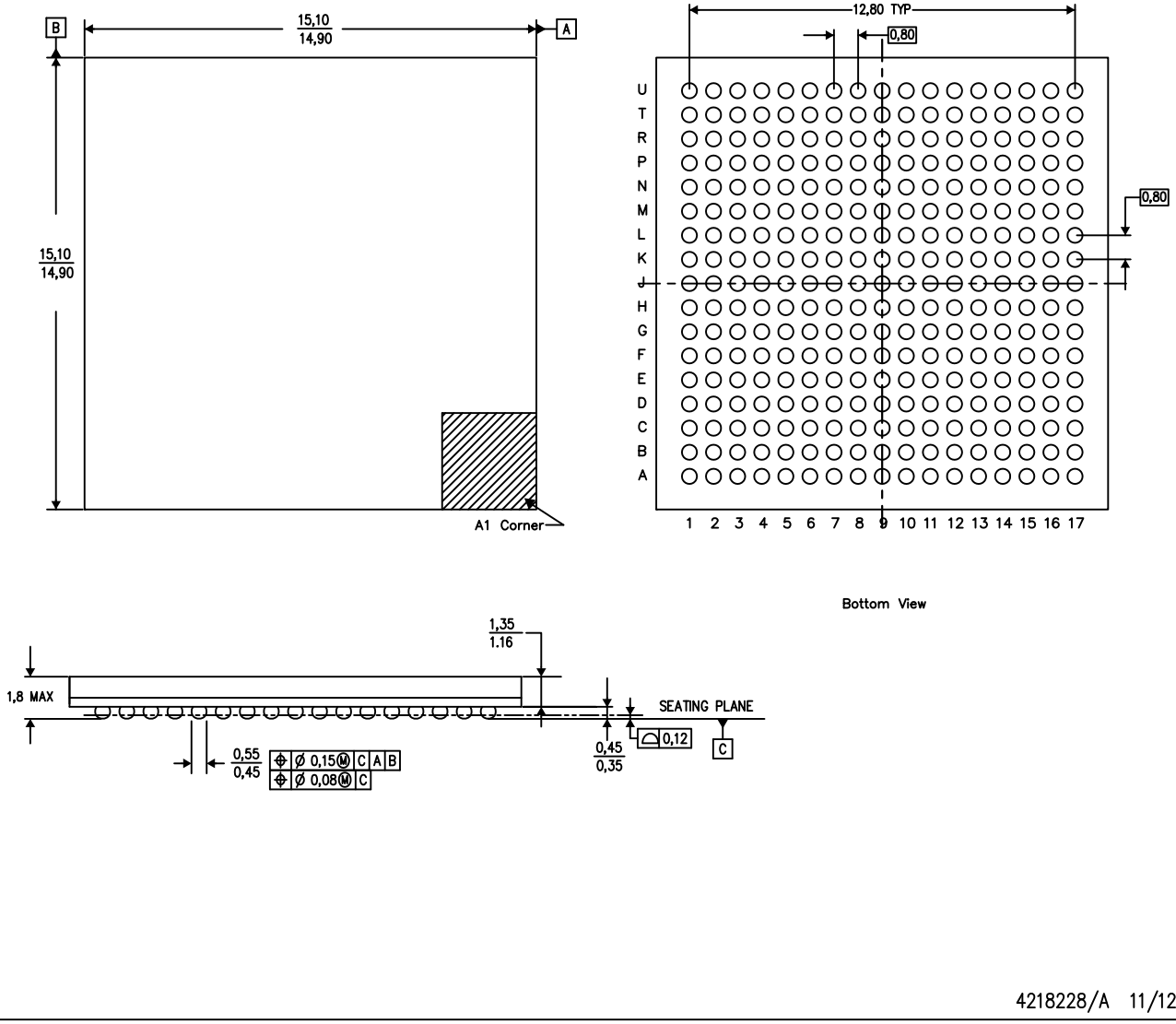


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE5818ZBV	ZBV	NFBGA	289	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35

ZBV (S–PBGA–N289) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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