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TEXAS INSTRUMENTS

TPS2412, TPS2413

ZHCSKC1D – JANUARY 2007 – REVISED OCTOBER 2019

TPS241x N+1 和 ORing 电源轨控制器

1 特性

- 可控制用于 N+1 和 ORing 的外部 FET
- 3V 至 16.5V 的宽电源电压范围
- 控制总线电压范围为 0.8V 至 16.5V
- 线性或开/关控制方法
- 适用于 N 沟道 MOSFET 的内部电荷泵
- 快速器件关断功能可保护总线完整性
- 在热插入时进行主动栅极控制
- 软启动可降低总线瞬变
- 工业温度范围：–40°C 至 85°C
- 8 引脚 TSSOP 和 SOIC 封装

2 应用

- 机架式服务器（机架式）
- 机架式服务器（刀片式）
- 商用网络和服务器 PSU
- 电池备份单元
- 电信系统

3 说明

TPS2412/13 控制器与外部 N 沟道 MOSFET 配合使用，可模拟低正向电压二极管的功能。该器件可用于将多电源与 N+1 配置中的公共总线相结合，或将冗余输入电源总线进行结合。TPS2412 可提供线性启动控制功能，而 TPS2413 可提供开/关控制方法。

TPS2412/13 可用于 各种系统，如服务器和电信系统。这些 应用 通常具有 N+1 冗余电源或冗余电源总线，或二者兼备。在故障和热插拔期间，冗余电源必须具有等效的二极管 OR 来防止产生反向电流。相比于肖特基二极管，TPS2412/13 和 N 沟道 MOSFET 能够以更小的功率损耗提供此功能。
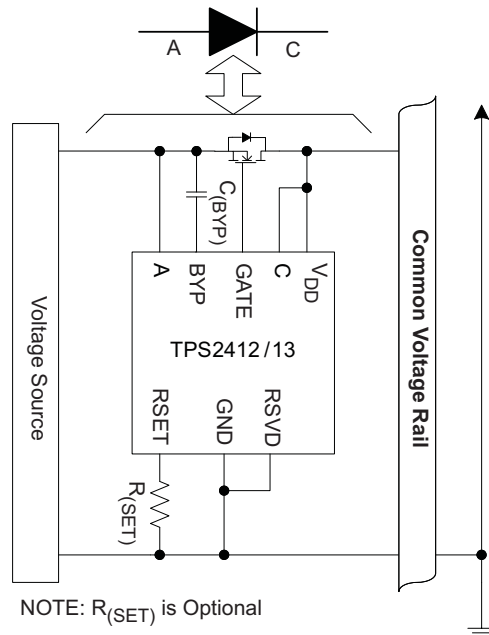
精确的电压感应和可编程关断阈值允许根据各种实施手段和总线特性量身定制运行方式。TPS2412/13 的引脚数更少，因此与 TPS2410/11 版本相比，特性减少。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TPS2412、TPS2413	TSSOP (8)	4.40mm x 3.00mm
	SOIC (8)	3.91mm x 4.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用图

NOTE: R(SET) is Optional

English Data Sheet: SLVS728

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4 修订历史记录

Changes from Revision C (November 2015) to Revision D   **Page**

• Changed Gate positve drive MAX voltage from 11.5 to 12.5 in the *Electrical Characteristics* table...................................... 5
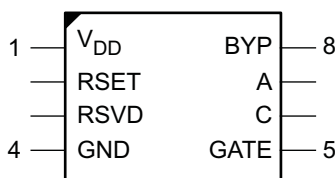
Changes from Revision B (September 2008) to Revision C   **Page**

• 添加了 *ESD* 额定值 表、特性 说明 部分、器件功能模式、应用和实施 部分、电源建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分 1

5   Device Comparison Table

	TPS2410	TPS2411	TPS2412	TPS2413
Linear gate control	√		√	
ON/OFF gate control		√		√
Adjustable turnoff threshold	√	√	√	√
Fast comparator filtering	√	√		
Voltage monitoring	√	√		
Enable control	√	√		
Mosfet fault monitoring	√	√		
Status pin	√	√		

6   Pin Configuration and Functions

PW and D Packages
8-Pins TSSOP and SOIC
Top View

```
      1 ─── ┌─────────────┐ ─── 8
            │ V_DD    BYP │
        ─── │ RSET      A │ ───
        ─── │ RSVD      C │ ───
      4 ─── │ GND    GATE │ ─── 5
            └─────────────┘
```

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1	PWR	Input power for the gate drive charge pump and internal controls. V_{DD} must be connected to a supply voltage ≥ 3 V.
RSET	2	I	Connect a resistor to ground to program the turnoff threshold. Leaving RSET open results in a slightly positive $V_{(A-C)}$ turnoff threshold.
RSVD	3	PWR	This pin must be connected to GND.
GND	4	PWR	Device ground.
GATE	5	O	Connect to the gate of the external MOSFET. Controls the MOSFET to emulate a low forward-voltage diode.
C	6	I	Voltage sense input that connects to the simulated diode cathode. Connect to the MOSFET drain in the typical configuration.
A	7	I	Voltage sense input that connects to the simulated diode anode. A also serves as the reference for the charge-pump bias supply on BYP. Connect to the MOSFET source in the typical configuration.
BYP	8	I/O	Connect a storage capacitor from BYP to A to filter the gate drive supply voltage.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted)[1]

		MIN	MAX	UNIT
	A, C, FLTR, V_{DD}, voltage	−0.3	18	V
	A above C voltage		7.5	V
	C above A voltage		18	V
	GATE[2], BYP voltage	−0.3	30	V
	BYP to A voltage	−0.3	13	V
	GATE above BYP[2] voltage		0.3	V
	RSET[2] voltage	−0.3	7	V
	GATE short to A or C or GND	Indefinite		
T_J	Maximum junction temperature	Internally limited		°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage should not be applied to these pins.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

voltages are referenced to GND (unless otherwise noted)

			MIN	NOM	MAX	UNIT
A, C	Input voltage range TPS2412	$V_{DD} = V_{(C)}$ [1]	3		16.5	V
		$3 \leq V_{DD} \leq 16.5$ V	0.8		16.5	
A to C	Operational voltage				5	V
$R_{(RSET)}$	Resistance range[2]		1.5		∞	kΩ
$C_{(BYP)}$	Capacitance Range[2] [3]		800	2200	10k	pF
T_J	Operating junction temperature		−40		125	°C
T_A	Operating free-air temperature		−40		85	°C

(1) V_{DD} must exceed 3 V to meet gate drive specification
(2) Voltage should not be applied to these pins.
(3) Capacitors should be X7R, 20% or better

7.4 Thermal Information

THERMAL METRIC[1]		TPS241x		UNIT
		PW (TSSOP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.3	110.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	54.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.9	50.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.2	9.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.4	50.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) [1][2][3][4][5][6]

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(A)}$, $V_{©}$, V_{DD}					
V_{DD} UVLO	V_{DD} rising	2.25		2.5	V
	Hysteresis		0.25		
A current	| $I_{(A)}$ |, Gate in active region		0.66	1	mA
	| $I_{(A)}$ |, Gate saturated high		0.1		
C current	| $I_{©}$ |, $V_{(AC)}$ ≤ 0.1 V			10	µA
V_{DD} current	Worst case, gate in active region		4.25	6	mA
	Gate saturated high		1.2		
TURNON					
TPS2412 forward turnon and regulation voltage		7	10	13	mV
TPS2412 forward turnon / turnoff difference	$R_{(RSET)}$ = open		7		mV
TPS2413 forward turnon voltage		7	10	13	mV
TURNOFF					
Fast turnoff threshold voltage	Gate sinks > 10 mA at $V_{(GATE-A)}$ = 2 V	1	3	5	mV
	$V_{(A-C)}$ falling, $R_{(RSET)}$ = open				
	$V_{(A-C)}$ falling, $R_{(RSET)}$ = 28.7 kΩ	−17	−13.25	−10	
	$V_{(A-C)}$ falling, $R_{(RSET)}$ = 3.24 kΩ	−170	−142	−114	
Turnoff delay	$V_{(A)}$ = 12 V, $V_{(A-C)}$: 20 mV → −20 mV, $V_{(GATE-A)}$ begins to decrease		70		ns
Turnoff time	$V_{(A)}$ = 12 V, $C_{(GATE-GND)}$ = 0.01 µF, $V_{(A-C)}$: 20 mV → −20 mV, measure the period to $V_{(GATE)}$ = $V_{(A)}$		130		ns
GATE					
Gate positive drive voltage, $V_{(GATE-A)}$	V_{DD} = 3 V, $V_{(A-C)}$ = 20 mV	6	7	8	V
	5 V ≤ V_{DD} ≤ 18 V, $V_{(A-C)}$ = 20 mV	9	10.2	12.5	
Gate source current	$V_{(A-C)}$ = 50 mV, $V_{(GATE-A)}$ = 4 V	250	290	350	µA
Soft turnoff sink current (TPS2412)	$V_{(A-C)}$ = 4 mV, $V_{(GATE-A)}$ = 2 V	2	5		mA
Fast turnoff pulsed current, $I_{(GATE)}$	$V_{(A-C)}$ = −0.1 V				A
	$V_{(GATE)}$ = 8 V	1.75	2.35		
	$V_{(GATE)}$ = 5 V	1.25	1.75		
	Period	7.5	12.5		µs
Sustain turnoff current, $I_{(GATE)}$	$V_{(A-C)}$ = −0.1 V, $V_{©}$ ≤ V_{DD}, 3 V ≤ V_{DD} ≤ 18 V, 2 V ≤ $V_{(GATE)}$ ≤ 18 V	15	19.5		mA
MISCELLANEOUS					
Thermal shutdown temperature	Temperature rising, T_J		135		°C
Thermal hysteresis			10		°C

(1) [3 V ≤ $V_{(A)}$ ≤ 18 V and $V_{©}$ = V_{DD}] or [0.8 V ≤ $V_{(A)}$ ≤ 3 V and 3 V ≤ V_{DD} ≤ 18 V]
(2) $C_{(BYP)}$ = 2200 pF, $R_{(RSET)}$ = open
(3) −40°C ≤ T_J ≤ 125°C
(4) Positive currents are into pins
(5) Typical values are at 25°C
(6) All voltages are with respect to GND.

7.6 Dissipation Ratings

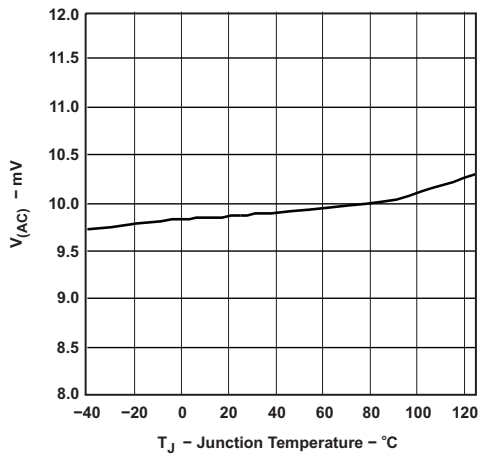| PACKAGE	θ_{JA} – Low k °C/W	θ_{JA} – High k °C/W	POWER RATING High k T_A = 85°C (mW)
PW (TSSOP)	258	159	250
D (SO)	176	97.5	410

7.7 Typical Characteristics

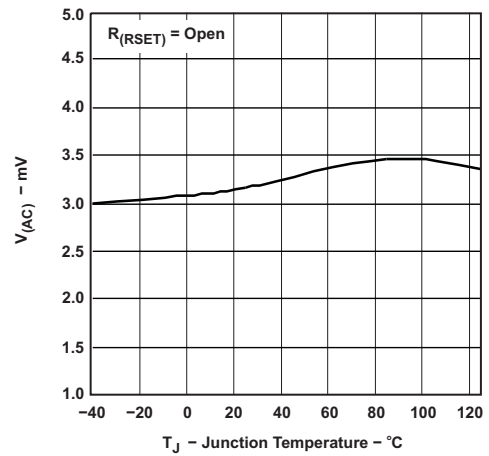Figure 1. TPS2412 $V_{(AC)}$ Regulation Voltage vs Temperature

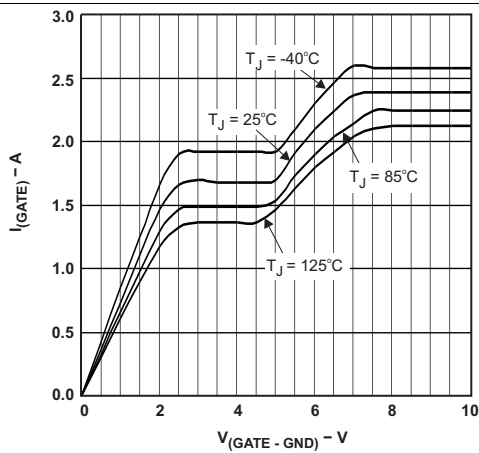Figure 2. Fast Turnoff Threshold vs Temperature

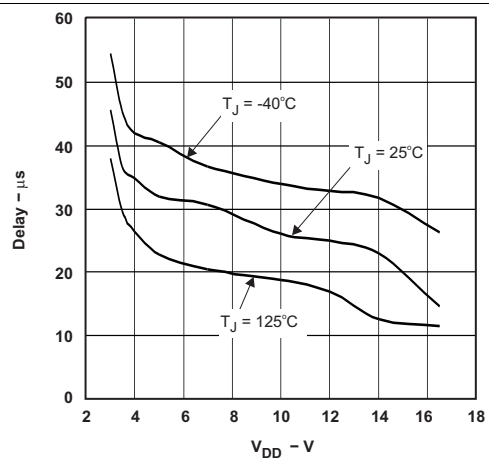

Figure 3. Pulsed Gate Sinking Current vs Gate Voltage

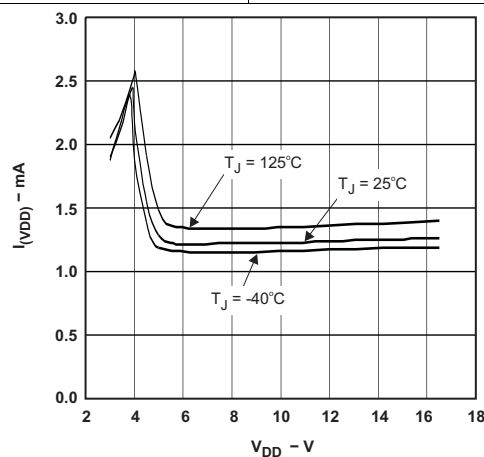Figure 4. Turnon Delay vs V_{DD} (Power Applied Until Gate is Active)

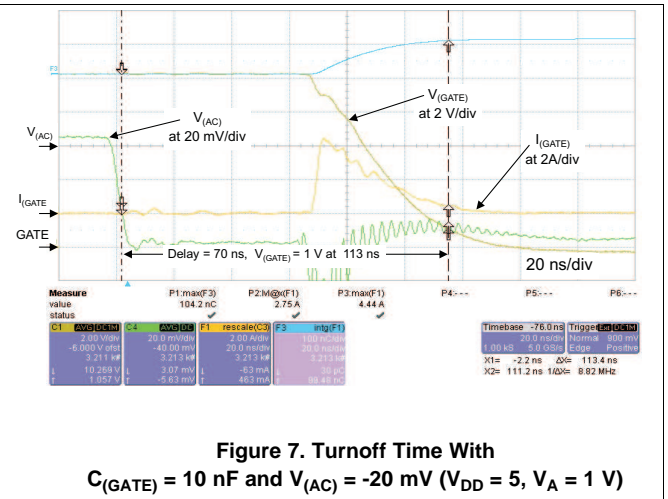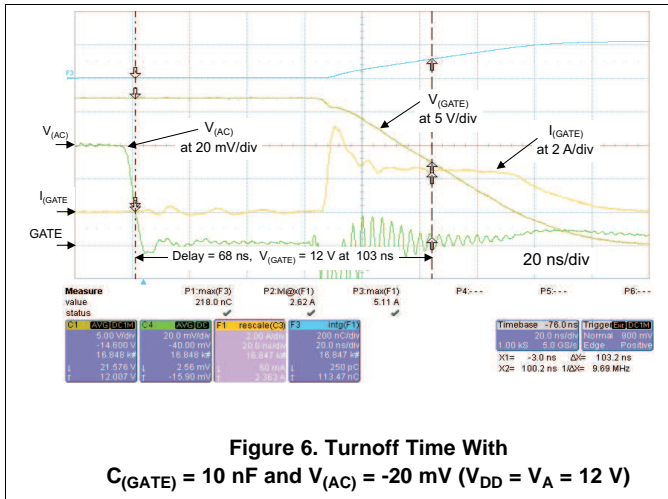Figure 5. V_{DD} Current vs V_{DD} Voltage (Gate Saturated High)

Typical Characteristics (continued)

Figure 6. Turnoff Time With
C(GATE) = 10 nF and V(AC) = -20 mV (VDD = VA = 12 V)

Figure 7. Turnoff Time With
C(GATE) = 10 nF and V(AC) = -20 mV (VDD = 5, VA = 1 V)

8 Detailed Description

8.1 Overview

The TPS2412/13 is designed to allow an output ORing in N+1 power supply applications (see Figure 9), and an input-power bus ORing in redundant source applications (see Figure 10). The TPS2412/13 and external MOSFET emulate a discrete diode to perform this unidirectional power combining function. The advantage to this emulation is lower forward voltage drop and the ability to tune the operation.

The TPS2412 turns the MOSFET on with a linear control loop that regulates $V_{(AC)}$ to 10 mV as shown in Figure 8. With the gate low, and $V_{(AC)}$ increasing to 10 mV, the amplifier drives GATE high with all available output current until regulation is reached. The regulator controls $V_{(GATE)}$ to maintain $V_{(AC)}$ at 10 mV as long as the MOSFET $r_{DS(on)} \times I_{(DRAIN)}$ is less than this the regulated voltage. The regulator drives GATE high, turning the MOSFET fully ON when the $r_{DS(on)} \times I_{(DRAIN)}$ exceeds 10 mV; otherwise, $V_{(GATE)}$ will be near $V_{(A)}$ plus the MOSFET gate threshold voltage. If the external circuits force $V_{(AC)}$ below 10 mV and above the programmed fast turnoff, GATE is slowly turned off. GATE is rapidly pulled to ground if $V_{(AC)}$ falls to the RSET programmed fast turnoff threshold.

The TPS2413 turns the MOSFET on and off like a comparator with hysteresis as shown in Figure 8. GATE is driven high when $V_{(AC)}$ exceeds 10 mV, and rapidly turned off if $V_{(AC)}$ falls to the RSET programmed fast turnoff threshold.

System designs should account for the inherent delay between a TPS2412/13 circuit becoming forward biased, and the MOSFET actually turning ON. The delay is the result of the MOSFET gate capacitance charge from ground to its threshold voltage by the 290 μA gate current. If there are no additional sources holding the ORed rail voltage up, the MOSFET internal diode will conduct and maintain voltage on the ORed output, but there will be some voltage droop. This condition is analogous to the power source being ORed in this case. The DC-DC converter output voltage droops when its load increases from zero to a high value. Load sharing techniques that keep all ORed sources active solve this condition.
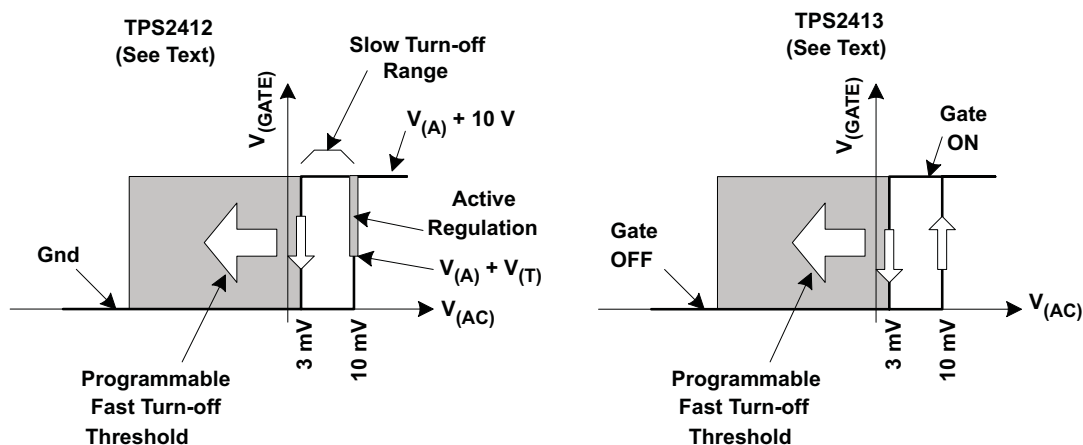
Figure 8. TPS241x Operation

The operation of the two parts is summarized in Table 1.

Table 1. Operation as a Function of V_{AC}

PART	$V_{(AC)} \leq$ TURNOFF THRESHOLD[1]	TURNOFF THRESHOLD[1] $\leq V_{AC} \leq$ 10 mV		$V_{(AC)} >$ 10 mV
		$V_{(AC)}$ FORCED < 10 mV	(MOSFET $r_{DS(on)} \times I_{LOAD}) \leq$ 10 mV	
TPS2412	Strong GATE pulldown (OFF)	Weak GATE pulldown (OFF)	$V_{(AC)}$ regulated to 10 mV	GATE pulled high (ON)
TPS2413	Strong GATE pulldown (OFF)	Depends on previous state (Hysteresis region)		GATE pulled high (ON)

(1)   Turnoff threshold is established by the value of RSET.

8.2 Functional Block Diagram
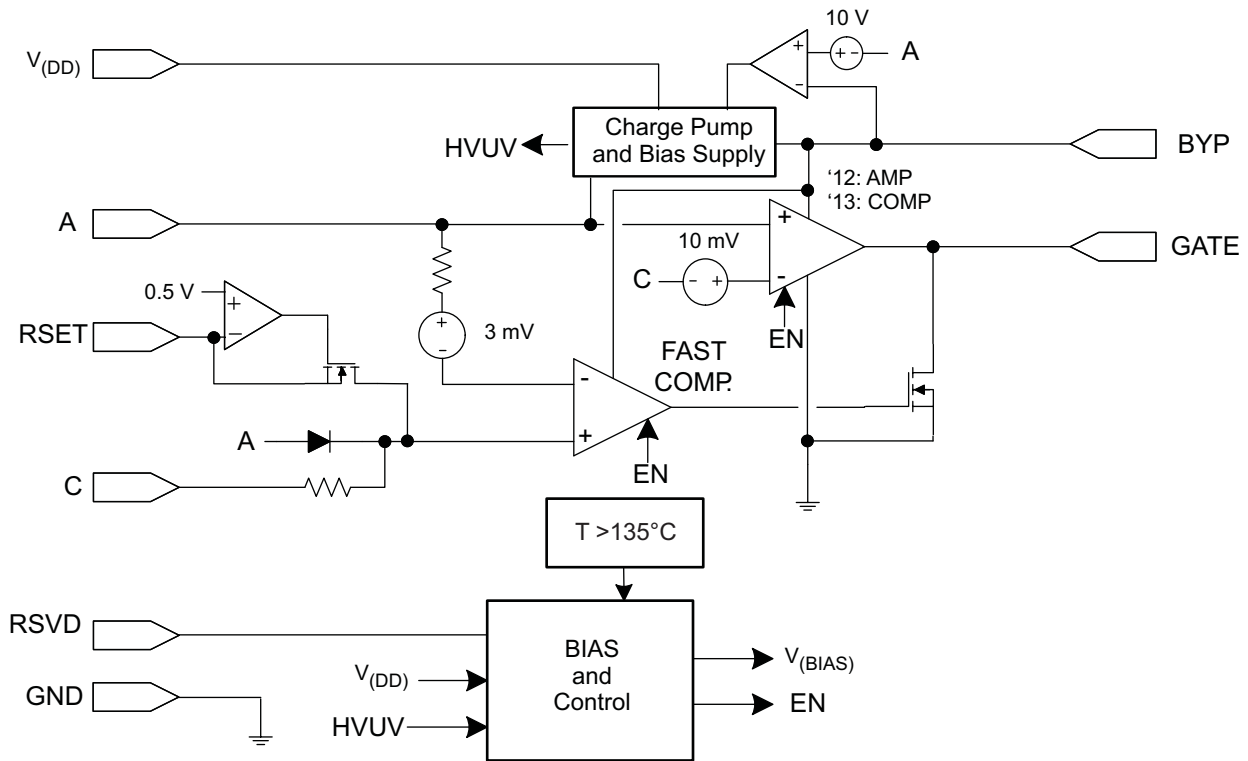
8.3 Feature Description

8.3.1 Definitions

The following descriptions refer to the pinout and the functional block diagram.

A, C: The A pin serves as the simulated diode anode and the C as the cathode. GATE is driven high when $V_{(AC)}$ exceeds 10 mV. Both devices provide a strong GATE pulldown when $V_{(AC)}$ is less than the programmable fast turnoff threshold. The TPS2412 has a soft pulldown when $V_{(AC)}$ is less than 10 mV but above the fast turnoff threshold.

Several internal comparator and amplifier circuits monitor these two pins. The inputs are protected from excess differential voltage by a clamp diode and series resistance. If C falls below A by more than about 0.7 V, a small current flows out of C. Protect the internal circuits with an external clamp if C can be more than 6 V lower than A.

The internal charge pump output, which provides bias power to the comparators and voltage to drive GATE, is referenced to A. Some charge pump current appears on A due to this topology. The A and C pins should be Kelvin connected to the MOSFET source and drain. A and C connections should also be short and low impedance, with special attention to the A connection. Residual noise from the charge pump can be reduced with a bypass capacitor at A if the application permits.

BYP: BYP is the internal charge pump output, and the positive supply voltage for internal comparator circuits and GATE driver. A capacitor must be connected from BYP to A. While the capacitor value is not critical, a 2200-pF ceramic is recommended. Traces to this part must be kept short and low impedance to provide adequate filtering.

CAUTION

Shorting this pin to a voltage below A damages the TPS241x.

Feature Description (continued)

GATE: Gate controls the external N channel MOSFET gate. GATE is driven positive with respect to A by a driver operating from the voltage on BYP. A time-limited high current discharge source pulls GATE to GND when the fast turnoff comparator is activated. The high-current discharge is followed by a sustaining pulldown. The turnoff circuits are disabled by the thermal shutdown, leaving a resistive pulldown to keep the gate from floating. The gate connection should be kept low impedance to maximize turnoff current.

GND: This is the input supply reference. GND should have a low impedance connection to the ground plane. It carries several Amperes of rapid-rising discharge current when the external MOSFET is turned off, and also carries significant charge pump currents.

RSET: A resistor connected from this pin to GND sets the fast $V_{(A-C)}$ comparator turnoff threshold. The threshold is slightly positive when the RSET pin is left open. Current drawn by the resistor programs the turnoff voltage to increasing negative values. The TPS2413 must have a negative threshold programmed to avoid an unstable condition at light load. The expression for $R_{(RSET)}$ in terms of the trip voltage, $V_{(OFF)}$, follows.

$$R_{(RSET)} = \left(\frac{-470.02}{V_{(OFF)} - 0.00314} \right)$$

(1)

The units of the numerator are (V × V/A). $V_{(OFF)}$ is positive for $V_{(A)}$ greater than $V_{(C)}$, $V_{(OFF)}$ is less than 3 mV, and $R_{(RSET)}$ is in ohms.

RSVD: Connect to ground.

V_DD: V_{DD} is the primary supply for the gate drive charge pump and other internal circuits. This pin must be connected a source that is 3 V or greater when the external MOSFET is to be turned on. V_{DD} may be greater or lower than the controlled bus voltage.

A 0.01-µF bypass capacitor, or 10-Ω and a 0.01-µF filter, is recommended because charge pump currents are drawn through V_{DD}.

8.3.2 TPS2412 vs TPS2413 – MOSFET Control Methods

The TPS2412 control method yields several benefits. First, the low-current GATE driver provides a gentle turnon and turnoff for slowly rising and falling input voltage. Second, it reduces the tendency for on/off cycling of a comparator based solution at light loads. Third, it avoids reverse currents if the fast turnoff threshold is left positive. The drawback to this method is that the MOSFET appears to have a high resistance at light load when the regulation is active. A momentary output voltage droop occurs when a large step load is applied from a light-load condition. The TPS2412 is a better solution for a mid-rail bus that is re-regulated.

The TPS2413 turns the MOSFET on if $V_{(AC)}$ is greater than 10 mV, and the rapid turnoff is activated at the programmed negative threshold. There is no linear control range and slow turnoff. The disadvantage is that the turnoff threshold must be negative (unless a minimum load is always present) permitting a continuous reverse current. Under a dynamic reverse voltage fault, the lower threshold voltage may permit a higher peak reverse current. There are a number of advantages to this control method. Step loads from a light load condition are handled without a voltage droop beyond I × R. If the redundant converter fails, applications with redundant synchronous converters may permit a small amount of reverse current at light load to assure that the MOSFET is all ready on. The TPS2413 is a better solution for low-voltage buses that are not re-regulated, and that may see large load steps transients.

These applications recommendations are meant as a starting point, with the needs of specific implementations overriding them.

8.3.3 N+1 Power Supply – Typical Connection

The N+1 power supply configuration shown in Figure 9 is used where multiple power supplies are paralleled for either higher capacity, redundancy or both. If it takes N supplies to power the load, adding an extra, identical unit in parallel permits the load to continue operation in the event that any one of the N supplies fails. The supplies are ORed together, rather than directly connected to the bus, to isolate the converter output from the bus when it is plugged-in or fails short. The TPS2412/13 with an external MOSFET emulates the function of the ORing diode.

Feature Description (continued)

It is possible for a malfunctioning converter in an ORed topology to create a bus overvoltage if the loading is less than the converter's capacity (for example, N = 1). The ORed topology shown cannot protect the bus from this condition, even if the ORing MOSFET can be turned off. One common solution is to use two MOSFETs in a back-to-back configuration to provide bidirectional blocking. The TPS2412/13 does not have a provision for forcing the gate off when the overvoltage condition occurs, use of the TPS2410/11 is recommended.

ORed supplies are usually designed to share power by various means, although the desired operation could implement an active and standby concept. Sharing approaches include both passive, or voltage droop, and active methods. Not all of the output ORing devices may be ON depending on the sharing control method, bus loading, distribution resistances, and TPS2412/13 settings.
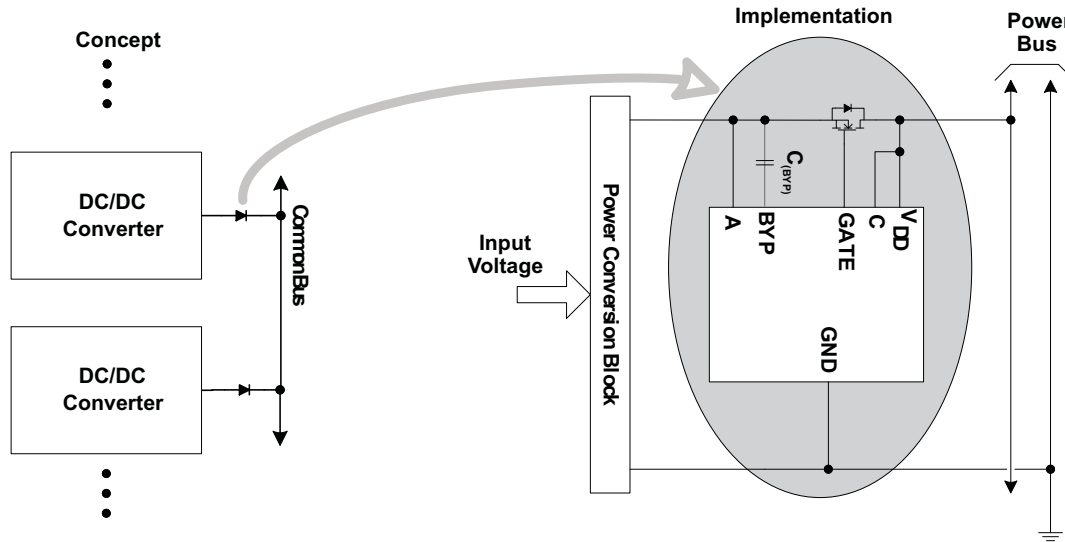

Figure 9. N+1 Power Supply Example

8.3.4 Input ORing – Typical Connection

Figure 10 shows how redundant buses may be ORed to a common point to achieve higher reliability. It is possible to have both MOSFETs ON at once if the bus voltages are matched, or the combination of tolerance and regulation causes both TPS2412/13 circuits to see a forward voltage. The ORing MOSFET disconnects the lower-voltage bus, protecting the remaining bus from potential overload by a fault.
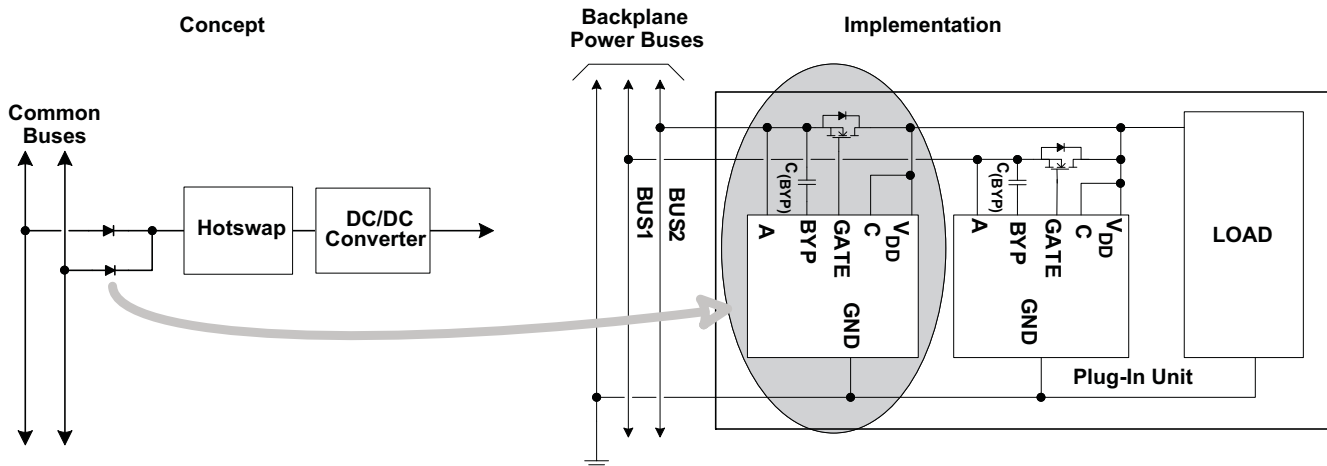

Figure 10. Example ORing of Input Power Buses

Feature Description (continued)

8.3.5 System Design and Behavior With Transients

The power system, perhaps consisting of multiple supplies, interconnections, and loads, is unique for every product. A power distribution has low impedance, and low loss, which yields high Q by its nature. While the addition of lossy capacitors helps at low frequencies, their benefit at high frequencies is compromised by parasitics. Transient events with rise times in the 10 ns range may be caused by inserting or removing units, load fluctuations, switched loads, supply fluctuations, power supply ripple, and shorts. These transients cause the distribution to ring, creating a situation where ORing controllers may trip off unnecessarily. In particular, when an ORing device turns off due to a reverse current fault, there is an abrupt interruption of the current, causing a fast ringing event. Because this ringing occurs at the same point in the topology as the other ORing controllers, they are the most likely to be effected.

The ability to operate in the presence of noise and transients is in direct conflict with the goal of precise ORing with rapid response to actual faults. A fast response reduces peak stress on devices, reduces transients, and promotes un-interrupted system operation. However, a control with small thresholds and high speed is most likely to be falsely tripped by transients that are not the result of a fault. The power distribution system should be designed to control the transient voltages seen by fast-responding devices such as ORing and hotswap devices.

While some applications may find it possible to use RSET to avoid false tripping, the TPS2410/11 provides features beyond the TPS2412/13 including fast-comparator input filtering and STAT to dynamically shift the turnoff threshold.

8.3.6 TPS2412 Regulation-Loop Stability

The TPS2412 uses an internal linear error amplifier to keep the external MOSFET from saturating at light load. This feature has the benefits of setting a turnoff above 0 V, providing a soft turnoff for slowly decaying input voltages, and helps droop-sharing redundancy at light load.

Although the control loop has been designed to accommodate a wide range of applications, there are a few guidelines to be followed to assure stability.

- Select a MOSFET $C_{(ISS)}$ of 1 nF or greater
- Use low ESR bulk capacitors on the output C terminal, typically greater than 100μF with less than 50 mΩ ESR
- Maintain some minimum operational load (for example, 10 mA or more)

Symptoms of stability issues include $V_{(AC)}$ undershoot and possible fast turnoff on large-transient recovery, and a worst-case situation where the gate continually cycles on and off. These conditions are solved by following the previous rules. Loop stability should not be confused with tripping the fast comparator due to $V_{(AC)}$ tripping the gate off.

Although not common, a condition may arise where the DC-DC converter transient response may cause the GATE to cycle on and off at light load. The converter experiences a load spike when GATE transitions from OFF to ON because the ORed bus capacitor voltage charges abruptly by as much as a diode drop. The load spike may cause the supply output to droop and overshoot, which can result in the ORed capacitor peak charging to the overshoot voltage. When the supply output settles to its regulated value, the ORed bus may be higher than the source, causing the TPS2412/13 to turn the GATE off. While this may not actually cause a problem, its occurrence may be mitigated by control of the power supply transient characteristic and increasing its output capacitance while increasing the ORed load to capacitance ratio. Adjusting the TPS2412/13 turnoff threshold to desensitize the redundant ORing device may help as well. Careful attention to layout and charge-pump noise around the TPS2412/13 helps with noise margin.

The linear gate driver has a pullup current of 290 μA and pulldown current of 3 mA typical.

8.3.7 MOSFET Selection and $R_{(RSET)}$

MOSFET selection criteria include voltage rating, voltage drop, power dissipation, size, and cost. The voltage rating consists of both the ability to withstand the rail voltage with expected transients, and the gate breakdown voltage. The MOSFET gate rating should be the minimum of 12 V, or the controlled rail voltage. Typically this requires a ±20-V GATE voltage rating.

Feature Description (continued)

While $r_{DS(on)}$ is often chosen with the power dissipation, voltage drop, size and cost in mind, there are several other factors to be concerned with in ORing applications. When using the TPS2412, the minimum voltage across the device is 10 mV. A device that would have a lower voltage drop at full-load would be overspecified. When using a TPS2413 or TPS2412 with RSET programmed to a negative voltage, the permitted static reverse current is equal to the turnoff threshold divided by the $r_{DS(on)}$. While this current may actually be desirable in some systems, the amount may be controlled by selection of $r_{DS(on)}$ and RSET. The practical range of $r_{DS(on)}$ for a single MOSFET runs from the low milliohms to 40 mΩ for a single MOSFET.

MOSFETs may be paralleled for lower voltage drop (power loss) at high current. For TPS2412 operation, one should plan for only one of the MOSFETs to carry current until the 10 mV regulation point is exceeded and the loop forces GATE fully ON. TPS2413 operation does not rely on linear range operation, so the MOSFETs are all ON or OFF together except for short transitional times. Beyond the control issues, current sharing depends on the resistance match including both the $r_{DS(on)}$ and the connection resistance.

The TPS2412 may be used without a resistor on RSET. In this case, the turnoff $V_{(AC)}$ threshold is about 3 mV. The TPS2413 may only be operated without an RSET programming resistor if the loading provides a higher $V_{(AC)}$. A larger negative turnoff threshold reduces sensitivity to false tripping due to noise on the bus, but permits larger static reverse current. Installing a resistor from RSET to ground creates a negative shift in the fast turnoff threshold per Equation 2.

$$R_{(RSET)} = \left(\frac{-470.02}{V_{(OFF)} - 0.00314} \right)$$
(2)

To obtain a −10 mV fast turnoff ($V_{(A)}$ is less than $V_{(C)}$ by 10 mV), $R_{(RSET)}$ = (−470.02/ (−0.01−0.00314)) ≈ 35,700Ω. If a 10 mΩ $r_{DS(on)}$ MOSFET was used, the reverse turnoff current would be calculated using Equation 3.

$$I_{(TURN\_OFF)} = \frac{V_{(THRESHOLD)}}{r_{DS(on)}}$$

$$I_{(TURN\_OFF)} = \frac{-10 \text{ mV}}{10 \text{ mΩ}}$$

$$I_{(TURN\_OFF)} = -1 \text{ A}$$
(3)

The sign indicates that the current is reverse, or flows from the MOSFET drain to source (C to A).

The turnoff speed of a MOSFET is influenced by the effective gate-source and gate-drain capacitance C_{ISS}). Because these capacitances vary a great deal between different vendor parts and technologies, they should be considered when selecting a MOSFET where the fastest turnoff is desired.

8.3.8 Gate Drive, Charge Pump and C(BYP)

Gate drive of 270 μA typical is generated by an internal charge pump and current limiter. A separate supply, V_{DD}, is provided to avoid having the large charge pump currents interfere with voltage sensing by the A and C pins. The GATE drive voltage is referenced to $V_{(A)}$ as GATE will only be driven high when $V_{(A)} > V_{(C)}$. The recommended capacitor on BYP (bypass) must be used to form a quiet supply for the internal high-speed comparator. $V_{(GATE)}$ must not exceed $V_{(BYP)}$.

8.4 Device Functional Modes

TPS2412 regulates MOSFET $V_{(AC)}$ to 10 mV linearly while TPS2413 operates in a comparator like manner. Both devices have a programmable ON/OFF threshold.

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2412 and TPS2413 are designed to allow output ORing in N+1 power supply applications and input-power bus ORing in redundant source applications. The external MOSFET in conjunction with the TPS2412/13 emulate a discrete diode to perform this unidirectional power combining function.

9.2 Typical Application

Applications with the TPS2412/13 are not limited to ORing of identical sections. The TPS2412/13 and external MOSFET form a general purpose function block. Figure 11 shows a circuit with ORing between a discrete diode and a TPS2412/MOSFET section. This circuit can be used to combine two different voltages in cases where the output is regulated, and the additional voltage drop in the Input 1 path is not a concern. An example is ORing of an AC adapter on Input 1 with a lower voltage on Input 2.
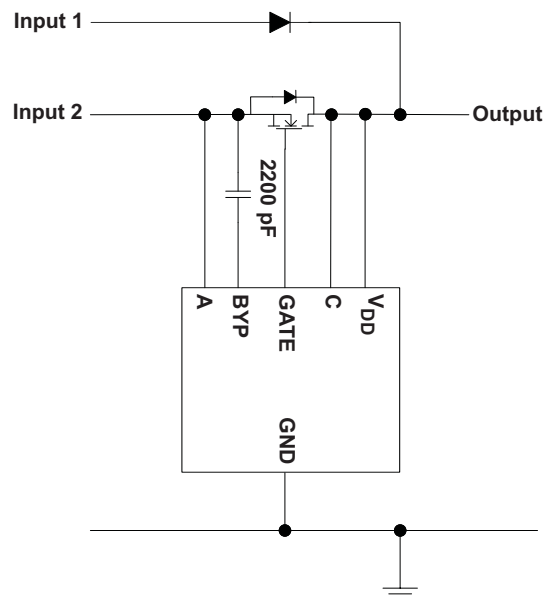

Figure 11. ORing Circuit

The TPS2412 may be a better choice in applications where inputs may be removed, causing an open-circuit input. If the MOSFET was ON when the input is removed, V_{AC} will be virtually zero. If the reverse turnoff threshold is programmed negative, the TPS2412/13 will not pull GATE low. A system interruption could then be created if a short is applied to the floating input. For example, if an AC adapter is first connected to the unit, and then connected to the AC mains, the adapter's output capacitors will look like a momentary short to the unit. A TPS2412 with RSET open will turn the MOSFET OFF when the input goes open circuit.

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V
Output voltage	12 V
Load current	5 A

9.2.2 Detailed Design Procedure

The following is a summarized design procedure:

1. Choose between the TPS2412 or 2413, see TPS2412 vs TPS2413 – MOSFET Control Methods.
2. Choose the V_{DD} source. Table 3 provides a guide for where to connect V_{DD} that covers most cases. V_{DD} may be directly connected to the supply, but an $R_{(VDD)}$ and $C_{(VDD)}$ of 10 Ω and 0.01 µF is recommended.

Table 3. V_{DD} Connection Guide

$V_A < 3$ V	3 V $\leq V_A \leq 3.6$ V	$V_A > 3.6$ V
Bias Supply > 3 V	V_A or Bias Supply > 3 V. V_C if always > 3 V	V_C, V_A, or Bias for special configurations

3. Noise voltage and impedance at the A pin should be kept low. $C_{(A)}$ may be required if there is noise on the bus, or A is not low impedance. If either of these is a concern, a $C_{(A)}$ of 0.01 µF or more may be required.
4. Select $C_{(BYP)}$ as 2200 pF, X7R, 25-V or 50-V ceramic capacitor.
5. Select the MOSFET based on considerations of voltage drop, power dissipated, voltage ratings, and gate capacitance. See sections: MOSFET Selection and RSET and TPS2412 Regulation-Loop Stability.
6. Select $R_{(RSET)}$ based on which MOSFET was chosen and reverse current considerations – see MOSFET Selection and RSET. If the noise and transient environment is not well known, make provision for $R_{(RSET)}$ even when using the TPS2412.
7. Make sure to connect RSVD to ground.
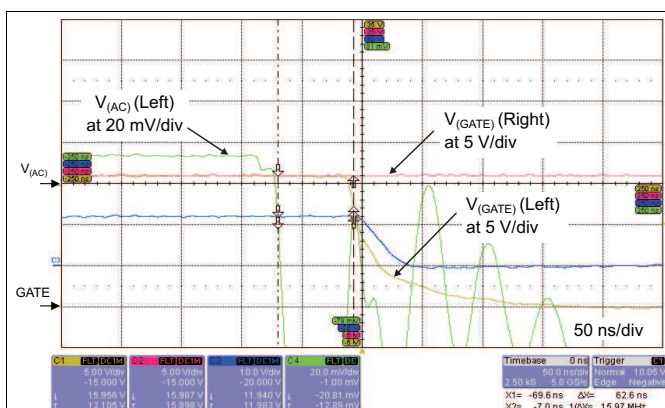
9.2.3 Application Curves

Figure 12. Typical Turnoff With Two ORED Devices Active (V_{DD} = 12 V, $I_{(LOAD)}$ = 5 A, IRL3713, Transient Applied to Left Side)
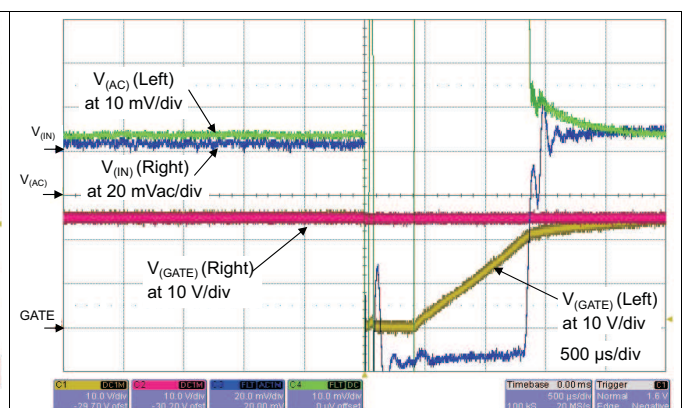

Figure 13. Typical Turnoff And Recovery With Two ORED Devices Active (V_{DD} = 3 V, V_A = 18 V, $I_{(LOAD)}$ = 5 A, IRL3713, Transient Applied to Left Side)

10 Power Supply Recommendations

10.1 Recommended Operating Range

The maximum recommended bus voltage is lower than the absolute maximum voltage ratings on A, C, and V_{DD} solely to provide some margin for transients on the bus. Most power systems experience transient voltages above the normal operating level. Short transients, or voltage spikes, may be clamped by the ORing MOSFET to an output capacitor and/or voltage rail depending on the system design. Transient protection, for example, a TVS diode (transient voltage suppressor, a type of Zener diode), may be required on the input or output if the system design does not inherently limit transient voltages below the TPS2412/13 absolute maximum ratings. If a TVS is required, it must protect to the absolute maximum ratings at the worst case clamping current. The TPS2412/13 will operate properly up to the absolute maximum voltage ratings on A, C, and V_{DD}.

10.2 V_{DD}, BYP, and Powering Options

The separate V_{DD} pin provides flexibility for operational power and controlled rail voltage. While the internal UVLO has been set to 2.5 V, the TPS2412/13 requires at least 3 V to generate the specified GATE drive voltage. Sufficient BYP voltage to run internal circuits occurs at V_{DD} voltages from 2.5 V to 3 V. There are three choices for power, A, C, or a separate supply, two of which are demonstrated in Figure 14. One choice for voltage rails over 3.3 V is to power from C, because it is typically the source of reliable power. Voltage rails below 3.3 V nominal, for example, 2.5 V and below, should use a separate supply such as 5 V. A separate V_{DD} supply can be used to control voltages above it, for example 5 V powering V_{DD} to control a 12-V bus.

V_{DD} is the main source of power for the internal control circuits. The charge pump that powers BYP draws most of its power from V_{DD}. The input should be low impedance, making a bypass capacitor a preferred solution. A 10-Ω series resistor may be used to limit inrush current into the bypass capacitor, and to provide noise filtering for the supply.

BYP is the interconnection point between a charge pump, $V_{(AC)}$ monitor amplifiers and comparators, and the gate driver. $C_{(BYP)}$ must be used to filter the charge pump. A 2200 pF is recommended, but the value is not critical.
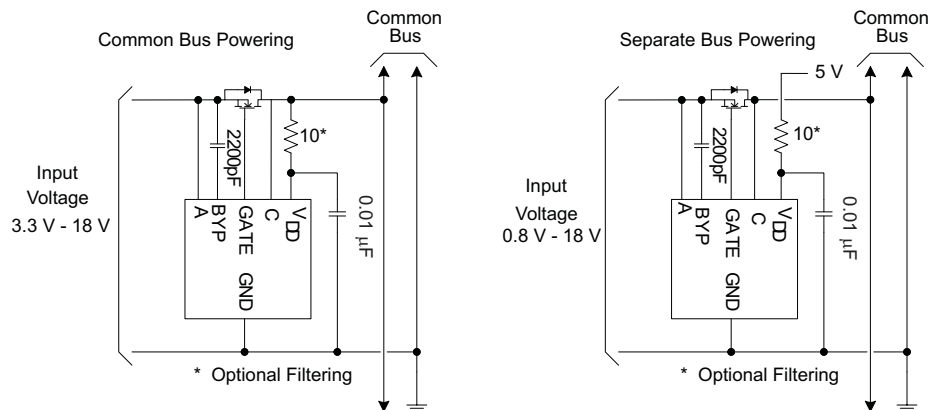

Figure 14. V_{DD} Powering Examples

11 Layout

11.1 Layout Guidelines

1. The TPS2412/13, MOSFET, and associated components should be used over a ground plane.
2. The GND connection should be short, with multiple vias to ground.
3. $C_{(VDD)}$ should be adjacent to the V_{DD} pin with a minimal ground connection length to the plane.
4. The GATE connection should be short and wide (for example, 0.025" minimum).
5. The C pin should be Kelvin connected to the MOSFET.
6. The A pin should be a short, wide, Kelvin connection to the MOSFET.
7. $R_{(SET)}$ should be kept immediately adjacent to the TPS2412/13 with short leads.
8. $C_{(BYP)}$ should be kept immediately adjacent to the TPS2412/13 with short leads.
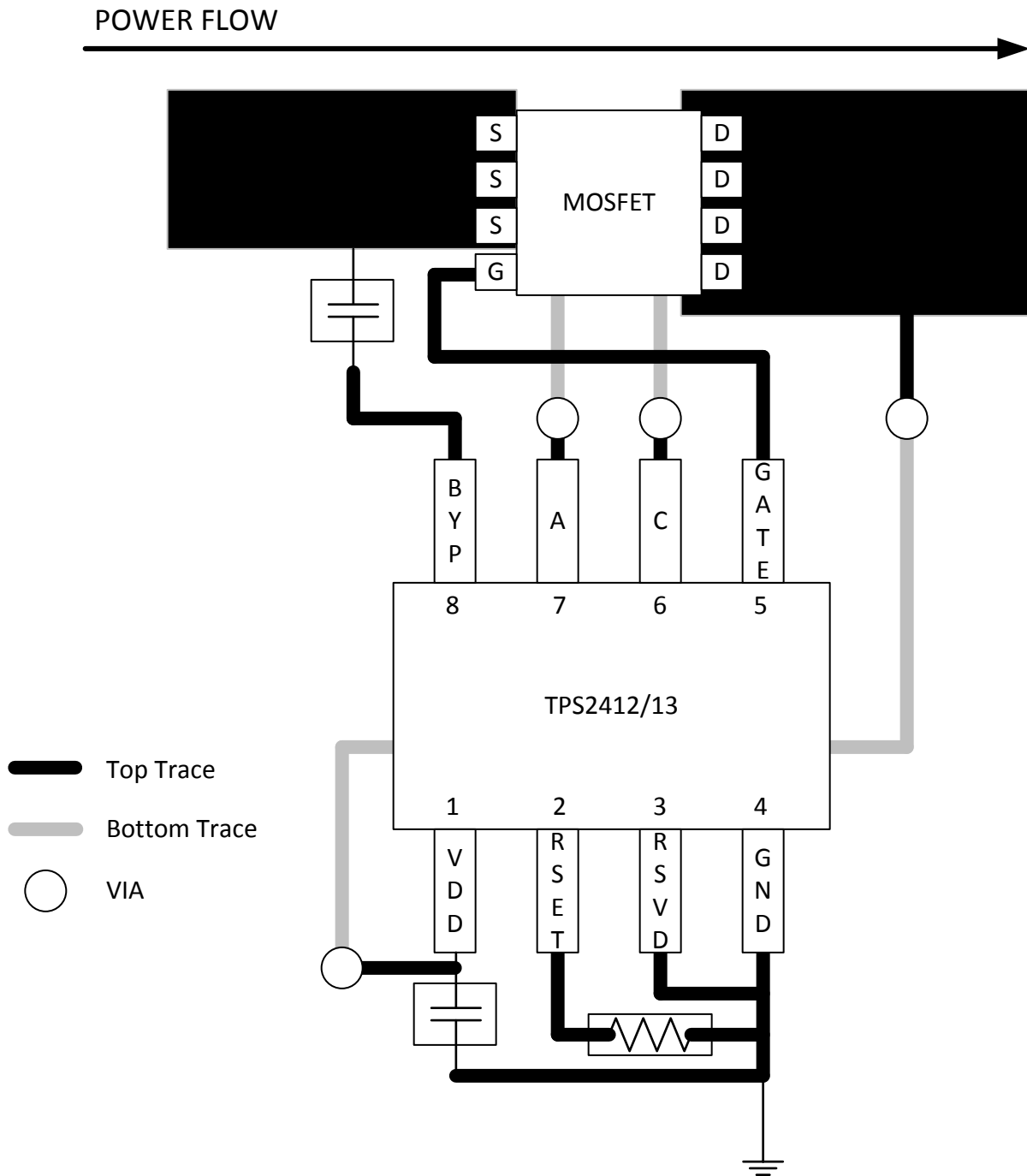
11.2 Layout Example

Figure 15. Layout Recommendation

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **4.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
TPS2412	单击此处	单击此处	单击此处	单击此处	单击此处
TPS2413	单击此处	单击此处	单击此处	单击此处	单击此处

12.2 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 **Glossary**

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

.228-.244   TYP
[5.80-6.19]

A

PIN 1 ID AREA

1

8

6X .050
[1.27]

2X

.150
[3.81]

.189-.197
[4.81-5.00]
NOTE 3

4

5

B

.150-.157
[3.81-3.98]
NOTE 4

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25] Ⓜ C A B

C

SEATING PLANE

⌒ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010   TYP
[0.13-0.25]

.010
[0.25]

0°- 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C   02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

SYMM

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM

(R.002) TYP
[0.05]

4

5

6X (.050)
[1.27]

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

SYMM

1

8X (.024)
[0.6]

SYMM

8

(R.002) TYP
[0.05]

5

6X (.050)
[1.27]

4

(.213)
[5.4]

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

6.6 / 6.2 TYP

PIN 1 ID AREA

1

3.1 / 2.9 NOTE 3

4

A

B

4.5 / 4.3 NOTE 4

8

5

6X 0.65

2X 1.95

8X 0.30 / 0.19

$\oplus$ | 0.1 Ⓜ | C | AⓈ | BⓈ

C

SEATING PLANE

◯ | 0.1 | C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0° - 8°

0.75 / 0.50

0.15 / 0.05

DETAIL A
TYPICAL

4221848/A   02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

TEXAS INSTRUMENTS
www.ti.com

8X (0.45)

8X (1.5)

SYMM

(R0.05)
TYP

1

8

SYMM

6X (0.65)

4

5

(5.8)

LAND PATTERN EXAMPLE
SCALE:10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A   02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A   02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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