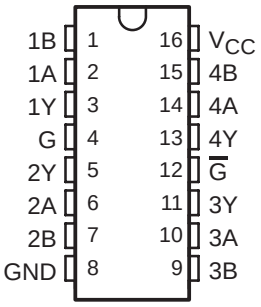
- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and ITU Recommendations V.10 and V.11.**
- **Designed to Operate With Pulse Durations as Short as 20 ns**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Input Sensitivity . . . ±200 mV**
- **Low-Power Consumption . . . 20 mA Max**
- **Open-Circuit Fail-Safe Design**
- **Pin Compatible With SN75173 and AM26LS32**

D OR N PACKAGE
(TOP VIEW)



description

The SN65LBC173 and SN75LBC173 are monolithic quadruple differential line receivers with 3-state outputs. Both are designed to meet the requirements of the ANSI standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and ITU Recommendations V.10 and V.11. The devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low.

Each receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of 12 V to −7 V. Fail-safe design ensures that if the inputs are open circuited, the output is always high. Both devices are designed using the Texas Instruments proprietary LinBiCMOS™ technology that provides low power consumption, high switching speeds, and robustness.

These devices offer optimum performance when used with the SN75LBC172 or SN75LBC174 quadruple line drivers. The SN65LBC173 and SN75LBC173 are available in the 16-pin DIP (N) and SOIC (D) packages.

The SN65LBC173 is characterized over the industrial temperature range of −40°C to 85°C. The SN75LBC173 is characterized for operation over the commercial temperature range of 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A−B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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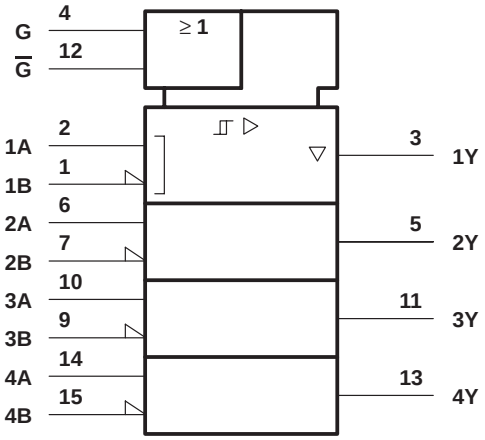
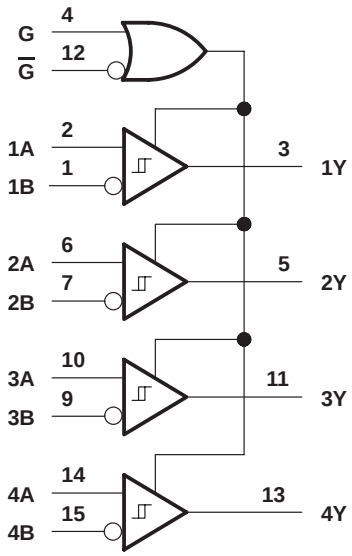
logic symbol†

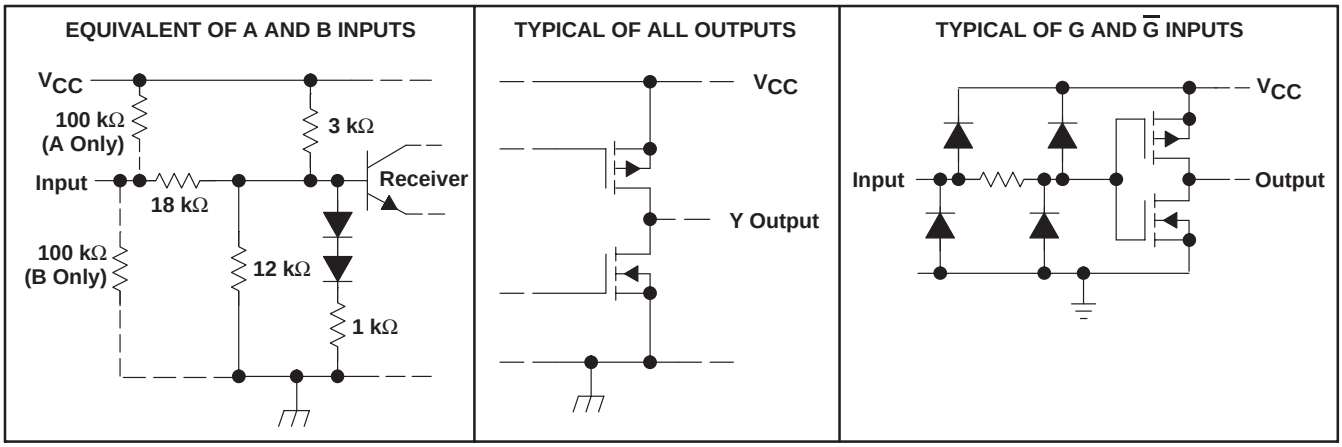


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Input voltage, V_I (A or B inputs) . . . . . ±25 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±25 V
Voltage range at Y, G, $\overline{G}$ . . . . . −0.3 V to V_{CC} + 0.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65LBC173 . . . . . −40°C to 85°C
SN75LBC173 . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	1100 mW	8.7 mW/°C	708 mW	578 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		−7		12	V
Differential input voltage, V_{ID}				±6	V
High-level input voltage, V_{IH}	G inputs	2			V
Low-level input voltage, V_{IL}	G inputs			0.8	V
High-level output current, I_{OH}				−8	mA
Low-level output current, I_{OL}				8	mA
Operating free-air temperature, T_A	SN65LBC173	−40		85	°C
	SN75LBC173	0		70	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = −8 mA					0.2	V
V_{IT-}	Negative-going input threshold voltage		I_O = 8 mA			−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)						45		mV
V_{IK}	Enable input clamp voltage		I_I = −18 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −8 mA		3.5	4.5		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 8 mA			0.3	0.5	V
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}					±20	µA
I_I	Bus input current	A or B inputs	V_{IH} = 12 V,	V_{CC} = 5 V,	Other inputs at 0 V		0.7	1	mA
			V_{IH} = 12 V,	V_{CC} = 0 V,	Other inputs at 0 V		0.8	1	
			V_{IH} = −7 V,	V_{CC} = 5 V,	Other inputs at 0 V		−0.5	−0.8	
			V_{IH} = −7 V,	V_{CC} = 0 V,	Other inputs at 0 V		−0.4	−0.8	
I_{IH}	High-level input current		V_{IH} = 5 V					±20	µA
I_{IL}	Low-level input current		V_{IL} = 0 V					−20	µA
I_{OS}	Short-circuit output current		V_O = 0				−80	−120	mA
I_{CC}	Supply current		Outputs enabled,	I_O = 0,	V_{ID} = 5 V		11	20	mA
			Outputs disabled				0.9	1.4	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V,	See Figure 1	11	22	30	ns
t_{PLH}	Propagation delay time, low- to high-level output			11	22	30	ns
t_{PZH}	Output enable time to high level	See Figure 2			17	30	ns
t_{PZL}	Output enable time to low level	See Figure 3			18	30	ns
t_{PHZ}	Output disable time from high level	See Figure 2			35	45	ns
t_{PLZ}	Output disable time from low level	See Figure 3			25	40	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	See Figure 2			0.5	6	ns
t_t	Transition time	See Figure 1			5	10	ns

PARAMETER MEASUREMENT INFORMATION

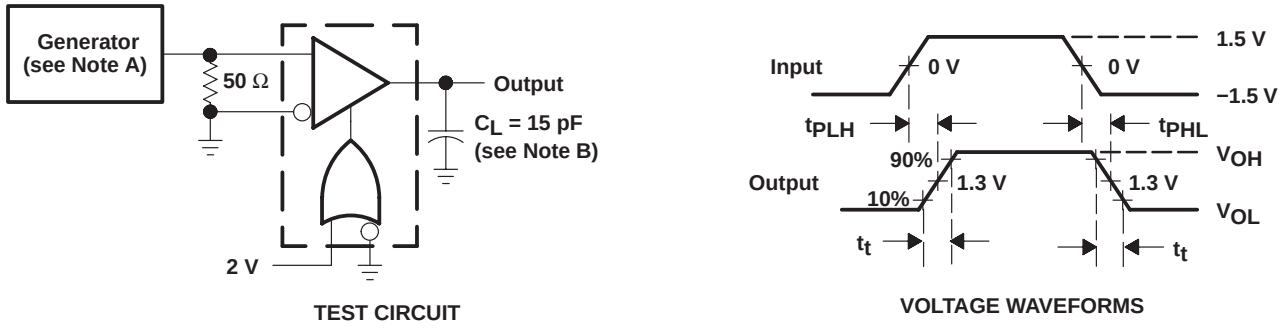


Figure 1. t_{pd} and t_t Test Circuit and Voltage Waveforms

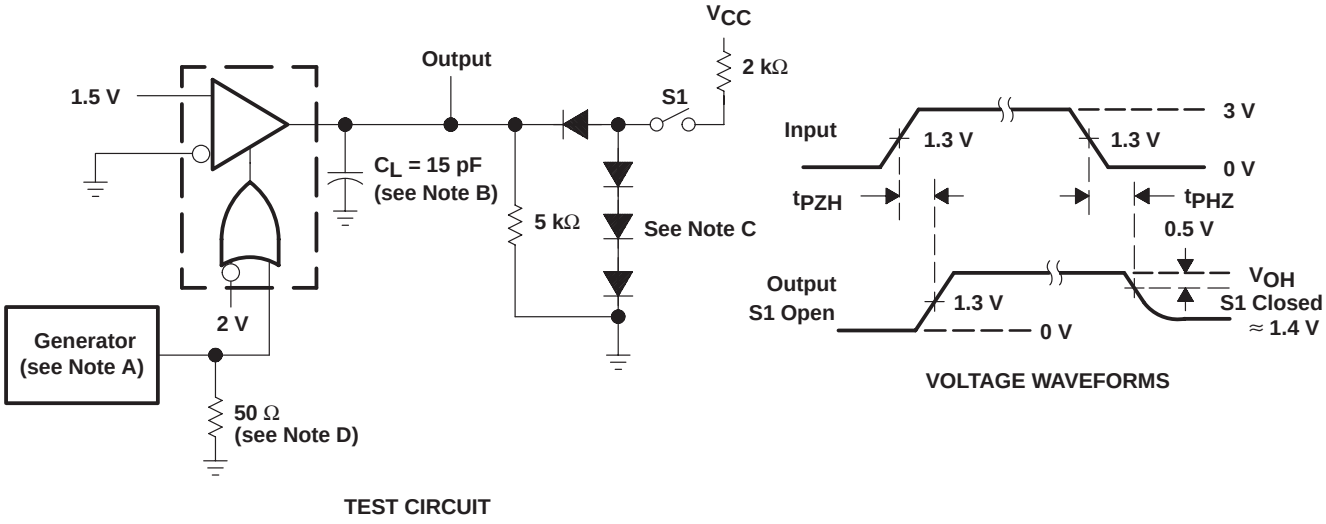
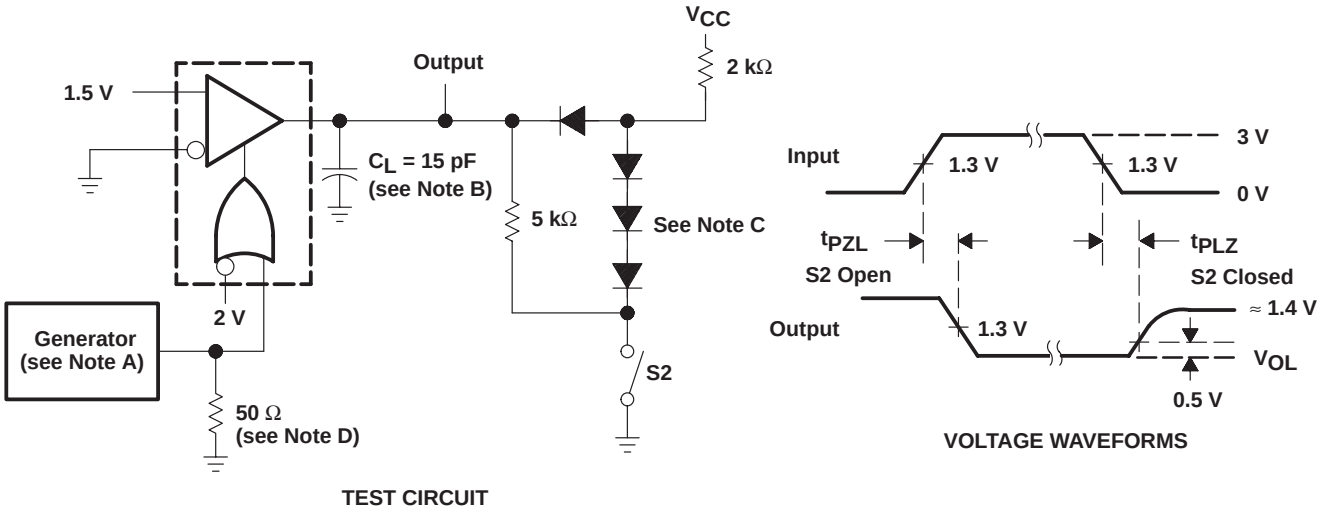


Figure 2. t_{PHZ} and t_{PZH} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

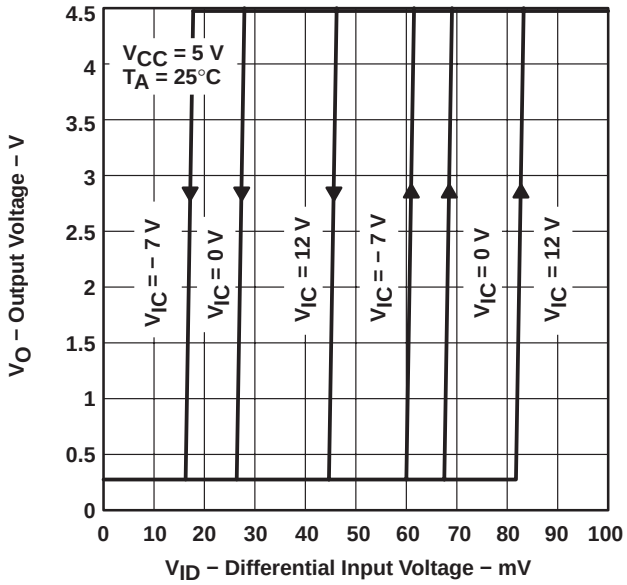


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

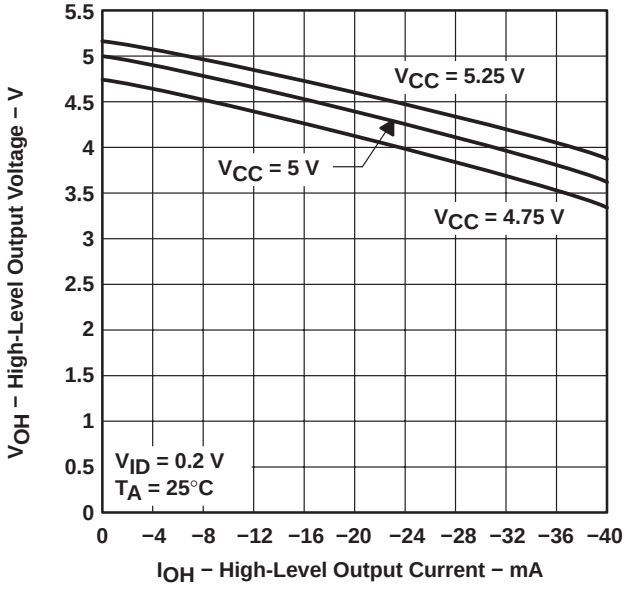


Figure 5

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

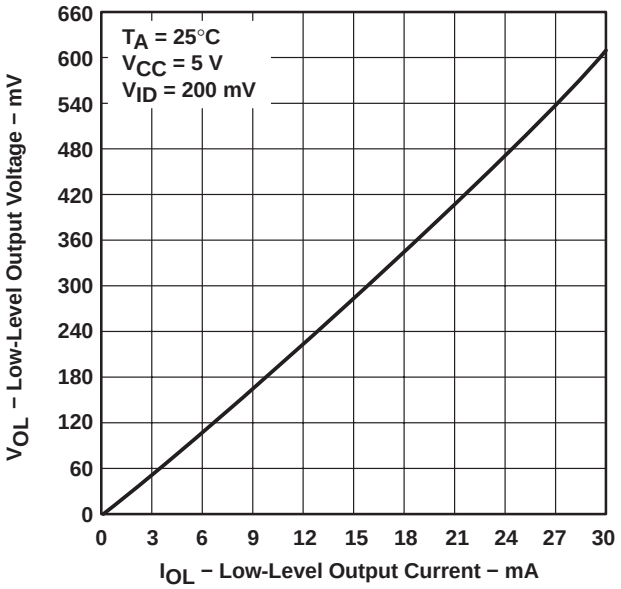


Figure 6

AVERAGE SUPPLY CURRENT vs FREQUENCY

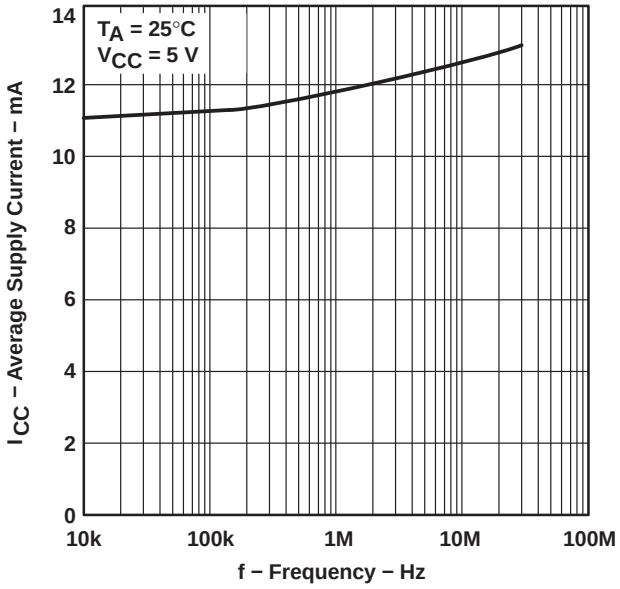


Figure 7

BUS INPUT CURRENT vs INPUT VOLTAGE (COMPLEMENTARY INPUT AT 0 V)

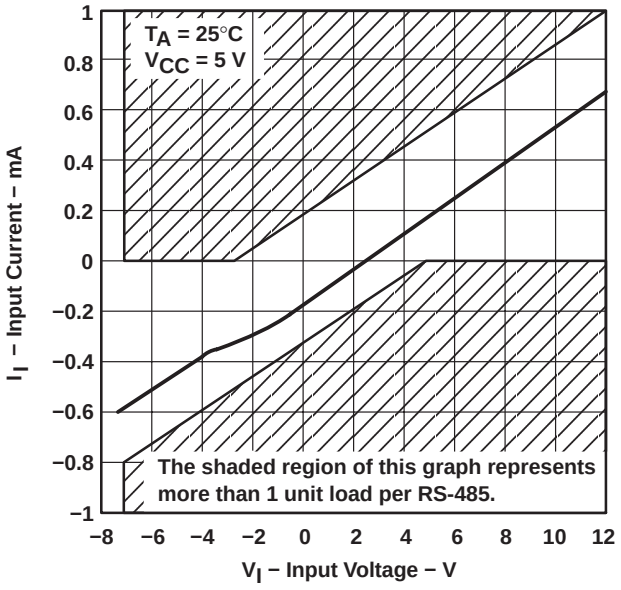


Figure 8

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

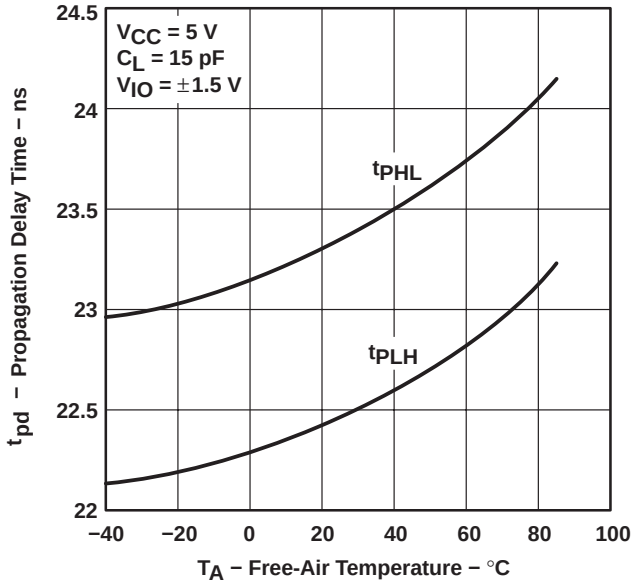
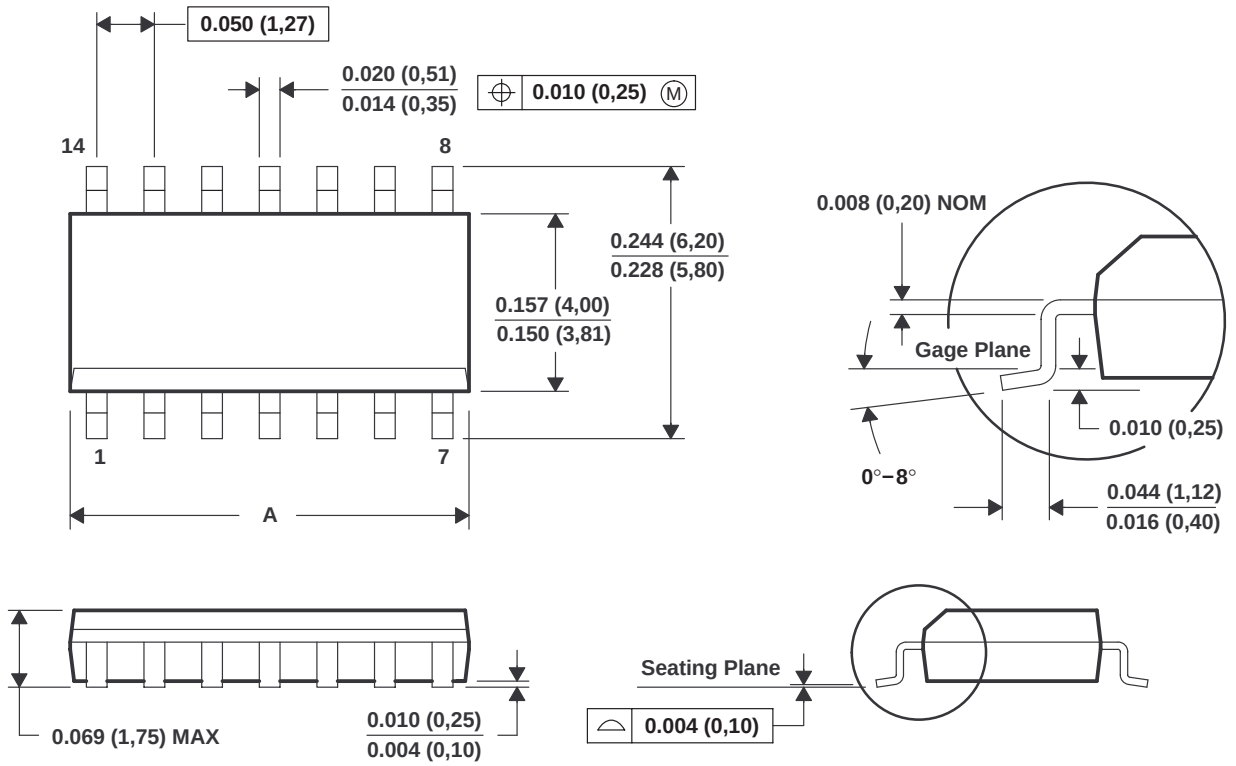


Figure 9

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

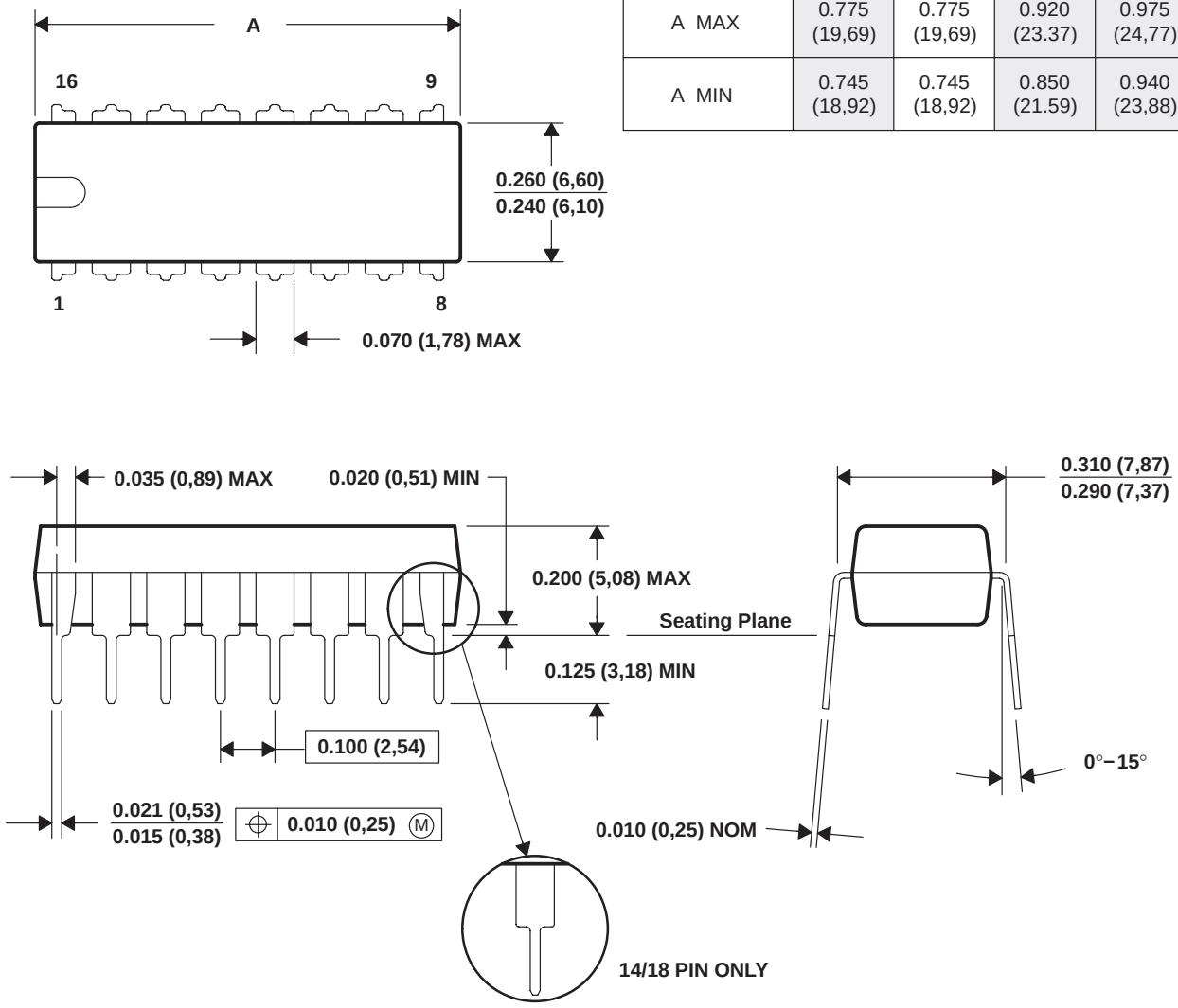
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC173D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC173	Samples
SN65LBC173DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC173	Samples
SN65LBC173N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65LBC173N	Samples
SN75LBC173D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC173	Samples
SN75LBC173DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC173	Samples
SN75LBC173N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC173N	Samples
SN75LBC173NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC173N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN75LBC173 :

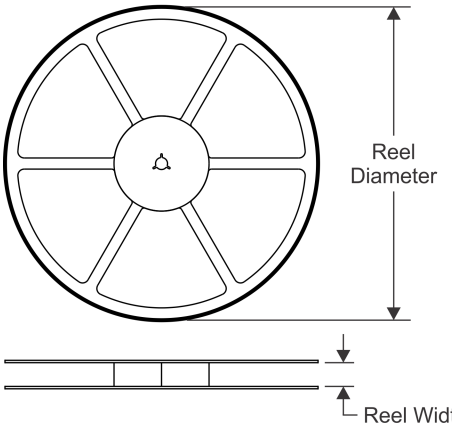
- Military : SN55LBC173

NOTE: Qualified Version Definitions:

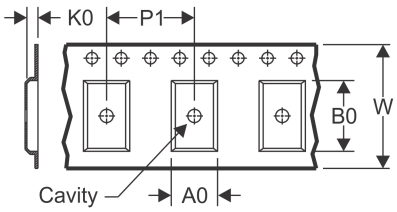
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

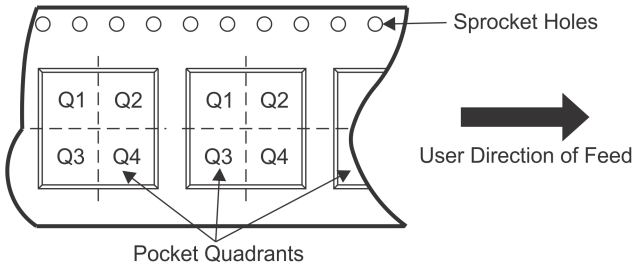


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

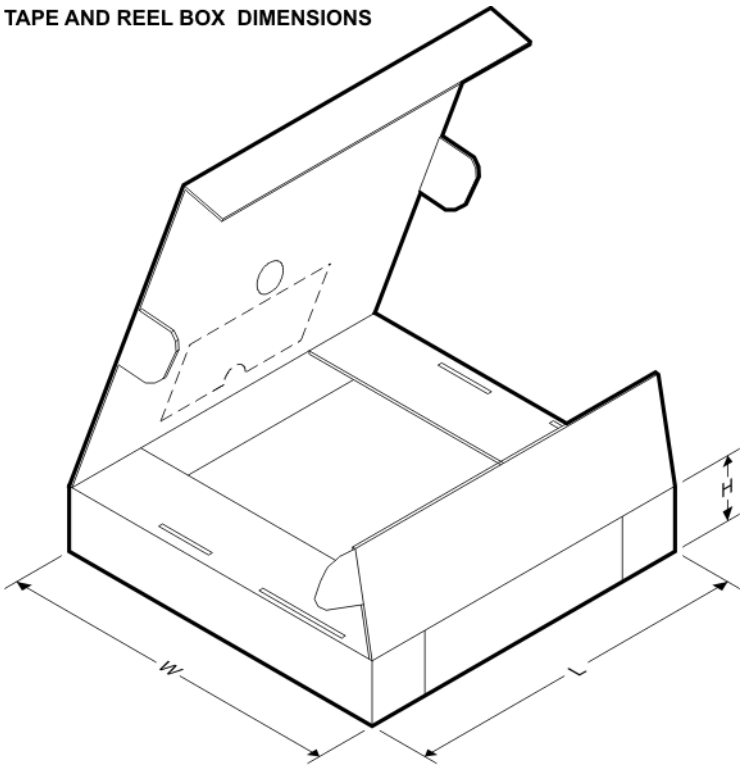
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC173DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75LBC173DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

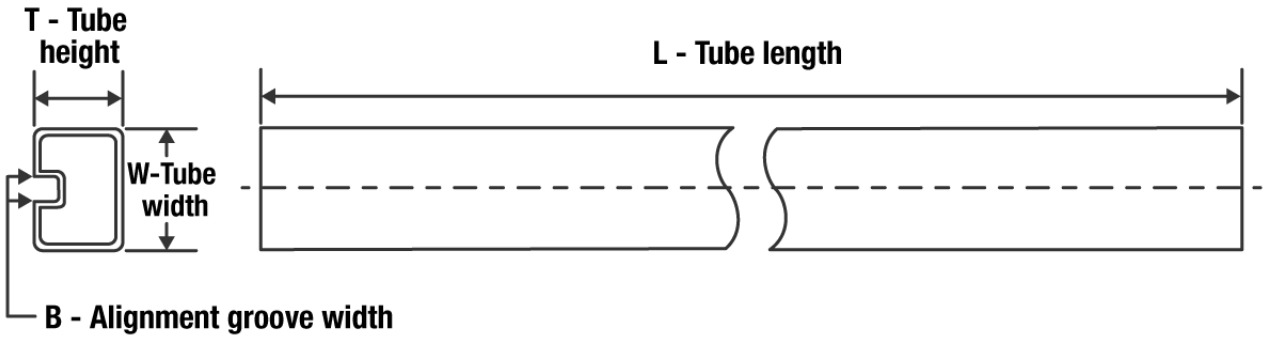
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC173DR	SOIC	D	16	2500	340.5	336.1	32.0
SN75LBC173DR	SOIC	D	16	2500	340.5	336.1	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC173D	D	SOIC	16	40	507	8	3940	4.32
SN65LBC173D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LBC173N	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC173D	D	SOIC	16	40	507	8	3940	4.32
SN75LBC173D	D	SOIC	16	40	505.46	6.76	3810	4
SN75LBC173N	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC173NE4	N	PDIP	16	25	506	13.97	11230	4.32

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