TS3A5017 双 SP4T 模拟开关/多路复用器/多路信号分离器

1 特性

- 在断电模式中提供了隔离，V_+ = 0
- 低导通状态电阻
- 低电荷注入
- 出色的通态电阻匹配
- 低总谐波失真 (THD)
- 2.3V 至 3.6V 单电源运行
- 锁断性能超过 100mA（符合 JESD 78，II 类规范的要求）
- 静电放电 (ESD) 性能测试符合 JESD 22 标准
  - 1500V 人体放电模型（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

2 应用

- 采样和保持电路
- 电池供电类设备
- 音频和视频信号路由
- 通信电路

3 说明

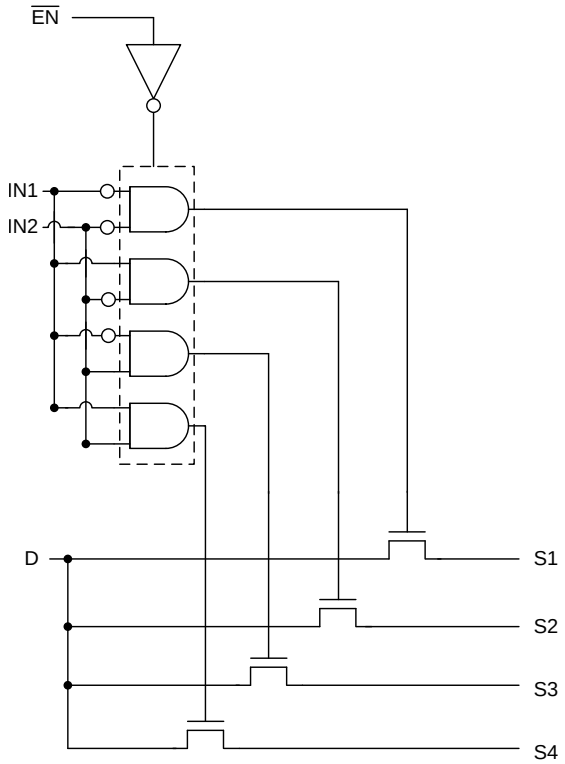
TS3A5017 器件是一款双通道单刀四掷 (4:1) 模拟开关，其设计工作电压为 2.3V 至 3.6V。此器件可以处理数字和模拟信号，并且高达 V_+ 的信号可在任一方向上传输。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS3A5017	SOIC (16)	9.90mm × 3.90mm
	SSOP (16)	4.90mm × 3.90mm
	TSSOP (16)	5.00mm × 4.40mm
	TVSOP (16)	4.40mm × 3.60mm
	UQFN (16)	2.50mm × 1.80mm
	VQFN (16)	4.00mm × 3.50mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

方框图



目录

4 修订历史记录

Changes from Revision F (October 2018) to Revision G **Page**

- 将*特性* 从“2000V 人体放电模型”更改为“1500V 人体放电模型” ... 1
- Changed the HBM value From: ±2000 V To: ±1500 V in the *ESD Ratings* ... 4

Changes from Revision E (April 2015) to Revision F **Page**

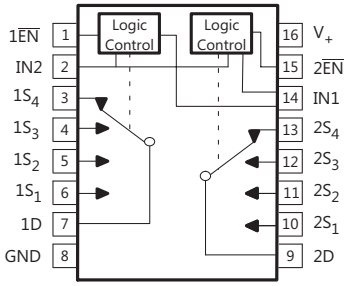
- Changed the X_{TALK} MAX value From:–49 dB To – 69 dB in the *Electrical Characteristics for 3.3-V Supply* ... 6

Changes from Revision D (December 2008) to Revision E **Page**

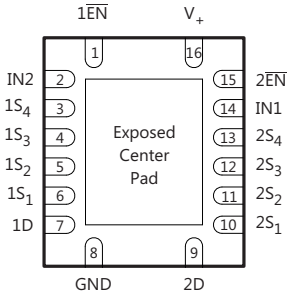
- 添加了*应用*、*器件信息* 表、*引脚功能* 表、*ESD 额定值* 表、*热性能信息* 表、*典型特性*、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1
- 已删除 *订购信息* 表。 ... 1

5 Pin Configuration and Functions

D, DBQ, DGV, and PW Package
16-Pin SOIC, SSOP, TVSOP and TSSOP
(Top View)

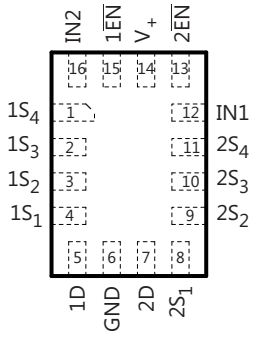


RGY Package
16-Pin VQFN
(Top View)



If exposed center pad is used, it must be connected as a secondary ground or left electrically open.

RSV Package
16-Pin UQFN
(Top View)



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC, SSOP, TVSOP, TSSOP, VQFN NO.	UQFN NO.		
1D	7	5	I/O	Common path for switch 1
1$\overline{EN}$	1	15	I	Active-low enable for switch 1
1S1	6	4	I/O	Switch 1 channel 1
1S2	5	3	I/O	Switch 1 channel 2
1S3	4	2	I/O	Switch 1 channel 3
1S4	3	1	I/O	Switch 1 channel 4
2D	9	7	I/O	Common path for switch 2
2$\overline{EN}$	15	13	I	Active-low enable for switch 2
2S1	10	8	I/O	Switch 2 channel 1
2S2	11	9	I/O	Switch 2 channel 2
2S3	12	10	I/O	Switch 2 channel 3
2S4	13	11	I/O	Switch 2 channel 4
GND	8	6	–	Ground
IN1	14	12	I	Switch 1 input select
IN2	2	16	I	Switch 2 input select
V+	16	14	–	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_+	Supply voltage(3)		–0.5	4.6	V
V_S, V_D	Analog voltage(3)(4)		–0.5	4.6	V
I_{SK}, I_{DK}	Analog port clamp current	V_S, V_D < 0	–50		mA
I_S, I_D	ON-state switch current	V_S, V_D = 0 to 7 V	–128	128	mA
V_I	Digital input voltage		–0.5	4.6	V
I_{IK}	Digital input clamp current(3)(4)	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage range	0	3.6	V
V+	Supply voltage range	2.3	3.6	V
V_I	Control input voltage range	0	3.6	V
T_A	Operating Temperature Range	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TS3A5018						UNIT
		D (SOIC)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	RSV (UQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	82	120	108	91.6	184	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 3.3-V Supply

V_+ = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_D, V_S	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	$0 \le V_S \le V_+$, I_D = –32 mA,	Switch ON, see Figure 12	25°C	3 V		11	12	Ω
				Full				14	
Δr_{on}	ON-state resistance match between channels	V_S = 2.1 V, I_D = –32 mA,	Switch ON, see Figure 12	25°C	3 V		1	2	Ω
				Full				3	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_S \le V_+$, I_D = –32 mA,	Switch ON, see Figure 12	25°C	3 V		7	9	Ω
				Full				10	
$I_{S(OFF)}$	S OFF leakage current	V_S = 1 V, V_D = 3 V, or V_S = 3 V, V_D = 1 V,	Switch OFF, see Figure 13	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
$I_{SPWR(OFF)}$		V_S = 0 to 3.6 V, V_D = 3.6 V to 0,		25°C	0 V	–1	0.5	1	
				Full		–5		5	
$I_{D(OFF)}$	D OFF leakage current	V_S = 1 V, V_D = 3 V, or V_S = 3 V, V_D = 1 V,	Switch OFF, see Figure 13	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
$I_{DPWR(OFF)}$		V_D = 0 to 3.6 V, V_S = 3.6 V to 0,		25°C	0 V	–1	0.5	1	
				Full		–5		5	
$I_{S(ON)}$	S ON leakage current	V_S = 1 V, V_D = Open, or V_S = 3 V, V_D = Open,	Switch ON, see Figure 14	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
$I_{D(ON)}$	D ON leakage current	V_D = 1 V, V_S = Open, or V_D = 3 V, V_S = Open,	Switch ON, see Figure 14	25°C	3.6 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(2)									
V_{IH}	Input logic high			Full		2		V_+	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = V_+ or 0		25°C	3.6 V	–1	0.05	1	µA
				Full		–1		1	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	3.3 V		5		pC
$C_{S(OFF)}$	S OFF capacitance	V_S = V_+ or GND, Switch OFF,	See Figure 15	25°C	3.3 V		4.5		pF
$C_{D(OFF)}$	D OFF capacitance	V_D = V_+ or GND, Switch OFF,	See Figure 15	25°C	3.3 V		19		pF
$C_{S(ON)}$	S ON capacitance	V_S = V_+ or GND, Switch ON,	See Figure 15	25°C	3.3 V		25		pF
$C_{D(ON)}$	D ON capacitance	V_D = V_+ or GND, Switch ON,	See Figure 15	25°C	3.3 V		25		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 15	25°C	3.3 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 17	25°C	3.3 V		165		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	3.3 V		–69		dB

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 2.7 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	See Figure 19	25°C	3.3 V		–69		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	R_L = 50 Ω, f = 1 MHz,	See Figure 20	25°C	3.3 V		–74		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 22	25°C	3.3 V		0.21%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		2.5	7	µA
				Full				10	

6.6 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_D, V_S	Analog signal range					0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_S ≤ V_+, I_D = –24 mA,	Switch ON, see Figure 12	25°C	2.3 V		20.5	22	Ω
				Full				24	
Δr_{on}	ON-state resistance match between channels	V_S = 1.6 V, I_D = –24 mA,	Switch ON, see Figure 12	25°C	2.3 V		1	2	Ω
				Full				3	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_S ≤ V_+, I_D = –24 mA,	Switch ON, see Figure 12	25°C	2.3 V		16	18	Ω
				Full				20	
$I_{S(OFF)}$	S OFF leakage current	V_S = 0.5 V, V_D = 2.2 V, or V_S = 2.2 V, V_D = 0.5 V,	Switch OFF, see Figure 13	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
$I_{SPWR(OFF)}$		V_S = 0 to 2.7 V, V_D = 2.7 V to 0,		25°C	0 V	–1	0.5	1	
				Full		–5		5	
$I_{D(OFF)}$	D OFF leakage current	V_S = 0.5 V, V_D = 2.2 V, or V_S = 2.2 V, V_D = 0.5V,	Switch OFF, see Figure 13	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
$I_{DPWR(OFF)}$		V_D = 0 to 2.7 V, V_S = 2.7 V to 0,		25°C	0 V	–1	0.5	1	
				Full		–5		5	
$I_{S(ON)}$	S ON leakage current	V_S = 0.5 V, V_D = Open, or V_S = 2.2 V, V_D = Open,	Switch ON, see Figure 14	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
$I_{D(ON)}$	D ON leakage current	V_D = 0.5 V, V_S = Open, or V_D = 2.2 V, V_S = Open,	Switch ON, see Figure 14	25°C	2.7 V	–0.1	0.05	0.1	µA
				Full		–0.2		0.2	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(2)									
V_{IH}	Input logic high			Full		1.7		V_+	V
V_{IL}	Input logic low			Full		0		0.7	V
I_{IH}, I_{IL}	Input leakage current	V_I = V_+ or 0		25°C	2.7 V	–1	0.05	1	µA
				Full		–1		1	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 0.1 nF,	See Figure 21	25°C	2.5 V				pC
$C_{S(OFF)}$	S OFF capacitance	V_S = V_+ or GND, Switch OFF,	See Figure 15	25°C	2.5 V		4.5		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$C_{D(OFF)}$	D OFF capacitance	V_D = V_+ or GND, Switch OFF,	See Figure 15	25°C	2.5 V		18.5		pF
$C_{S(ON)}$	S ON capacitance	V_S = V_+ or GND, Switch ON,	See Figure 15	25°C	2.5 V		24		pF
$C_{D(ON)}$	D ON capacitance	V_D = V_+ or GND, Switch ON,	See Figure 15	25°C	2.5 V		24		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 15	25°C	2.5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 17	25°C	2.5 V		165		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	2.5 V		–69		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	See Figure 19	25°C	2.5 V		–69		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	R_L = 50 Ω, f = 1 MHz,	See Figure 20	25°C	2.5 V		–74		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see Figure 22	25°C	2.5 V		0.29%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		2.5	7	μA
				Full				10	

6.7 Switching Characteristics for 3.3-V supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	V_D = 2 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	3.3 V	1	5	9.5	ns
				Full	3 V to 3.6 V	1		10.5	
t_{OFF}	Turnoff time	V_D =2 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	3.3 V	0.5	1.5	3.5	ns
				Full	3 V to 3.6 V	0.5		4.5	

6.8 Switching Characteristics for 2.5-V supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	2.5 V	1.5	5	8	ns
				Full	2.3 V to 2.7 V	1		10	
t_{OFF}	Turnoff time	V_{COM} =2 V, R_L = 300 Ω,	C_L = 35 pF, see Figure 16	25°C	2.5 V	0.3	2	4.5	ns
				Full	2.3 V to 2.7 V	0.3		6	

6.9 Typical Characteristics

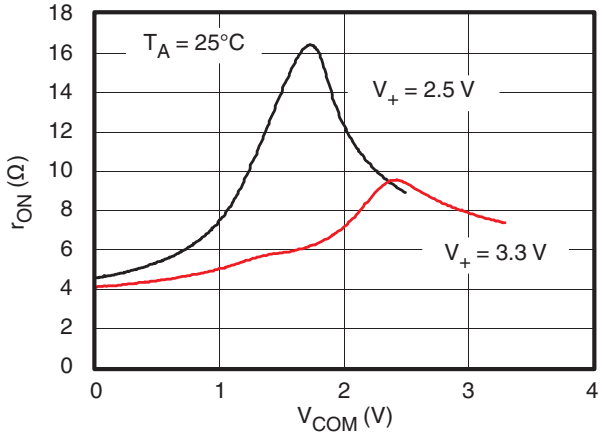


Figure 1. r_{on} vs V_{COM}

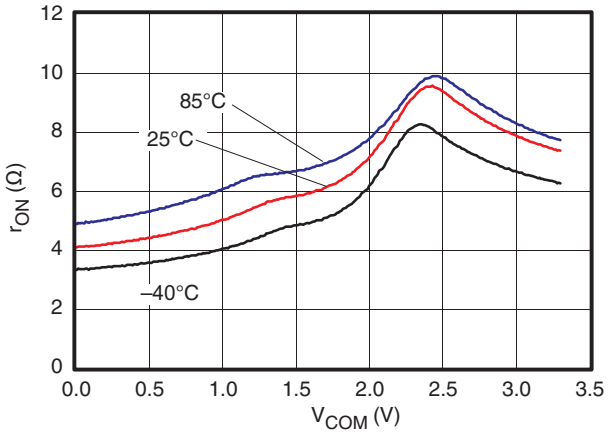


Figure 2. r_{on} vs V_{COM} (V_+ = 3.3 V)

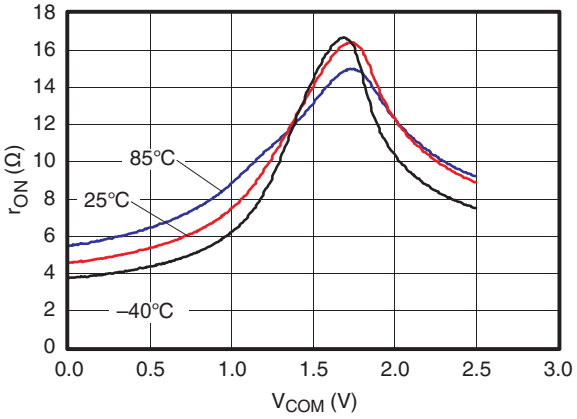


Figure 3. r_{on} vs V_{COM} (V_+ = 2.5 V)

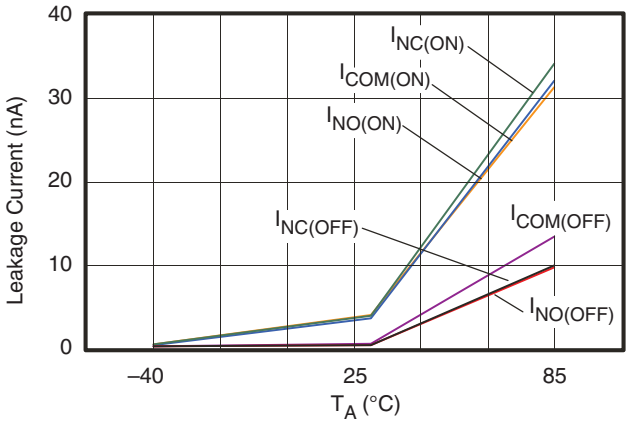


Figure 4. Leakage Current vs Temperature (V_+ = 3.6 V)

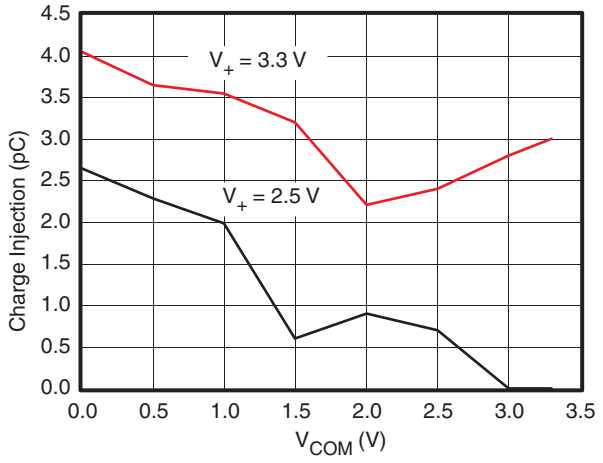


Figure 5. Charge Injection (Q_C) vs V_{COM}

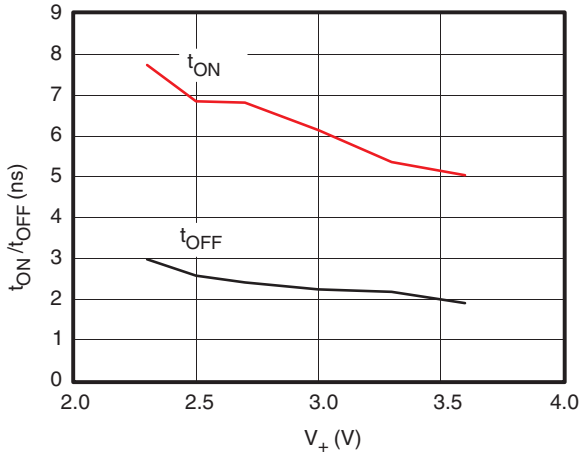


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

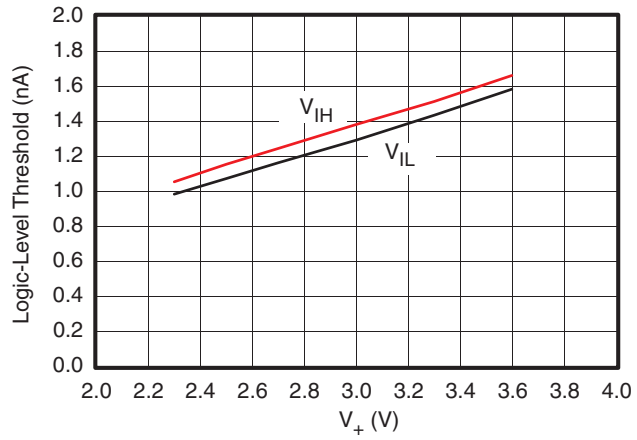


Figure 7. Logic-Level Threshold vs V_+

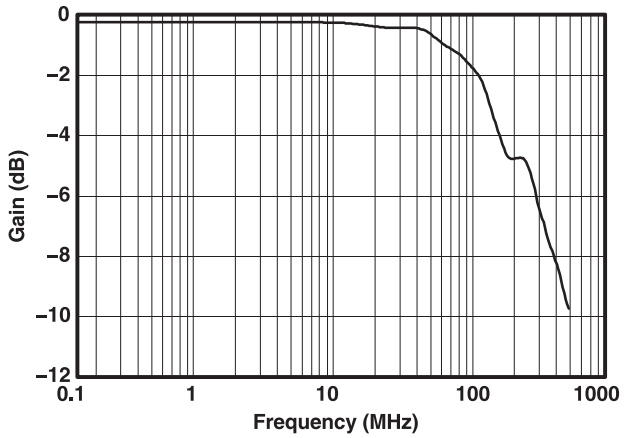


Figure 8. Bandwidth (Gain vs Frequency) (V_+ = 3.3 V)

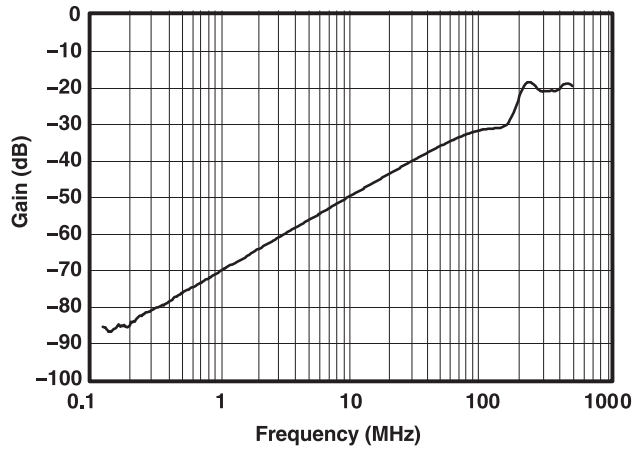


Figure 9. OFF Isolation and Crosstalk vs Frequency (V_+ = 3.3 V)

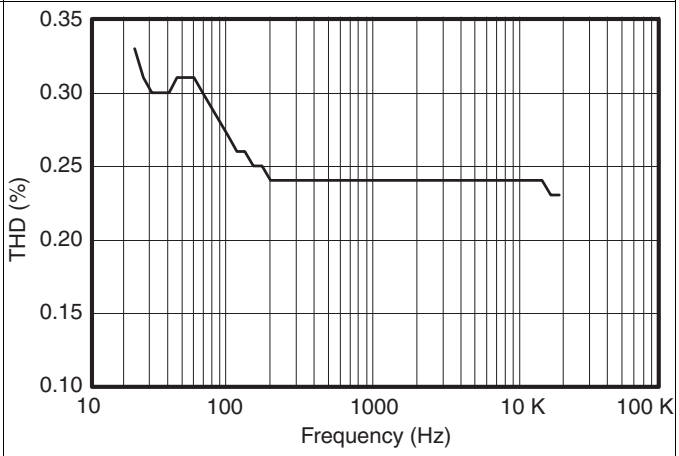


Figure 10. Total Harmonic Distortion vs Frequency

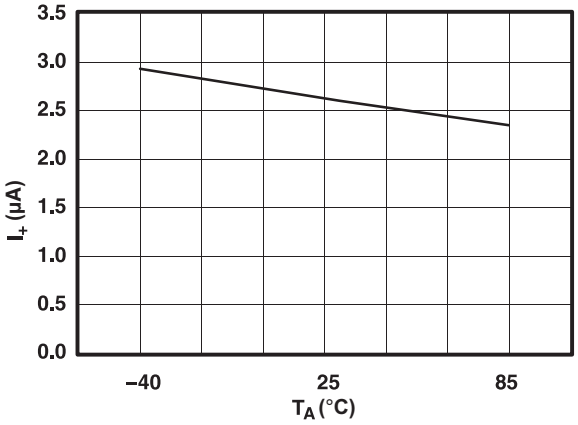


Figure 11. Power-Supply Current vs Temperature (V_+ = 3.6 V)

7 Parameter Measurement Information

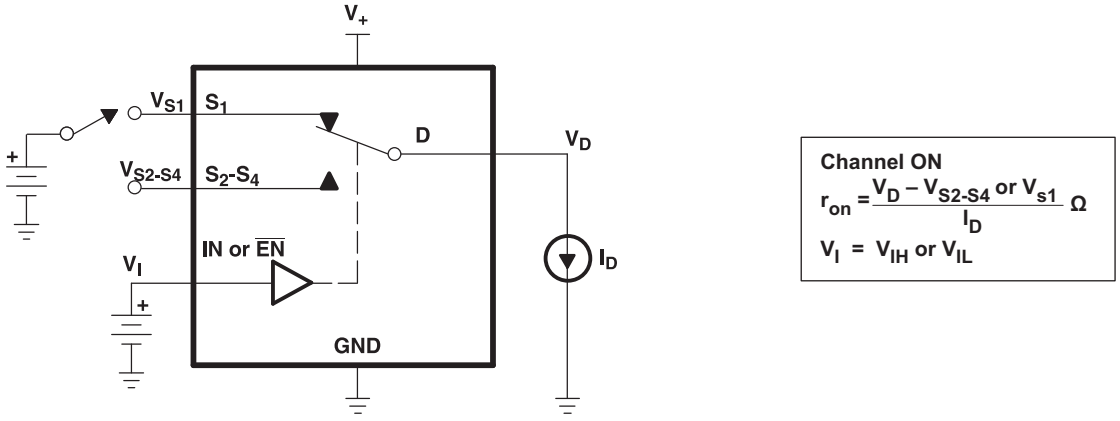


Figure 12. ON-State Resistance (r_{on})

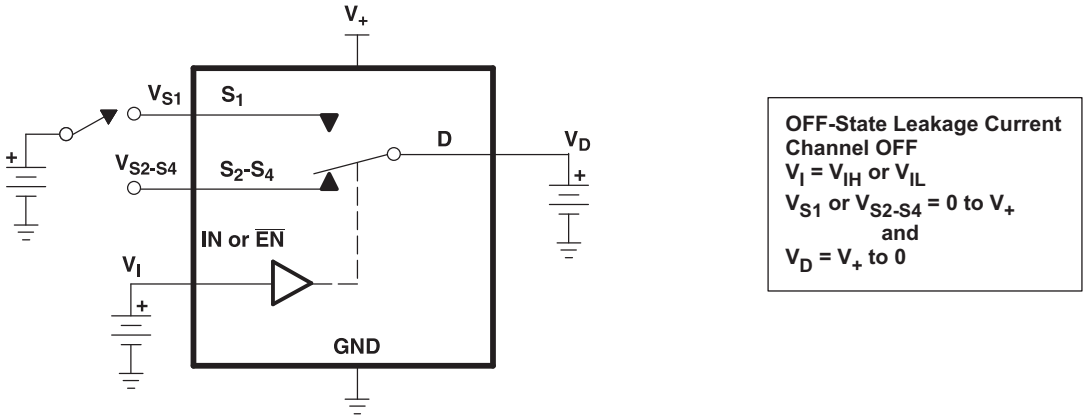


Figure 13. OFF-State Leakage Current ($I_{D(OFF)}$, $I_{S(OFF)}$)

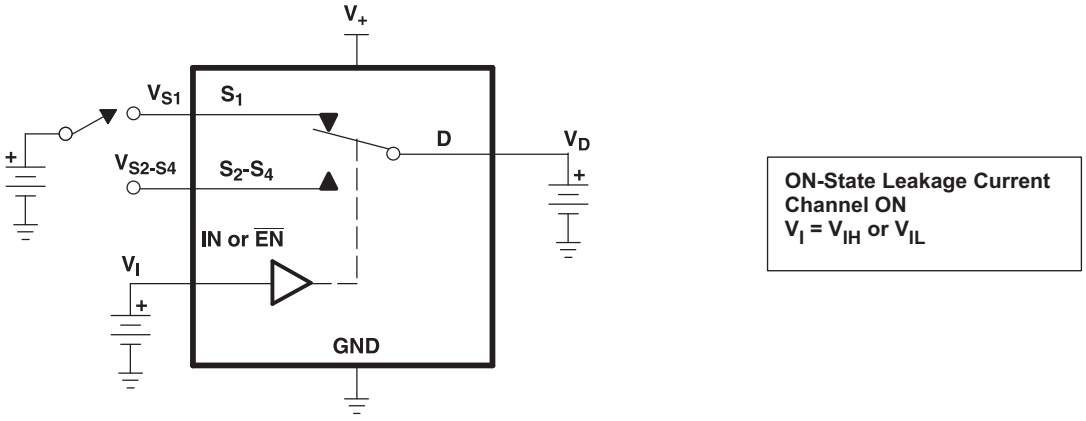


Figure 14. ON-State Leakage Current ($I_{D(ON)}$, $I_{S(ON)}$)

Parameter Measurement Information (continued)

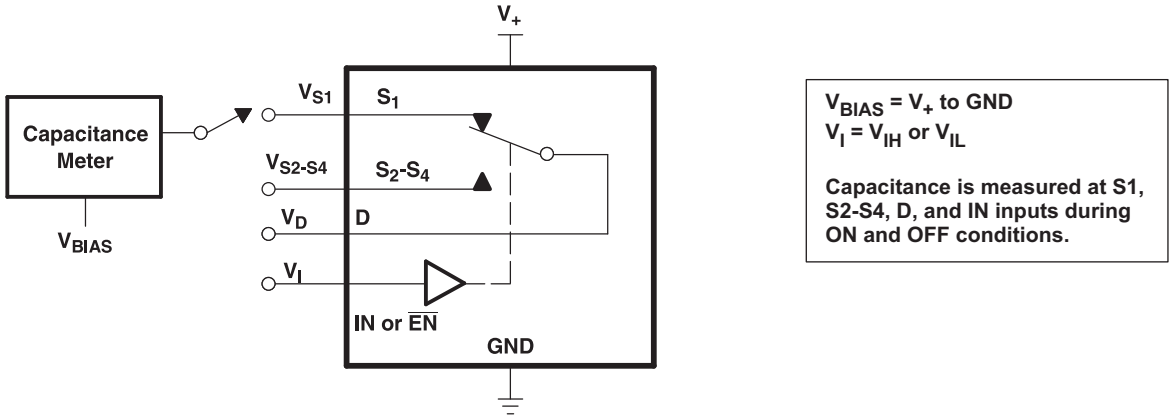
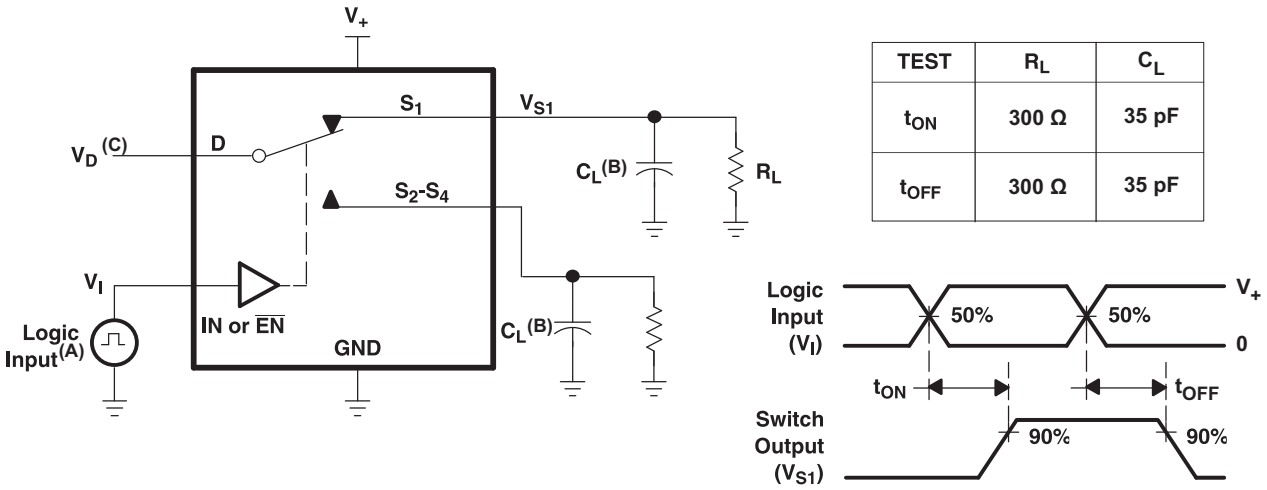


Figure 15. Capacitance (C_I, $C_{D(OFF)}$, $C_{D(ON)}$, $C_{S(OFF)}$, $C_{S(ON)}$)



TEST	R_L	C_L
t_{ON}	300 Ω	35 pF
t_{OFF}	300 Ω	35 pF

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

C. See Electrical Characteristics for V_D.

Figure 16. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

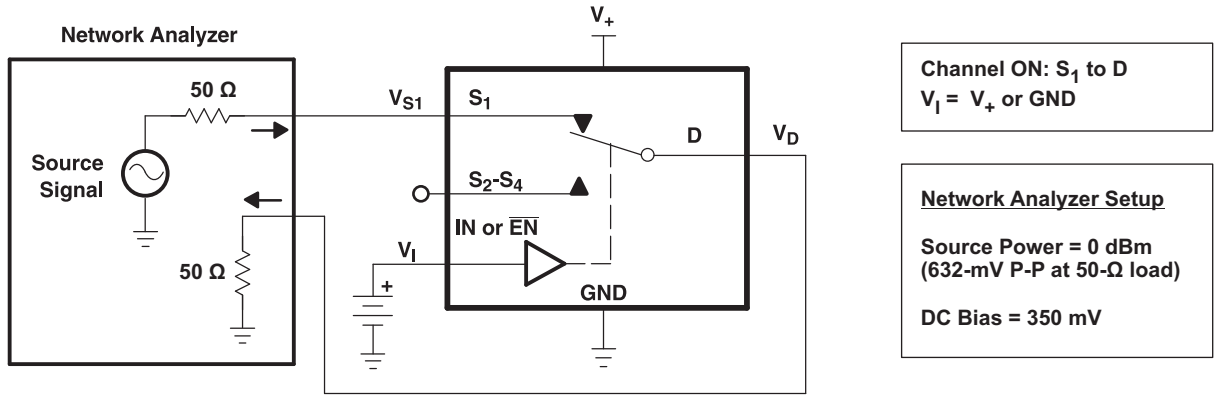


Figure 17. Bandwidth (BW)

Parameter Measurement Information (continued)

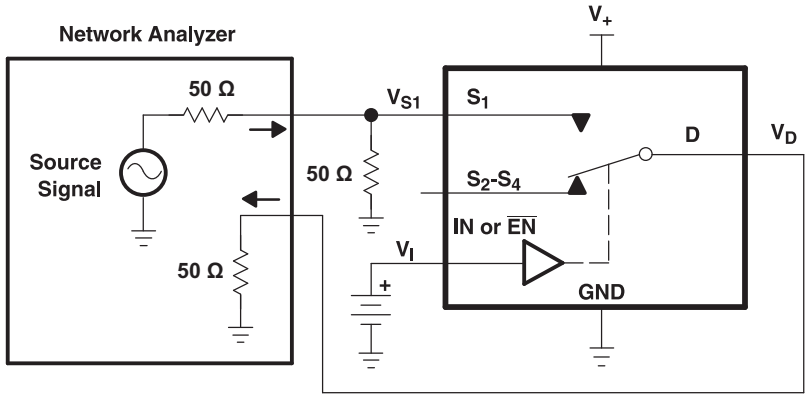


Figure 18. OFF Isolation (O_{ISO})

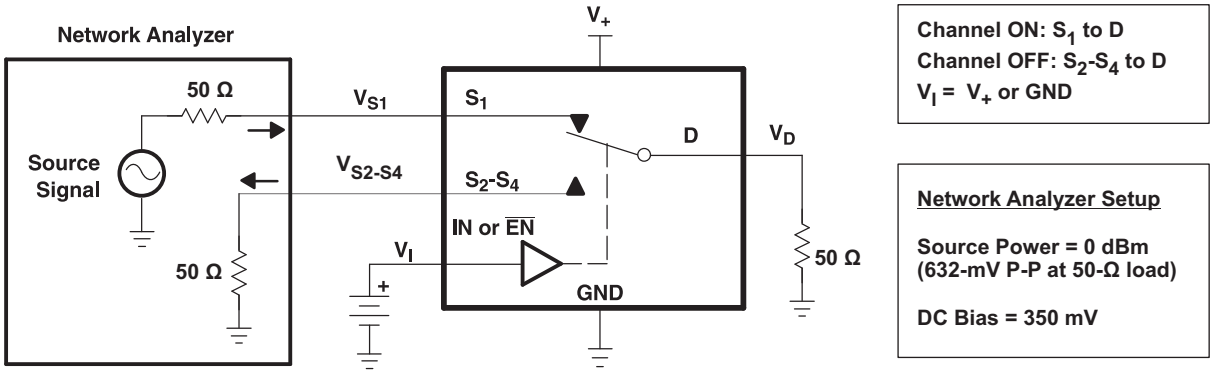


Figure 19. Crosstalk (X_{TALK})

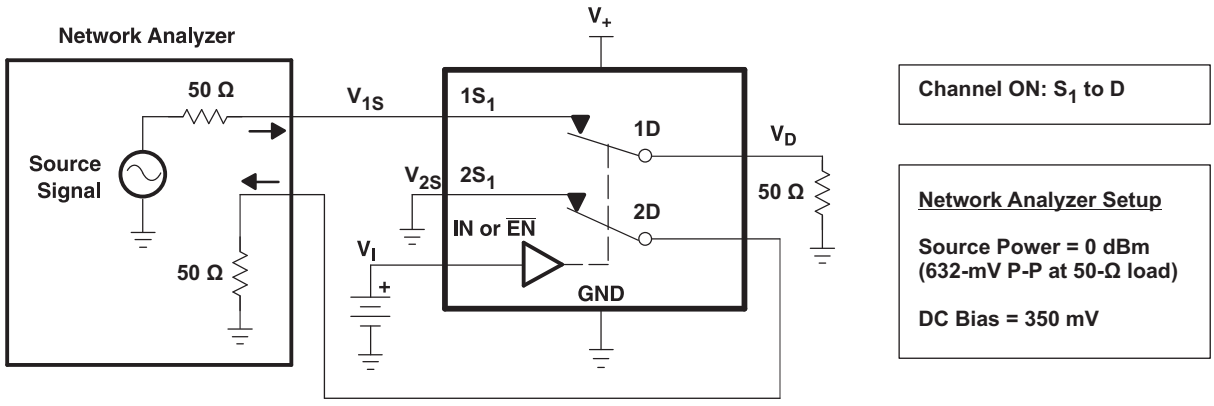
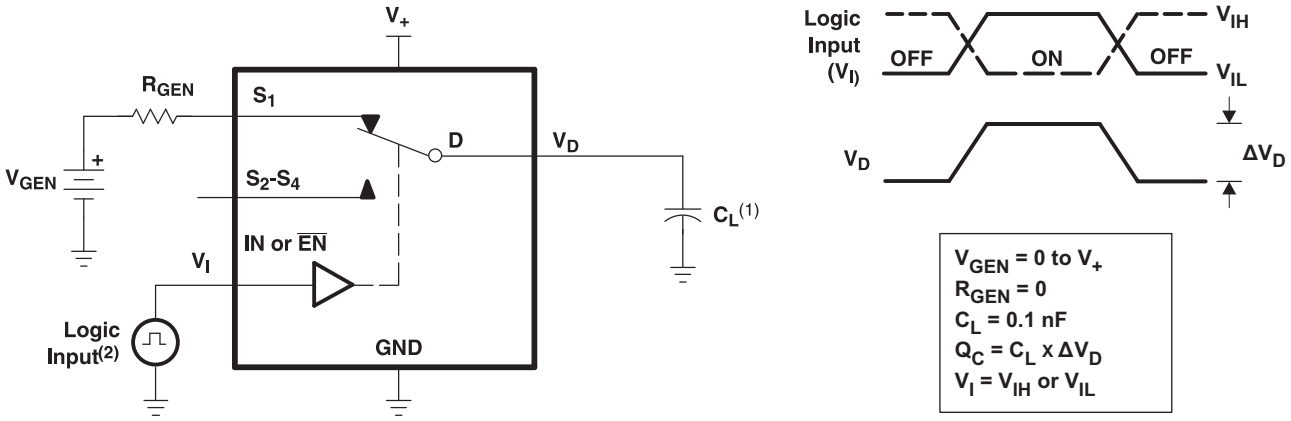


Figure 20. Adjacent Crosstalk (X_{TALK})

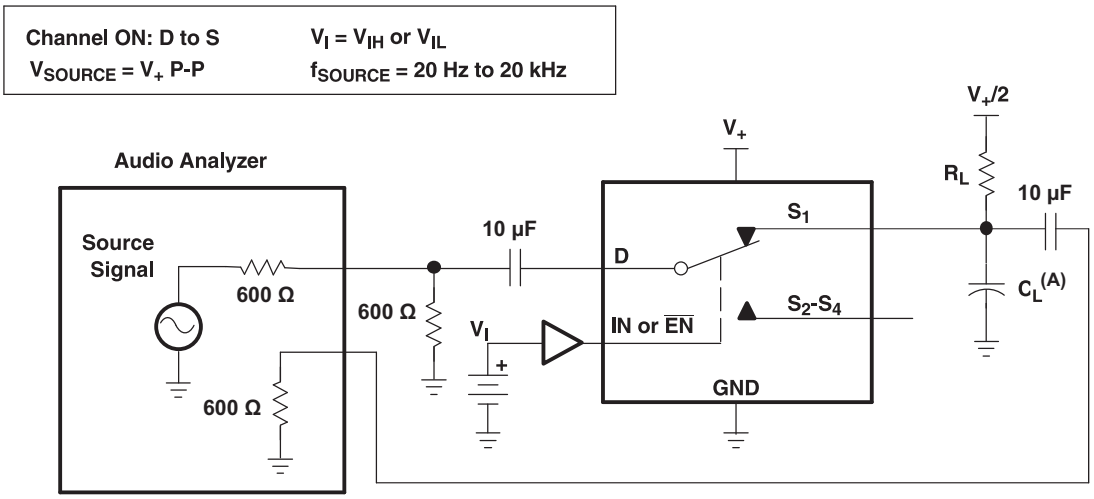
Parameter Measurement Information (continued)



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 21. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

Figure 22. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS3A5017 is a dual Single-Pole-4-Throw (SP4T) solid-state analog switch. The TS3A5017, like all analog switches, is bidirectional. Each D pin connects to its four respective S pins, with the switch connection dependent on the status of $\overline{EN}$, IN2, and IN1. See Table 1 for the switch configuration truth table.

8.2 Functional Block Diagram

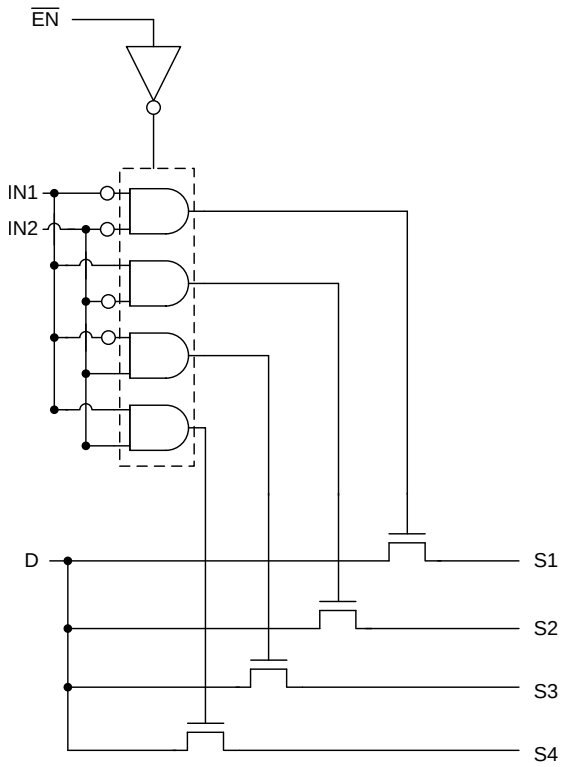


Figure 23. Functional Block Diagram (Each Switch)

8.3 Feature Description

Isolation in powered-down mode allows signals to be present at the inputs while the switch is powered off without causing damage to the device. The low ON-state resistance and low charge injection give the TS3A5017 better performance at higher speeds.

8.4 Device Functional Modes

Table 1. Function Table

$\overline{EN}$	IN2	IN1	D TO S, S TO D
L	L	L	D = S_1
L	L	H	D = S_2
L	H	L	D = S_3
L	H	H	D = S_4
H	X	X	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3A5018 can be used in a variety of customer systems. The TS3A5018 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

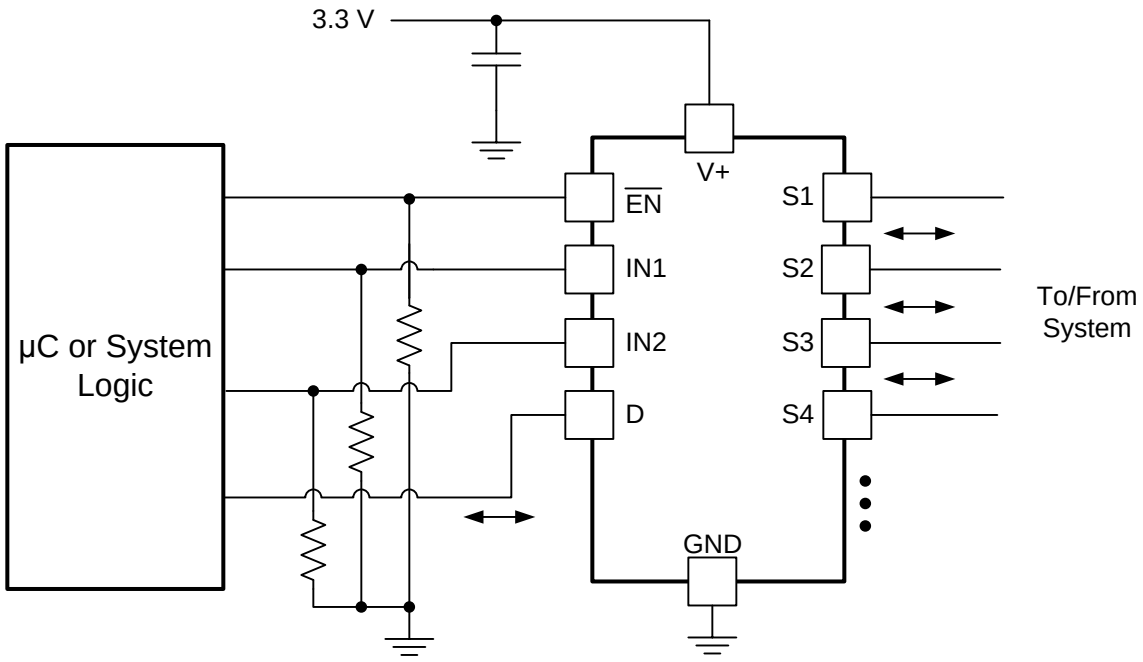


Figure 24. System Schematic for TS3A5017

9.2.1 Design Requirements

In this particular application, V+ was 3.3 V, although V+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, $\overline{EN}$, IN1, and IN2 are, by default, pulled low to GND. Choose these resistor sizes based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (continued)

9.2.3 Application Curve

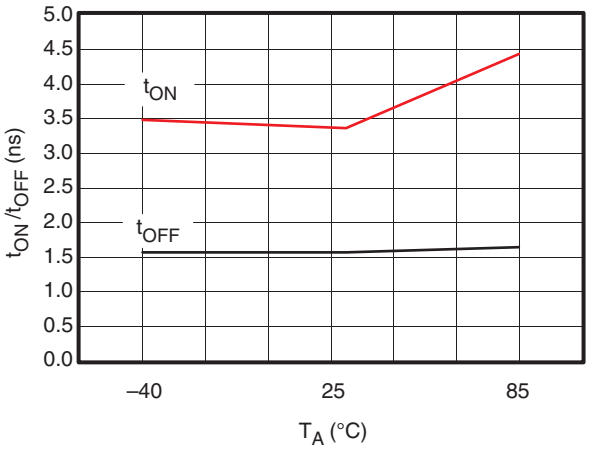


Figure 25. t_{ON} and t_{OFF} vs Temperature (V_+ = 3.3 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN1, IN2, and $\overline{EN}$ pins must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states. See *Implications of Slow or Floating CMOS Inputs,* SCBA004 for more details.

11.2 Layout Example

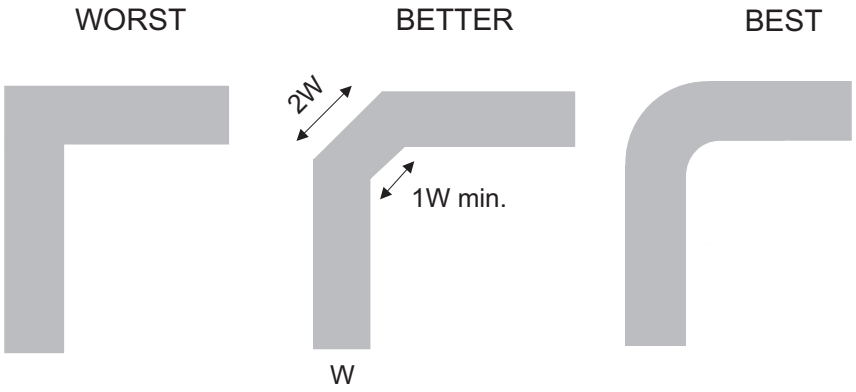


Figure 26. Trace Example

12 器件和文档支持

12.1 器件支持

12.1.1 器件命名规则

表 2. 参数 说明

符号	说明
V_{COM}	COM 处的电压
V_{NC}	NC 处的电压
V_{NO}	NO 处的电压
r_{on}	通道打开时 COM 和 NC 或 NO 端口之间的电阻
Δr_{on}	特定器件中通道间 r_{on} 的差值
$r_{on(flat)}$	额定条件范围下，同一通道内 r_{on} 最大值与最小值之间的差值
$I_{NC(OFF)}$	相应通道（NC 到 COM）处于关断状态时，在 NC 端口测得的泄漏电流
$I_{NC(ON)}$	相应通道（NC 到 COM）处于导通状态且输出 (COM) 处于开路状态时，在 NC 端口测得的泄漏电流
$I_{NO(OFF)}$	相应通道（NO 到 COM）处于关断状态时，在 NO 端口测得的泄漏电流
$I_{NO(ON)}$	相应通道（NO 到 COM）处于导通状态且输出 (COM) 处于开路状态时，在 NO 端口测得的泄漏电流
$I_{COM(OFF)}$	相应通道（COM 到 NC 或 NO）处于关断状态时，在 COM 端口测得的泄漏电流
$I_{COM(ON)}$	相应通道（COM 到 NC 或 NO）处于导通状态且输出 (NC 或 NO) 处于开路状态时，在 COM 端口测得的泄漏电流
V_{IH}	控制输入 (IN, $\overline{EN}$) 逻辑高电平的最小输入电压
V_{IL}	控制输入 (IN, $\overline{EN}$) 逻辑低电平的最大输入电压
V_I	控制输入 (IN, $\overline{EN}$) 处的电压
I_{IH}、I_{IL}	控制输入 (IN, $\overline{EN}$) 处测量的泄漏电流
t_{ON}	开关开通时间。此参数是在特定条件范围下，开关开通时，通过数字控制 (IN) 信号和模拟输出 NC 或 NO）信号之间的传播延迟测量得出。
t_{OFF}	开关关断时间。此参数是在特定条件范围下，开关开通时，通过数字控制 (OFF) 信号和模拟输出（NC 或 NO）信号之间的传播延迟测量得出。
Q_C	电荷注入是测量从控制 (IN) 输入到模拟（NC 或 NO）输入产生的不需要的信号耦合的方法。电荷注入以库仑为单位，可通过测量开关控制输入产生的总感应电荷得出该值。电荷注入，$Q_C = C_L \times \Delta V_{COM}$，$C_L$ 是负载电容，ΔV_{COM} 是模拟输出电压的变化。
$C_{NC(OFF)}$	相应通道（NC 到 COM）关闭时 NC 端口的电容
$C_{NC(ON)}$	相应通道（NC 到 COM）开启时 NC 端口的电容
$C_{NO(OFF)}$	相应通道（NO 到 COM）关闭时 NC 端口的电容
$C_{NO(ON)}$	相应通道（NO 到 COM）开启时 NC 端口的电容
$C_{COM(OFF)}$	相应通道（COM 到 NC）关闭时 COM 端口的电容
$C_{COM(ON)}$	相应通道（COM 到 NC）开启时 COM 端口的电容
C_I	控制输入 (IN, $\overline{EN}$) 电容
O_{ISO}	开关关断隔离用于衡量关断状态开关阻抗的大小。关断隔离以 dB 为单位，当相应通道（NC 到 COM）处于关断状态时，在额定频率下测量得出。
X_{TALK}	串扰是测量从开启状态的通道到关断状态的通道（NC1 到 NO1）产生的不必要信号耦合的方法。相邻串扰是测量从一条开启状态的通道到相邻开启状态的通道（NC1 到 NC2）产生的不必要信号耦合的方法。相邻串扰在额定频率下测量得出且以 dB 为单位。
BW	开关带宽。这是导通通道增益低于直流增益 -3dB 时的频率。
THD	总谐波失真用于描述由模拟开关导致的信号失真。其定义为二次、三次和更高次谐波与基波绝对幅度之比的均方根 (RMS) 值。
I_+	静态电源电流，以及 V_+ 或 GND 的控制 (IN) 引脚

12.2 文档支持

12.2.1 相关文档

- 《*慢速或浮点 CMOS 输入的影响*》，SCBA004

12.3 商标

All trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A5017D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5017	Samples
TS3A5017DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA017	Samples
TS3A5017DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	Samples
TS3A5017DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3A5017	Samples
TS3A5017PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	Samples
TS3A5017PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	Samples
TS3A5017PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA017	Samples
TS3A5017RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA017	Samples
TS3A5017RGYRG4	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YA017	Samples
TS3A5017RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TS3A5017 :

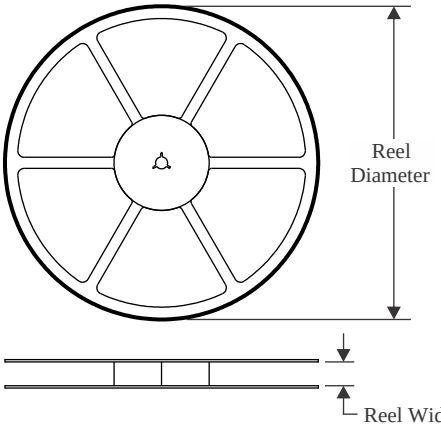
- Automotive : TS3A5017-Q1

NOTE: Qualified Version Definitions:

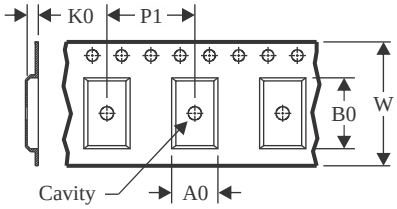
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

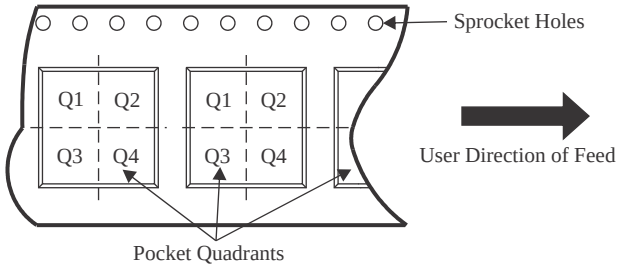


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

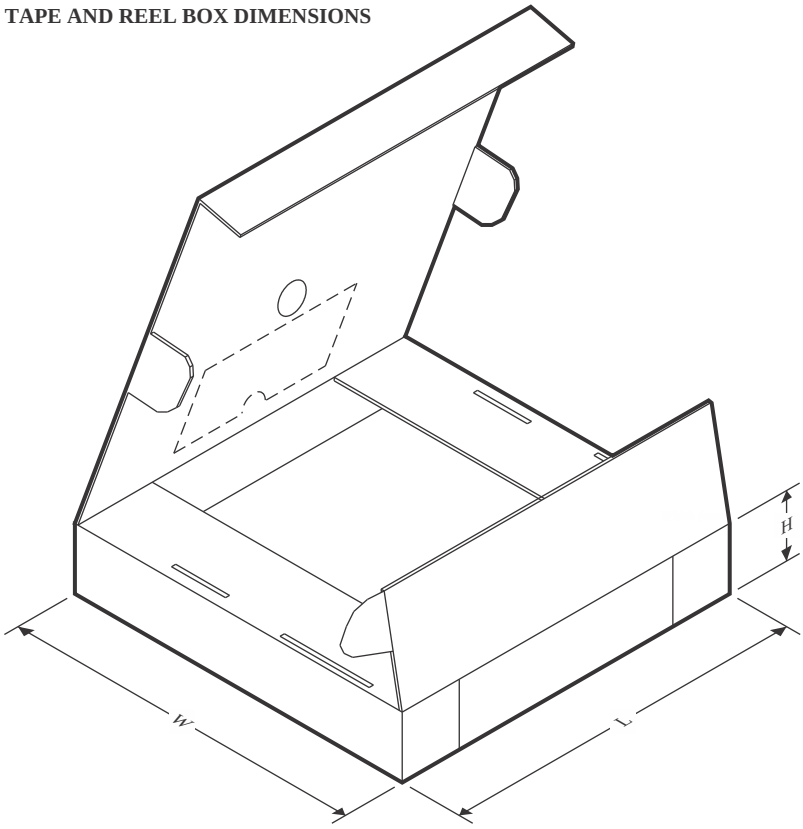
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5017DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TS3A5017DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
TS3A5017DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS3A5017PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A5017RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TS3A5017RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

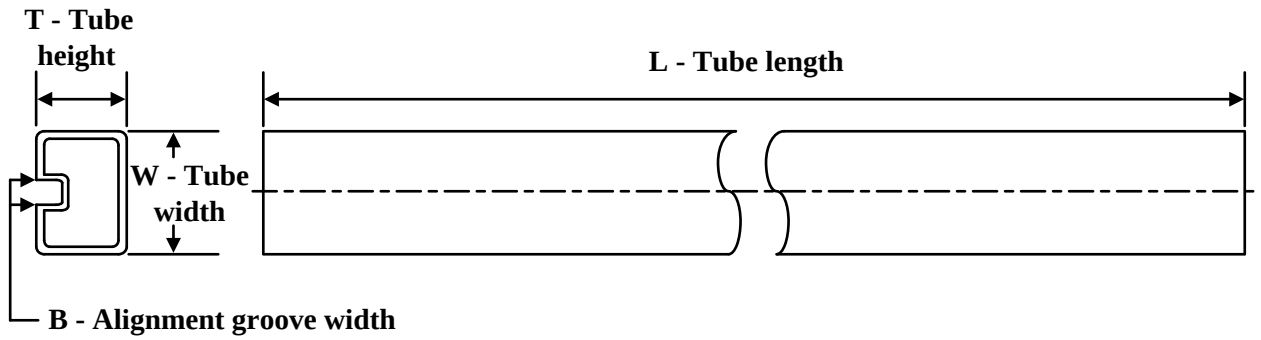
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5017DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
TS3A5017DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
TS3A5017DR	SOIC	D	16	2500	340.5	336.1	32.0
TS3A5017PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TS3A5017RGYR	VQFN	RGY	16	3000	356.0	356.0	35.0
TS3A5017RSVR	UQFN	RSV	16	3000	200.0	183.0	25.0

TUBE



*All dimensions are nominal

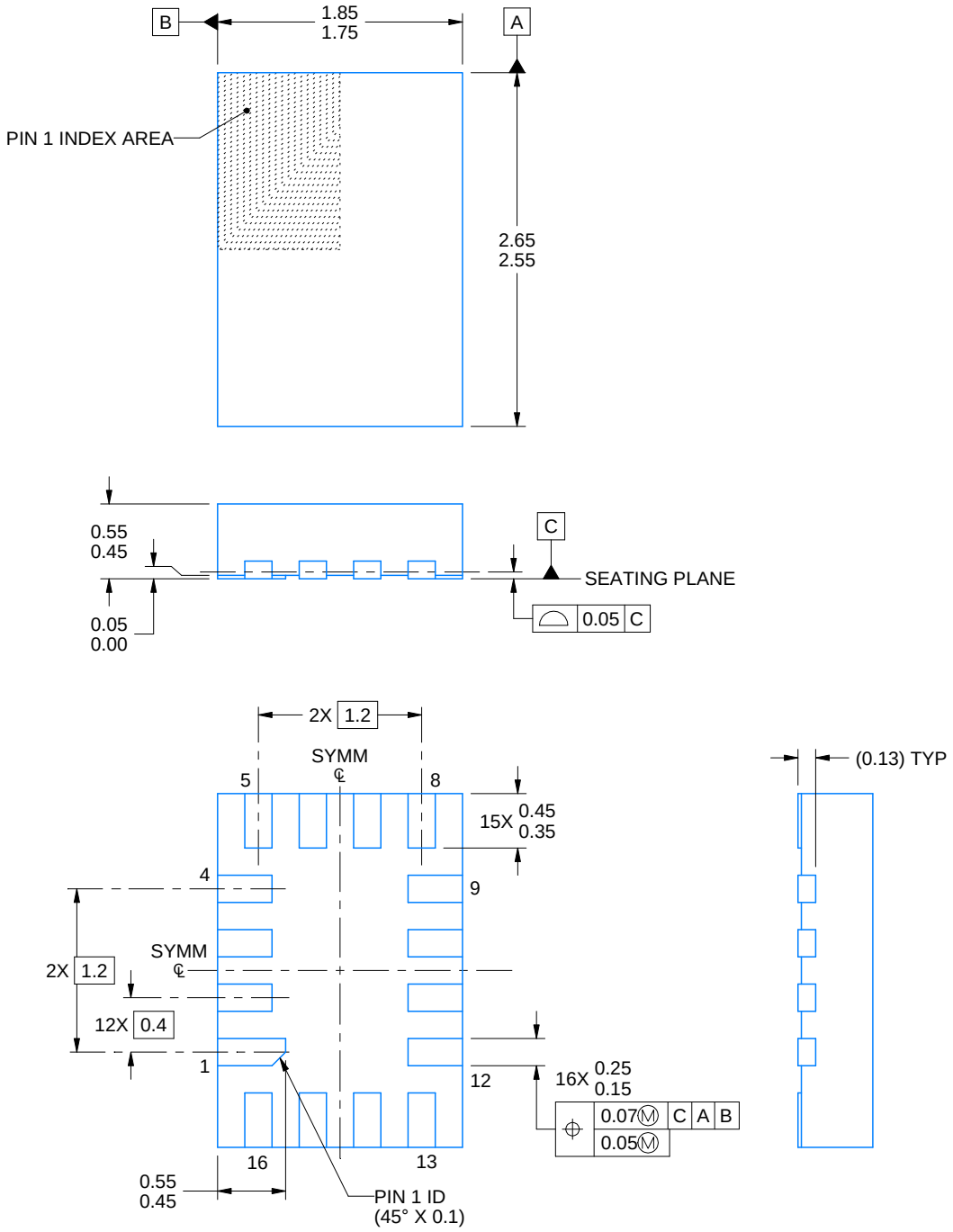
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TS3A5017D	D	SOIC	16	40	507	8	3940	4.32
TS3A5017PW	PW	TSSOP	16	90	530	10.2	3600	3.5

RSV0016A

PACKAGE OUTLINE

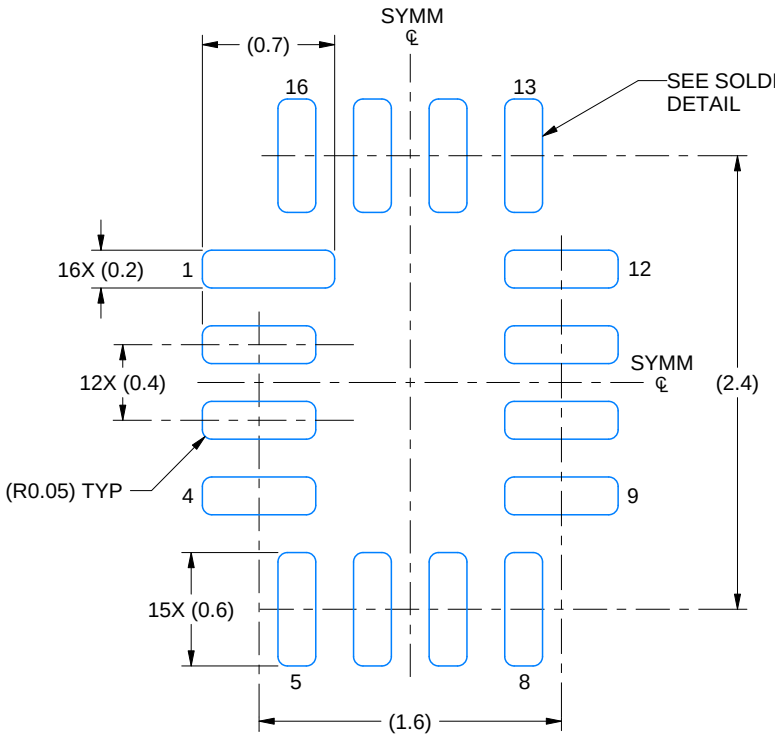
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

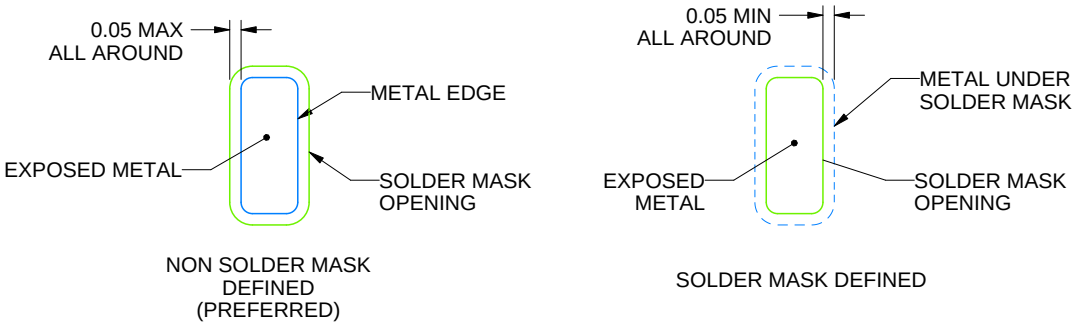


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

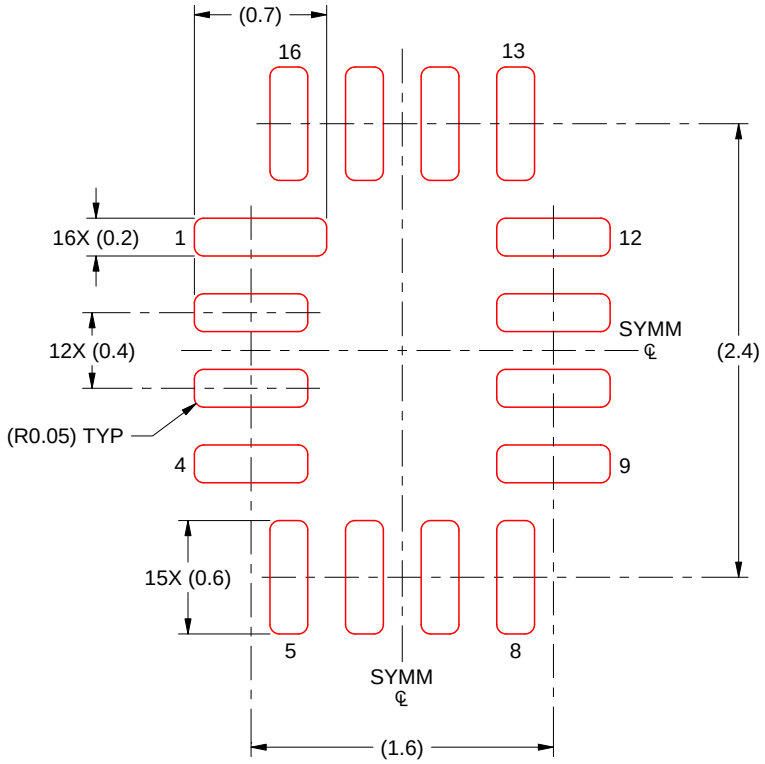


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



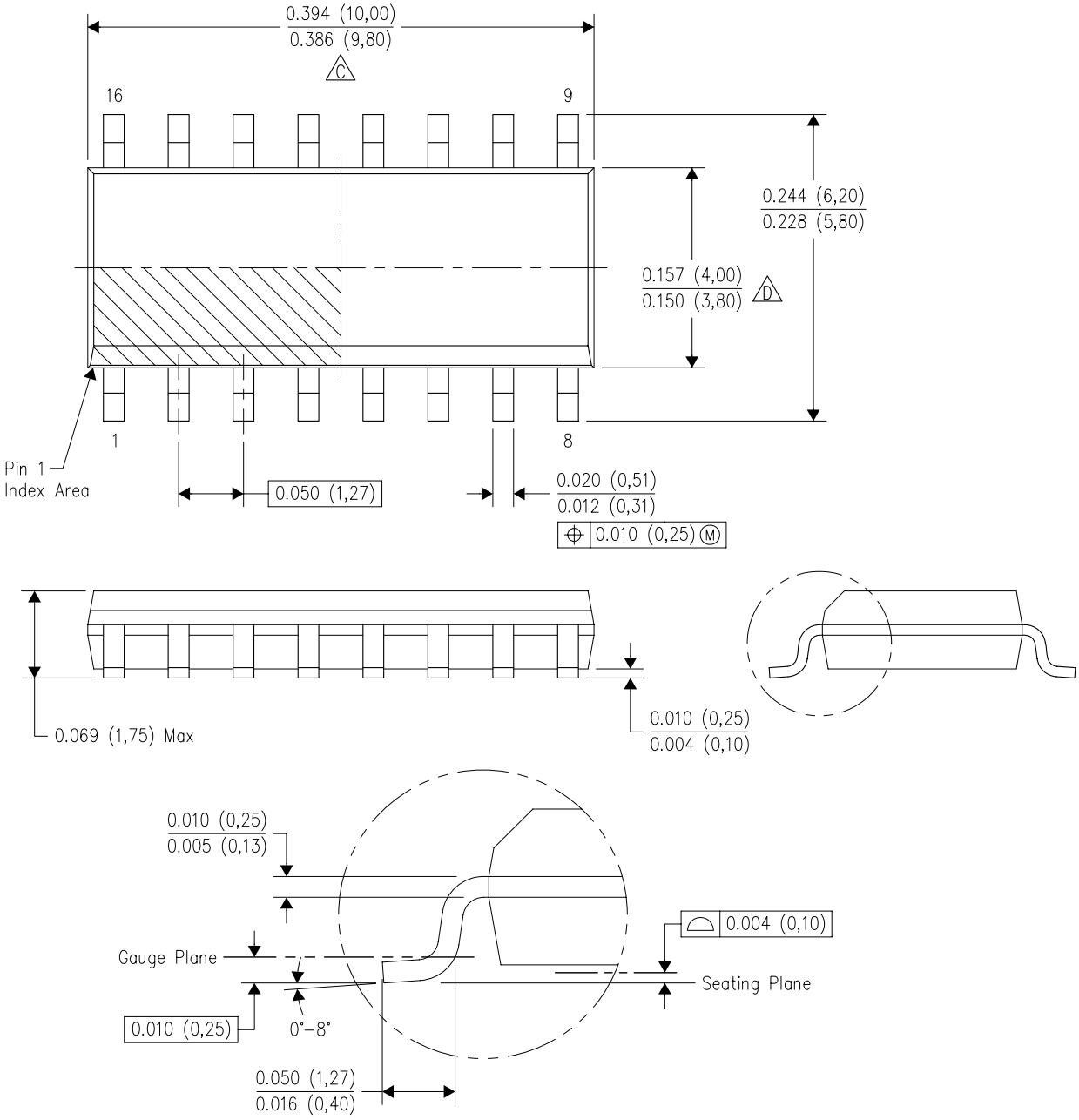
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

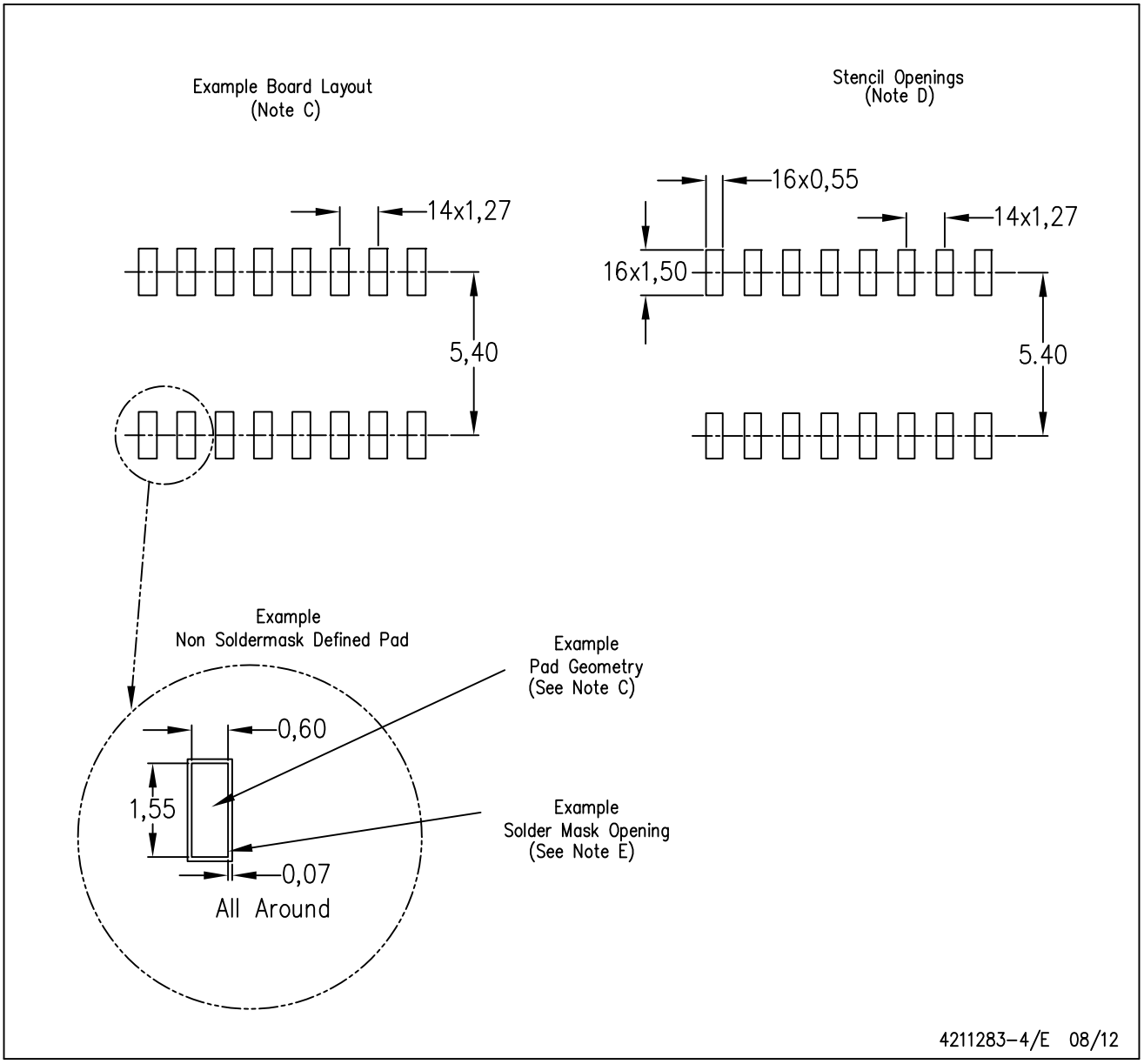
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



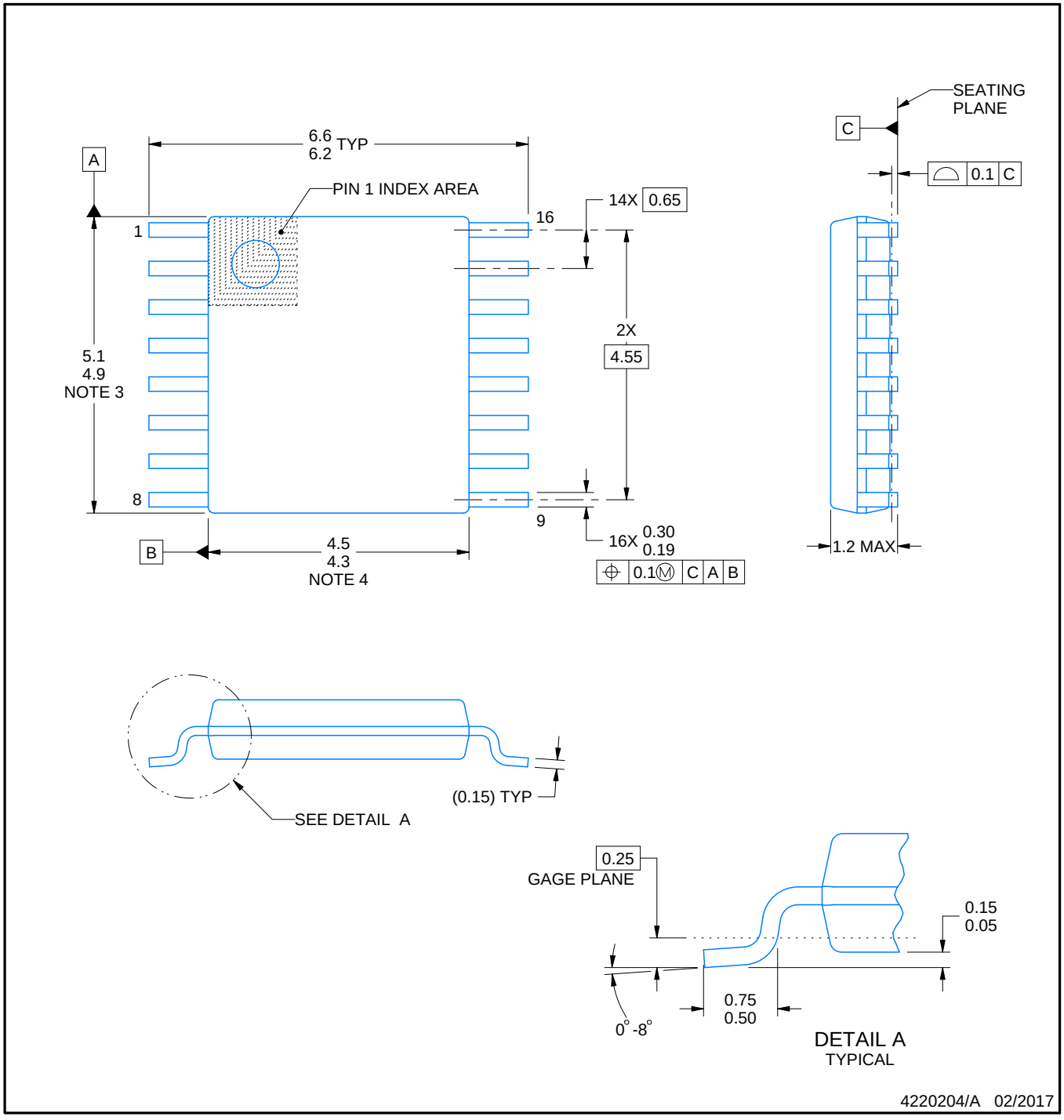
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

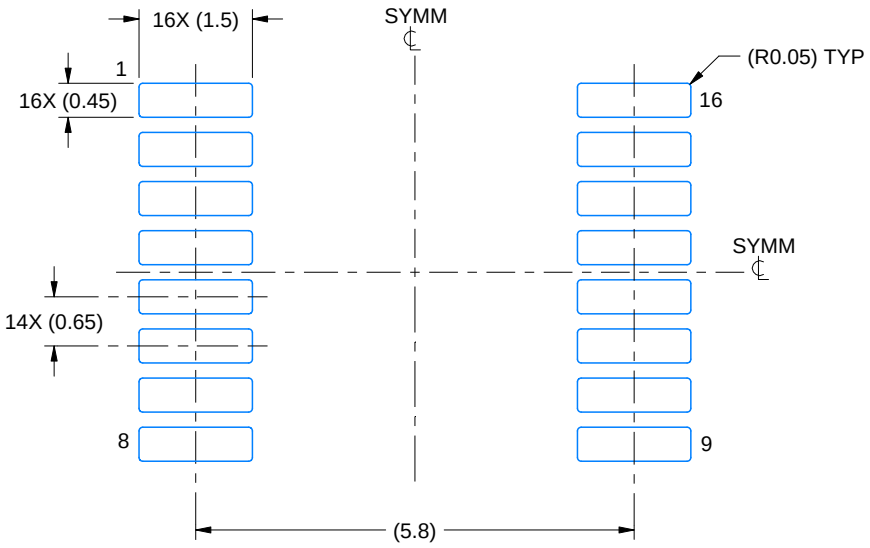
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

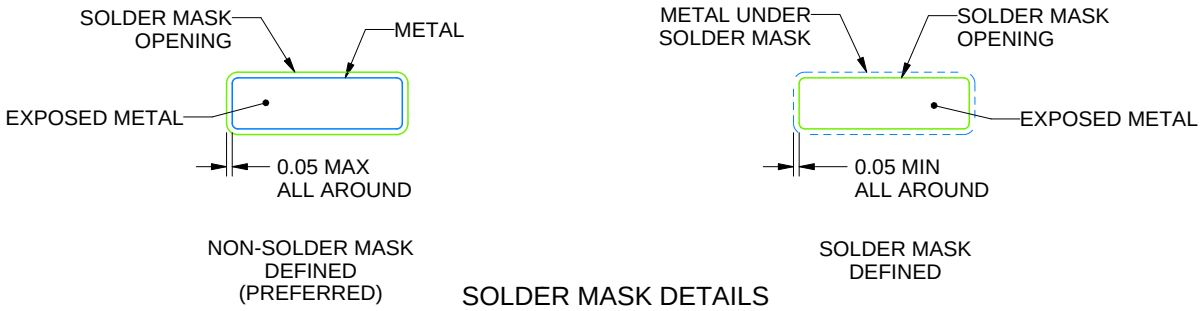


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

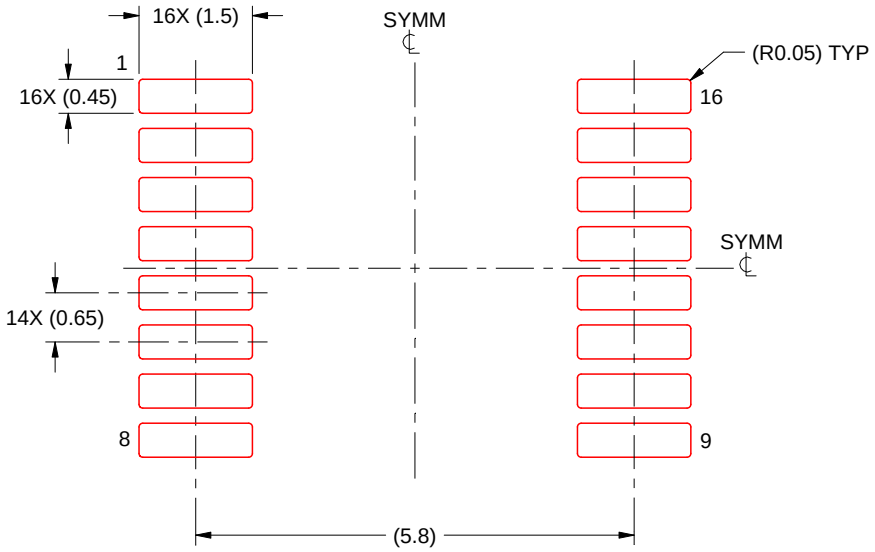


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

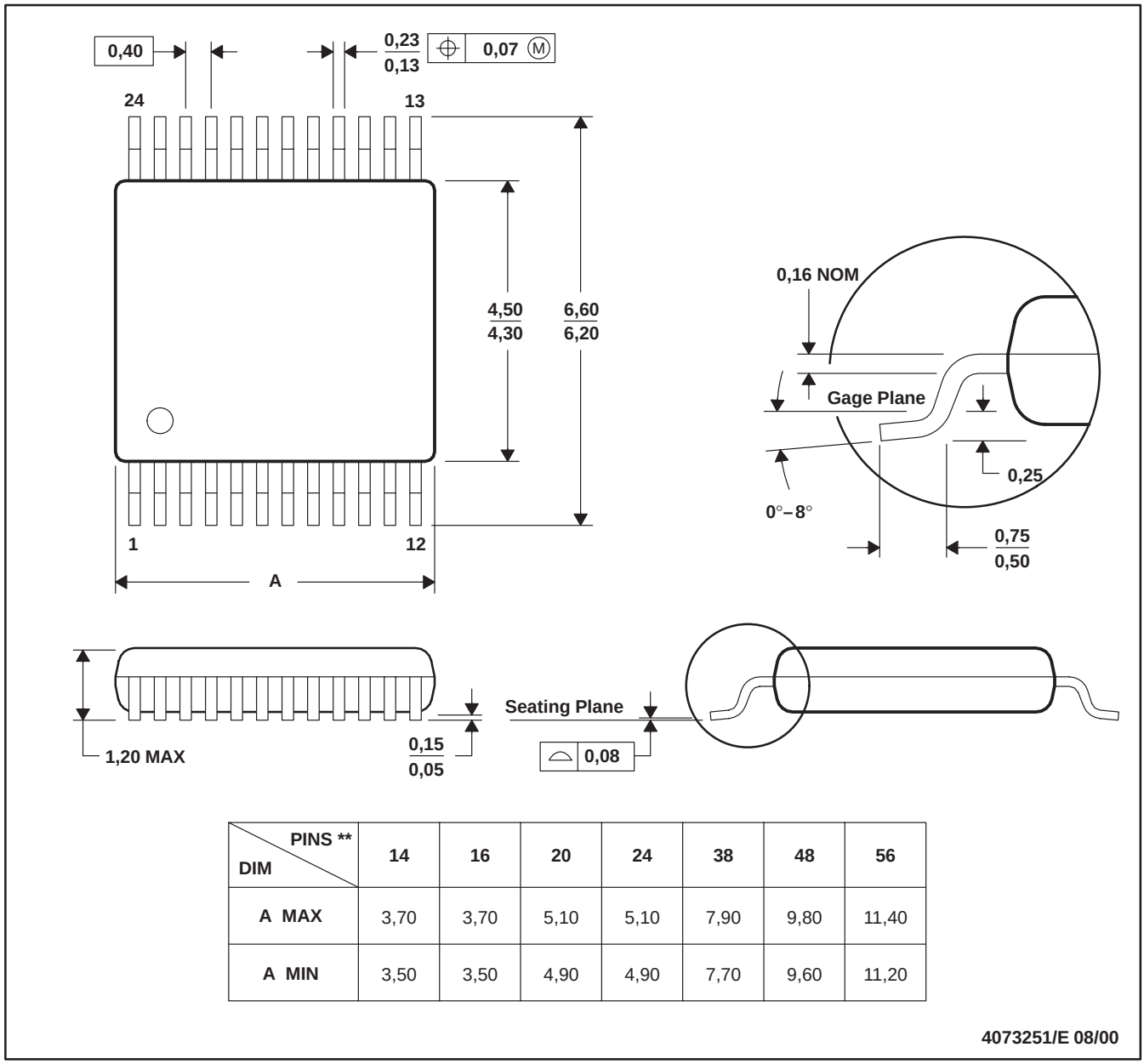
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

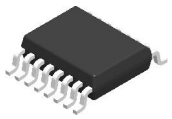
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

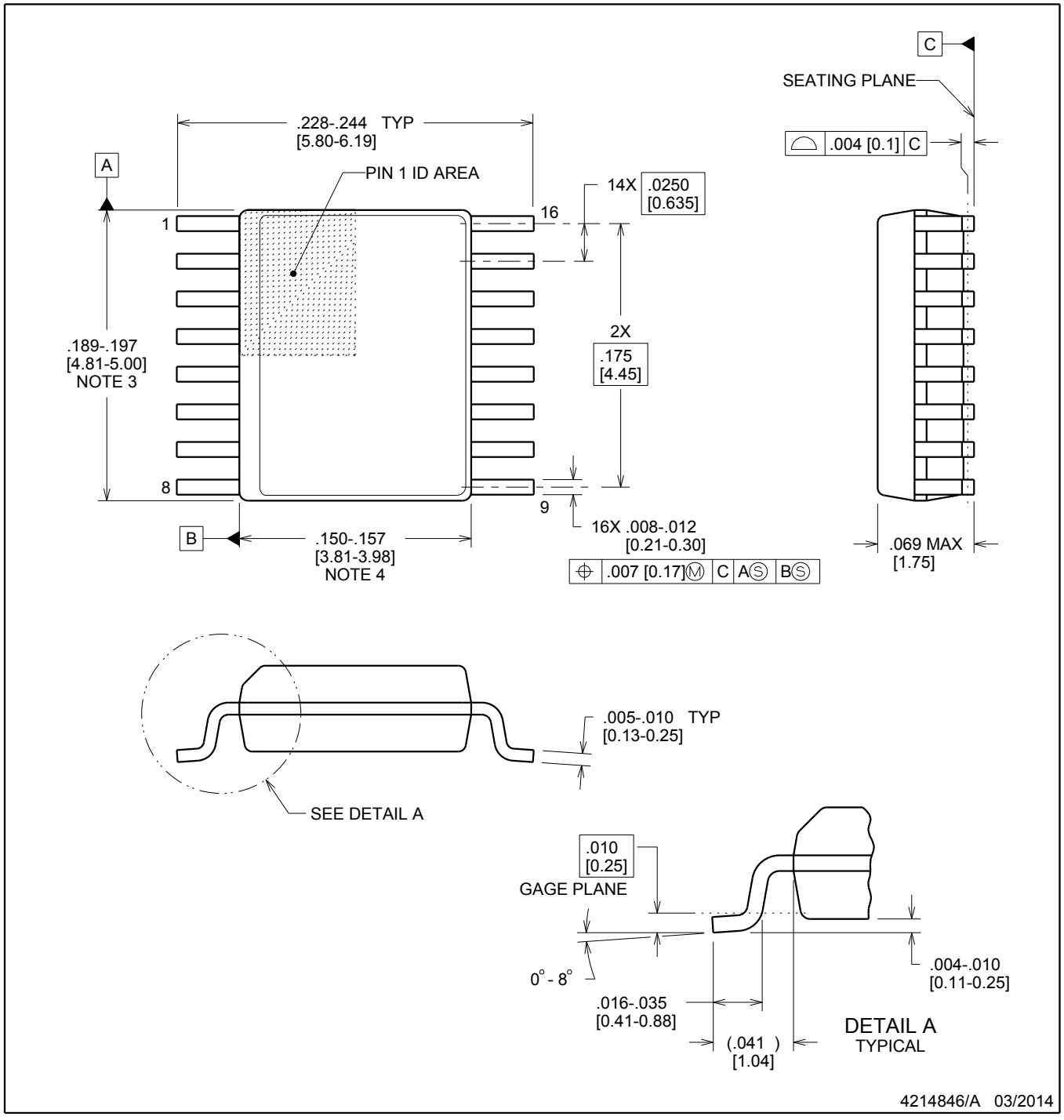


PACKAGE OUTLINE

DBQ0016A

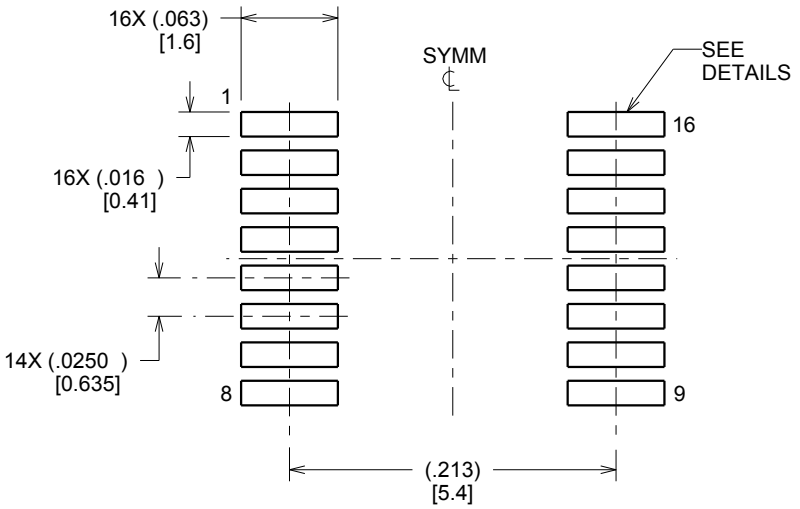
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

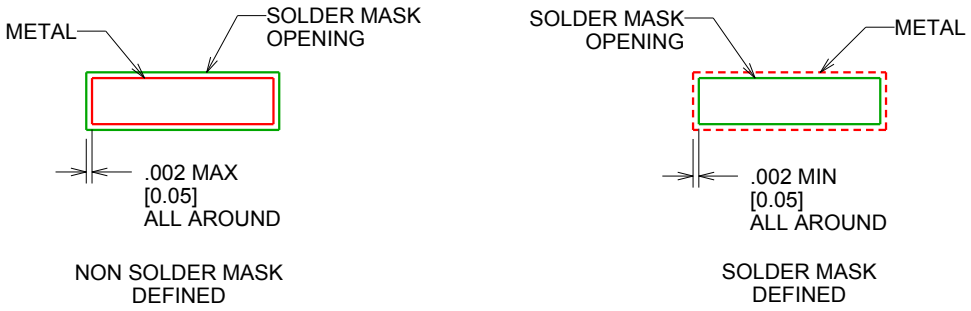


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

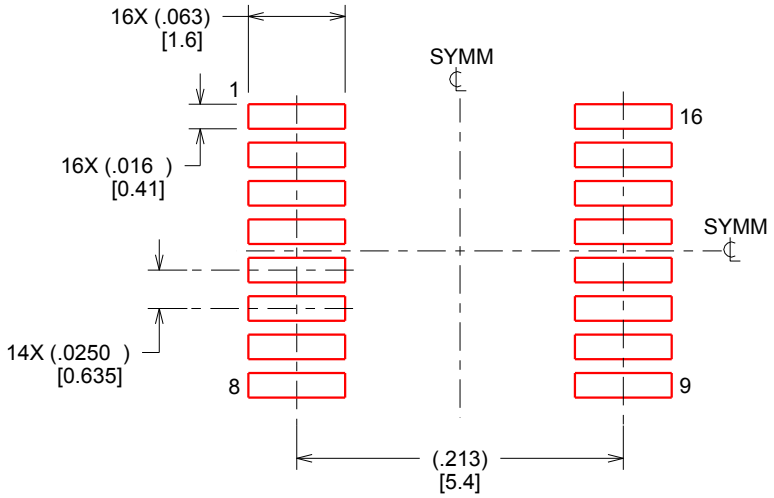
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



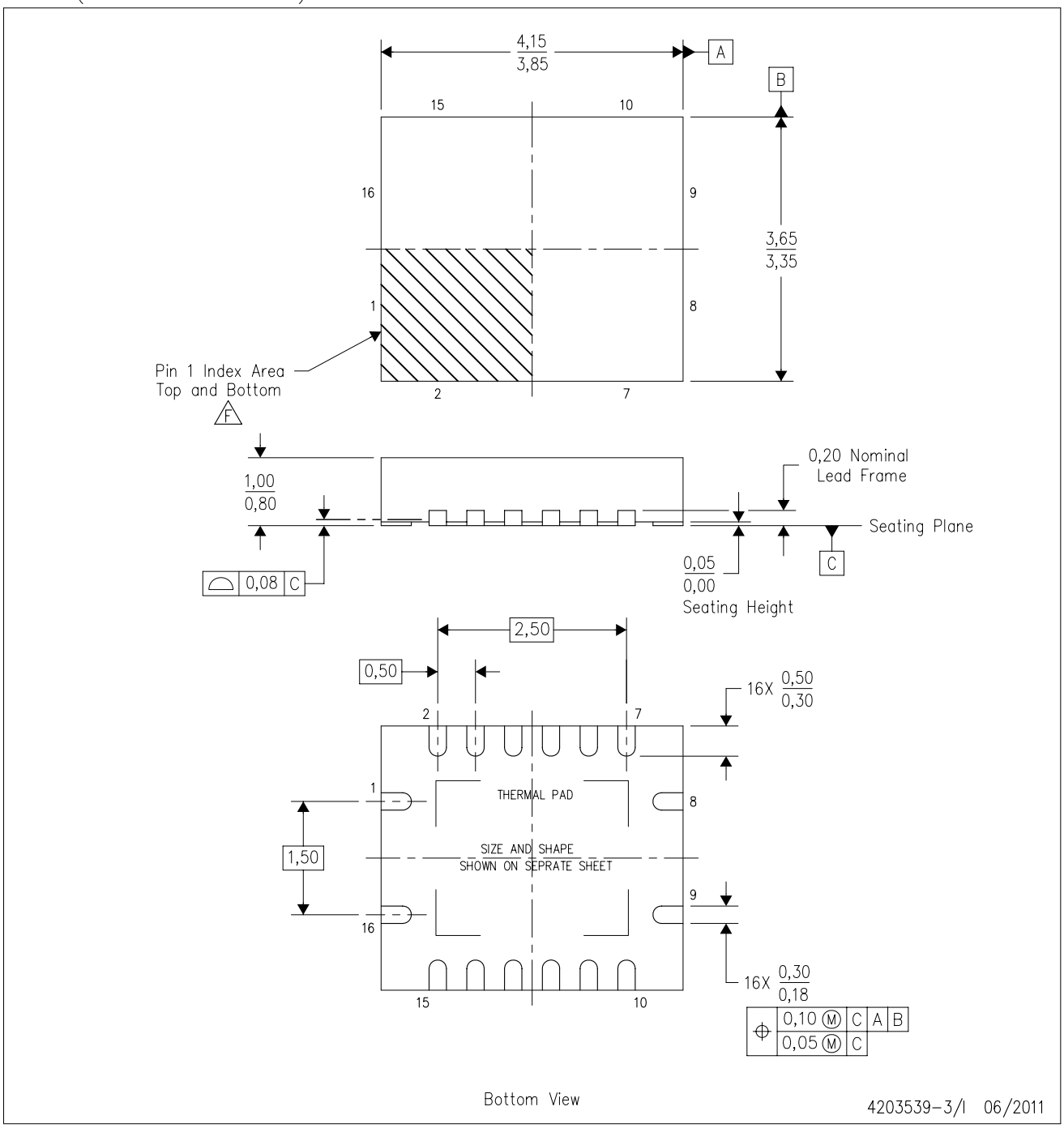
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

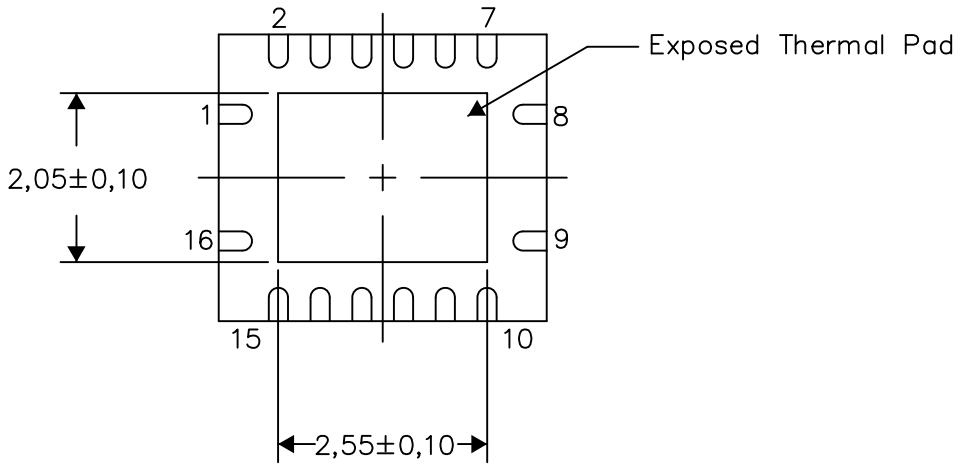
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



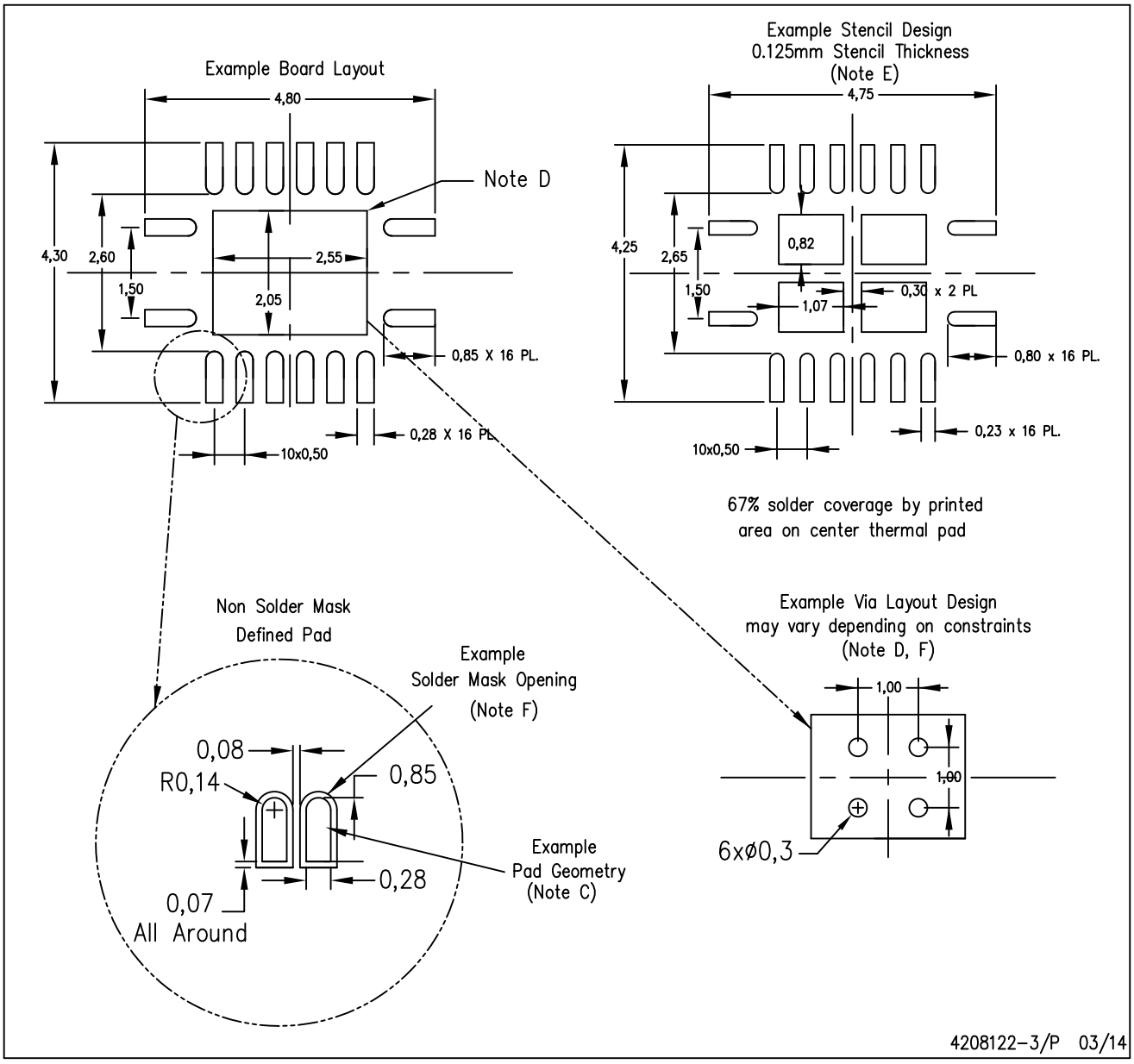
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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