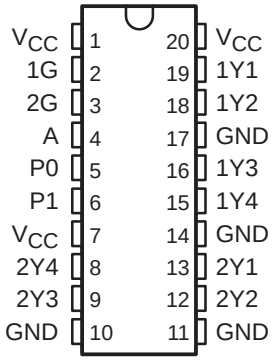
- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Eight Outputs**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs (–48-mA I_{OH}, 48-mA I_{OL})**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Packaging Options Include Plastic Small-Outline (DW) Packages**

DW PACKAGE
(TOP VIEW)



description

The CDC341 is a high-performance clock-driver circuit that distributes one (A) input signal to eight (Y) outputs with minimum skew for clock distribution. Through the use of the control pins (1G and 2G), the outputs can be placed in a low state regardless of the A input.

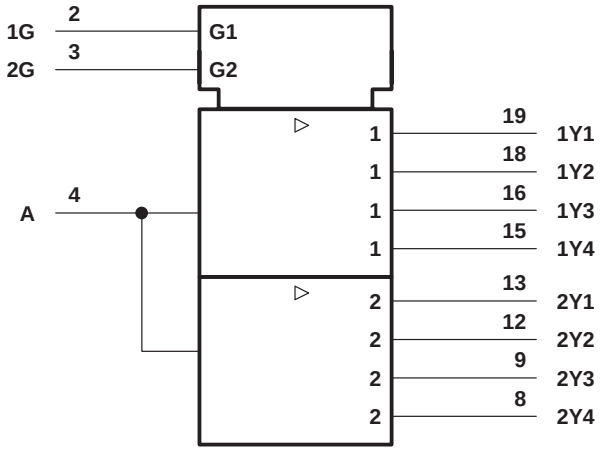
The propagation delays are adjusted at the factory using the P0 and P1 pins. These pins are not intended for customer use and should be strapped to GND.

The CDC341 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

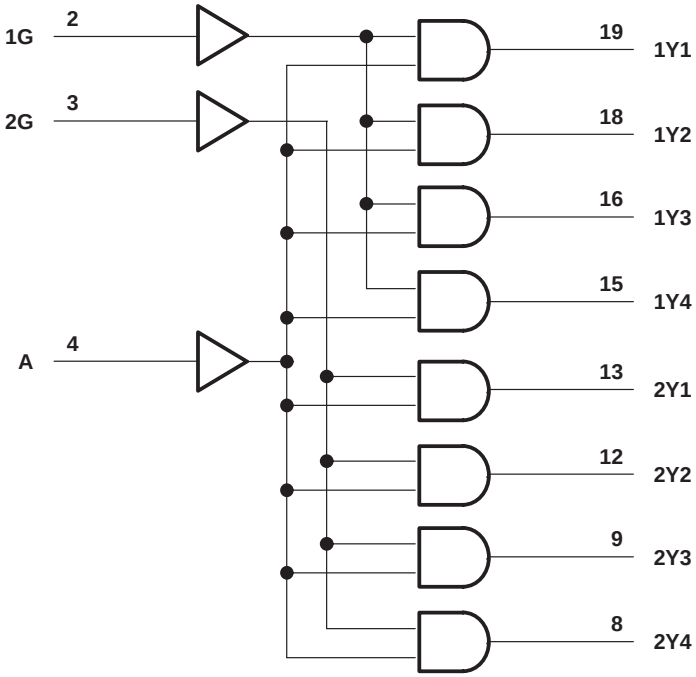
INPUTS			OUTPUTS	
1G	2G	A	1Y1–1Y4	2Y1–2Y4
X	X	L	L	L
L	L	H	L	L
L	H	H	L	H
H	L	H	H	L
H	H	H	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state,
V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . 96 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 1.6 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current			–48	mA
I_{OL}	Low-level output current			48	mA
f_{clock}	Input clock frequency	One output bank loaded		80	MHz
		Both output banks loaded		40	
T_A	Operating free-air temperature		0	70	°C

NOTE 3: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP†	MAX			
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2		–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = – 3 mA		2.5			2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		
	V_{CC} = 4.75 V,	I_{OH} = – 48 mA		2			2		
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA						0.5	V
I_I	V_{CC} = 5.25 V,	V_I = V_{CC} or GND				±1		±1	µA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.5 V		–50	–100	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.25 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		2			3.5	mA
			Outputs low		24			33	
C_i	V_I = 2.5 V or 0.5 V				3				pF

† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

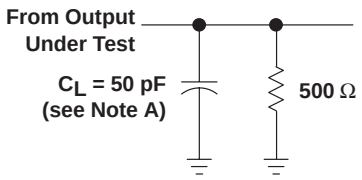
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	3.5		4.5	3.1	4.9	ns
t_{PHL}			3.5		4.3	3.1	4.9	
t_{PLH}	G	Y	2		3.8	2	4	ns
t_{PHL}			2		3.8	2	4	
$t_{sk(o)}$	A	Y		0.3	0.5		0.6	ns
$t_{sk(p)}$				0.6	0.8		0.9	
$t_{sk(pr)}$					1		1	
t_r	A	Y					1.5	ns
t_f	A	Y					1.5	ns

t_{pd} performance information relative to V_{CC} and temperature variation (see Note 4)

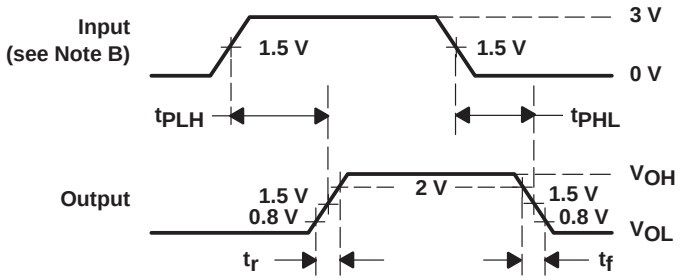
$Dt_{PLH(TA)}$†	Temperature drift of t_{PLH} from 0°C to 70°C	–41 ps/10°C
$Dt_{PHL(TA)}$†	Temperature drift of t_{PHL} from 0°C to 70°C	–52 ps/10°C
$Dt_{PLH(VCC)}$‡	V_{CC} drift of t_{PLH} from 4.75 V to 5.25 V	28 ps/100 mV
$Dt_{PHL(VCC)}$‡§	V_{CC} drift of t_{PHL} from 4.75 V to 5.25 V	20 ps/100 mV

† Virtually independent of V_{CC}
‡ Virtually independent of temperature
NOTE 4: The data extracted is from a wide range of characterization material.

PARAMETER MEASUREMENT INFORMATION



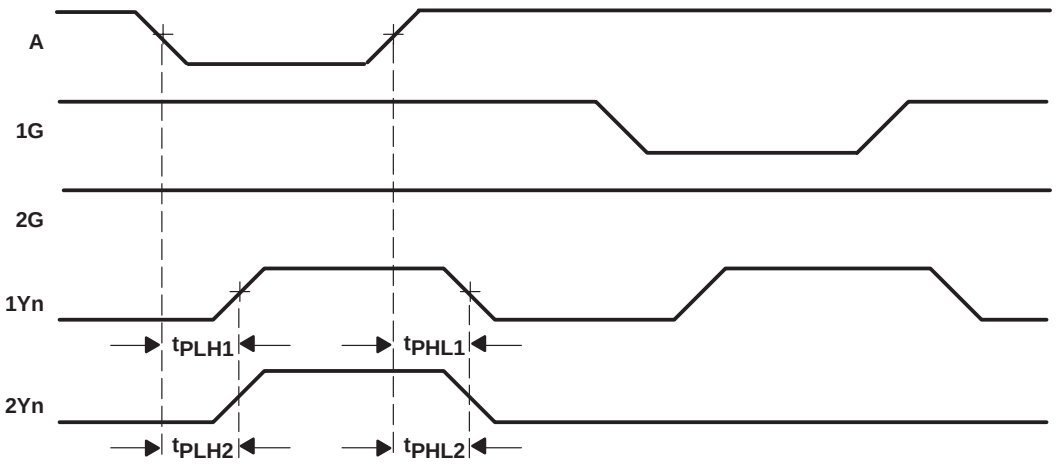
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
– The difference between the fastest and slowest of t_{PLHn} (n = 1, 2)
– The difference between the fastest and slowest of t_{PHLn} (n = 1, 2)
B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of | $t_{PLHn} - t_{PHLn}$ | (n = 1, 2).
C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
– The difference between the fastest and slowest of t_{PLHn} (n = 1, 2) across multiple devices under identical operating conditions
– The difference between the fastest and slowest of t_{PHLn} (n = 1, 2) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC341DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC341	Samples
CDC341DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC341	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

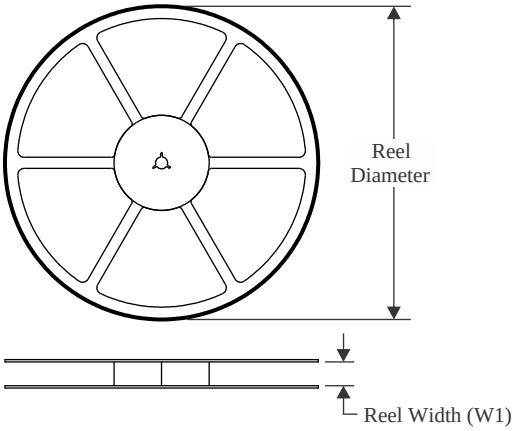
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

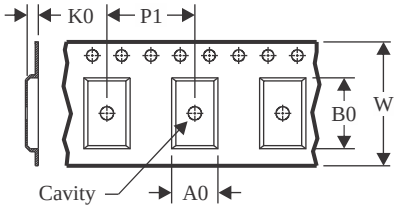
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

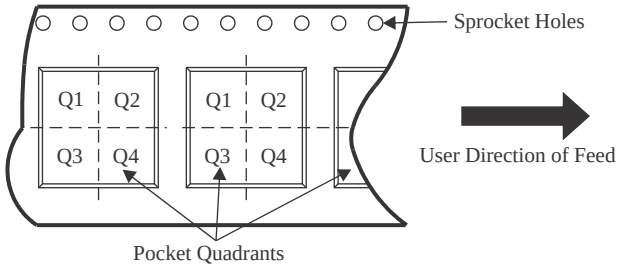


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

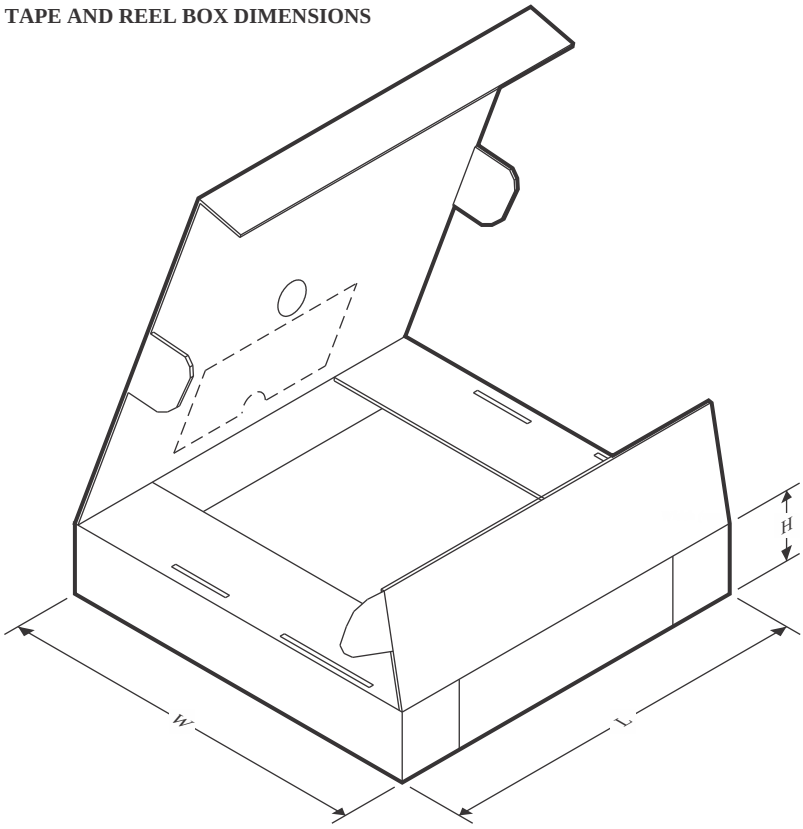
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC341DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

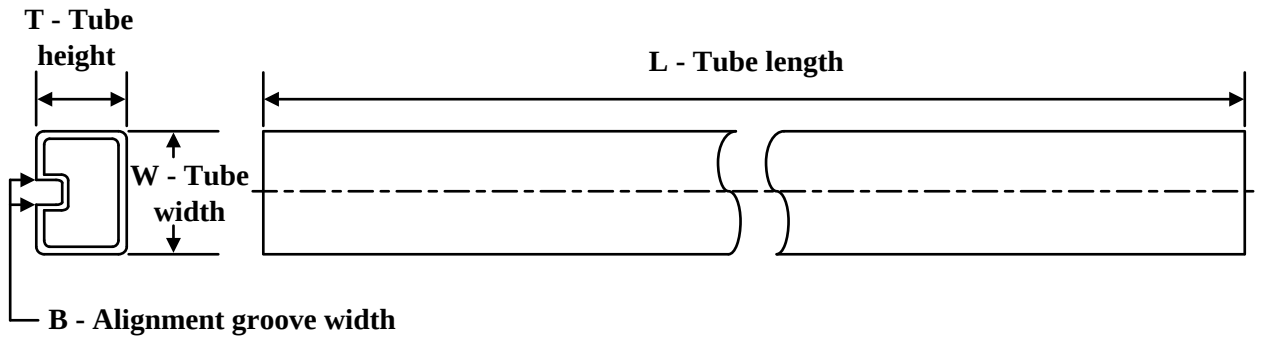
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC341DWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDC341DW	DW	SOIC	20	25	507	12.83	5080	6.6

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