

# SN74LV245A 具有三态输出的八路总线收发器

## 1 特性

- 2V 至 5.5V  $V_{CC}$  运行
- 5V 时  $t_{pd}$  最大值为 6.5 ns
- $V_{OLP}$  (输出接地反弹) 典型值  
小于 0.8V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$  时)
- $V_{OHV}$  (输出  $V_{OH}$  下冲) 典型值  
大于 2.3 V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$  时)
- 支持所有端口上的混合模式电压运行
- $I_{off}$  支持局部断电模式运行
- 闩锁性能超过 250mA, 符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)
  - 1000V 充电器件模型 (C101)

## 2 应用

- 服务器
- LED 显示屏
- 网络交换机
- 电信基础设施
- 电机驱动器
- I/O 扩展器

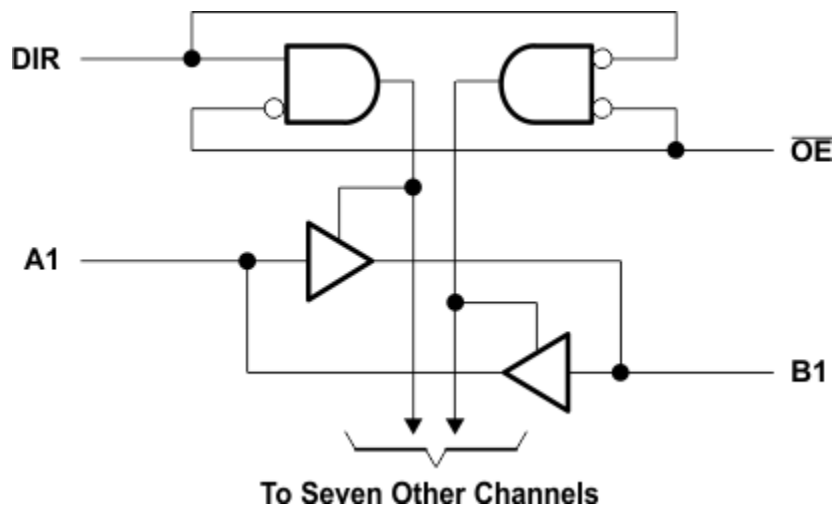
## 3 说明

这些八路总线收发器旨在 2V 至 5.5V  $V_{CC}$  下运行。

### 封装信息<sup>(1)</sup>

| 器件型号       | 封装                            | 封装尺寸 (NOM)       |
|------------|-------------------------------|------------------|
| SN74LV245A | DB (SSOP, 20)                 | 7.20mm × 5.30mm  |
|            | DGV (TVSOP, 20)               | 5.00mm × 4.40mm  |
|            | PW (TSSOP, 20)                | 6.50mm × 4.40mm  |
|            | RGY (VQFN, 20)                | 4.50mm × 3.50mm  |
|            | DW (SOIC, 20)                 | 12.80mm × 7.50mm |
|            | RKS (VQFN, 20) <sup>(2)</sup> | 4.50mm × 2.50mm  |

- (1) 如需了解所有可用封装, 请参阅数据表末尾的封装选项附录。  
 (2) 预发布



简化原理图



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## 4 Revision History

| Changes from Revision O (September 2014) to Revision P (December 2022)                       | Page |
|----------------------------------------------------------------------------------------------|------|
| • 更新了整个文档中的表格、图和交叉参考的编号格式.....                                                               | 1    |
| • 添加了 RKS 封装信息.....                                                                          | 1    |
| Changes from Revision N (August 2012) to Revision O (September 2014)                         | Page |
| • 将文档更新为新的 TI 数据表格式.....                                                                     | 1    |
| • 删除了“订购信息”表.....                                                                            | 1    |
| • 添加了“应用”.....                                                                               | 1    |
| • 添加了“器件信息”表.....                                                                            | 1    |
| • Added Pin Functions table.....                                                             | 3    |
| • Added Handling Ratings table.....                                                          | 4    |
| • Changed MAX operating temperature to 125°C in Recommended Operating Conditions table. .... | 5    |
| • Added - 40°C to 125°C for SN74LV245A in <i>Electrical Characteristics</i> table.....       | 6    |
| • Added - 40°C to 125°C for SN74LV245A in all three Switching Characteristics tables.....    | 6    |
| • Added Typical Characteristics.....                                                         | 8    |
| • Added Application and Implementation section.....                                          | 11   |
| • Added Power Supply Recommendations and Layout sections.....                                | 12   |

## 5 Pin Configuration and Functions

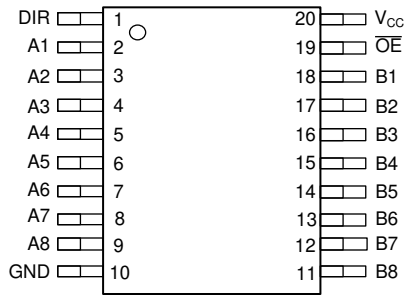


图 5-1. SN74LV245A: DB, DGV, DW, N, NS or PW (Top View)

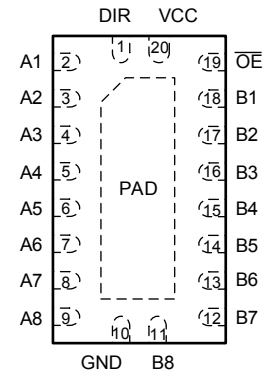


图 5-2. SN74LV245A: RGY or RKS Package, 20-Pin VQFN (Top View)

表 5-1. Pin Functions

| PIN |                 | TYPE <sup>(1)</sup> | DESCRIPTION   |
|-----|-----------------|---------------------|---------------|
| NO. | NAME            |                     |               |
| 1   | DIR             | I                   | Direction Pin |
| 2   | A1              | I/O                 | A1 I/O        |
| 3   | A2              | I/O                 | A2 I/O        |
| 4   | A3              | I/O                 | A3 I/O        |
| 5   | A4              | I/O                 | A4 I/O        |
| 6   | A5              | I/O                 | A5 I/O        |
| 7   | A6              | I/O                 | A6 I/O        |
| 8   | A7              | I/O                 | A7 I/O        |
| 9   | A8              | I/O                 | A8 I/O        |
| 10  | GND             | —                   | Ground Pin    |
| 11  | B8              | I/O                 | B8 I/O        |
| 12  | B7              | I/O                 | B7 I/O        |
| 13  | B6              | I/O                 | B6 I/O        |
| 14  | B5              | I/O                 | B5 I/O        |
| 15  | B4              | I/O                 | B4 I/O        |
| 16  | B3              | I/O                 | B3 I/O        |
| 17  | B2              | I/O                 | B2 I/O        |
| 18  | B1              | I/O                 | B1 I/O        |
| 19  | OE              | I                   | Output Enable |
| 20  | V <sub>CC</sub> | —                   | Power Pin     |

(1) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                                                                             | MIN                                   | MAX                   | UNIT |   |
|-----------------|---------------------------------------------------------------------------------------------|---------------------------------------|-----------------------|------|---|
| V <sub>CC</sub> | Supply voltage range                                                                        | - 0.5                                 | 7                     | V    |   |
| V <sub>I</sub>  | Input voltage range                                                                         | Except I/O ports <sup>(2)</sup>       | - 0.5                 | 7    | V |
|                 |                                                                                             | I/O ports <sup>(2) (3)</sup>          | - 0.5                 | 7    |   |
| V <sub>O</sub>  | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | - 0.5                                 | 7                     | V    |   |
| V <sub>O</sub>  | Output voltage range applied in the high or low state <sup>(2) (3)</sup>                    | - 0.5                                 | V <sub>CC</sub> + 0.5 | V    |   |
| I <sub>IK</sub> | Input clamp current                                                                         | V <sub>I</sub> < 0                    | - 20                  | mA   |   |
| I <sub>OK</sub> | Output clamp current                                                                        | V <sub>O</sub> < 0                    | - 50                  | mA   |   |
| I <sub>O</sub>  | Continuous output current                                                                   | V <sub>O</sub> = 0 to V <sub>CC</sub> | ±35                   | mA   |   |
|                 | Continuous current through V <sub>CC</sub> or GND                                           |                                       | ±70                   | mA   |   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

### 6.2 Handling Ratings

|                    |                           | MIN                                                                                      | MAX | UNIT |   |
|--------------------|---------------------------|------------------------------------------------------------------------------------------|-----|------|---|
| T <sub>stg</sub>   | Storage temperature range | - 65                                                                                     | 150 | °C   |   |
| V <sub>(ESD)</sub> | Electrostatic discharge   | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | 0   | 2000 | V |
|                    |                           | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | 0   | 1000 |   |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    | SN74LV245A                       |                       | UNIT            |
|-----------------|------------------------------------|----------------------------------|-----------------------|-----------------|
|                 |                                    | MIN                              | MAX                   |                 |
| V <sub>CC</sub> | Supply voltage                     | 2                                | 5.5                   | V               |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2 V            | 1.5                   | V               |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.7 |                 |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.7 |                 |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.7 |                 |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2 V            | 0.5                   | V               |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.3 |                 |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.3 |                 |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.3 |                 |
| V <sub>I</sub>  | Input voltage                      | 0                                | 5.5                   | V               |
| V <sub>O</sub>  | Output voltage                     | High or low state                | 0                     | V <sub>CC</sub> |
|                 |                                    | 3-state                          | 0                     | 5.5             |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2 V            | -50                   | μA              |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | -2                    | mA              |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | -8                    |                 |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | -16                   |                 |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V            | 50                    | μA              |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | 2                     | mA              |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | 8                     |                 |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | 16                    |                 |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 2.3 V to 2.7 V | 200                   | ns/V            |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | 100                   |                 |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | 20                    |                 |
| T <sub>A</sub>  | Operating free-air temperature     | -40                              | 125                   | °C              |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LV245A |       |      |      |       |      |      | UNIT |
|-------------------------------|----------------------------------------------|------------|-------|------|------|-------|------|------|------|
|                               |                                              | DB         | DGV   | DW   | NS   | PW    | RGY  | RKS  |      |
|                               |                                              | 20 PINS    |       |      |      |       |      |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 94.6       | 114.8 | 77.5 | 76.6 | 101.5 | 34.1 | 67.7 | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 56.3       | 30.1  | 43.7 | 43.0 | 35.6  | 38.4 | 72.4 |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 49.8       | 56.3  | 45.1 | 44.1 | 52.5  | 12.0 | 40.4 |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 18.3       | 0.9   | 16.9 | 16.7 | 2.2   | 0.8  | 10.3 |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 49.4       | 55.6  | 44.7 | 43.7 | 52.0  | 12.0 | 40.4 |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | —          | —     | —    | —    | —     | 7.1  | 24.1 |      |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS           | V <sub>CC</sub>                                             | - 40°C to 85°C<br>SN74LV245A |     |     | - 40°C to 125°C<br>SN74LV245A |     |     | UNIT |
|------------------|---------------------------|-------------------------------------------------------------|------------------------------|-----|-----|-------------------------------|-----|-----|------|
|                  |                           |                                                             | MIN                          | TYP | MAX | MIN                           | TYP | MAX |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = - 50 μA | 2 V to 5.5 V                                                | V <sub>CC</sub> - 0.1        |     |     | V <sub>CC</sub> - 0.1         |     |     | V    |
|                  | I <sub>OH</sub> = - 2 mA  | 2.3 V                                                       | 2                            |     |     | 2                             |     |     |      |
|                  | I <sub>OH</sub> = - 8 mA  | 3 V                                                         | 2.48                         |     |     | 2.48                          |     |     |      |
|                  | I <sub>OH</sub> = - 16 mA | 4.5 V                                                       | 3.8                          |     |     | 3.8                           |     |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 50 μA   | 2 V to 5.5 V                                                | 0.1                          |     |     | 0.1                           |     |     | V    |
|                  | I <sub>OL</sub> = 2 mA    | 2.3 V                                                       | 0.4                          |     |     | 0.4                           |     |     |      |
|                  | I <sub>OL</sub> = 8 mA    | 3 V                                                         | 0.44                         |     |     | 0.44                          |     |     |      |
|                  | I <sub>OL</sub> = 16 mA   | 4.5 V                                                       | 0.55                         |     |     | 0.55                          |     |     |      |
| I <sub>I</sub>   | Control inputs            | V <sub>I</sub> = 5.5 V or GND                               | 0 to 5.5 V                   |     |     | ±1                            |     |     | μA   |
| I <sub>OZ</sub>  | A or B port               | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V                        |     |     | ±5                            |     |     | μA   |
| I <sub>CC</sub>  |                           | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V                        |     |     | 20                            |     |     | μA   |
| I <sub>off</sub> |                           | V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V               | 0                            |     |     | 5                             |     |     | μA   |
| C <sub>i</sub>   | Control inputs            | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 3.3 V                        |     |     | 3                             |     |     | pF   |
|                  |                           |                                                             | 5 V                          |     |     | 3                             |     |     |      |
| C <sub>io</sub>  | A or B port               | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 3.3 V                        |     |     | 5.5                           |     |     | pF   |
|                  |                           |                                                             | 5 V                          |     |     | 5.5                           |     |     |      |

## 6.6 Switching Characteristics, V<sub>CC</sub> = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [图 7-1](#))

| PARAMETER          | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE       | T <sub>A</sub> = 25°C |      |      | - 40°C to 85°C |     | - 40°C to 125°C |     | UNIT |
|--------------------|--------------|-------------|------------------------|-----------------------|------|------|----------------|-----|-----------------|-----|------|
|                    |              |             |                        | MIN                   | TYP  | MAX  | MIN            | MAX | MIN             | MAX |      |
| t <sub>pd</sub>    | A or B       | B or A      | C <sub>L</sub> = 15 pF |                       | 8.3  | 13   | 1              | 15  | 1               | 17  | ns   |
| t <sub>en</sub>    | OE           | A or B      |                        | 11.8                  | 19.9 | 1    | 22             | 1   | 24              |     |      |
| t <sub>dis</sub>   | OE           | A or B      |                        | 11.8                  | 18.1 | 1    | 20             | 1   | 22              |     |      |
| t <sub>pd</sub>    | A or B       | B or A      | C <sub>L</sub> = 50 pF |                       | 11.2 | 15.9 | 1              | 18  | 1               | 21  | ns   |
| t <sub>en</sub>    | OE           | A or B      |                        | 14.1                  | 22.7 | 1    | 26             | 1   | 28              |     |      |
| t <sub>dis</sub>   | OE           | A or B      |                        | 17.6                  | 23.1 | 1    | 25             | 1   | 27              |     |      |
| t <sub>sk(o)</sub> |              |             |                        |                       |      | 2    |                | 2   |                 |     |      |

### 6.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| PARAMETER   | FROM (INPUT)    | TO (OUTPUT) | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |      |      | $-40^\circ\text{C to } 85^\circ\text{C}$ |      | $-40^\circ\text{C to } 125^\circ\text{C}$ |      | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|------|------|------------------------------------------|------|-------------------------------------------|------|------|
|             |                 |             |                      | MIN                      | TYP  | MAX  | MIN                                      | MAX  | MIN                                       | MAX  |      |
| $t_{pd}$    | A or B          | B or A      | $C_L = 15\text{ pF}$ |                          | 5.9  | 8.4  | 1                                        | 10   | 1                                         | 11   | ns   |
| $t_{en}$    | $\overline{OE}$ | A or B      |                      |                          | 8.2  | 13.2 | 1                                        | 15.5 | 1                                         | 16.5 |      |
| $t_{dis}$   | $\overline{OE}$ | A or B      |                      |                          | 9.6  | 16.5 | 1                                        | 19.5 | 1                                         | 20.5 |      |
| $t_{pd}$    | A or B          | B or A      | $C_L = 50\text{ pF}$ |                          | 7.9  | 11.9 | 1                                        | 13.5 | 1                                         | 14.5 | ns   |
| $t_{en}$    | $\overline{OE}$ | A or B      |                      |                          | 9.9  | 16.7 | 1                                        | 19   | 1                                         | 20   |      |
| $t_{dis}$   | $\overline{OE}$ | A or B      |                      |                          | 13.9 | 19.8 | 1                                        | 22   | 1                                         | 23   |      |
| $t_{sk(o)}$ |                 |             |                      |                          |      |      |                                          | 1.5  |                                           | 1.5  |      |

### 6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

| PARAMETER   | FROM (INPUT)    | TO (OUTPUT) | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |      |      | $-40^\circ\text{C to } 85^\circ\text{C}$ |      | $-40^\circ\text{C to } 125^\circ\text{C}$ |      | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|------|------|------------------------------------------|------|-------------------------------------------|------|------|
|             |                 |             |                      | MIN                      | TYP  | MAX  | MIN                                      | MAX  | MIN                                       | MAX  |      |
| $t_{pd}$    | A or B          | B or A      | $C_L = 15\text{ pF}$ |                          | 4.3  | 5.5  | 1                                        | 6.5  | 1                                         | 7    | ns   |
| $t_{en}$    | $\overline{OE}$ | A or B      |                      |                          | 5.7  | 8.5  | 1                                        | 10   | 1                                         | 10.5 |      |
| $t_{dis}$   | $\overline{OE}$ | A or B      |                      |                          | 7.8  | 12.8 | 1                                        | 14.2 | 1                                         | 14.7 |      |
| $t_{pd}$    | A or B          | B or A      | $C_L = 50\text{ pF}$ |                          | 5.6  | 7.5  | 1                                        | 8.5  | 1                                         | 9    | ns   |
| $t_{en}$    | $\overline{OE}$ | A or B      |                      |                          | 7    | 10.6 | 1                                        | 12   | 1                                         | 12.5 |      |
| $t_{dis}$   | $\overline{OE}$ | A or B      |                      |                          | 10.9 | 14.7 | 1                                        | 16   | 1                                         | 16.5 |      |
| $t_{sk(o)}$ |                 |             |                      |                          |      |      |                                          | 1    |                                           | 1    |      |

### 6.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER   |                                        | SN74LV245A |      |      | UNIT |
|-------------|----------------------------------------|------------|------|------|------|
|             |                                        | MIN        | TYP  | MAX  |      |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |            | 0.5  | 0.8  | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |            | -0.4 | -0.8 | V    |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |            | 2.9  |      | V    |
| $V_{IH(D)}$ | High-level dynamic input voltage       | 2.31       |      |      | V    |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |            |      | 0.99 | V    |

### 6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER |                               |                 | TEST CONDITIONS                            | $V_{CC}$ | TYP | UNIT |
|-----------|-------------------------------|-----------------|--------------------------------------------|----------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | Outputs enabled | $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | 3.3 V    | 20  | pF   |
|           |                               |                 |                                            | 5 V      | 25  |      |

### 6.11 Typical Characteristics

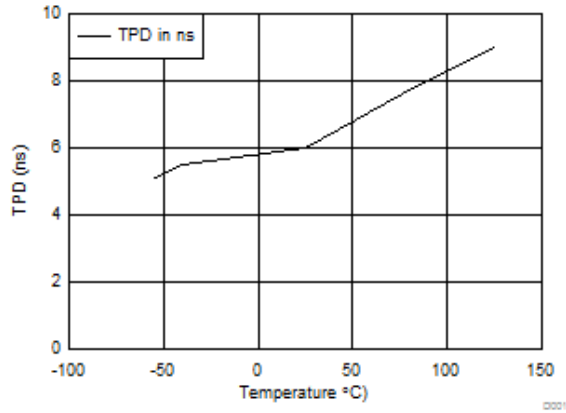


图 6-1. TPD vs Temperature at 3.3 V

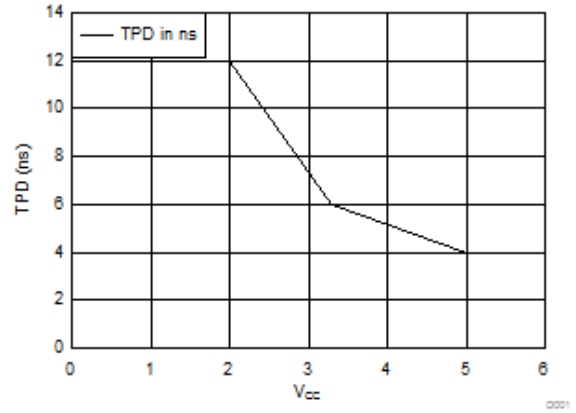
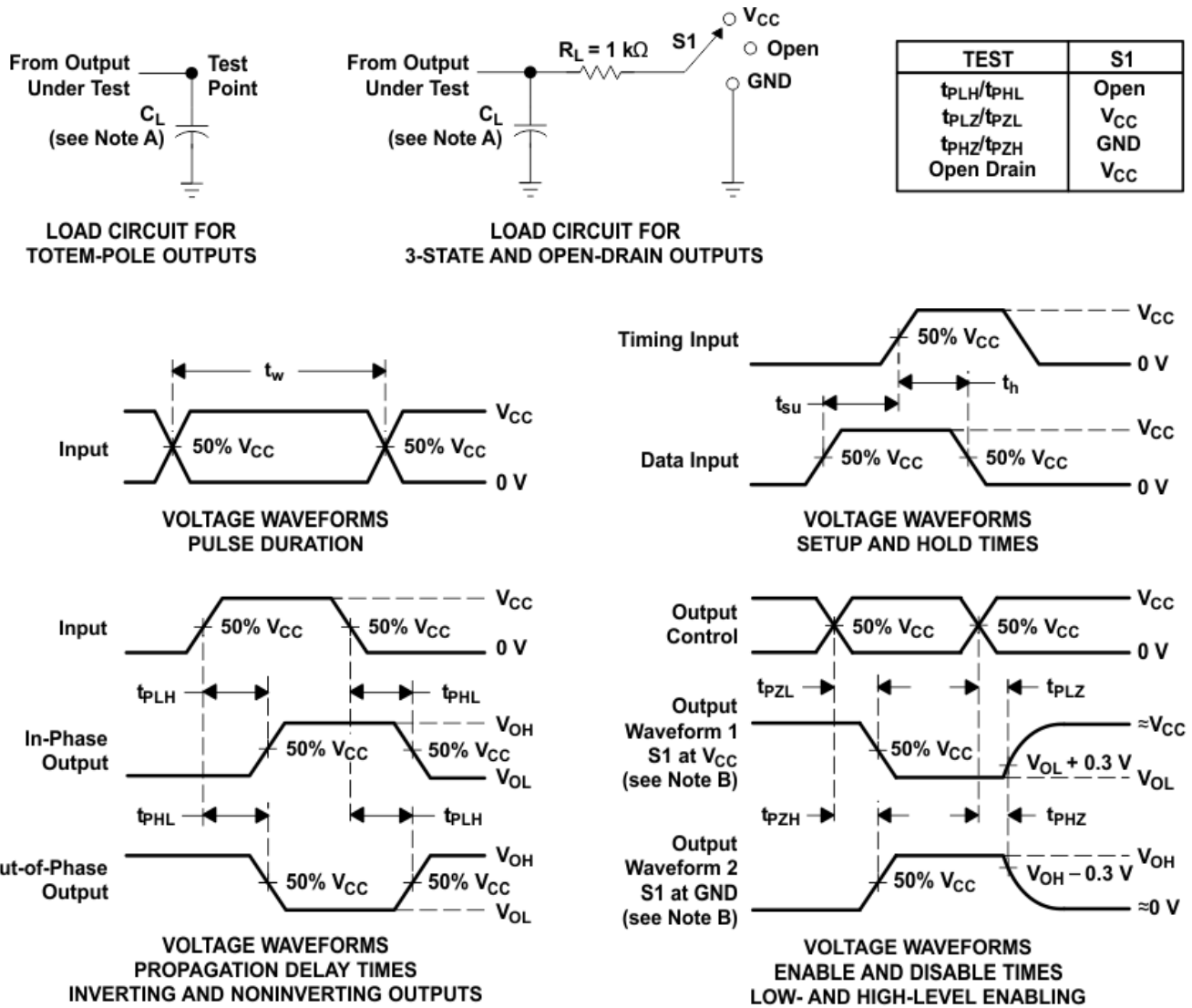


图 6-2. TPD vs V<sub>CC</sub>



## 7 Parameter Measurement Information



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

The SN74LV245A devices are designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### 8.2 Functional Block Diagram

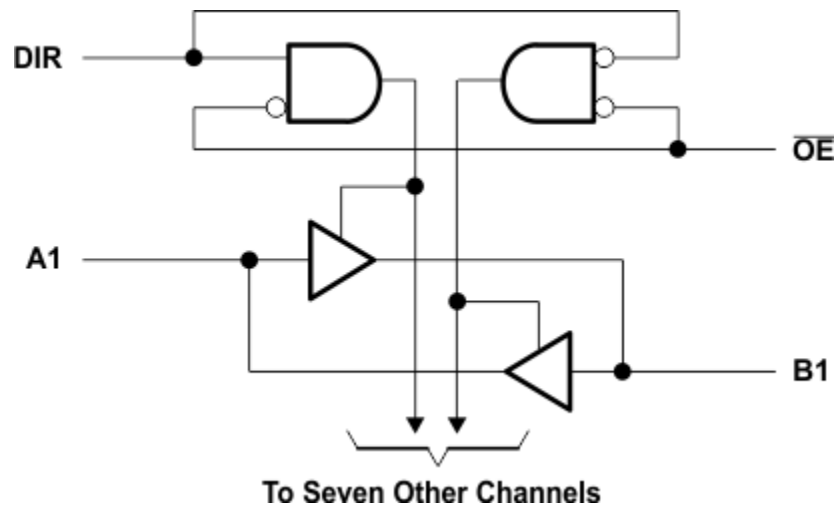


图 8-1. Logic Diagram (Positive Logic)

### 8.3 Feature Description

- Allows down voltage translation from 5 V to 3.3 V
  - Inputs accept voltage levels up to 5.5 V
- Slow edge rates minimize output ringing

### 8.4 Device Functional Modes

表 8-1. Function Table

| INPUTS          |     | OPERATION       |
|-----------------|-----|-----------------|
| $\overline{OE}$ | DIR |                 |
| L               | L   | B data to A bus |
| L               | H   | A data to B bus |
| H               | X   | Isolation       |

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

The SN74LV245A is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid  $V_{CC}$  making the device ideal for down translation.

### 9.2 Typical Application

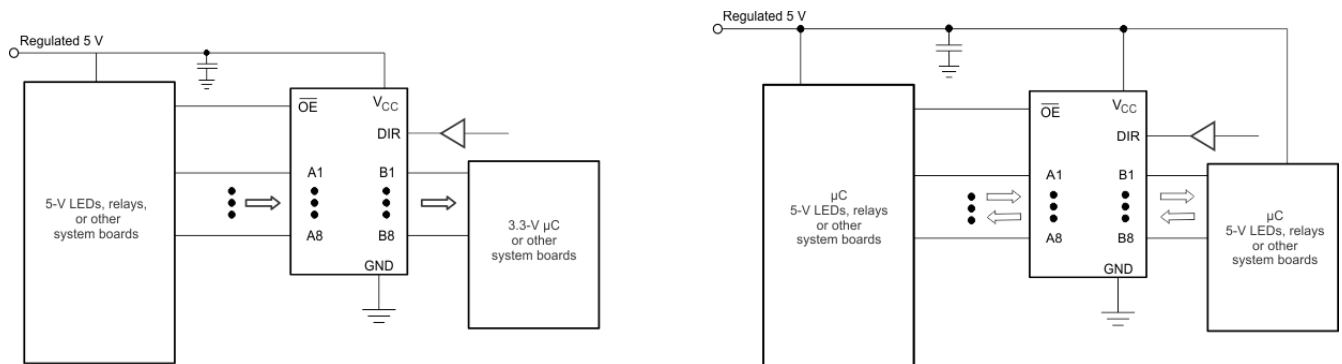


图 9-1. Typical Application Schematic

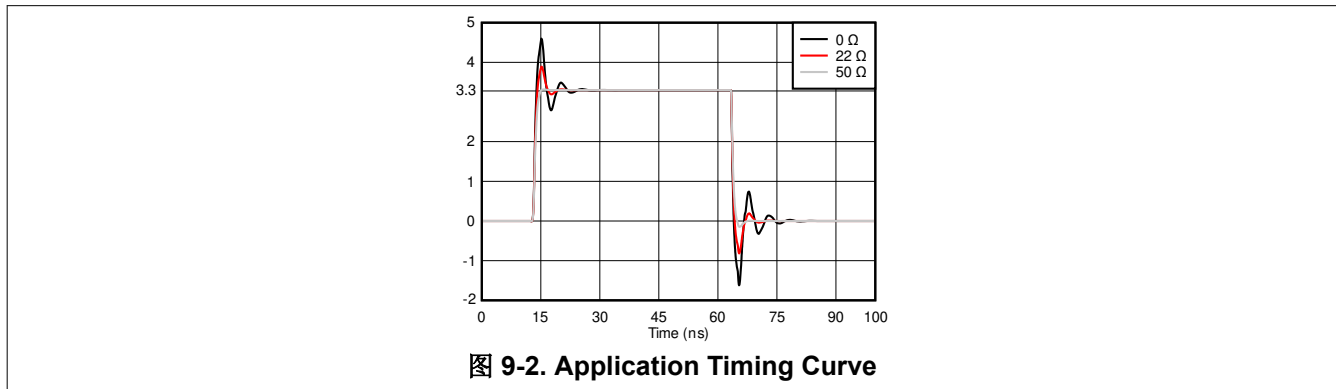
#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention, because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive, but the high drive will also create faster edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Rise time and fall time specifications, see ( $\Delta t / \Delta V$ ) in [Recommended Operating Conditions](#) table.
  - Specified high and low levels, see ( $V_{IH}$  and  $V_{IL}$ ) in [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant, allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
- Recommend output conditions:
  - Load currents should not exceed 35 mA per output and 70 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended and if there are multiple  $V_{CC}$  terminals then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [图 11-1](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they cannot float when disabled.

### 11.2 Layout Example

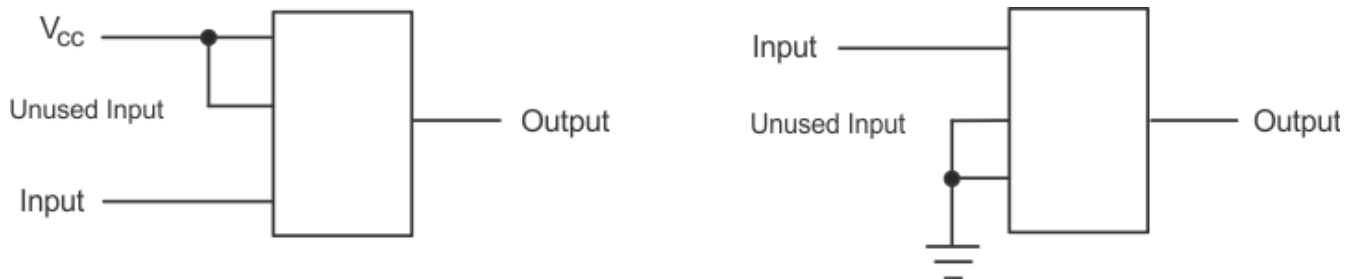


图 11-1. Layout Diagram

## 12 Device and Documentation Support

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 支持资源

**TI E2E™ 支持论坛** 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| PSN74LV245ARKSR  | ACTIVE        | VQFN         | RKS             | 20   | 3000        | TBD             | Call TI                              | Call TI              | -40 to 125   |                         | <a href="#">Samples</a> |
| SN74LV245ADBR    | ACTIVE        | SSOP         | DB              | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV245A                  | <a href="#">Samples</a> |
| SN74LV245ADGVR   | ACTIVE        | TVSOP        | DGV             | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV245A                  | <a href="#">Samples</a> |
| SN74LV245ADW     | ACTIVE        | SOIC         | DW              | 20   | 25          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV245A                  | <a href="#">Samples</a> |
| SN74LV245ADWR    | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV245A                  | <a href="#">Samples</a> |
| SN74LV245ANSR    | ACTIVE        | SO           | NS              | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 74LV245A                | <a href="#">Samples</a> |
| SN74LV245APW     | ACTIVE        | TSSOP        | PW              | 20   | 70          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV245A                  | <a href="#">Samples</a> |
| SN74LV245APWG4   | ACTIVE        | TSSOP        | PW              | 20   | 70          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV245A                  | <a href="#">Samples</a> |
| SN74LV245APWR    | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | LV245A                  | <a href="#">Samples</a> |
| SN74LV245APWRE4  | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV245A                  | <a href="#">Samples</a> |
| SN74LV245APWRG3  | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green    | SN                                   | Level-1-260C-UNLIM   | -40 to 125   | LV245A                  | <a href="#">Samples</a> |
| SN74LV245APWRG4  | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | LV245A                  | <a href="#">Samples</a> |
| SN74LV245ARGYR   | ACTIVE        | VQFN         | RGY             | 20   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | LV245A                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV245ADBR   | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV245ADGVR  | TVSOP        | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV245ADWR   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LV245ANSR   | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74LV245APWR   | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LV245APWR   | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74LV245APWRG3 | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74LV245APWRG4 | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74LV245ARGYR  | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.8     | 4.8     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV245ADBR   | SSOP         | DB              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV245ADGVR  | TVSOP        | DGV             | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV245ADWR   | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LV245ANSR   | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LV245APWR   | TSSOP        | PW              | 20   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LV245APWR   | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV245APWRG3 | TSSOP        | PW              | 20   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LV245APWRG4 | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV245ARGYR  | VQFN         | RGY             | 20   | 3000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LV245ADW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74LV245APW   | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| SN74LV245APWG4 | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GENERIC PACKAGE VIEW

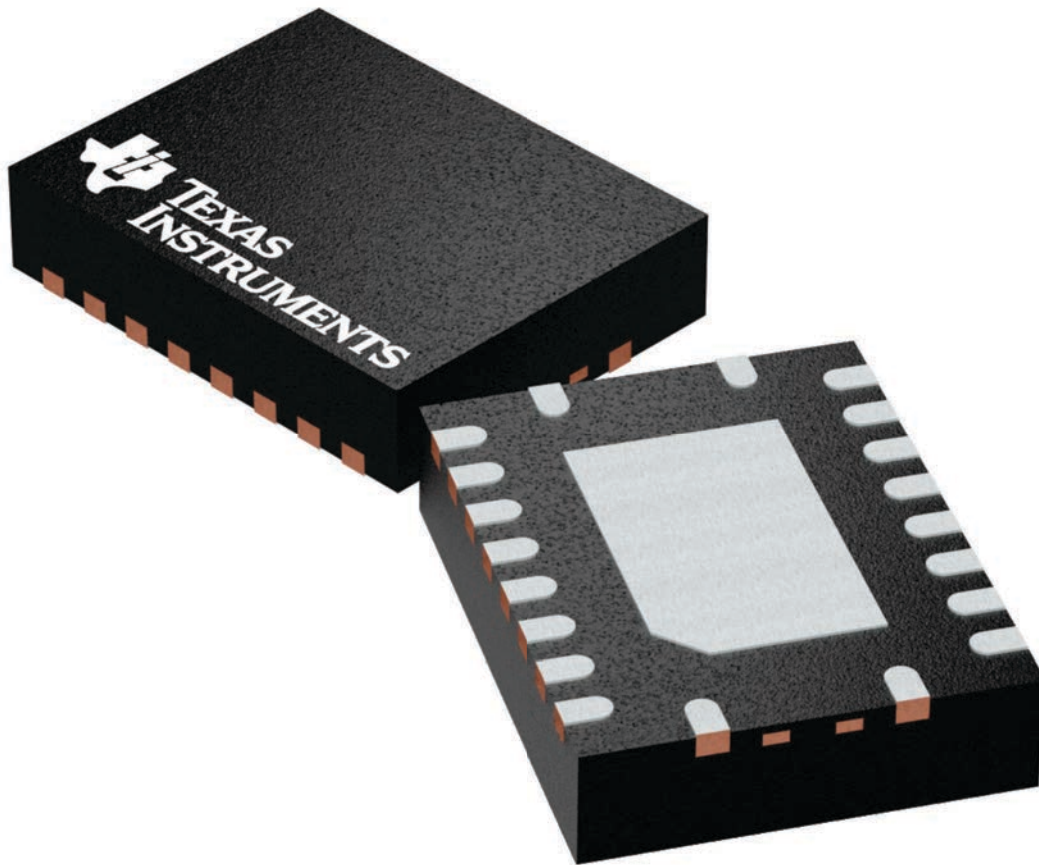
**RGY 20**

**VQFN - 1 mm max height**

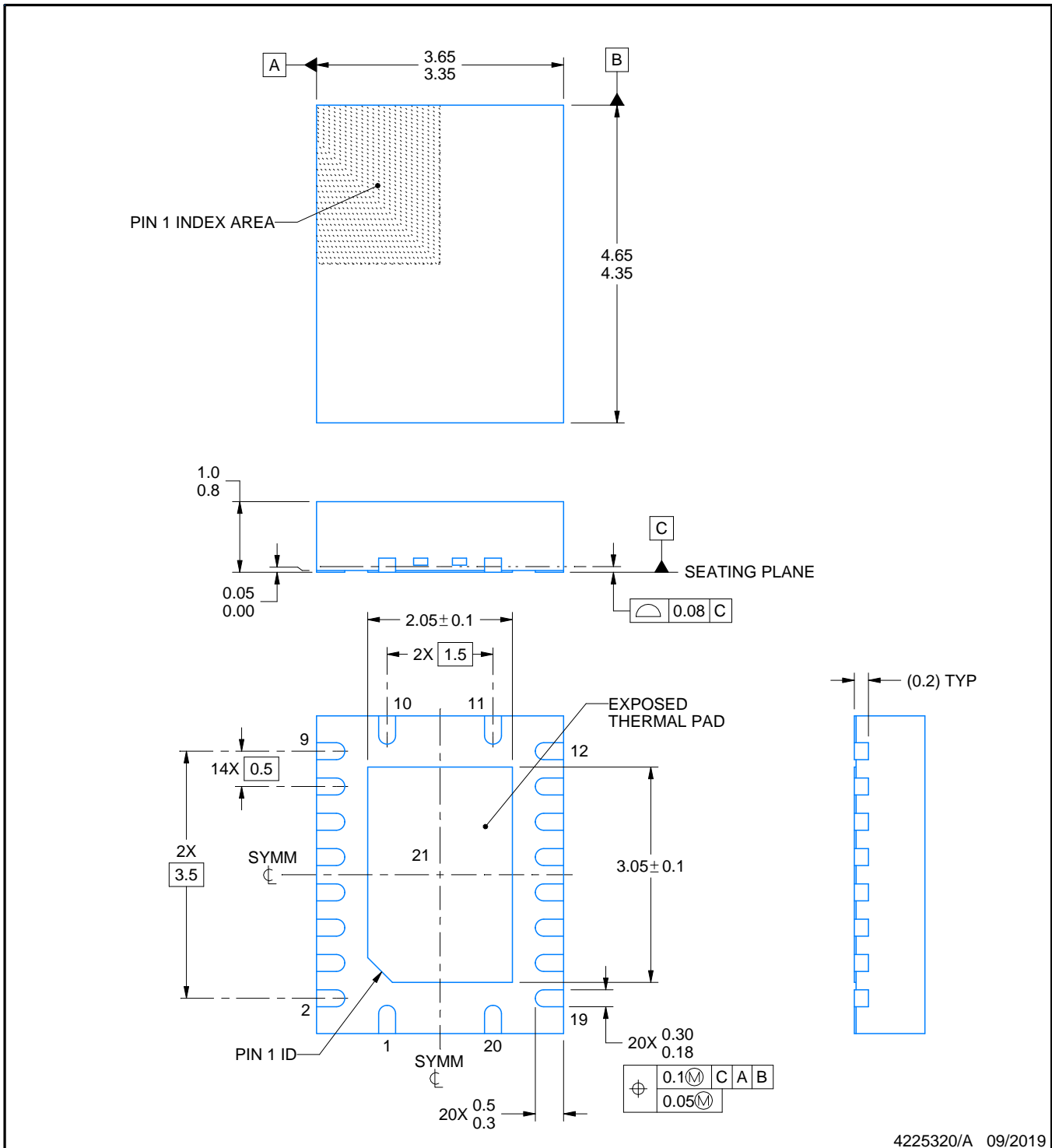
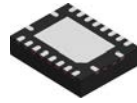
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

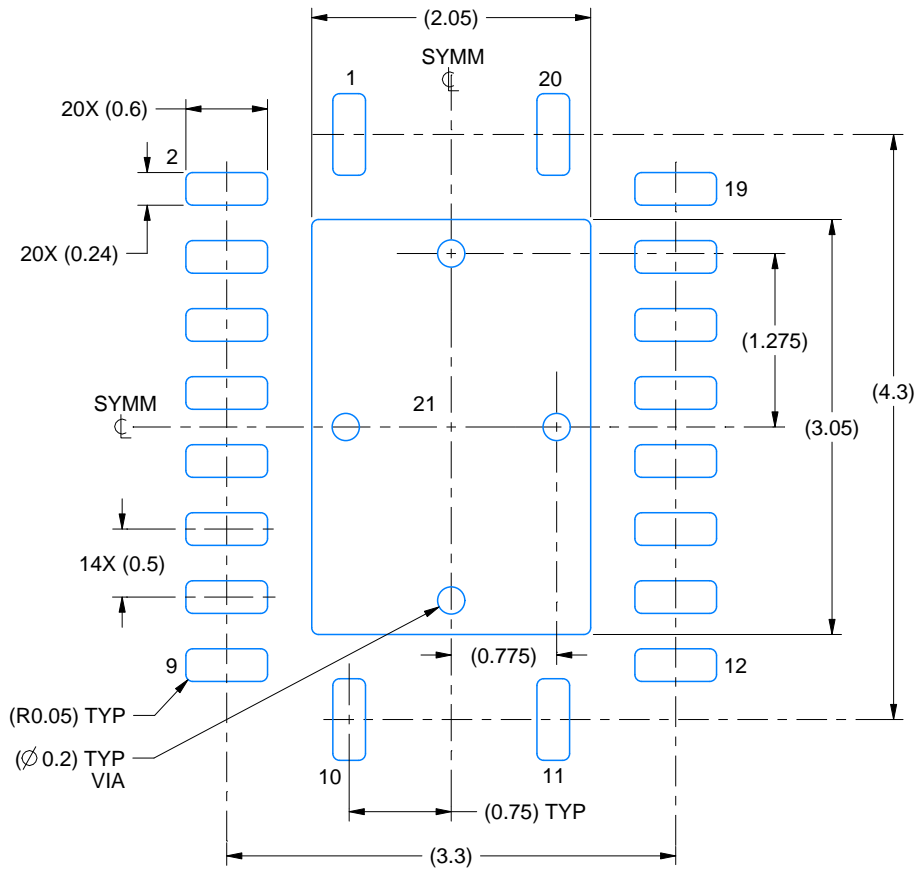
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

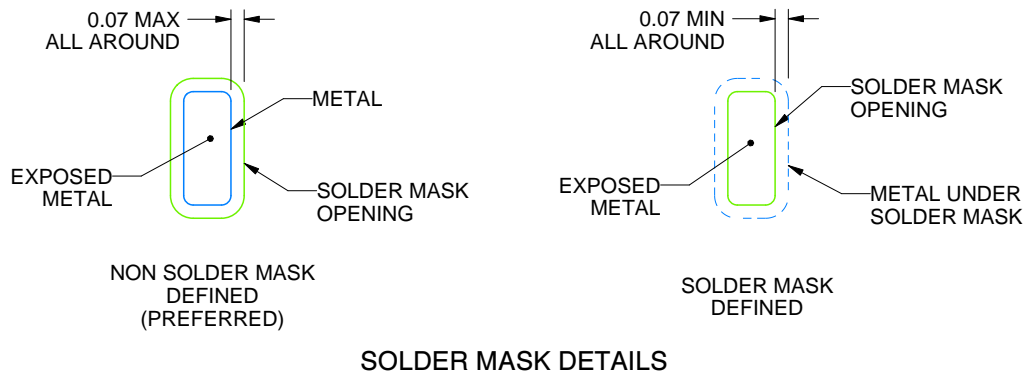
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:18X



**SOLDER MASK DETAILS**

4225320/A 09/2019

NOTES: (continued)

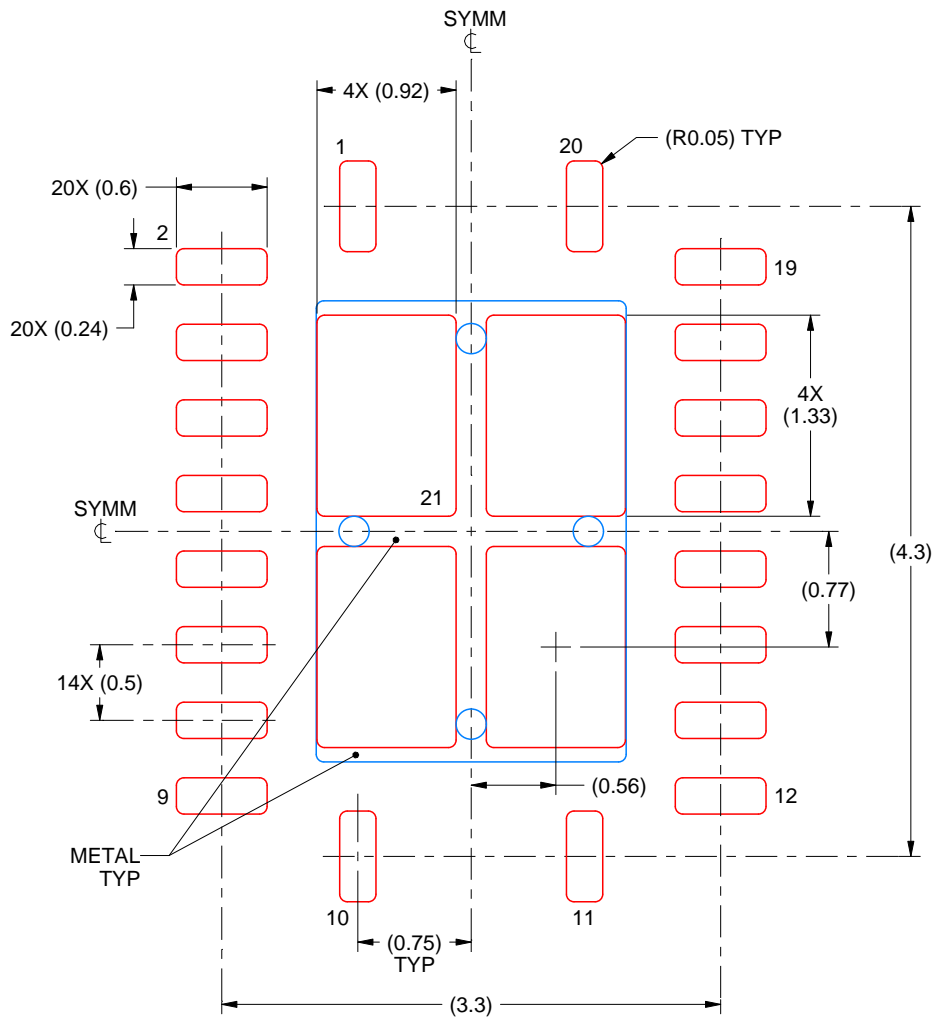
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



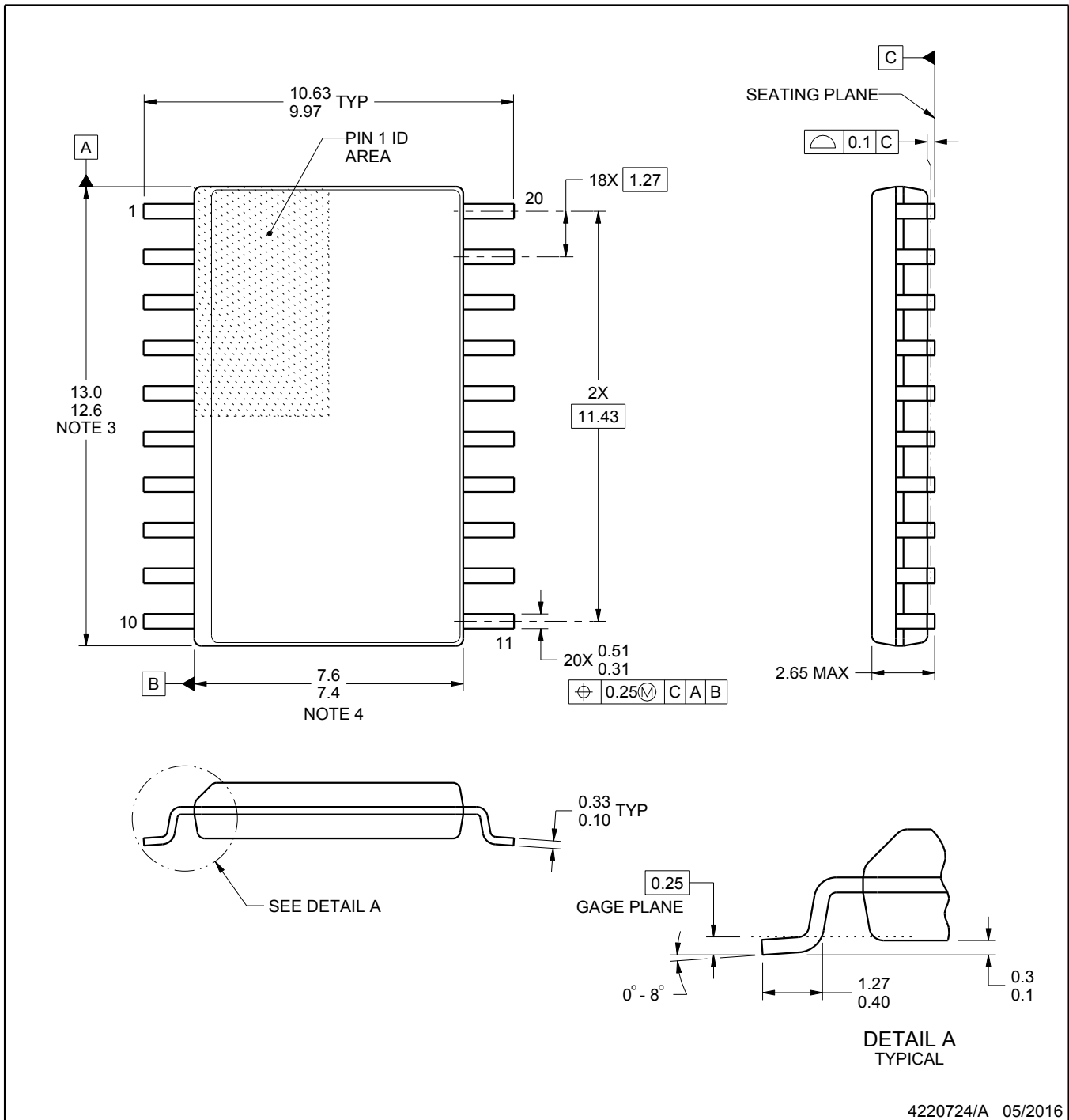
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

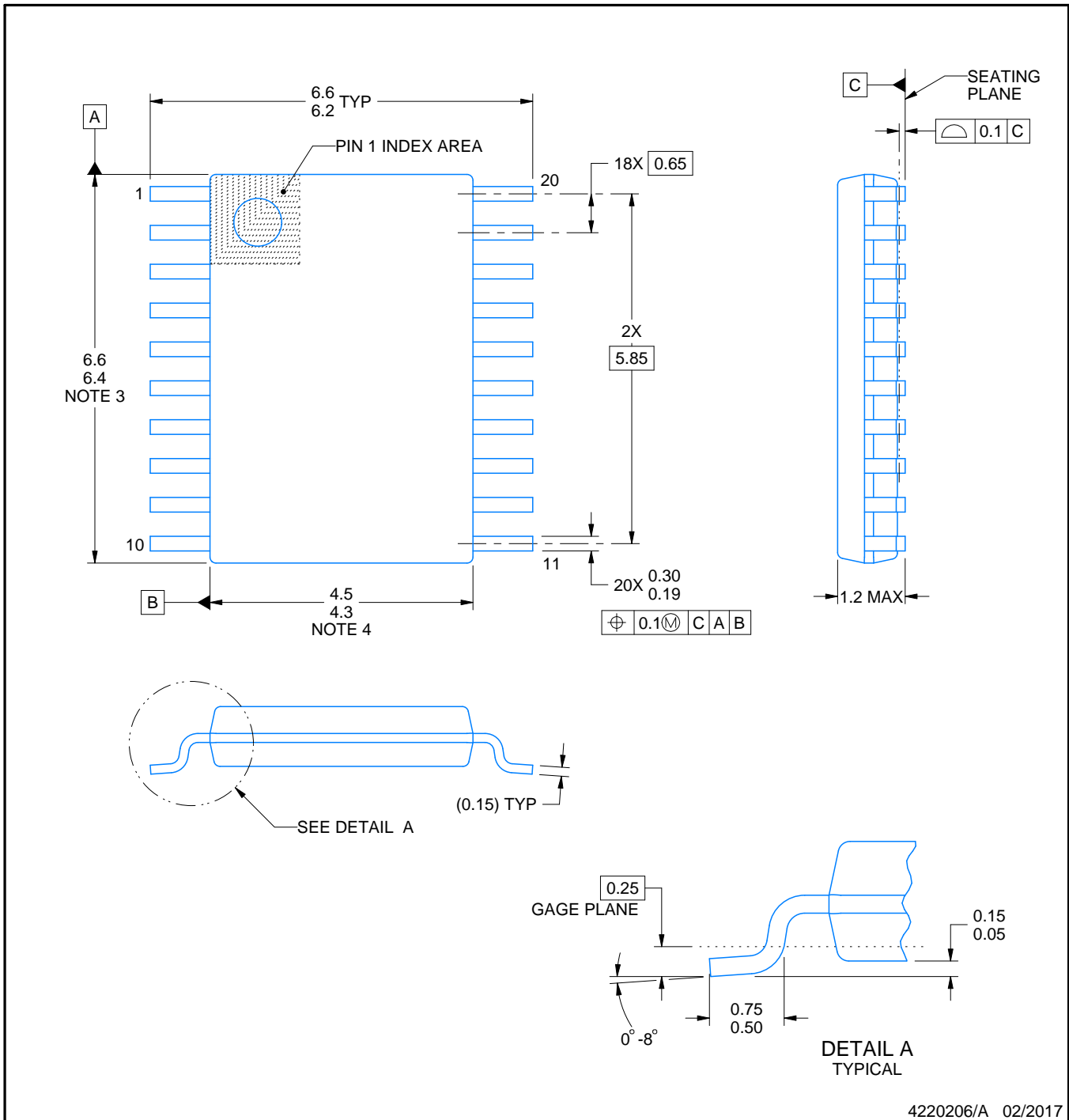
PW0020A



# PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



# EXAMPLE BOARD LAYOUT

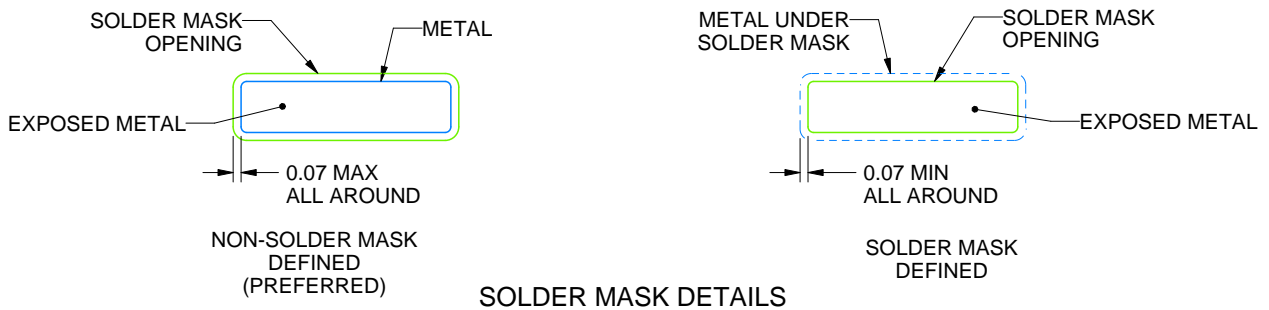
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

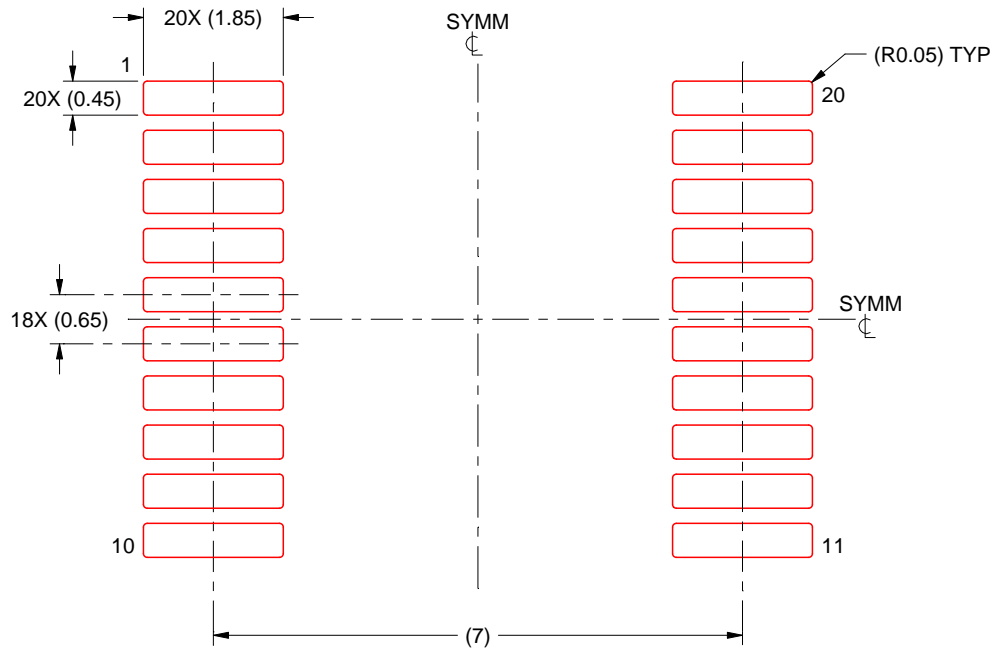
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

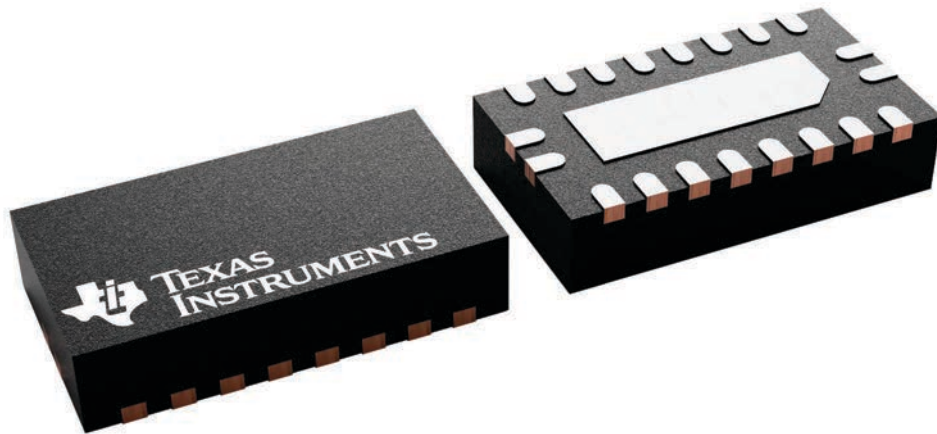
**RKS 20**

**VQFN - 1 mm max height**

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226872/A

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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