- **Members of the Texas Instruments**
  ***Widebus*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design
  Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per
  MIL-STD-883, Method 3015; Exceeds 200 V
  Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per
  JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce)
  < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up
  and Power Down**
- **Distributed V_{CC} and GND Pin Configuration
  Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB
  Layout**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic 300-mil
  Shrink Small-Outline (DL) Package and
  380-mil Fine-Pitch Ceramic Flat (WD)
  Package Using 25-mil Center-to-Center
  Spacings**

**SN54ABT16841 . . . WD PACKAGE
SN74ABT16841 . . . DL PACKAGE
(TOP VIEW)**

1$\overline{OE}$	1	56	1LE
1Q1	2	55	1D1
1Q2	3	54	1D2
GND	4	53	GND
1Q3	5	52	1D3
1Q4	6	51	1D4
V_{CC}	7	50	V_{CC}
1Q5	8	49	1D5
1Q6	9	48	1D6
1Q7	10	47	1D7
GND	11	46	GND
1Q8	12	45	1D8
1Q9	13	44	1D9
1Q10	14	43	1D10
2Q1	15	42	2D1
2Q2	16	41	2D2
2Q3	17	40	2D3
GND	18	39	GND
2Q4	19	38	2D4
2Q5	20	37	2D5
2Q6	21	36	2D6
V_{CC}	22	35	V_{CC}
2Q7	23	34	2D7
2Q8	24	33	2D8
GND	25	32	GND
2Q9	26	31	2D9
2Q10	27	30	2D10
2$\overline{OE}$	28	29	2LE
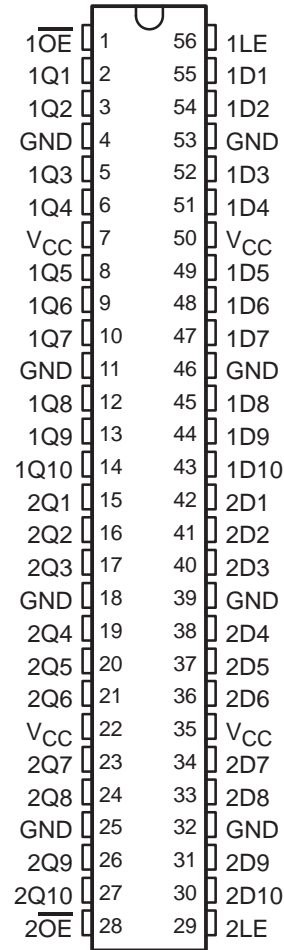
description

These 20-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ABT16841 can be used as two 10-bit latches or one 20-bit latch. The 20 transparent D-type latches provide true data at the outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (1$\overline{OE}$ or 2$\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

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description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16841 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16841 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 10-bit latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol[†]
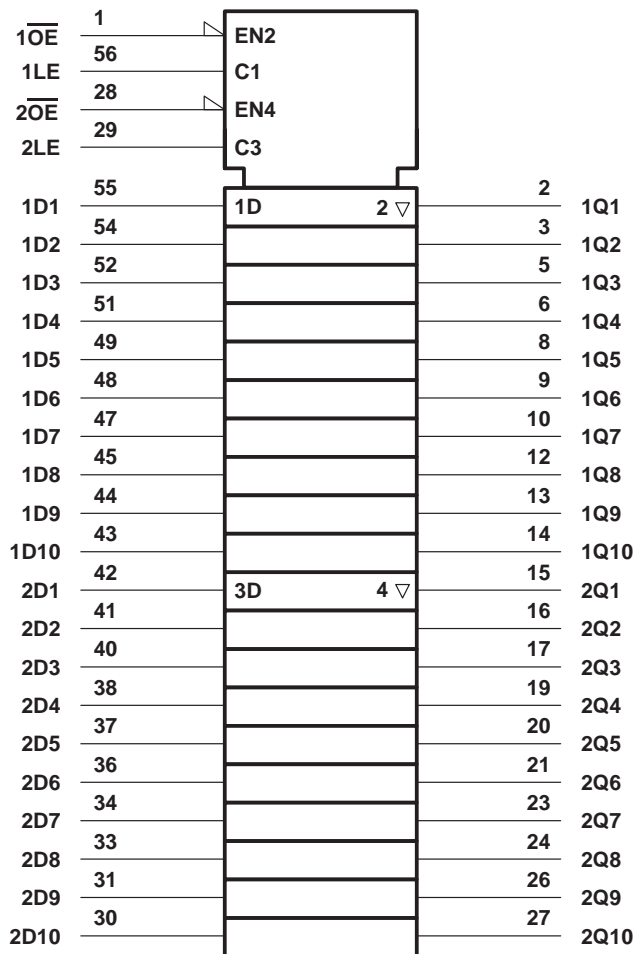
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)

To Nine Other Channels   **To Nine Other Channels**
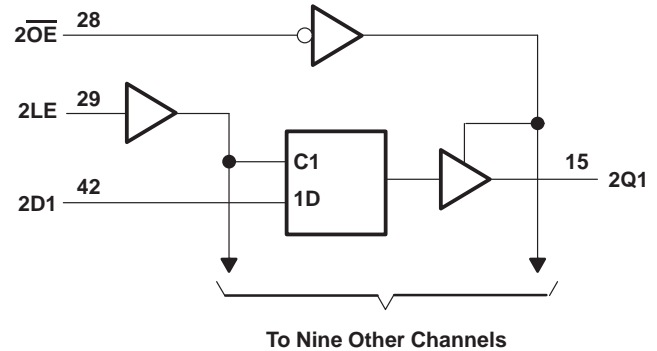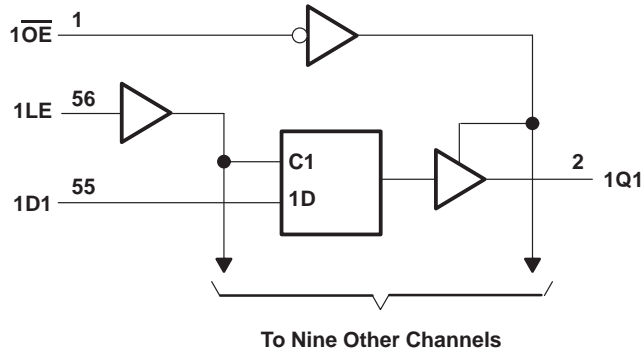
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16841 .... 96 mA
                                                                SN74ABT16841 .... 128 mA
Input clamp current, I_{IK} (V_I < 0) .... –18 mA
Output clamp current, I_{OK} (V_O < 0) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DL package .... 74°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
        2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABT16841		SN74ABT16841		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$			SN54ABT16841		SN74ABT16841		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = −3 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = −24 mA	2			2				
			I_{OH} = −32 mA	2*					2		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55*				0.55	
V_{hys}					100						mV
I_I		V_{CC} = 0 to 5.5 V, V_I = V_{CC} or GND				±1				±1	μA
		V_{CC} = 5 V, V_I = V_{CC} or GND						±5			
I_{OZPU}‡		V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50		±50	μA
I_{OZPD}‡		V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50		±50	μA
I_{OZH}		V_{CC} = 2.1 V to 5.5 V, V_O = 2.7 V, $\overline{OE}$ ≥ 2 V				10		10		10	μA
I_{OZL}		V_{CC} = 2.1 V to 5.5 V, V_O = 0.5 V, $\overline{OE}$ ≥ 2 V				−10		−10		−10	μA
I_{off}		V_{CC} = 0, V_I or V_O ≤ 4.5 V				±100				±100	μA
I_{CEX}	Outputs high	V_{CC} = 5.5 V, V_O = 5.5 V				50		50		50	μA
I_O§		V_{CC} = 5.5 V, V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	Outputs high	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND				0.5		0.5			mA
	Outputs low					89		89		89	
	Outputs disabled					0.5		0.5		0.5	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i		V_I = 2.5 V or 0.5 V			3.5						pF
C_o		V_O = 2.5 V or 0.5 V			7.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ This parameter is characterized, but not production tested.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ABT16841				UNIT
		V_{CC} = 5 V, $T_A = 25°C$		MIN	MAX	
		MIN	MAX			
t_w	Pulse duration, LE high or low	4		4		ns
t_{su}	Setup time, data before LE↓	3		3		ns
t_h	Hold time, data after LE↓	2.6		2.6		ns

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN74ABT16841				UNIT
		V_{CC} = 5 V, T_A = 25°C		MIN	MAX	
		MIN	MAX			
t_w	Pulse duration, LE high or low	4		4		ns
t_{su}	Setup time, data before LE↓	1		1		ns
t_h	Hold time, data after LE↓	2		2		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16841					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.1	3.2	4.3	1.1	5.7	ns
t_{PHL}			1.6	3.5	4.5	1.6	5.3	
t_{PLH}	LE	Q	1.1	3.2	4.4	1.1	5.6	ns
t_{PHL}			1.6	3.4	5	1.6	5.5	
t_{PZH}	$\overline{OE}$	Q	1.2	3.2	4.7	1.2	5.8	ns
t_{PZL}			1.7	3.6	5	1.7	5.7	
t_{PHZ}	$\overline{OE}$	Q	2.2	4.1	6.6	2.2	7.7	ns
t_{PLZ}			1.9	4.4	5.8	1.2	8.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16841					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.1	3.2	4.3	1.1	5	ns
t_{PHL}			1.6	3.5	4.5	1.6	5.1	
t_{PLH}	LE	Q	1.1	3.2	4.4	1.1	5	ns
t_{PHL}			1.6	3.4	4.6	1.6	5	
t_{PZH}	$\overline{OE}$	Q	1.2	3.2	4.7	1.2	5.7	ns
t_{PZL}			1.7	3.6	5	1.7	5.6	
t_{PHZ}	$\overline{OE}$	Q	2.2	4.1	5.7	2.2	6.5	ns
t_{PLZ}			1.9	4.4	5.8	1.9	7.1	

PARAMETER MEASUREMENT INFORMATION

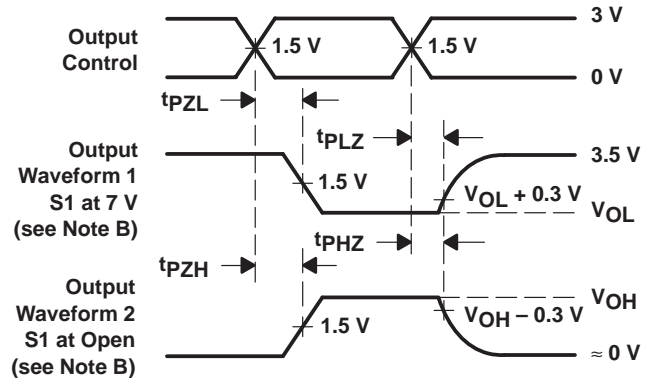| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

VOLTAGE WAVEFORMS
PULSE DURATION
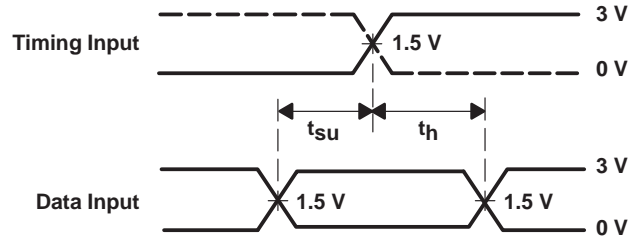
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
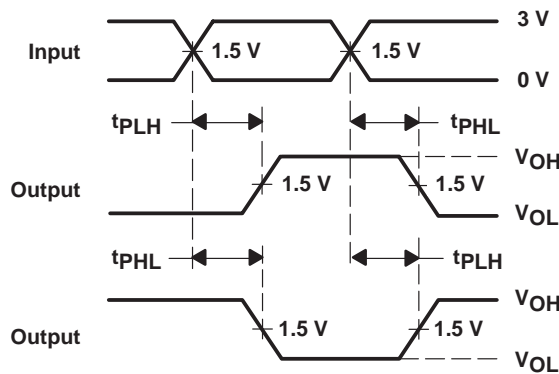
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT16841DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16841	Samples
SN74ABT16841DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16841	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16841DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16841DLR	SSOP	DL	56	1000	367.0	367.0	55.0

PACKAGE MATERIALS INFORMATION

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABT16841DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R−PDSO−G56)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

$\dfrac{0.0135\ (0,343)}{0.008\ (0,203)}$

⊕ | 0.005 (0,13) Ⓜ

56   29

$\dfrac{0.420\ (10,67)}{0.395\ (10,03)}$

$\dfrac{0.010\ (0,25)}{0.005\ (0,13)}$

$\dfrac{0.299\ (7,59)}{0.291\ (7,39)}$

Gage Plane

0.010 (0,25)

1   28

0°−8°

$\dfrac{0.730\ (18,54)}{0.720\ (18,29)}$

$\dfrac{0.040\ (1,02)}{0.020\ (0,51)}$

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ | 0.004 (0,10)

4040048−4/F 05/13

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MO−118

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