

SN54HC191-DIE 4 位同步加/减二进制计数器

1 特性

- 宽工作电压范围
- 低功耗
- 低输入电流
- 单条加/减计数控制线路
- 前瞻电路提高了级联计数器的速度
- 计数模式下的完全同步
- 异步可预先设定的负载控制

2 说明

SN54HC191-DIE 是一款 4 位同步，可逆的，加/减二进制计数器。通过使所有触发电路同时计时来提供同步计数运行，这样，当控制计数方向的逻辑电路发出指令时，输出变化相互间保持一致。这个运行模式消除了通常与异步（纹波时钟）计数器相关的输出计数尖峰。

如果计数-使能 (\overline{CTEN}) 输入为低位，四个触发电路的输出在时钟 (CLK) 输入从低电平向高电平转换时触发。 \overline{CTEN} 位于高位时禁止计数操作。计数的方向由向下/向上 (D/\overline{U}) 输入的电平决定。当 D/\overline{U} 为低位时，计数器作加计数，而当 D/\overline{U} 为高位时，计数器作减计数。

这些计数器特有一个完全独立的时钟电路。改变运行模式的控制 (\overline{CTEN} 和 D/\overline{U}) 输入上的变化对于计数器在计时发生前的内容没有影响。计数器的功能只能由符合稳定设置和保持时间要求的条件控制。

这些计数器是完全可编程的；也就是说，通过在负载 (\overline{LOAD}) 输入上放置一个低电平，并且在数据输入上敲入所需的数据可将每个输出预先设定为其中任一电平。输出变化为与数据输入一致，而这一变化与 CLK 电平无关。这个特性使这些计数器可被用作模块化 N 驱动器，只需用预先设定的输入修改计数长度。

可提供两个输出来执行级联功能：纹波时钟 (\overline{RCO}) 和最大/最小 (MAX/MIN) 计数。在计数为零（所有输出低电平）下计数，或者最大（9 或 15）上计数时，MAX/MIN 产生一个持续时间大致等于一个完整时钟周期的高电平输出脉冲。 \overline{RCO} 在同样的条件下产生一个低电平输出脉冲，但仅限于 CLK 为低位的情况下。如果使用并行计时，可通过将 \overline{RCO} 馈入随后计数器的 \overline{CTEN} 来轻松实现计数器级联，或者在使用并行启用时馈入 CLK 来实现计数器级联。MAX/MIN 可为高速运行提供前瞻性。

Ordering Information⁽¹⁾

| PRODUCT | PACKAGE DESIGNATOR | PACKAGE | ORDERABLE PART NUMBER | PACKAGE QUANTITY |
|-----------|--------------------|----------------------------------------|-----------------------|------------------|
| SN54HC191 | TD | Bare die in waffle pack ⁽²⁾ | SN54HC191TDE1 | 154 |
| | | | SN54HC191TDE2 | 10 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Processing is per the Texas Instruments space production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.



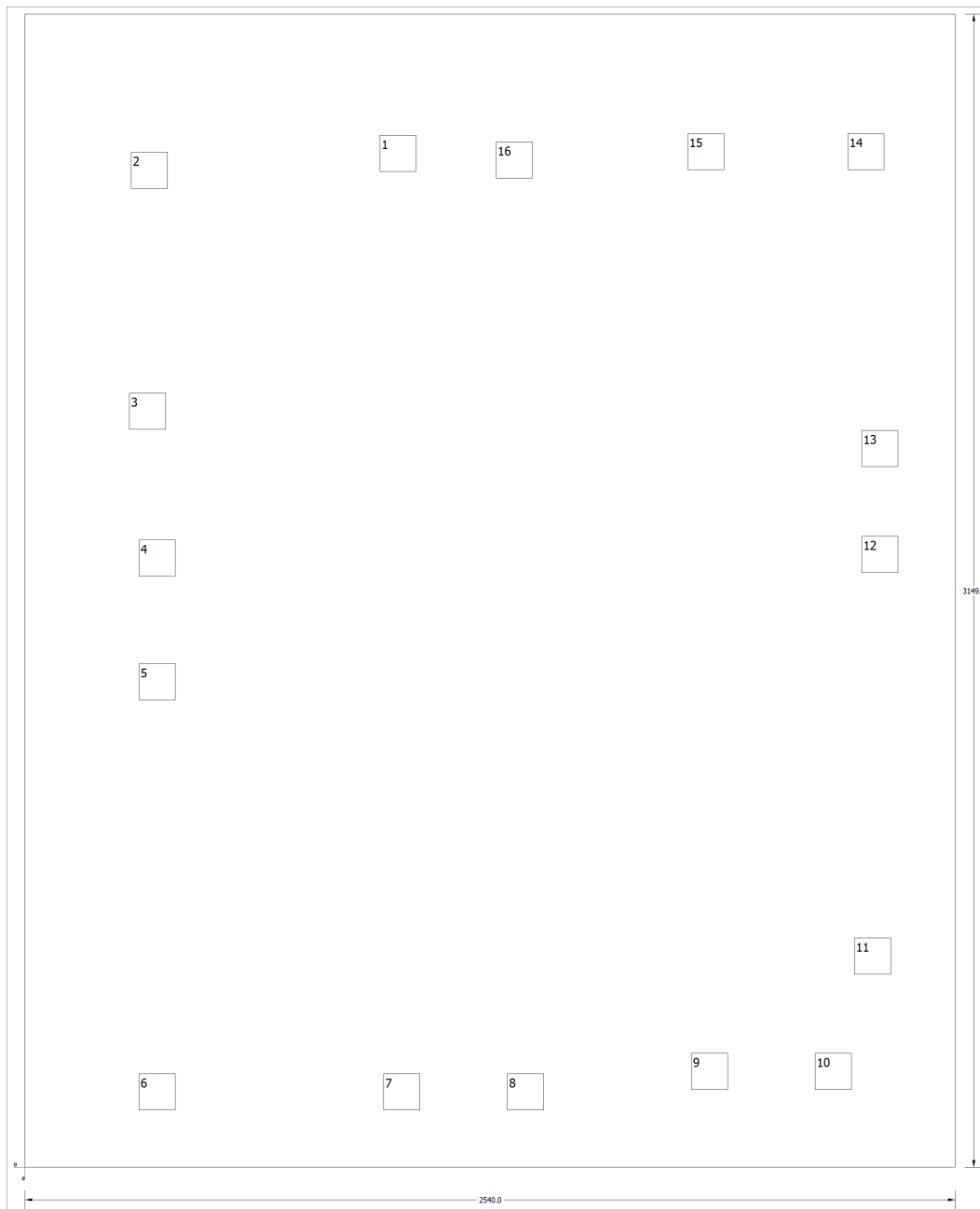


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

3 Bare Die Information

| DIE THICKNESS | BACKSIDE FINISH | BACKSIDE POTENTIAL | BOND PAD METALLIZATION COMPOSITION | BOND PAD THICKNESS |
|---------------|------------------------|--------------------|------------------------------------|--------------------|
| 10.5 mils. | Silicon with backgrind | Floating | TiW/AlCu2% | 1199 nm |



Bond Pad Coordinates in Microns

| DESCRIPTION | PAD NUMBER | X MIN | Y MIN | X MAX | Y MAX |
|-------------------------------|------------|----------|----------|----------|----------|
| B | 1 | 968.527 | 2718.587 | 1068.553 | 2818.613 |
| QB | 2 | 290.347 | 2672.867 | 390.373 | 2772.893 |
| QA | 3 | 285.267 | 2015.007 | 385.293 | 2115.033 |
| $\overline{\text{CTEN}}$ | 4 | 310.667 | 1613.687 | 410.693 | 1713.713 |
| $\text{D}\overline{\text{U}}$ | 5 | 310.667 | 1275.867 | 410.693 | 1375.893 |
| QC | 6 | 310.667 | 155.727 | 410.693 | 255.753 |
| QD | 7 | 978.687 | 155.727 | 1078.713 | 255.753 |
| GND | 8 | 1316.507 | 155.727 | 1416.533 | 255.753 |
| D | 9 | 1819.427 | 211.607 | 1919.453 | 311.633 |
| C | 10 | 2157.247 | 211.607 | 2257.273 | 311.633 |
| $\overline{\text{LOAD}}$ | 11 | 2263.927 | 526.567 | 2363.953 | 626.593 |
| MAX/MIN | 12 | 2284.247 | 1623.847 | 2384.273 | 1723.873 |
| $\overline{\text{RCO}}$ | 13 | 2284.247 | 1913.407 | 2384.273 | 2013.433 |
| CLK | 14 | 2246.147 | 2723.667 | 2346.173 | 2823.693 |
| A | 15 | 1809.267 | 2723.667 | 1909.293 | 2823.693 |
| VCC | 16 | 1286.027 | 2700.807 | 1386.053 | 2800.833 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN54HC191TDE1 | ACTIVE | | | 0 | 154 | RoHS & Green | Call TI | N / A for Pkg Type | 25 to 25 | | Samples |
| SN54HC191TDE2 | ACTIVE | | | 0 | 10 | RoHS & Green | Call TI | N / A for Pkg Type | 25 to 25 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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