SNx4HCT244 具有三态输出的八路缓冲器和线路驱动器

1 特性

- 4.5V 至 5.5V 的工作电压范围
- 高电流输出可驱动多达 15 个 LSTTL 负载
- 低功耗：最大 80μA I_{CC}
- t_{pd} 典型值 = 13ns
- ±6mA 输出驱动（电压为 5V 时）
- 低输入电流，最大值为 1μA
- 输入兼容 TTL 电压
- 三态输出驱动总线和缓冲存储器地址寄存器

2 应用

- 服务器
- 发光二极管 (LED) 显示屏
- 网络交换机
- 电信基础设施
- 电机驱动器
- I/O 扩展器

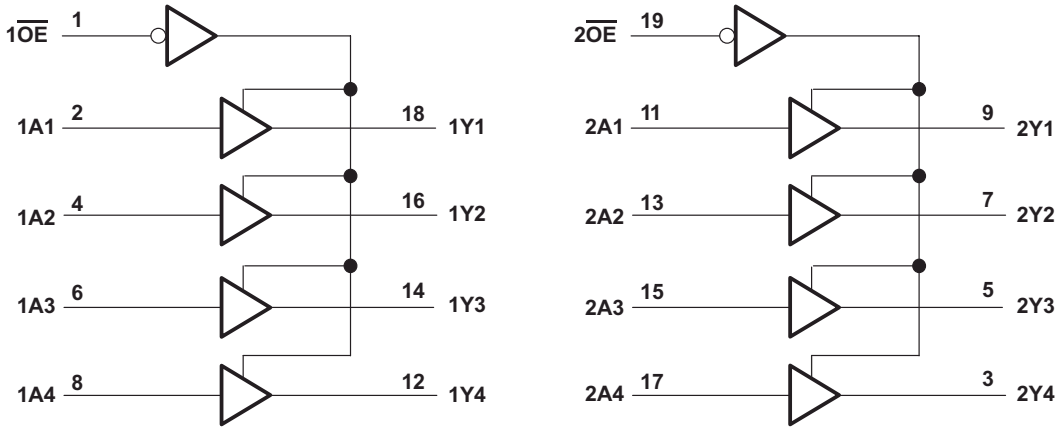
3 说明

这些八路缓冲器和线路驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发送器的性能和密度。SNx4HCT244 器件配备两个具有独立输出使能 ($\overline{OE}$) 输入的 4 位缓冲器或驱动器。当 $\overline{OE}$ 为低电平时，该器件将来自 A 输入的同相数据传递到 Y 输出。当 $\overline{OE}$ 为高电平时，输出处于高阻态。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
SN74HCT244	DB（SSOP，20）	7.20mm × 5.30mm
	DW（SOIC，20）	12.80mm × 7.50mm
	N（PDIP，20）	24.33mm × 6.35mm
	NS（SO，20）	12.60mm × 5.30mm
	PW（TSSOP，20）	6.50mm × 4.40mm
	DGS（VSSOP，20）	5.10mm × 3.00mm
SN54HCT244	J（CDIP，20）	24.20mm × 6.92mm
	FK（LCCC，20）	8.89mm × 8.89mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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逻辑图（正逻辑）

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Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (May 2022) to Revision G (December 2022) — **Page**

- 添加了 DGS (SOT) 封装信息 1
- Added DGS (SOT) package information 3
- Added DGS (SOT) package thermal information 5

Changes from Revision E (August 2016) to Revision F (May 2022) — **Page**

- Junction-to-ambient thermal resistance values increased. DW was 76.6 is now 109.1, DB was 89.4 is now 122.7, N was 44.8 is now 84.6, NS was 71.8 is now 113.4, PW was 97.4 is now 131.8 5

Changes from Revision D (August 2013) to Revision E (August 2016) — **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 删除了*订购信息* 表；请参阅数据表末尾的 POA 1
- Changed *Thermal Information* table 5
- Added ESD warning 9

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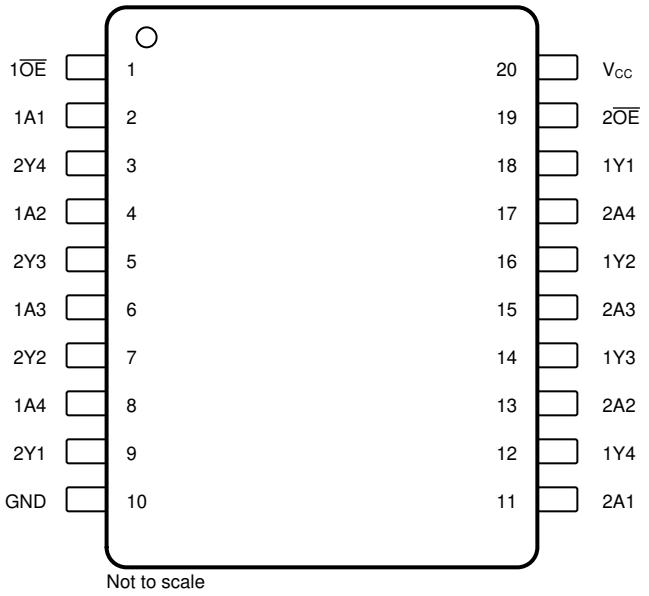
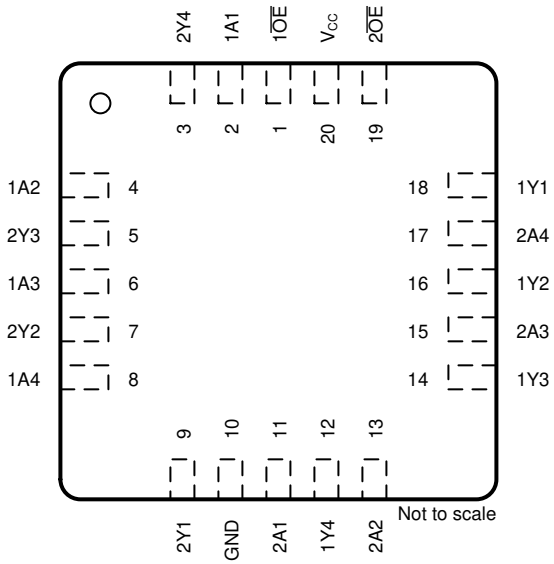
5 Pin Configuration and Functions



J, W, DB, DW, N, NS, PW or DGS Packages 20-Pin CDIP, CFP, SSOP, SOIC, PDIP, SO, TSSOP or VSSOP Top View



FK Package 20-Pin LCCC Top View

Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	1 $\overline{OE}$	I	Output enable
2	1A1	I	Input
3	2Y4	O	Output
4	1A2	I	Input
5	2Y3	O	Output
6	1A3	I	Input
7	2Y2	O	Output
8	1A4	I	Input
9	2Y1	O	Output
10	GND	—	Ground
11	2A1	I	Input
12	1Y4	O	Output
13	2A2	I	Input
14	1Y3	O	Output
15	2A3	I	Input
16	1Y2	O	Output
17	2A4	I	Input
18	1Y1	O	Output
19	2 $\overline{OE}$	I	Output enable
20	V_{CC}	—	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous channel current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
SN74HCT244 in DB, DW, N, NS, or PW package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
SN54HCT244 in J, W, or FK package				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time				500	ns
T_A	Operating free-air temperature	SN54HCT244	–55		125	°C
		SN74HCT244	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

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6.4 Thermal Information

THERMAL METRIC		SN74HCT244						UNIT
		DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	DGS (VSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	109.1	122.7	84.6	113.4	131.8	130.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76	81.6	72.5	78.6	72.2	68.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	77.5	65.3	78.4	82.8	85.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	51.5	46.1	55.3	47.1	21.5	10.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.1	77.1	65.2	78.1	82.4	85.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = – 20 µA	T_A = 25°C	4.5 V	4.4	4.499		V
			SN54HCT244		4.4			
			SN74HCT244		4.4			
		I_{OH} = – 6 mA	T_A = 25°C		3.98	4.3		
			SN54HCT244		3.7			
			SN74HCT244		3.84			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	T_A = 25°C	4.5 V		0.001	0.1	V
			SN54HCT244				0.1	
			SN74HCT244				0.1	
		I_{OL} = 6 mA	T_A = 25°C			0.17	0.26	
			SN54HCT244				0.4	
			SN74HCT244				0.33	
I_I	$V_I = V_{CC}$ or 0	T_A = 25°C		5.5 V		±0.1	±100	nA
		SN54HCT244					±1000	
		SN74HCT244					±1000	
I_{OZ}	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or V_{IL}	T_A = 25°C		5.5 V		±0.01	±0.5	µA
		SN54HCT244					±10	
		SN74HCT244					±5	
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0	T_A = 25°C		5.5 V			8	µA
		SN54HCT244					160	
		SN74HCT244					80	
ΔI_{CC} (1)	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}	T_A = 25°C		5.5 V		1.4	2.4	mA
		SN54HCT244					3	
		SN74HCT244					2.9	

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over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_i	T_A = 25°C	4.5 V to 5.5 V		3	10	pF
	SN54HCT244				10	
	SN74HCT244				10	

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.6 Switching Characteristics: C_L = 50 pF

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	4.5 V	T_A = 25°C		15	28	ns
				SN54HCT244			42	
				SN74HCT244			35	
			5.5 V	T_A = 25°C		13	25	
				SN54HCT244			38	
				SN74HCT244			32	
t_{en}	$\overline{OE}$	Y	4.5 V	T_A = 25°C		21	35	ns
				SN54HCT244			53	
				SN74HCT244			44	
			5.5 V	T_A = 25°C		19	32	
				SN54HCT244			48	
				SN74HCT244			40	
t_{dis}	$\overline{OE}$	Y	4.5 V	T_A = 25°C		19	35	ns
				SN54HCT244			53	
				SN74HCT244			44	
			5.5 V	T_A = 25°C		18	32	
				SN54HCT244			48	
				SN74HCT244			40	
t_t		Y	4.5 V	T_A = 25°C		8	12	ns
				SN54HCT244			18	
				SN74HCT244			15	
			5.5 V	T_A = 25°C		7	11	
				SN54HCT244			16	
				SN74HCT244			14	

6.7 Switching Characteristics: C_L = 150 pF

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	4.5 V	T_A = 25°C		21	45	ns
				SN54HCT244			68	
				SN74HCT244			56	
			5.5 V	T_A = 25°C		18	40	
				SN54HCT244			61	
				SN74HCT244			51	

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over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en}	$\overline{OE}$	Y	4.5 V	T_A = 25°C		25	52	ns
				SN54HCT244			79	
				SN74HCT244			65	
			5.5 V	T_A = 25°C		22	47	
				SN54HCT244			71	
				SN74HCT244			59	
t_t		Y	4.5 V	T_A = 25°C		17	42	ns
				SN54HCT244			63	
				SN74HCT244			53	
			5.5 V	T_A = 25°C		14	38	
				SN54HCT244			57	
				SN74HCT244			48	

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer or driver	No load	40	pF

6.9 Typical Characteristics

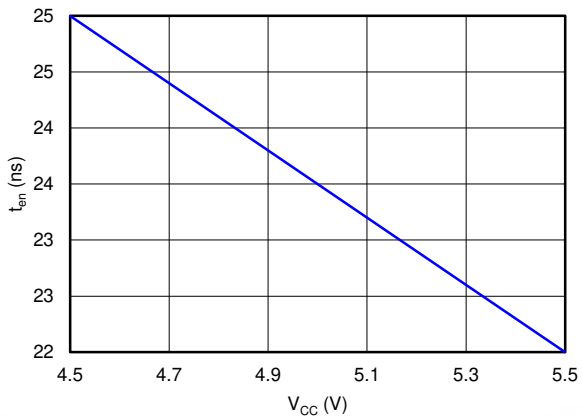
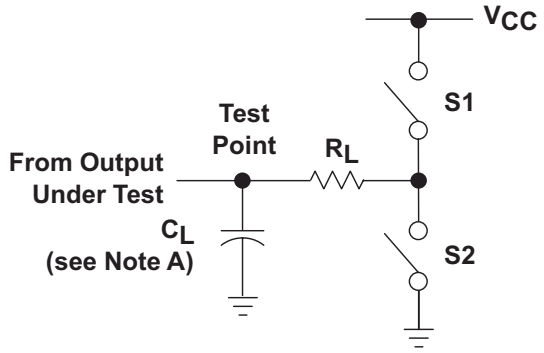


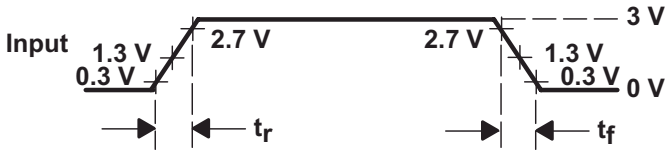
图 6-1. Enable Time vs V_{CC}

7 Parameter Measurement Information

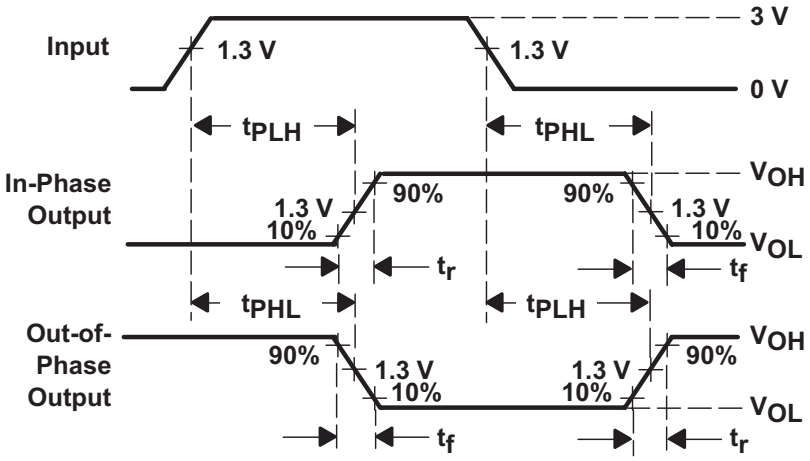


LOAD CIRCUIT

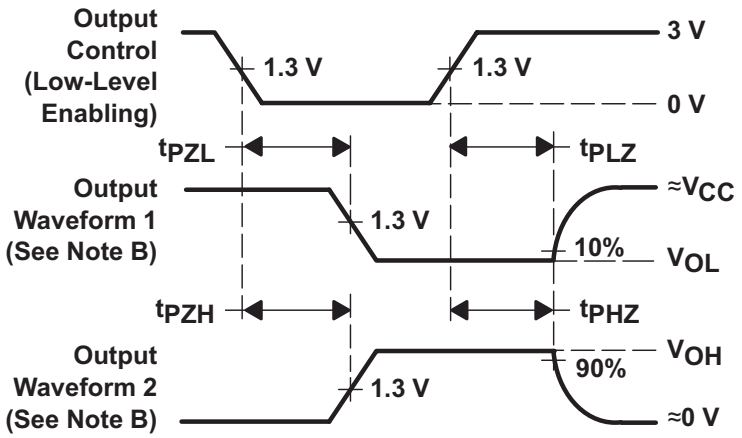
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

图 7-1. Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

The SNx4HCT244 device is organized as two 4-bit buffers and line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram

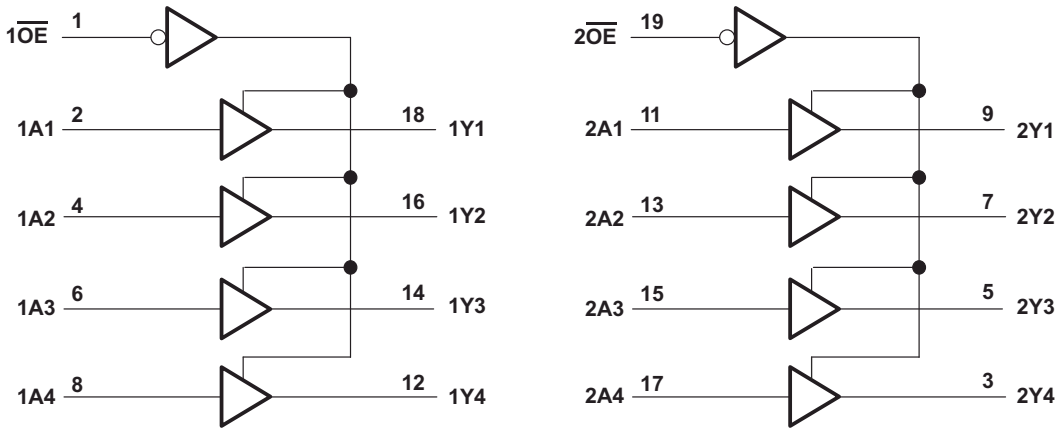

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图 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The SN74HCT244 device can drive up to 15 LSTTL loads. This device has low power consumption of 80-µA I_{CC}. The SN74HCT244 also has 3 state outputs that allow the outputs to go to high impedance, low or high.

8.4 Device Functional Modes

表 8-1 lists the functions of the SNx4HC244.

表 8-1. Function Table

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The SN74HC244 is a high-drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

9.2 Typical Application

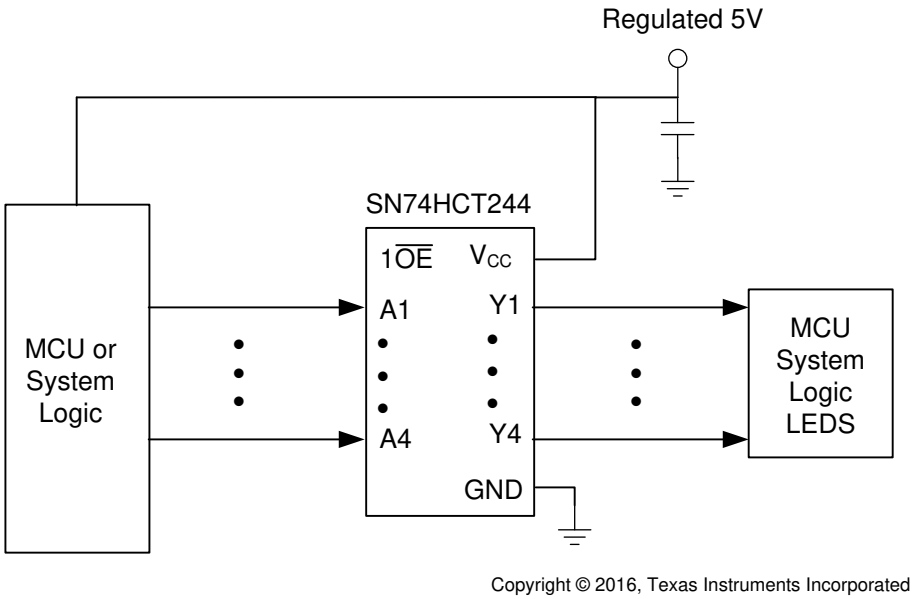

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图 9-1. Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For rise time and fall time specifications, see $\Delta t/\Delta V$ in *Recommended Operating Conditions*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
2. Recommend output conditions:
   - Load currents must not exceed the I_O maximum per output and must not exceed the continuous current through V_{CC} or GND total current for the part. These limits are located in *Absolute Maximum Ratings*.
   - Outputs must not be pulled above V_{CC}.

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9.2.3 Application Curve

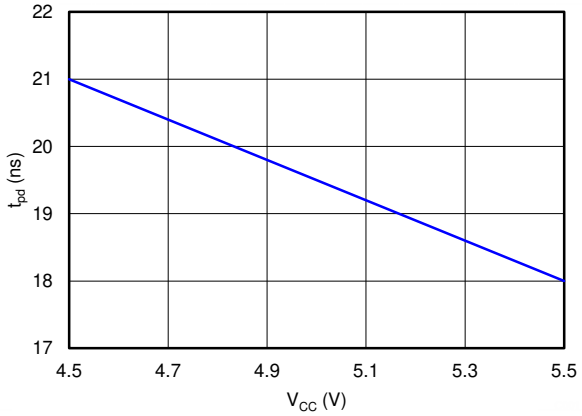

图 9-2. Propagation Delay vs V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor. If there are multiple V_{CC} terminals, then TI recommends 0.01-µF or 0.022-µF capacitors for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input and gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 图 11-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient.

11.2 Layout Example

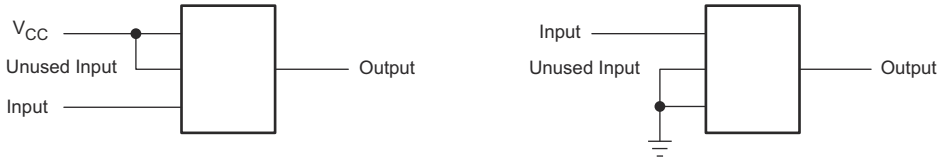

图 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HCT244	Click here	Click here	Click here	Click here	Click here
SN74HCT244	Click here	Click here	Click here	Click here	Click here

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8513001VRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8513001VR A SNV54HCT244J	Samples
5962-8513001VSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8513001VS A SNV54HCT244W	Samples
85130012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85130012A SNJ54HCT 244FK	Samples
8513001RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8513001RA SNJ54HCT244J	Samples
JM38510/65755B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65755B2A	Samples
JM38510/65755BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65755BRA	Samples
M38510/65755B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65755B2A	Samples
M38510/65755BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65755BRA	Samples
SN54HCT244J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HCT244J	Samples
SN74HCT244DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT244	Samples
SN74HCT244DGSR	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HT244	Samples
SN74HCT244DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	Samples
SN74HCT244DWE4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	Samples
SN74HCT244DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	Samples
SN74HCT244DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	Samples
SN74HCT244DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	Samples
SN74HCT244DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT244N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT244N	Samples
SN74HCT244NE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT244N	Samples
SN74HCT244NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT244	Samples
SN74HCT244PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT244	Samples
SN74HCT244PWE4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT244	Samples
SN74HCT244PWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT244	Samples
SN74HCT244PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HT244	Samples
SN74HCT244PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT244	Samples
SN74HCT244PWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT244	Samples
SNJ54HCT244FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85130012A SNJ54HCT 244FK	Samples
SNJ54HCT244J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8513001RA SNJ54HCT244J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HCT244, SN54HCT244-SP, SN74HCT244 :

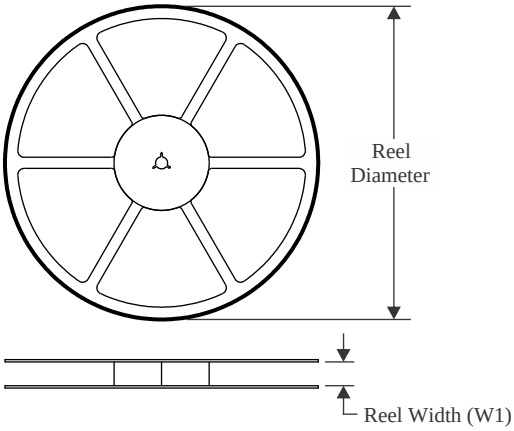
- Catalog : SN74HCT244, SN54HCT244
- Automotive : SN74HCT244-Q1, SN74HCT244-Q1
- Enhanced Product : SN74HCT244-EP, SN74HCT244-EP
- Military : SN54HCT244
- Space : SN54HCT244-SP

NOTE: Qualified Version Definitions:

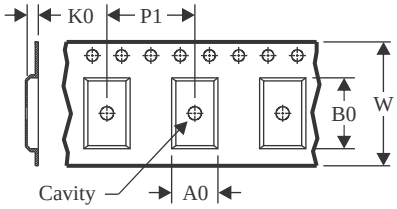
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

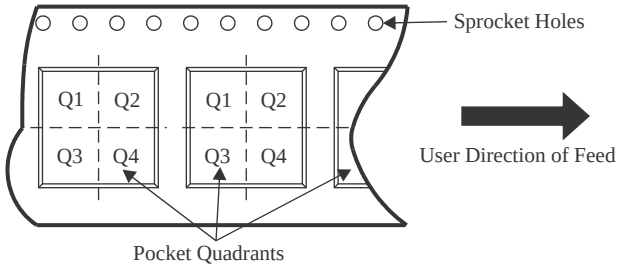


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

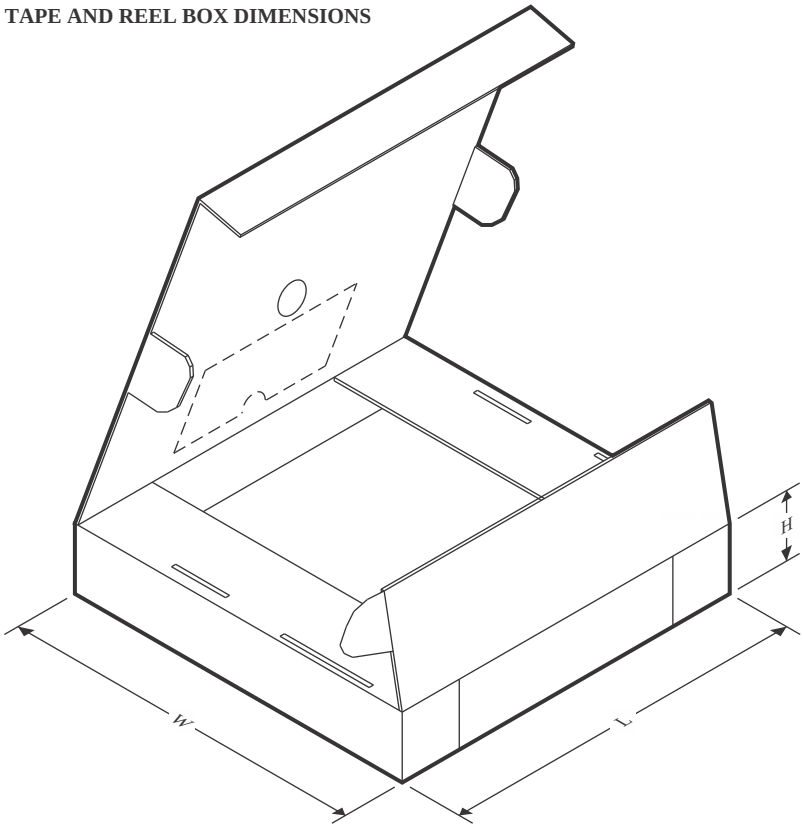
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HCT244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HCT244DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74HCT244DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HCT244NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HCT244NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HCT244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HCT244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT244PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT244PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT244PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

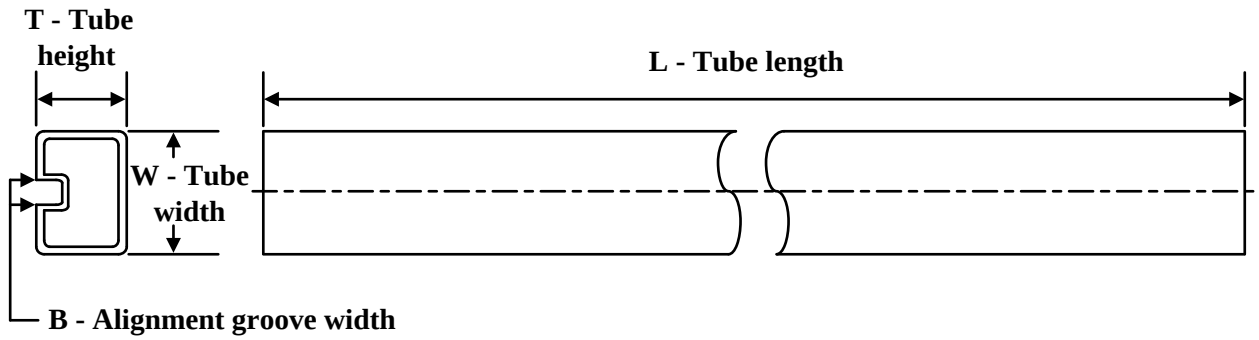
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT244DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HCT244DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HCT244DGSR	VSSOP	DGS	20	5000	356.0	356.0	35.0
SN74HCT244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HCT244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HCT244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HCT244PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT244PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74HCT244PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT244PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT244PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HCT244PWT	TSSOP	PW	20	250	356.0	356.0	35.0

TUBE



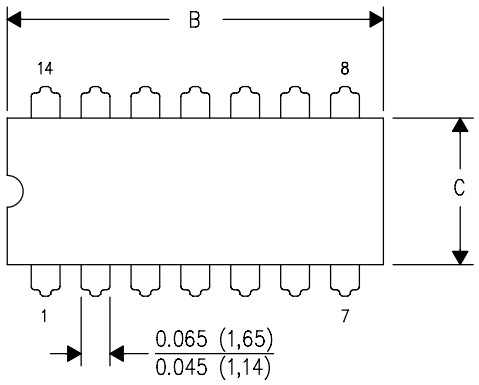
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8513001VSA	W	CFP	20	1	506.98	26.16	6220	NA
85130012A	FK	LCCC	20	1	506.98	12.06	2030	NA
JM38510/65755B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
M38510/65755B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74HCT244DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HCT244DWE4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HCT244DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HCT244N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HCT244NE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74HCT244PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74HCT244PWE4	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74HCT244PWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54HCT244FK	FK	LCCC	20	1	506.98	12.06	2030	NA

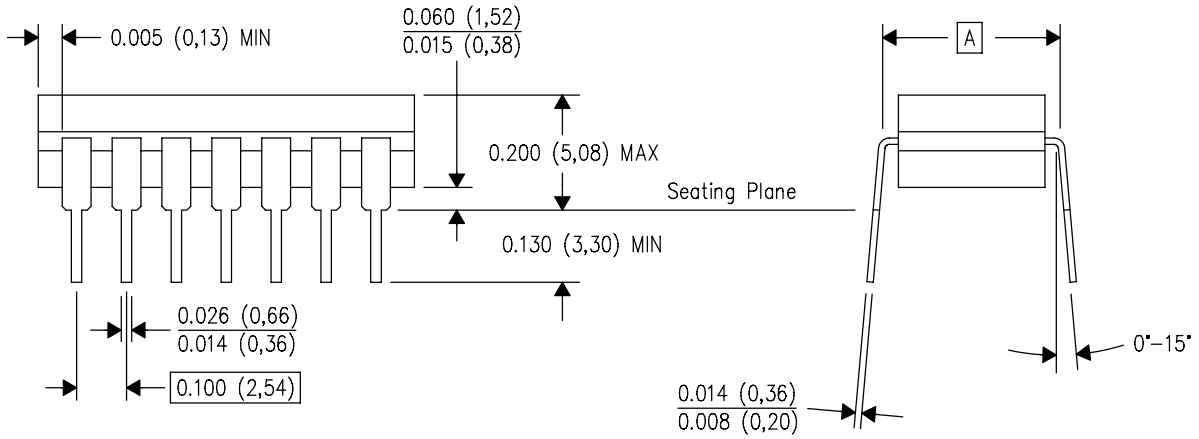
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



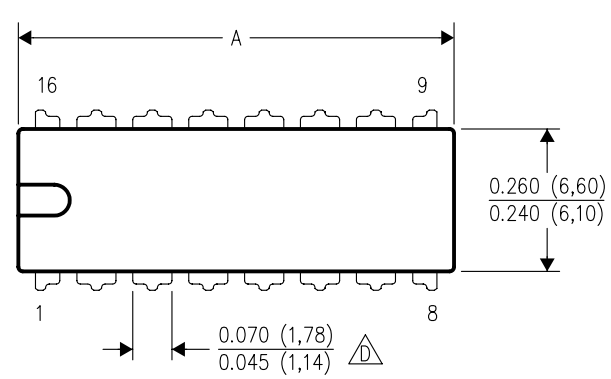
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

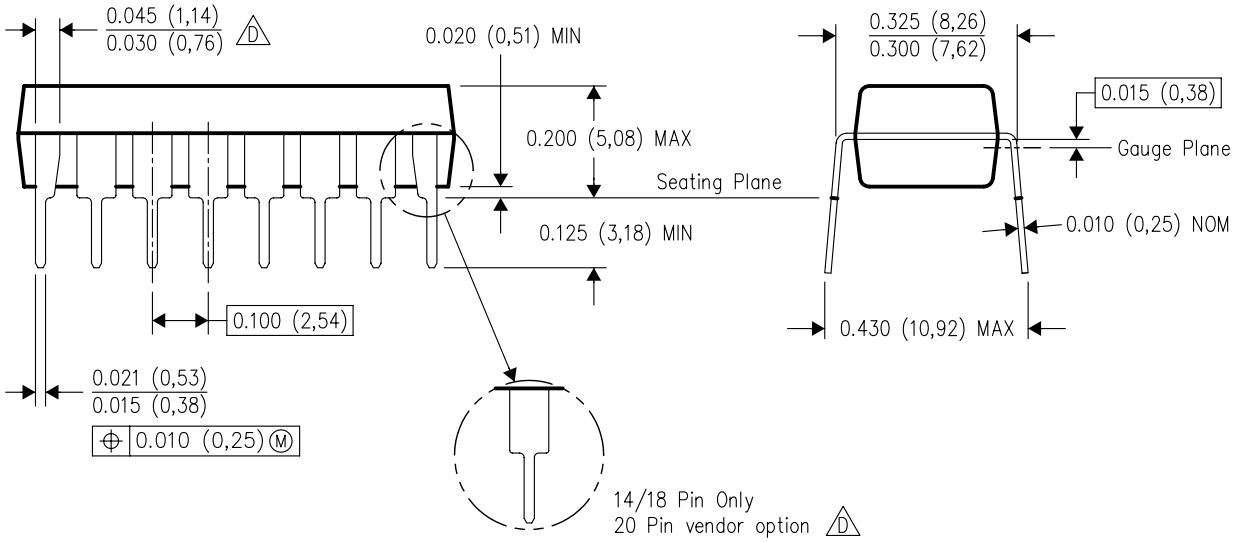
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

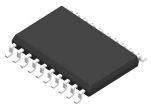


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

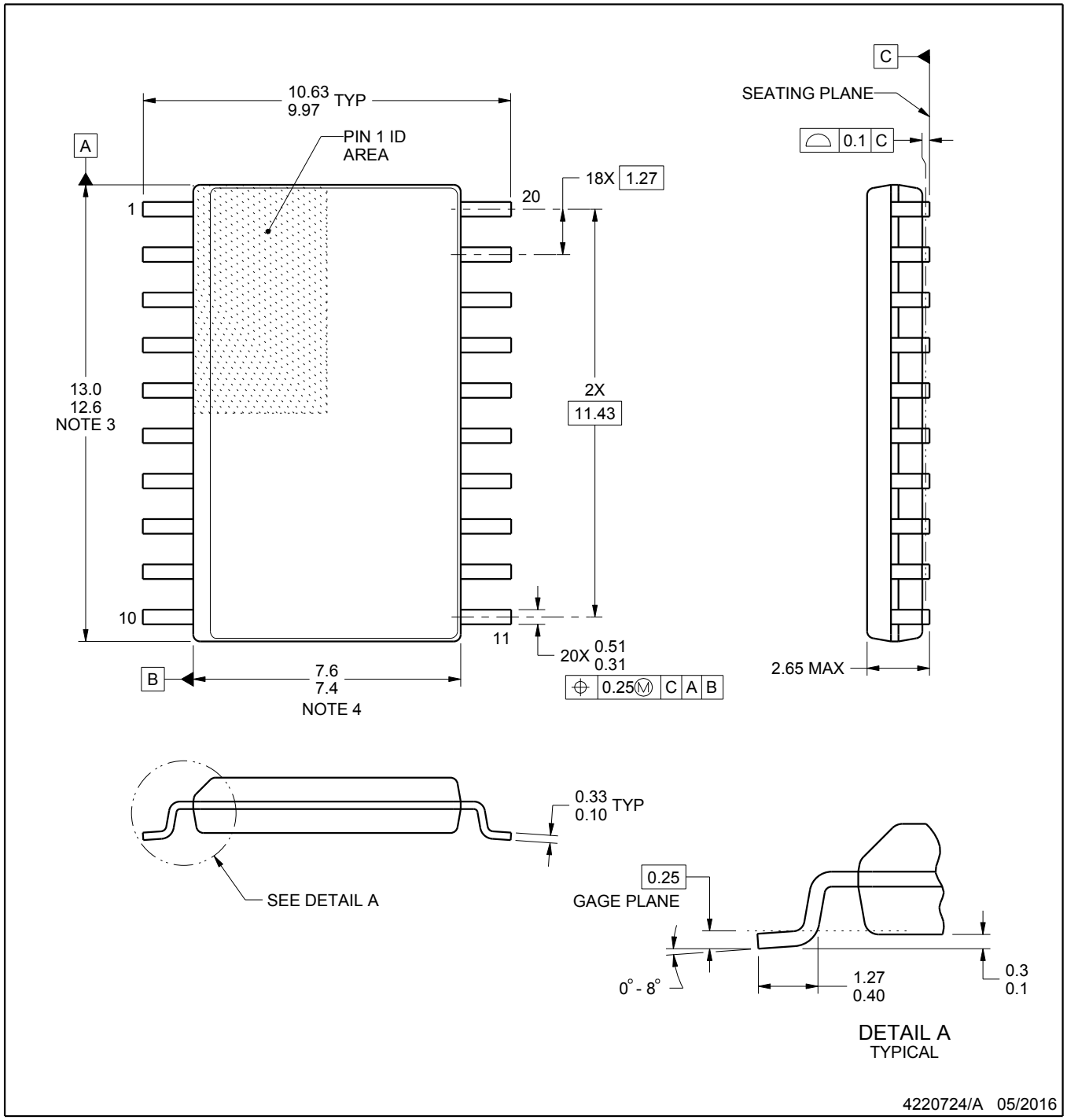


PACKAGE OUTLINE

DW0020A

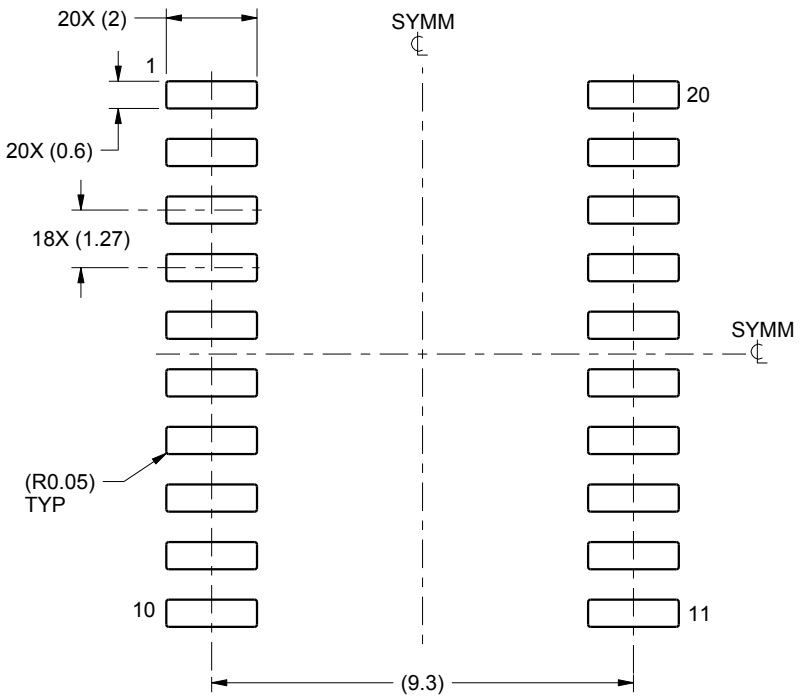
SOIC - 2.65 mm max height

SOIC

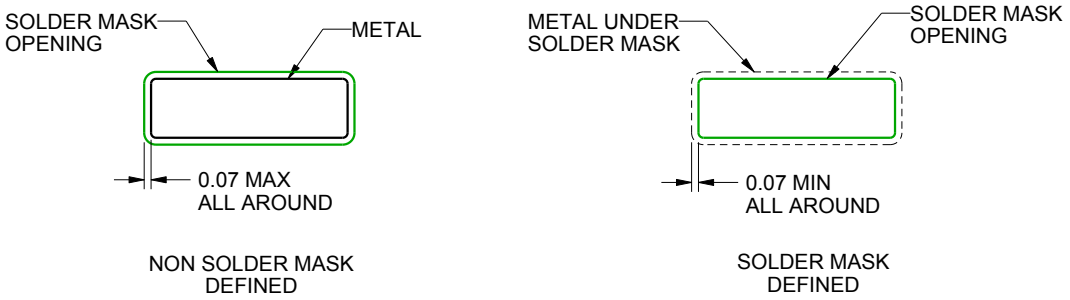


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

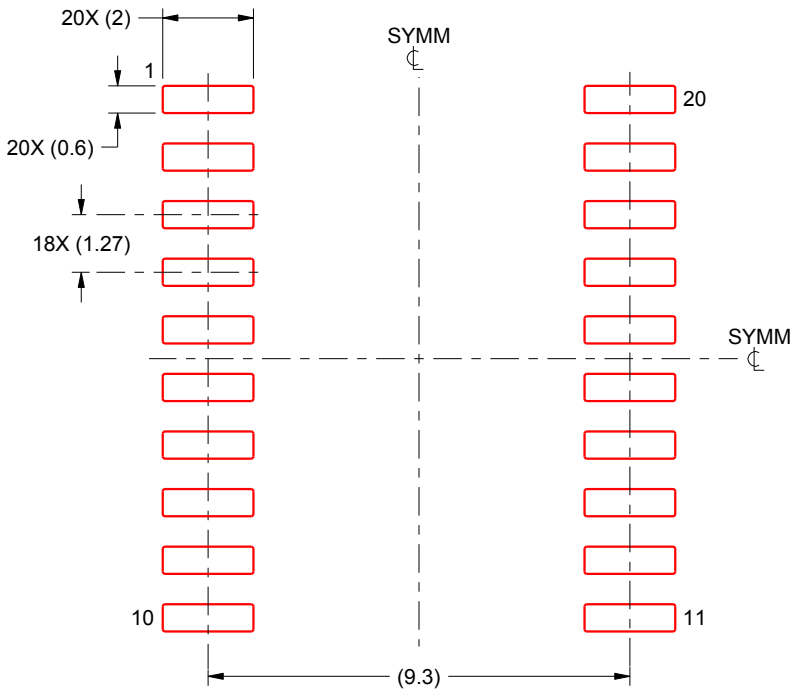


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



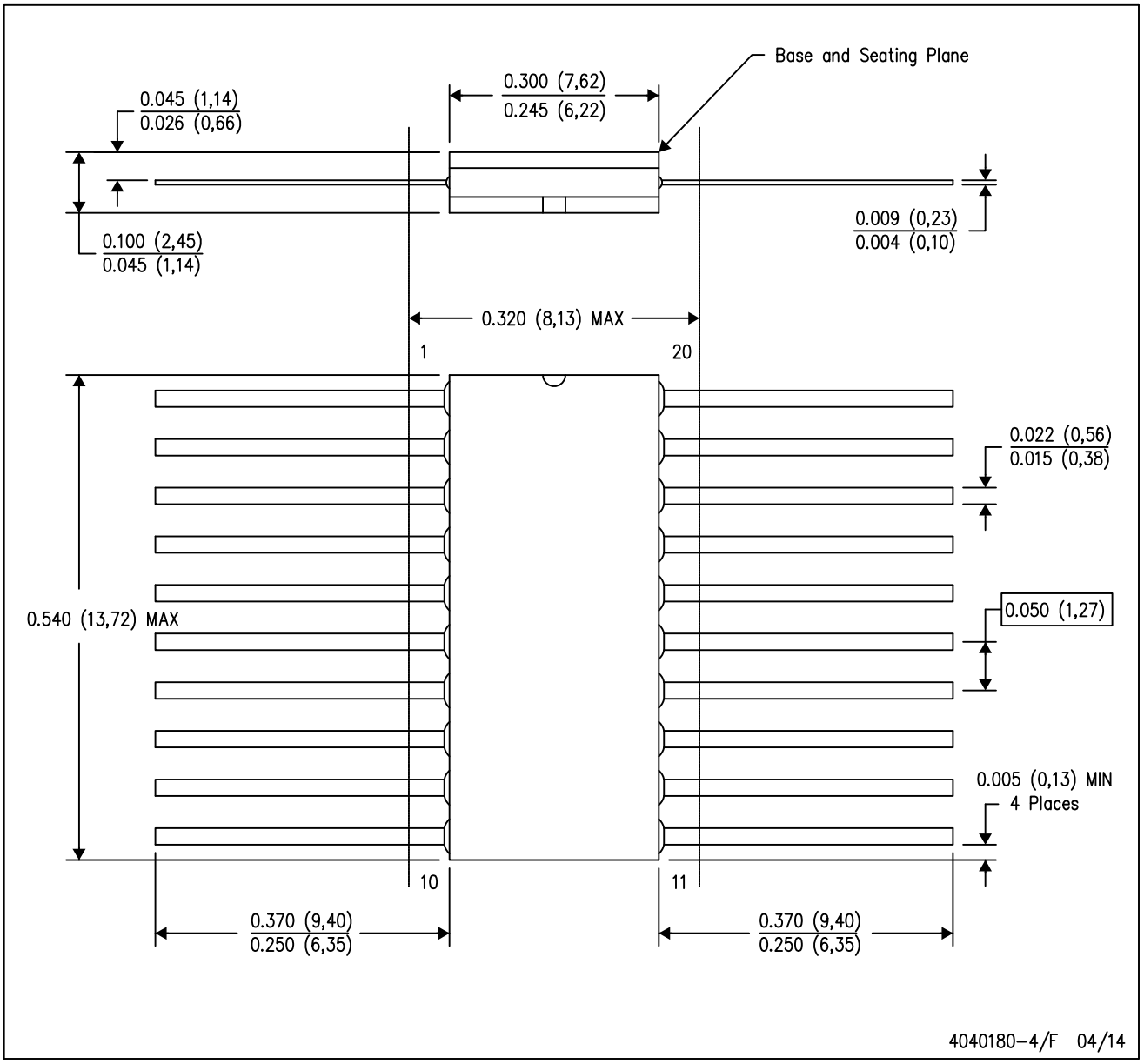
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



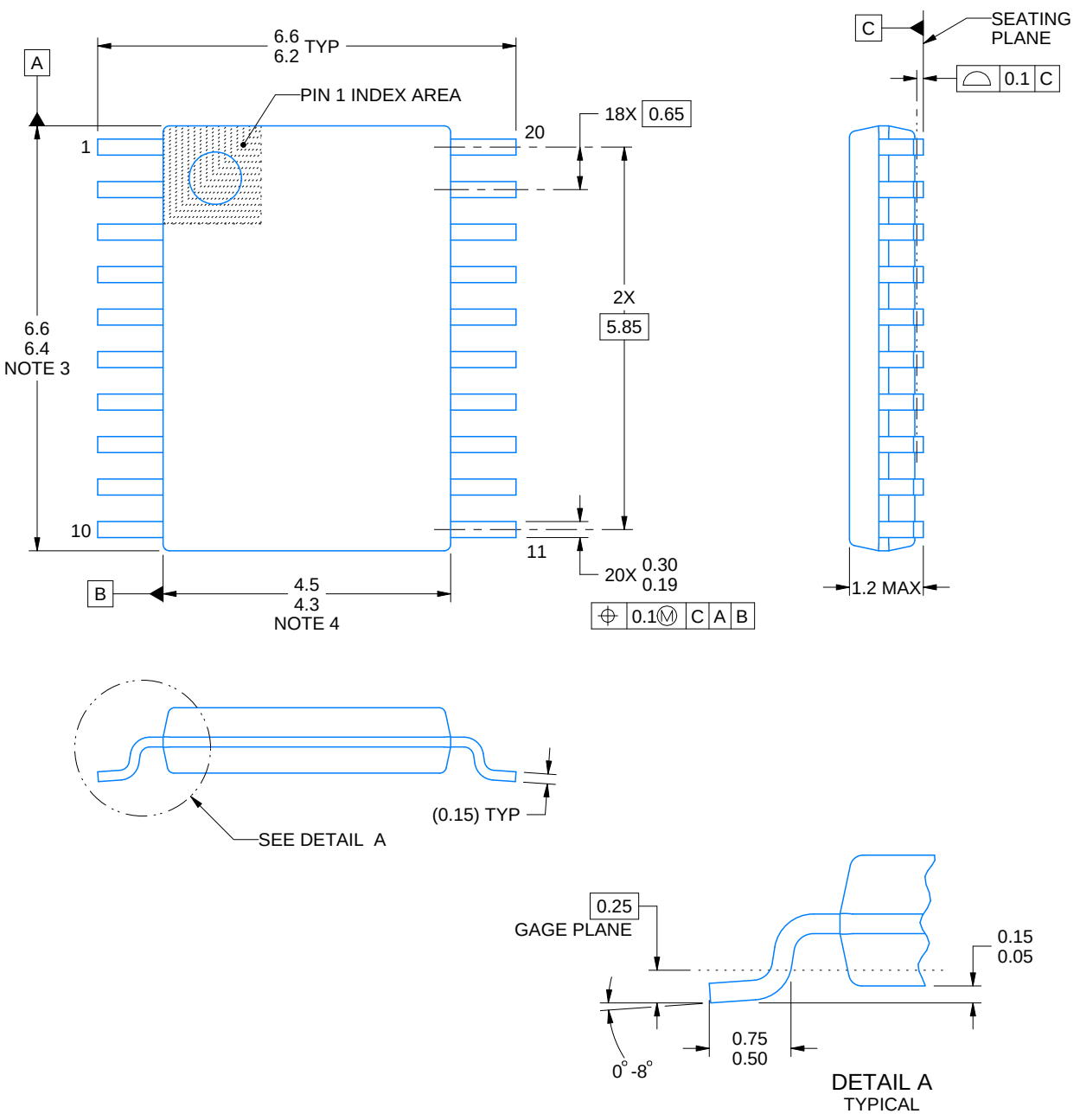
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

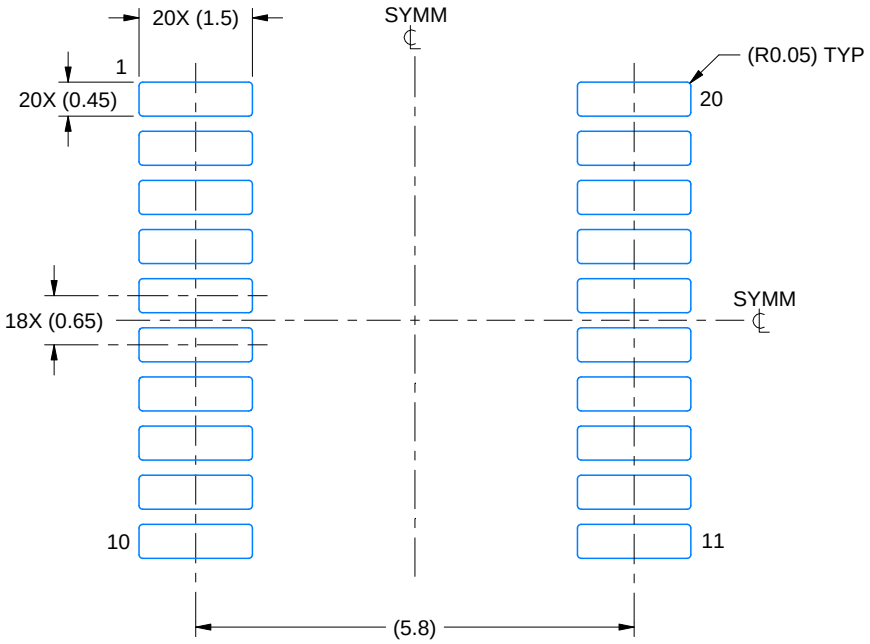
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



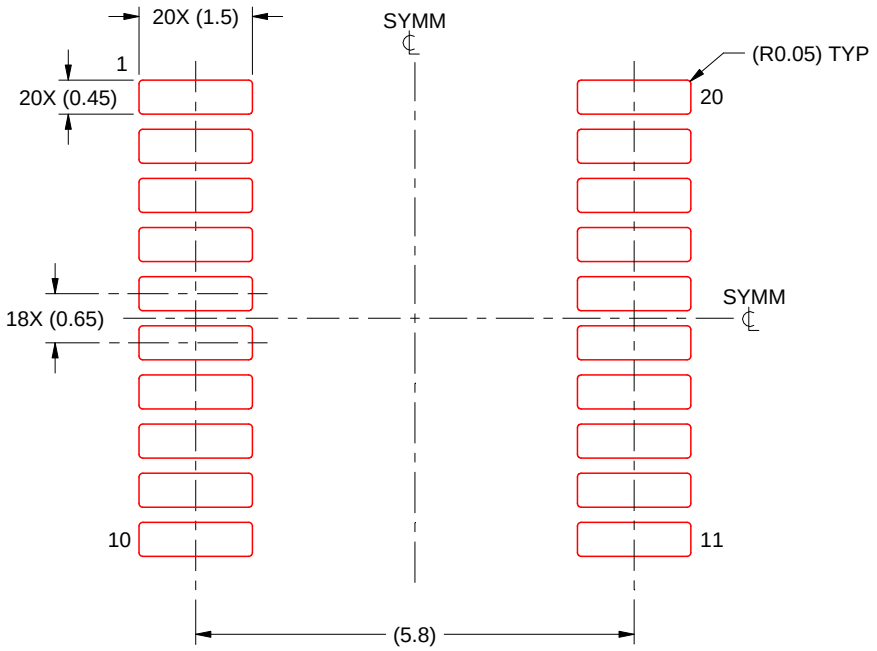
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



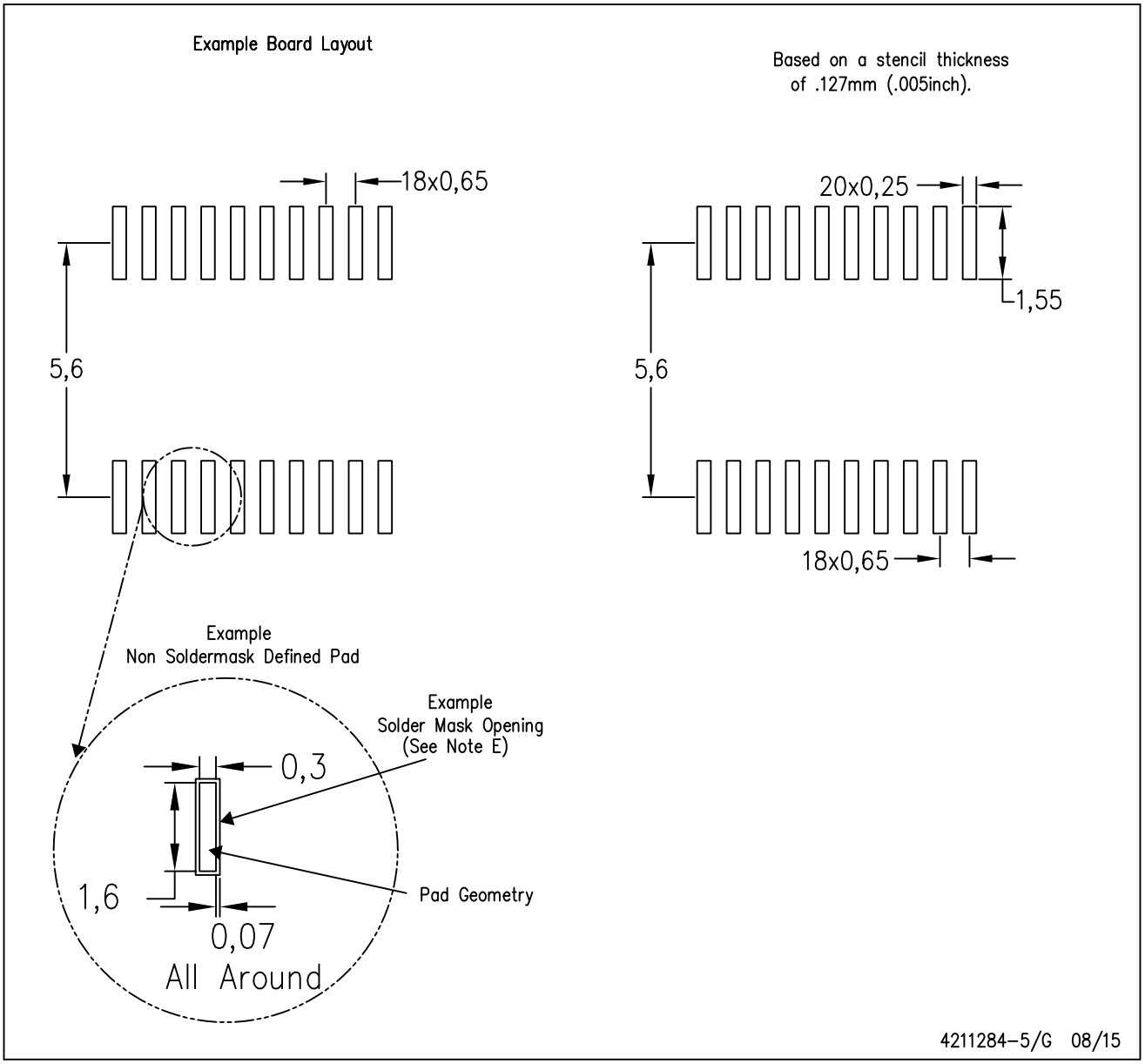
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



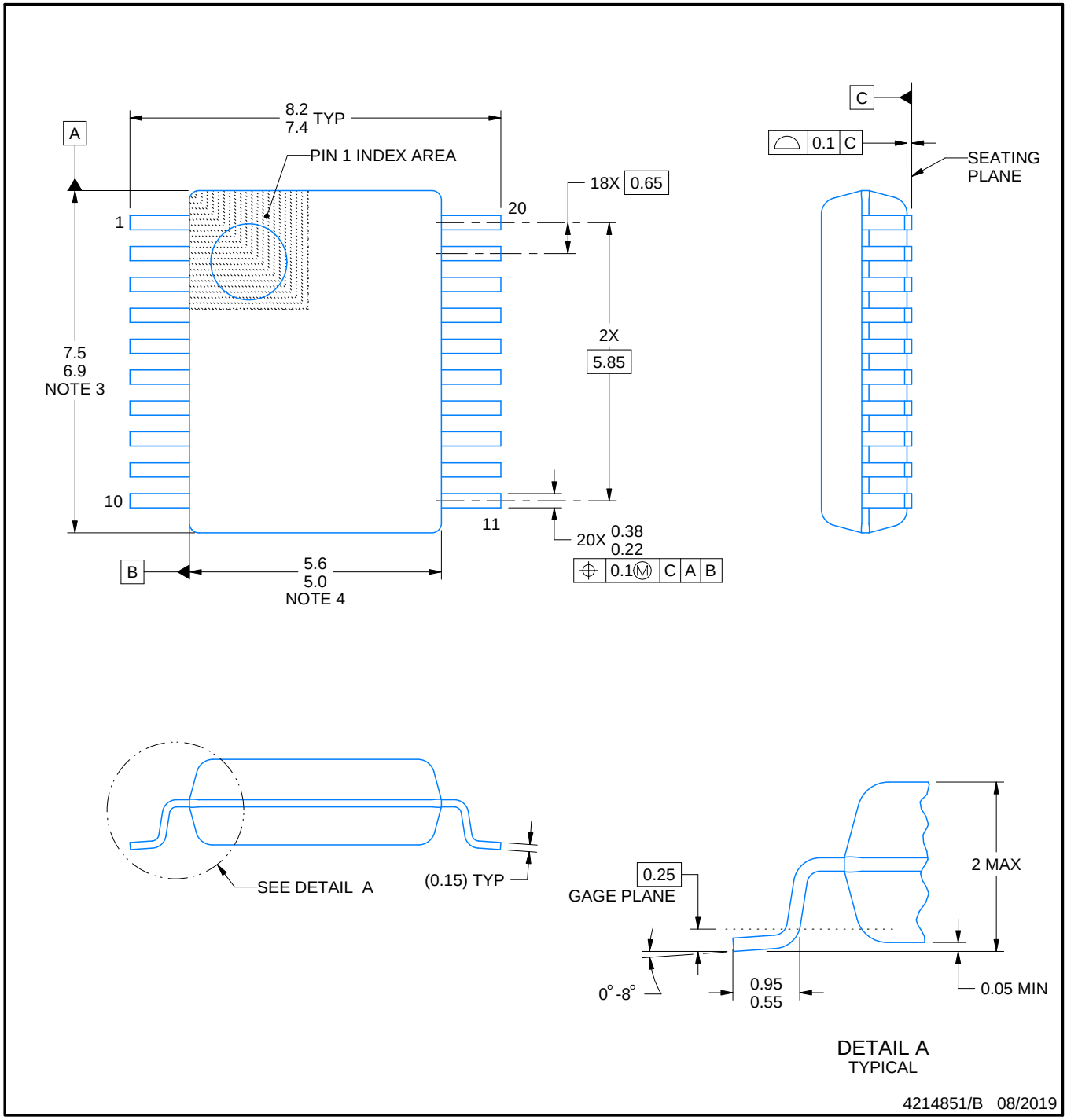
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DB0020A

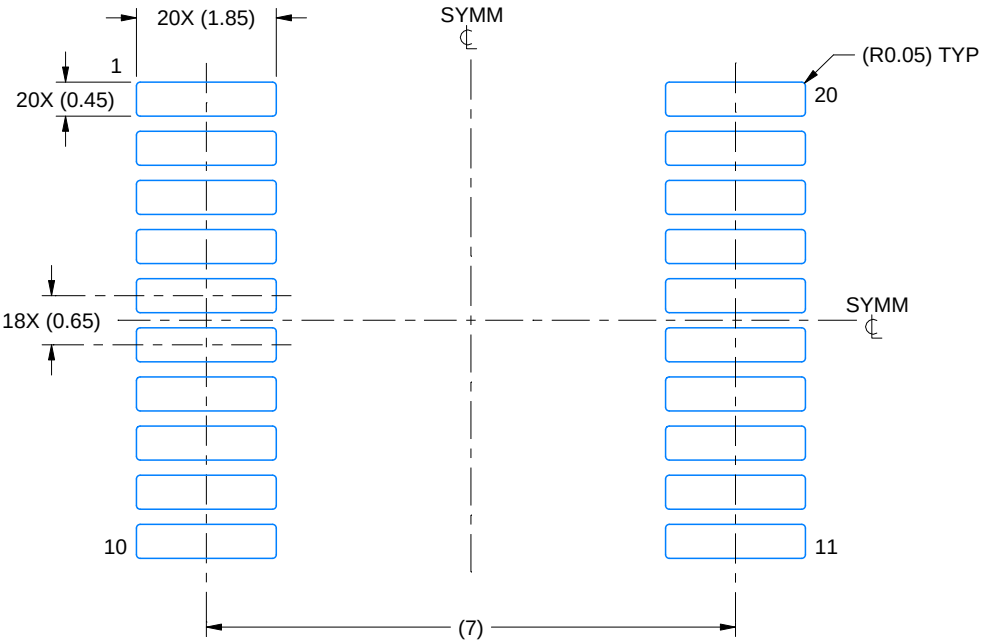
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

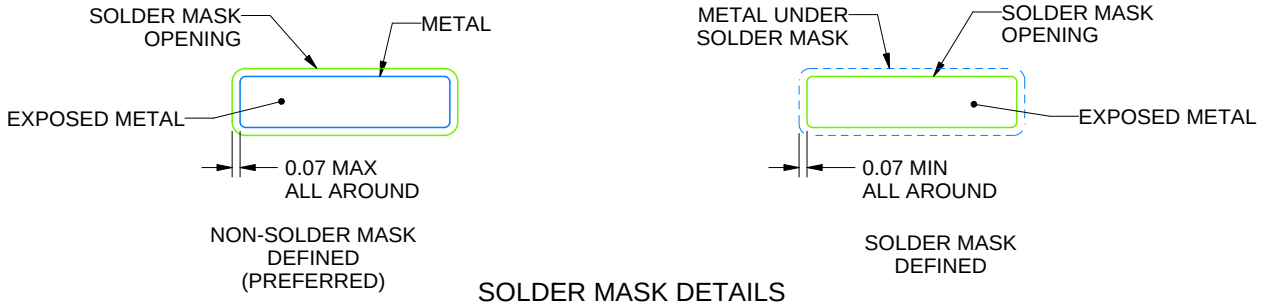


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

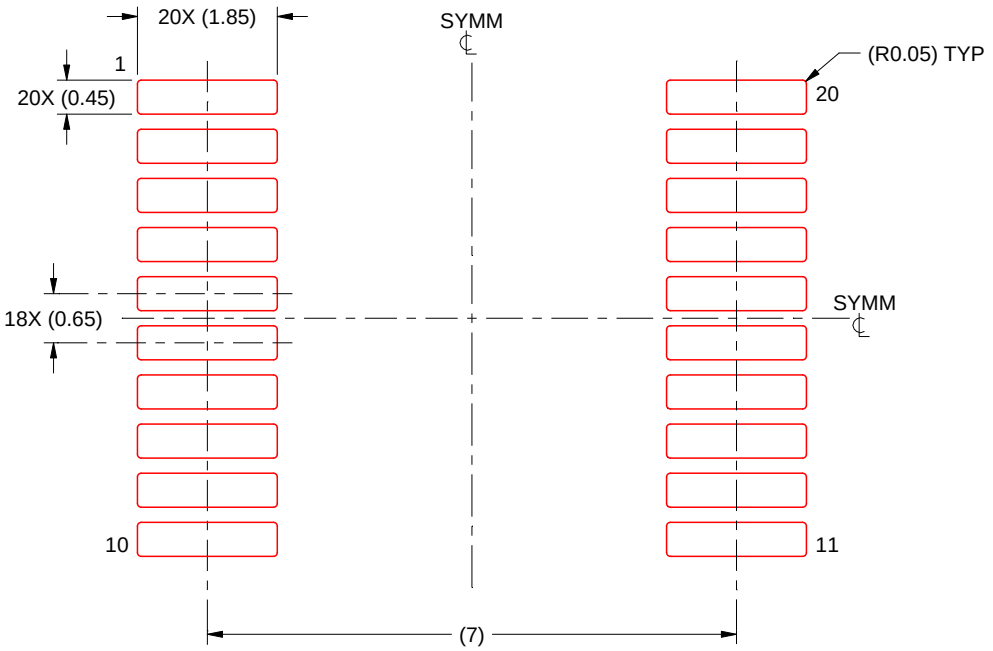
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

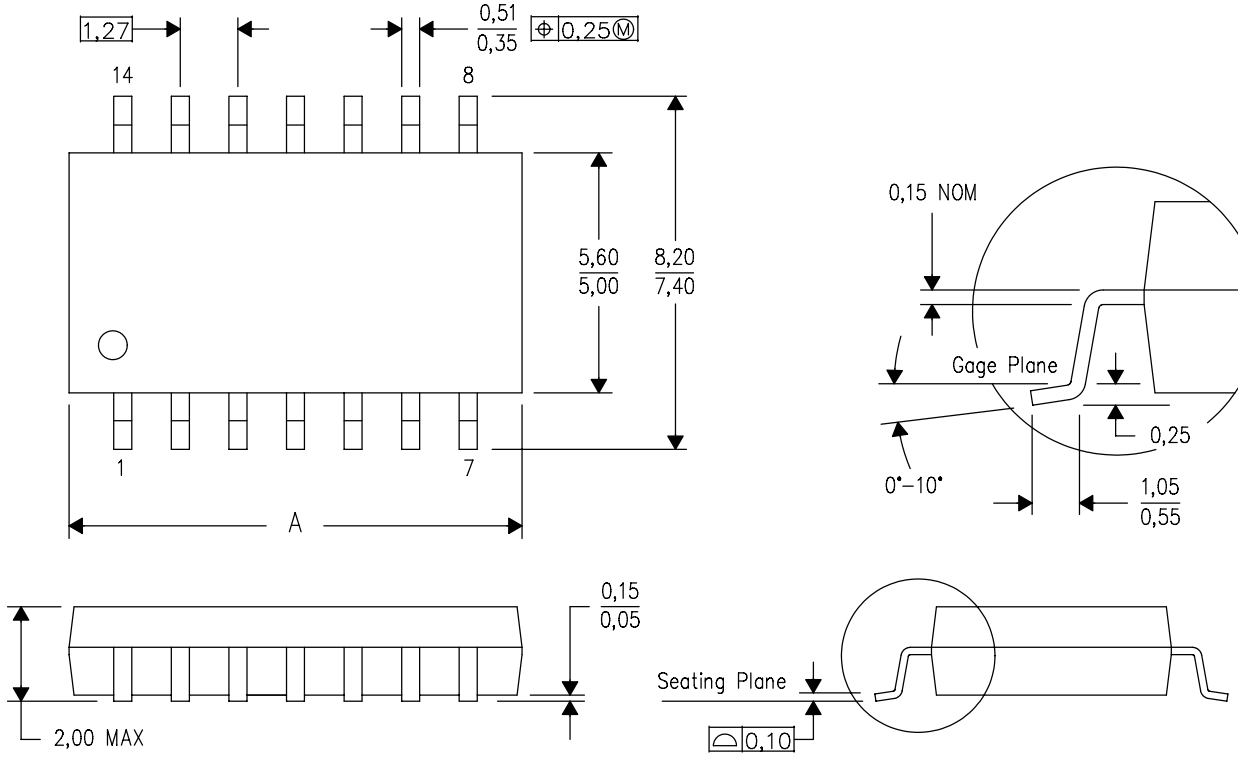
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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