TEXAS INSTRUMENTS

LM5100A, LM5100B, LM5100C
LM5101A, LM5101B, LM5101C

SNOSAW2Q – SEPTEMBER 2006 – REVISED NOVEMBER 2015

LM5100A/B/C, LM5101A/B/C 3-A, 2-A, and 1-A High-Voltage, High-Side and Low-Side Gate Drivers

1 Features

- Drives Both a High-Side and Low-Side N-Channel MOSFETs
- Independent High- and Low-Driver Logic Inputs
- Bootstrap Supply Voltage up to 118 V DC
- Fast Propagation Times (25-ns Typical)
- Drives 1000-pF Load With 8-ns Rise and Fall Times
- Excellent Propagation Delay Matching (3-ns Typical)
- Supply Rail Undervoltage Lockout
- Low Power Consumption
- Pin Compatible With HIP2100/HIP2101

2 Applications

- Current-Fed Push-Pull Converters
- Half and Full Bridge Power Converters
- Synchronous Buck Converters
- Two Switch Forward Power Converters
- Forward with Active Clamp Converters

3 Description

The LM5100A/B/C and LM5101A/B/C high-voltage gate drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100 V. The A versions provide a full 3-A of gate drive, while the B and C versions provide 2 A and 1 A, respectively. The outputs are independently controlled with CMOS input thresholds (LM5100A/B/C) or TTL input thresholds (LM5101A/B/C).

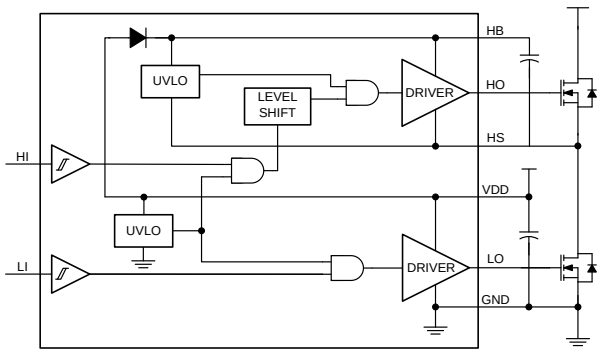
An integrated high-voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout is provided on both the low-side and the high-side power rails. These devices are available in the standard SOIC-8 pin, SO PowerPAD-8 pin, and the WSON-10 pin packages. The LM5100C and LM5101C are also available in MSOP-PowerPAD-8 package. The LM5101A is also available in WSON-8 pin package.

Device Information(1)

PART NUMBER	INPUT THRESHOLD	PEAK OUTPUT CURRENT
LM5100A	CMOS	3 A
LM5101A	TTL	3 A
LM5100B	CMOS	2 A
LM5101B	TTL	2 A
LM5100C	CMOS	1 A
LM5101C	TTL	1 A

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (March 2013) to Revision Q — **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision O (March 2013) to Revision P — **Page**

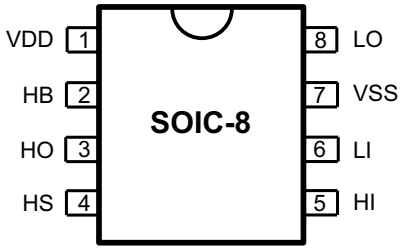
- Changed layout of National Data Sheet to TI format ... 19

5 Device Comparison Table

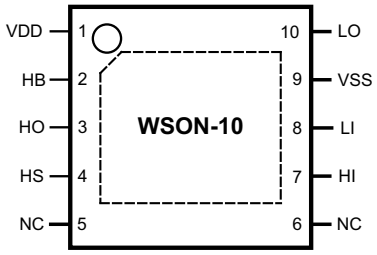
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5100A, LM5100C	WSON (10)	4.00 mm × 4.00 mm
	SO PowerPAD™ (8)	3.90 mm × 4.89 mm
	SOIC (8)	3.91 mm × 4.90 mm
LM5100B, LM5101B	WSON (10)	4.00 mm × 4.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
LM5101A	WSON (8)	4.00 mm × 4.00 mm
	WSON (10)	4 .00mm × 4.00 mm
	SO PowerPAD (8)	3.90 mm × 4.89 mm
	SOIC (8)	3.91 mm × 4.90 mm
LM5101C	MSOP PowerPAD (8)	3.00 mm × 3.00 mm
	WSON (10)	4.00 mm × 4.00 mm
	SOIC (8)	3.91 mm × 4.90 mm

6 Pin Configuration and Functions

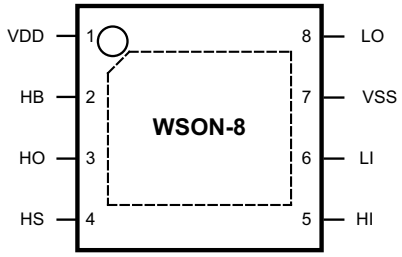
D Package
8-Pin SOIC
Top View



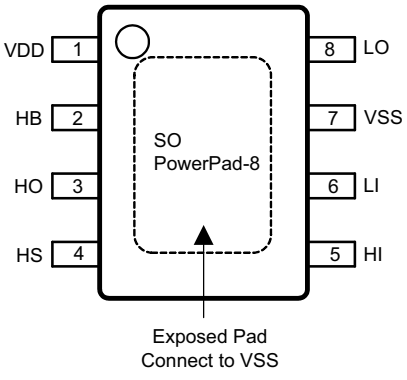
DPR Package
10-Pin WSON With Exposed Thermal Pad
Top View



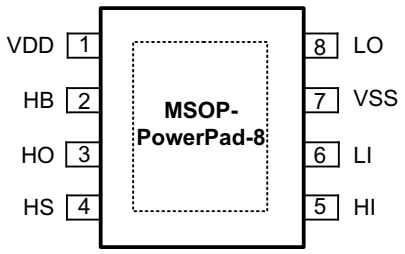
NGT Package
8-Pin WSON With Exposed Thermal Pad
Top View



DDA Package
8-Pin SO PowerPAD
Top View



DGN Package
8-Pin MSOP-PowerPAD
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	8 PINS	10 PINS(1)		
HB	2	2	I	High-side gate driver bootstrap supply. Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to the IC as possible.
HI	5	7	I	High-side driver control input. The LM5100A/B/C inputs have CMOS type thresholds. The LM5101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
HO	3	3	O	High-side gate driver output. Connect to the gate of high-side MOSFET with a short, low inductance path.
HS	4	4	—	High-side MOSFET source connection. Connect to the bootstrap capacitor negative terminal and the source of the high-side MOSFET.
LI	6	8	I	Low-side driver control input. The LM5100A/B/C inputs have CMOS type thresholds. The LM5101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
LO	8	10	O	Low-side gate driver output. Connect to the gate of the low-side MOSFET with a short, low inductance path.
VDD	1	1	I	Positive gate drive supply . Locally decouple to VSS using low ESR/ESL capacitor located as close to the IC as possible.
VSS	7	9	—	Ground return. All signals are referenced to this ground.
EP(2)			—	TI recommends that the exposed pad on the bottom of the package is soldered to ground plane on the PC board, and that ground plane should extend out from beneath the IC to help dissipate heat.

(1) For WSON-10 package, pins 5 and 6 have no connection.
(2) Exposed pad is not available on the 8-pin SOIC package.

7 Specifications

7.1 Absolute Maximum Ratings

See (1)(2)

	MIN	MAX	UNIT
VDD to VSS	−0.3	18	V
HB to HS	−0.3	18	V
LI or HI input	−0.3	V_{DD} + 0.3	V
LO output	−0.3	V_{DD} + 0.3	V
HO output	V_{HS} − 0.3	V_{HB} + 0.3	V
HS to VSS (3)	−5	100	V
HB to VSS		118	V
Junction temperature		150	°C
Storage temperature	−55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military or Aerospace specified devices are required, contact the Texas Instruments Sales Office or Distributors for availability and specifications.
(3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS node will generally not exceed –1 V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur, the HS voltage must never be more negative than VDD – 15 V. For example if VDD = 10 V, the negative transients at HS must not exceed –5 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)		±2000	V
	Machine Model (MM) (2)	Option A	50	
		Option B and C	100	

(1) The Human Body Model (HBM) is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 1000 V for HBM.
(2) Machine Model (MM) ratings are: 100 V(MM) for Options B and C; 50 V(MM) for Option A.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
VDD	9		14	V
HS	–1		100	V
HB	V_{HS} + 8		V_{HS} + 14	V
HS slew rate			< 50	V/ns
Junction temperature	−40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		LM5100A, LM5100C, LM5101A	LM5101C	LM5101A	LM5100x, LM5101x		UNIT
		SO PowerPAD	MSOP-PowerPAD[2]	WSON[2]	WSON[2]	SOIC	
		8 PINS	8 PINS	8 PINS	10 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[3]	40	80	37.8	40	170	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	36.7	—	—	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	—	14.9	—	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	—	0.3	—	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	—	—	15.2	—	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	4.4	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) 4-layer board with Cu finished thickness 1.5, 1, 1, 1.5 oz. Maximum die size used. 5× body length of Cu trace on PCB top. 50-mm × 50-mm ground and power planes embedded in PCB. See Application Note AN-1187 (SNOA401).
(3) The $R_{\theta JA}$ is not a given constant for the package and depends on the printed circuit board design and the operating environment.

7.5 Electrical Characteristics

unless otherwise specified, limits are for T_J = 25°C, V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0 V, no load on LO or HO [1].

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENTS							
I_{DD}	VDD quiescent current, LM5100A/B/C	LI = HI = 0 V	T_J = 25°C		0.1		mA
			T_J = –40°C to 125°C			0.2	
	VDD quiescent current, LM5101A/B/C	LI = HI = 0 V	T_J = 25°C		0.25		mA
			T_J = –40°C to 125°C			0.4	
I_{DDO}	VDD operating current	f = 500 kHz	T_J = 25°C		2		mA
			T_J = –40°C to 125°C			3	
I_{HB}	Total HB quiescent current	LI = HI = 0 V	T_J = 25°C		0.06		mA
			T_J = –40°C to 125°C			0.2	
I_{HBO}	Total HB operating current	f = 500 kHz	T_J = 25°C		1.6		mA
			T_J = –40°C to 125°C			3	
I_{HBS}	HB to VSS current, quiescent	HS = HB = 100 V	T_J = 25°C		0.1		µA
			T_J = –40°C to 125°C			10	
I_{HBSO}	HB to VSS current, operating	f = 500 kHz			0.4		mA
INPUT PINS							
V_{IL}	Input voltage threshold LM5100A/B/C	Rising Edge	T_J = 25°C		5.4		V
			T_J = –40°C to 125°C	4.5		6.3	
V_{IL}	Input voltage threshold LM5101A/B/C	Rising Edge	T_J = 25°C		1.8		V
			T_J = –40°C to 125°C	1.3		2.3	
V_{IHYS}	Input voltage hysteresis LM5100A/B/C				500		mV
V_{IHYS}	Input voltage hysteresis LM5101A/B/C				50		mV
R_I	Input pulldown resistance	T_J = 25°C			200		kΩ
		T_J = –40°C to 125°C		100		400	

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

unless otherwise specified, limits are for T_J = 25°C, V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0 V, no load on LO or HO [(1)].

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
UNDER VOLTAGE PROTECTION							
V_{DDR}	VDD rising threshold	T_J = 25°C			6.9		V
		T_J = –40°C to 125°C		6		7.4	
V_{DDH}	VDD threshold hysteresis				0.5		V
V_{HBR}	HB rising threshold	T_J = 25°C			6.6		V
		T_J = –40°C to 125°C		5.7		7.1	
V_{HBH}	HB threshold hysteresis				0.4		V
BOOT STRAP DIODE							
V_{DL}	Low-current forward voltage	I_{VDD-HB} = 100 µA	T_J = 25°C		0.52		V
			T_J = –40°C to 125°C			0.85	
V_{DH}	High-current forward voltage	I_{VDD-HB} = 100 mA	T_J = 25°C		0.8		V
			T_J = –40°C to 125°C			1	
R_D	Dynamic resistance LM5100A/B/C, LM5101A/B/C	I_{VDD-HB} = 100 mA	T_J = 25°C		1.0		Ω
			T_J = –40°C to 125°C			1.65	
LO AND HO GATE DRIVER							
V_{OL}	Low-level output voltage LM5100A/LM5101A	I_{HO} = I_{LO} = 100 mA	T_J = 25°C		0.12		V
			T_J = –40°C to 125°C			0.25	
	Low-level output voltage LM5100B/LM5101B		T_J = 25°C		0.16		V
			T_J = –40°C to 125°C			0.4	
	Low-level output voltage LM5100C/LM5101C		T_J = 25°C		0.28		V
			T_J = –40°C to 125°C			0.65	
V_{OH}	High-level output voltage LM5100A/LM5101A	I_{HO} = I_{LO} = 100 mA V_{OH} = VDD– LO or V_{OH} = HB - HO	T_J = 25°C		0.24		V
			T_J = –40°C to 125°C			0.45	
	High-level output voltage LM5100B/LM5101B		T_J = 25°C		0.28		V
			T_J = –40°C to 125°C			0.60	
	High-level output voltage LM5100C/LM5101C		T_J = 25°C		0.6		V
			T_J = –40°C to 125°C			1.10	
I_{OHL}	Peak pullup current LM5100A/LM5101A	HO, LO = 0 V	T_J = 25°C		3		A
	Peak pullup current LM5100B/LM5101B				2		A
	Peak pullup current LM5100C/LM5101C				1		A
I_{OLL}	Peak pulldown current LM5100A/LM5101A	HO, LO = 12 V	T_J = 25°C		3		A
	Peak pulldown current LM5100B/LM5101B				2		A
	Peak pulldown current LM5100C/LM5101C				1		A

7.6 Switching Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of –40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0 V, No Load on LO or HO (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LPHL}	LO turnoff propagation delay LM5100A/B/C	LI Falling to LO Falling		20	45	ns
	LO turnoff propagation delay LM5101A/B/C			22	56	ns
t_{LPLH}	LO turnon propagation delay LM5100A/B/C	LI Rising to LO Rising		20	45	ns
	LO turnon propagation delay LM5101A/B/C			26	56	ns
t_{HPHL}	HO turnoff propagation delay LM5100A/B/C	HI Falling to HO Falling		20	45	ns
	HO turnoff propagation delay LM5101A/B/C			22	56	ns
t_{HPLH}	LO turnon propagation delay LM5100A/B/C	HI Rising to HO Rising		20	45	ns
	LO turnon propagation delay LM5101A/B/C			26	56	ns
t_{MON}	Delay matching: LO on and HO off LM5100A/B/C			1	10	ns
	Delay matching: LO on and HO off LM5101A/B/C			4	10	ns
t_{MOFF}	Delay matching: LO off and HO on LM5100A/B/C			1	10	ns
	Delay matching: LO on and HO off LM5101A/B/C			4	10	ns
t_{RC}, t_{FC}	Either output rise and fall time	C_L = 1000 pF		8		ns
t_R	Output rise time (3 V to 9 V) LM5100A/LM5101A	C_L = 0.1 µF		430		ns
	Output rise time (3 V to 9 V) LM5100B/LM5101B			570		ns
	Output rise time (3 V to 9 V) LM5100C/LM5101C			990		ns
t_F	Output fall time (3 V to 9 V) LM5100A/LM5101A	C_L = 0.1 µF		260		ns
	Output fall time (3 V to 9 V) LM5100B/LM5101B			430		ns
	Output fall time (3 V to 9 V) LM5100C/LM5101C			715		ns
t_{PW}	Minimum input pulse width that changes the output			50		ns
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100 mA, I_R = 100 mA		37		ns

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

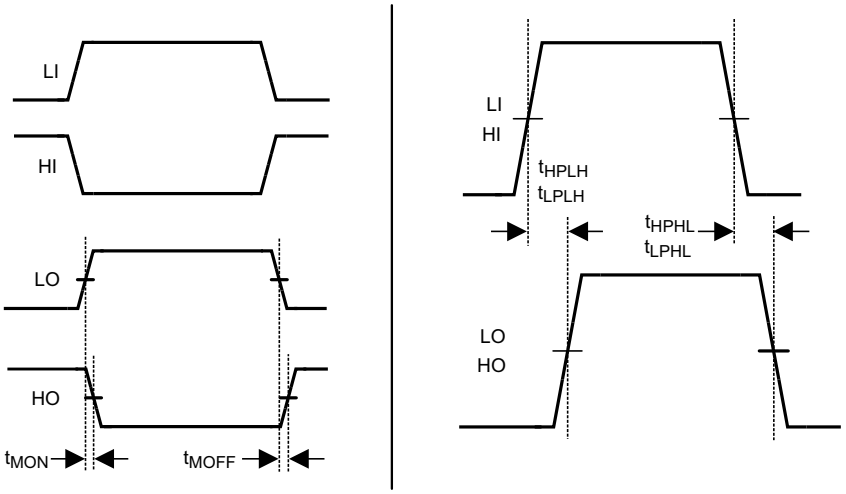


Figure 1. Timing Diagram

7.7 Typical Characteristics

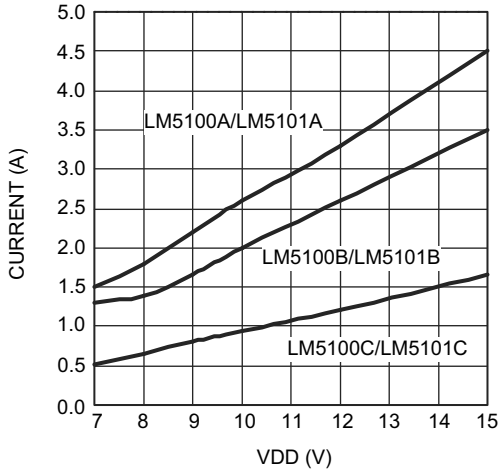


Figure 2. Peak Sourcing Current vs VDD

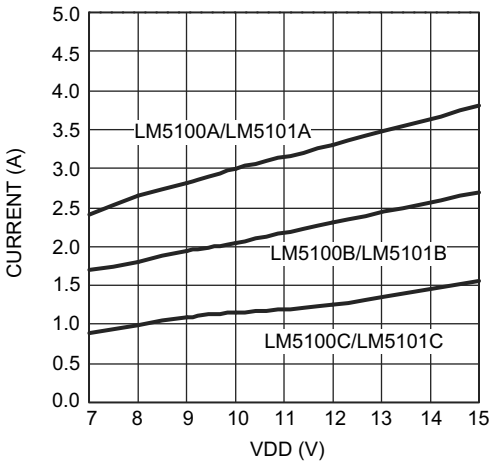


Figure 3. Peak Sinking Current vs VDD

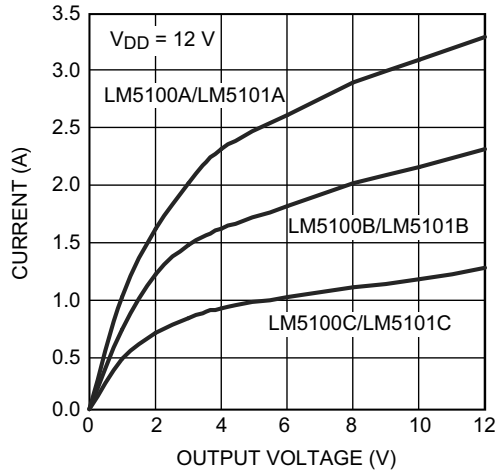


Figure 4. Sink Current vs Output Voltage

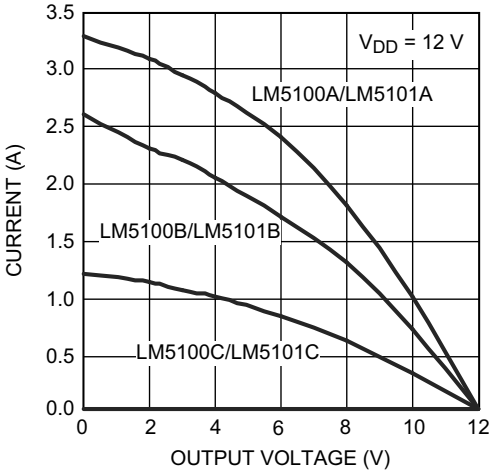


Figure 5. Source Current vs Output Voltage

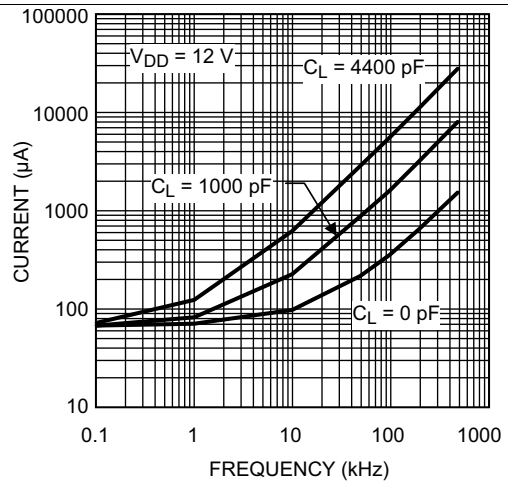


Figure 6. LM5100A/B/C I_{DD} vs Frequency

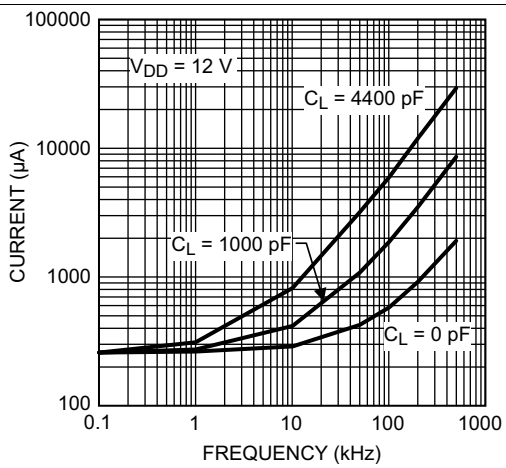


Figure 7. LM5101A/B/C I_{DD} vs Frequency

Typical Characteristics (continued)

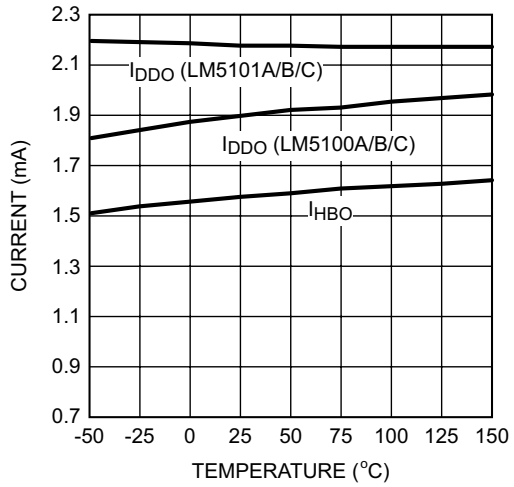


Figure 8. Operating Current vs Temperature

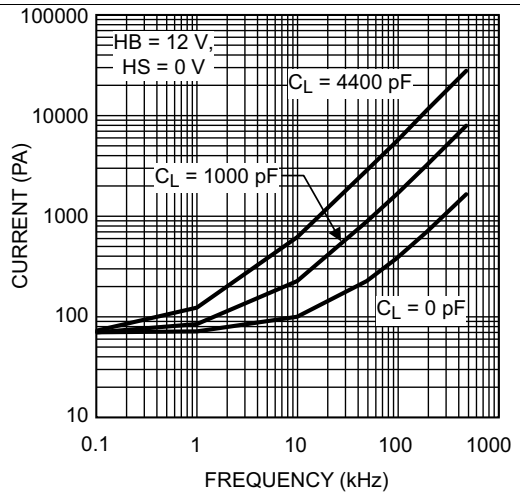


Figure 9. I_{HB} vs Frequency

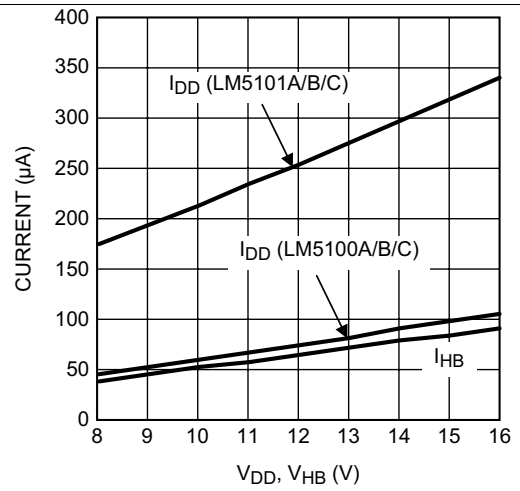


Figure 10. Quiescent Current vs Supply Voltage

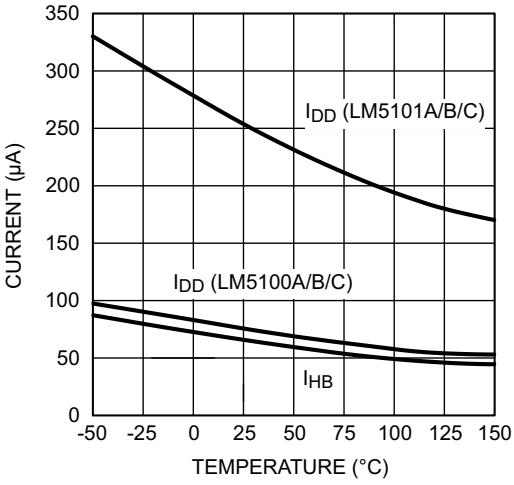


Figure 11. Quiescent Current vs Temperature

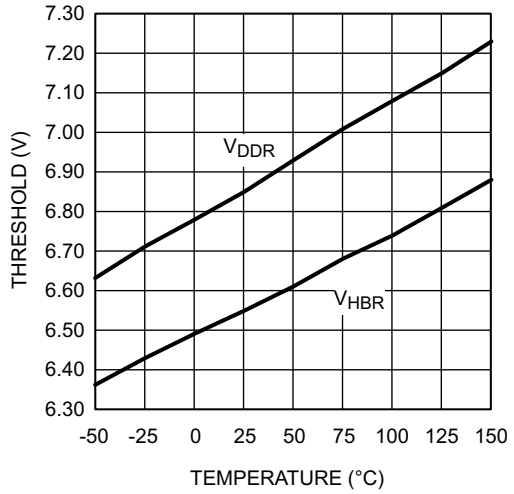


Figure 12. Undervoltage Rising Thresholds vs Temperature

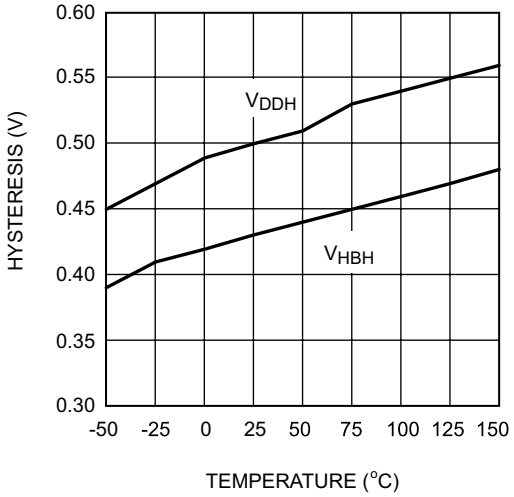


Figure 13. Undervoltage Threshold Hysteresis vs Temperature

Typical Characteristics (continued)

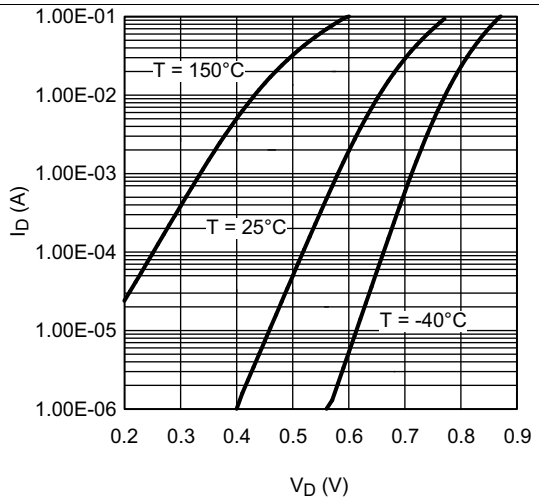


Figure 14. Bootstrap Diode Forward Voltage

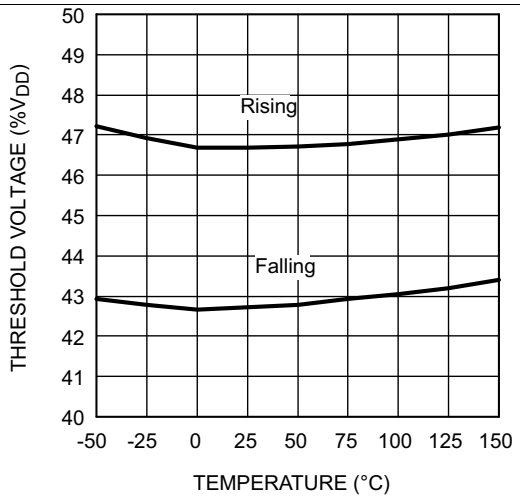


Figure 15. LM5100A/B/C Input Threshold vs Temperature

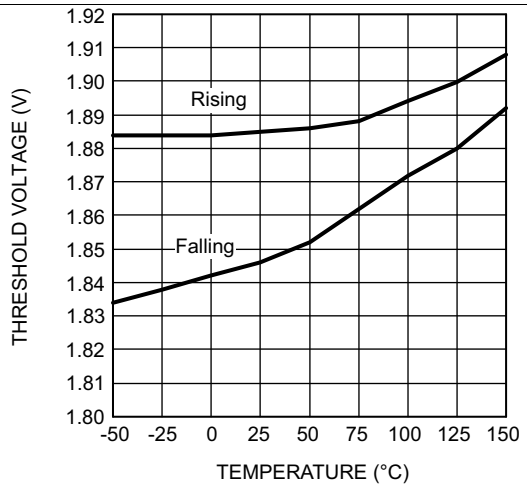


Figure 16. LM5101A/B/C Input Threshold vs Temperature

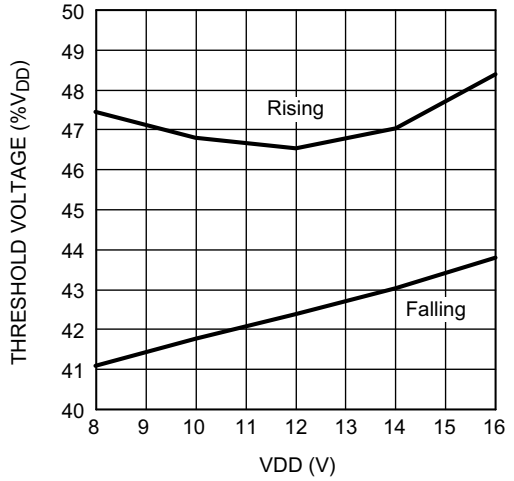


Figure 17. LM5100A/B/C Input Threshold vs VDD

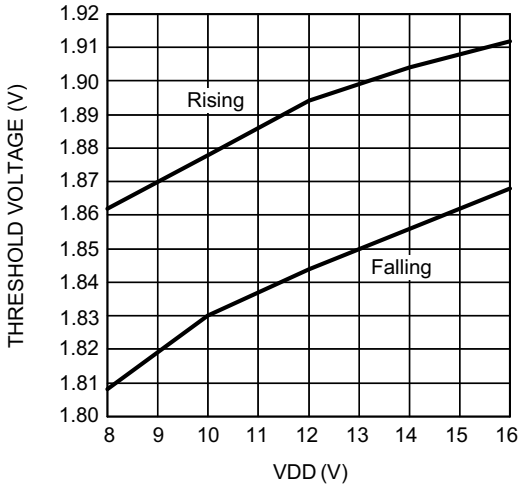


Figure 18. LM5101A/B/C Input Threshold vs VDD

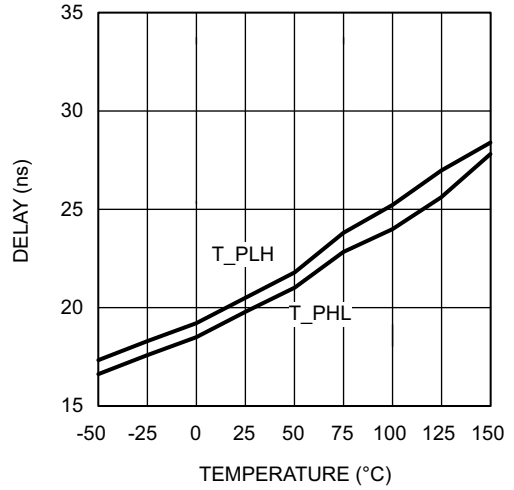


Figure 19. LM5100A/B/C Propagation Delay vs Temperature

Typical Characteristics (continued)

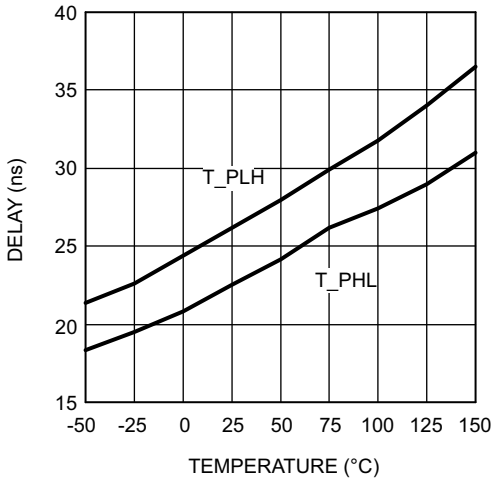


Figure 20. LM5101A/B/C Propagation Delay vs Temperature

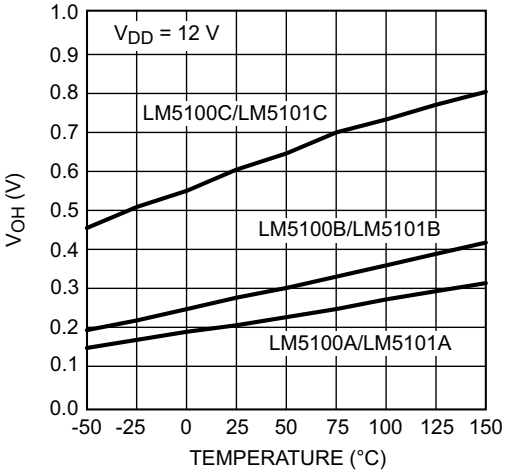


Figure 21. LO and HO Gate Drive - High Level Output Voltage vs Temperature

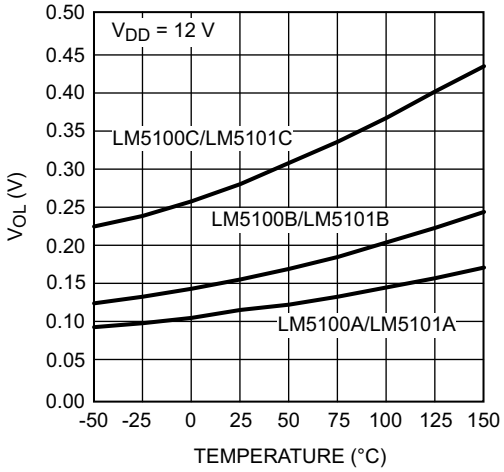


Figure 22. LO and HO Gate Drive - Low Level Output Voltage vs Temperature

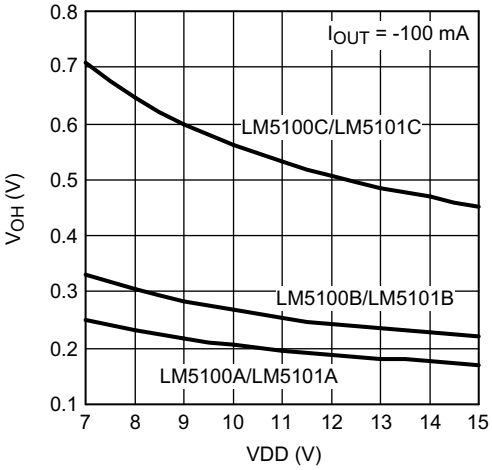


Figure 23. LO and HO Gate Drive - Output High Voltage vs VDD

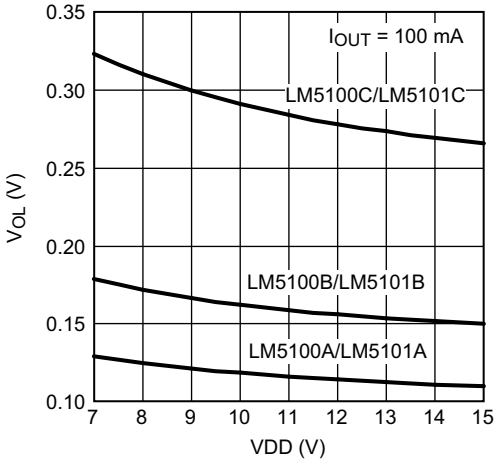


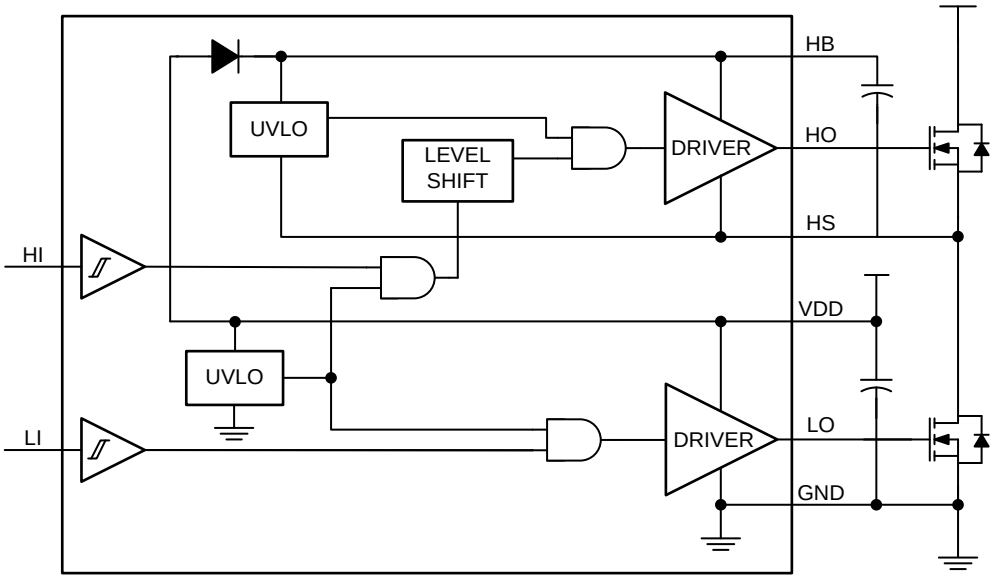
Figure 24. LO and HO Gate Drive - Output Low Voltage vs VDD

8 Detailed Description

8.1 Overview

The LM5100A/B/C and LM5101A/B/C are designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configuration. The outputs are independently controlled with CMOS input thresholds(LM5101A/B/C) or TTL input thresholds(LM5101A/B/C). The floating high-side driver is capable of working with supply voltages up to 100 V. An integrated high voltage diode is provided to charge high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Start-up and UVLO

Both high and low-side drivers include under voltage lockout (UVLO) protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage ($V_{HB–HS}$) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn on the external MOSFETs, and the built-in UVLO hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to the V_{DD} pin of the LM5100A/B/C and LM5101A/B/C, the outputs of the low-side and high-side are held low until V_{DD} exceeds the UVLO threshold, typically about 6.6 V. Any UVLO condition on the bootstrap capacitor will disable only the high-side output (HO).

8.3.2 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

Feature Description (continued)

8.3.3 Bootstrap Diode

The bootstrap diode necessary to generate the high-side bias is included in the LM5100/1 family. The diode anode is connected to V_{DD} and cathode connected to V_{HB}. With the V_{HB} capacitor connected to HB and the HS pins, the V_{HB} capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

8.3.4 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance, and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from V_{DD} to V_{SS} and the high-side is referenced from V_{HB} to V_{HS}.

8.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See *Start-up and UVLO* for more information on UVLO operation mode. In normal mode, the output stage is dependent on the states of the HI and LI pins.

Table 1. Input/Output Logic Table

HI	LI	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
x(3)	x	L	L

(1) HO is measured with respect to the HS.
(2) LO is measured with the respect to the VSS.
(3) x is floating condition

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

To affect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LM5100A/B/C and LM5101A/B/C are the high voltage gate drivers that are designed to drive both the high-side and low-side N-Channel MOSFETs in a half-bridge/full bridge configuration or in a synchronous buck circuit. The floating high side driver is capable of operating with supply voltages up to 100 V. This allows for N-Channel MOSFET control in half-bridge, full-bridge, push-pull, two switch forward and active clamp topologies. The outputs are independently controlled. Each channel is controlled by its respective input pins (HI and LI), allowing full and independent flexibility to control on and off state of the output.

9.2 Typical Application

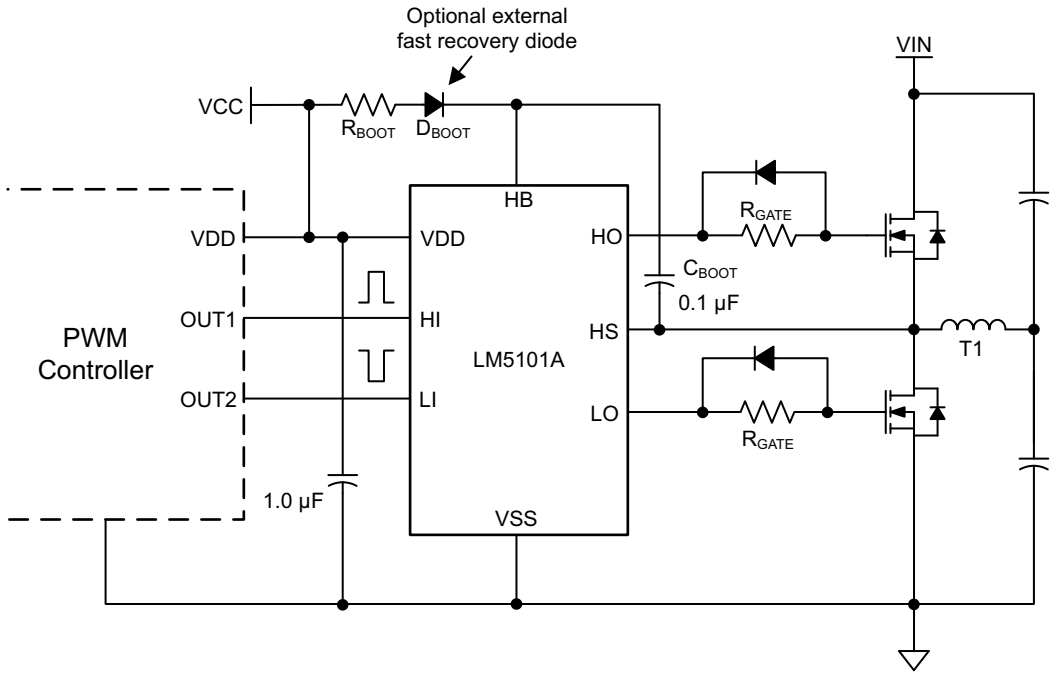


Figure 25. LM5101A Driving MOSFETs in Half-Bridge Configuration

Typical Application (continued)

9.2.1 Design Requirements

See Table 2 for the parameter and values.

Table 2. Operating Parameters

PARAMETER	VALUE
Gate Driver	LM5101A
MOSFET	CSD18531Q5A
VDD	10 V
Qgmax	43 nC
Fsw	100 kHz
Dmax	95%
I_{HBS}	10 µA
V_{DH}	1.0 V
V_{HBR}	7.1 V
V_{HBH}	0.4 V

9.2.2 Detailed Design Procedure

9.2.2.1 Select Bootstrap and VDD capacitor

The bootstrap capacitor must maintain the HB pin voltage above the UVLO voltage for the HB circuit in any circumstances during normal operation. Calculate the maximum allowable drop across the bootstrap capacitor with Equation 1.

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL} = 10\ V - 1.0\ V - 6.7\ V = 2.3\ V \quad (1)$$

where

- V_{DD} = Supply voltage of the gate drive IC
- V_{DH} = Bootstrap diode forward voltage drop
- $V_{HBL} = V_{HBR} - V_{HBH}$ = 6.7 V, HB falling threshold

The quiescent current of the bootstrap circuit is 10 µA, which is negligible compared to the Qgs of the MOSFET (see Equation 2 and Equation 3).

$$Q_{TOTAL} = Q_{gmax} + I_{HBS}\frac{D_{MAX}}{F_{SW}} = 43\ nC + 10\ \mu A\frac{0.95}{100\ kHz} = 43.01\ nC \quad (2)$$

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{HB}} = \frac{43.01\ nC}{2.3\ V} = 18.7\ nF \quad (3)$$

In practice the value for the CBOOT capacitor should be greater than that calculated to allow for situations where the power stage may skip pulse due to load transients. It is recommended to place the bootstrap capacitor as close to the HB and HS pins as possible.

$$C_{BOOT} = 100\ nF \quad (4)$$

As a general rule the local VDD bypass capacitor should be 10 times greater than the value of CBOOT.

$$C_{VDD} = 10 \times C_{BOOT} = 1\ \mu F \quad (5)$$

The bootstrap and bias capacitors should be ceramic types with X7R dielectric. The voltage rating should be twice that of the maximum VDD to allow for loss of capacitance once the devices have a DC bias voltage across them and to ensure long-term reliability of the devices.

9.2.2.2 Select External Bootstrap Diode and Resistor

The bootstrap capacitor is charged by the VDD through the internal bootstrap diode every cycle when low side MOSFET turns on. The charging of the capacitor involves high peak currents, and therefore transient power dissipation in the internal bootstrap diode may be significant and dependent on its forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver and need to be considered in the gate driver IC power dissipation.

For high frequency and high capacitive loads, it may be necessary to consider using an external bootstrap diode placed in parallel with internal bootstrap diode to reduce power dissipation of the driver. For the selection of external bootstrap diodes for LM510x device, please refer to the application note SNVA083.

Bootstrap resistor R_{BOOT} is selected to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of HB-HS. It is recommended that R_{BOOT} is between 2 Ω and 10 Ω. For this design, a current limiting resistor of 2.2 Ω is selected to limit inrush current of bootstrap diode.

$$I_{DBOOT(pk)} = \frac{V_{DD} - V_{DBOOT}}{R_{BOOT}} = \frac{10\ V - 0.6\ V}{2.2\ \Omega} = 4.27\ A \quad (6)$$

9.2.2.3 Select Gate driver Resistor

Resistor R_{GATE} is sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver. For this design 4.7-Ω resistors were selected for this design. Maximum HO and LO drive current are calculated by Equation 7 through Equation 10.

$$I_{HOH} = \frac{V_{DD} - V_{DH} - V_{OH}}{R_{GATE}} = \frac{10\ V - 1.0\ V - 0.45\ V}{4.7\ \Omega} = 1.819\ A \quad (7)$$

$$I_{LOH} = \frac{V_{DD} - V_{OH}}{R_{GATE}} = \frac{10\ V - 0.45\ V}{4.7\ \Omega} = 2.032\ A \quad (8)$$

$$I_{HOL} = \frac{V_{DD} - V_{DH} - V_{OL}}{R_{GATE}} = \frac{10\ V - 1.0\ V - 0.25\ V}{4.7\ \Omega} = 1.862\ A \quad (9)$$

$$I_{LOL} = \frac{V_{DD} - V_{OH}}{R_{GATE}} = \frac{10\ V - 0.25\ V}{4.7\ \Omega} = 2.074\ A$$

where

- I_{HOH} = Maximum HO source current
- I_{LOH} = Maximum LO source current
- I_{HOL} = Maximum HO sink current
- I_{LOH} = Maximum HO sink current
- V_{OH} = High-Level output voltage drop across HB to HO or VDD to LO
- V_{OL} = Low-Level output voltage drop across HO to HS or LO to GND (10)

9.2.2.4 Estimate the Driver Power Losses

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f_{sw}), output load capacitance on LO and HO (C_L), and supply voltage (VDD). The gate charge losses can be calculated by Equation 11.

$$P_{DGATES} = 2 \times V_{DD}^2 \times C_L \times f_{sw} \quad (11)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with Equation 11. Figure 26 can be used to approximate the power losses due to the gate drivers.

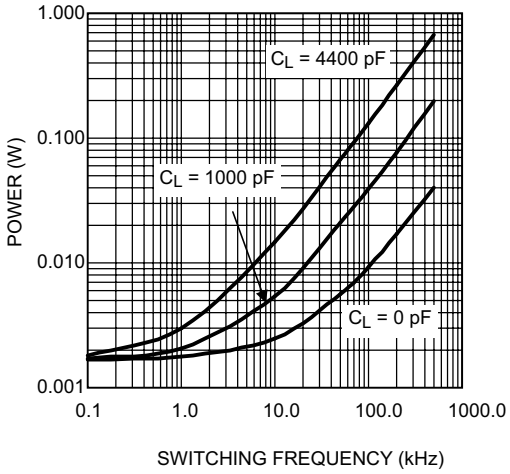


Figure 26. Gate Driver Power Dissipation (LO + HO)
V_{DD} = 12 V, Neglecting Diode Losses

The internal bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculation and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the internal diode power dissipation. If the diode losses can be significant, an external diode placed in parallel with the internal bootstrap diode can be helpful to reduce power dissipation within the IC.

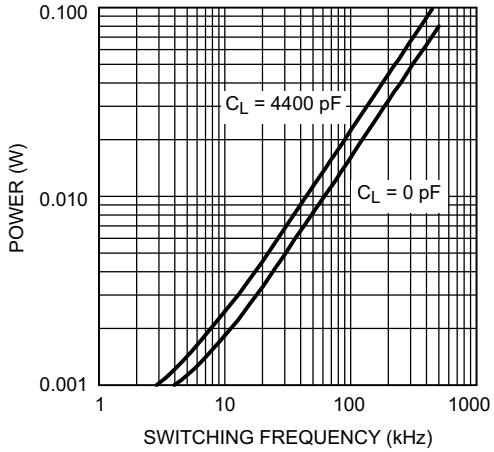


Figure 27. Diode Power Dissipation V_{IN} = 50 V

The total IC power dissipation can be estimated from the plots shown in Figure 26 and Figure 27 by summing the gate drive losses with the internal bootstrap diode losses for the intended application. For a given ambient temperature, the maximum allowable power loss of the IC can be defined as equation Equation 12.

$$P_{loss} = \frac{T_J - T_A}{R_{\theta JA}} \quad (12)$$

where

- P_{loss} = The total power dissipation of the driver
- T_J = Junction temperature
- T_A = Ambient temperature
- $R_{\theta JA}$ = Junction-to-ambient thermal resistance

The thermal metrics for the driver package is summarized in the *Thermal Information* table. For detailed information regarding the thermal information table, refer to the Application Note from Texas Instruments entitled *Semiconductor and IC Package Thermal Metrics* SPRA953.

9.2.3 Application Curves

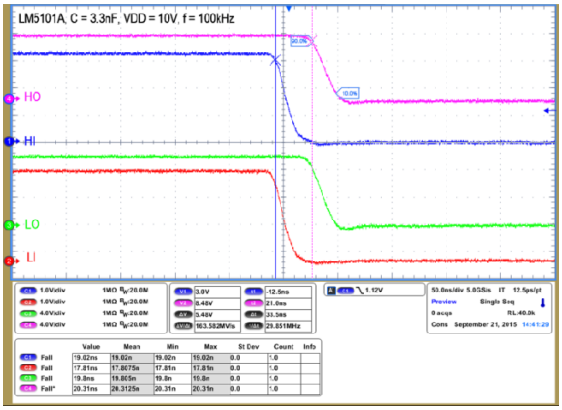


Figure 28. HI/LI to HO/LO Turnon Propagation Delay

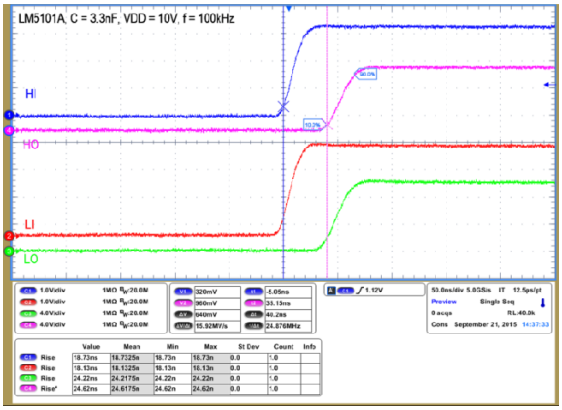


Figure 29. HI/LI to HO/LO Turnoff Propagation Delay

10 Power Supply Recommendations

The bias supply voltage range for which the device is rated to operate is from 9 V to 14 V. The lower end of this range is governed by the internal under voltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the VDDR supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 18-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 4-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 14 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDDH. Therefore, ensuring that, while operating at or near the 9-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the threshold (V_{DDR} – V_{DDH}), which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start up, the device does not begin operation until the VDD pin voltage has exceeded above the V_{DDR} threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Keep in mind that the charge for source current pulses delivered by the LO pin is also supplied through the same VDD pin. As a result, every time a current is sourced out of the LO pin a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that a local bypass capacitor is provided between the VDD and GND pins and located as close as possible to the device for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is necessary. TI recommends using two capacitors between VDD and GND: a 100-nF ceramic surface-mount capacitor that can be nudged very close to the pins of the device and another surface-mount capacitor in the range 0.22 µF to 10 µF added in parallel. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore, a 0.022-µF to 1-µF local decoupling capacitor is recommended between the HB and HS pins.

11 Layout

11.1 Layout Guidelines

The optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. Low-ESR/ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak currents being drawn from VDD during turnon of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS pin), the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
   – The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   – The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

A recommended layout pattern for the driver is shown in Figure 30. If possible a single layer placement is preferred.

11.2 Layout Example

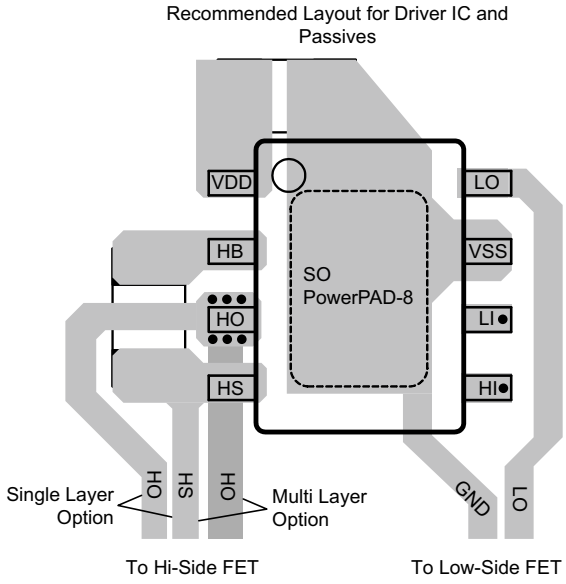


Figure 30. PCB Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401)
- *AN-1317 Selection of External Bootstrap Diode for LM510X Devices* (SNVA083)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM5100A	Click here	Click here	Click here	Click here	Click here
LM5100B	Click here	Click here	Click here	Click here	Click here
LM5100C	Click here	Click here	Click here	Click here	Click here
LM5101A	Click here	Click here	Click here	Click here	Click here
LM5101B	Click here	Click here	Click here	Click here	Click here
LM5101C	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5100AM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5100 AM	Samples
LM5100AMR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR		L5100 AMR	Samples
LM5100AMRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	Call TI | SN	Level-3-260C-168 HR		L5100 AMR	Samples
LM5100AMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5100 AM	Samples
LM5100ASD/NOPB	ACTIVE	WSON	DPR	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	5100ASD	Samples
LM5100BMA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5100 BMA	Samples
LM5100BMAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5100 BMA	Samples
LM5100BSD/NOPB	ACTIVE	WSON	DPR	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	5100BSD	Samples
LM5100CMAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5100 CMA	Samples
LM5101AM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5101 AM	Samples
LM5101AMR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR		L5101 AMR	Samples
LM5101AMRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR		L5101 AMR	Samples
LM5101AMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5101 AM	Samples
LM5101ASD	NRND	WSON	DPR	10	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	5101ASD	
LM5101ASD-1/NOPB	ACTIVE	WSON	NGT	8	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM		5101A-1	Samples
LM5101ASD/NOPB	ACTIVE	WSON	DPR	10	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	5101ASD	Samples
LM5101ASDX	NRND	WSON	DPR	10	4500	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	5101ASD	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5101ASDX-1/NOPB	ACTIVE	WSON	NGT	8	4500	RoHS & Green	SN	Level-1-260C-UNLIM		5101A-1	Samples
LM5101ASDX/NOPB	ACTIVE	WSON	DPR	10	4500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	5101ASD	Samples
LM5101BMA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5101 BMA	Samples
LM5101BMAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5101 BMA	Samples
LM5101BSD/NOPB	ACTIVE	WSON	DPR	10	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	5101BSD	Samples
LM5101BSDX/NOPB	ACTIVE	WSON	DPR	10	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	5101BSD	Samples
LM5101CMA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5101 CMA	Samples
LM5101CMAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5101 CMA	Samples
LM5101CMY/NOPB	ACTIVE	HVSSOP	DGN	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM		SXDB	Samples
LM5101CMYE/NOPB	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	SN	Level-1-260C-UNLIM		SXDB	Samples
LM5101CMYX/NOPB	ACTIVE	HVSSOP	DGN	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM		SXDB	Samples
LM5101CSD/NOPB	ACTIVE	WSON	DPR	10	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	5101CSD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

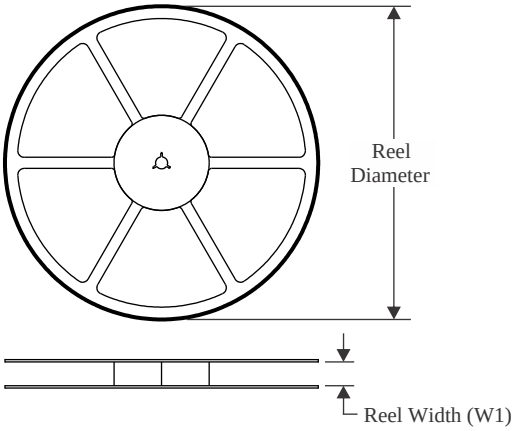
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

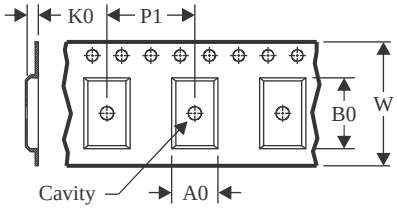
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

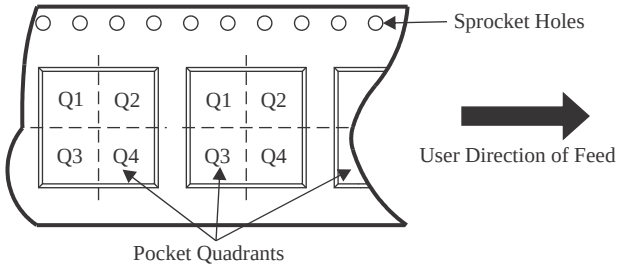


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

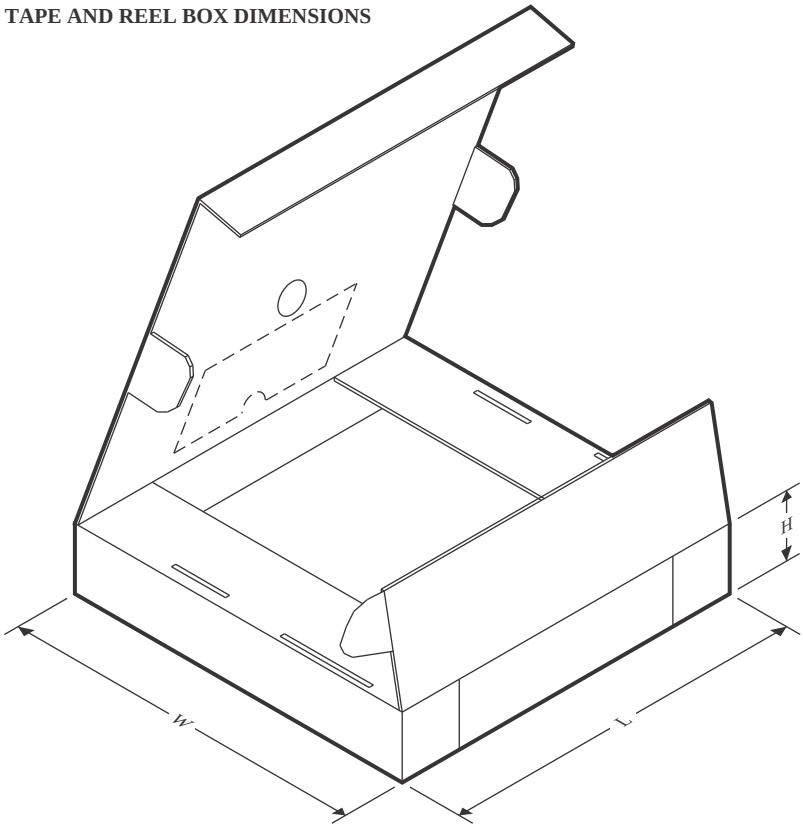


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5100AMRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100ASD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100BMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100BSD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100CMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101AMRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101ASD-1/NOPB	WSON	NGT	8	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5101ASD/NOPB	WSON	DPR	10	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5101ASD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101ASDX-1/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101BMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101BSD/NOPB	WSON	DPR	10	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5101BSDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5101CMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101CMY/NOPB	HVSSOP	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5101CMYE/NOPB	HVSSOP	DGN	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5101CMYX/NOPB	HVSSOP	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5101CSD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

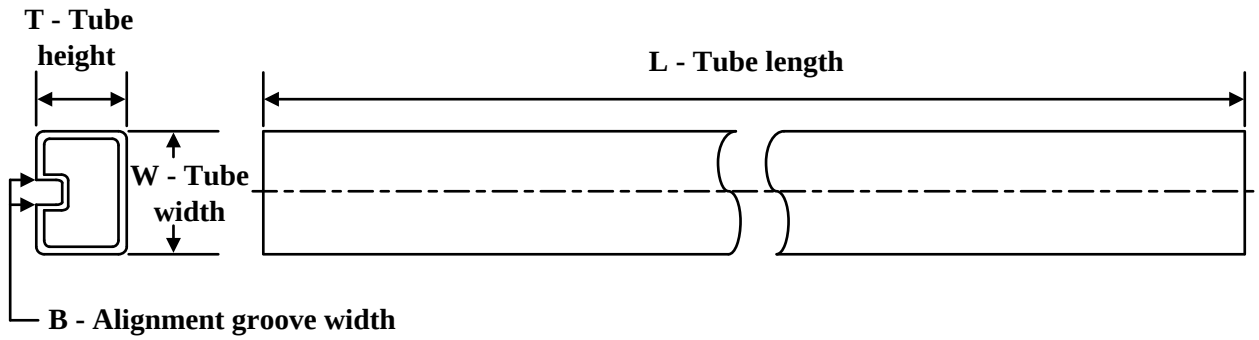


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5100AMRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	35.0
LM5100AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5100ASD/NOPB	WSON	DPR	10	1000	208.0	191.0	35.0
LM5100BMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5100BSD/NOPB	WSON	DPR	10	1000	208.0	191.0	35.0
LM5100CMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101AMRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	35.0
LM5101AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101ASD-1/NOPB	WSON	NGT	8	1000	200.0	183.0	25.0
LM5101ASD/NOPB	WSON	DPR	10	1000	200.0	183.0	25.0
LM5101ASD/NOPB	WSON	DPR	10	1000	208.0	191.0	35.0
LM5101ASDX-1/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0
LM5101BMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101BSD/NOPB	WSON	DPR	10	1000	200.0	183.0	25.0
LM5101BSDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5101CMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101CMY/NOPB	HVSSOP	DGN	8	1000	208.0	191.0	35.0
LM5101CMYE/NOPB	HVSSOP	DGN	8	250	208.0	191.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5101CMYX/NOPB	HVSSOP	DGN	8	3500	367.0	367.0	35.0
LM5101CSD/NOPB	WSON	DPR	10	1000	208.0	191.0	35.0

TUBE



*All dimensions are nominal

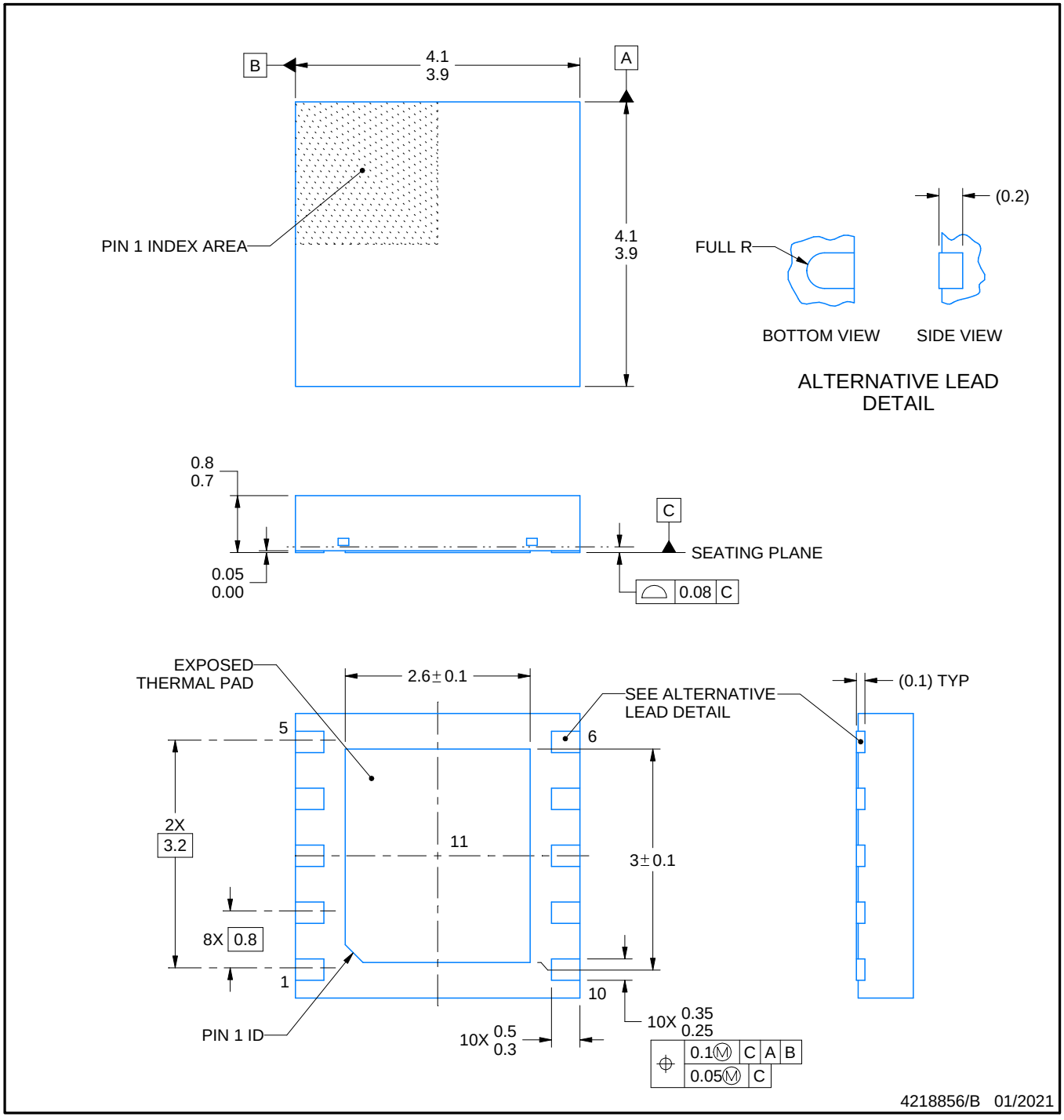
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5100AM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM5100AMR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LM5100BMA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM5101AM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM5101AM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM5101AMR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LM5101BMA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM5101CMA/NOPB	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DPR0010A

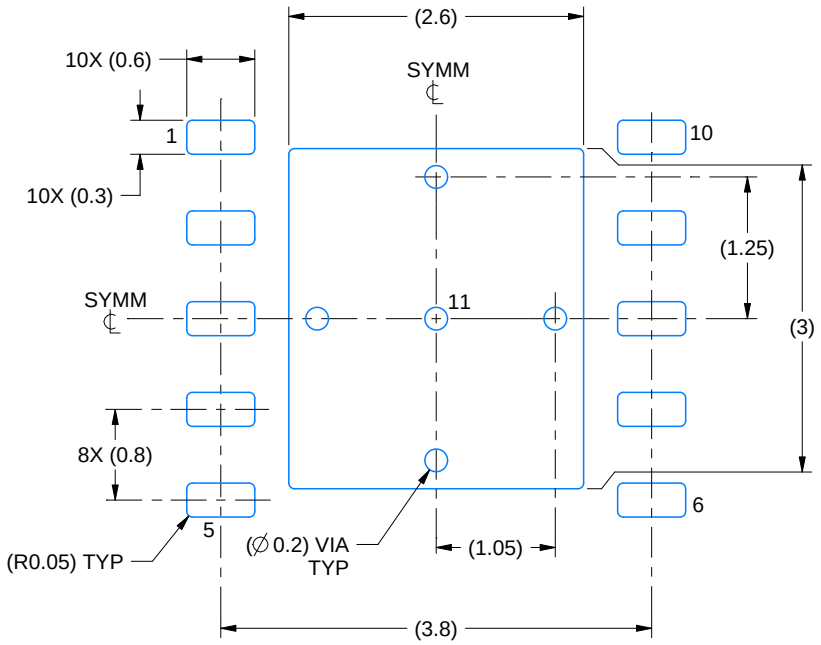
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

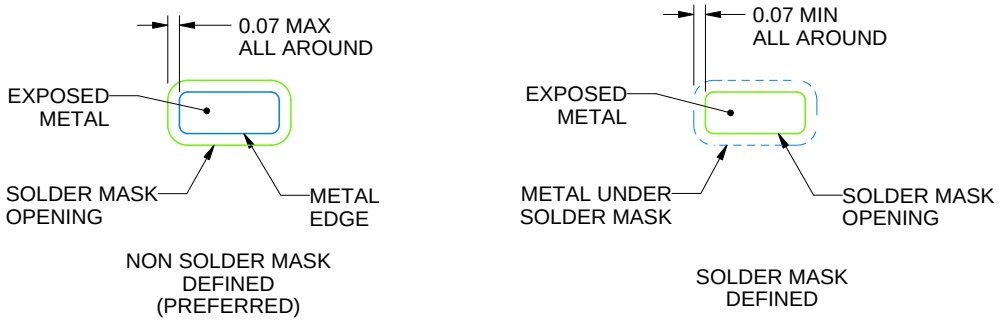


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

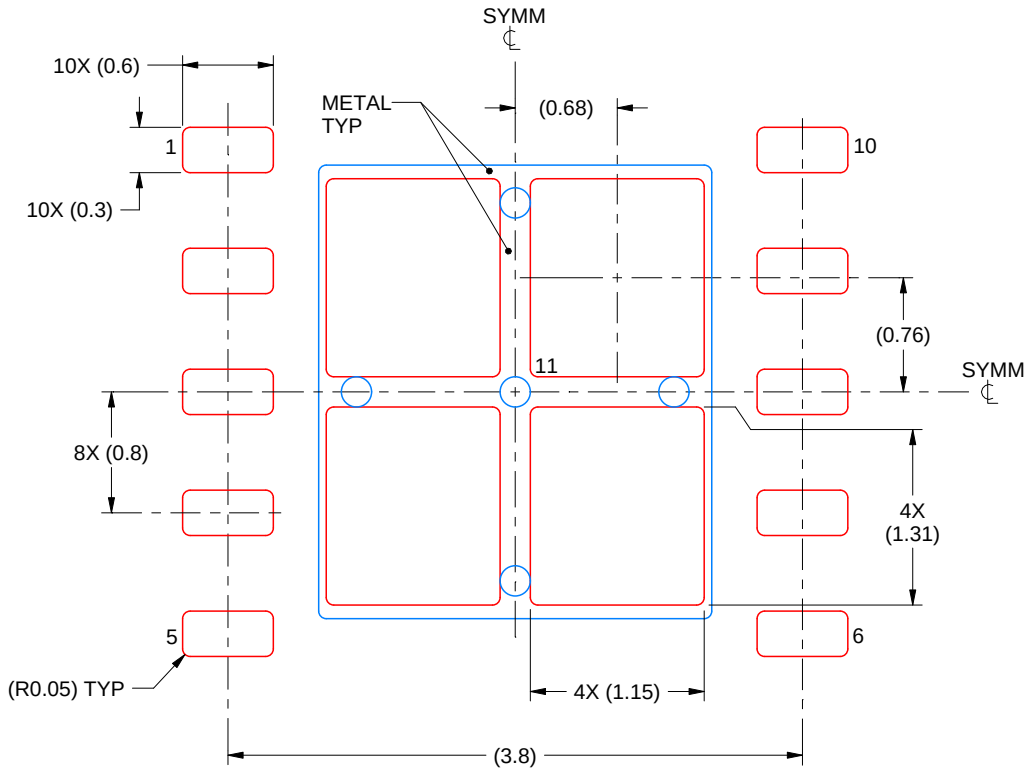


SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

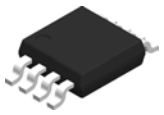
4218856/B 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

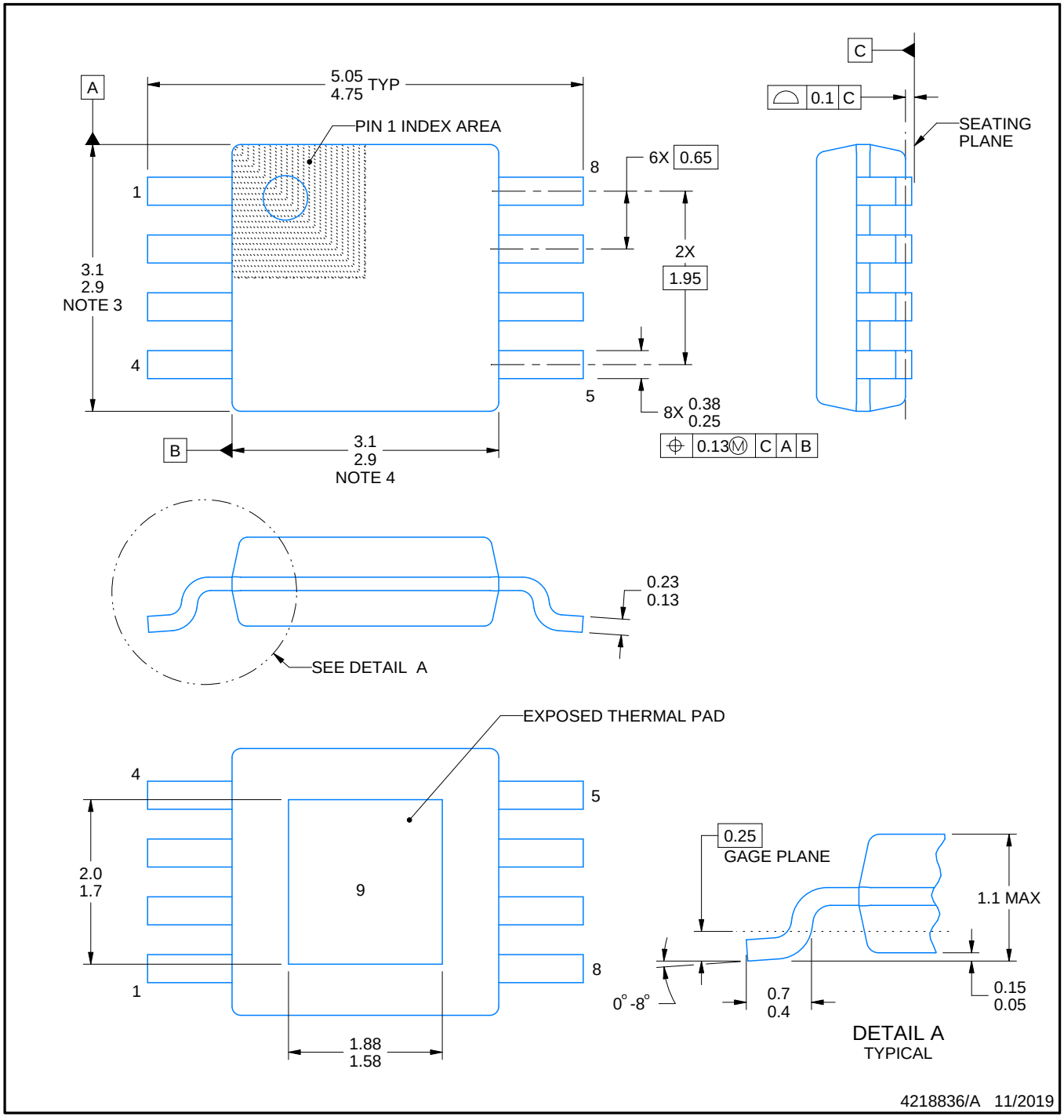
PACKAGE OUTLINE

DGN0008A



PowerPAD™ VSSOP - 1.1 mm max height

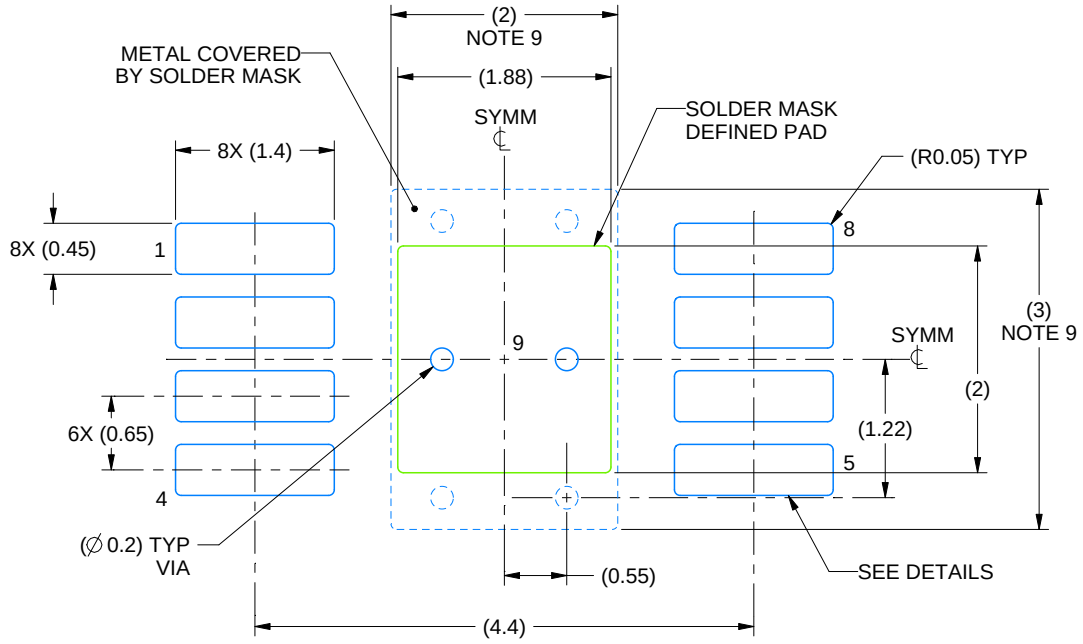
SMALL OUTLINE PACKAGE



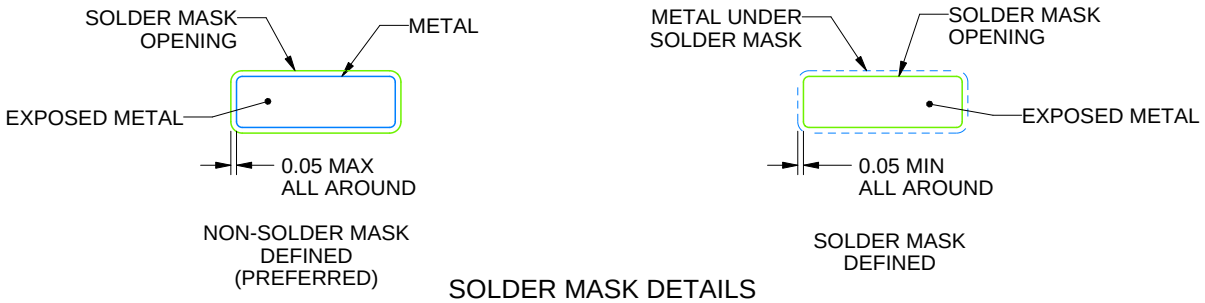
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4218836/A 11/2019

NOTES: (continued)

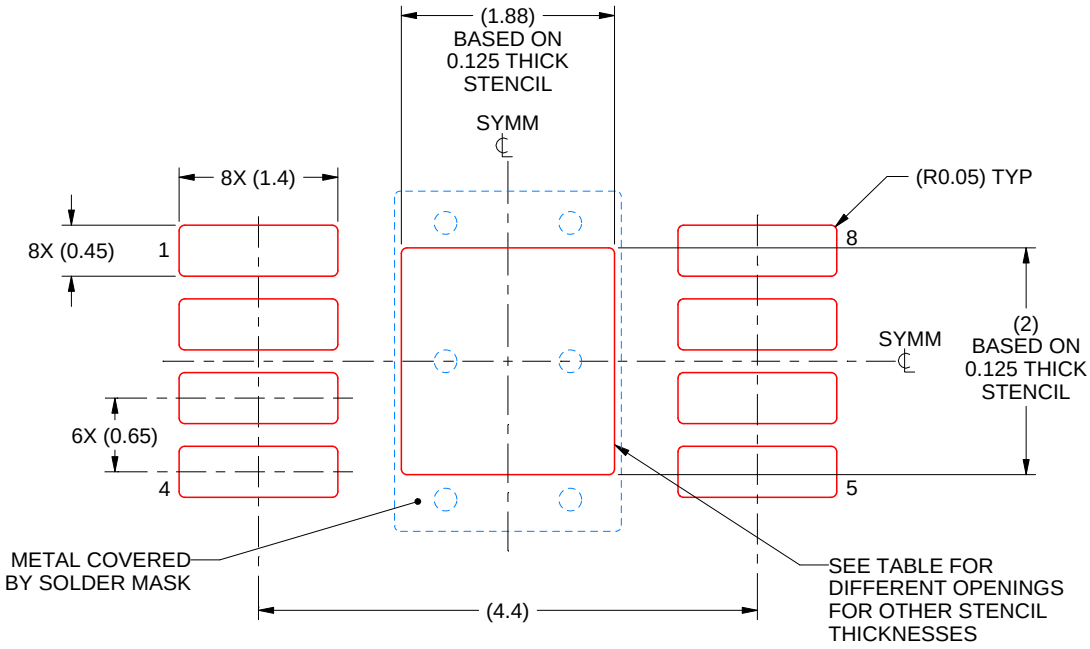
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



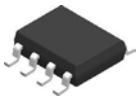
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.24
0.125	1.88 X 2.00 (SHOWN)
0.15	1.72 X 1.83
0.175	1.59 X 1.69

4218836/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

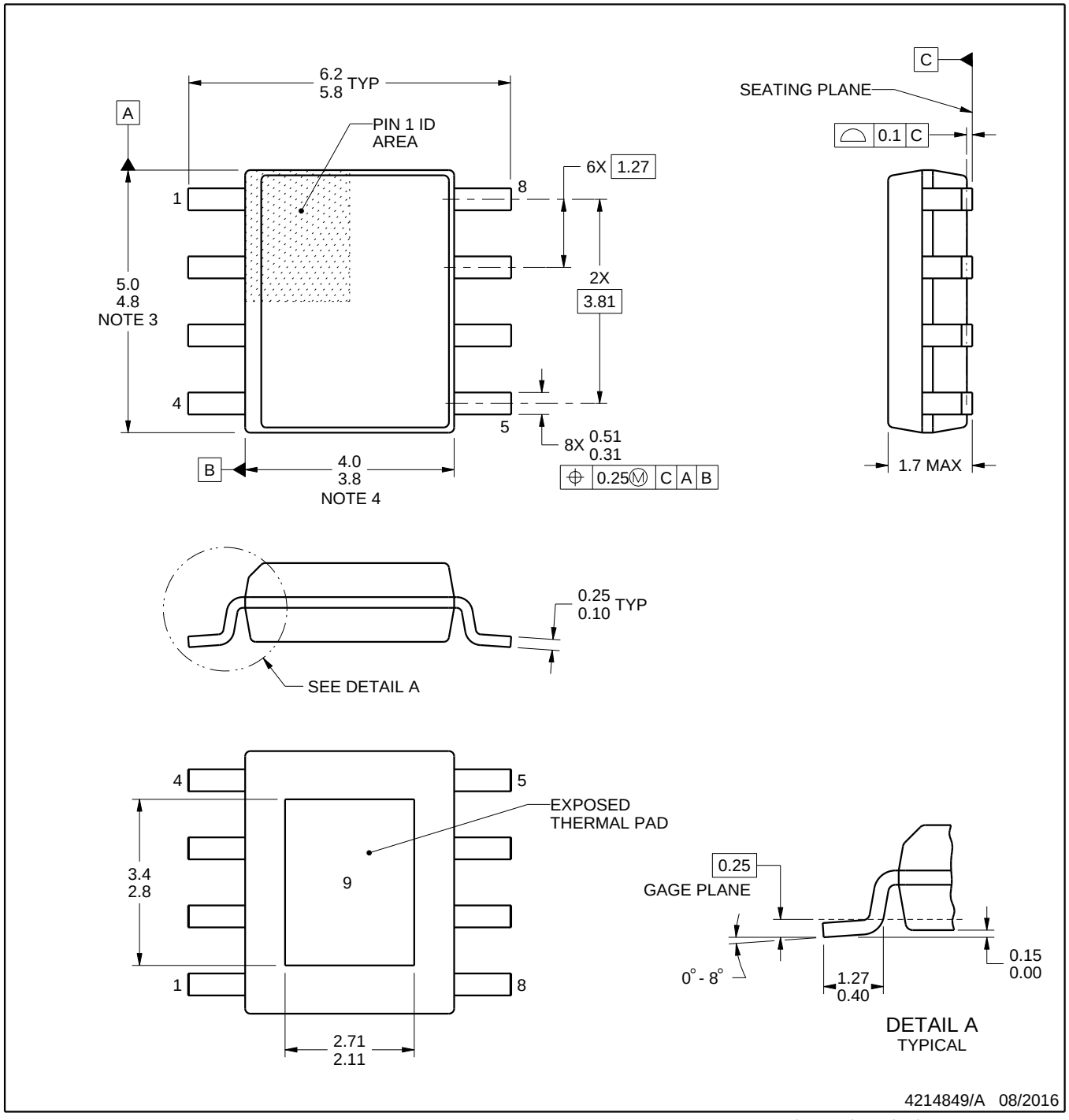


PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

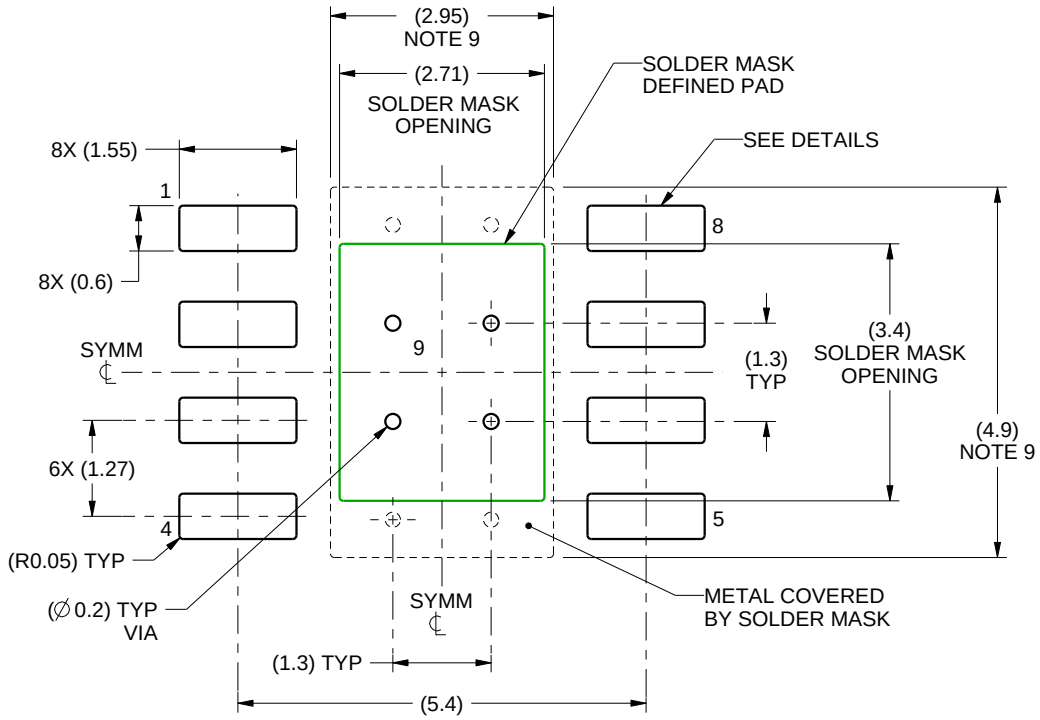
PLASTIC SMALL OUTLINE



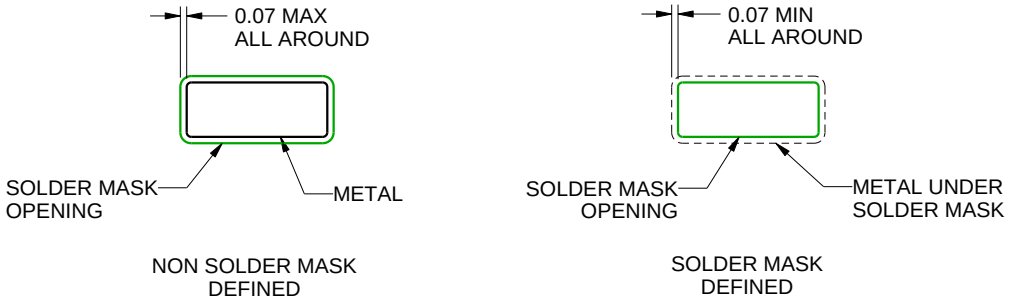
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

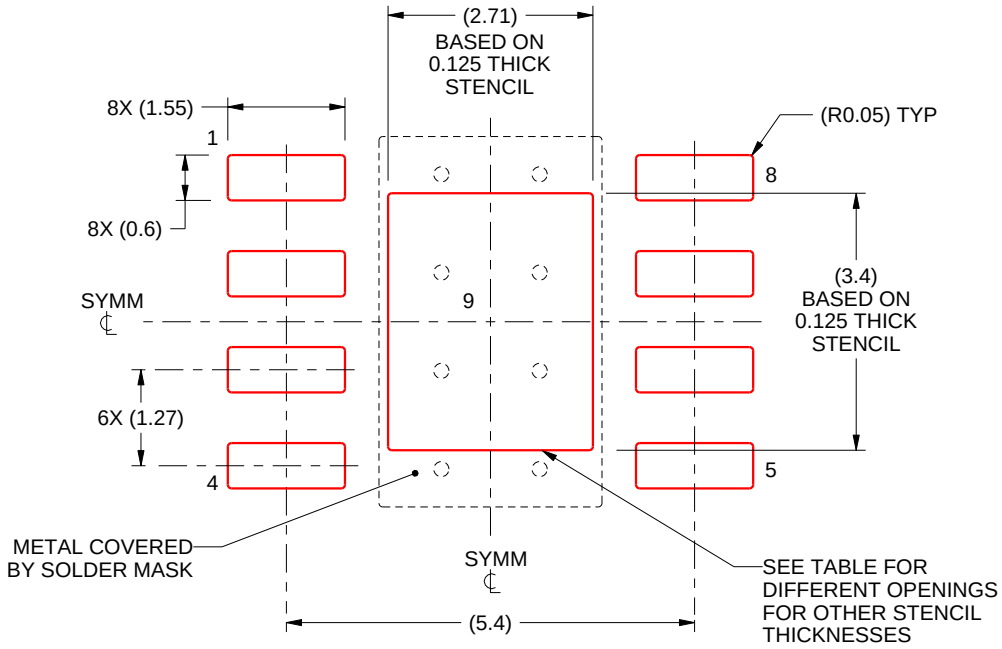
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

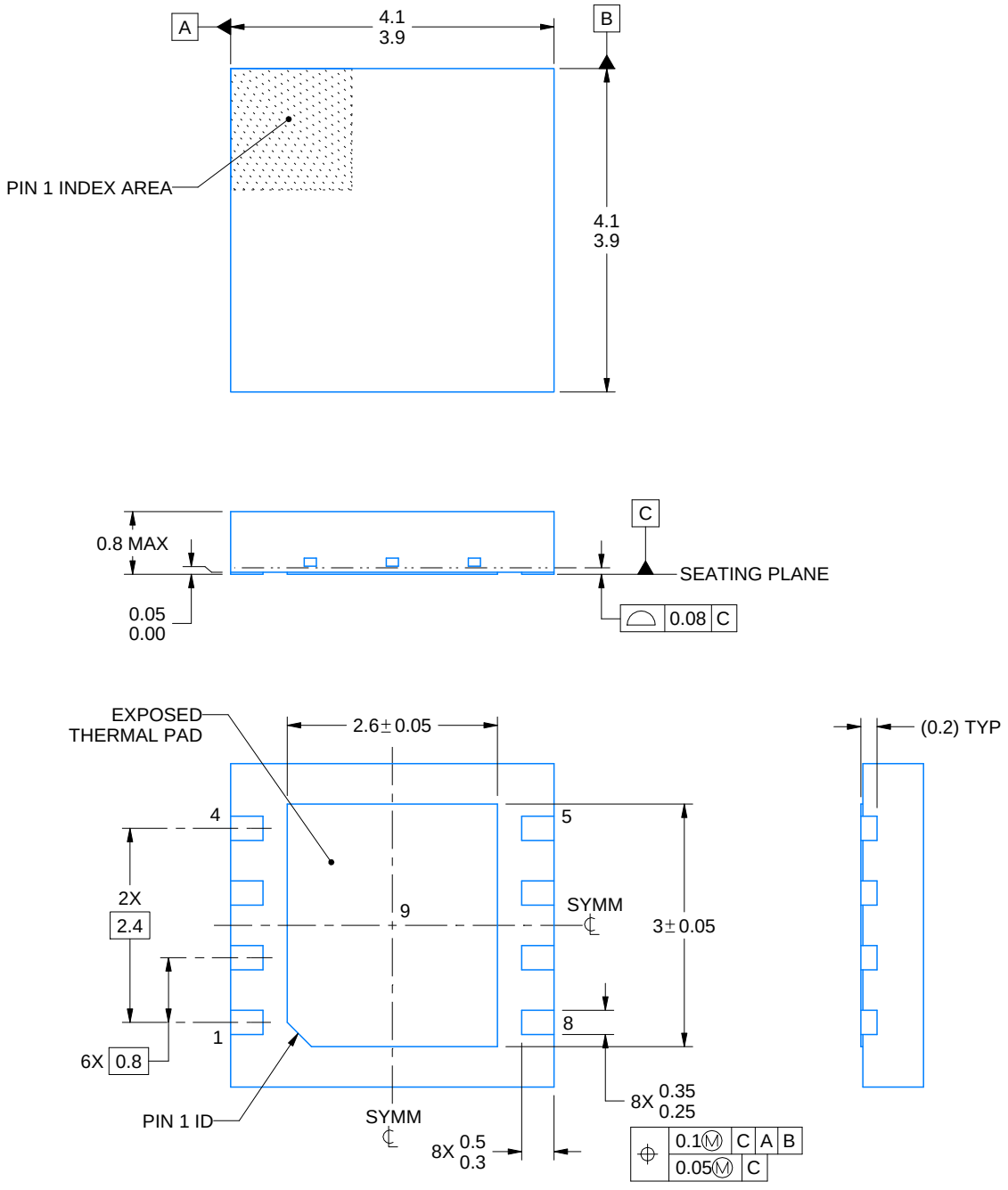
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

NGT0008A

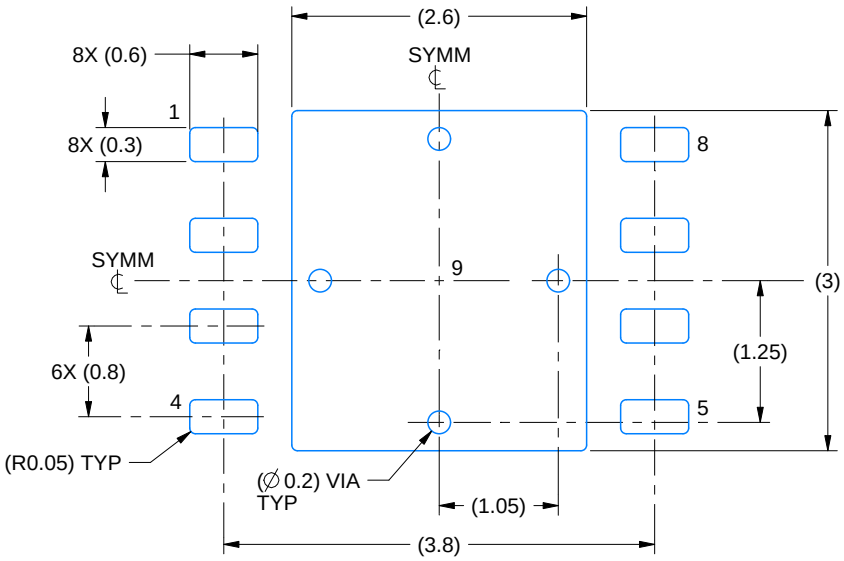
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

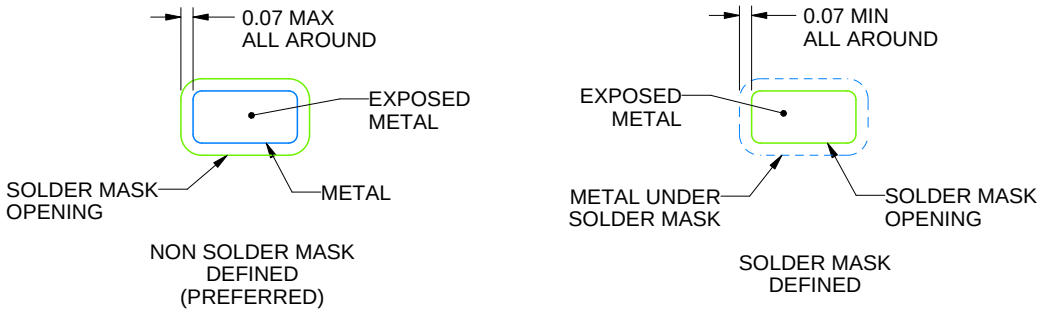


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

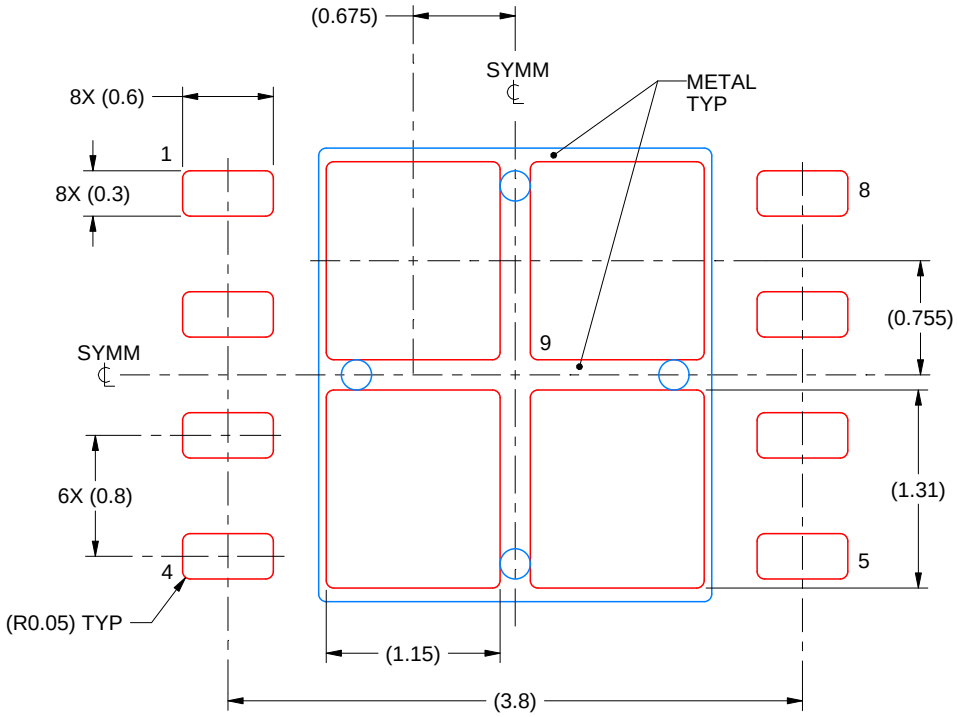


SOLDER MASK DETAILS

4214935/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



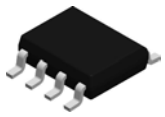
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214935/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

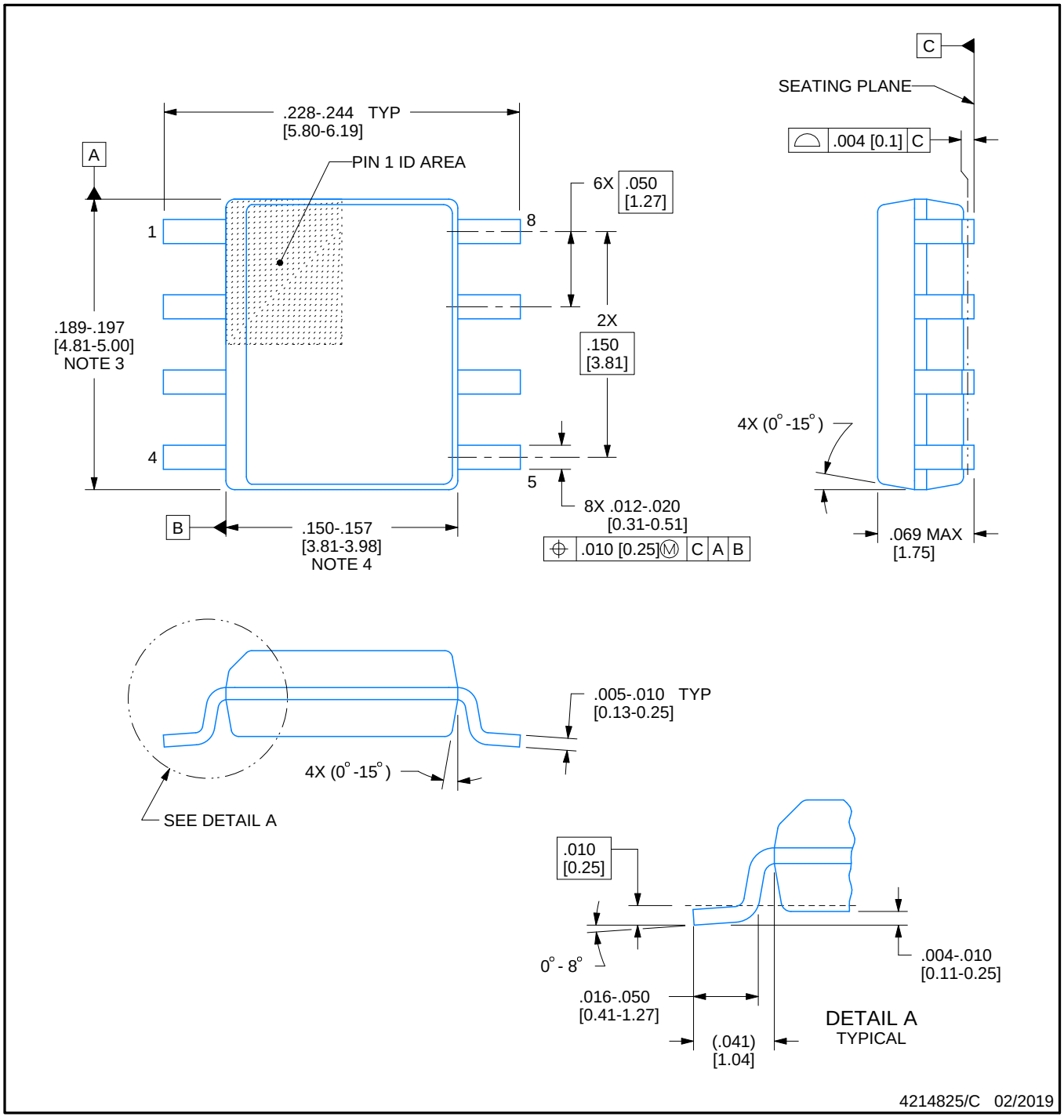


PACKAGE OUTLINE

D0008A

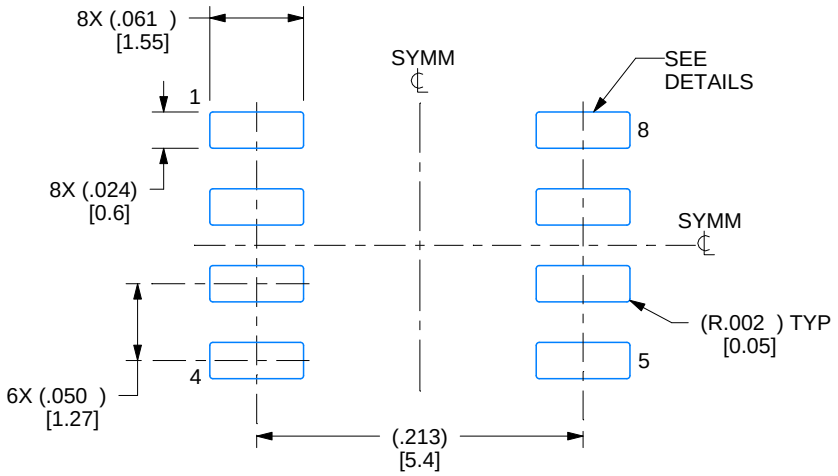
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

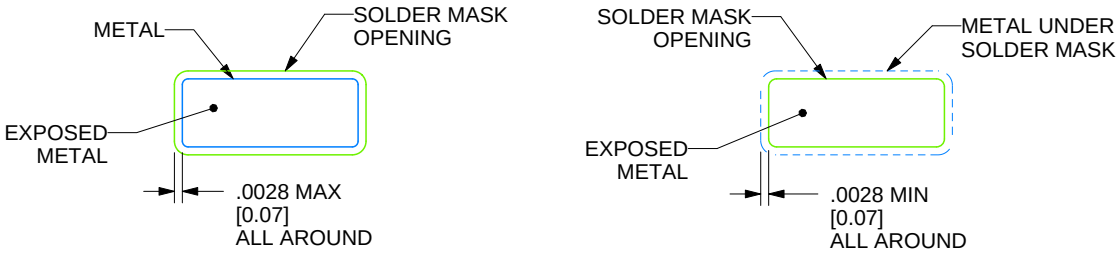


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

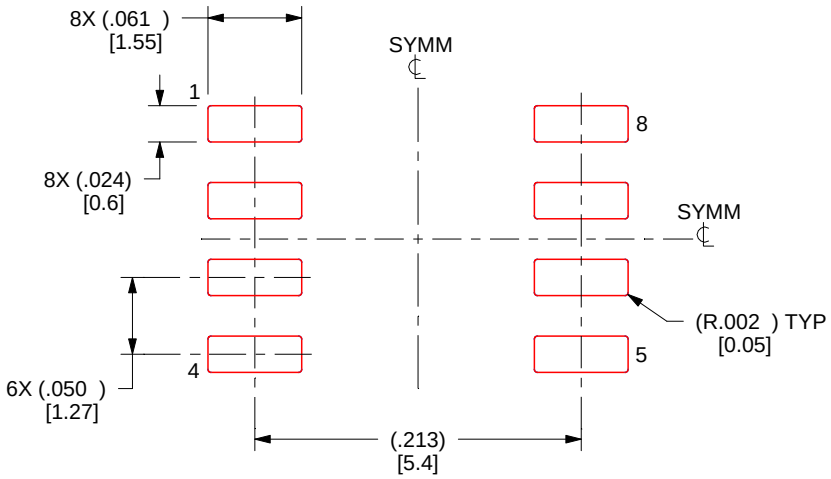
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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