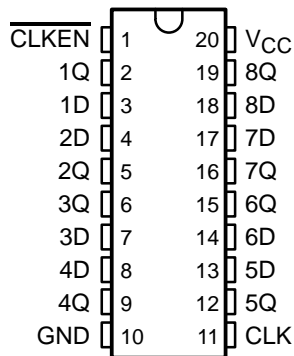


# SN54HCT377, SN74HCT377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

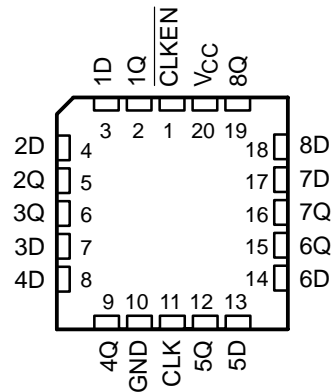
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- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible
- Contain Eight Flip-Flops With Single-Rail Outputs
- Clock Enable Latched to Avoid False Clocking
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

SN54HCT377 . . . J OR W PACKAGE  
SN74HCT377 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54HCT377 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

These devices are positive-edge-triggered D-type flip-flops. The 'HCT377 devices are similar to the 'HCT273 devices, but feature a latched clock-enable (CLKEN) input instead of a common clear.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse if CLKEN is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. These devices are designed to prevent false clocking by transitions at CLKEN.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74HCT377N	HCT377
	SOIC – DW	Tube	SN74HCT377DW	
		Tape and reel	SN74HCT377DWR	
-55°C to 125°C	CDIP – J	Tube	SNJ54HCT377J	SNJ54HCT377J
	CFP – W	Tube	SNJ54HCT377W	SNJ54HCT377W
	LCCC – FK	Tube	SNJ54HCT377FK	SNJ54HCT377FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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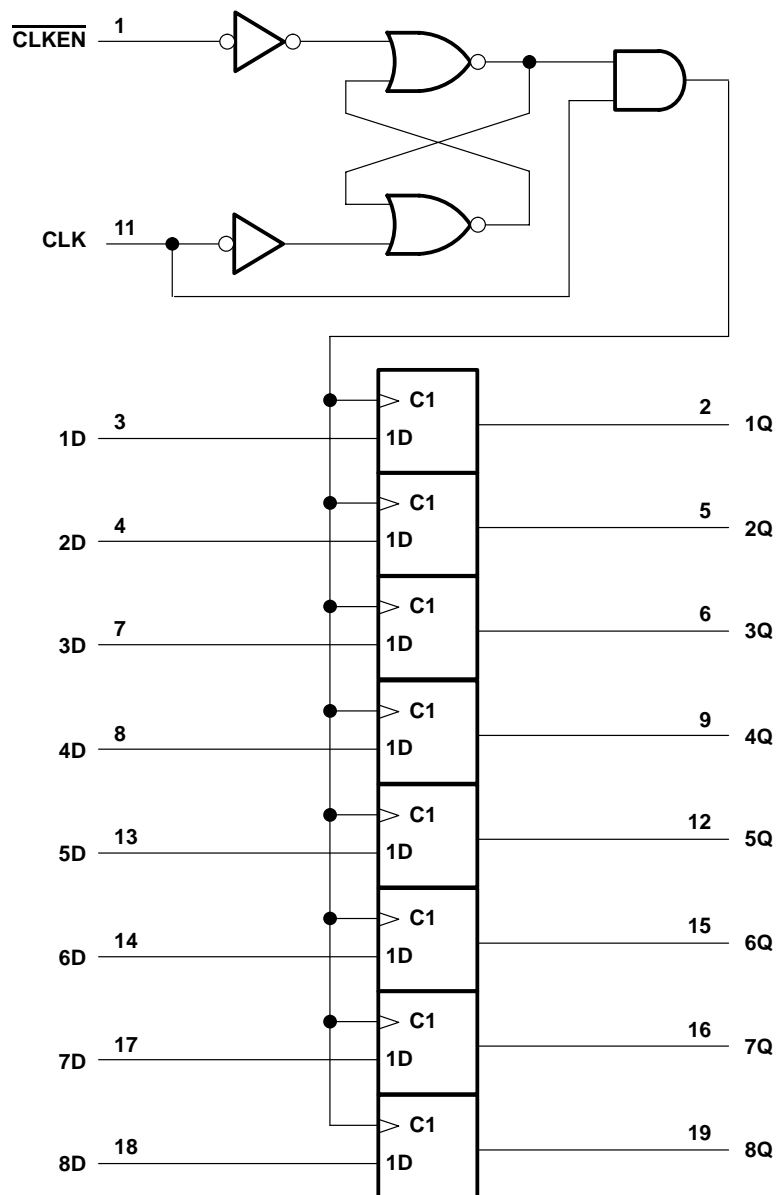
# SN54HCT377, SN74HCT377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

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FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
CLKEN	CLK	D	Q
H	X	X	Q <sub>0</sub>
L	↑	H	H
L	↑	L	L
X	L	X	Q <sub>0</sub>

## logic diagram (positive logic)



# SN54HCT377, SN74HCT377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package	58°C/W
N package	69°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

	SN54HCT377			SN74HCT377			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$			2			V
$V_{IL}$ Low-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$			0.8			V
$V_I$ Input voltage	0	$V_{CC}$		0	$V_{CC}$		V
$V_O$ Output voltage	0	$V_{CC}$		0	$V_{CC}$		V
$t_t$ Input transition (rise and fall) times	500			500			ns
$T_A$ Operating free-air temperature	–55	125		–40	85		°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HCT377		SN74HCT377		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\ \mu\text{A}$	4.5 V	4.4	4.499	4.4	4.4	V		
		$I_{OH} = -4\ \text{mA}$	4.5 V	3.98	4.30	3.7	3.84			
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\ \mu\text{A}$	4.5 V	0.001	0.1	0.1	0.1	V		
		$I_{OL} = 4\ \text{mA}$	4.5 V	0.17	0.26	0.4	0.33			
$I_I$	$V_I = V_{CC}$ or 0	5.5 V		±0.1	±100	±1000	±1000	nA		
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V			8	160	80	μA		
$\Delta I_{CC}^\ddagger$	One input at 0.5 V or 2.4 V, Other inputs at GND or $V_{CC}$	5.5 V		1.4	2.4	3	2.9	mA		
$C_i$		4.5 V to 5.5 V		3	10	10*	10	pF		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or  $V_{CC}$ .

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# SN54HCT377, SN74HCT377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HCT377		SN74HCT377		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		4.5 V	25	17	20			MHz	
			5.5 V	30	19	22				
t <sub>w</sub>	Pulse duration	CLK high or low	4.5 V	20	30	25			ns	
			5.5 V	18	28	23				
t <sub>su</sub>	Setup time before CLK↑	Data	4.5 V	12	18	15			ns	
			5.5 V	10	17	14				
		CLKEN high or low	4.5 V	12	18	15				
			5.5 V	10	17	14				
t <sub>h</sub>	Hold time data after CLK↑	Data	4.5 V	3	3	3			ns	
			5.5 V	3	3	3				
		CLKEN inactive or active	4.5 V	5	5	5				
			5.5 V	5	5	5				

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN54HCT377				UNIT	
				T <sub>A</sub> = 25°C			MIN		MAX
				MIN	TYP	MAX			
f <sub>max</sub>			4.5 V	25	31	17		MHz	
			5.5 V	30	37	19			
t <sub>pd</sub>	CLK	Any	4.5 V		15	30	45	ns	
			5.5 V		12	28	40		
t <sub>t</sub>		Any	4.5 V		8	15	22	ns	
			5.5 V		6	14	21		

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN74HCT377				UNIT	
				T <sub>A</sub> = 25°C			MIN		MAX
				MIN	TYP	MAX			
f <sub>max</sub>			4.5 V	25	31	20		MHz	
			5.5 V	30	37	22			
t <sub>pd</sub>	CLK	Any	4.5 V		15	30	38	ns	
			5.5 V		12	28	35		
t <sub>t</sub>		Any	4.5 V		8	15	19	ns	
			5.5 V		6	14	17		

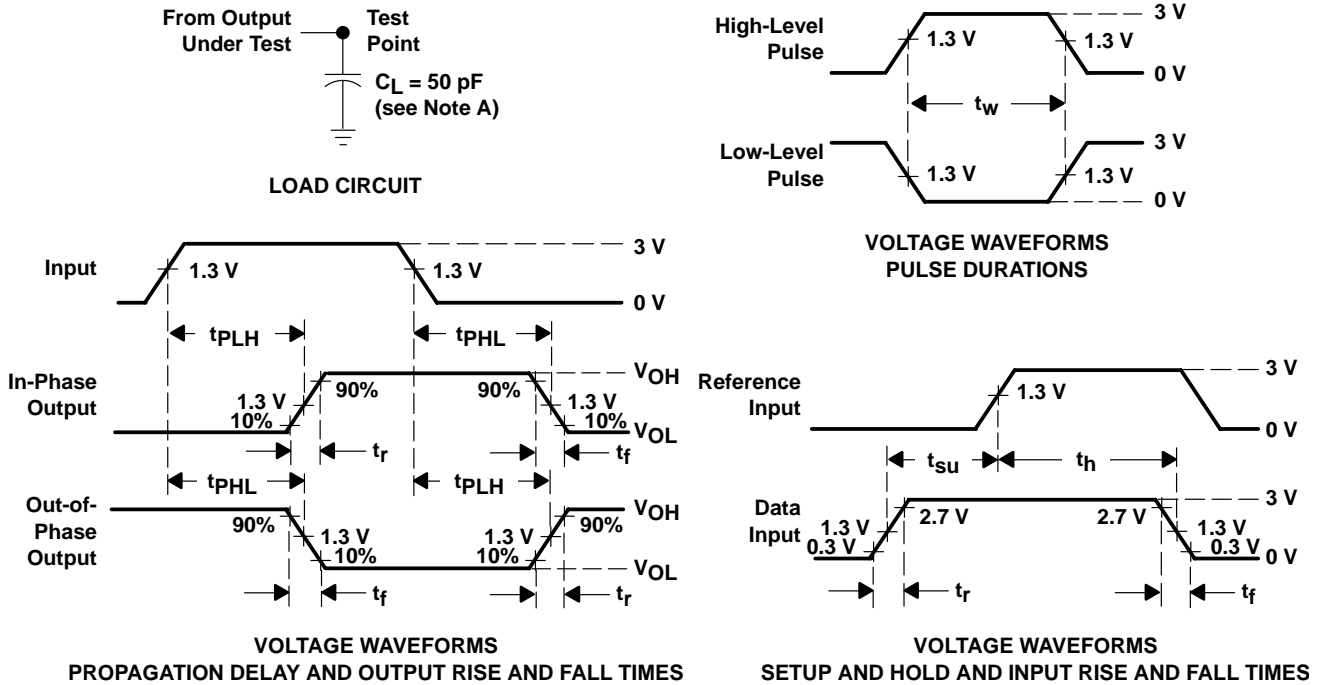
operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load	30	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. The outputs are measured one at a time with one input transition per measurement.
  - D. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT377DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT377	<a href="#">Samples</a>
SN74HCT377DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT377	<a href="#">Samples</a>
SN74HCT377N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT377N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

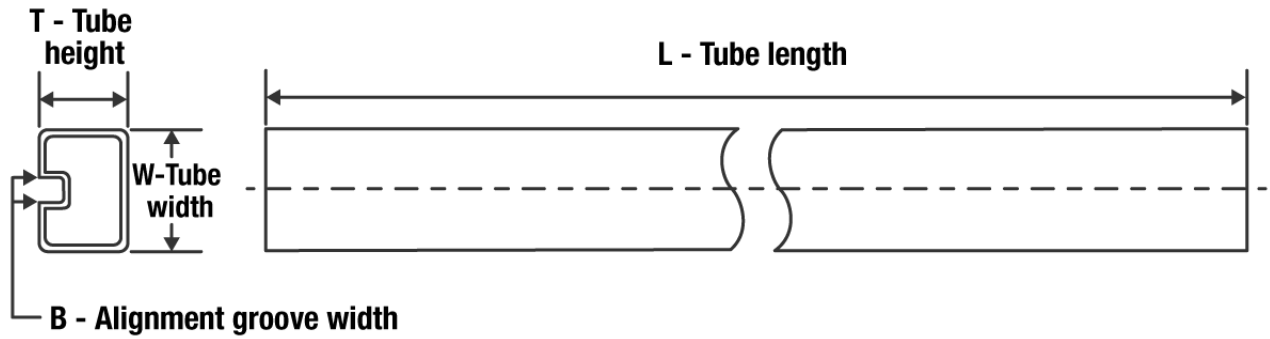
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT377DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT377DWR	SOIC	DW	20	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HCT377DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HCT377N	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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