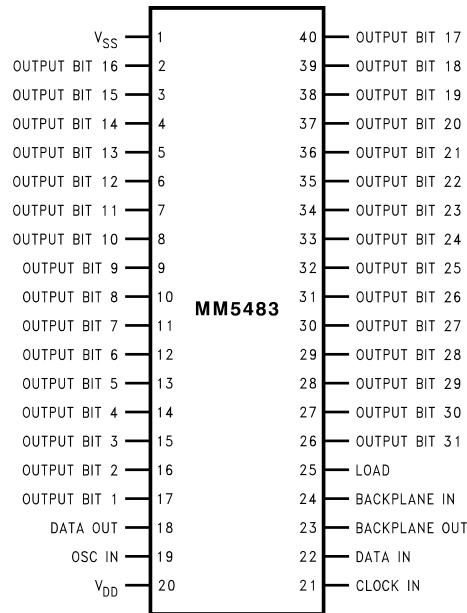


Connection Diagrams



**Figure 2. Dual-In-Line Package
Top View
See Package Number NFJ0040A**

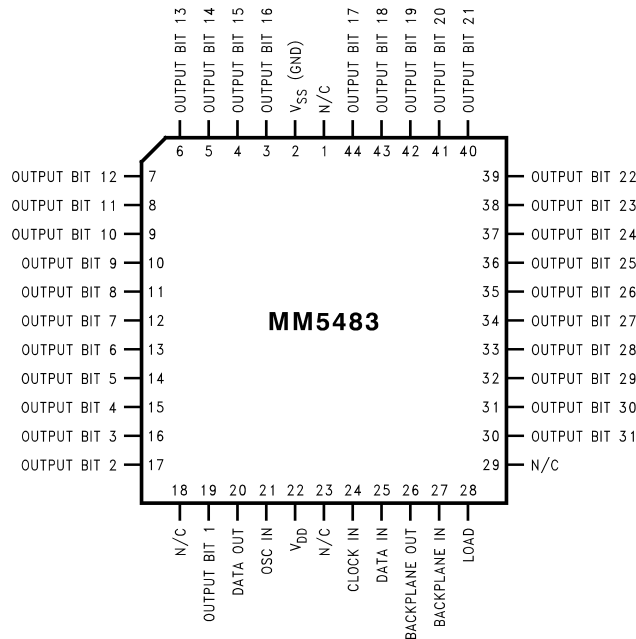


Figure 3. See Package Number FN0044A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Voltage at Any Pin	V_{SS} to $V_{SS} + 10V$
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Power Dissipation	300 mW at +85°C 350 mW at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	300°C

- (1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

DC Electrical Characteristics

T_A within operating range, $V_{DD} = 3.0V$ to $10V$, $V_{SS} = 0V$, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3.0		10	V
Average Supply Current, I_{DD}	All Outputs Bits = Open, Data Out = Open, BP_Out = Open, Clock In = 0V, Data In = 0V, Data Load = 0V, Osc In = 0V, BP_In = 32Hz				
	$V_{DD} = 3.0V$		1.5	2.5	μA
	$V_{DD} = 5.0V$			10	μA
	$V_{DD} = 10.0V$			40	μA
Input Voltage Levels Logic “0” Logic “1” Logic “0” Logic “1”	Load, Clock, Data				
	$V_{DD} = 5.0V$	2.4		0.9	V
	$V_{DD} = 5.0V$				V
	$V_{DD} = 3.0V$	2.0		0.4	V
$V_{DD} = 3.0V$				V	
Output Current Levels ⁽¹⁾ Segments and Data Out Sink Source	$V_{DD} = 3.0V$, $V_{OUT} = 0.3V$	20			μA
	$V_{DD} = 3.0V$, $V_{OUT} = 2.7V$	20			μA
BP Out Sink	$V_{DD} = 3.0V$, $V_{OUT} = 0.3V$	320			μA
BP Out Source	$V_{DD} = 3.0V$, $V_{OUT} = 2.7V$	320			μA

- (1) Output offset voltage is ± 50 mV with $C_{SEGMENT} = 250$ pF, $C_{BP} = 8750$ pF.

AC Electrical Characteristics

$V_{DD} \geq 4.7V$, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
f_C	Clock Frequency, $V_{DD} = 3V$			500	kHz
t_{CH}	Clock Period High	⁽¹⁾⁽²⁾ 500			ns
t_{CL}	Clock Period Low	500			ns
t_{DS}	Data Set-Up before Clock	300			ns
t_{DH}	Data Hold Time after Clock	100			ns
t_{LW}	Minimum Load Pulse Width	500			ns
t_{LTC}	Load to Clock	400			ns
t_{CDO}	Clock to Data Valid		400	750	ns

- (1) AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, $f = 500$ kHz, 50% \pm 10% duty cycle.
- (2) Clock input rise and fall times must not exceed 300 ms.

FUNCTIONAL DESCRIPTION

A block diagram for the MM5483 is shown in Figure 1 and a package pinout is shown in Figure 3. Figure 4 shows a possible 3-wire connection system with a typical signal format for Figure 4. Shown in Figure 5, the load input is an asynchronous input and lets data through from the shift register to the output buffers any time it is high. The load input can be connected to V_{DD} for 2-wire control as shown in Figure 6. In the 2-wire control mode, 31 bits (or less depending on the number of segments used) of data are clocked into the MM5483 in a short time frame (with less than 0.1 second there probably will be no noticeable flicker) with no more clocks until new information is to be displayed. If data was slowly clocked in, it can be seen to “walk” across the display in the 2-wire mode. An AC timing diagram can be seen in Figure 7. It should be noted that data out is not a TTL-compatible output.

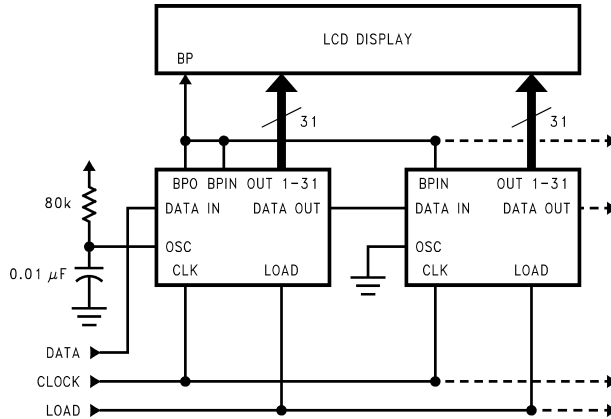


Figure 4. Three-Wire Control Mode

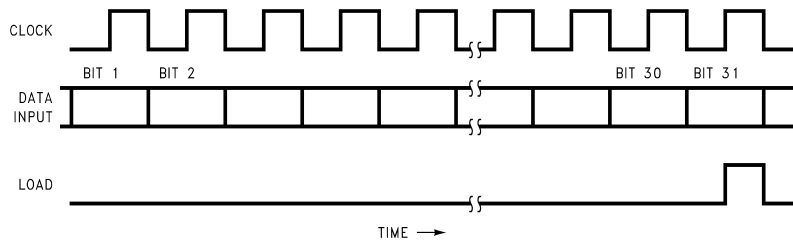


Figure 5. Data Format Diagram

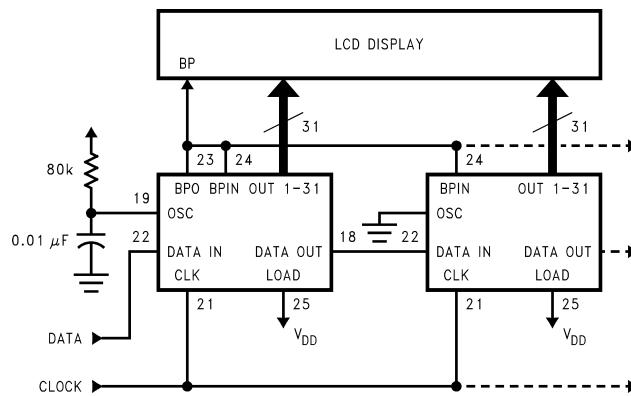


Figure 6. Two-Wire Control Mode

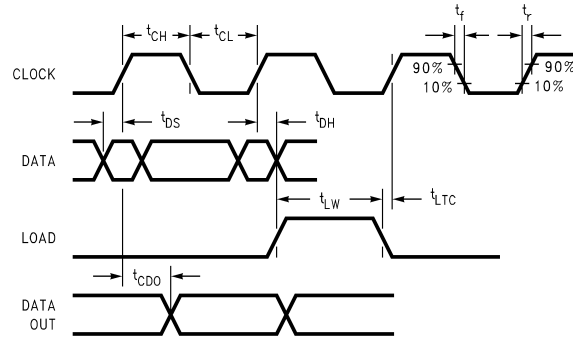


Figure 7. Timing Diagram

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MM5483V/NOPB	ACTIVE	PLCC	FN	44	25	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 85	MM5483V	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

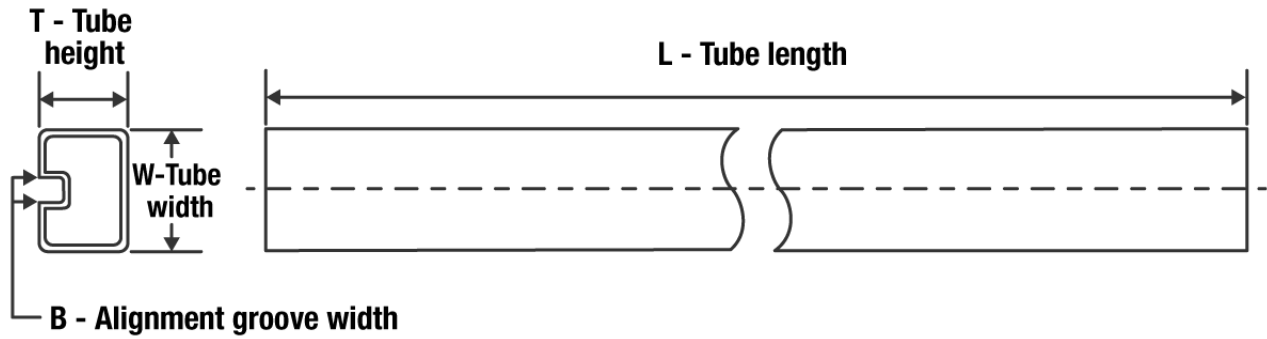
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

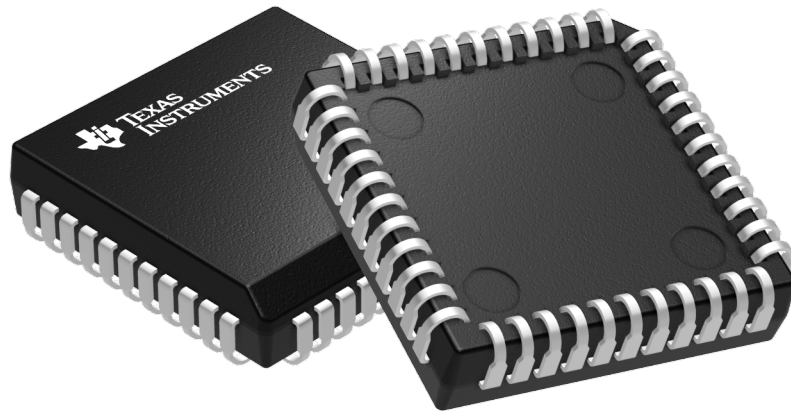
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MM5483V/NOPB	FN	PLCC	44	25	466	21	8001	15.74

GENERIC PACKAGE VIEW

FN 44

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040005-4/C

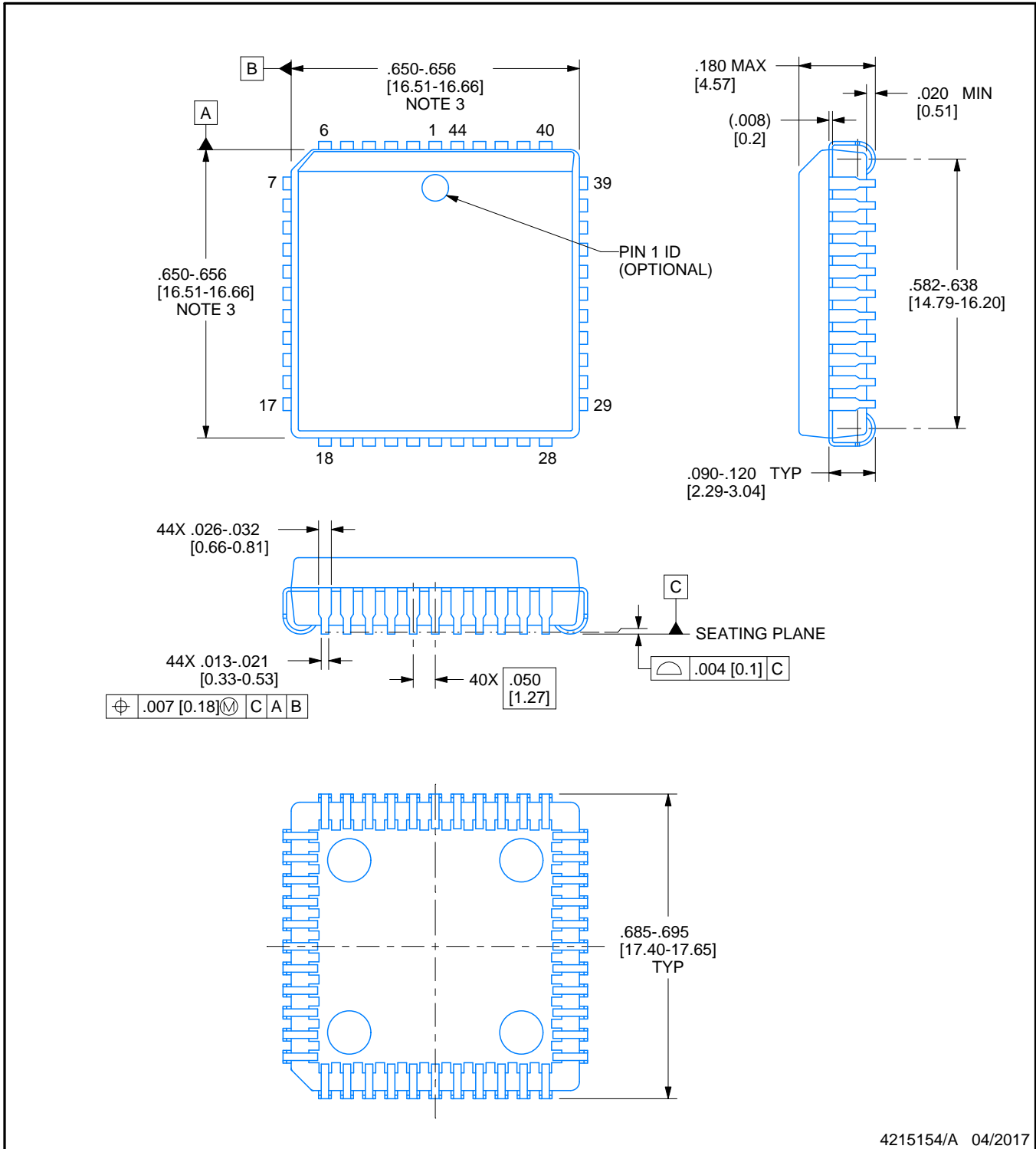


PACKAGE OUTLINE

FN0044A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



4215154/A 04/2017

NOTES:

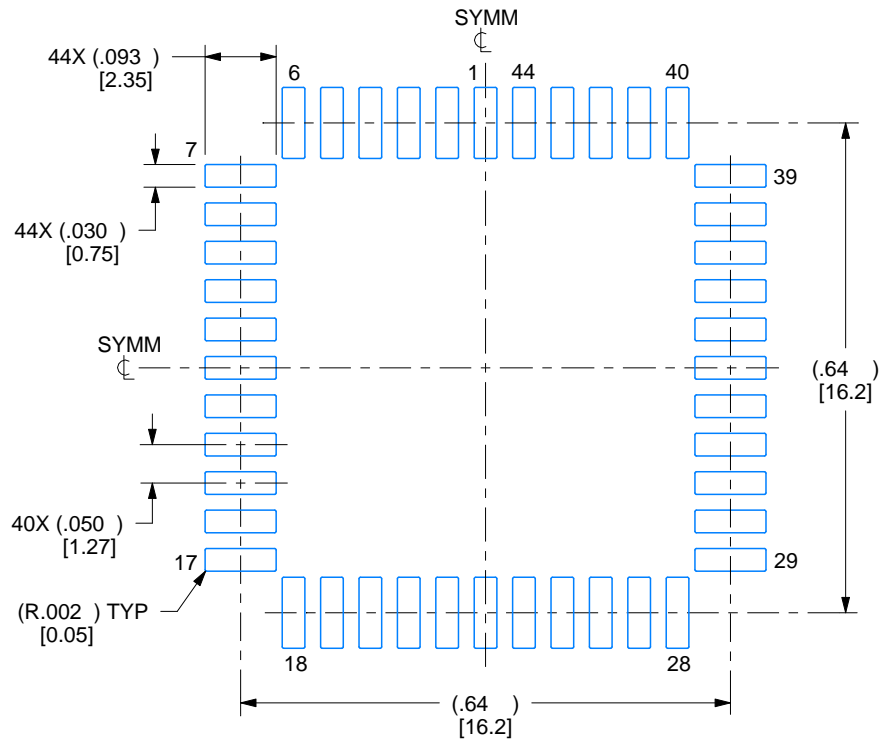
1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.

EXAMPLE BOARD LAYOUT

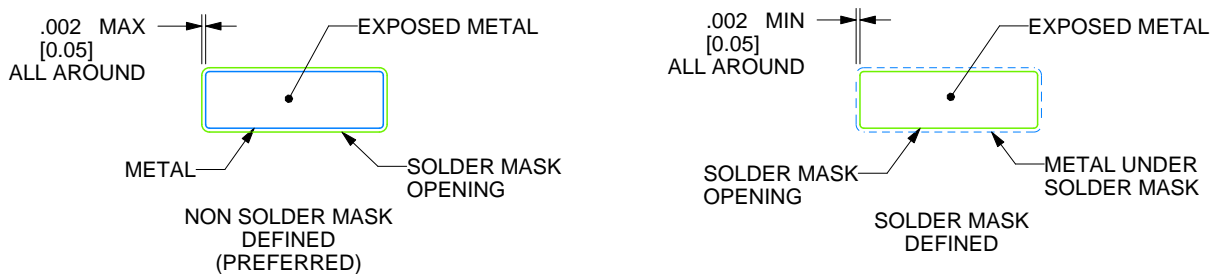
FN0044A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X



SOLDER MASK DETAILS

4215154/A 04/2017

NOTES: (continued)

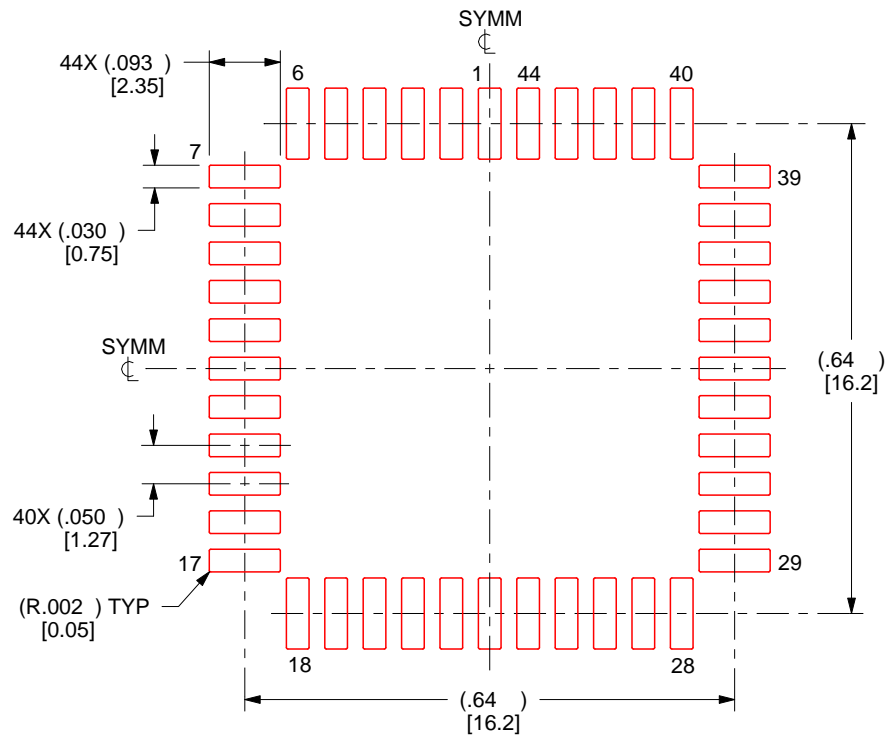
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

FN0044A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4215154/A 04/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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