具有无源连续波 (CW) 混频器和数字 I/Q 解调器，0.75nV/rtHz，14位，12位，65MSPS，158mW/CH 的完全集成，8 通道超声波模拟前端

查询样片: AFE5809

特性

- 8 通道完全模拟前端
  - LNA, VCAT, PGA, LPF, ADC和 CW 混频器
- 可编程增益低噪音放大器 (LNA)
  - 24，18，12dB 增益
  - 0.25，0.5，1V_{PP} 线性输入范围
  - 0.63，0.7，0.9nV/rtHz 输入参考噪音
  - 可编程主动终止
- 40dB 低噪音压控衰减器 (VACT)
- 24/30dB 可编程增益放大器 (PGA)
- 3rd 阶线性相位低通滤波器 (LPF)
  - 10，15，20，30MHz
- 14 位模数转换器 (ADC)
  - 65MSPS 时为 77dBFS 信噪比 (SNR)
  - LVDS 输出
- 噪声、功率优化（无数字解调器）
  - 0.75nV/rtHz，65MSPS 时为 158mW/CH
  - 1.1nV/rtHz，40MSPS 时为 101mW/CH
  - 在 CW 模式下为 80mW/CH
- 出色的器件到器件增益匹配
  - ±0.5dB（典型值）和 ±1dB（最大值）
- 模数转换器 (ADC) 之后的数字 I/Q 解调器
  - 宽范围解调频率
  - <1KHz 的频率分辨率
  - 抽取滤波器因数 M =1 至 32
  - 16xM 抽头有限冲击响应 (FIR) 抽取滤波器
  - 解调之后的低压差分信令 (LVDS) 速率衰减
  - 带有 32 个预设定参数的片载 RAM
- 低谐波失真
- 低频声纳信号处理
- 快速且持续的过载恢复
- 针对连续声波多普勒 (CWD) 的无源混频器
  - 低接近相位噪声-在低于 1KHz 至 2.5MHz 载波时为 156dBc/Hz
  - 1/16λ 的相位分辨率
  - 支持 16X，8X，4X 和 1X CW 时钟
  - 在 3rd和 5th 谐波上的 12dB 抑制
  - 灵活的输入时钟
- 小型封装：15mm x 9mm，135 球状引脚栅格阵列 (BGA) 封装

应用范围

- 医疗超声波成像
- 非侵入性评估设备
- 声纳应用

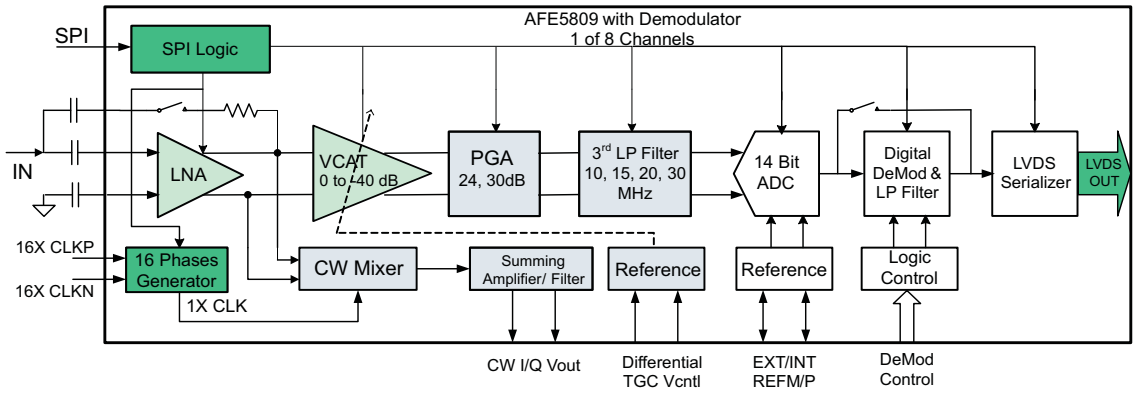


图 1. 方框图

说明

AFE5809 是一款高度集成的模拟前端 (AFE) 解决方案，此解决方案设计用于高性能和小型超声波系统。 AFE5809 集成了一个完整的时间增益控制 (TGC) 成像路径和一个连续波多普勒 (CWD) 路径。 它还使得用户可以选择不同的功率/噪音组合来优化系统性能。 因此，AFE5809 是一款不但适合于高端系统，而且也适用于便携式系统的超声波模拟前端解决方案。

AFE5809 包含 8 通道压控放大器 (VCA)，14 和 12 位模数转换器 (ADC) 和 CW 混频器。 此 VCA 包括低噪音放大器 (LNA)，电压控制衰减器 (VCAT)，可编程增益放大器 (PGA)，和低通滤波器 (LPF)。 LNA 增益可编程以支持 $250mV_{PP}$ 至 $1V_{PP}$ 的输入信号。 LNA 还支持可编程主动终止。 此超低噪音 VCAT 提供了一个 40dB 的衰减控制范围并提升了有益于谐波成像和近场成像的总体低增益 SNR。 PGA 提供了 24dB 和 30dB 的增益选项。 在 ADC 之前，一个 LPF 可被配置为 10MHz，15MHz，20MHz 或者 30MHz 以支持不同频率下的超声波应用。 此外，AFE5809 的信号链能够处理频率低于 100KHz 的信号，这使得 AFE5809 能够被用于声纳和医疗应用中。 AFE5809 中的高性能 14 位 / 65MSPS ADC 可实现 77dBFS SNR。 它确保了低链路增益下的出色 SNR。 ADC 的 LVDS 输出可实现小型化系统所需的灵活系统集成。

AFE5809 集成了一个低功耗无源混波器和一个低噪声加法放大器来实现片载 CWD 波束成型器。16 个可选相位延迟可被应用于每个模拟输入信号。 同时，执行一个特有的 3^{rd}和 5^{th} 次序谐波抑制滤波器来提高 CW 敏感度。

AFE5809 还包括一个数字相内和正交 (I/Q) 解调器和一个低通抽取滤波器。 解调块的主要用途是为了减少 LVDS 数据速率并提升系统总体功效。 I/Q 解调器可接受高达 65MSPS 采样速率和 14 位分辨率的 ADC 输出。 例如，数字解调和 4x 抽取滤波之后，相内或正交输出的数据速率被减少到 16.25MSPS，从而将数据分辨率提升至 16 位。因此，总体 LVDS 激励衰减系数可以为 2。这个解调器可被旁通，如果需要的话，也可将其完全断电。

AFE5809 采用 15mm × 9mm，135 引脚 BGA 封装并且其额定运行温度范围为 0°C 至 85°C。

注

日期编码在 2014 年之后的 AFE5809，即日期编码 > 41XXXX，具有以下可由寄存器 61[15,14,13] 启用的功能。 现有模拟性能保持不变。

- 61[13] 在 PGA 的 V2I 输入上启用一个额外电压钳位。 这限制了 PGA 上可见的过载信号数量。
- 61[14] 启用一个一阶 5MHz 低通 (LPF) 滤波器来抑制大于 5MHz 的信号或者高阶谐波。
- 61[15] 启用一个 -6dB PGA 钳位设置。 实际 PGA 输出少于 ADC 的满量程振幅 2Vpp。

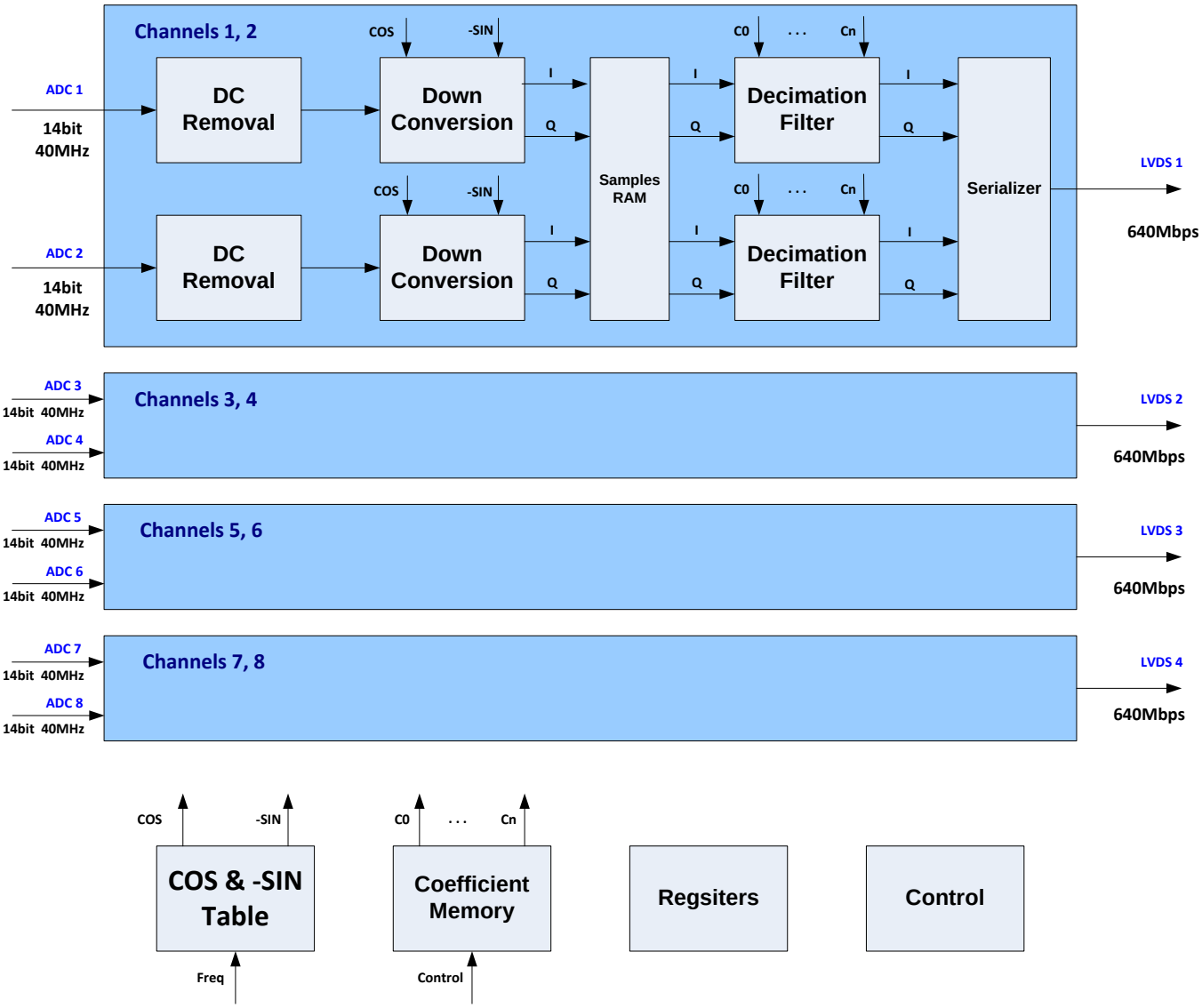


Figure 2. Digital Demodulator Block Diagram

PACKAGING/ORDERING INFORMATION(1)

PRODUCT	PACKAGE TYPE	OPERATING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
AFE5809	ZCF	0°C to 85°C	AFE5809ZCF	Tray, 160

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range	AVDD	–0.3	3.9	V
	AVDD_ADC	–0.3	2.2	V
	AVDD_5V	–0.3	6	V
	DVDD	–0.3	2.2	V
	DVDD_LDO	–0.3	1.6	V
Voltage between AVSS and LVSS		–0.3	0.3	V
Voltage at analog inputs and digital inputs		–0.3	min [3.6,AVDD+0.3]	V
Peak solder temperature(2)			260	°C
Maximum junction temperature (T_J), any condition			105	°C
Storage temperature range		–55	150	°C
Operating temperature range		0	85	°C
ESD Ratings	Human Body Model (HBM)		2000	V
	Charged Device Model (CDM)		500	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) Device complies with JSTD-020D.

THERMAL INFORMATION

THERMAL METRIC(1)		AFE5809 BGA 135 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	34.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	5	
θ_{JB}	Junction-to-board thermal resistance	11.5	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	10.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNIT
AVDD	3.15	3.6	V
AVDD_ADC	1.7	1.9	V
DVDD	1.7	1.9	V
DVDD_LDO1/2 (Internal Generated)	1.2	1.4	V
AVDD_5V	4.75	5.5	V
Ambient Temperature, T_A	0	85	°C

PINOUT INFORMATION

Top View
ZCF (BGA-135)

	1	2	3	4	5	6	7	8	9
A	AVDD	INP8	INP7	INP6	INP5	INP4	INP3	INP2	INP1
B	CM_BYP	ACT8	ACT7	ACT6	ACT5	ACT4	ACT3	ACT2	ACT1
C	AVSS	INM8	INM7	INM6	INM5	INM4	INM3	INM2	INM1
D	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	AVDD
E	CW_IP_AMPINP	CW_IP_AMPINM	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	AVDD
F	CW_IP_OUTM	CW_IP_OUTP	AVSS	AVSS	AVSS	AVSS	AVSS	CLKP_16X	CLKM_16X
G	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	CLKP_1X	CLKM_1X
H	CW_QP_OUTM	CW_QP_OUTP	AVSS	AVSS	AVSS	AVSS	AVSS	PDN_GLOBAL	RESET
J	CW_QP_AMPINP	CW_QP_AMPINM	AVSS	AVSS	AVSS	AVDD_ADC	AVDD_ADC	PDN_VCA	SCLK
K	AVDD	AVDD_5V	VCNTLP	VCNTLM	VHIGH	AVSS	DNC	AVDD_ADC	SDATA
L	CLKP_ADC	CLKM_ADC	AVDD_ADC	REFM	DNC	LDO_EN	TX_SYNC_IN	PDN_ADC	SEN
M	AVDD_ADC	AVDD_ADC	VREF_IN	REFP	DNC	LDO_SETV	SPI_DIG_EN	DNC	SDOUT
N	D8P	D8M	DVDD	DVDD_LDO1	DVSS	DVDD_LDO2	DVDD	D1M	D1P
P	D7M	D6M	D5M	FCLKM	DVSS	DCLKM	D4M	D3M	D2M
R	D7P	D6P	D5P	FCLKP	DVSS	DCLKP	D4P	D3P	D2P

PIN FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
B9 to B2	ACT1...ACT8	ActI've termination input pins for CH1 to 8.
A1, D8, D9, E8, E9, K1	AVDD	3.3 V Analog supply for LNA, VCAT, PGA, LPF and CWD blocks.
K2	AVDD_5V	5 V Analog supply for LNA, VCAT, PGA, LPF and CWD blocks.
J6, J7, K8, L3, M1, M2	AVDD_ADC	1.8 V Analog power supply for ADC.
C1, D1 to D7, E3 to E7, F3 to F7, G1 to G7, H3 to H7,J3 toJ5, K6	AVSS	Analog ground.
L2	CLKM_ADC	Negative input of differential ADC clock. In the single-end clock mode, it can be tied to GND directly or through a 0.1 µF capacitor.
L1	CLKP_ADC	Positive input of differential ADC clock. In the single-end clock mode, it can be tied to clock signal directly or through a 0.1 µF capacitor.
F9	CLKM_16X	Negative input of differential CW 16X clock. Tie to GND when the CMOS clock mode is enabled. In the 4X, and 8X CW clock modes, this pin becomes the 4X or 8X CLKM input. In the 4X and 8X CW clock modes, this pin becomes the 4X or 8X CLKM input. In the 1X CW clock mode, this pin becomes the in-phase 1X CLKM for the CW mixer. Can be floated if CW mode is not used. See register 0x36[11:10].
F8	CLKP_16X	Positive input of differential CW 16X clock. In 4X, and 8X clock modes, this pin becomes the 4X, and 8X CLKP input. In the 1X CW clock mode, this pin becomes the in-phase 1X CLKP for the CW mixer. Can be floated if CW mode is not used. See register 0x36[11:10].
G9	CLKM_1X	Negative input of differential CW 1X clock. Tie to GND when the CMOS clock mode is enabled (Refer to Figure 105 for details). In the 1X clock mode, this pin is the quadrature-phase 1X CLKM for the CW mixer. Can be floated if CW mode is not used.
G8	CLKP_1X	Positive input of differential CW 1X clock. In the 1X clock mode, this pin is the quadrature-phase 1X CLKP for the CW mixer. Can be floated if CW mode is not used.
B1	CM_BYP	Bias voltage and bypass to ground. 1µF is recommended. To suppress the ultra low frequency noise, 10µF can be used.
E2	CW_IP_AMPINM	Negative differential input of the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINM and CW_IP_OUTP. This pin provides the current output for the CW mixer. This pin becomes the CH7 PGA negative output when PGA test mode is enabled. Can be floated if not used.

PIN FUNCTIONS (continued)

PIN		DESCRIPTION
NO.	NAME	
E1	CW_IP_AMPINP	Positive differential input of the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINP and CW_IP_OUTM. This pin provides the current output for the CW mixer. This pin becomes the CH7 PGA positive output when PGA test mode is enabled. Can be floated if not used.
F1	CW_IP_OUTM	Negative differential output for the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINP and CW_IP_OUTPM. Can be floated if not used.
F2	CW_IP_OUTP	Positive differential output for the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINM and CW_IP_OUTP. Can be floated if not used.
J2	CW_QP_AMPINM	Negative differential input of the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINM and CW_QP_OUTP. This pin provides the current output for the CW mixer. This pin becomes CH8 PGA negative output when PGA test mode is enabled. Can be floated if not used.
J1	CW_QP_AMPINP	Positive differential input of the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINP and CW_QP_OUTM. This pin provides the current output for the CW mixer. This pin becomes CH8 PGA positive output when PGA test mode is enabled. Can be floated if not used.
H1	CW_QP_OUTM	Negative differential output for the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINP and CW_QP_OUTM. Can be floated if not used.
H2	CW_QP_OUTP	Positive differential output for the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINM and CW_QP_OUTP. Can be floated if not used.
N8, P9~P7, P3 to P1, N2	D1M to D8M	ADC CH1 to 8 LVDS negative outputs
N9, R9~R7, R3 to R1, N1	D1P to D8P	ADC CH1 to 8 LVDS positive outputs
P6	DCLKM	LVDS bit clock (7x) negative output
R6	DCLKP	LVDS bit clock (7x) positive output
N3, N7	DVDD	ADC digital and I/O power supply, 1.8 V
N5, P5, R5	DVSS	ADC digital ground
N4, N6	DVDD_LDO1, DVDD_LDO2	Demodulator digital power supply generated internally. These two pins should be separated on PCB and decoupled respectively with 0.1μF capacitors.
P4	FCLKM	LVDS frame clock (1X) negative output
R4	FCLKP	LVDS frame clock (1X) positive output
C9 to C2	INM1…INM8	CH1 to 8 complimentary analog inputs. Bypass to ground with ≥ 0.015μF capacitors. The HPF response of the LNA depends on the capacitors.
A9 to A2	INP1...INP8	CH1to 8 analog inputs. AC couple to inputs with ≥ 0.1μF capacitors.
L6	LDO_EN	Must be tied to 1.8 V DVDD.
M6	LDO_SETV	Must be tied to 1.8 V DVDD.
L8	PDN_ADC	ADC partial (fast) power down control pin with an internal pull down resistor of 100 kΩ. Active High. Either 1.8 V or 3.3 logic level can be used.
J8	PDN_VCA	VCA partial (fast) power down control pin with an internal pull down resistor of 20 kΩ. Active High. 3.3 V logic level should be used.
H8	PDN_GLOBAL	Global (complete) power-down control pin for the entire chip with an internal pull down resistor of 20 kΩ. Active High. 3.3 V logic level should be used.
L4	REFM	0.5 V reference output in the internal reference mode. Must leave floated in the internal reference mode. Adding a test point on the PCB is recommended for monitoring the reference output
M4	REFP	1.5 V reference output in the internal reference mode. Must leave floated in the internal reference mode. Adding a test point on the PCB is recommended for monitoring the reference output
H9	RESET	Hardware reset pin with an internal pull-down resistor of 20 kΩ. Active high. 3.3 logic level can be used.
J9	SCLK	Serial interface clock input with an internal pull-down resistor of 20 kΩ. This pin is connected to both ADC and VCA. 3.3 V logic should be used.
K9	SDATA	Serial interface data input with an internal pull-down resistor of 20 kΩ. This pin is connected to both ADC and VCA. 3.3 V logic should be used.

PIN FUNCTIONS (continued)

PIN		DESCRIPTION
NO.	NAME	
M9	SDOUT	Serial interface data readout. High impedance when readout is disabled. This pin is connected to ADC only. 1.8 V logic can be used.
L9	SEN	Serial interface enable with an internal pull up resistor of 20 kΩ. Active low. This pin is connected to both ADC and VCA. 3.3V logic should be used.
M7	SPI_DIG_EN	Serial interface enable for the digital demodulator memory space. SPI_DIG_EN pin is required to be set to '0' during SPI transactions to demodulator registers. Each transaction starts by setting SEN as '0' and terminates by setting it back to '1' (similar to other register transactions). Pull up internally through a 20 KΩ resistor. This pin is connected to both ADC and VCA. 3.3V logic should be used.
L7	TX_SYNC_IN	System trig signal input. It indicates the start of signal transmission. Either 3. 3 V or 1. 8 V logic level can be used.
K4	VCNTLM	Negative differential attenuation control pin.
K3	VCNTLP	Positive differential attenuation control pin
K5	VHIGH	Bias voltage; bypass to ground with ≥ 1 µF.
M3	VREF_IN	ADC 1.4V reference input in the external reference mode; bypass to ground with 0.1µF.
K7,L5, M5, M8	DNC	Do not connect. Must leave floated

ELECTRICAL CHARACTERISTICS

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14Bit, sample rate = 65MSPS, LPF Filter = 15 MHz, low noise mode, V_{OUT} = –1 dBFS, Single-ended V_{CNTL} mode, VCNTLM = GND, ADC configured in internal reference mode, internal 500 Ω CW feedback resistor, CMOS CW clocks, at ambient temperature T_A = 25°C, Digital demodulator is disabled unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
TGC FULL SIGNAL CHANNEL (LNA+VCAT+LPF+ADC)						
en (RTI)	Input voltage noise over LNA Gain(low noise mode)	Rs = 0Ω, f = 2 MHz, LNA = 24, 18, 12 dB, PGA = 2 4dB		0.76, 0.83, 1.16		nV/rtHz
		Rs = 0 Ω, f = 2 MHz,LNA = 24, 18, 12 dB, PGA = 30 dB		0.75, 0.86, 1.12		
	Input voltage noise over LNA Gain(low power mode)	Rs = 0 Ω, f = 2 MHz,LNA = 24, 18, 12 dB, PGA = 24 dB		1.1, 1.2, 1.45		nV/rtHz
		Rs = 0 Ω, f = 2 MHz, LNA = 24, 18, 12 dB, PGA = 30 dB		1.1, 1.2, 1.45		
	Input Voltage Noise over LNA Gain(Medium Power Mode)	Rs = 0 Ω, f = 2 MHz,LNA = 24, 18, 12 dB, PGA = 24 dB		1, 1.05, 1.25		nV/rtHz
		Rs = 0 Ω, f = 2 MHz, LNA = 24, 18, 12 dB, PGA = 30 dB		0.95, 1, 1.2		
en (RTI)	Input voltage noise at low frequency	f = 100 KHz, INM Cap=1uF, PGA integrator disabled		0.9		nV/rtHz
	Input referred current noise	Low Noise Mode/Medium Power Mode/Low Power Mode		2.7, 2.1, 2		pA/rtHz
NF	Noise figure	Rs = 200Ω, 200Ω active termination, PGA=24dB,LNA = 12, 18, 24 dB		3.85, 2.4, 1.8		dB
		Rs = 100 Ω, 100 Ω active termination, PGA = 2 4dB,LNA = 12, 18, 24 dB		5.3, 3.1, 2.3		dB
NF	Noise figure	Rs = 500 Ω, 1KΩ, no terminaiton, Low NF mode is enabled (Reg53[9]=1)		0.94, 1.08		dB
NF	Noise figure	Rs=50Ω/200Ω, no terminaiton, Low noise mode (Reg53[9]=0)		2.35, 1.05		dB
V_{MAX}	Maximum Linear Input Voltage	LNA gain = 24, 18, 12 dB		250, 500, 1000		mVpp
V_{CLAMP}	Clamp Voltage	Reg52[10:9] = 0, LNA = 24, 18, 12 dB		350, 600, 1150		
	PGA Gain	Low noise mode		24, 30		dB
		Medium/Low power mode		24, 28.5		
	Total gain	LNA = 2 4dB, PGA = 30 dB, Low noise mode		54		dB
		LNA = 24 dB, PGA = 30 dB, Med power mode		52.5		
		LNA = 24 dB, PGA = 30 dB, Low power mode		52.5		
	Ch-CH Noise Correlation Factor without Signal (1)	Summing of 8 channels		0		
	Ch-CH Noise Correlation Factor with Signal (1)	Full band (V_{CNTL} = 0, 0.8)		0.15, 0.17		
		1MHz band over carrier (V_{CNTL}= 0, 0.8)		0.18, 0.75		
	Signal to Noise Ratio (SNR)	V_{CNTL}= 0.6V(22 dB total channel gain)	68	70		dBFS
		V_{CNTL}= 0, LNA = 18dB, PGA = 24dB	59.3	63		
		V_{CNTL}= 0, LNA = 24dB, PGA = 24dB		58		
	Narrow Band SNR	SNR over 2 MHz band around carrier at V_{CNTL} = 0.6 V (22 dB total gain)	75	77		dBFS
	Input Common-mode Voltage	At INP and INM pins		2.4		V
	Input resistance			8		kΩ
		Preset active termination enabled		50,100,200,400		Ω
	Input capacitance			20		pF
	Input Control Voltage	V_{CNTLP} - V_{CNTLM}	0		1.5	V
	Common-mode voltage	V_{CNTLP} and V_{CNTLM}		0.75		V
	Gain Range			-40		dB
	Gain Slope	V_{CNTL}= 0.1 V to 1.1V		35		dB/V
	Input Resistance	Between V_{CNTLP} and V_{CNTLM}		200		KΩ
	Input Capacitance	Between V_{CNTLP} and V_{CNTLM}		1		pF
	TGC Response Time	V_{CNTL}= 0V to 1.5V step function		1.5		µs
	3rd order-Low-pass Filter			10, 15, 20, 30		MHz
	Settling time for change in LNA gain			14		µs
	Settling time for change in active termination setting			1		µs

(1) Noise correlation factor is defined as Nc/(Nu+Nc), where Nc is the correlated noise power in single channel; and Nu is the uncorrelated noise power in single channel. Its measurement follows the below equation, in which the SNR of single channel signal and the SNR of summed eight channel signal are measured.

$$\frac{N_C}{Nu + N_C} = \frac{10^{-\frac{8CH\_SNR}{10}}}{10^{-\frac{1CH\_SNR}{10}}} \times \frac{1}{56} - \frac{1}{7}$$

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14Bit, sample rate = 65MSPS, LPF Filter = 15 MHz, low noise mode, V_{OUT} = –1 dBFS, Single-ended V_{CNTL} mode, VCNTLM = GND, ADC configured in internal reference mode, internal 500 Ω CW feedback resistor, CMOS CW clocks, at ambient temperature T_A = 25°C, Digital demodulator is disabled unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
AC ACCURACY						
	LPF Bandwidth tolerance			±5%		
	CH-CH group delay variation	2 MHz to 15 MHz		2		ns
	CH-CH Phase variation	15 MHz signal		11		Degree
	Gain matching	0V < V_{CNTL}< 0.1V (Dev-to-Dev)		±0.5		dB
		0.1V < V_{CNTL}<1.1V(Dev-to-Dev), T_A = 25°C	–1	±0.5	+1	
		1.1V < V_{CNTL}<1.5 V (Dev-to-Dev)		±0.5		
		0.1V < V_{CNTL}<1.1 V (Dev-to-Dev), T_A = 0°C and 85°C	–1.1		1.1	
	Gain matching	Channel-to-Channel		±0.25		dB
	Output offset	V_{CNTL}= 0, PGA = 30dB, LNA = 24dB	–75		75	LSB
AC PERFORMANCE						
HD2	Second-Harmonic Distortion	F_{IN} = 2MHz; V_{OUT} = -1 dBFS		–60		dBc
		F_{IN} = 5 MHz; V_{OUT} = -1 dBFS		–60		
		F_{IN} = 5 MHz; V_{IN}= 500 mV_{PP}, V_{OUT} =–1dBFS, LNA = 18 dB, V_{CNTL}=0.88V		–55		
		F_{IN} = 5 MHz; V_{IN} = 250 mV_{PP}, V_{OUT} = –1 dBFS, LNA = 24 dB, V_{CNTL}= 0.88V		–55		
HD3	Third-Harmonic Distortion	F_{IN} = 2 MHz; V_{OUT} = –1dBFS		–55		dBc
		F_{IN} = 5 MHz; V_{OUT} = –1dBFS		–55		
		F_{IN} = 5 MHz; V_{IN} = 500mV_{PP}, V_{OUT} = –1 dBFS, LNA = 18 dB, V_{CNTL} = 0.88 V		–55		
		F_{IN} = 5 MHz; V_{IN} = 250 mV_{PP}, V_{OUT} = –1dBFS, LNA = 2 4dB, V_{CNTL}= 0.88 V		–55		
THD	Total Harmonic Distortion	F_{IN} = 2 MHz; V_{OUT} = –1 dBFS		–55		dBc
		F_{IN} = 5 MHz; V_{OUT} = – 1dBFS		–55		
IMD3	Intermodulation distortion	f1 = 5 MHz at –1 dBFS, f2 = 5.01 MHz at –27 dBFS		–60		dBc
XTALK	Cross-talk	F_{IN} = 5 MHz; V_{OUT}= –1 dBFS		–65		dB
	Phase Noise	kHz off 5 MHz (V_{CNTL}= 0 V)		–132		dBc/Hz
LNA						
	Input Referred Voltage Noise	Rs = 0 Ω, f = 2 MHz, Rin = High Z, Gain = 24, 18, 12 dB		0.63, 0.70, 0.9		nV/rtHz
	High-Pass Filter	-3 dB Cut-off Frequency		50, 100, 150, 200		KHz
	LNA linear output			4		Vpp
VCAT+ PGA						
	VCAT Input Noise	0 dB, -40 dB Attenuation		2, 10.5		nV/rtHz
	PGA Input Noise	24dB, 30dB		1.75		nV/rtHz
	-3dB HPF cut-off Frequency			80		KHz

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14Bit, sample rate = 65MSPS, LPF Filter = 15 MHz, low noise mode, V_{OUT} = –1 dBFS, Single-ended V_{CNTL} mode, VCNTLM = GND, ADC configured in internal reference mode, internal 500 Ω CW feedback resistor, CMOS CW clocks, at ambient temperature T_A = 25°C, Digital demodulator is disabled unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
CW DOPPLER						
en (RTI)	Input voltage noise (CW)	1 channel mixer, LNA = 24 dB, 500 Ω feedback resistor		0.8		nV/rtHz
		8 channel mixer, LNA = 24 dB, 62.5 Ω feedback resistor		0.33		
en (RTO)	Output voltage noise (CW)	1 channel mixer, LNA = 24 dB, 500 Ω feedback resistor		12		nV/rtHz
		8 channel mixer, LNA = 24 dB, 62. 5Ω feedback resistor		5		
en (RTI)	Input voltage noise (CW)	1 channel mixer, LNA = 18 dB, 500 Ω feedback resistor		1.1		nV/rtHz
		8 channel mixer, LNA = 18 dB, 62.5 Ω feedback resistor		0.5		
en (RTO)	Output voltage noise (CW)	1 channel mixer, LNA = 18 dB, 50 0Ω feedback resistor		8.1		nV/rtHz
		8 channel mixer, LNA = 18 dB, 62.5 Ω feedback resistor		4.0		
NF	Noise figure	Rs = 100 Ω,R_{IN} =High Z, F_{IN} = 2MHz (LNA, I/Q mixer and summing amplifier/filter)		1.8		dB
f_{CW}	CW Operation Range (2)	CW signal carrier frequency		8		MHz
	CW Clock frequency	1X CLK (16X mode)			8	MHz
		16X CLK(16X mode)			128	
		4X CLK(4X mode)		32		
	AC coupled LVDS clock amplitude	CLKM_16X-CLKP_16X; CLKM_1X-CLKP_1X		0.7		Vpp
	AC coupled LVPECL clock amplitude			1.6		
	CLK duty cycle	1X and 16X CLKs	35%		65%	
	Common-mode voltage	Internal provided		2.5		V
V_{CMOS}	CMOS Input clock amplitude		4		5	V
	CW Mixer conversion loss			4		dB
	CW Mixer phase noise	1 kHz off 2 MHz carrier		156		dBc/Hz
DR	Input dynamic range	F_{IN} = 2MHz, LNA = 24/18/12dB		160, 164, 165		dBFS/Hz
IMD3	Intermodulation distortion	f1 = 5.00 MHz, f2 = 5.01 MHz, both tones at -8.5 dBm amplitude, 8 channels summed up in-phase, CW feedback resistor = 87 Ω		–50		dBc
		f1 = 5 MHz, F2= 5.01 MHz, both tones at –8. 5dBm amplitude, Single channel case, CW feed back resistor = 500 Ω		–60		dBc
	I/Q Channel gain matching	16X mode		±0.04		dB
	I/Q Channel phase matching	16X mode		±0.1		Degree
	I/Q Channel gain matching	4X mode		±0.04		dB
	I/Q Channel phase matching	4X mode		±0.1		Degree
	Image rejection ratio	F_{IN} = 2.01 MHz, 300 mV input amplitude, CW clock frequency = 2.00 MHz		–50		dBc

(2) In the 16X operation mode, the CW operation range is limited to 8MHz due to the 16X CLK. The maximum clock frequency for the 16X CLK is 128MHz. In the 8X, 4X, and 1X modes, higher CW signal frequencies up to 15 MHz can be supported with small degradation in performance, see application information: CW clock selection

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14Bit, sample rate = 65MSPS, LPF Filter = 15 MHz, low noise mode, V_{OUT} = –1 dBFS, Single-ended V_{CNTL} mode, VCNTLM = GND, ADC configured in internal reference mode, internal 500 Ω CW feedback resistor, CMOS CW clocks, at ambient temperature T_A = 25°C, Digital demodulator is disabled unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
CW SUMMING AMPLIFIER						
V_{CMO}	Common-mode voltage	Summing amplifier inputs/outputs		1.5		V
	Summing amplifier output			4		Vpp
	Input referred voltage noise	100 Hz		2		nV/rtHz
		1 kHz		1.2		nV/rtHz
		2 KHz - 100 MHz		1		nV/rtHz
	Input referred current noise			2.5		pA/rtHz
	Unit gain bandwidth			200		MHz
	Max output current	Linear operation range		20		mApp
ADC SPECIFICATIONS						
	Sample rate		10		65	MSPS
SNR	Signal-to-noise ratio	Idle channel SNR of ADC 14b		77		dBFS
	Internal reference mode	REFP		1.5		V
		REFM		0.5		V
	External reference mode	VREF_IN Voltage		1.4		V
		VREF_IN Current		50		µA
	ADC input full-scale range			2		Vpp
	LVDS Rate	65MSPS at 14 bit		910		Mbps
POWER DISSIPATION						
	AVDD Voltage		3.15	3.3	3.6	V
	AVDD_ADC Voltage		1.7	1.8	1.9	V
	AVDD_5V Voltage		4.75	5	5.5	V
	DVDD Voltage		1.7	1.8	1.9	V
	Total power dissipation per channel	TGC low noise mode, 65 MSPS		158	190	mW/CH
		TGC low noise mode, 40 MSPS		145		
		TGC medium power mode, 40 MSPS		114		
		TGC low power mode, 40 MSPS		101.5		
	AVDD (3.3V) Current	TGC low noise mode, no signal		202	240	mA
		TGC medium power mode, no signal		126		
		TGC low power mode, no signal		99		
		CW-mode, no signal		147	170	
		TGC low noise mode, 500 mV_{PP} Input,1% duty cycle		210		
		TGC medium power mode, 500 mV_{PP} Input, 1% duty cycle		133		
		TGC low power, 50 0mV_{PP} Input, 1% duty cycle		105		
		CW-mode, 500 mV_{PP} Input		375		
	AVDD_5V Current	TGC mode no signal		25.5	35	mA
		CW Mode no signal, 16X clock = 32MHz		32		
		TGC mode, 50 0mVpp Input,1% duty cycle		26		
		CW-mode, 50 0mVpp Input		42.5		
	VCA Power dissipation	TGC low noise mode, no signal		99	121	mW/CH
		TGC medium power mode, no signal		68		
		TGC low power mode, no signal		55.5		
		TGC low noise mode, 500 mV_{PP} input,1% duty cycle		102.5		
		TGC medium power mode, 500 mV_{PP} Input, 1% duty cycle		71		
		TGC low power mode, 500 mVpp input,1% duty cycle		59.5		
	CW Power dissipation	No signal, ADC shutdown CW Mode no signal, 16X clock = 32 MHz		80		mW/CH
		500 mV_{PP} input, ADC shutdown , 16X clock = 32 MHz		173		
	AVDD_ADC(1.8V) Current	65MSPS		187	205	mA
	DVDD(1.8V) Current	65 MSPS		77	110	mA

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1 µF at INP and bypassed to ground with 15 nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14Bit, sample rate = 65MSPS, LPF Filter = 15 MHz, low noise mode, V_{OUT} = –1 dBFS, Single-ended V_{CNTL} mode, VCNTLM = GND, ADC configured in internal reference mode, internal 500 Ω CW feedback resistor, CMOS CW clocks, at ambient temperature T_A = 25°C, Digital demodulator is disabled unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
ADC Power dissipation/CH	65 MSPS		59	69	mW/CH
	50 MSPS		51		
	40 MSPS		46		
	20 MSPS		35		
Power dissipation in power down mode	PDN_VCA = High, PDN_ADC =High		25		mW/CH
	Complete power-down PDN_Global = High		0.6		
Power-down response time	Time taken to enter power down		1		µs
Power-up response time	VCA power down		2 µs+1% of PDN time		µs
	ADC power down		1		
	Complete power down		2.5		ms
Power supply modulation ratio, AVDD and AVDD_5V	F_{IN} = 5 MHz, at 50 mV_{PP} noise at 1 KHz on supply(3)		–65		dBc
	F_{IN} = 5 MHz, at 50mVpp noise at 50 KHz on supply(3)		–65		
Power supply rejection ratio	f = 10 kHz,V_{CNTL} = 0 V (high gain), AVDD		–40		dBc
	f = 10 kHz,V_{CNTL} = 0 V (high gain), AVDD_5 V		–55		dBc
	f = 1 0kHz,V_{CNTL} = 1 V (low gain), AVDD		–50		dBc

(3) PSMR specification is with respect to carrier signal amplitude.

DIGITAL DEMODULATOR ELECTRICAL CHARACTERISTICS

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8V, DVDD_LDO = 1.4V (internal generated), 14Bit/65MSPS, 4X decimation factor, at ambient temperature T_A = +25C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Addtional Power Consumption on DVDD (1.8V)	65MSPS, 4X decimation factor		90		mW/CH
	Additonal Power Consumption on DVDD (1.8V)	40MSPS, 4X decimation factor		61		mW/CH
	Addtional Power Consumption on DVDD (1.8V)	65MSPS, 32X decimation factor, half LVDS pairs are powered down		77		mW/CH
	Additonal Power Consumption on DVDD (1.8V)	40MSPS, 32X decimation factor, half LVDS pairs are powered down		55		mW/CH
V_{IH}	Logic high input voltage, TX_SYNC pin	Support 1.8-V and 3.3-V CMOS logic	1.3		3.3	V
V_{IL}	Logic low input voltage, TX_SYNC pin	Support 1.8-V and 3.3-V CMOS logic	0		0.3	V
I_{IH}	Logic high input current, TX_SYNC pin	V_{HIGH} = 1.8-V		11		µA
I_{IL}	Logic low input current, TX_SYNC pin	V_{LOW} = 0-V		<0.1		µA

DIGITAL CHARACTERISTICS

Typical values are at +25°C, AVDD = 3.3V, AVDD_5 = 5V and AVDD_ADC = 1.8V, DVDD = 1.8V unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = 0°C to T_{MAX} = +85°C,.

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS (1)
DIGITAL INPUTS/OUTPUTS						
V_{IH}	Logic high input voltage		2		3.3	V
V_{IL}	Logic low input voltage		0		0.3	V
	Logic high input current			200		µA
	Logic low input current			200		µA
	Input capacitance			5		pF
V_{OH}	Logic high output voltage	SDOUT pin		DVDD		V
V_{OL}	Logic low output voltage	SDOUT pin		0		V
LVDS OUTPUTS						
	Output differential voltage	with 100 ohms external differential termination		400		mV
	Output offset voltage	Common-mode voltage		1100		mV
	FCLKP and FCLKM	1X clock rate	10		65	MHz
	DCLKP and DCLKM	7X clock rate	70		455	MHz
		6X clock rate	60		390	MHz
t_{su}	Data setup time (2)			350		ps
t_h	Data hold time (2)			350		ps
ADC INPUT CLOCK						
	CLOCK frequency		10		65	MSPS
	Clock duty cycle		45%	50%	55%	
	Clock input amplitude, differential(V_{CLKP_ADC}–V_{CLKM_ADC})	Sine-wave, ac-coupled	0.5			Vpp
		LVPECL, ac-coupled		1.6		Vpp
		LVDS, ac-coupled		0.7		Vpp
	Common-mode voltage	biased internally		1		V
	Clock input amplitude V_{CLKP_ADC} (single-ended)	CMOS CLOCK		1.8		Vpp

(1) The DC specifications refer to the condition where the LVDS outputs are not switching, but are permanently at a valid logic level 0 or 1 with 100Ω external termination.
(2) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margins

TYPICAL CHARACTERISTICS

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1 µF caps at INP and 15 nF caps at INM, No active termination, V_{CNTL} = 0 V, F_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14Bit, sample rate = 65 MSPS, LPF Filter = 15 MHz, low noise mode, Single-ended V_{CNTL} mode, V_{CNTLM} = GND, ADC is configured in internal reference mode, V_{OUT} = -1 dBFS, 500 Ω CW feedback resistor, CMOS 16X clock, digital demodulator is disabled, at ambient temperature TA = +25°C, unless otherwise noted.

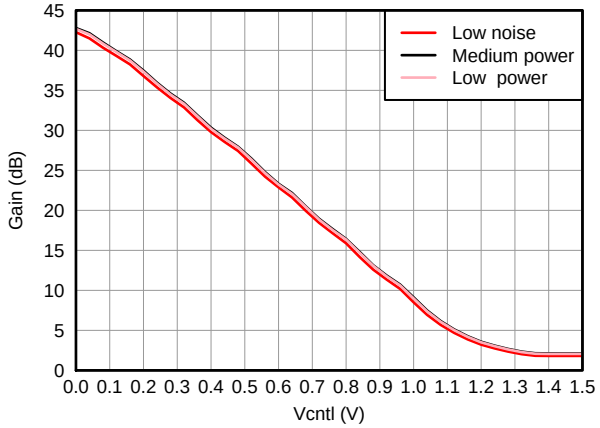


Figure 3. Gain vs V_{CNTL}, LNA = 18 dB and PGA = 24 dB

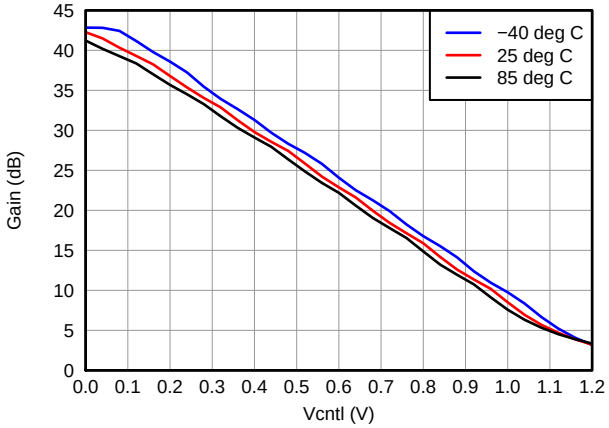


Figure 4. Gain Variation vs Temperature, LNA = 18 dB and PGA = 24 dB

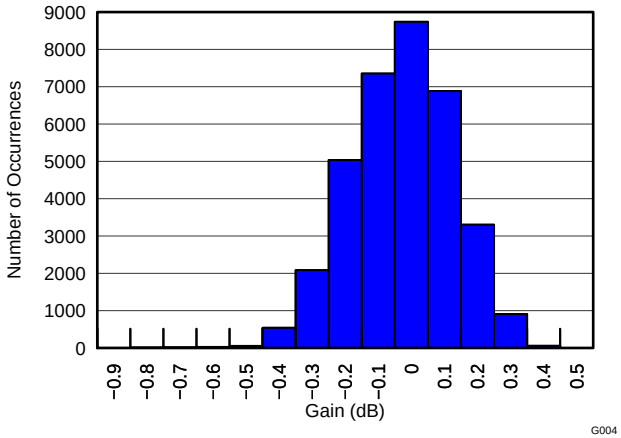


Figure 5. Gain Matching Histogram, V_{CNTL} = 0.3 V (34951 Channels)

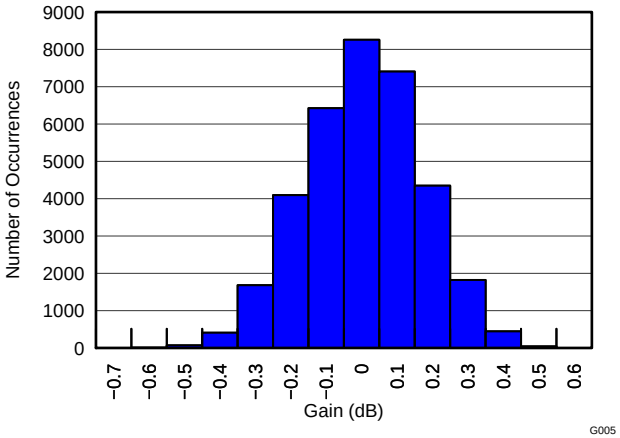


Figure 6. Gain Matching Histogram, V_{CNTL} = 0.6 V (34951 Channels)

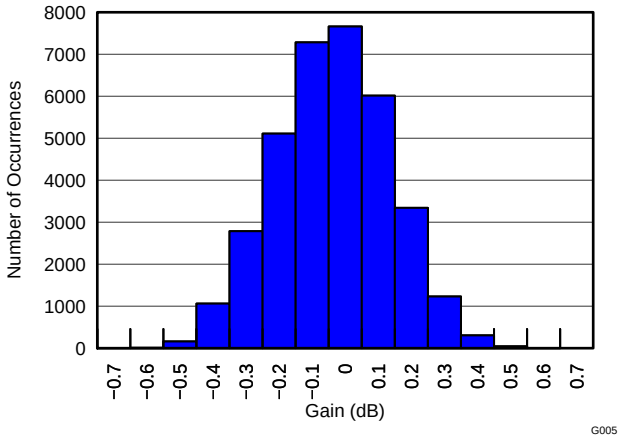


Figure 7. Gain Matching Histogram, V_{CNTL} = 0.9 V (34951 Channels)

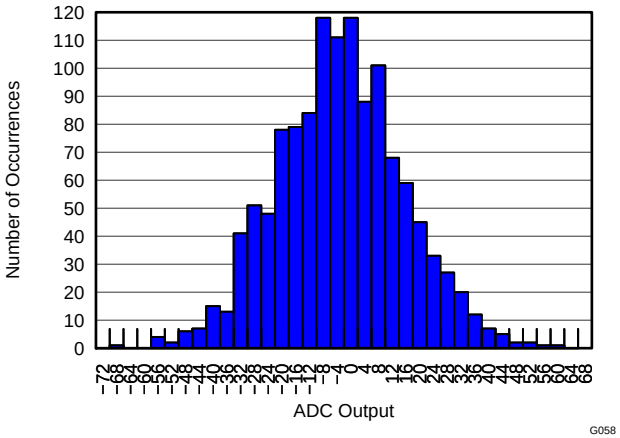


Figure 8. Output Offset Histogram, V_{CNTL} = 0 V (1247 Channels)

TYPICAL CHARACTERISTICS (continued)

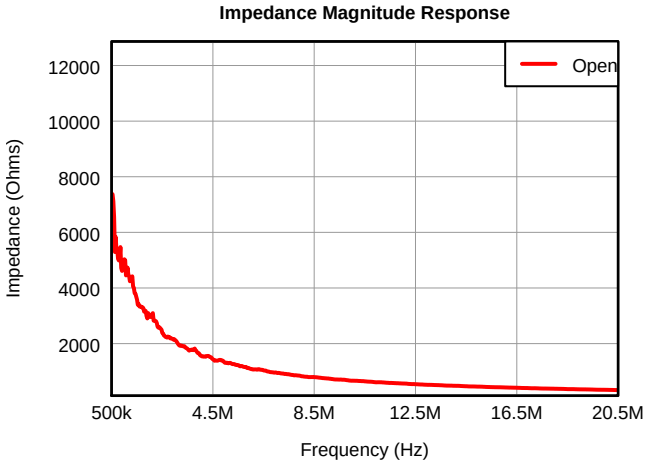


Figure 9. Input Impedance without Active Termination (Magnitude)

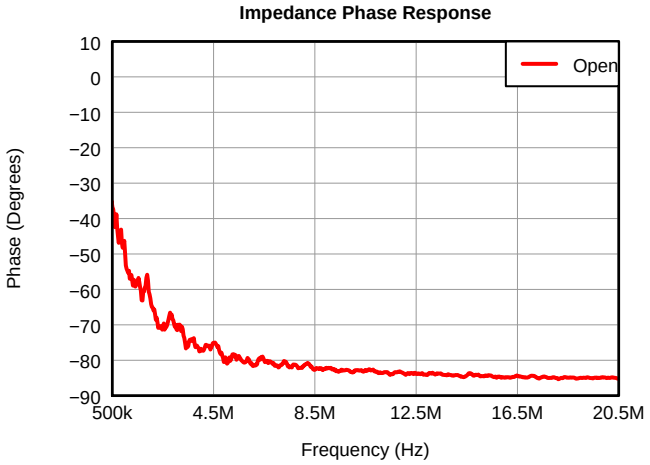


Figure 10. Input Impedance without Active Termination (Phase)

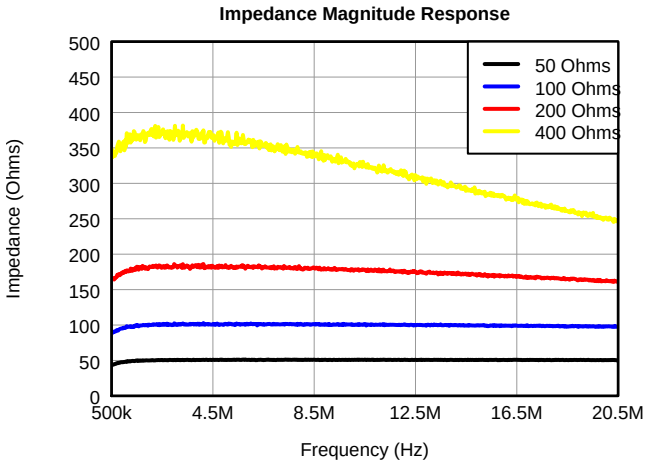


Figure 11. Input Impedance with Active Termination (Magnitude)

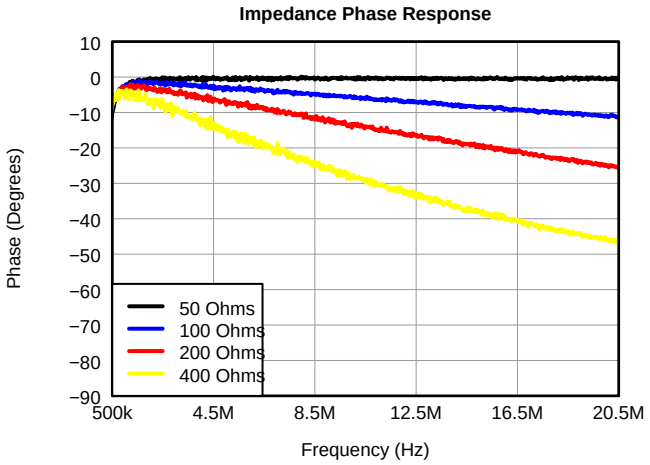


Figure 12. Input Impedance with Active Termination (Phase)

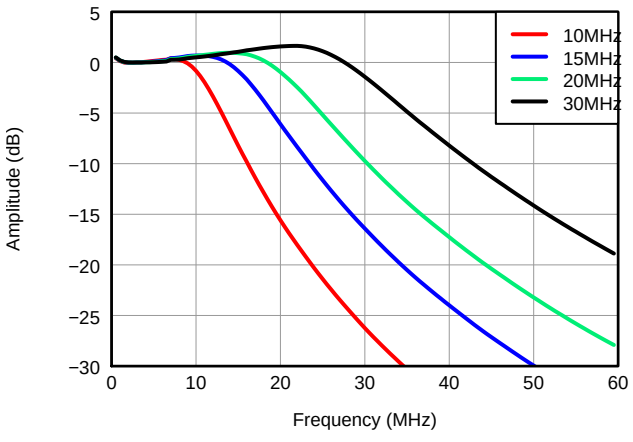


Figure 13. Low-Pass Filter Response

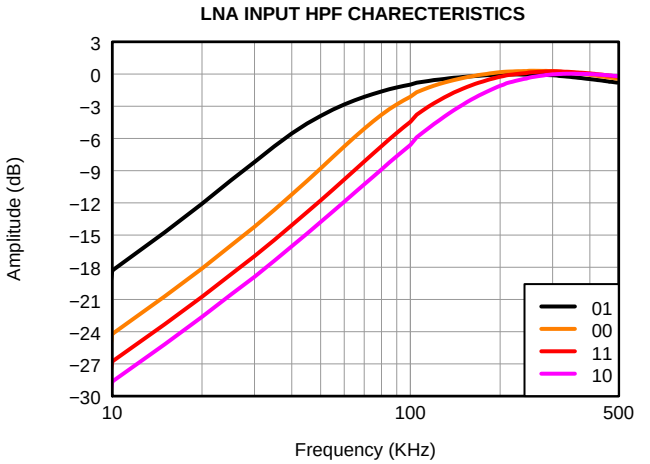


Figure 14. LNA High-Pass Filter Response vs. Reg59[3:2]

TYPICAL CHARACTERISTICS (continued)

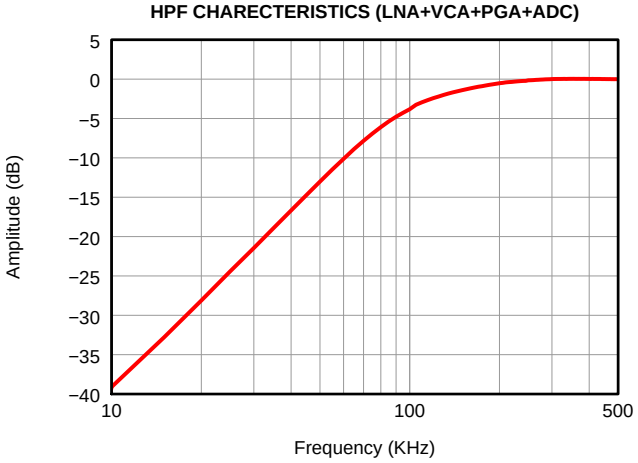


Figure 15. Full Channel High-Pass Filter Response at Default Register Setting

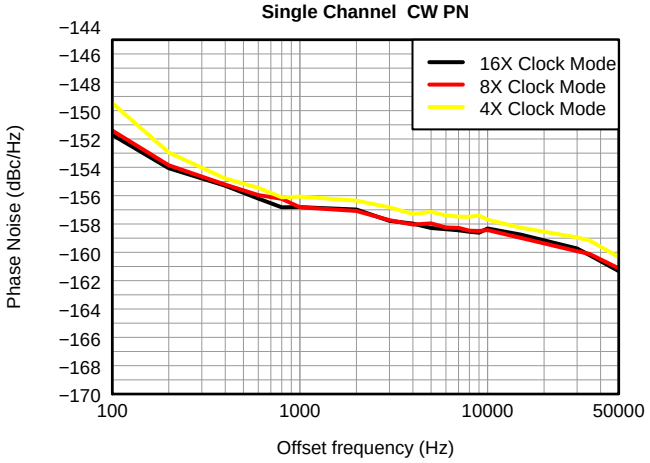


Figure 16. CW Phase Noise, F_{IN} = 2 MHz

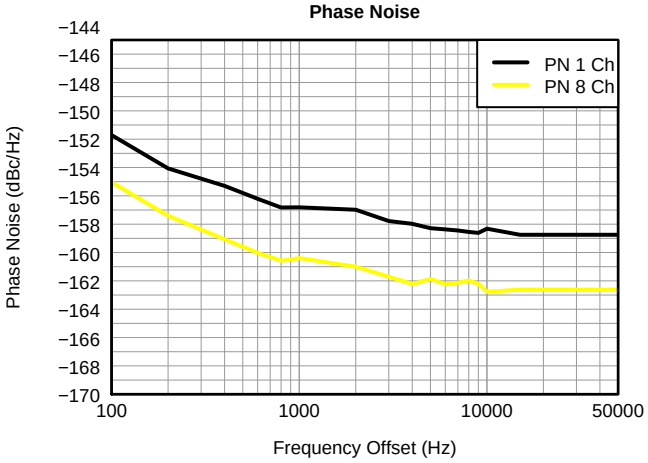


Figure 17. CW Phase Noise, F_{IN} = 2 MHz, 1 Channel vs 8 Channel

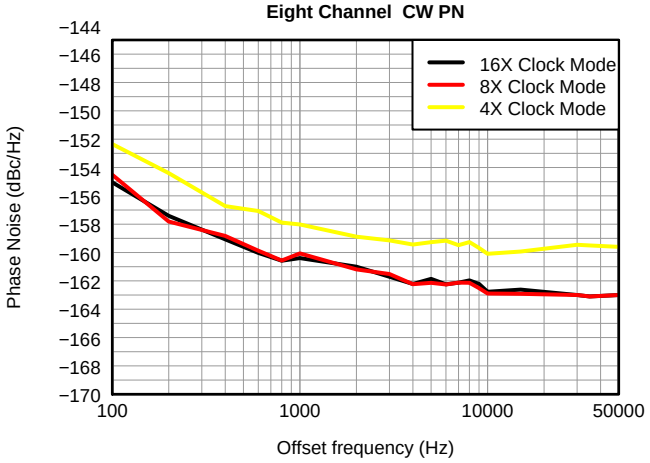


Figure 18. CW Phase Noise vs Clock Modes, F_{IN}= 2 MHz

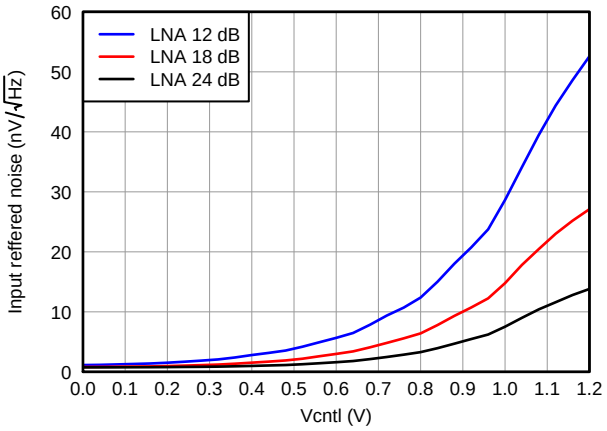


Figure 19. IRN, PGA = 24 dB and Low Noise Mode

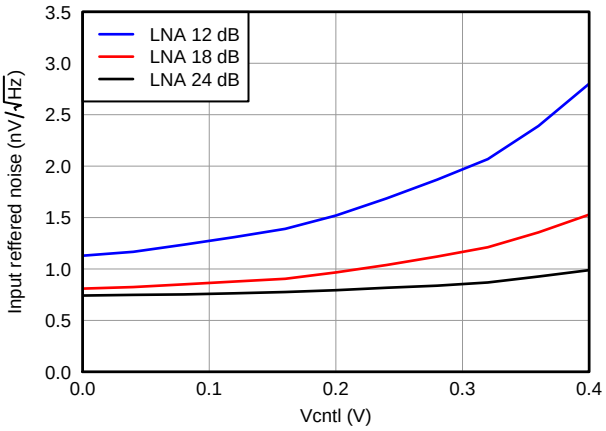


Figure 20. IRN, PGA = 24 dB and Low Noise Mode

TYPICAL CHARACTERISTICS (continued)

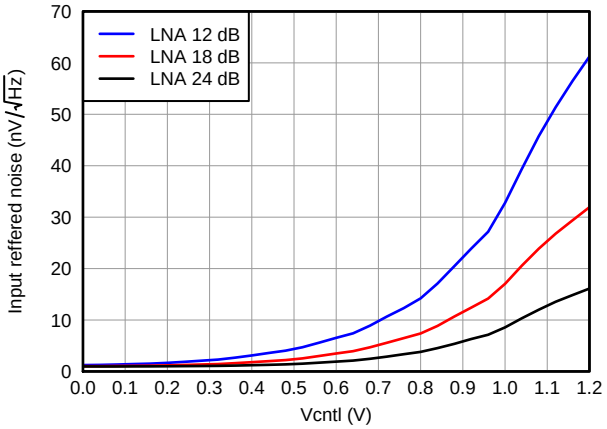


Figure 21. IRN, PGA = 24 dB and Medium Power Mode

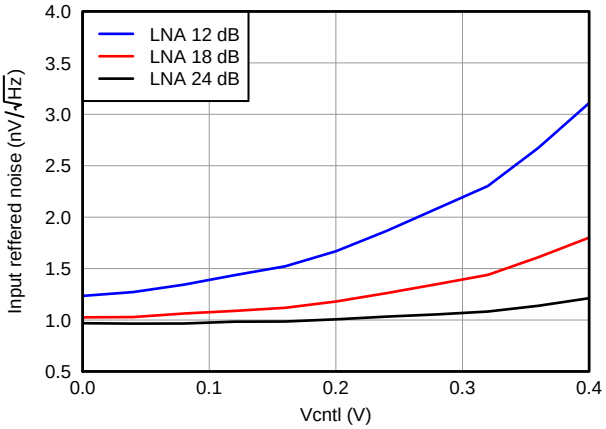


Figure 22. IRN, PGA = 24 dB and Medium Power Mode

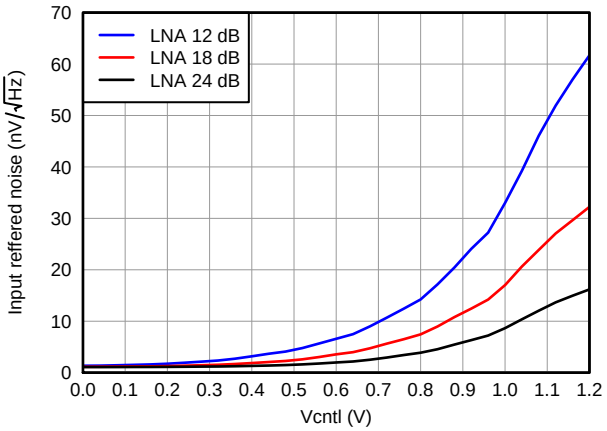


Figure 23. IRN, PGA = 24 dB and Low Power Mode

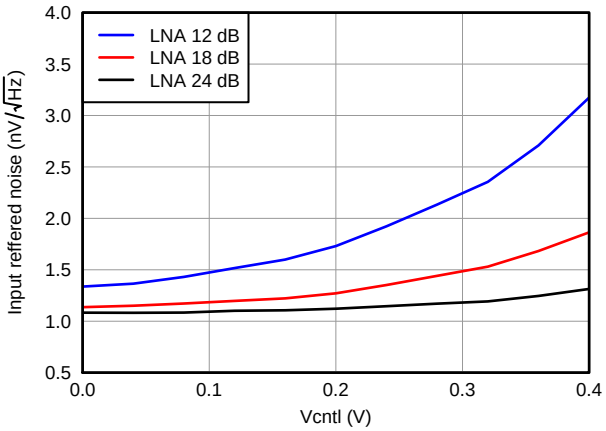


Figure 24. IRN, PGA = 24 dB and Low Power Mode

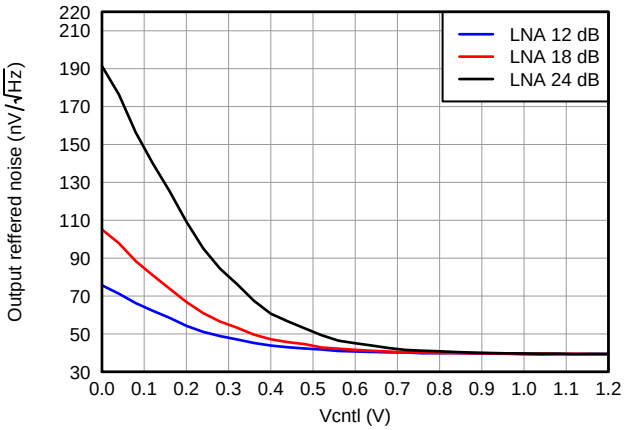


Figure 25. ORN, PGA = 24 dB and Low Noise Mode

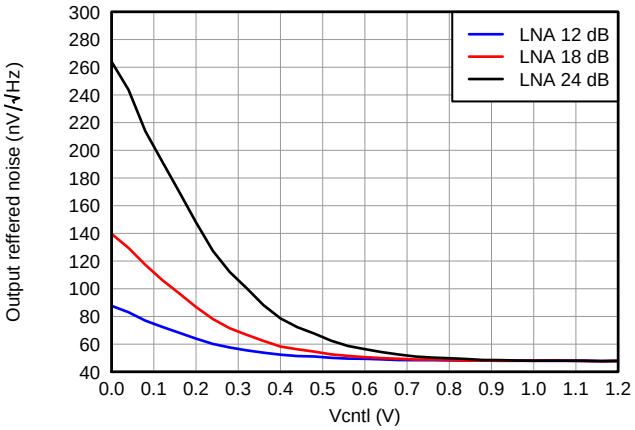


Figure 26. ORN, PGA = 24 dB and Medium Power Mode

TYPICAL CHARACTERISTICS (continued)

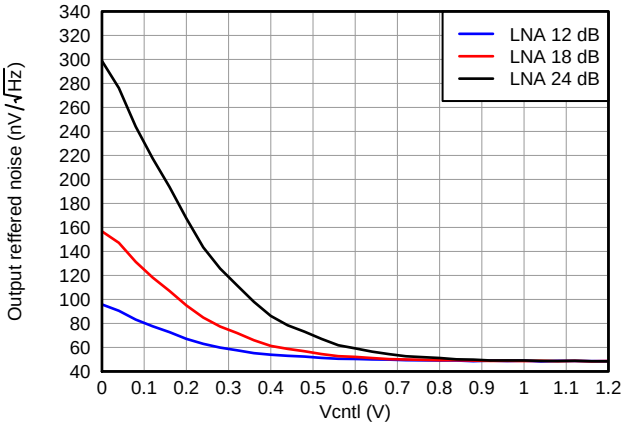


Figure 27. ORN, PGA = 24 dB and Low Power Mode

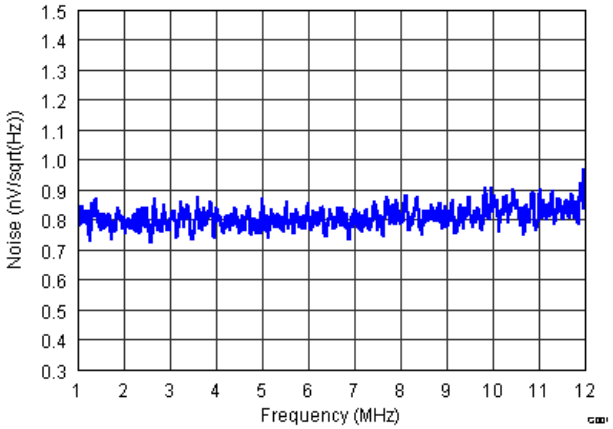


Figure 28. IRN, PGA = 24 dB and Low Noise Mode

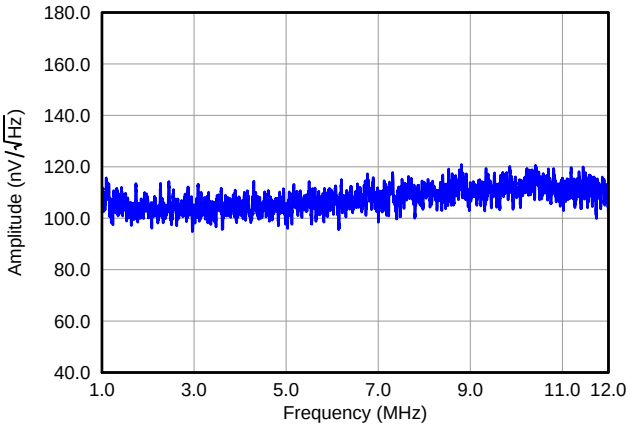


Figure 29. ORN, PGA = 24 dB and Low Noise Mode

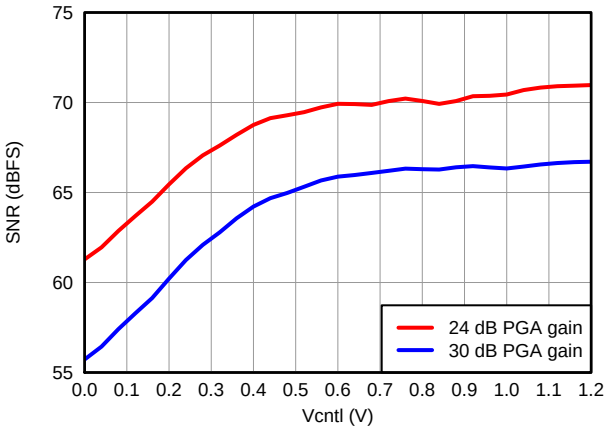


Figure 30. SNR, LNA = 18 dB and Low Noise Mode

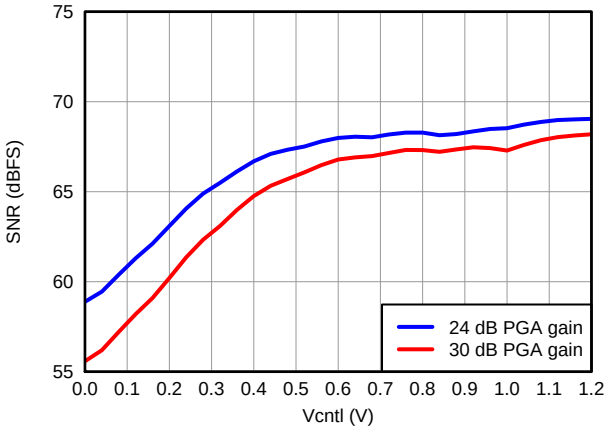


Figure 31. SNR, LNA = 18 dB and Low Power Mode

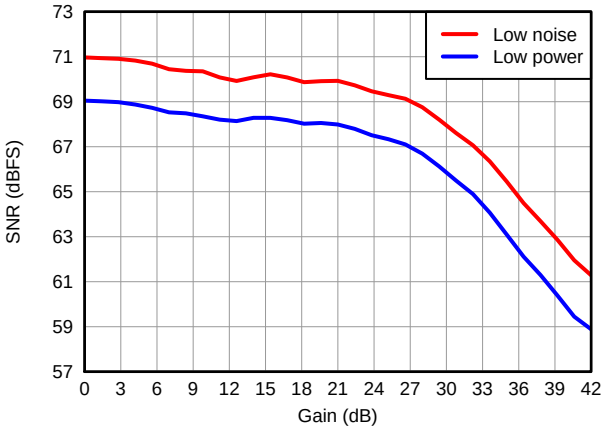


Figure 32. SNR vs. Different Power Modes

TYPICAL CHARACTERISTICS (continued)

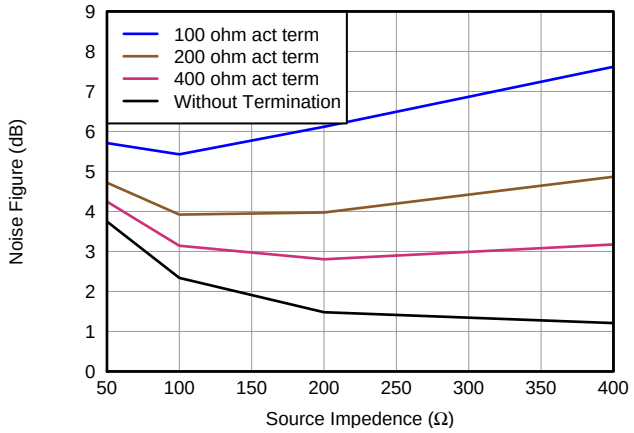


Figure 33. Noise Figure, LNA = 12 dB and Low Noise Mode

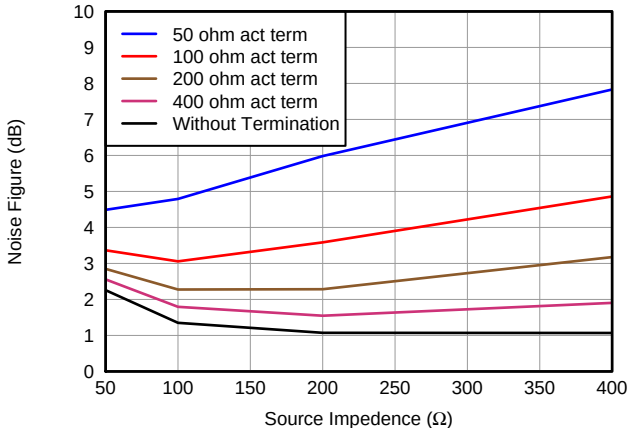


Figure 34. Noise Figure, LNA = 18 dB and Low Noise Mode

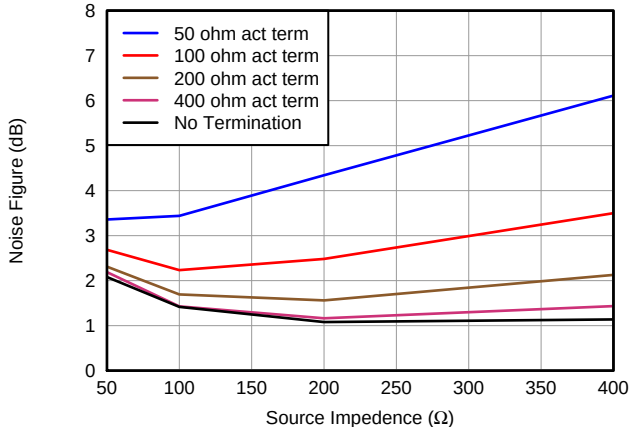


Figure 35. Noise Figure, LNA = 24 dB and Low Noise Mode

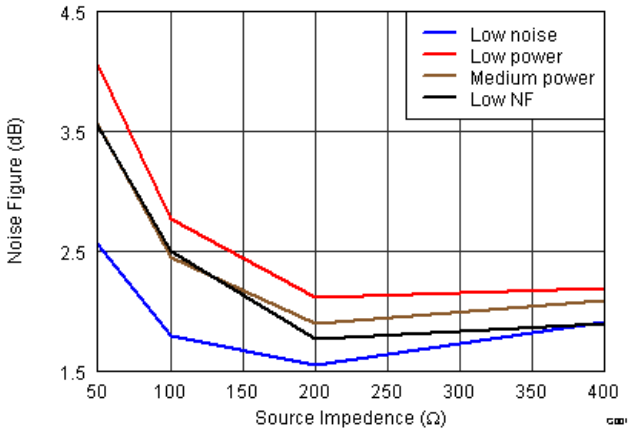


Figure 36. Noise Figure vs Power Modes with 400 Ω Termination

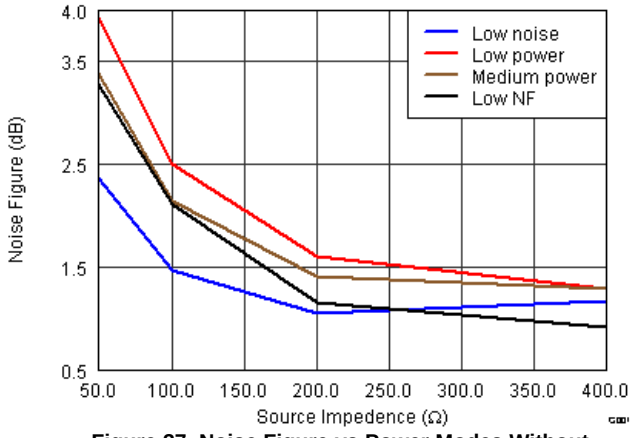


Figure 37. Noise Figure vs Power Modes Without Termination

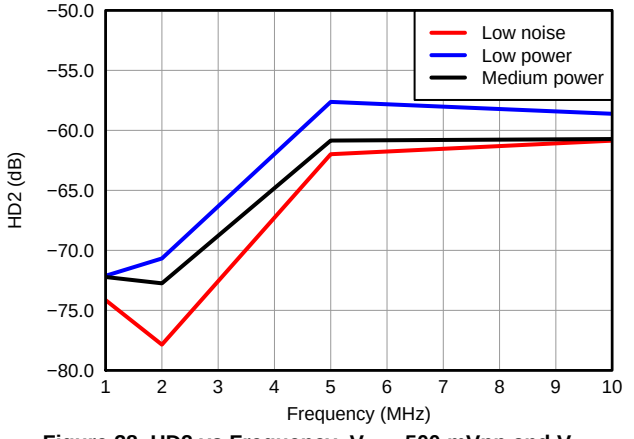


Figure 38. HD2 vs Frequency, V_{IN} = 500 mVpp and V_{OUT} = -1 dBFS

TYPICAL CHARACTERISTICS (continued)

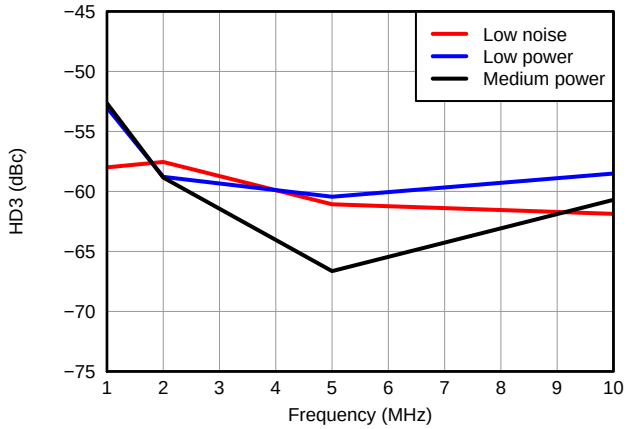


Figure 39. HD3 vs Frequency, V_{IN} = 500 mVpp and V_{OUT} = -1 dBFS

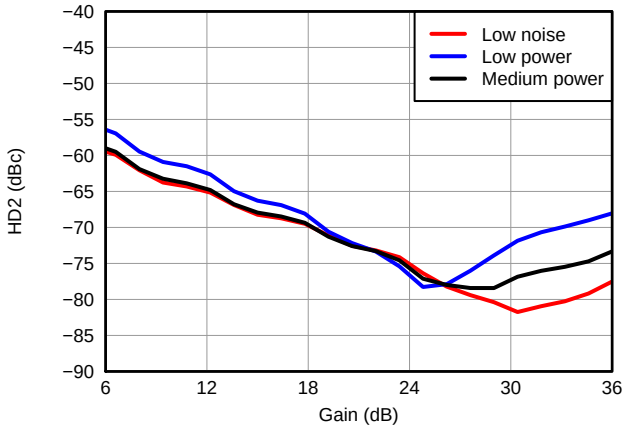


Figure 40. HD2 vs Gain, LNA = 12 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

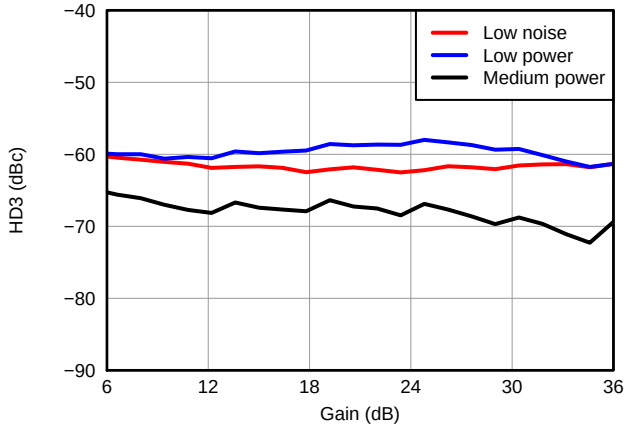


Figure 41. HD3 vs Gain, LNA = 12 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

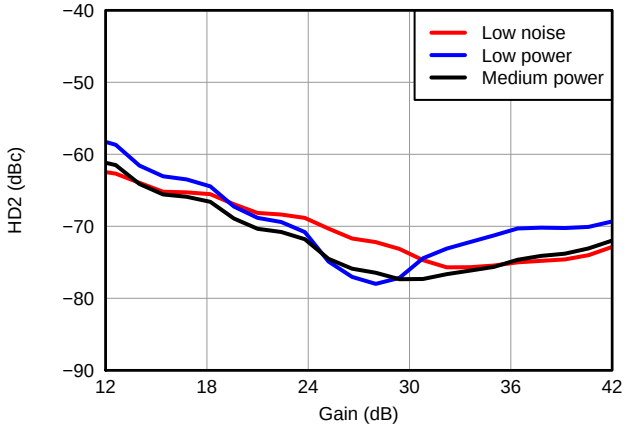


Figure 42. HD2 vs Gain, LNA = 18 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

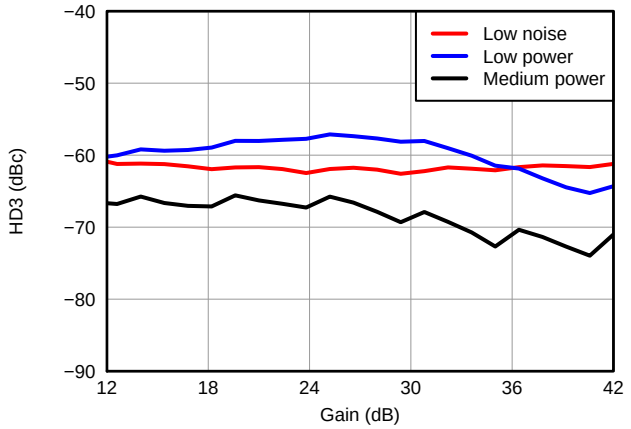


Figure 43. HD3 vs Gain, LNA = 18 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

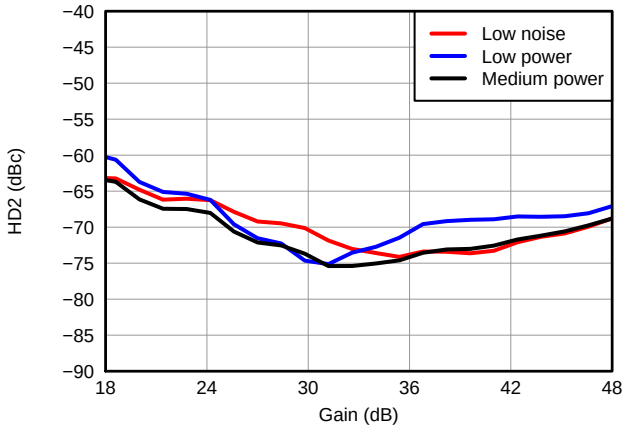


Figure 44. HD2 vs Gain, LNA = 24 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

TYPICAL CHARACTERISTICS (continued)

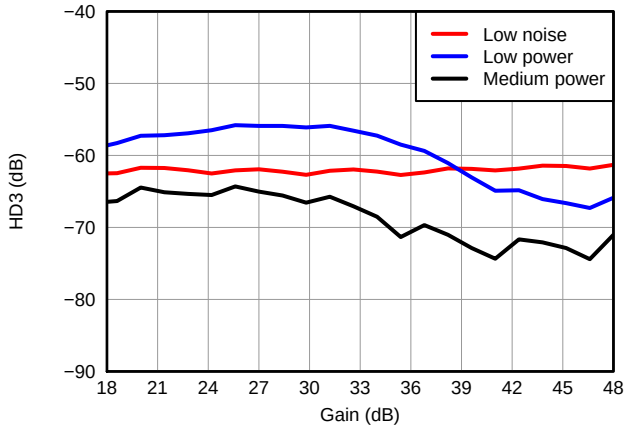


Figure 45. HD3 vs Gain, LNA = 24 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

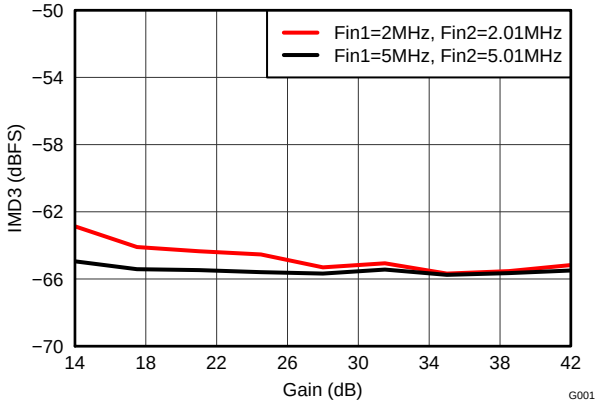


Figure 46. IMD3, Fout1 = -7 dBFS and Fout2 = -21 dBFS

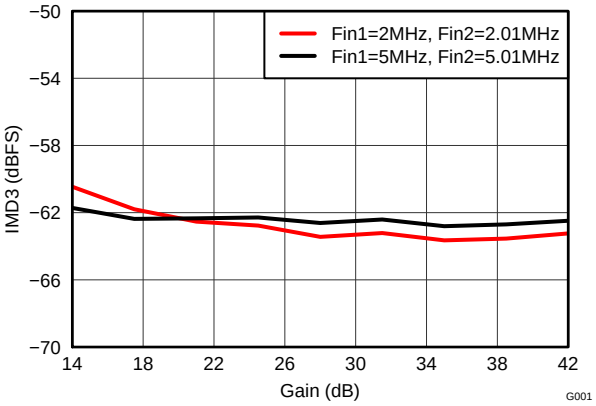


Figure 47. IMD3, Fout1 = -7 dBFS and Fout2 = -7 dBFS

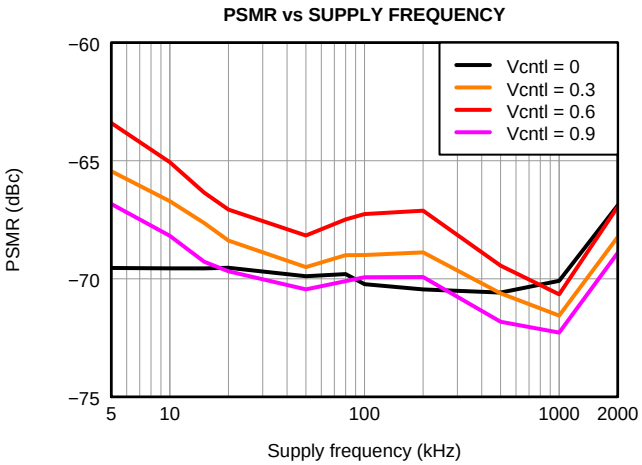


Figure 48. AVDD Power Supply Modulation Ratio, 100 mVpp Supply Noise with Different Frequencies

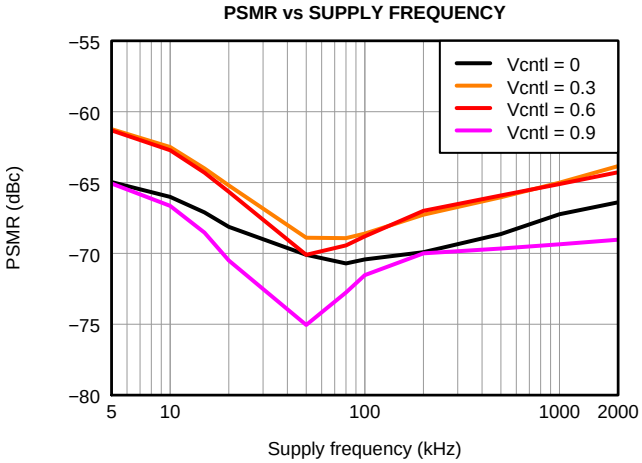


Figure 49. AVDD_5V Power Supply Modulation Ratio, 100 mVpp Supply Noise with Different Frequencies

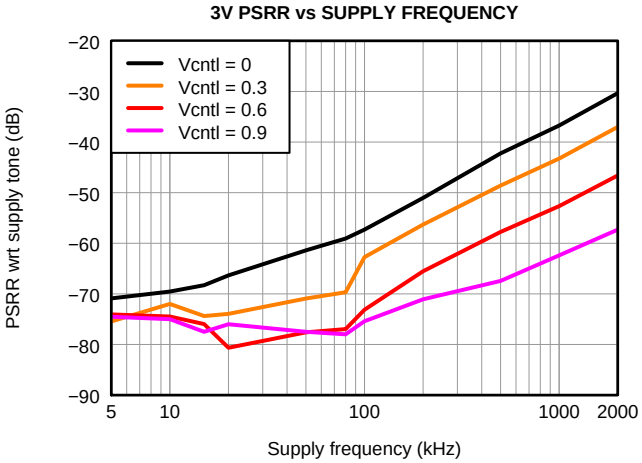


Figure 50. AVDD Power Supply Rejection Ratio, 100 mVpp Supply Noise with Different Frequencies

TYPICAL CHARACTERISTICS (continued)

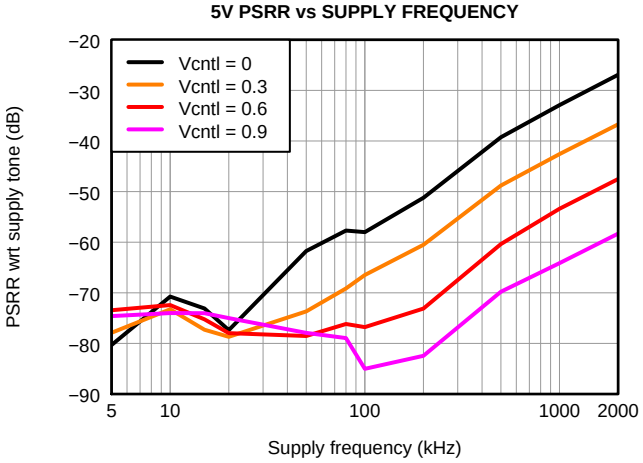


Figure 51. AVDD_5V Power Supply Rejection Ratio, 100 mVpp Supply Noise with Different Frequencies

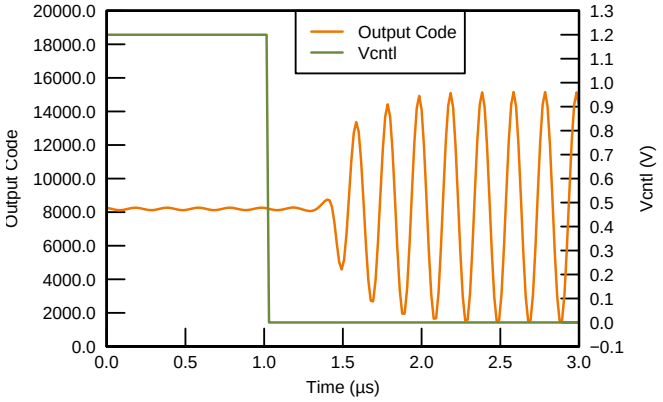


Figure 52. V_{CNTL} Response Time, LNA = 18 dB and PGA = 24 dB

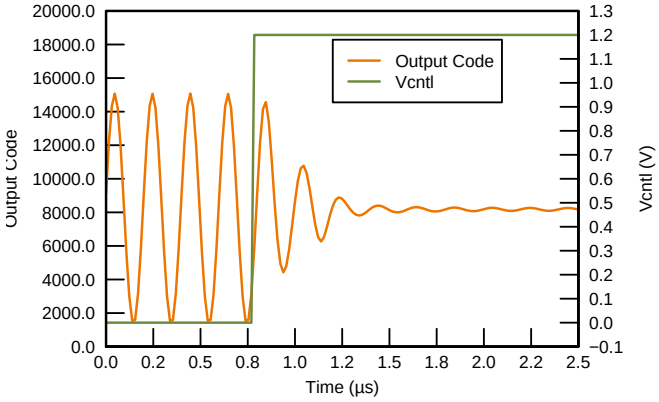


Figure 53. V_{CNTL} Response Time, LNA = 18 dB and PGA = 24 dB

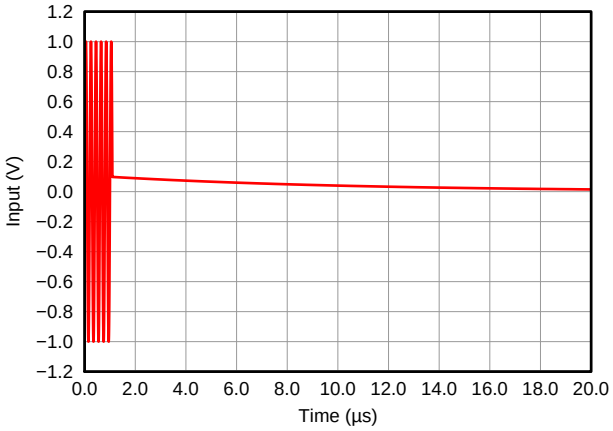


Figure 54. Pulse Inversion Asymmetrical Positive Input

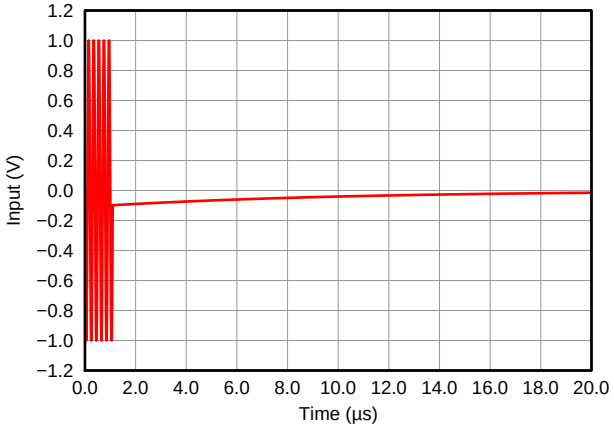


Figure 55. Pulse Inversion Asymmetrical Negative Input

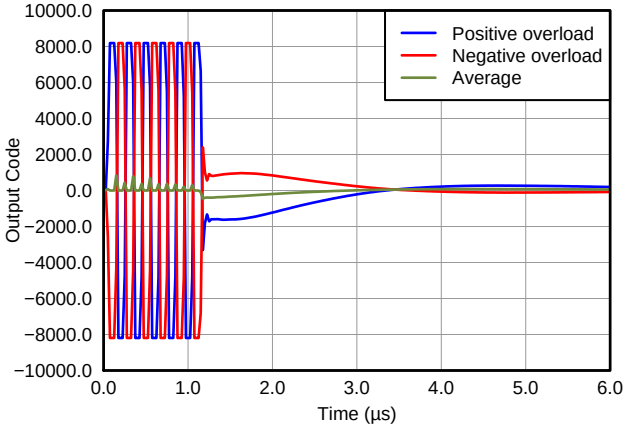


Figure 56. Pulse Inversion, V_{IN} = 2 Vpp, PRF = 1 KHz, Gain = 21 dB

TYPICAL CHARACTERISTICS (continued)

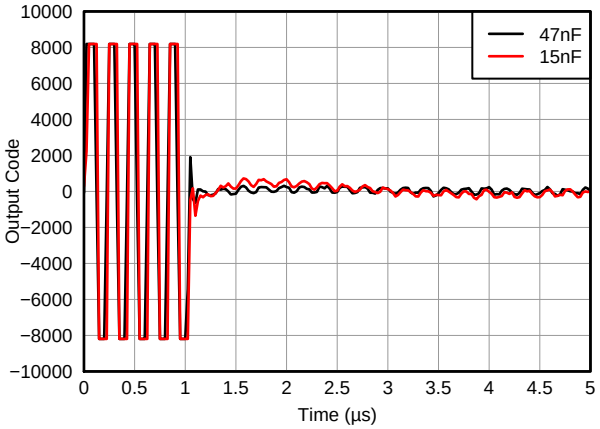


Figure 57. Overload Recovery Response vs INM capacitor, V_{IN} = 50 mVpp/100 µVpp, Max Gain

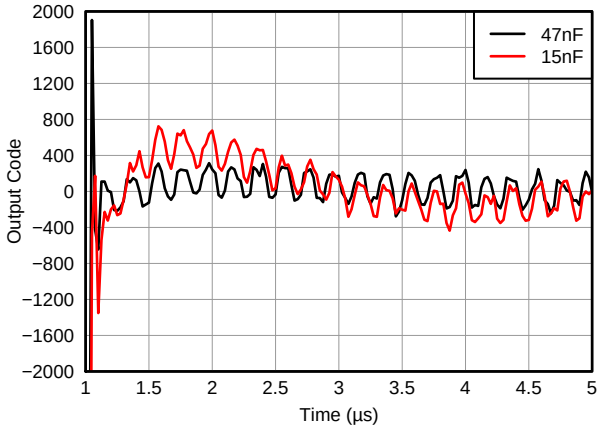


Figure 58. Overload Recovery Response vs INM Capacitor (Zoomed), V_{IN} = 50 mVpp/100 µVpp, Max Gain

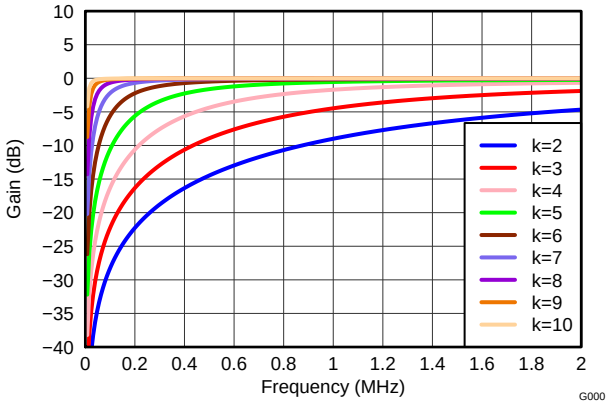


Figure 59. Digital High-Pass Filter Response

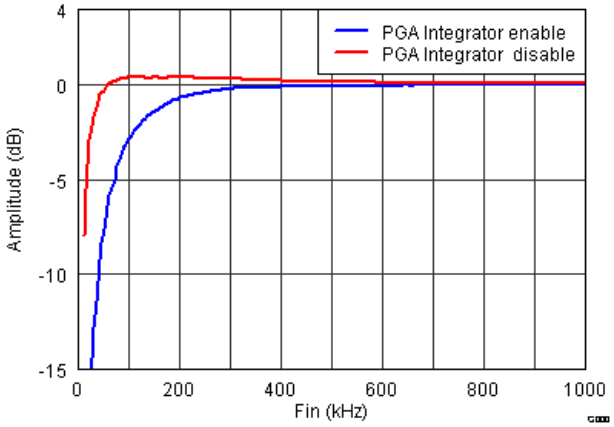


Figure 60. Signal Chain Low Frequency Response with INM Capacitor = 1 µF

TIMING CHARACTERISTICS(1)

Typical values are at 25°C, AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, Differential clock, C_{LOAD} = 5 pF, R_{LOAD} = 100Ω, 14Bit, sample rate = 65MSPS, digital demodulator is disabled, unless otherwise noted. Minimum and maximum values are across the full temperature range T_{MIN} = 0°C to T_{MAX} = 85°C with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ta	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs	0.7	3		ns
	Aperture delay matching	Across channels within the same device		±150		ps
t_j	Aperture jitter			450		Fs rms
	ADC latency	Default, after reset, or / 0 x 2 [12] = 1, LOW_LATENCY = 1		11/8		Input clock cycles
t_{delay}	Data and frame clock delay	Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus 3/7 of the input clock period (T).	3	5.4	7	ns
Δt_{delay}	Delay variation	At fixed supply and 20°C T difference. Device to device	–1		1	ns
t_{RISE}	Data rise time Data fall time	Rise time measured from –100 mV to 100 mV Fall time measured from 100 mV to –100 mV 10 MHz < f_{CLKIN} < 65 MHz		0.14		ns
t_{FALL}				0.15		
$t_{FCLKRISE}$	Frame clock rise time Frame clock fall time	Rise time measured from –100 mV to 100 mV Fall time measured from 10 0mV to –100 mV 10 MHz < f_{CLKIN} < 6 5 MHz		0.14		ns
$t_{FCLKFALL}$				0.15		
	Frame clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge	48%	50%	52%	
$t_{DCLKRISE}$	Bit clock rise time Bit clock fall time	Rise time measured from –100 mV to 100 mV Fall time measured from 100 mV to –10 0mV 10 MHz < f_{CLKIN} < 65 MHz		0.13		ns
$t_{DCLKFALL}$				0.12		
	Bit clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge 10 MHz < f_{CLKIN} < 65 MHz	46%		54%	

(1) Timing parameters are ensured by design and characterization; not production tested.

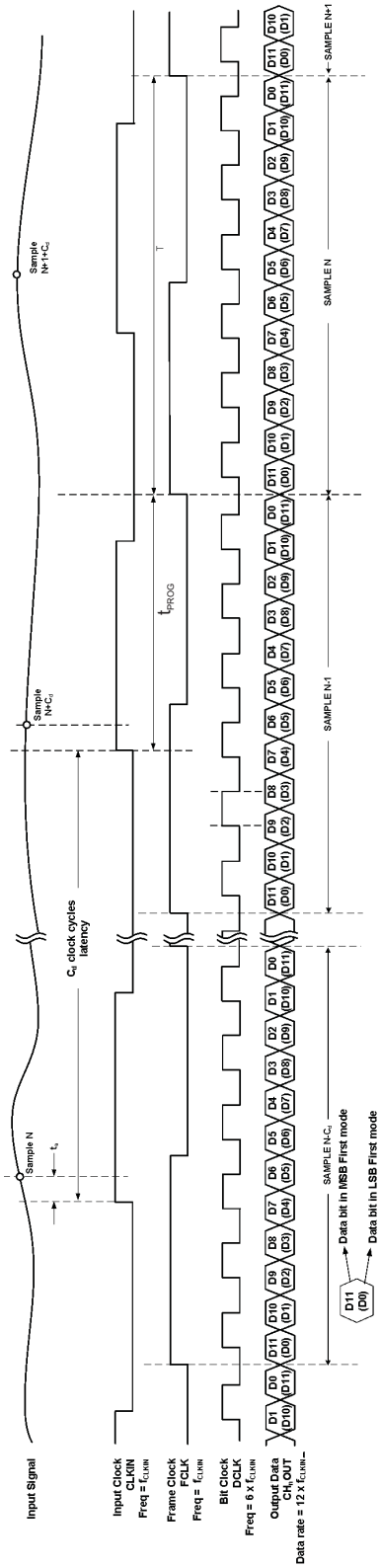
OUTPUT INTERFACE TIMING (14-bit)(1)(2)(3)

f_{CLKIN}, Input Clock Frequency	Setup Time (t_{su}), ns (for output data and frame clock)			Hold Time (t_h), ns (for output data and frame clock)			t_{PROG} = (3/7)x T + t_{delay}, ns		
	Data Valid to Input Clock Zero-Crossing			Input Clock Zero-Crossing to Data Invalid			Input Clock Zero-Cross (rising edge) to Frame Clock Zero-Cross (rising edge)		
MHz	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65	0.24	0.37		0.24	0.38		11	12	12.5
50	0.41	0.54		0.46	0.57		13	13.9	14.4
40	0.55	0.70		0.61	0.73		15	16	16.7
30	0.87	1.10		0.94	1.1		18.5	19.5	20.1
20	1.30	1.56		1.46	1.6		25.7	26.7	27.3

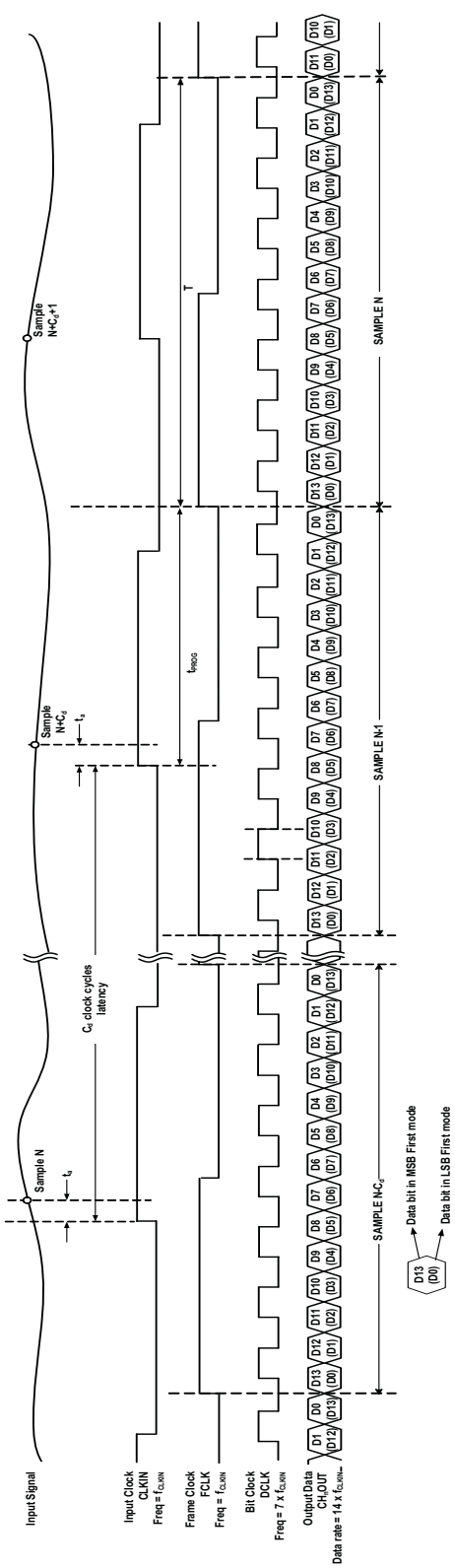
(1) FCLK timing is the same as for the output data lines. It has the same relation to DCLK as the data pins. Setup and hold are the same for the data and the frame clock.
(2) Data valid is logic HIGH = +100 mV and logic LOW = -100 mV
(3) Timing parameters are ensured by design and characterization; not production tested.

NOTE

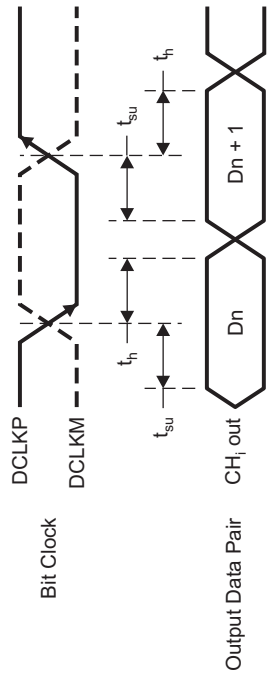
The above timing data can be applied to 12-bit or 16-bit LVDS rates as well. For example, the maximum LVDS output rate at 65MHz and 14-bit is equal to 910 MSPS, which is approximately equivalent to the rate at 56 MHz and 16-bit.



12-Bit 6x serialization mode



14-Bit 7x serialization mode



LVDS Setup and Hold Timing

Figure 61. LVDS Timing Diagrams

LVDS Output Interface Description

AFE5809 has LVDS output interface which supports multiple output formats. The ADC resolutions can be configured as 12bit or 14bit as shown in the LVDS timing diagrams Figure 61. The ADCs in the AFE5809 are running at 14bit; 2 LSBs are removed when 12-bit output is selected; and two 0s are added at LSBs when 16-bit output is selected. Appropriate ADC resolutions can be selected for optimizing system performance-cost effectiveness. When the devices run at 16bit mode, higher end FPGAs are required to process higher rate of LVDS data. Corresponding register settings are listed in Table 1.

Table 1. Corresponding Register Settings

LVDS Rate	12 bit (6X DCLK)	14 bit (7X DCLK)	16 bit (8X DCLK)
Reg 3 [14:13]	11	00	01
Reg 4 [2:0]	010	000	000
Description	2 LSBs removed	N/A	2 0s added at LSBs

Serial Peripheral Interface (SPI) Operation

Serial Register Write Description

Programming of different modes can be done through the serial interface formed by pins SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and RESET. All these pins have a pull-down resistor to GND of 20kΩ . Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every rising edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiple of 24-bit words within a single active SEN pulse (there is an internal counter that counts groups of 24 clocks after the falling edge of SEN). The interface can work with the SCLK frequency from 20 MHz down to low speeds (few Hertz) and even with non-50% duty cycle SCLK. The data is divided into two main portions: a register address (8 bits) and the data itself (16 bits), to load on the addressed register. When writing to a register with unused bits, these should be set to 0. Figure 62 illustrates this process.

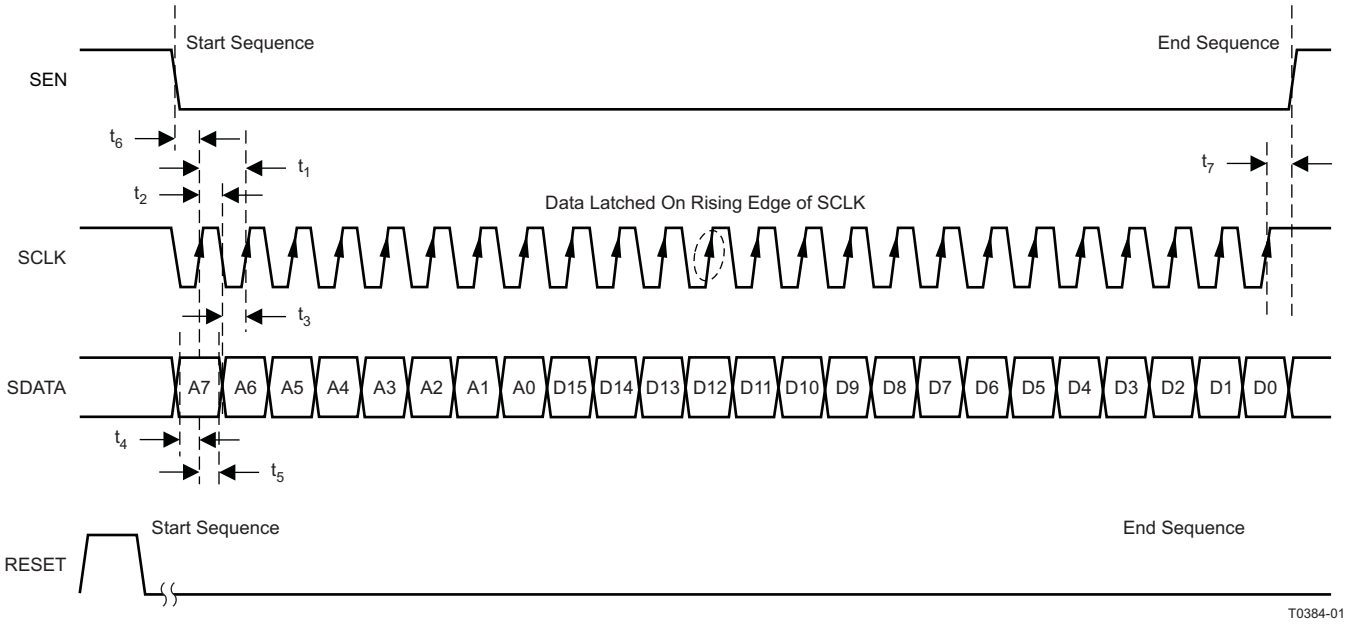


Figure 62. SPI Timing

SPI Timing Characteristics

Minimum values across full temperature range T_{MIN} = 0°C to T_{MAX} = 85°C, AVDD_5V = 5V, AVDD=3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	SCLK period	50			ns
t_2	SCLK high time	20			ns
t_3	SCLK low time	20			ns
t_4	Data setup time	5			ns
t_5	Data hold time	5			ns
t_6	$\overline{SEN}$ fall to SCLK rise	8			ns
t_7	Time between last SCLK rising edge to $\overline{SEN}$ rising edge	8			ns
t_8	SDOUT delay	12	20	28	ns

Serial Register Readout

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic test to verify the serial interface communication between the external controller and the AFE. First, the <REGISTER READOUT ENABLE> bit (Reg0[1]) needs to be set to '1'. Then user should initiate a serial interface cycle specifying the address of the register (A7-A0) whose content has to be read. The data bits are "don't care". The device will output the contents (D15-D0) of the selected register on the SDOUT pin. SDOUT has a typical delay, t_8, of 20nS from the falling edge of the SCLK. For lower speed SCLK, SDOUT can be latched on the rising edge of SCLK. For higher speed SCLK,e.g. the SCLK period lesser than 60nS, it is better to latch the SDOUT at the next falling edge of SCLK. The following timing diagram shows this operation (the time specifications follow the same information provided. In the readout mode, users still can access the <REGISTER READOUT ENABLE> through SDATA/SCLK/SEN. To enable serial register writes, set the <REGISTER READOUT ENABLE> bit back to '0'.

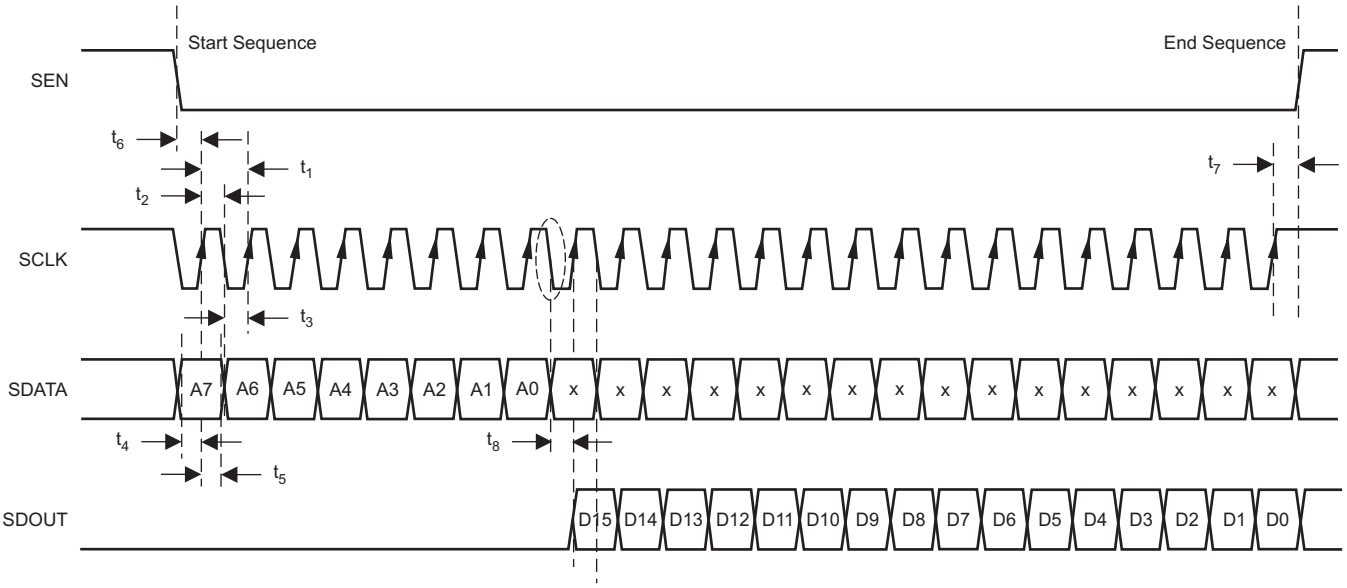
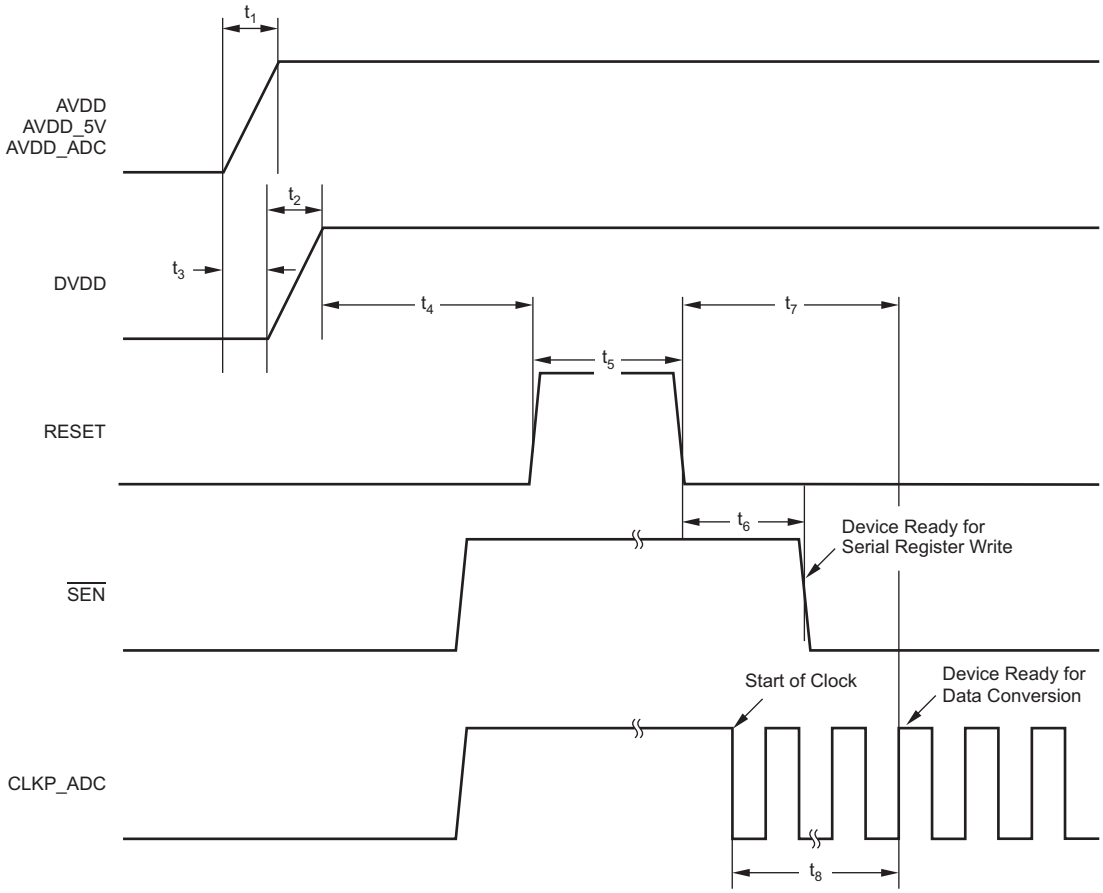


Figure 63. Serial Interface Register Read

The AFE5809 SDOUT buffer is tri-stated and will get enabled only when 0[1] (REGISTER READOUT ENABLE) is enabled. SDOUT pins from multiple AFE5809s can be tied together without any pull-up resistors. Level shifter SN74AUP1T04 can be used to convert 1.8V logic to 2.5V/3.3V logics if needed.



10µs < t1 < 50ms, 10µs < t2 < 50ms, –10ms < t3 < 10ms, t4 > 10ms, t5 > 100ns, t6 > 100ns, t7 > 10ms, and t8 > 100µs.

The AVDDx and DVDD power-on sequence does not matter as long as –10ms < t3 < 10ms. Similar considerations apply while shutting down the device.

Figure 64. Recommended Power-up Sequencing and Reset Timing

ADC and VCA Register Description

A reset process is required at the AFE5809 initialization stage. Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a positive pulse in the RESET pin
2. Through a software reset, using the serial interface, by setting the SOFTWARE RESET bit to high. Setting this bit initializes the internal registers to the respective default values (all zeros) and then self-resets the SOFTWARE RESET bit to low. In this case, the RESET pin can stay low (inactive).

After reset, all ADC and VCA registers are set to '0', that is default setting. During register programming, all unlisted register bits need to be set as '0'.

Note some demodulator registers are set as '1' after reset. During register programming, all unlisted register bits need to be set as '0'. In addtion, the demodulator registers can be reset when 0x16[0] is set as '0'. Thus it is required to reconfigure the demodulator registers after toggling the 0x16[0] from '1' to '0'.

ADC Register Map

Table 2. ADC Register Map

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
0[0]	0x0[0]	0	SOFTWARE_RESET	0: Normal operation; 1: Resets the device and self-clears the bit to '0'
0[1]	0x0[1]	0	REGISTER_READOUT_ENABLE	0:Disables readout; 1: enables readout of register at SDOUT Pin
1[0]	0x1[0]	0	ADC_COMPLETE_PDN	0: Normal 1: Complete Power down
1[1]	0x1[1]	0	LVDS_OUTPUT_DISABLE	0: Output Enabled; 1: Output disabled
1[9:2]	0x1[9:2]	0	ADC_PDN_CH<7:0>	0: Normal operation; 1: Power down. Power down Individual ADC channels. 1[9]→CH8…1[2]→CH1
1[10]	0x1[10]	0	PARTIAL_PDN	0: Normal Operation; 1: Partial Power Down ADC
1[11]	0x1[11]	0	LOW_FREQUENCY_ NOISE_SUPPRESSION	0: No suppression; 1: Suppression Enabled
1[13]	0x1[13]	0	EXT_REF	0: Internal Reference; 1: External Reference. VREF_IN is used. Both 3[15] and 1[13] should be set as 1 in the external reference mode
1[14]	0x1[14]	0	LVDS_OUTPUT_RATE_2X	0: 1x rate; 1: 2x rate. Combines data from 2 channels on 1 LVDS pair. When ADC clock rate is low, this feature can be used
1[15]	0x1[15]	0	SINGLE-ENDED_CLK_MODE	0: Differential clock input; 1: Single-ended clock input
2[2:0]	0x2[2:0]	0	RESERVED	Set to 0
2[10:3]	0x2[10:3]	0	POWER-DOWN_LVDS	0: Normal operation; 1: PDN Individual LVDS outputs. 2[10]→CH8…2[3]→CH1
2[11]	0x2[11]	0	AVERAGING_ENABLE	0: No averaging; 1: Average 2 channels to increase SNR
2[12]	0x2[12]	0	LOW_LATENCY	0: Default Latency with digital features supported 1: Low Latency with digital features bypassed.
2[15:13]	0x2[15:13]	0	TEST_PATTERN_MODES	000: Normal operation; 001: Sync; 010: De-skew; 011: Custom; 100:All 1's; 101: Toggle; 110: All 0's; 111: Ramp.
3[7:0]	0x3[7:0]	0	INVERT_CHANNELS	0: No inverting; 1:Invert channel digital output. 3[7]→CH8;3[0]→CH1
3[8]	0x3[8]	0	CHANNEL_OFFSET_ SUBSTRACTION_ENABLE	0: No offset subtraction; 1: Offset value Subtract Enabled

Table 2. ADC Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
3[9:11]	0x3[9:11]	0	RESERVED	Set to 0
3[12]	0x3[12]	0	DIGITAL_GAIN_ENABLE	0: No digital gain; 1: Digital gain Enabled
3[14:13]	0x3[14:13]	0	SERIALIZED_DATA_RATE	Serialization factor 00: 14x 01: 16x 10: reserved 11: 12x when 4[1]=1. In the 16x serialization rate, two 0s are filled at two LSBs (see Table 1). Note: Make sure the settings aligning with the demod register 0x3[14:13]. Please also aware that the same setting , e.g. "00", in these two registers can represent different LVDS data rates respectively.
3[15]	0x3[15]	0	ENABLE_EXTERNAL_ REFERENCE_MODE	0: Internal reference mode; 1: Set to external reference mode Note: Both 3[15] and 1[13] should be set as 1 when configuring the device in the external reference mode
4[1]	0x4[1]	0	ADC_RESOLUTION_SELECT	0: 14bit; 1: 12bit
4[3]	0x4[3]	0	ADC_OUTPUT_FORMAT	0: 2's complement; 1: Offset binary **Note: When the demodulation feature is enabled, only 2's complement format can be selected.**
4[4]	0x4[4]	0	LSB_MSB_FIRST	0: LSB first; 1: MSB first
5[13:0]	0x5[13:0]	0	CUSTOM_PATTERN	Custom pattern data for LVDS output (2[15:13]=011)
10[8]	0xA[8]	0	SYNC_PATTERN	0: Test pattern outputs of 8 channels are NOT synchronized. 1: Test pattern outputs of 8 channels are synchronized.
13[9:0]	0xD[9:0]	0	OFFSET_CH1	Value to be subtracted from channel 1 code
13[15:11]	0xD[15:11]	0	DIGITAL_GAIN_CH1	0dB to 6dB in 0.2 dB steps
15[9:0]	0xF[9:0]	0	OFFSET_CH2	value to be subtracted from channel 2 code
15[15:11]	0xF[15:11]	0	DIGITAL_GAIN_CH2	0dB to 6dB in 0.2 dB steps
17[9:0]	0x11[9:0]	0	OFFSET_CH3	value to be subtracted from channel 3 code
17[15:11]	0x11[15:11]	0	DIGITAL_GAIN_CH3	0dB to 6dB in 0. 2dB steps
19[9:0]	0x13[9:0]	0	OFFSET_CH4	value to be subtracted from channel 4 code
19[15:11]	0x13[15:11]	0	DIGITAL_GAIN_CH4	0dB to 6dB in 0.2 dB steps
21[0]	0x15[0]	0	DIGITAL_HPF_FILTER_ENABLE _ CH1-4	0: Disable the digital HPF filter; 1: Enable for 1-4 channels
21[4:1]	0x15[4:1]	0	DIGITAL_HPF_FILTER_K_CH1-4	Set K for the high-pass filter (k from 2 to 10, that is 0010B to 1010B). This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k/(2^k + 1) [x(n) – x(n – 1) + y(n – 1)]$ (please see Table 3)
22[0]	0x16[0]	0	EN_DEMOD	0: Digital demodulator is enabled 1: Digital demodulator is disabled. Note: The demodulator registers can be reset when 0x16[0] is set as '0'. Thus it is required to reconfigure the demodulator registers after toggling the 0x16[0].
25[9:0]	0x19[9:0]	0	OFFSET_CH8	value to be subtracted from channel 8 code
25[15:11]	0x19[15:11]	0	DIGITAL_GAIN_CH8	0dB to 6dB in 0.2 dB steps
27[9:0]	0x1B[9:0]	0	OFFSET_CH7	value to be subtracted from channel 7 code
27[15:11]	0x1B[15:11]	0	DIGITAL_GAIN_CH7	0dB to 6dB in 0. dB steps
29[9:0]	0x1D[9:0]	0	OFFSET_CH6	value to be subtracted from channel 6 code
29[15:11]	0x1D[15:11]	0	DIGITAL_GAIN_CH6	0dB to 6dB in 0.2 dB steps
31[9:0]	0x1F[9:0]	0	OFFSET_CH5	value to be subtracted from channel 5 code
31[15:11]	0x1F[15:11]	0	DIGITAL_GAIN_CH5	0dB to 6dB in 0. 2dB steps
33[0]	0x21[0]	0	DIGITAL_HPF_FILTER_ENABLE _ CH5-8	0: Disable the digital HPF filter; 1: Enable for 5-8 channels

Table 2. ADC Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
33[4:1]	0x21[4:1]	0	DIGITAL_HPF_FILTER_K_CH5-8	Set K for the high-pass filter (k from 2 to 10, 0010B to 1010B) This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k/(2^k + 1)\ [x(n) – x(n – 1) + y(n – 1)]$ (please see Table 3)

AFE5809 ADC Register/Digital Processing Description

The ADC in the AFE5809 has extensive digital processing functionalities which can be used to enhance ultrasound system performance. The digital processing blocks are arranged as in Figure 65.

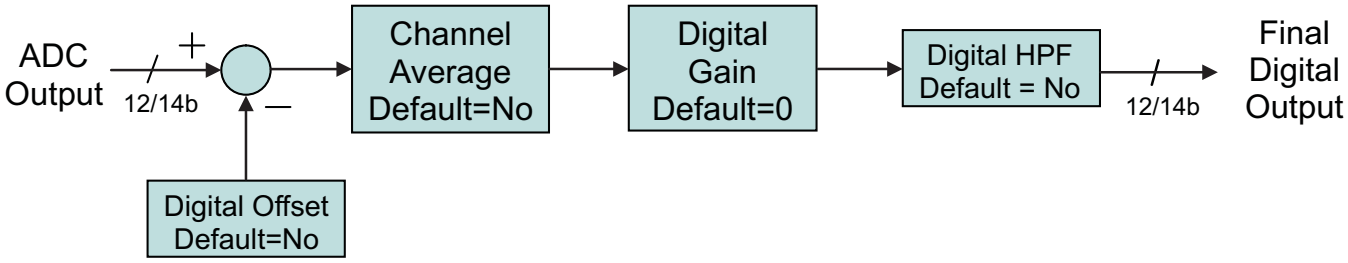


Figure 65. ADC Digital Block Diagram

AVERAGING_ENABLE: Address: 2[11]

When set to 1, two samples, corresponding to two consecutive channels, are averaged (channel 1 with 2, 3 with 4, 5 with 6, and 7 with 8). If both channels receive the same input, the net effect is an improvement in SNR. The averaging is performed as:

- Channel 1 + channel 2 comes out on channel 3
- Channel 3 + channel 4 comes out on channel 4
- Channel 5 + channel 6 comes out on channel 5
- Channel 7 + channel 8 comes out on channel 6

ADC_OUTPUT_FORMAT: Address: 4[3]

The ADC output, by default, is in 2's-complement mode. Programming the ADC_OUTPUT_FORMAT bit to 1 inverts the MSB, and the output becomes straight-offset binary mode. **When the demodulation feature is enabled, only 2's complement format can be selected**.

ADC Reference Mode: Address 1[13] & 3[15]

The following shows the regester settings for the ADC internal reference mode and external reference mode.

- 0x1[13] 0x3[15]=00: ADC internal reference mode, VREF_IN floating (pin M3)
- 0x1[13] 0x3[15]=01: N/A
- 0x1[13] 0x3[15]=10: N/A
- 0x1[13] 0x3[15]=11: ADC external eference mode, VREF_IN=1.4V (pin M3)

DIGITAL_GAIN_ENABLE: Address: 3[12]

Setting this bit to 1 applies to each channel i the corresponding gain given by DIGTAL_GAIN_CHi <15:11>. The gain is given as 0dB + 0.2dB × DIGTAL_GAIN_CHi<15:11>. For instance, if DIGTAL_GAIN_CH5<15:11> = 3, channel 5 is increased by 0.6dB gain. DIGTAL_GAIN_CHi <15:11> = 31 produces the same effect as DIGTAL_GAIN_CHi <15:11> = 30, setting the gain of channel i to 6dB.

DIGITAL_HPF_ENABLE

- CH1-4: Address 21[0]
- CH5-8: Address 33[0]

DIGITAL_HPF_FILTER_K_CHX

- CH1-4: Address 21[4:1]
- CH5-8: Address 33[4:1]

This group of registers controls the characteristics of a digital high-pass transfer function applied to the output data, following Equation 1.

$$y(n) = \frac{2^k}{2^k + 1}\left[x(n) - x(n-1) + y(n-1)\right] \quad (1)$$

These digital HPF registers (one for the first four channels and one for the second group of four channels) describe the setting of K. The digital high pass filter can be used to suppress low frequency noise which commonly exists in ultrasound echo signals. The digital filter can significantly benefit near field recovery time due to T/R switch low frequency response. Table 3 shows the cut-off frequency vs K.

Table 3. Digital HPF –1dB Corner Frequency vs. K and Fs

k	40 MSPS	50 MSPS	65 MSPS
2	2780 KHz	3480 KHz	4520 KHz
3	1490 KHz	1860 KHz	2420 KHz
4	770 KHz	960 KHz	1250 KHz

LOW_FREQUENCY_NOISE_SUPPRESSION: Address: 1[11]

The low-frequency noise suppression mode is especially useful in applications where good noise performance is desired in the frequency band of 0MHz to 1MHz (around dc). Setting this mode shifts the low-frequency noise of the AFE5809 to approximately Fs/2, thereby moving the noise floor around dc to a much lower value. Register bit 1[11] is used for enabling or disabling this feature. When this feature is enabled, power consumption of the device will be increased slightly by approximate 1mW/CH.

LVDS_OUTPUT_RATE_2X: Address: 1[14]

The output data always uses a DDR format, with valid/different bits on the positive as well as the negative edges of the LVDS bit clock, DCLK. The output rate is set by default to 1X (LVDS_OUTPUT_RATE_2X = 0), where each ADC has one LVDS stream associated with it. If the sampling rate is low enough, two ADCs can share one LVDS stream, in this way lowering the power consumption devoted to the interface. The unused outputs will output zero. To avoid consumption from those outputs, no termination should be connected to them. The distribution on the used output pairs is done in the following way:

- Channel 1 and channel 2 come out on channel 3. Channel 1 comes out first.
- Channel 3 and channel 4 come out on channel 4. Channel 3 comes out first.
- Channel 5 and channel 6 come out on channel 5. Channel 5 comes out first.
- Channel 7 and channel 8 come out on channel 6. Channel 7 comes out first

CHANNEL_OFFSET_SUBSTRACTION_ENABLE: Address: 3[8]

Setting this bit to 1 enables the subtraction of the value on the corresponding OFFSET_CHx<9:0> (offset for channel i) from the ADC output. The number is specified in 2s-complement format. For example, OFFSET_CHx<9:0> = 11 1000 0000 means subtract –128. For OFFSET_CHx<9:0> = 00 0111 1111 the effect is to subtract 127. In effect, both addition and subtraction can be performed. Note that the offset is applied before the digital gain (see DIGITAL_GAIN_ENABLE). The whole data path is 2s-complement throughout internally, with digital gain being the last step. Only when ADC_OUTPUT_FORMAT = 1 (straight binary output format) is the 2s-complement word translated into offset binary at the end.

SERIALIZED_DATA_RATE: Address: 3[14:13]

Please see Table 1 for detail description.

TEST_PATTERN_MODES: Address: 2[15:13]

The AFE5809 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. The device may also be made to output 6 preset patterns:

1. **Ramp:** Setting Register 2[15:13]=111causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.
2. **Zeros:** The device can be programmed to output all zeros by setting Register 2[15:13]=110;
3. **Ones:** The device can be programmed to output all 1s by setting Register 2[15:13]=100;
4. **Deskew Patten:** When 2[15:13]= 010; this mode replaces the 14-bit ADC output with the 01010101010101

word.

5. **Sync Pattern:** When 2[15:13]= 001, the normal ADC output is replaced by a fixed 11111110000000 word.
6. **Toggle:** When 2[15:13]=101, the normal ADC output is alternating between 1's and 0's. The start state of ADC word can be either 1's or 0's.
7. **Custom Pattern:** It can be enabled when 2[15:13]= 011;. Users can write the required VALUE into register bits <CUSTOM PATTERN> which is Register 5[13:0]. Then the device will output VALUE at its outputs, about 3 to 4 ADC clock cycles after the 24th rising edge of SCLK. So, the time taken to write one value is 24 SCLK clock cycles + 4 ADC clock cycles. To change the customer pattern value, users can repeat writing Register 5[13:0] with a new value. Due to the speed limit of SPI, the refresh rate of the custom pattern may not be high. For example, 128 points custom pattern will take approximately 128 x (24 SCLK clock cycles + 4 ADC clock cycles).

NOTE

only one of the above patterns can be active at any given instant.

SYNC_PATTERN: Address: 10[8]

By enabling this bit, all channels' test pattern outputs are synchronized. When 10[8] is set as 1, the ramp patterns of all 8 channels start simultaneously.

VCA Register Map

Table 4. VCA Register Map

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
51[0]	0x33[0]	0	RESERVED	0
51[3:1]	0x33[3:1]	0	LPF_PROGRAMMABILITY	000: 15MHz, 010: 20 MHz, 011: 30MHz, 100: 10 MHz. Please note: 0x3D[14], i.e. 5MHz LPF, should be set a 0.
51[4]	0x33[4]	0	PGA_INTEGRATOR_DISABLE (PGA_HPF_DISABLE)	0: Enable 1: Disable offset integrator for PGA. See the explanation for the PGA integrator function in the APPLICATION INFORMATION section
51[7:5]	0x33[7:5]	0	PGA_CLAMP_LEVEL	Low Noise mode: 53[11:10]=00 000: –2 dBFS 010: 0 dBFS 1XX: Clamp is disabled Low power/Medium Power mode; 53[11:10]=01/10 100: –2 dBFS 110: 0 dBFS 0XX: clamp is disabled Note: the clamp circuit makes sure that PGA output is in linear range. For example, at 000 setting, PGA output HD3 will be worsen by 3 dB at –2 dBFS ADC input. In normal operation, clamp function can be set as 000 in the low noise mode. The maximum PGA output level can exceed 2Vpp with the clamp circuit enabled. Note: in the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0. . Note: Reg.61[15] should be set as 0; otherwise PGA_CLAMP_LEVEL is determined by Reg. 61[15].
51[13]	0x33[13]	0	PGA_GAIN_CONTROL	0:24 dB; 1:30 dB.
52[4:0]	0x34[4:0]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_CNTL	SeeTable 9 Reg 52[5] should be set as '1' to access these bits
52[5]	0x34[5]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_ENABLE	0: Disable; 1: Enable internal active termination individual resistor control
52[7:6]	0x34[7:6]	0	PRESET_ACTIVE_ TERMINATIONS	00: 50 Ω, 01: 100 Ω 10: 200 Ω 11: 400 Ω (Note: the device will adjust resistor mapping (52[4:0]) automatically. 50 Ω active termination is NOT supported in 12 dB LNA setting. Instead, '00' represents high impedance mode when LNA gain is 12 dB)
52[8]	0x34[8]	0	ACTIVE TERMINATION ENABLE	0: Disable; 1: Enable active termination
52[10:9]	0x34[10:9]	0	LNA_INPUT_CLAMP_SETTING	00: Auto setting, 01: 1.5 Vpp, 10: 1.15 Vpp and 11: 0.6 Vpp
52[11]	0x34[11]	0	RESERVED	Set to 0

Table 4. VCA Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
52[12]	0x34[12]	0	LNA_INTEGRATOR_DISABLE (LNA_HPF_DISABLE)	0: Enable; 1: Disable offset integrator for LNA. See the explanation for this function in the following section
52[14:13]	0x34[14:13]	0	LNA_GAIN	00: 18 dB; 01: 24 dB; 10: 12 dB; 11: Reserved
52[15]	0x34[15]	0	LNA_INDIVIDUAL_CH_CNTL	0: Disable; 1: Enable LNA individual channel control. See Register 57 for details
53[7:0]	0x35[7:0]	0	PDN_CH<7:0>	0: Normal operation; 1: Powers down corresponding channels. Bit7→CH8, Bit6→CH7…Bit0→CH1. PDN_CH will shut down whichever blocks are active depending on TGC mode or CW mode
53[8]	0x35[8]	0	RESERVED	Set to 0
53[9]	0x35[9]	0	LOW_NF	0: Normal operation 1: Enable low noise figure mode for high impedance probes
53[11:10]	0x35[11:10]	0	POWER_MODES	00: Low noise mode; 01: Set to low power mode. At 30dB PGA, total chain gain may slightly change. See typical characteristics 10:Set to medium power mode.At 30dB PGA, total chain gain may slightly change. See typical characteristics 11: Reserved
53[12]	0x35[12]	0	PDN_VCAT_PGA	0: Normal operation; 1: Powers down VCAT (voltage-controlled-attenuator) and PGA
53[13]	0x35[13]	0	PDN_LNA	0: Normal operation; 1: Powers down LNA only
53[14]	0x35[14]	0	VCA_PARTIAL_PDN	0: Normal operation; 1: Powers down LNA, VCAT, and PGA partially(fast wake response)
53[15]	0x35[15]	0	VCA_COMPLETE_PDN	0: Normal operation; 1: Power down LNA, VCAT, and PGA completely (slow wake response). This bit can overwrite 53[14].
54[4:0]	0x36[4:0]	0	CW_SUM_AMP_GAIN_CNTL	Select Feedback resistor for the CW Amplifier as per Table 9 below
54[5]	0x36[5]	0	CW_16X_CLK_SEL	0: Accept differential clock; 1: Accept CMOS clock
54[6]	0x36[6]	0	CW_1X_CLK_SEL	0: Accept CMOS clock; 1: Accept differential clock
54[7]	0x36[7]	0	RESERVED	Set to 0
54[8]	0x36[8]	0	CW_TGC_SEL	0: TGC Mode; 1 : CW Mode Note : VCAT and PGA are still working in CW mode. They should be powered down separately through 53[12]
54[9]	0x36[9]	0	CW_SUM_AMP_ENABLE	0: Enable CW summing amplifier; 1: Disable CW summing amplifier Note: 54[9] is only effective in CW mode.

Table 4. VCA Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
54[11:10]	0x36[11:10]	0	CW_CLK_MODE_SEL	00: 16X mode; 01: 8X mode; 10: 4X mode; 11: 1X mode
55[3:0]	0x37[3:0]	0	CH1_CW_MIXER_PHASE	0000→1111, 16 different phase delays, see Table 8
55[7:4]	0x37[7:4]	0	CH2_CW_MIXER_PHASE	
55[11:8]	0x37[11:8]	0	CH3_CW_MIXER_PHASE	
55[15:12]	0x37[15:12]	0	CH4_CW_MIXER_PHASE	
56[3:0]	0x38[3:0]	0	CH5_CW_MIXER_PHASE	
56[7:4]	0x38[7:4]	0	CH6_CW_MIXER_PHASE	
56[11:8]	0x38[11:8]	0	CH7_CW_MIXER_PHASE	
56[15:12]	0x38[15:12]	0	CH8_CW_MIXER_PHASE	
57[1:0]	0x39[1:0]	0	CH1_LNA_GAIN_CNTL	00: 18 dB; 01: 24 dB; 10: 12 dB; 11: Reserved REG52[15] should be set as '1'
57[3:2]	0x39[3:2]	0	CH2_LNA_GAIN_CNTL	
57[5:4]	0x39[5:4]	0	CH3_LNA_GAIN_CNTL	00: 18dB; 01: 24 dB; 10: 12 dB; 11: Reserved REG52[15] should be set as '1'
57[7:6]	0x39[7:6]	0	CH4_LNA_GAIN_CNTL	
57[9:8]	0x39[9:8]	0	CH5_LNA_GAIN_CNTL	
57[11:10]	0x39[11:10]	0	CH6_LNA_GAIN_CNTL	
57[13:12]	0x39[13:12]	0	CH7_LNA_GAIN_CNTL	
57[15:14]	0x39[15:14]	0	CH8_LNA_GAIN_CNTL	
59[3:2]	0x3B[3:2]	0	HPF_LNA	00: 100 KHz; 01: 50 Khz; 10: 200 Khz; 11: 150 KHz with 0.015 µF on INMx
59[6:4]	0x3B[6:4]	0	DIG_TGC_ATT_GAIN	000: 0 dB attenuation; 001: 6 dB attenuation; N: ~N×6 dB attenuation when 59[7] = 1
59[7]	0x3B[7]	0	DIG_TGC_ATT	0: disable digital TGC attenuator; 1: enable digital TGC attenuator
59[8]	0x3B[8]	0	CW_SUM_AMP_PDN	0: Power down; 1: Normal operation Note: 59[8] is only effective in TGC test mode.
59[9]	0x3B[9]	0	PGA_TEST_MODE	0: Normal CW operation; 1: PGA outputs appear at CW outputs
61[13]	0x3D[13]	0	V2I_CLAMP	0: Clamp disabled; 1: Clamp enabled at the V2I input. An additional voltage clamp at the V2I input.This limits the amount of overload signal the PGA sees. Note: this bit is supported by AFE5809 with date code later than 2014, i.e. date code >41XXXX.
61[14]	0x3D[14]	0	5MHz_LPF	0: 5MHz LPF disabled; 1: 5MHz LPF enabled. Suppress signals >5MHz or high order harmonics. The other low pass filter 10/15/20/30MHz set by Reg.51[3:1] is not active. Note: this bit is supported by AFE5809 with date code later than 2014, i.e. date code >41XXXX.

Table 4. VCA Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
61[15]	0x3D[15]	0	PGA_CLAMP_-6dBFS	0: Disable the -6dBFS clamp. PGA_CLAMP is set by Reg51[7:5]. 1: Enable the -6dBFS clamp. i.e. PGA output HD3 will be worsen by 3 dB at –6 dBFS ADC input. The actual PGA output is reduced to ~1.5Vpp. As a result, AFE5809's low pass filter (LPF) is not saturated and it can suppress harmonic signals better at PGA output. Due to reduction PGA output, the ADC output dynamic range is impacted. PGA_CLAMP set by Reg51[7:5] is NOT active. Note: this bit is supported by AFE5809 with date code later than 2014, i.e. date code >41XXXX.

VCA Register Description

LNA Input Impedances Configuration (Active Termination Programmability)

Different LNA input impedances can be configured through the register 52[4:0]. By enabling and disabling the feedback resistors between LNA outputs and ACTx pins, LNA input impedance is adjustable accordingly. Table 5 describes the relationship between LNA gain and 52[4:0] settings. The input impedance settings are the same for both TGC and CW paths.

The AFE5809 also has 4 preset active termination impedances as described in 52[7:6]. An internal decoder is used to select appropriate resistors corresponding to different LNA gain.

Table 5. Register 52[4:0] Description

52[4:0]/0x34[4:0]	FUNCTION
00000	No feedback resistor enabled
00001	Enables 450 Ω feedback resistor
00010	Enables 900 Ω feedback resistor
00100	Enables 1800 Ω feedback resistor
01000	Enables 3600 Ω feedback resistor
10000	Enables 4500 Ω feedback resistor

Programmable Gain for CW Summing Amplifier

Different gain can be configured for the CW summing amplifier through the register 54[4:0]. By enabling and disabling the feedback resistors between the summing amplifier inputs and outputs, the gain is adjustable accordingly to maximize the dynamic range of CW path. Table 6 describes the relationship between the summing amplifier gain and 54[4:0] settings.

Table 6. Register 54[4:0] Description

54[4:0]/0x36[4:0]	FUNCTION
00000	No feedback resistor
00001	Enables 250 Ω feedback resistor
00010	Enables 250 Ω feedback resistor
00100	Enables 500 Ω feedback resistor
01000	Enables 1000 Ω feedback resistor
10000	Enables 2000 Ω feedback resistor

Table 7. Register 54[4:0] vs Summing Amplifier Gain

54[4:0]/0x36[4:0]	00000	00001	00010	00011	00100	00101	00110	00111
CW I/V Gain	N/A	0.50	0.50	0.25	1.00	0.33	0.33	0.20
54[4:0]/0x36[4:0]	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**

Table 7. Register 54[4:0] vs Summing Amplifier Gain (continued)

54[4:0]/0x36[4:0]	**00000**	**00001**	**00010**	**00011**	**00100**	**00101**	**00110**	**00111**
CW I/V Gain	2.00	0.40	0.40	0.22	0.67	0.29	0.29	0.18
54[4:0]/0x36[4:0]	**10000**	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**10111**
CW I/V Gain	4.00	0.44	0.44	0.24	0.80	0.31	0.31	0.19
54[4:0]/0x36[4:0]	**11000**	**11001**	**11010**	**11011**	**11100**	**11101**	**11110**	**11111**
CW I/V Gain	1.33	0.36	0.36	0.21	0.57	0.27	0.27	0.17

Programmable Phase Delay for CW Mixer

Accurate CW beamforming is achieved through adjusting the phase delay of each channel. In the AFE5809, 16 different phase delays can be applied to each LNA output; and it meets the standard requirement of typical ultrasound beamformer, that is $\frac{1}{16}\lambda$ beamformer resolution. Table 6 describes the relationship between the phase delays and the register 55 and 56 settings.

Table 8. CW Mixer Phase Delay vs Register Settings
CH1 - 55[3:0], CH2 - 55[7:4], CH3 - 55[11:8], CH4 - 55[15:12],
CH5- 56[3:0], CH6 - 56[7:4], CH7 - 56[11:8], CH8 - 56[15:12],

CHX_CW_MIXER_PHASE	0000	0001	0010	0011	0100	0101	0110	0111
PHASE SHIFT	0	22.5°	45°	67.5°	90°	112.5°	135°	157.5°
CHX_CW_MIXER_PHASE	1000	1001	1010	1011	1100	1101	1110	1111
PHASE SHIFT	180°	202.5°	225°	247.5°	270°	292.5°	315°	337.5°

Table 9. Register 52[4:0] vs LNA Input Impedances

52[4:0]/0x34[4:0]	**00000**	**00001**	**00010**	**00011**	**00100**	**00101**	**00110**	**00111**
LNA:12dB	High Z	150 Ω	300 Ω	100 Ω	600 Ω	120 Ω	200 Ω	86 Ω
LNA:18dB	High Z	90 Ω	180 Ω	60 Ω	360 Ω	72 Ω	120 Ω	51 Ω
LNA:24dB	High Z	50 Ω	100 Ω	33 Ω	200 Ω	40 Ω	66.67 Ω	29 Ω
52[4:0]/0x34[4:0]	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
LNA:12dB	1200 Ω	133 Ω	240 Ω	92 Ω	400 Ω	109 Ω	171 Ω	80 Ω
LNA:18dB	720 Ω	80 Ω	144 Ω	55 Ω	240 Ω	65 Ω	103 Ω	48 Ω
LNA:24dB	400 Ω	44 Ω	80 Ω	31 Ω	133 Ω	36 Ω	57 Ω	27 Ω
52[4:0]/0x34[4:0]	**10000**	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**10111**
LNA:12dB	1500 Ω	136 Ω	250 Ω	94 Ω	429 Ω	111 Ω	176 Ω	81 Ω
LNA:18dB	900 Ω	82 Ω	150 Ω	56 Ω	257 Ω	67 Ω	106 Ω	49 Ω
LNA:24dB	500 Ω	45 Ω	83 Ω	31 Ω	143 Ω	37 Ω	59 Ω	27 Ω
52[4:0]/0x34[4:0]	**11000**	**11001**	**11010**	**11011**	**11100**	**11101**	**11110**	**11111**
LNA:12dB	667 Ω	122 Ω	207 Ω	87 Ω	316 Ω	102 Ω	154 Ω	76 Ω
LNA:18dB	400 Ω	73 Ω	124 Ω	52 Ω	189 Ω	61 Ω	92 Ω	46 Ω
LNA:24dB	222 Ω	41 Ω	69 Ω	29 Ω	105 Ω	34 Ω	51 Ω	25 Ω

SPI Interface for Demodulator

Demodulator is enabled after software or hardware reset. It can be disabled by setting the LSB of register 0x16 as '1'. This is done using the ADC SPI interface, that is SPI_DIG_EN=1. The demodulator SPI interface is independent from the ADC/VCA SPI interface as shown in Figure 66:

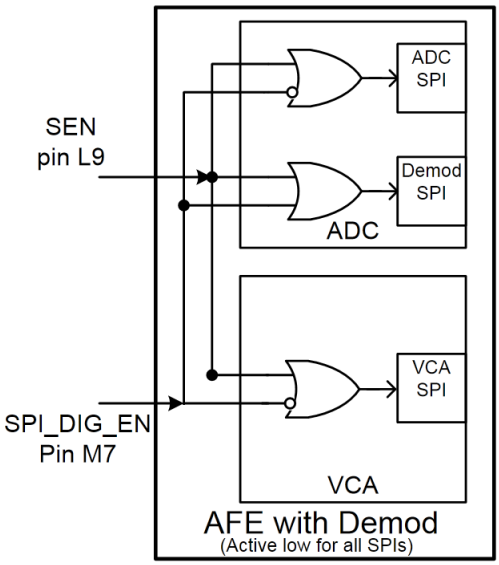


Figure 66. SPI Interface in the AFE5809

To access the specific demodulator registers:

1. SPI_DIG_EN pin is required to be set as '0' during SPI transactions to demodulator registers. Meanwhile ADC SEN needs to be set as '0' during demodulator SPI programming.
2. SPI register address is 8 bits and is made of 2 sub-chip select bits and 6 register address bits. SPI register data is 16bits.

Table 10. Register Address Bit Description

Bit7	Bit6	Bit 5:0
SCID1_SEL	SCID0_SEL	Register Address <5:0>

3. SCID0_SEL enables configuration of channels 1-4. 'SCID1_SEL' enables configuration of channels 5-7. When performing Demodulator SPI write transactions, these SCID bits can be individually or mutually used with a specific register address.
4. Register configuration is normally shared by both subchips (both 'SCID' bits should be set as '1'). An exception to this rule would be the DC OFFSET registers (0x14-0x17) for which specific channel access is expected.

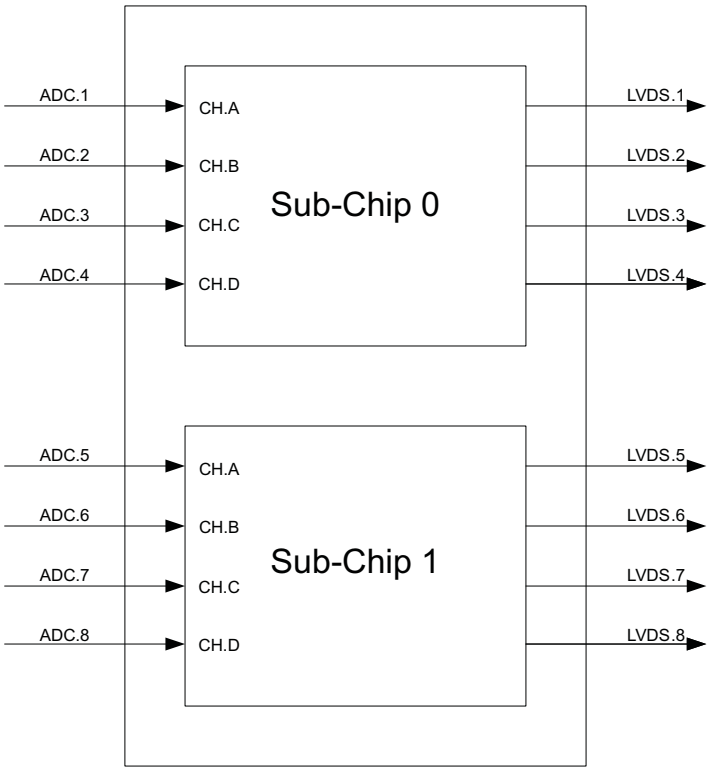


Figure 67. Each of Two Sub-chips Supports 4 Channels. Each of Two Demodulators has 4 Channels Named as A, B, C, D

5. Demodulator register readout follows the following procedures:
   - Write '1' to register 0x0[1]; pin SPI_DIG_EN should be '0' while writing. This is the readout enable register for demodulator.
   - Write '1' to register 0x0[1], pin SPI_DIG_EN should be '1' while writing.This is the readout enable register for ADC and VCA.
   - Set SPI_DIG_EN as '0' and write anything to the register whose stored data needs to be known. Device finds the address of the register and sends its stored data at the SDOUT pin serially.

NOTE

After enabling the register 0x0[1] REGISTER_READOUT_ENABLE, data can't be written to the register (whose data needs to be known) but stored data would come serially at the SDOUT pin.

   - To disable the register readout, first write '0' to register 0x0[1] while SPI_DIG_EN is '1'; then write '0' to register 0x0[1] while SPI_DIG_EN is '0'.

Table 11. Digital Demodulator Register Map

Note: 1. When programming the SPI, 8-bit address is required. The below table and following sections only list the Add_Bit5 to Add_Bit0. The Add_Bit7=SCID1_SEL and Add_Bit6=SCID0_SEL need to be appended as 11, 10, or 01, which determines either SubChip1 or SubChip0 is being programmed. If SCID1_SEL,SCID0_SEL = 11, then both subchips get written with the same register value. Please see Table 10. 2. Reserved register bits must be programmed based on their descriptions. 3. Unlisted register bits must be programmed as 0s

Register Name	Add(Hex) Bit[5:0]	Add(Dec) Bit[5:0]	Default	Description
MANUAL_TX_TRIG	00[2]	00[2]	0	1: generate internal tx_trig (self clear, Write Only). This is an alternative for TX_SYNC hardware pulse.
REGISTER_READOUT_ENABLE	00[1]	00[1]	0	1:enables readout of register at SDOUT pin (Write Only)
CHIP_ID	01[4:0]	01[4:0]	0	Unique Chip ID
OUTPUT_MODE	02[15:13]	02[15:13]	0	000-normal operation 011- custom pattern (set by register 05). NOTE: LSB always comes out first no matter 0x04[4]=0 or 1 111- chipID + ramp test pattern. ChipID (5 bit) and Sub-chip information (3 bit) are the 8 LSBs and the ramp pattern is in the rest MSBs. (0x0A[9] = 1)
SERZ_FACTOR	03[14:13]	03[14:13]	11	Serialization factor (output rate) 00-10x 01-12x 10-14x 11-16x. Note: this register is different from the ADC SERIALIZED_DATA_RATE. The demod and ADC serilization factors must be matched. Please see LVDS Serialization Factor.
OUTPUT_RESOLUTION	03[11:9]	03[11:9]	0	Output resoluiton of the demodulator. It refers to the ADC resolution when the demodulator is bypassed. 100-16bit(DEMOD only) 000-14bit 001-13bit 010-12bit
MSB_FIRST	04[4]	04[4]	0	0-LSB first; 1-MSB first. This bit will not affect the test mode: customer pattern, that is 02[15:13]=011B. Note: in the CUSTOM_PATTERN mode, the output is always set as LSB first regardless of this bit setting.
CUSTOM_PATTERN	05[15:0]	05[15:0]	0000	Custom data pattern for LVDS (0x02[15:13]=011)
COEFF_MEM_ADDR_WR	06[7:0]	06[7:0]	0	Write address offset to coefficient memory (auto increment)
COEFF_BANK	07[111:0]	07[111:0]	---	Writes chunks of 112 bits to the coefficient memory. This RAM does not have default values, so it is necessary to write required values to the RAM. It is recommended to configure the RAM before other registers.
PROFILE_MEM_ADDR_WR	08[4:0]	08[4:0]	0	Write address offset to profile memory (auto increment)
PROFILE_BANK	09 [63:0]	09 [63:0]	---	Writes chunks of 64 bits to the profile memory (effective 62 bits since two LSBs are ignored). This RAM does not have default values, so it is necessary to write required values to the RAM. It is recommended to configure the RAM before other registers.
RESERVED	0A[15]	10[15]	0	**Must set to 0.**
MODULATE_BYPASS	0A[14]	10[14]	0	Arrange the demodulator output format for I/Q data. Please see Table 13.
DEC_SHIFT_SCALE	0A[13]	10[13]	0	0- no addtional shift applied to the decimation filter output. 1-shift the decimation filter output by 2 bits addtionally, that is apply 12dB addtional digital gain.
RESERVED	0A[12]	10[12]	1	**Must set to 1**.
OUTPUT_CHANNEL_SEL	0A[11]	10[11]	0	Swap channel pairs. It is used in 4 LVDS bypass configuration to select which of the two possible data streams to pass on. See table 13.
SIN_COS_RESET_ON_TX_TRIG	0A[10]	10[10]	1	0-Continuous phase 1-Reset down convertion phase on TX_TRIG
FULL_LVDS_MODE	0A[9]	10[9]	0	0-Use 4 LVDS lines (1,3,5,7) 1-Use 8 LVDS lines (1-8) Note: 4 LVDS mode valid only for decimation factors ≥4. Please see Table 13.
RESERVED	0A[8:5]	10[8:5]	0	**Must set to 0.**
RESERVED	0A[4]	10[4]	0	**Must set to 1.**
DEC_BYPASS	0A[3]	10[3]	0	0-Enable decimation filter 1-Bypass decimation filter

Table 11. Digital Demodulator Register Map (continued)

Note: 1. When programming the SPI, 8-bit address is required. The below table and following sections only list the Add_Bit5 to Add_Bit0. The Add_Bit7=SCID1_SEL and Add_Bit6=SCID0_SEL need to be appended as 11, 10, or 01, which determines either SubChip1 or SubChip0 is being programmed. If SCID1_SEL,SCID0_SEL = 11, then both subchips get written with the same register value. Please see Table 10. 2. Reserved register bits must be programmed based on their descriptions. 3. Unlisted register bits must be programmed as 0s				
Register Name	**Add(Hex) Bit[5:0]**	**Add(Dec) Bit[5:0]**	**Default**	**Description**
DWN_CNV_BYPASS	0A[2]	10[2]	0	0-Enable down conversion block 1-Bypass down conversion block. Note: the decimaiton filter still can be used when the down conversion block is bypassed.
RESERVED	0A[1]	10[1]	1	**Must be set as 1.**
DC_REMOVAL_BYPASS	0A[0]	10[0]	0	0-Enable DC removal block 1-Bypass DC removal block
SYNC_WORD	0B[15:0]	11[15:0]	0x2772	LVDS sync word. When MODULATE_BYPASS=1, there is no sync word output.
PROFILE_INDX	0E[15:11]	14[15:11]	0	Profile word selector. The Profile Index register is a Special 5 bit data register. Read value still uses 16 bit convention which means data will be available on LSB 0e[4:0])
DC_REMOVAL_1_5	14[13:0]	20[13:0]	0	54[13:0]→DC offset for channel 1, SCID1_SEL,SCID0_SEL=01 94[13:0]→DC offset for channel 5, SCID1_SEL,SCID0_SEL=10 Note: considering the CH to CH DC offset variation, the offset value has to be set individually. Therefore, SCID1_SEL,SCID0_SEL should not be set as 11.
DC_REMOVAL_2_6	15[13:0]	21[13:0]	0	55[13:0]→DC offset for channel 2, SCID1_SEL,SCID0_SEL=01 95[13:0] →DC offset for channel 6, SCID1_SEL,SCID0_SEL=10 Note: considering the CH to CH DC offset variation, the offset value has to be set individually. Therefore SCID1_SEL,SCID0_SEL should not be set as 11.
DC_REMOVAL_3_7	16[13:0]	22[13:0]	0	56[13:0] →DC offset for channel 3, SCID1_SEL,SCID0_SEL=01 96[13:0] →DC offset for channel 7, SCID1_SEL,SCID0_SEL=10 Note: considering the CH to CH DC offset variation, the offset value has to be set individually. Therefore SCID1_SEL,SCID0_SEL should not be set as 11.
DC_REMOVAL_4_8	17[13:0]	23[13:0]	0	57[13:0] →DC offset for channel 4, SCID1_SEL,SCID0_SEL=01 97[13:0] →DC offset for channel 8, SCID1_SEL,SCID0_SEL=10 Note: considering the CH to CH DC offset variation, the offset value has to be set individually. Therefore SCID1_SEL,SCID0_SEL should not be set as 11.
DEC_SHIFT_FORCE_EN	1D[7]	29[7]	0	0-Profile vector specifies the number of bit to shift for the decimation filter output. 1-Reg.1D[6:4] specifies the number of bit to shift for the decimation filter output.
DEC_SHIFT_FORCE	1D[6:4]	29[6:4]	0	Specify that the decimation filter output is right shifted by (20-N) bit, N=0x1D[6:4]. N=0, minimal digital gain; N=7 maximal digital gain; additional 12 dB digital gain can be applied by setting DEC_SHIFT_SCALE = 1,that is 0x0A[13]=1;
TM_COEFF_EN	1D[3]	29[3]	0	1-set coefficient output test mode
TM_SINE_EN	1D[2]	29[2]	0	1-set sine output mode; the sine waveform specifications can be configured through register 0x1E.
RESERVED	1D[1]	29[1]	0	**MUST set to 0**
RESERVED	1D[0]	29[0]	0	**MUST set to 0**
TM_SINE_DC	1E[15:9]	30[15:9]	0	7 bit signed value for sine wave DC offset control.
TM_SINE_AMP	1E[8:5]	30[8:5]	0	4 bit unsigned value, controlling the sin wave amplitude (powers of two), from unity to the full scale of 14 bit, including saturation. 0: no sine (only DC).
TM_SINE_STEP	1E[4:0]	30[4:0]	0	5 bit unsigned value, controlling the sin wave frequency with resolution of $Fs/2^6$, which is 0.625MHz for 40 MHz ADC clock.

Table 11. Digital Demodulator Register Map (continued)

Note: 1. When programming the SPI, 8-bit address is required. The below table and following sections only list the Add_Bit5 to Add_Bit0. The Add_Bit7=SCID1_SEL and Add_Bit6=SCID0_SEL need to be appended as 11, 10, or 01, which determines either SubChip1 or SubChip0 is being programmed. If SCID1_SEL,SCID0_SEL = 11, then both subchips get written with the same register value. Please see Table 10. 2. Reserved register bits must be programmed based on their descriptions. 3. Unlisted register bits must be programmed as 0s				
Register Name	**Add(Hex) Bit[5:0]**	**Add(Dec) Bit[5:0]**	**Default**	**Description**
MANUAL_COEFF_START_EN	1F[15]	31[15]	0	0: The starting address of the coefficient RAM is set by the profile vector. that is the starting address is set manually. 1: The starting address of the coefficient RAM is set by the register 0x1F[14:7].
MANUAL_COEFF_START_ADDR	1F[14:7]	31[14:7]	0	When 0x1F[15] is set, the starting address of coefficient RAM is set by these 8 bits.
MANUAL_DEC_FACTOR_EN	1F[6]	31[6]	0	0: The decimation factor is set by profile vector. 1: The decimation factor is set by the register 0x1F[5:0].
MANUAL_DEC_FACTOR	1F[5:0]	31[5:0]	0	When 0x1F[6] is set, the decimation factor is set by these 6 bits. Note: it is from 1 to 32.
MANUAL_FREQ_EN	20[0]	32[0]	0	0: The down convert frequency is set by profile vector. 1: The down convert frequency is set by the register 0x21[15:0].
MANUAL_FREQ	21[15:0]	33[15:0]	0	When 0x20[0] is set, the value of manual down convert frequency is calculated as N x Fs /2^{16}

Digital Demodulator Register Description

Table 12. Configuring Data Output:

Register Name	**SPI Address**
SERZ_FACTOR	0x03[14:13]
OUTPUT_RESOLUTION	0x03[11:9]
MSB_FIRST	0x04[4]
OUT_MODE	0x02[15:13]
CUSTOM_PATTERN	0x05[15:0]
OUTPUT_CHANNEL_SEL	0x0A[11]
MODULATE_BYPASS	0x0A[14]
FULL_LVDS_MODE	0x0A[9]

1. Serializer Configuration:
   - Serialization Factor 0x03[14:13]: It can be set using demodulator register SERZ_FACTOR. Default serialization factor for the demodulator is 16x. However, the actual LVDS clock speed can be set by the serialization factor in the ADC SPI interface as well; the ADC serialization factor is adjusted to 14x by default. Therefore, it is necessary to sync these two settings when demodulator is enabled, that is set the ADC register 0x03[14:13]=01.
   - Output Resolution 0x03[11:9]: In the default setting, it is 14 bit. The demodulator output resolution depends on the decimation factor. 16 bit resolution can be used when higher decimation factor is selected.
2. Channel Selection:
   - Using register MODULATE_BYPASS 0x0A[14], channel output mode can be selected as IQ modulated or single channel I or Q output.
   - Channel output is also selected using registers OUTPUT_CHANNEL_SEL 0x0A[11]& FULL_LVDS_MODE 0x0A[9] and decimation factor.
   - Each of two demodulator sub-chips in a device has 4 channels named as A, B, C, D. After decimation, the LVDS FCLK rate keeps the same as the ADC sampling rate. Considering the reduced data amount, zeros will be appended after I and Q data and ensure the LVDS data rate matches the LVDS clock rate.

For detailed information about channel multiplexing, see Table 13. In the table, A.I refers to CHA In-phase output, and A.Q refers to CHA Quadrature output.

3. Output Mode:
   - Using register OUT_MODE, ramp pattern and custom pattern can be enabled.
   - Custom Pattern: In case of custom pattern, custom pattern value can be set using register CUSTOM_PATTERN. Please Note: LSB always comes out first no matter 0x04[4]=0 or 1, that is MSB_FIRST= 0 or 1.
   - Ramp Pattern: Demodulator generated ramp pattern includes information of chip_id as well. 8 MSB (that is Data[15..8]) bits are ramp pattern. Next 5 bits (that is Data[3..7]) gives value of chip ID. Data[2] corresponds to sub-chip ID, 0 or 1; Data[1:0] are filled with zeros.

Table 13. Channel Selection

Decimation Factor (M)	Modulate bypass	Output Channel Select	Full LVDS mode	Decimation Factor M	LVDS Output Description
M>= 2	0	0	0	M <4	LVDS1: A.I, A.Q,(zeros)
					LVDS2: B.I, B.Q,(zeros)
					LVDS3: C.I, C.Q,(zeros)
					LVDS4: D.I, D.Q,(zeros)
				M>= 4	LVDS1: A.I, A.Q, B.I, B.Q, (zeros) LVDS2: idle
					LVDS3: C.I, C.Q, D.I, D.Q, (zeros) LVDS4: idle
			1	X	LVDS1: A.I, A.Q,(zeros)
					LVDS2: B.I, B.Q,(zeros)
					LVDS3: C.I, C.Q,(zeros)
					LVDS4: D.I, D.Q,(zeros)
		1	0	M<4	LVDS1: B.I, B.Q,(zeros)
					LVDS2: A.I, A.Q,(zeros)
					LVDS3: D.I, D.Q,(zeros)
					LVDS4: C.I, C.Q,(zeros)
				M>=4	LVDS1: B.I, B.Q, A.I, A.Q, (zeros)
					LVDS2: idle
					LVDS3: D.I, D.Q, C.I, C.Q, (zeros)
					LVDS4: idle
			1	X	LVDS1: B.I, B.Q,(zeros)
					LVDS2: A.I, A.Q,(zeros)
					LVDS3: D.I, D.Q,(zeros)
					LVDS4: C.I, C.Q,(zeros)
M>= 2	1	0	X	X	LVDS1: A.I; Note: the same A.I is repeated by M times.
					LVDS2: A.Q; Note: the same A.Q is repeated by M times.
					LVDS3: C.I; Note: the same C.I is repeated by M times.
					LVDS4: C.Q; Note: the same C.Q is repeated by M times.
		1	X	X	LVDS1: B.I; Note: the same B.I is repeated by M times.
					LVDS2: B.Q; Note: the same B.Q is repeated by M times.
					LVDS3: D.I; Note: the same D.I is repeated by M times.
					LVDS4: D.Q; Note: the same D.Q is repeated by M times.
M=1	0	0	X	1	LVDS1: A.I; LVDS2: B.I; LVDS3: C.I; LVDS4: D.I
M=1	0	1	X	1	LVDS1: B.I; LVDS2: A.I; LVDS3: D.I; LVDS4: C.I
M=1	1	0	X	1	LVDS1: A.I; LVDS2: A.Q; LVDS3: C.I; LVDS4: C.Q
M=1	1	1	X	1	LVDS1: B.I; LVDS2: B.Q; LVDS3: D.I; LVDS4: D.Q
	Note: This table refers to individual demodulator subchip, which has 4 LVDS outputs, i.e.LVDS1~4; and 4 Input CHs, i.e. CH.A to CH.D. Please see Figure 67				

Table 14. DC Removal Block

Register Name	SPI Address
DC_REMOVAL_BYPASS	0x0A[0]
DC_REMOVAL_1_5	0x14[13:0]
DC_REMOVAL_2_6	0x15[13:0]
DC_REMOVAL_3_7	0x16[13:0]
DC_REMOVAL_4_8	0x17[13:0]

- DC removal block can be bypassed using the register bit DC_REMOVAL_BYPASS.
- DC removal is designed to be done manually.
- Manual DC offset removal: Registers DC_REMOVAL_1_5, DC_REMOVAL_2_6, DC_REMOVAL_3_7, DC_REMOVAL_4_8 can be used to give manual offset. Value should be given in 2's compliment format. In case of these registers, SCID values should be given accordingly (check section "SPI interface for Demodulator" for more information). Example: For DC offset of channel 5, address of the register would be 0x91 (in hex). Here SCID0 is '0' and SCID1 is '1'.

Table 15. Down Conversion Block

Register Name	SPI Address
DWN_CNV_BYPASS	0x0A[2]
SIN_COS_RESET_ON_TX_TRIG	0x0A[10]
MANUAL_FREQ_EN	0x20 [0]
MANUAL_FREQ	0x21[15:0]

- Down Conversion Block can be bypassed using register DWN_CNV_BYPASS.
- Down Conversion Frequency can be given using "Down Conversion Frequency (f)" parameter of Profile Vector. Alternatively manual registers MANUAL_FREQ_EN and MANUAL_FREQ can be used to provide down conversion frequency.
- Down Conversion frequency (f): 'f' can be set with resolution Fs /2^{16}. (Where Fs is the sampling frequency). An integer value of "2^{16}f / Fs" is to be given to the profile vector or respective register
- Down conversion signal can be configured to be reset at each TX_TRIG pulse. This facility can be enabled using SIN_COS_RESET_ON_TX_TRIG.

Table 16. Decimation Block

Register Name	SPI Address
DEC_BYPASS	0x0A[3]
MANUAL_DEC_FACTOR_EN	0x1F [6]
MANUAL_DEC_FACTOR	0x1F[5:0]
MANUAL_COEFF_START_EN	0x1F[15]
MANUAL_COEFF_START_ADDR	0x1F[14:7]
DEC_SHIFT_FORCE_EN	0x1D[7]
DEC_SHIFT_FORCE	0x1D[6:4]
DEC_SHIFT_SCALE	0x0A[13]

- Decimation block can be bypassed using register DEC_BYPASS.
- Decimation Factor: This can be set using "Decimation Factor (M)" parameter of profile vector. Alternatively it can be set using registers MANUAL_DEC_FACTOR_EN and MANUAL_DEC_FACTOR.
- Filter Coefficients: Filter coefficients should be written to coefficient RAM (check Coefficient RAM section above). Format of filter coefficient is 2's compliment. Its address pointer should be given in profile vector or alternatively registers MANUAL_COEFF_START_EN and MANUAL_COEFF_START_ADDR can be used.
- Filter Digital Gain: Decimation block takes 14 bit input data and 14 bit input coefficients and gives 36 bit output internally. While implementing this FIR filter, after multiplication and addition, the 36 bit internal filter output should be scaled approximately to make final demod output as 16 bit, that is applying digital gain or attenuation. Filter gain or attenuation depends on two parameters: Decimation Shift Scale and Gain Compensation factor.
- Decimation Shift Scale can be chosen using register DEC_SHIFT_SCALE. Gain Compensation factor can be given to "Gain Compensation Factor (G)" parameter of Profile Vector; or can be given using registers DEC_SHIFT_FORCE_EN and DEC_SHIFT_FORCE.
- The internal 36 bit filter output is right shifted by N bits, where N equals to
  - 20-G when Dec_Shift_Scale=0.
  - 20-G-2 when Dec_Shift_Scale=1.

  The minimal gain occurs when G=0 and DEC_SHIFT_SCALE=0. The total scaling range can be a factor of 2^9, that is ~54 dB.

Table 17. Test Modes

Register Name	SPI Address
TM_SINE_DC	0x1E[15:9]
TM_SINE_AMP	0x1E[8:5]
TM_SINE_STEP	0x1E[4:0]
TM_SINE_EN	0x1D[2]
TM_COEFF_EN	0x1D[3]

1. Sine test mode:

   The normal ADC output can be replaced by:

$$x_n = C + 2^k \sin(\frac{\pi N n}{2^5}) \quad (2)$$

   - N is 5 bit unsigned value, controlling the sin wave frequency with resolution of $F_S/2^6$, which is 0.625 MHz for 40 MHz ADC clock.
   - k is 4 bit unsigned value, controlling the wave amplitude, from unity to the full scale of 14 bit, including saturation.
   - C is 7 bit signed value for DC offset control.

   The controlling values fit into one 16bit register. This test pattern shall allow testing of demodulation, decimation filter, DC removal, gain control, and so on.
2. Coefficient output test mode:
   - The Input to the decimating filter can be replaced with a sequence of "one impulse" and "zero" samples, where "one impulse(that is 0x4000)" is followed by (16 x M) "zeros (that is 0 × 0000)".
   - This mode is useful to check decimation filter coefficients.
   - This mode can be enabled using register TM_COEFF_EN.

Profile RAM and Coefficient RAM

Writing data to Profile RAM and Coefficient RAM is similar to registers. Both RAMs do not get reset after resetting the device. RAM does not have default values, so it is necessary to write required values to RAM. RAM address values needs to be given to pointer register that points to the location wherever data needs to be written. Since both RAMs are part of Demodulator, SPI_DIG_EN should be low while writing.

It is recommended to program the RAMs before configuring other registers.

Table 18. Profile Related Registers

Register Name	SPI Address
PROFILE_MEM_ADDR_WR	0x08[4:0]
PROFILE_BANK	0x09[63:0]
PROFILE_INDEX	0x0E[15:11]

- Profile RAM can store up to 32 Vectors/Profiles. Each Vector/Profile has 64 bits.
- Pointer Value should be given to the register PROFILE_MEM_ADDR_WR before writing to RAM.
- The 64 bits of each Vector/Profile are arranged as follows:

Table 19. Profile RAM

Name of parameter	Address	Description
Reserved	RAM[63:50]	Set to 0
Reserved	RAM[49:36]	Set to 0
Pointer to Coeff Memory (P)*	RAM[35:28]	A pointer to filter coefficient memory (8 bit), pointing to 8coefficients blocks. The relevant coefficients will start from address P*8 in the coefficients memory and will continue for M blocks.
Decimation Factor (M)*	RAM[27:22]	Decimation Factor for Decimation Block
Down Conversion Frequency (f)*	RAM[21:6]	Down Conversion frequency for Down Conversion Block
Reserved	RAM[5]	Set to 0
Gain Compensation Factor (G) *	RAM[4:2]	Gain Compensation Factor Parameter for Decimation block
*Alternate manual register is available • 2 LSB's (that is RAM[1:0]) are ignored and can be set as 0s. • A particular profile vector can be activated using register PROFILE_INDEX. Address pointing to the location of particular vector is to be given in PROFILE_INDEX.		

Table 20. Coefficient RAM

Register Name	SPI Address
COEFF_MEM_ADDR_WR	0x06[7:0]
COEFF_BANK	0x07[111:0]
MANUAL_COEFF_START_ADDR	0x1F[14:7]
MANUAL_COEFF_START_EN	0x1F[15]

- Coefficient RAM can store up to 256 coefficient memory blocks. Size of each block is 112 bits.
- Pointer Value should be given to the register COEFF_MEM_ADDR_WR before writing to RAM.
- Write 112 bits to SPI address 0xC7 (MSB first). Each coefficient memory block consists of 8 14bit coefficients which are aligned in the following manner: (Coefficient order from right to left. Bit order from right to left).
- **Note: the coefficients are in 2's complement format.**

Table 21. Coefficient RAM mapping.

Note that SPI serialization is done from left to right (0xCoeff 7[13] first and 0xCoeff 0[0] last)

Coeff 7[13:0]	Coeff 6[13:0]	Coeff 5[13:0]	Coeff 4[13:0]	Coeff 3[13:0]	Coeff 2[13:0]	Coeff 1[13:0]	Coeff 0[13:0]
111:98	97:84	83:70	69:56	55:42	41:28	27:14	13:0

- Since Decimation block uses 16 x M tap FIR filter and filter coefficients are symmetric, only half (that is 8 x M) filter coefficients are necessary to be stored (M is the decimation factor). Each 8 coefficient block that is written to the memory represents a single phase of a polyphase filter. Therefore; the relation between the filter coefficients Cn and their index (i,j) in the coefficients memory is given by:

$$n = M \times (1 + I) - (1 + j) \quad (3)$$

where I is the index in the coefficients block, from 0 to 7, and j is the block index, from 0 to (M-1) . Example for M = 4

Table 22. Coefficient RAM Mapping

j\I	7	6	5	4	3	2	1	0
0	Coeff 31	Coeff 27	Coeff 23	Coeff 19	Coeff 15	Coeff 11	Coeff 7	Coeff 3
1	Coeff 30	Coeff 26	Coeff 22	Coeff 18	Coeff 14	Coeff 10	Coeff 6	Coeff 2
2	Coeff 29	Coeff 25	Coeff 21	Coeff 17	Coeff 13	Coeff 9	Coeff 5	Coeff 1
3	Coeff 28	Coeff 24	Coeff 20	Coeff 16	Coeff 12	Coeff 8	Coeff 4	Coeff 0

- Coefficient start address can be given using "Pointer to Coeff Memory (P)" parameter of profile RAM. Alternatively start address can be given using register MANUAL_COEFF_START_ADDR. (While using this register, register enable bit MANUAL_COEFF_START_EN should be set to '1').

Register Readout

While reading data from Demodulator registers Procedure:

- Write '1' to register 0x0[1]; pin SPI_DIG_EN should be '0' while writing, that is it is the readout enable register for demodulator.
- Write '1' to register 0x0[1]; pin SPI_DIG_EN should be '1' while writing, that is it is the readout enable register for VCA and ADC.
- Put SPI_DIG_EN 'low' and write anything to the register whose stored data needs to be known. Device finds the address of the register and sends its stored data at the SDOUT pin serially. Note: After enabling the register 0x0[1] REGISTER_READOUT_ENABLE, register data can not be written to the register, whose data needs to be known. The stored data would come serially at the SDOUT pin.
- To disable the register readout, first write '0' to register 0x0[1] while SPI_DIG_EN is high; then write '0' to register 0x0[1] while SPI_DIG_EN is low.

LVDS Serialization Factor

Default serialization factor for the demodulator is 16×. However, the actual LVDS clock speed is set by the serialization factor in the ADC SPI interface and is adjusted to 14× serialization by default. It is therefore necessary to sync these two settings when demodulator is enabled. When using the default demodulator serialization factor, register 0x03[14:13] in the ADC SPI interface should be set to '01'. For RF mode (passing 14 bits only), demodulator serialization factor can be changed to 14x by setting demodulator register 0xC3[14:13] to '10'.

Programming the Coefficient RAM

1. Set SPI address 0xC6[7:0] with the base address, e.g. 0x0000. 0xC6 means both demodulator subchips are enabled.
2. Write 112 bits to SPI address 0xC7 (MSB first). Each coefficient memory word consists of eight 14bit coefficients which are aligned in the following manner. **Note: the coefficients are in 2's complement format.**

Figure 68. Coefficient Order from Right to left. Bit Order from Right to Left

Coeff 7[13:0]	Coeff 6[13:0]	Coeff 5[13:0]	Coeff 4[13:0]	Coeff 3[13:0]	Coeff 2[13:0]	Coeff 1[13:0]	Coeff 0[13:0]
111:98	97:84	83:70	69:56	55:42	41:28	27:14	13:0

NOTE

Note that SPI serialization is done from left to right (Coeff 7[13] first and Coeff 0[0] last).

3. Repeat step 2 for the following coefficient bulk entries (the address in register 0xC6 auto increments).

Programming the Profile RAM

1. Set SEN and SPI_DIG_EN as '0'.
2. Set SPI address 0xC8[4:0] with the base address, e.g. 0x0000. 0xC8 means both demodulator subchips are enabled.
3. The 64 profile vector bits are arranged as following:
   - RAM[63:50] = 0 Reserved
   - RAM[49:36] = 0 Reserved
   - RAM[35:28]- Pointer to coeff Memory (8bit)
   - RAM[27:22]- decimation factor (6bit)
   - RAM[21:6]- Demodulation frequency (16bit)
   - RAM[5] = 0
   - RAM[4:2]- Gain Compensation Factor (3bit)
   - RAM[1:0]- 2 LSBs are ignored, can be set as 0s.
4. Write the above 64 bits to SPI address 0xC9. MSB first.
5. Repeat step 3 and 4 for the following profile entries (the address in register 0xC8 will auto increment).
6. Set SEN and SPI_DIG_EN as '1'.

Procedure for configuring next vector

1. Write profile index (5 bits) to SPI address 0xCE[15:11]. 0xCE means both demodulator subchips are enabled.

RF Mode

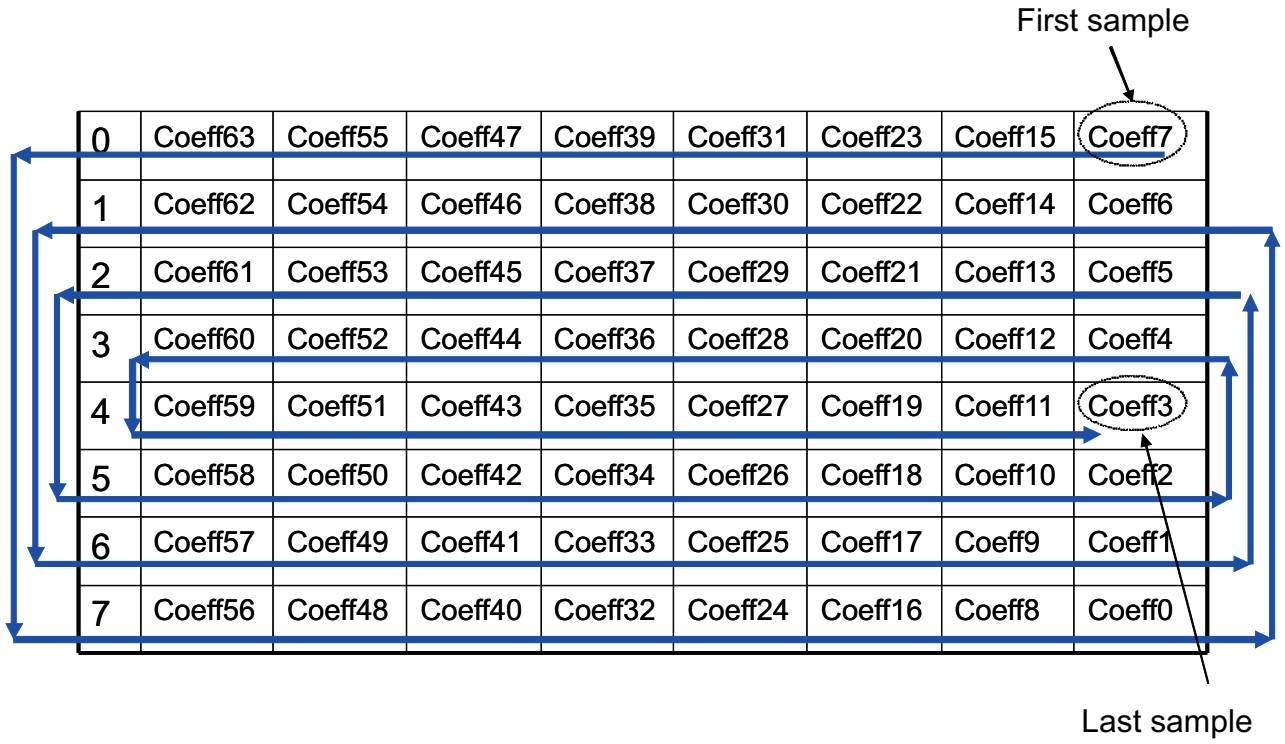
RF mode allows for the streaming of ADC data through the demodulator to the LVDS. Note: test pattern from the ADC output stage cannot be sent to the demodulator (it can only be sent to the LVDS when the demodulator is off). RF mode without sync word can be set by the following:

1. Write 0x0041 to register 0xDF; that is MANUAL_DEC_FACTOR_EN=1 and MANUAL_DEC_FACTOR=1.
2. Write 0x121F to register 0xCA; that is MODULATE_BYPASS=0 , FULL_LVDS_MODE=1, DC_REMOVAL_BYPASS=1, DWN_CNV_BYPASS=1. DEC_BYPASS=1, SYN_COS_RESET_ON_TX_TRIG=0.
3. Write 0x6800 to register 0xC3; that is SERZ_FACTOR=16x, OUTPUT_RESOLUTION=16x,
4. Write 0x0010 to register 0xC4; that is MSB_FIRST=1
5. Provide TX_TRIG pulse or set Reg 0xC0[2] MANUAL_TX_TRIG

Filter Coefficent Test mode

Coefficent test mode allows for the streaming of coefficents through the demodulator to the LVDS. Filter coefficent test mode can be set by the following:

1. Enable TM_COEFF_EN.
2. Write OUTPUT_RESOLUTION (0x03[11:9]) = 0b100 , that is16 bit output (Note that output bit resolution of 14 bit will not give proper result).
3. Write DC_REMOVAL_BYPASS (0x0A[0]) =1, DWN_CNV_BYPASS (0x0A[2])=1.
4. Write DC_DEC_SHIFT_FORCE_EN (0x1D[7])=1, DEC_SHIFT_FORCE (0x1D[6:4]=0b110 and DEC_SHIFT_SCALE (0x0a[13])=1
5. Write MODULATE_BYPASS (0x0A[14]) =1. After writing all of the above settings, coefficients come at the output in the sequence as below
6. M=2
   - Address 0: C15 C13 C11 C09 C07 C05 C03 C01; Address 1: C14 C12 C10 C08 C06 C04 C02 C00
   - The order in which coefficients will come at the output will be: 0 C01 C03 C05 C07 C09 C11 C13 C15 C14 C12 C10 C08 C06 C04 C02 C00 C00 C02 C04 C06 C08 C10 C12 C14 C15 C13 C11 C09 C07 C05 C03 C01 0
7. M=8
   - The coefficents come to the output as shown in Figure 69.



Note: once it reaches to last sample, it will start giving coefficients in the reverse direction till it reaches the point it started.

Figure 69. Coefficient Readout Sequence

TX_SYNC and SYNC_WORD TIMING

As shown in the below figure, hardware TX_SYNC is latched at the next negative edge of the ADC Clock after 0 to 1 transition of TX_SYNC. The time gap between latched edge and the start of the LVDS SYNC_WORD is kT ns where T is the time period of ADC Clock and k = 16 + decFactor + 1. t_{SETUP} and t_{HOLD} can be considered as 1.5ns in the normal condition. Both will be at the negative edge of the ADC Clock.

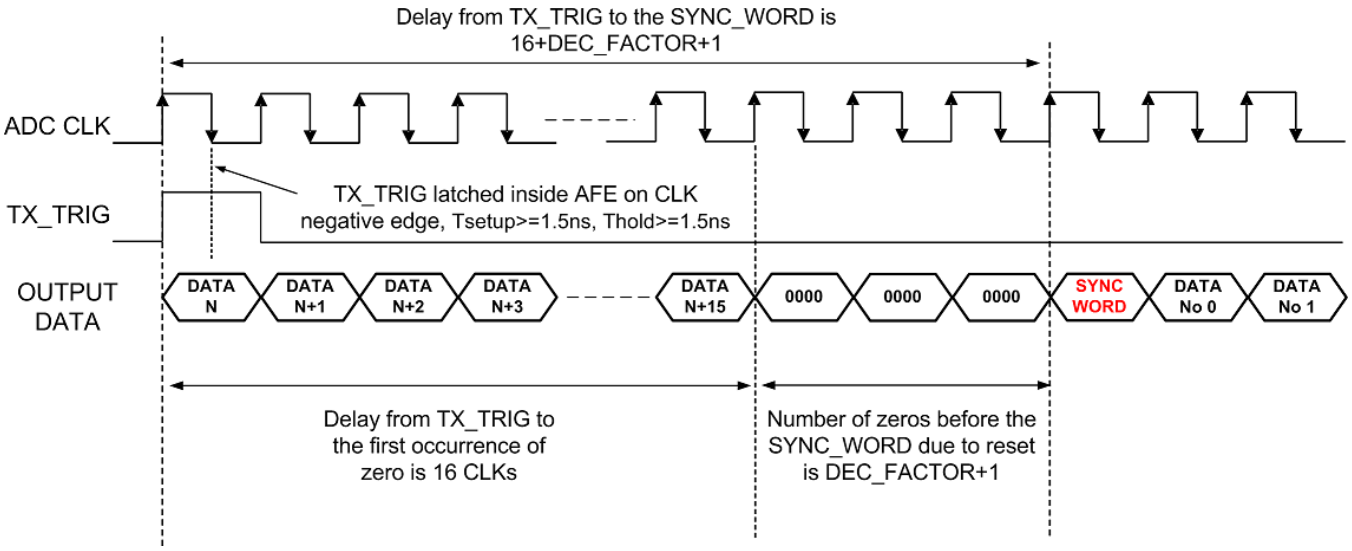


Figure 70. Sync Word Generation with Respect to TX_TRIG

FIR Filter Delay vs. TX_TRIG Timing

AFE5809's decimation filter is a symmetric M×16 order FIR filter, where M is the decimation factor from 1 to 32. Half of the M×16 coefficients are stored in the filter coefficient memory.

For a discrete-time FIR filter, its output is a weighted sum of the current and a finite number of previous values of the input as the below equation shows:

$$Y[n] = C0 \times X[n] + C1 \times X[n-1] ... + C_N \times X[n-N] \quad (4)$$

where X[n] is the input signal, Y[n] is the output signal, CN is the filter coefficients, and N is the filter order. Therefore the delay of AFE5809 output is related to decimation factor M. The TX_TRIG timing also plays a role in this. In the below description, we use M=1 and M=2 as examples to derive a generic timing relationship among TX_TRIG, AFE input and AFE output.

The below register settings are used when the delay relationship was measured:

- Enable demodulator (22[0]=1, or 0x16[0]=1)
- Set different decimation factor and other settings in profile RAM.
- Write filter coefficients in coefficient memory.
- Set DEC_SHIFT_FORCE_EN (29[7] =1 or 0x1D[7]=1)
- Set DEC_SHIFT_SCALE (10[13]=1 or 0xA[13]=1)
- Set DEC_SHIFT_FORCE (29[6:4]=6, or 0x1D[6:4]=6)
- Set RESERVED bits (10[15]=0, 10[12]=1, 10[4]=1, 10[1]=1; or 0xA[15]=0, 0xA[12]=1, 0xA[4]=1, 0xA[1]=1)
- Set DC_REMOVAL_BYPASS (10[0] = 1 or 0xA[0]=1)
- SIN_COS_RESET_ON_TX_TRIG (10[10]=1 or 0xA[10]=1)
- SERZ_FACTOR (03[14:13] = 11) (16X serialization)
- OUTPUT_RESOLUTION (03[11:9] = 100) (16 bit)
- MSB_FIRST (04[4] =1)
- SYNC_WORD (11[15:0] or 0xB[15:0]) (Set sync word. It can be user dependent)
- Down conversion is enabled and down convert frequency set to 0 i.e. multiply input signal with DC. Please

note even this frequency is set to value other than 0, will not change the demod latency. For experiment ease mixing with DC is performed.

- • Please note that, ADC sampling frequency and VCA LPF settings has been kept such that AFE5809's demod sees a single pulse.

When M=1, 8 filter coefficients written in the memory are C0, C1 to C7. An impulse signal is applied at both VCA input and TX_TRIG. Due to the impulse input, coefficients starts coming at the output according to timing diagram shown in the figure below, where 20 cycle delay is observed.

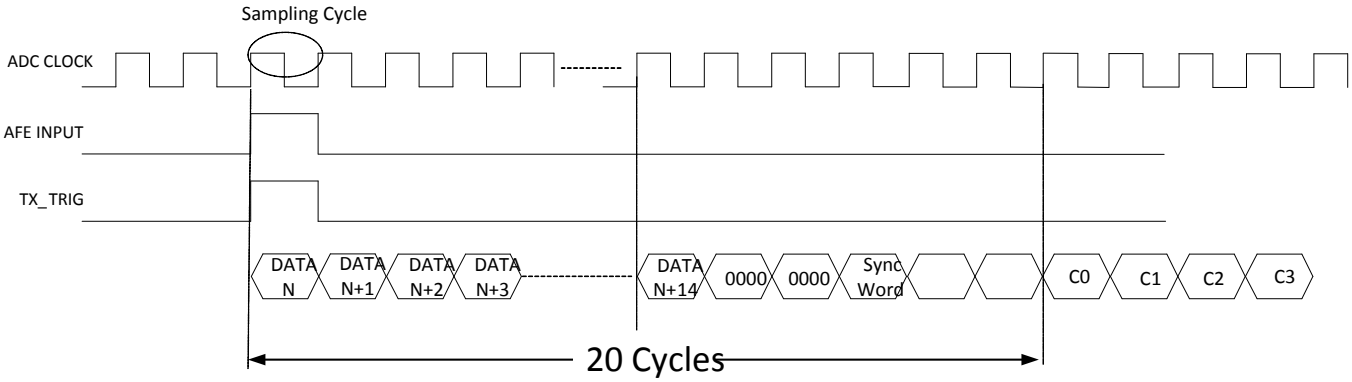


Figure 71. Expected Latency Timing when M=1

By adjusting the timing between AFE input and TX_TRIG, we can obtain a timing diagram similar as Figure 71

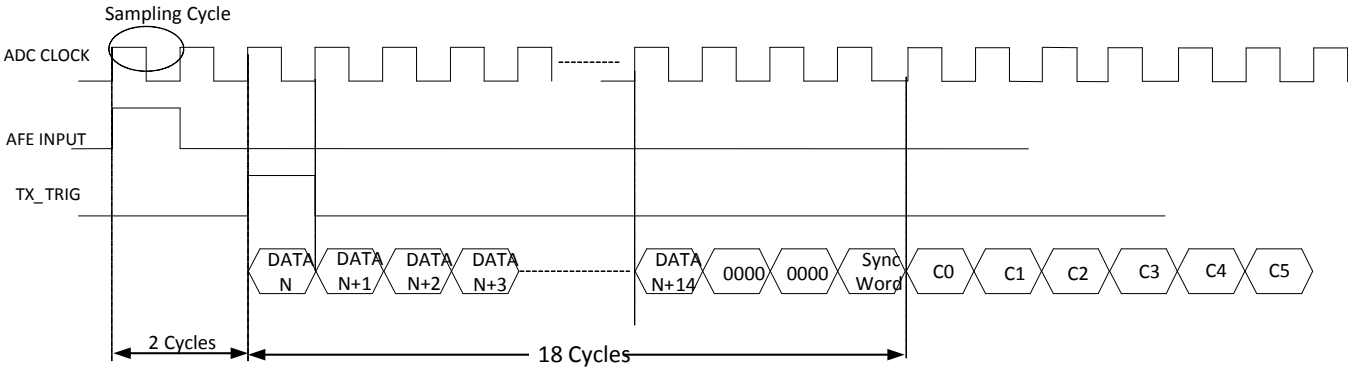


Figure 72. Measured Latency Timing when M=1

By adjusting the timing between AFE input and TX_TRIG, we can obtain a timing diagram similar as Figure 72

When M = 2, if impulse is given one clock before TX_TRIG signal, then sample followed after SYNC WORD gives impulse response of the filter as shown in Figure 73.

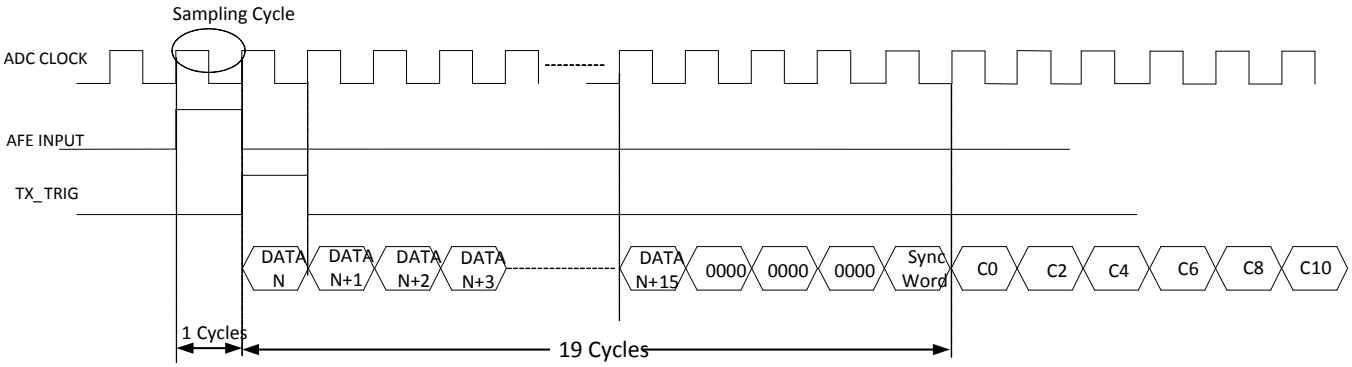


Figure 73. Measured Latency Timing when M=2

A generic timing diagram is shown below. Here number of zeros comes before sync word is equals to Z. Sync word comes after S number of cycles, impulse response starts coming after L number of cycles, and input impulse is given after IP cycles with respect to TX_TRIG signal. Therefore for different decimation factor (M), values of these numbers are listed down in Table 23 andFigure 74.

Table 23. Generic Latency vs. Decimation factor M

M	No of Zeros (ZNo)	Sync Word Latency (S)	Data Latency (L)	Input Impulse (IP)
1	2	17	18	-2
2	3	18	19	-1
3	4	19	20	0
4	5	20	21	1
5	6	21	22	2
6	7	22	23	3
7	8	23	24	4
8	9	24	25	5
M	M+1	16+M	17+M	M-3
Notes	• Negative number represents input is given in advance with respect to TX_TRIG signal. • When DC_REMOVAL_BYPASS 10[0] = 0 or 0xA[0]=0, the Sync word Latency and Data Latency becomes 17+M and 18+M • ADC's low latency mode enabled by Reg. 0x2[12] doesn't impact S and L.			

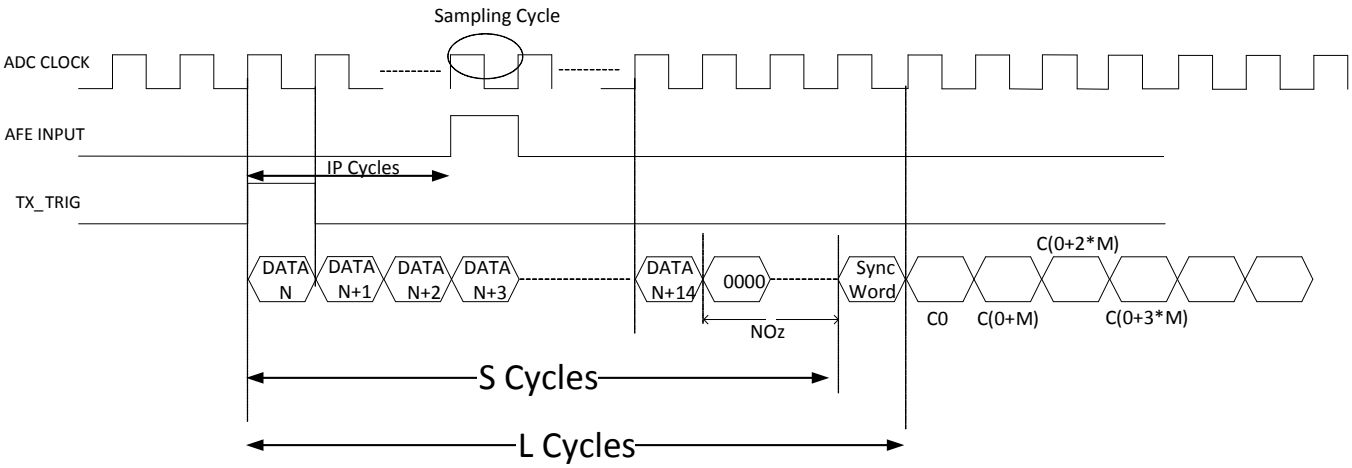


Figure 74. Measured Latency Timing at any M

Expression of Decimation Filter Response

Based on the above table, the decimation filter's response is formulated. Fig.5 indicates that the Tx_Trig sample is considered as the reference for time scale. So the input to the device at Tx_Trig clock shall be expressed as X[0], the next sample input as X[1] and so on. Similarly the output of device followed by the AFE5809's demodulator shall be expressed as Y[0] at the instant of Tx_Trig, Y[1] at the next clock and so on; Cn or C(n) indicates the coefficient of nth index.

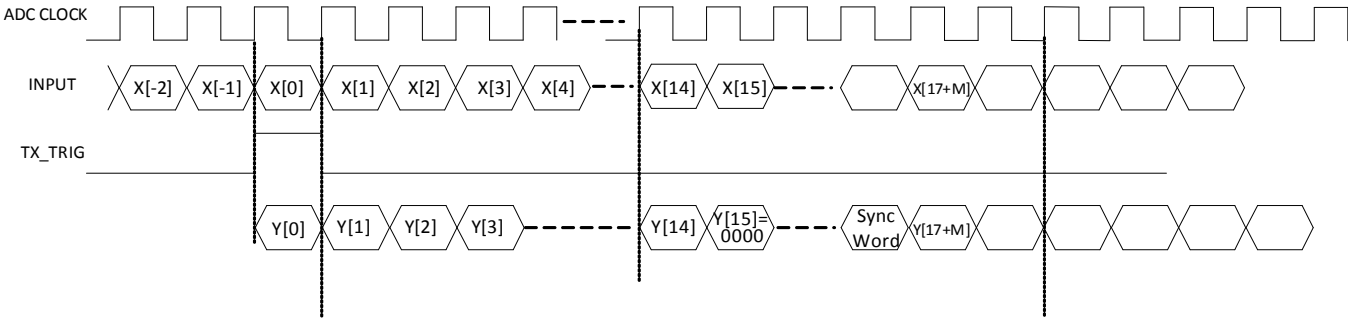


Figure 75. Typical Timing Expression among ADC CLK, Input, TX_TRIG and Output.

For M=1, the number of zeroes, ZNo=2 ; Sync Word Latency S= 17. So the output values from sample 18 will be relevant and the first few samples are:

$$Y[18] = C0 \times X[-2] + C1 \times X[-3] + C2 \times X[-4] + \ldots + C7 \times X[-9] + C7 \times X[-10] + \ldots + C[0] \times X[-17]$$
$$Y[19] = C0 \times X[-1] + C1 \times X[-2] + C2 \times X[-3] + \ldots + C7 \times X[-8] + C7 \times X[-9] + \ldots + C[0] \times X[-16]$$
$$Y[20] = C0 \times X[0] + C1 \times X[-1] + C2 \times X[-2] + \ldots + C7 \times X[-7] + C7 \times X[-8] + \ldots + C[0] \times X[-15]$$
$$\ldots \quad (5)$$

All these samples appear at the output since no samples are dropped for decimation factor = 1.

For M=2, the number of zeroes, ZNo=3 ; Sync Word Latency S = 18. So the output values from sample 19 will be relevant and the first few samples are described here:

$$Y[18] = C0 \times X[-2] + C1 \times X[-3] + C2 \times X[-4] + \ldots + C7 \times X[-9] + C7 \times X[-10] + \ldots + C[0] \times X[-17]$$
$$Y[19] = C0 \times X[-1] + C1 \times X[-2] + C2 \times X[-3] + \ldots + C7 \times X[-8] + C7 \times X[-9] + \ldots + C[0] \times X[-16]$$
$$Y[20] = C0 \times X[0] + C1 \times X[-1] + C2 \times X[-2] + \ldots + C7 \times X[-7] + C7 \times X[-8] + \ldots + C[0] \times X[-15]$$
$$\ldots \quad (6)$$

But for M=2, every alternate sample has to be dropped. The decimation is adjusted in such a way that the first sample after sync is retained. Hence in this case Y[19], Y[21], Y[23] etc… are retained and Y[20], Y[22], Y[24] are dropped.

For M=3,the number of zeroes, ZNo=4 ; Sync Word Latency S = 19. So the output values from sample 20 will be relevant and the first few samples are described here:

$$Y[18] = C0 \times X[-2] + C1 \times X[-3] + C2 \times X[-4] + \ldots + C7 \times X[-9] + C7 \times X[-10] + \ldots + C[0] \times X[-17]$$
$$Y[19] = C0 \times X[-1] + C1 \times X[-2] + C2 \times X[-3] + \ldots + C7 \times X[-8] + C7 \times X[-9] + \ldots + C[0] \times X[-16]$$
$$Y[20] = C0 \times X[0] + C1 \times X[-1] + C2 \times X[-2] + \ldots + C7 \times X[-7] + C7 \times X[-8] + \ldots + C[0] \times X[-15]$$
$$\ldots \quad (7)$$

But for M=3, every two among three samples have to be dropped. The decimation is adjusted in such a way that the first sample after sync is retained. Hence in this case Y[20], Y[23], Y[26] etc… are retained and Y[21], Y[22], Y[24], Y[25] etc… are dropped.

For any M,This pattern can be generalized for a decimation factor of M. The number of ZNo=M+1, Sync Word Latency S = 16+M. So the output values from sample (17+M) will be relevant and the first few samples are described here:

$$Y[18] = C0 \times X[-2] + C1 \times X[-3] + C2 \times X[-4] + \ldots + C7 \times X[-9] + C7 \times X[-10] + \ldots + C[0] \times X[-17]$$

$$Y[19] = C0 \times X[-1] + C1 \times X[-2] + C2 \times X[-3] + \ldots + C7 \times X[-8] + C7 \times X[-9] + \ldots + C[0] \times X[-16]$$

$$Y[20] = C0 \times X[0] + C1 \times X[-1] + C2 \times X[-2] + \ldots + C7 \times X[-7] + C7 \times X[-8] + \ldots + C[0] \times X[-15]$$

... (8)

For a decimation factor of M which is not 1, the decimation is adjusted in such a way that the first sample after sync is retained. Hence in this case Y[17+M], Y[17+2M], Y[17+3M] etc… are retained and the rest of samples between these i.e. Y[18+M], Y[19+2M],…, Y[16+2M] are dropped.

THEORY OF OPERATION

AFE5809 OVERVIEW

The AFE5809 is a highly integrated Analog Front-End (AFE) solution specifically designed for ultrasound systems in which high performance and small size are required. The AFE5809 integrates a complete time-gain-control (TGC) imaging path and a continuous wave Doppler (CWD) path. It also enables users to select one of various power/noise combinations to optimize system performance. The AFE5809 contains eight channels; each channels includes a Low-Noise Amplifier (LNA), a Voltage Controlled Attenuator (VCAT), a Programmable Gain Amplifier (PGA), a Low-pass Filter (LPF), a 14-bit Analog-to-Digital Converter (ADC), a digital I/Q demodulator, and a CW mixer.

Multiple features in the AFE5809 are suitable for ultrasound applications, such as active termination, individual channel control, fast power up/down response, programmable clamp voltage control, fast and consistent overload recovery, and so on. Therefore, the AFE5809 brings premium image quality to ultraportable, handheld systems all the way up to high-end ultrasound systems.

In addition, the signal chain of the AFE5809 can handle signal frequency as low as 50KHz and as high as 30 MHz. This enables the AFE5809 to be used in both sonar and medical applications.

The simplified function block diagram is shown in Figure 76.

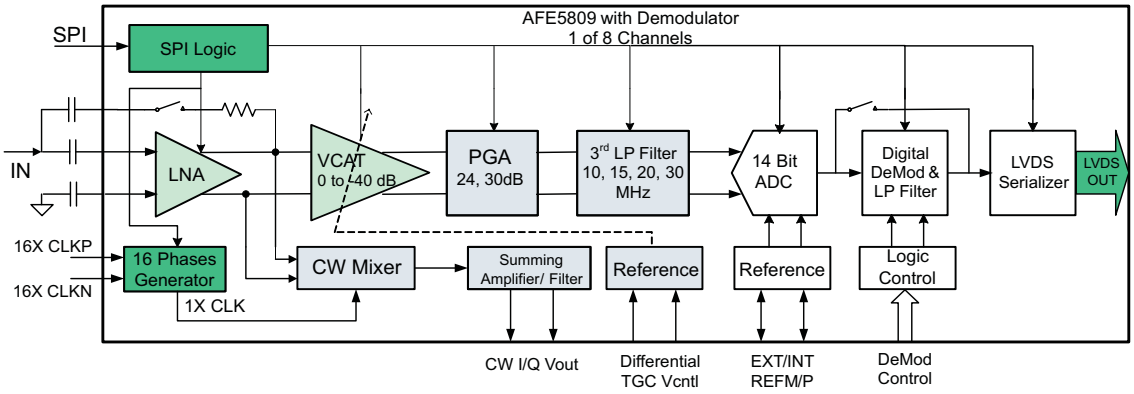


Figure 76. Functional Block Diagram

LOW-NOISE AMPLIFIER (LNA)

In many high-gain systems, a low noise amplifier is critical to achieve overall performance. Using a new proprietary architecture, the LNA in the AFE5809 delivers exceptional low-noise performance, while operating on a low quiescent current compared to CMOS-based architectures with similar noise performance. The LNA performs single-ended input to differential output voltage conversion. It is configurable for a programmable gain of 24, 18. 12 dB and its input-referred noise is only 0.63, 0.70, 0.9nV/√Hz respectively. Programmable gain settings result in a flexible linear input range up to 1 Vpp, realizing high signal handling capability demanded by new transducer technologies. Larger input signal can be accepted by the LNA; however the signal can be distorted since it exceeds the LNA's linear operation region. Combining the low noise and high input range, a wide input dynamic range is achieved consequently for supporting the high demands from various ultrasound imaging modes.

The LNA input is internally biased at approximately +2.4 V; the signal source should be ac-coupled to the LNA input by an adequately-sized capacitor, e.g. ≥ 0.1µF. To achieve low DC offset drift, the AFE5809 incorporates a DC offset correction circuit for each amplifier stage. To improve the overload recovery, an integrator circuit is used to extract the DC component of the LNA output and then fed back to the LNA's complementary input for DC offset correction. This DC offset correction circuit has a high-pass response and can be treated as a high-pass filter. The effective corner frequency is determined by the capacitor C_{BYPASS} connected at INM. With larger capacitors, the corner frequency is lower. For stable operation at the highest HP filer cut-off frequency, a ≥ 15 nF

capacitor can be selected. This corner frequency scales almost linearly with the value of the C_{BYPASS}. For example, 15 nF gives a corner frequency of approximately 100 kHz, while 47 nF can give an effective corner frequency of 33 KHz. The DC offset correction circuit can also be disabled/enabled through register 52[12]. A large capacitor like 1 µF can be used for setting low corner frequency (<2 KHz) of the LNA DC offset correction circuit. Figure 60 shows the frequency responses for low frequency applicaitons.

The AFE5809 can be terminated passively or actively. Active termination is preferred in ultrasound application for reducing reflection from mismatches and achieving better axial resolution without degrading noise figure too much. Active termination values can be preset to 50, 100, 200, 400 Ω; other values also can be programmed by users through register 52[4:0]. A feedback capacitor is required between ACTx and the signal source as Figure 77 shows. On the active termination path, a clamping circuit is also used to create a low impedance path when overload signal is seen by the AFE5809. The clamp circuit limits large input signals at the LNA inputs and improves the overload recovery performance of the AFE5809. The clamp level can be set to 350mVpp, 600 mVpp, 1.15 Vpp automatically depending on the LNA gain settings when register 52[10:9]=0. Other clamp voltages, such as 1.15 Vpp, 0.6 Vpp, and 1.5 Vpp, are also achievable by setting register 52[10:9]. This clamping circuit is also designed to obtain good pulse inversion performance and reduce the impact from asymmetric inputs.

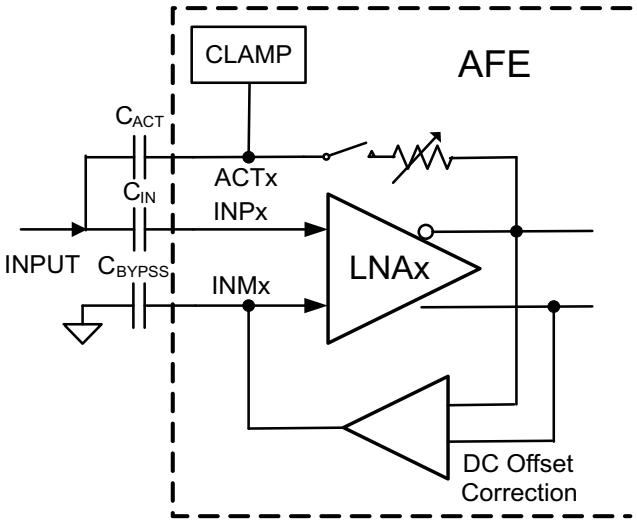


Figure 77. AFE5809 LNA with DC Offset Correction Circuit

VOLTAGE-CONTROLLED ATTENUATOR

The voltage-controlled attenuator is designed to have a linear-in-dB attenuation characteristic; that is, the average gain loss in dB (refer to Figure 3) is constant for each equal increment of the control voltage (VCNTL) as shown in Figure 78. A differential control structure is used to reduce common mode noise. A simplified attenuator structure is shown in the following Figure 78 and Figure 79.

The attenuator is essentially a variable voltage divider that consists of the series input resistor (RS) and seven shunt FETs placed in parallel and controlled by sequentially activated clipping amplifiers (A1 through A7). VCNTL is the effective difference between VCNTLP and VCNTLM. Each clipping amplifier can be understood as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltage. Reference voltages V1 through V7 are equally spaced over the 0V to 1.5Vcontrol voltage range. As the control voltage increases through the input range of each clipping amplifier, the amplifier output rises from a voltage where the FET is nearly OFF to VHIGH where the FET is completely ON. As each FET approaches its ON state and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic. Thus, low control voltages have most of the FETs turned OFF, producing minimum signal attenuation. Similarly, high control voltages turn the FETs ON, leading to maximum signal attenuation. Therefore, each FET acts to decrease the shunt resistance of the voltage divider formed by Rs and the parallel FET network.

Additionally, a digitally controlled TGC mode is implemented to achieve better phase-noise performance in the AFE5809. The attenuator can be controlled digitally instead of the analog control voltage V_{CNTL}. This mode can be set by the register bit 59[7]. The variable voltage divider is implemented as a fixed series resistance and FET as the shunt resistance. Each FET can be turned ON by connecting the switches SW1-7. Turning on each of the switches can give approximately 6 dB of attenuation. This can be controlled by the register bits 59[6:4]. This digital control feature can eliminate the noise from the V_{CNTL} circuit and ensure the better SNR and phase noise for the TGC path.

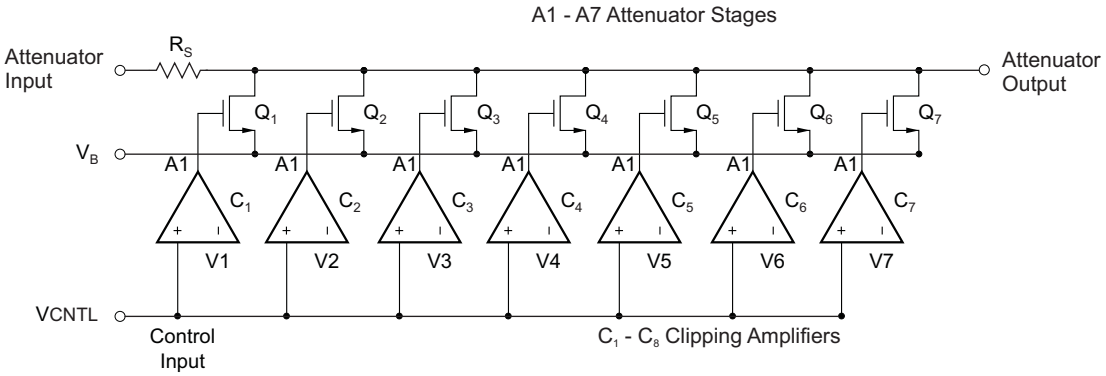


Figure 78. Simplified Voltage Controlled Attenuator (Analog Structure)

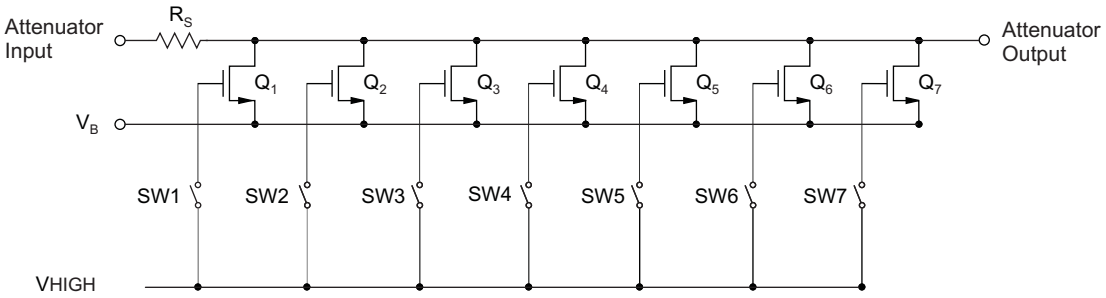


Figure 79. Simplified Voltage Controlled Attenuator (Digital Structure)

The voltage controlled attenuator's noise follows a monotonic relationship to the attenuation coefficient. AAt higher attenuation, the input-referred noise is higher and vice-versa. The attenuator's noise is then amplified by the PGA and becomes the noise floor at ADC input. In the attenuator's high attenuation operating range, that is V_{CNTL} is high, the attenuator's input noise may exceed the LNA output noise; the attenuator then becomes the dominant noise source for the following PGA stage and ADC. Therefore, the attenuator noise should be minimized compared to the LNA output noise. The AFE5809 attenuator is designed for achieving very low noise even at high attenuation (low channel gain) and realizing better SNR in near field. The input referred noise for different attenuations is listed in Table 24:

Table 24. Voltage-Controlled-Attenuator Noise vs Attenuation

Attenuation (dB)	Attenuator Input Referred noise (nV/rtHz)
–40	10.5
–36	10
–30	9
–24	8.5
–18	6
–12	4
–6	3
0	2

PROGRAMMABLE GAIN AMPLIFIER (PGA)

After the voltage controlled attenuator, a programmable gain amplifier can be configured as 24dB or 30dB with a constant input referred noise of 1.75 nV/rtHz. The PGA structure consists of a differential voltage-to-current converter with programmable gain, clamping circuits, a transimpedance amplifier with a programmable low-pass filter, and a DC offset correction circuit. Its simplified block diagram is shown in Figure 80.

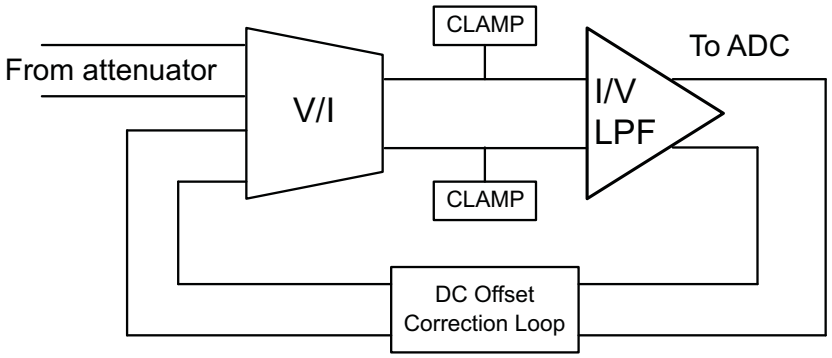


Figure 80. Simplified Block Diagram of PGA

Low input noise is always preferred in a PGA and its noise contribution should not degrade the ADC SNR too much after the attenuator. At the minimum attenuation (used for small input signals), the LNA noise dominates; at the maximum attenuation (large input signals), the PGA and ADC noise dominates. Thus 24 dB gain of PGA achieves better SNR as long as the amplified signals can exceed the noise floor of the ADC.

The PGA clamping circuit can be enabled (register 51) to improve the overload recovery performance of the AFE. If we measure the standard deviation of the output just after overload, for 0.5 V V_{CNTL}, it is about 3.2 LSBs in normal case, i.e the output is stable in about 1 clock cycle after overload. With the clamp disabled, the value approaches 4 LSBs meaning a longer time duration before the output stabilizes; however, with the clamp enabled, there will be degradation in HD3 for PGA output levels > -2dBFS. For example, for a –2 dBFS output level, the HD3 degrades by approximately 3dB. In order to maximize the output dynamic range, the maximum PGA output level can be above 2Vpp even with the clamp circuit enabled; the ADC in the AFE5809 has excellent overload recovery performance to detect small signals right after the overload.

NOTE

In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0

The AFE5809 integrates an anti-aliasing filter in the form of a programmable low-pass filter (LPF) in the transimpedance amplifier. The LPF is designed as a differential, active, 3rd order filter with Butterworth characteristics and a typical 18dB per octave roll-off. Programmable through the serial interface, the –1 dB frequency corner can be set to one of 10MHz, 15MHz, 20MHz, and 30MHz. The filter bandwidth is set for all channels simultaneously.

A selectable DC offset correction circuit is implemented in the PGA as well. This correction circuit is similar to the one used in the LNA. It extracts the DC component of the PGA outputs and feeds back to the PGA complimentary inputs for DC offset correction. This DC offset correction circuit also has a high-pass response with a cut-off frequency of 80 KHz.

ANALOG TO DIGITAL CONVERTER

The analog-to-digital converter (ADC) of the AFE5809 employs a pipelined converter architecture that consists of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 14-bit level. The 14 bits given out by each channel are serialized and sent out on a single pair of pins in LVDS format. All eight channels of the AFE5809 operate from a common input clock (CLKP/M). The sampling clocks for each of the eight channels are generated from the input clock using a carefully matched clock buffer tree. The 14x clock required for the

serializer is generated internally from the CLKP/M pins. A 7x and a 1x clock are also given out in LVDS format, along with the data, to enable easy data capture. The AFE5809 operates from internally-generated reference voltages that are trimmed to improve the gain matching across devices. The nominal values of REFP and REFM are 1.5 V and 0.5 V, respectively. Alternately, the device also supports an external reference mode that can be enabled using the serial interface.

Using serialized LVDS transmission has multiple advantages, such as a reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital noise coupling to the analog circuit inside the AFE5809.

CONTINUOUS-WAVE (CW) BEAMFORMER

Continuous-wave Doppler is a key function in mid-end to high-end ultrasound systems. Compared to the TGC mode, the CW path needs to handle high dynamic range along with strict phase noise performance. CW beamforming is often implemented in analog domain due to the mentioned strict requirements. Multiple beamforming methods are being implemented in ultrasound systems, including passive delay line, active mixer, and passive mixer. Among all of them, the passive mixer approach achieves optimized power and noise. It satisfies the CW processing requirements, such as wide dynamic range, low phase noise, accurate gain and phase matching.

A simplified CW path block diagram and an In-phase or Quadrature (I/Q) channel block diagram are illustrated below respectively. Each CW channel includes a LNA, a voltage-to-current converter, a switch-based mixer, a shared summing amplifier with a low-pass filter, and clocking circuits.

NOTE

The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH respectively. Depending on users' CW Doppler complex FFT processing, swapping I/Q channels in FPGA or DSP may be needed in order to get correct blood flow directions.

All blocks include well-matched in-phase and quadrature channels to achieve good image frequency rejection as well as beamforming accuracy. As a result, the image rejection ratio from an I/Q channel is better than -46 dBc which is desired in ultrasound systems.

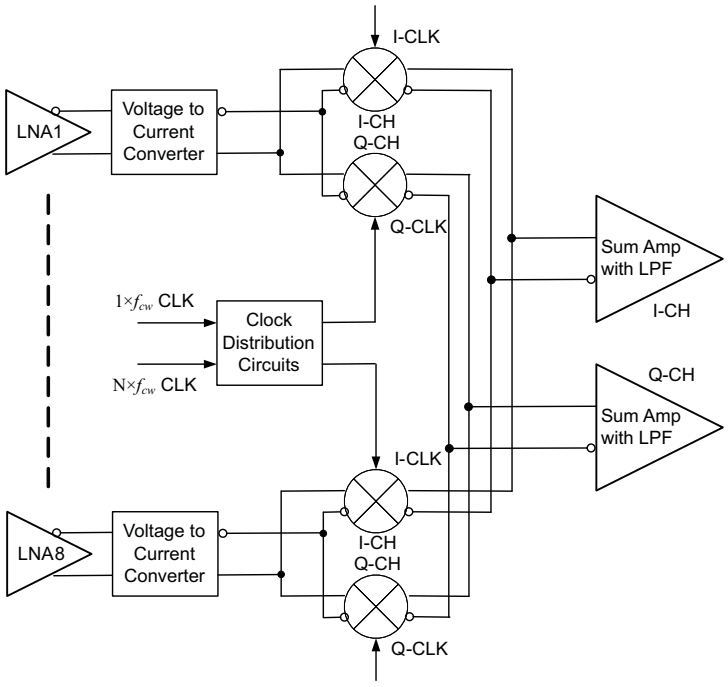
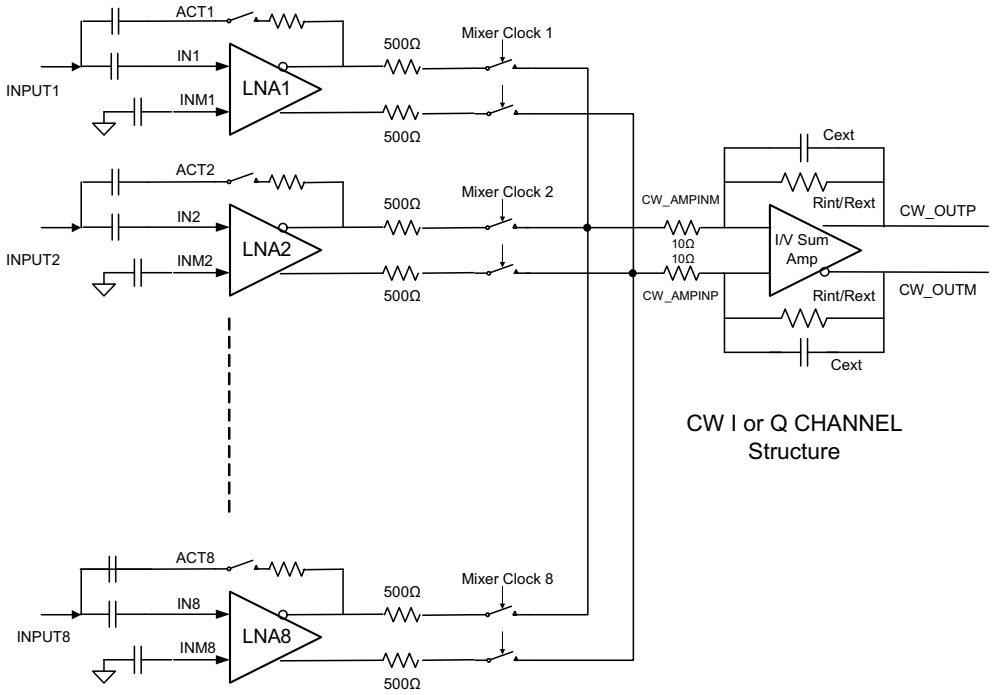


Figure 81. Simplified Block Diagram of CW Path



Note: the 10~15Ω resistors at CW_AMPINM/P are due to internal IC routing and can create slight attenuation.

Figure 82. A Complete In-phase or Quadrature Phase Channel

The CW mixer in the AFE5809 is passive and switch based; passive mixer adds less noise than active mixers. It achieves good performance at low power. Figure 83 and the equations describe the principles of mixer operation, where Vi(t), Vo(t) and LO(t) are input, output and local oscillator (LO) signals for a mixer respectively. The LO(t) is square-wave based and includes odd harmonic components as shown in Equation 9:

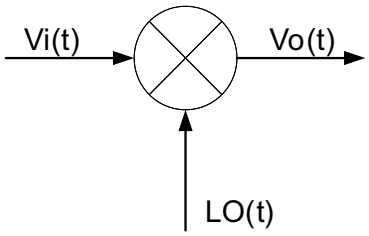


Figure 83. Block Diagram of Mixer Operation

$$Vi(t) = \sin\left(\omega_0 t + \omega_d t + \varphi\right) + f\left(\omega_0 t\right)$$

$$LO(t) = \frac{4}{\pi}\left[\sin\left(\omega_0 t\right) + \frac{1}{3}\sin\left(3\omega_0 t\right) + \frac{1}{5}\sin\left(5\omega_0 t\right)...\right]$$

$$Vo(t) = \frac{2}{\pi}\left[\cos\left(\omega_d t + \phi\right) - \cos\left(2\omega_0 t - \omega_d t + \phi\right)...\right] \quad (9)$$

From the above equations, the 3rd and 5th order harmonics from the LO can interface with the 3rd and 5th order harmonic signals in the Vi(t); or the noise around the 3rd and 5th order harmonics in the Vi(t). Therefore. the mixer's performance is degraded. In order to eliminate this side effect due to the square-wave demodulation, a proprietary harmonic suppression circuit is implemented in the AFE5809. The 3rd and 5th harmonic components from the LO can be suppressed by over 12 dB. Thus the LNA output noise around the 3rd and 5th order harmonic bands will not be down-converted to base band. Hence, better noise figure is achieved. The conversion loss of the mixer is about -4 dB which is derived from $20\log_{10}\frac{2}{\pi}$

The mixed current outputs of the 8 channels are summed together internally. An internal low noise operational amplifier is used to convert the summed current to a voltage output. The internal summing amplifier is designed to accomplish low power consumption, low noise, and ease of use. CW outputs from multiple AFE5809s can be further combined on system board to implement a CW beamformer with more than 8 channels. More detail information can be found in the application information section.

Multiple clock options are supported in the AFE5809 CW path. Two CW clock inputs are required: N × f_{cw} clock and 1 × f_{cw} clock, where f_{cw} is the CW transmitting frequency and N could be 16, 8, 4, or 1. Users have the flexibility to select the most convenient system clock solution for the AFE5809. In the 16 × f_{cw} and 8 × $f$cw modes, the 3rd and 5th harmonic suppression feature can be supported. Thus the 16 × f_{cw} and 8 × f_{cw} modes achieves better performance than the 4 × f_{cw} and 1 × f_{cw} modes

16 × f_{cw} Mode

The 16 × f_{cw} mode achieves the best phase accuracy compared to other modes. It is the default mode for CW operation. In this mode, 16 × f_{cw} and 1 × f_{cw} clocks are required. 16×fcw generates LO signals with 16 accurate phases. Multiple AFE5809s can be synchronized by the 1 × f_{cw} , that is LO signals in multiple AFEs can have the same starting phase. The phase noise spec is critical only for 16X clock. 1X clock is for synchronization only and doesn't require low phase noise. Please see the phase noise requirement in the section of application information.

The top level clock distribution diagram is shown in the below Figure 84. Each mixer's clock is distributed through a 16 × 8 cross-point switch. The inputs of the cross-point switch are 16 different phases of the 1x clock. It is recommended to align the rising edges of the 1 x f_{cw} and 16 x f_{cw} clocks.

The cross-point switch distributes the clocks with appropriate phase delay to each mixer. For example, Vi(t) is a received signal with a delay of $\frac{1}{16}T$, a delayed LO(t) should be applied to the mixer in order to compensate for the $\frac{1}{16}T$ delay. Thus a 22.5º delayed clock, that is $\frac{2\pi}{16}$, is selected for this channel. The mathematic calculation is expressed in the following equations:

$$\mathrm{Vi}(t)=\sin\left[\omega_0\left(t+\frac{1}{16f_0}\right)+\omega_d t\right]=\sin\left[\omega_0 t+22.5^\circ+\omega_d t\right]$$

$$\mathrm{LO}(t)=\frac{4}{\pi}\sin\left[\omega_0\left(t+\frac{1}{16f_0}\right)\right]=\frac{4}{\pi}\sin\left[\omega_0 t+22.5^\circ\right]$$

$$\mathrm{Vo}(t)=\frac{2}{\pi}\cos\left(\omega_d t\right)+f\left(\omega_n t\right) \quad (10)$$

Vo(t) represents the demodulated Doppler signal of each channel. When the doppler signals from N channels are summed, the signal to noise ratio improves.

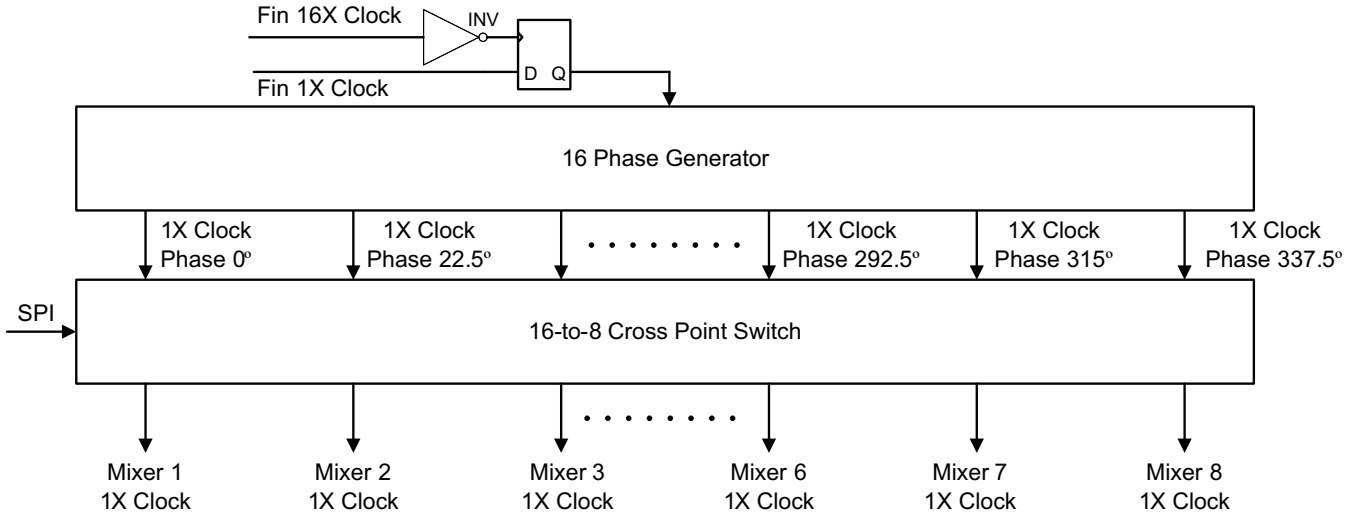


Figure 84.

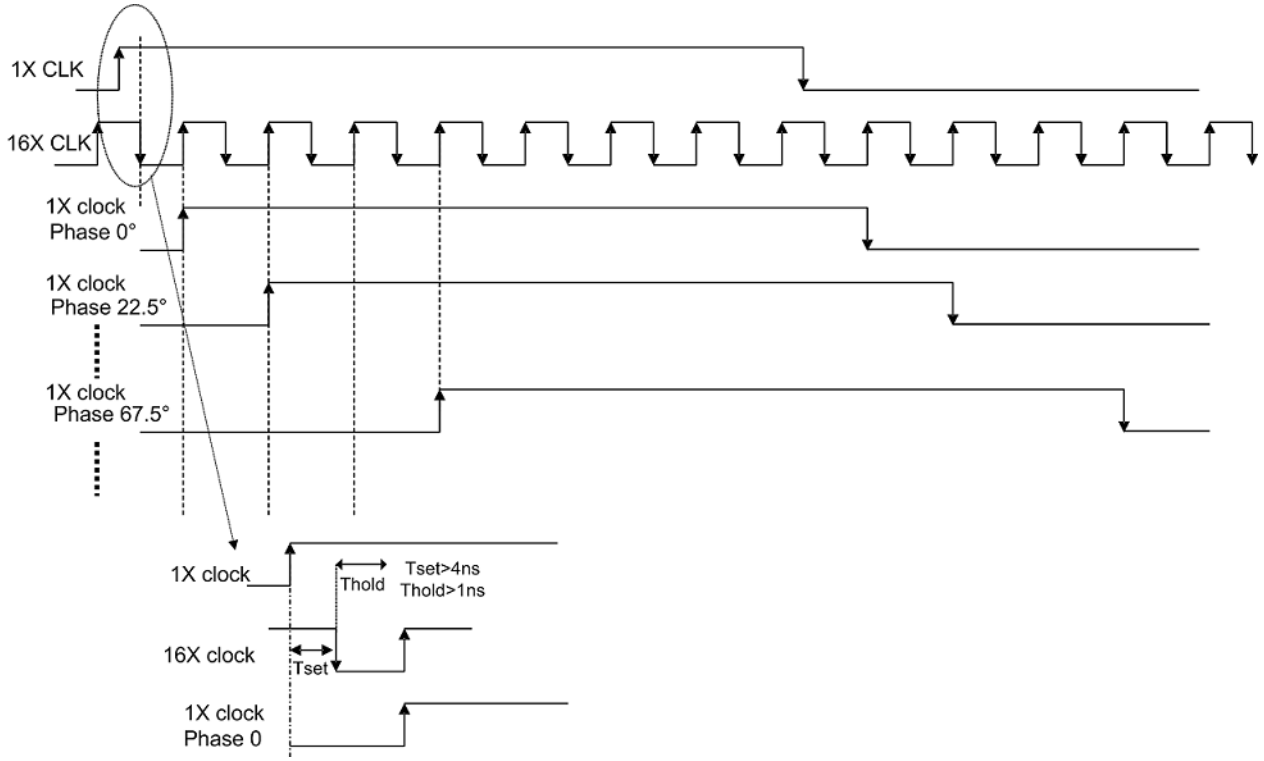


Figure 85. 1x and 16x CW Clock Timing

8 × f_{cw} and 4 × f_{cw} Modes

8 × f_{cw} and 4 × f_{cw} modes are alternative modes when higher frequency clock solution (that is 16 × f_{cw} clock) is not available in system. The block diagram of these two modes is shown below.

Good phase accuracy and matching are also maintained. Quadature clock generator is used to create in-phase and quadrature clocks with exact 90° phase difference. The only difference between 8 × f_{cw} and 4 × f_{cw} modes is the accessibility of the 3rd and 5th harmonic suppression filter. In the 8 × f_{cw} mode, the suppression filter can be supported. In both modes, $\frac{1}{16}T$ phase delay resolution is achieved by weighting the in-phase and quadrature paths correspondingly. For example, if a delay of $\frac{1}{16}T$ or 22.5° is targeted, the weighting coefficients should follow the below equations, assuming I_{in} and Q_{in} are sin($\omega_0 t$) and cos($\omega_0 t$) respectively:

$$I_{delayed}(t) = I_{in}\cos\left(\frac{2\pi}{16}\right) + Q_{in}\sin\left(\frac{2\pi}{16}\right) = I_{in}\left(t + \frac{1}{16f_0}\right)$$

$$Q_{delayed}(t) = Q_{in}\cos\left(\frac{2\pi}{16}\right) - I_{in}\sin\left(\frac{2\pi}{16}\right) = Q_{in}\left(t + \frac{1}{16f_0}\right) \quad (11)$$

Therefore, after I/Q mixers, phase delay in the received signals is compensated. The mixers' outputs from all channels are aligned and added linearly to improve the signal to noise ratio. It is preferred to have the 4 × f_{cw} or 8 × f_{cw} and 1 × f_{cw} clocks aligned both at the rising edge.

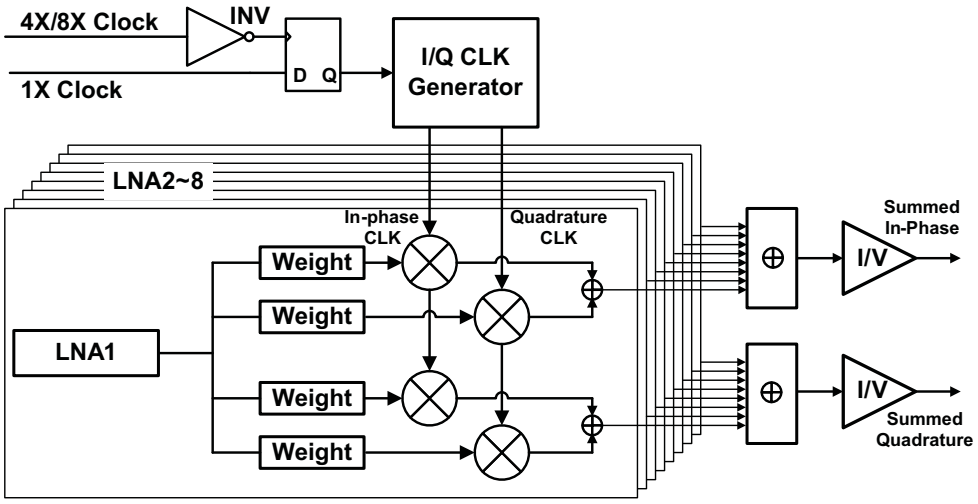


Figure 86. 8 X f_{cw} and 4 X f_{cw} Block Diagram

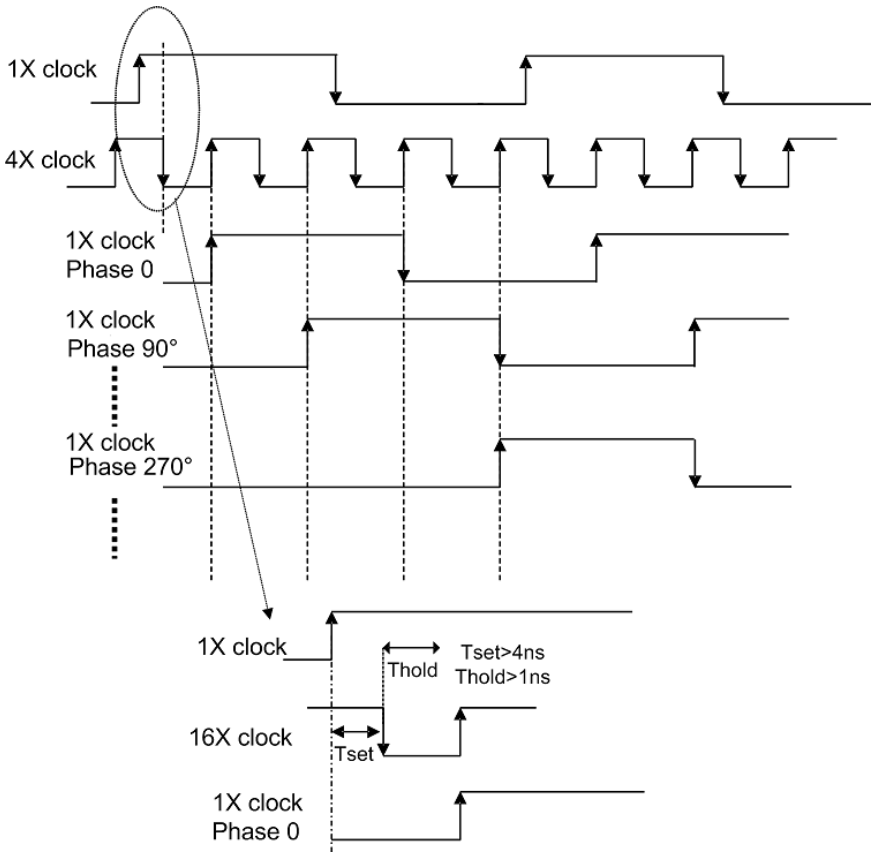


Figure 87. 8 x f_{cw} and 4 x f_{cw} Timing Diagram

1 × f_{cw} Mode

The 1x f_{cw} mode requires in-phase and quadrature clocks with low phase noise specifications. The $\frac{1}{16}T$ phase delay resolution is also achieved by weighting the in-phase and quadrature signals as described in the 8 × f_{cw} and 4 × f_{cw} modes.

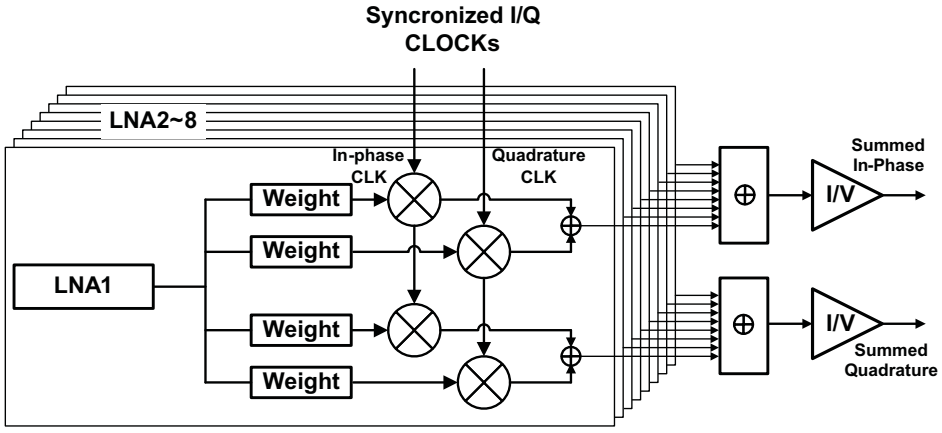


Figure 88. Block Diagram of 1 x f_{cw} mode

DIGITAL I/Q DEMODULATOR

AFE5809 also includes a digital in-phase and quadrature (I/Q) demodulator and a low-pass decimation filter. The main purpose of the demodulation block is to reduce the LVDS data rate and improve overall system power efficiency. The I/Q demodulator accepts ADC output with up to 65MSPS sampling rate and 14 bit resolution. For example, after digital demodulation and 4× decimation filtering, the data rate for either in-phase or quadrature output is reduced to 16.25MSPS, and the data resolution is improved to 16 bit consequently. Hence, the overall LVDS trace reduction can be a factor of 2. This demodulator can be bypassed and powered down completely if it is not needed.

The digital demodulator block given in AFE5809 is designed to do down-conversion followed by decimation. The top level block is divided into two exactly similar blocks: 1. Subchip0 2. Subchip1. Both sub-chips share 4 channels each that is sub-chip0 (ADC.1, ADC.2, ADC.3 and ADC.4) and sub-chip1 (ADC.5, ADC.6, ADC.7 and ADC.8).

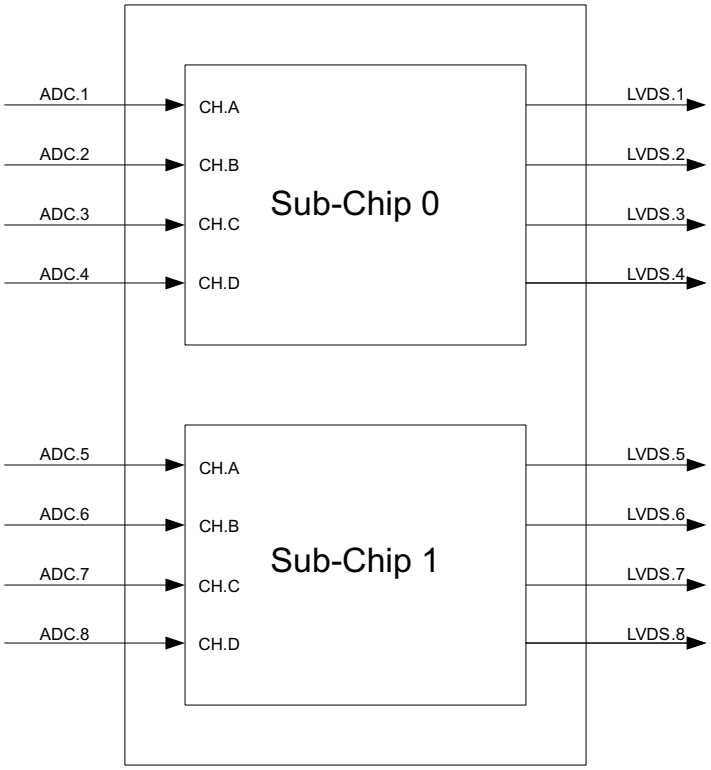


Figure 89. Sub-Chip

The following 4 functioning blocks are given in each demodulator. Every block can be bypassed.

1. DC Removal Block
2. Down Conversion
3. Decimator
4. Channel Multiplexing

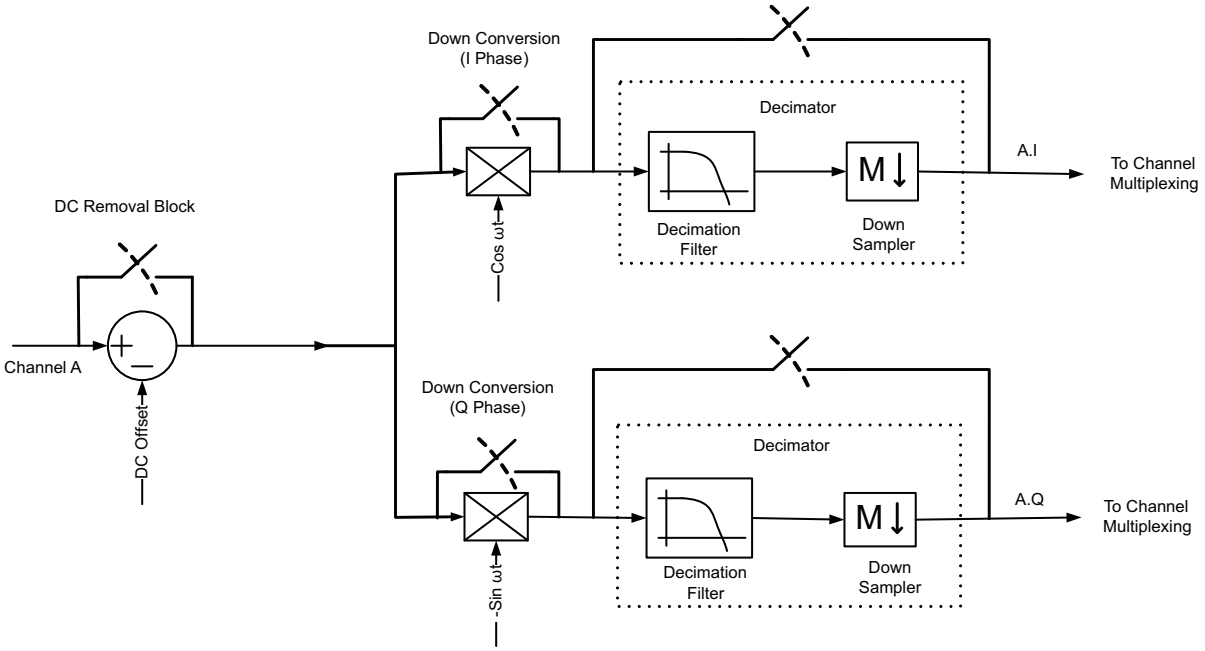


Figure 90. Digital Demodulator Block

1. DC Removal Block is used to remove DC offset. An offset value can be given to specific register.
2. Down Conversion or Demodulation of signal is done by multiplying signal by $\cos(\omega_0 t)$ and by $-\sin(\omega_0 t)$ to give out I phase and Q phase respectively. $\cos(\omega t)$ and $-\sin(\omega t)$ are 14-bit wide plus a sign bit. $\omega = 2\pi f$, f can be set with resolution Fs $/2^{16}$, where Fs is the ADC sampling frequency.

NOTE

The digital demodulator is based on a conventional down converter, that is, $-\sin(\omega_0 t)$ is used for Q phase.

3. Decimator Block has two functions, Decimation Filter and Down Sampler. Decimation Filter is a variable coefficient symmetric FIR filter and it's coefficients can be given using Coefficient RAM. Number of taps of FIR filter is 16 x decimation factor (M). For decimation factor of M, 8M coefficients have to be stored in Coefficient Bank. Each coefficient is 14 bit wide. Down-sampler gives out 1 sample followed by M-1 samples zeros.
4. In Figure 91, channel multiplexing is implemented for flexible data routing. :

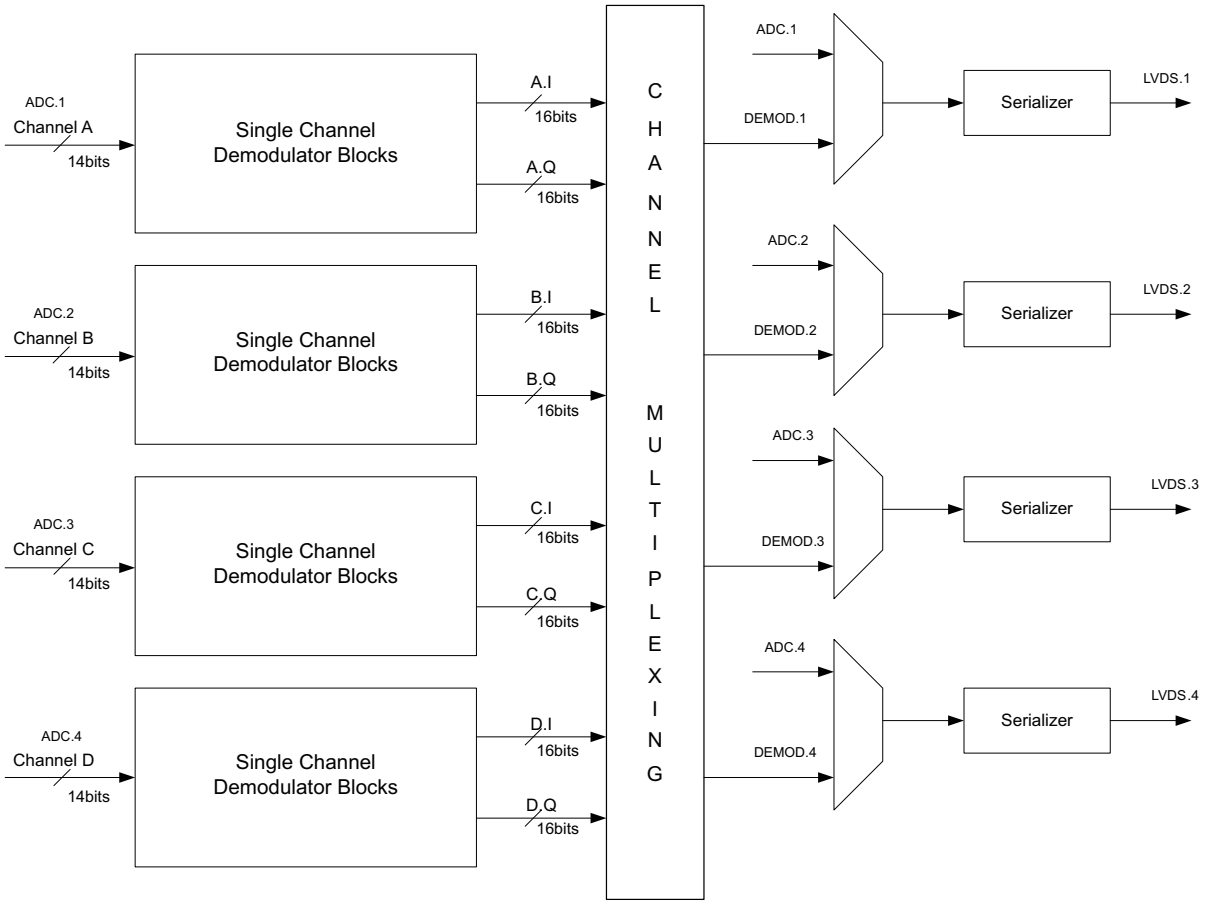


Figure 91. Channel Multiplexing

EQUIVALENT CIRCUITS

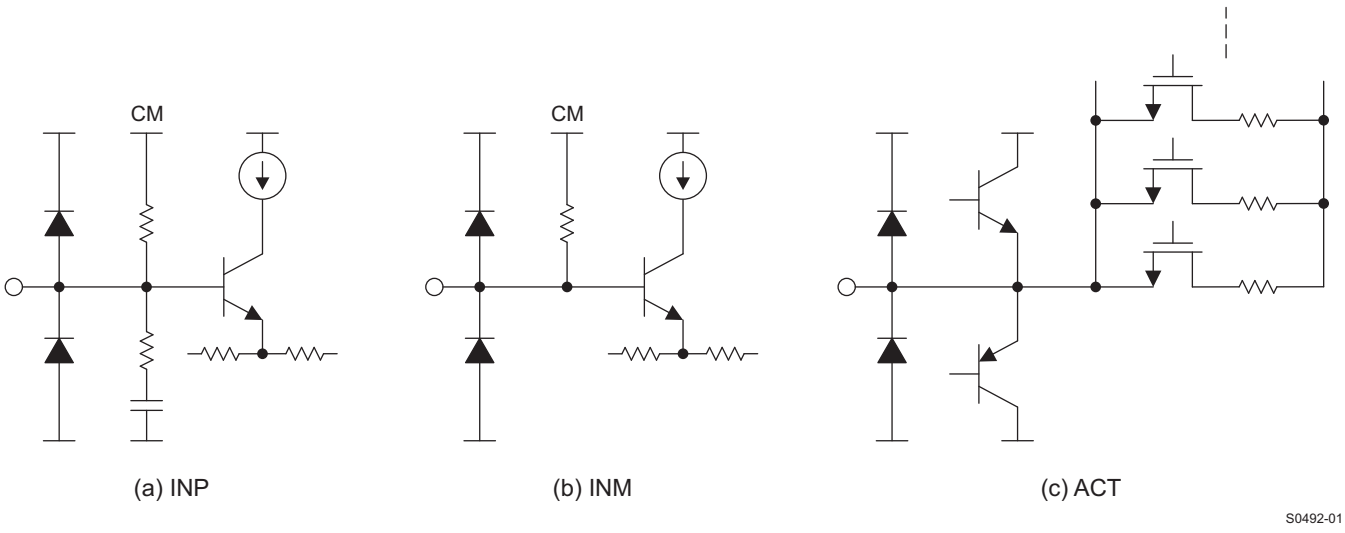


Figure 92. Equivalent Circuits of LNA inputs

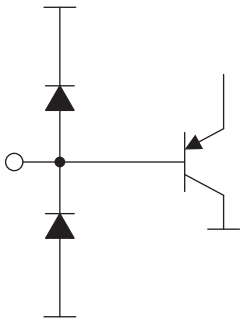


Figure 93. Equivalent Circuits of $V_{CNTLP/M}$

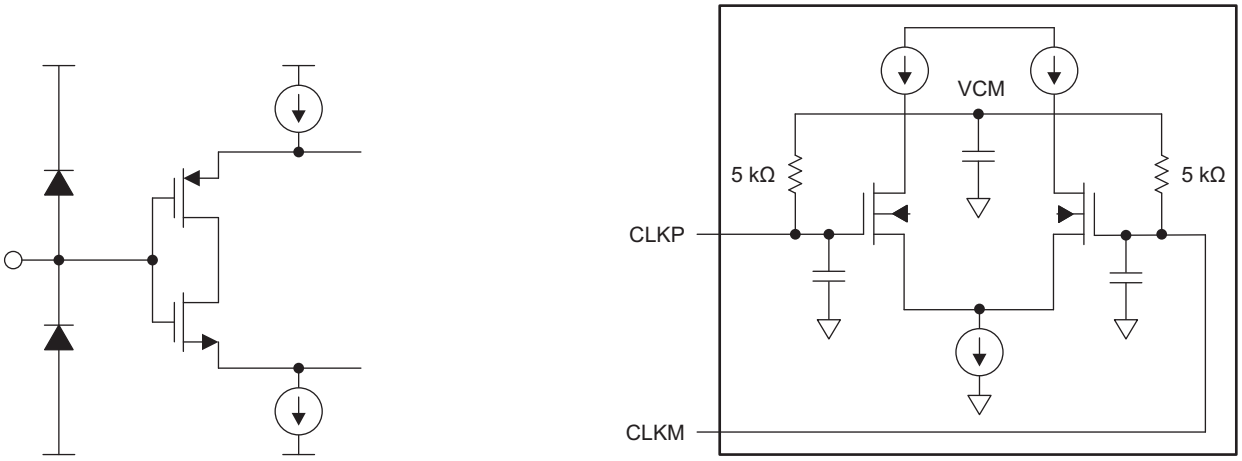


Figure 94. Equivalent Circuits of Clock Inputs

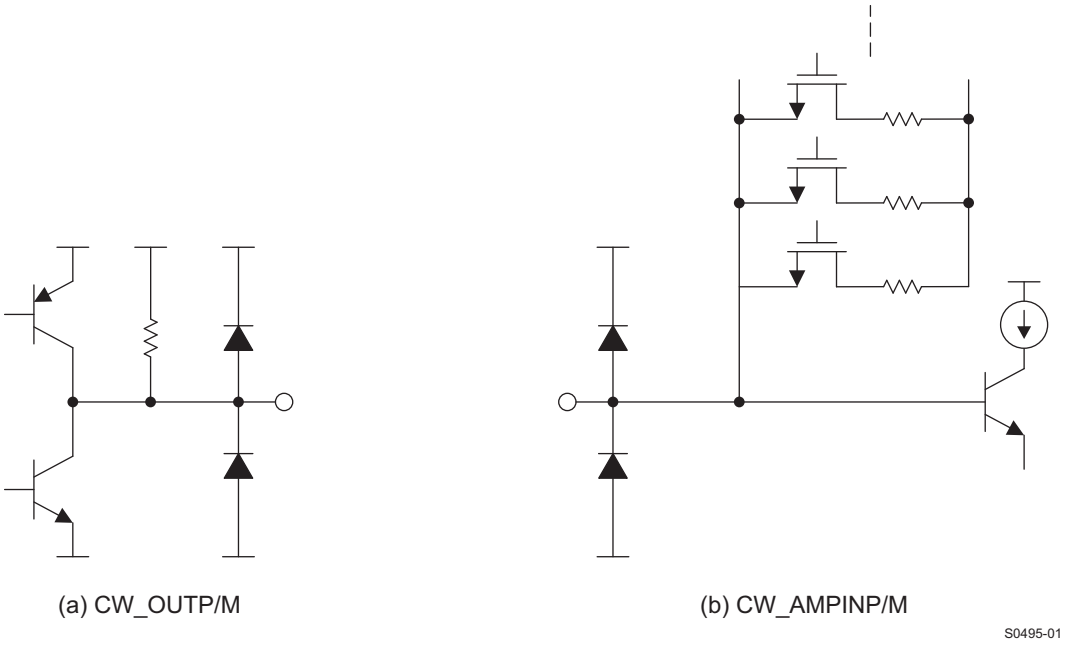


Figure 95. Equivalent Circuits of CW Summing Amplifier Inputs and Outputs

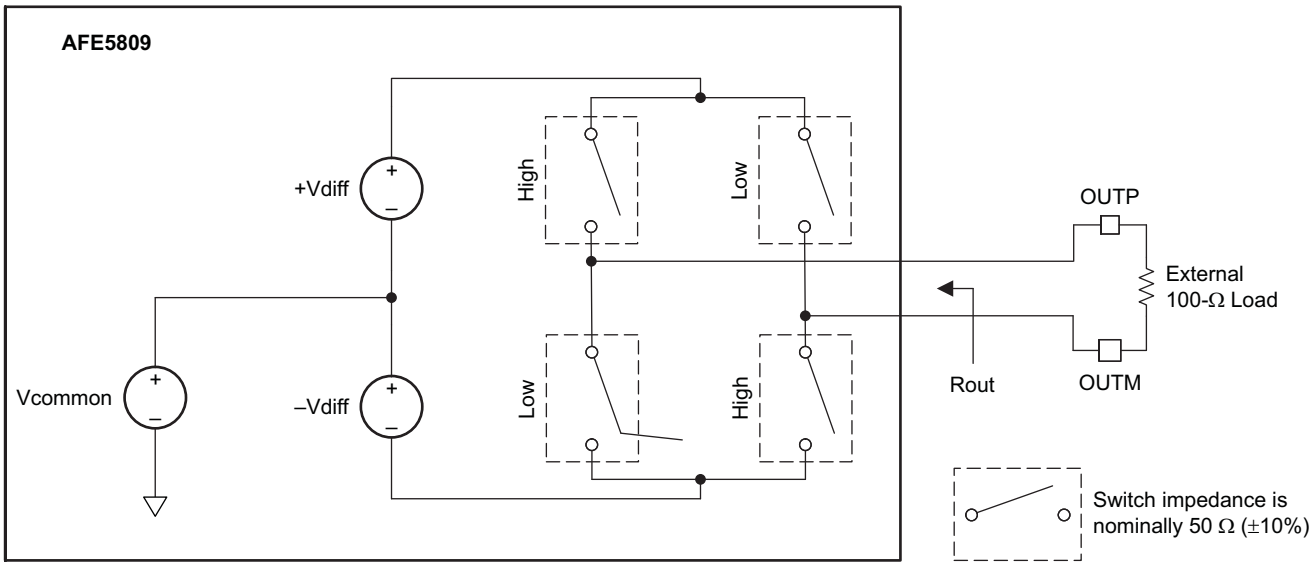


Figure 96. Equivalent Circuits of LVDS Outputs

APPLICATION INFORMATION

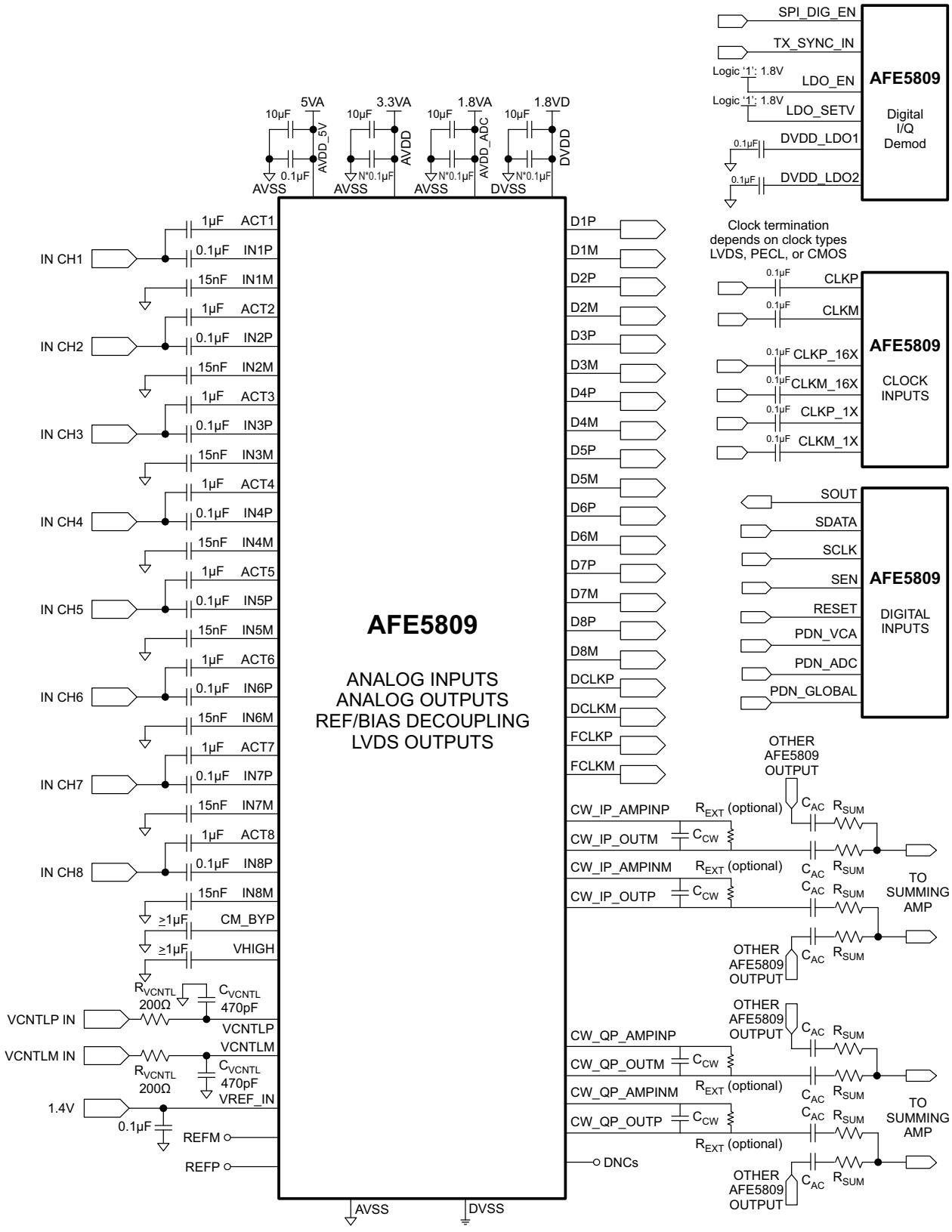


Figure 97. Application Circuit with Digital Demodulator

A typical application circuit diagram is listed in Figure 97. The configuration for each block is discussed below.

LNA CONFIGURATION

LNA Input Coupling and Decoupling

The LNA closed-loop architecture is internally compensated for maximum stability without the need of external compensation components. The LNA inputs are biased at 2.4 V and AC coupling is required. A typical input configuration is shown in Figure 98. C_{IN} is the input AC coupling capacitor. C_{ACT} is a part of the active termination feedback path. Even if the active termination is not used, the C_{ACT} is required for the clamp functionality. Recommended values for C_{ACT} is ≥ 1 µF and C_{IN} is ≥ 0.1 µF. A pair of clamping diodes is commonly placed between the T/R switch and the LNA input. Schottky diodes with suitable forward drop voltage (e.g. the BAT754/54 series, the BAS40 series, the MMBD7000 series, or similar) can be considered depending on the transducer echo amplitude.

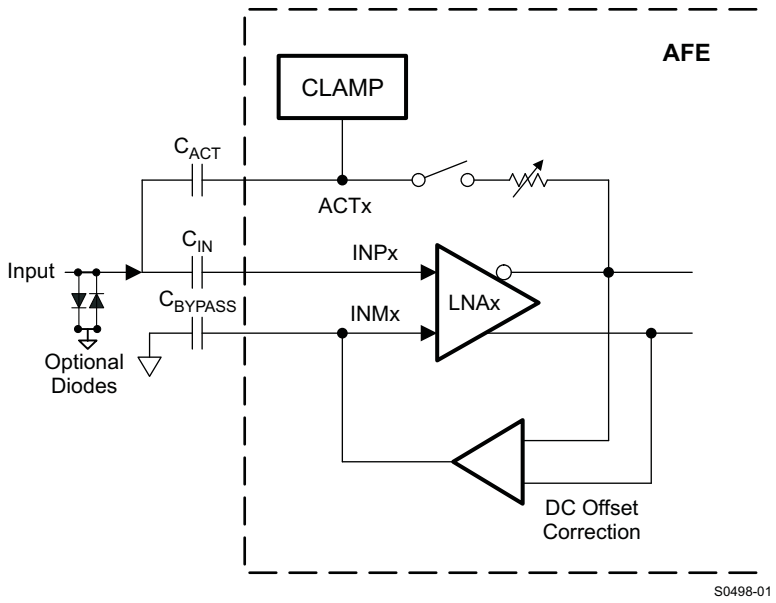


Figure 98. LNA Input Configurations

This architecture minimizes any loading of the signal source that may lead to a frequency-dependent voltage divider. The closed-loop design yields low offsets and offset drift. C_{BYPASS} (≥ 0.015 µF) is used to set the high-pass filter cut-off frequency and decouple the complimentary input. Its cut-off frequency is inversely proportional to the C_{BYPASS} value, The HPF cut-off frequency can be adjusted through the register 59[3:2] a Table 25 lists. Low frequency signals at T/R switch output, such as signals with slow ringing, can be filtered out. In addition, the HPF can minimize system noise from DC-DC converters, pulse repetition frequency (PRF) trigger, and frame clock. Most ultrasound systems' signal processing unit includes digital high-pass filters or band-pass filters (BPFs) in FPGAs or ASICs. Further noise suppression can be achieved in these blocks. In addition, a digital HPF is available in the AFE5809 ADC. If low frequency signal detection is desired in some applications, the LNA HPF can be disabled.

Table 25. LNA HPF Settings (C_{BYPASS} = 15 nF)

Reg59[3:2] (0x3B[3:2])	Frequency
00	100 KHz
01	50 KHz
10	200 KHz
11	150 KHz

CM_BYP and VHIGH pins, which generate internal reference voltages, need to be decoupled with ≥1µF capacitors. Bigger bypassing capacitors (>2.2µF) may be beneficial if low frequency noise exists in system.

LNA Noise Contribution

The noise spec is critical for LNA and it determines the dynamic range of entire system. The LNA of the AFE5809 achieves low power and an exceptionally low-noise voltage of 0.63 nV/√Hz, and a low current noise of 2.7 pA/√Hz.

Typical ultrasonic transducer's impedance R_s varies from tens of ohms to several hundreds of ohms. Voltage noise is the dominant noise in most cases; however, the LNA current noise flowing through the source impedance (Rs) generates additional voltage noise.

$$LNA\_Noise_{total} = \sqrt{V^2_{LNAnoise} + R^2_s \times I^2_{LNAnoise}} \quad (12)$$

The AFE5809 achieves low noise figure (NF) over a wide range of source resistances as shown in Figure 33, Figure 34, andFigure 35.

Active Termination

In ultrasound applications, signal reflection exists due to long cables between transducer and system. The reflection results in extra ringing added to echo signals in PW mode. Since the axial resolution depends on echo signal length, such ringing effect can degrade the axial resolution. Hence, either passive termination or active termination, is preferred if good axial resolution is desired. Figure 99 shows three termination configurations:

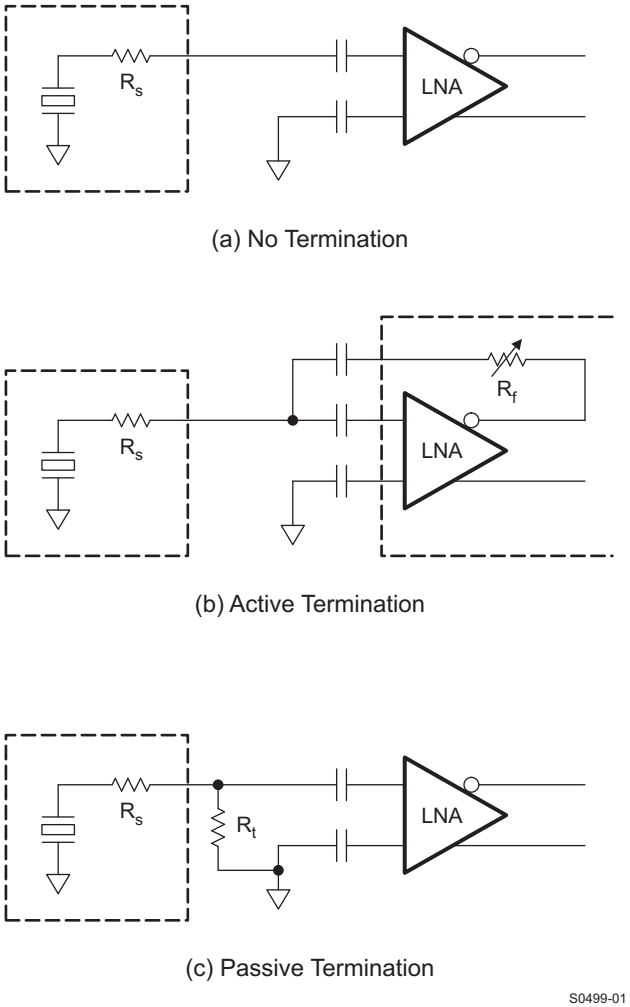


Figure 99. Termination Configurations

Under the no termination configuration, the input impedance of the AFE5809 is about 6 KΩ (8 K//20pF) at 1 MHz. Passive termination requires external termination resistor R_t, which contributes to additional thermal noise.

The LNA supports active termination with programmable values, as shown in Figure 100 .

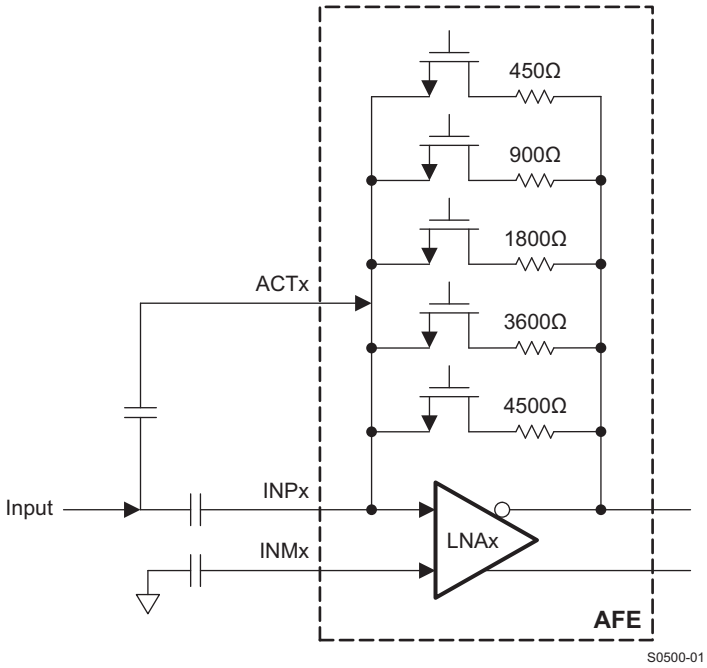


Figure 100. Active Termination Implementation

The AFE5809 has four pre-settings 50,100, 200 and 400Ω which are configurable through the registers. Other termination values can be realized by setting the termination switches shown in Figure 100. Register [52] is used to enable these switches. The input impedance of the LNA under the active termination configuration approximately follows:

$$Z_{IN} = \frac{R_f}{1 + \frac{A\nu_{LNA}}{2}} \quad (13)$$

Table 5 lists the LNA R_{IN}s under different LNA gains. System designers can achieve fine tuning for different probes.

The equivalent input impedance is given by Equation 14 where R_{IN} (8K) and C_{IN} (20pF) are the input resistance and capacitance of the LNA.

$$Z_{IN} = \frac{R_f}{1 + \frac{A\nu_{LNA}}{2}} / /C_{IN} / /R_{IN} \quad (14)$$

Therefore, the Z_{IN} is frequency dependent and it decreases as frequency increases shown in Figure 11. Since 2 MHz to 10 MHz is the most commonly used frequency range in medical ultrasound, this rolling-off effect doesn't impact system performance greatly. Active termination can be applied to both CW and TGC modes. Since each ultrasound system includes multiple transducers with different impedances, the flexibility of impedance configuration is a great plus.

Figure 33, Figure 34, andFigure 35 shows the NF under different termination configurations. It indicates that no termination achieves the best noise figure; active termination adds less noise than passive termination. Thus termination topology should be carefully selected based on each use scenario in ultrasound.

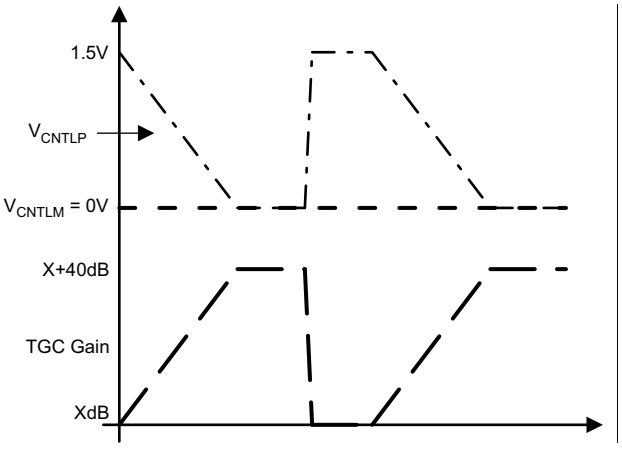
LNA Gain Switch Response

The LNA gain is programmable through SPI. The gain switching time depends on the SPI speed as well as the LNA gain response time. During the switching, glitches might occur and they can appear as artifacts in images. In addtion, the signal chain needs about 14 us to settle after the LNA gain change. Thus LNA gain switching may not be preferred when switching time or settling time for the signal chain is limited.

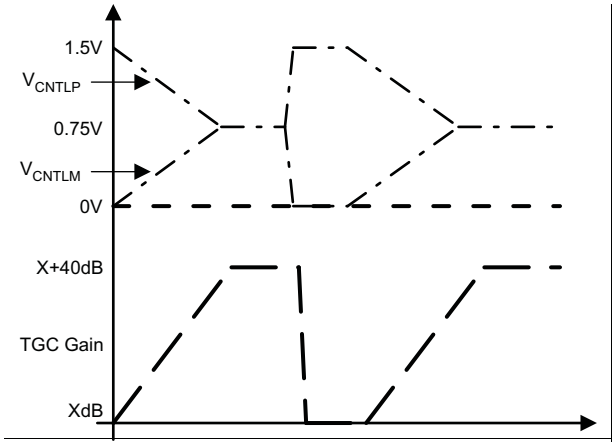
VOLTAGE-CONTROLLED-ATTENUATOR

The attenuator in the AFE5809 is controlled by a pair of differential control inputs, the $V_{CNTLM,P}$ pins. The differential control voltage spans from 0V to 1.5V. This control voltage varies the attenuation of the attenuator based on its linear-in-dB characteristic. Its maximum attenuation (minimum channel gain) appears at V_{CNTLP}-V_{CNTLM}= 1.5V, and minimum attenuation (maximum channel gain) occurs at V_{CNTLP} - V_{CNTLM}= 0. The typical gain range is 40dB and remains constant, independent of the PGA setting.

When only single-ended V_{CNTL} signal is available, this 1.5Vpp signal can be applied on the V_{CNTLP} pin with the V_{CNTLM} pin connected to ground; As the below figures show, TGC gain curve is inversely proportional to the V_{CNTLP}-V_{CNTLM}.



(a) Single-Ended Input at V_{CNTLP}



(b) Differential Inputs at V_{CNTLP} and V_{CNTLM}

W0004-01

Figure 101. V_{CNTLP} and V_{CNTLM} Configurations

As discussed in the theory of operation, the attenuator architecture uses seven attenuator segments that are equally spaced in order to approximate the linear-in-dB gain-control slope. This approximation results in a monotonic slope; the gain ripple is typically less than ±0.5dB.

The control voltage input ($V_{CNTLM,P}$ pins) represents a high-impedance input. The $V_{CNTLM,P}$ pins of multiple AFE5809 devices can be connected in parallel with no significant loading effects. When the voltage level (V_{CNTLP}-V_{CNTLM}) is above 1.5 V or below 0 V, the attenuator continues to operate at its maximum attenuation level or minimum attenuation level respectively. It is recommended to limit the voltage from -0.3 V to 2 V.

When the AFE5809 operates in CW mode, the attenuator stage remains connected to the LNA outputs. Therefore, it is recommended to power down the VCA using the PDN_VCA register bit. In this case, V_{CNTLP}-V_{CNTLM} voltage does not matter.

The AFE5809 gain-control input has a –3dB bandwidth of approximately 800KHz. This wide bandwidth, although useful in many applications (e.g. fast V_{CNTL} response), can also allow high-frequency noise to modulate the gain control input and finally affect the Doppler performance. In practice, this modulation can be avoided by additional external filtering (RV_{CNTL} and CV_{CNTL}) at $V_{CNTLM,P}$ pins as Figure 96 shows. However, the external filter's cutoff frequency cannot be kept too low as this results in low gain response time. Without external filtering, the gain control response time is typically less than 1 µs to settle within 10% of the final signal level of 1VPP (–6dBFS) output as indicated in Figure 52 and Figure 53.

Typical $V_{CNTLM,P}$ signals are generated by an 8bit to 12bit 10MSPS digital to analog converter (DAC) and a differential operation amplifier. TI's DACs, such as TLV5626 and DAC7821/11 (10MSPS/12bit), could be used to generate TGC control waveforms. Differential amplifiers with output common mode voltage control (that is, THS4130 and OPA1632) can connect the DAC to the $V_{CNTLM/P}$ pins. The buffer amplifier can also be configured as an active filter to suppress low frequency noise. The $V_{CNTLM/P}$ circuit shall achieve low noise in order to prevent the $V_{CNTLM/P}$ noise being modulated to RF signals. It is recommended that $V_{CNTLM/P}$ noise is below 25 nV/rtHz at 1KHz and 5 nV/rtHz at 50 KHz. More information can be found in the literatures SLOS318F and SBAA150. The V_{CNTL} vs Gain curves can be found in Figure 3. The below table also shows the absolute gain vs. V_{CNTL}, which may help program DAC correspondingly.

In PW Doppler and color Doppler modes, V_{CNTL} noise should be minimized to achieve the best close-in phase noise and SNR. Digital V_{CNTL} feature is implemented to address this need in the AFE5809. In the digital V_{CNTL} mode, no external V_{CNTL} is needed.

Table 26. V_{CNTLP}–V_{CNTLM} vs Gain Under Different LNA and PGA Gain Settings (Low Noise Mode)

V_{CNTLP}–V_{CNTLM} (V)	Gain (dB) LNA = 12 dB PGA = 24 dB	Gain (dB) LNA = 18 dB PGA = 24 dB	Gain (dB) LNA = 24 dB PGA = 24 dB	Gain (dB) LNA = 12 dB PGA = 30 dB	Gain (dB) LNA = 18 dB PGA = 30 dB	Gain (dB) LNA = 24 dB PGA = 30 dB
0	36.45	42.45	48.45	42.25	48.25	54.25
0.1	33.91	39.91	45.91	39.71	45.71	51.71
0.2	30.78	36.78	42.78	36.58	42.58	48.58
0.3	27.39	33.39	39.39	33.19	39.19	45.19
0.4	23.74	29.74	35.74	29.54	35.54	41.54
0.5	20.69	26.69	32.69	26.49	32.49	38.49
0.6	17.11	23.11	29.11	22.91	28.91	34.91
0.7	13.54	19.54	25.54	19.34	25.34	31.34
0.8	10.27	16.27	22.27	16.07	22.07	28.07
0.9	6.48	12.48	18.48	12.28	18.28	24.28
1.0	3.16	9.16	15.16	8.96	14.96	20.96
1.1	–0.35	5.65	11.65	5.45	11.45	17.45
1.2	–2.48	3.52	9.52	3.32	9.32	15.32
1.3	–3.58	2.42	8.42	2.22	8.22	14.22
1.4	–4.01	1.99	7.99	1.79	7.79	13.79
1.5	–4	2	8	1.8	7.8	13.8

CW OPERATION

CW Summing Amplifier

In order to simplify CW system design, a summing amplifier is implemented in the AFE5809 to sum and convert 8-channel mixer current outputs to a differential voltage output. Low noise and low power are achieved in the summing amplifier while maintaining the full dynamic range required in CW operation.

This summing amplifier has 5 internal gain adjustment resistors which can provide 32 different gain settings (register 54[4:0], Figure 100 and Table 6). System designers can easily adjust the CW path gain depending on signal strength and transducer sensitivity. For any other gain values, an external resistor option is supported. The gain of the summation amplifier is determined by the ratio between the 500Ω resistors after LNA and the internal or external resistor network $R_{EXT/INT}$. Thus the matching between these resistors plays a more important role than absolute resistor values. Better than 1% matching is achieved on chip. Due to process variation, the absolute resistor tolerance could be higher. If external resistors are used, the gain error between I/Q channels or among multiple AFEs may increase. It is recommended to use internal resistors to set the gain in order to achieve better gain matching (across channels and multiple AFEs). With the external capacitor C_{EXT} , this summing amplifier has 1st order LPF response to remove high frequency components from the mixers, such as 2f0±fd. Its cut-off frequency is determined by:

$$f_{HP} = \frac{1}{2\pi R_{INT/EXT} C_{EXT}} \quad (15)$$

Note that when different gain is configured through register 54[4:0], the LPF response varies as well.

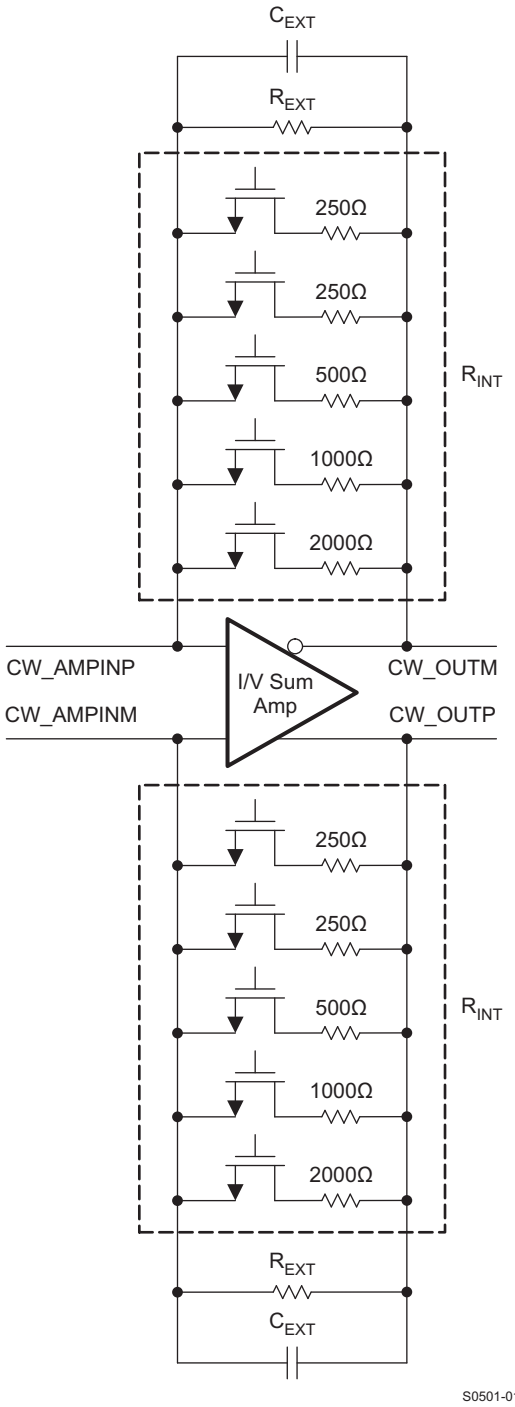


Figure 102. CW Summing Amplifier Block Diagram

Multiple AFE5809s are usually utilized in parallel to expand CW beamformer channel count. These AFE5809 CW's voltage outputs can be summed and filtered externally further to achieve desired gain and filter response. AC coupling capacitors C_{AC} are required to block DC component of the CW carrier signal. C_{AC} can vary from 1 µF to 10s µF depending on the desired low frequency Doppler signal from slow blood flow. Multiple AFE5809s' I/Q outputs can be summed together with a low noise external differential amplifiers before 16, 18-bit differential audio ADCs. The TI ultralow noise differential precision amplifier OPA1632 and THS4130 are suitable devices.

An alternative current summing circuit is shown in Figure 104. However this circuit only achieves good performance when a lower noise operational amplfier is avablie compared to the AFE5809's internal summing differential amplifier.

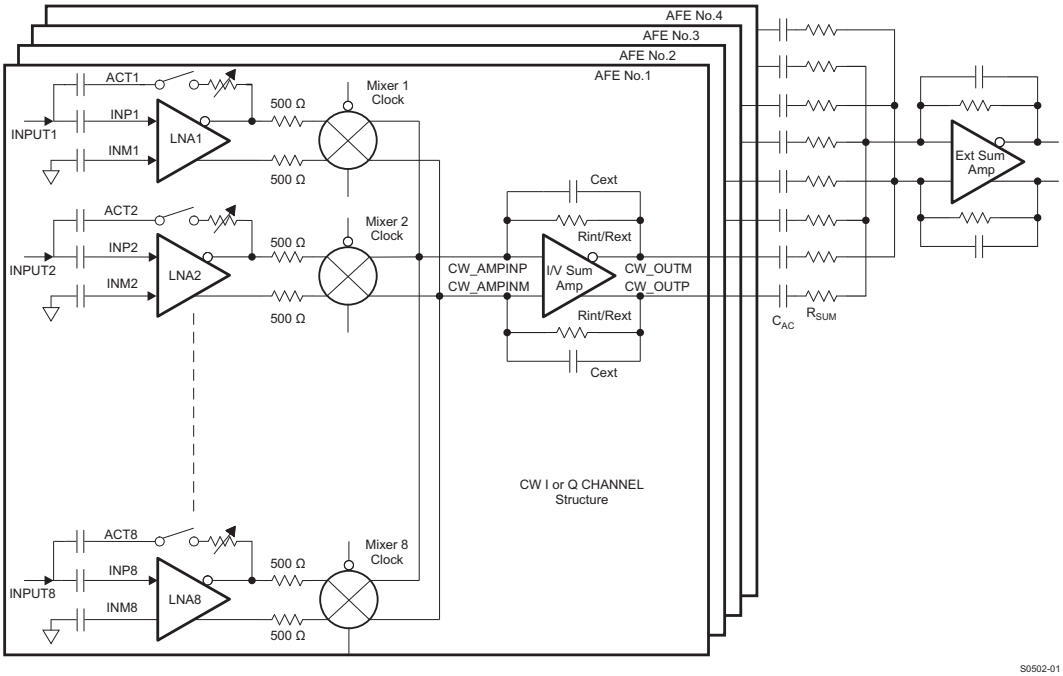


Figure 103. CW Circuit with Multiple AFE5809s (Voltage output mode)

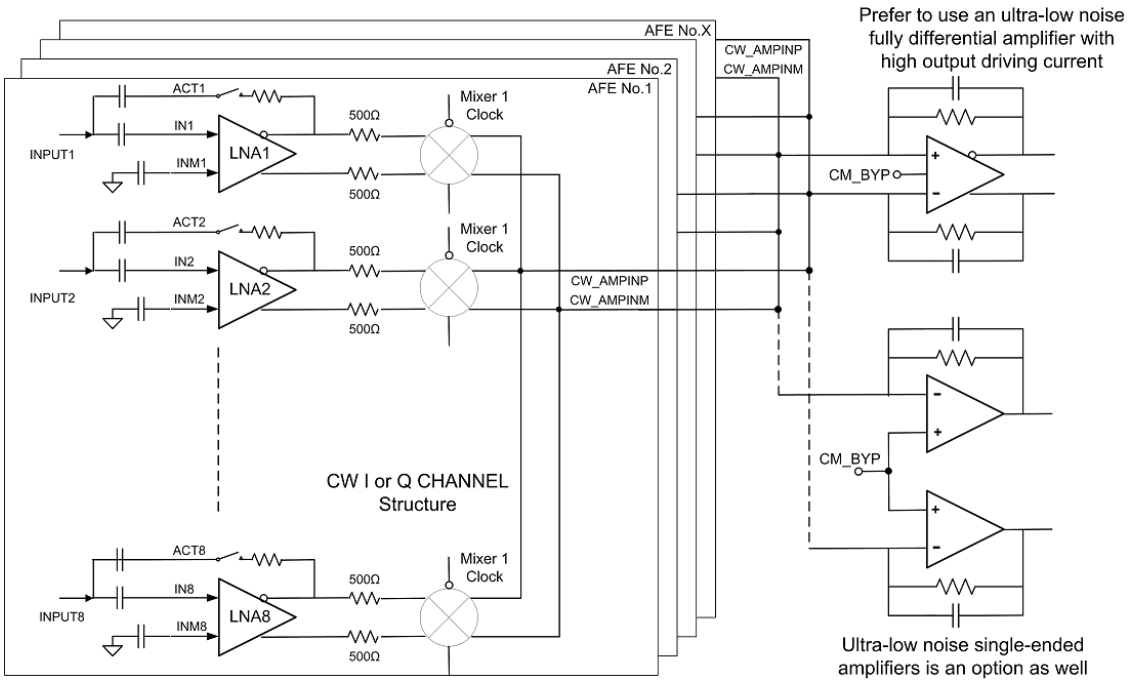


Figure 104. CW Circuit with Multiple AFE5809s (Current output mode)

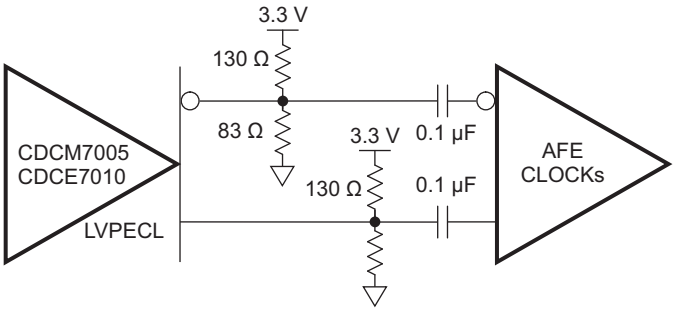
The CW I/Q channels are well matched internally to suppress image frequency components in Doppler spectrum. Low tolerance components and precise operational amplifiers should be used for achieving good matching in the external circuits as well.

NOTE

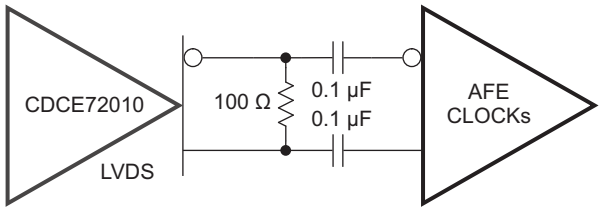
The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH respectively. Depending on users' CW Doppler complex FFT processing, swapping I/Q channels in FPGA or DSP may be needed in order to get correct blood flow directions.

CW Clock Selection

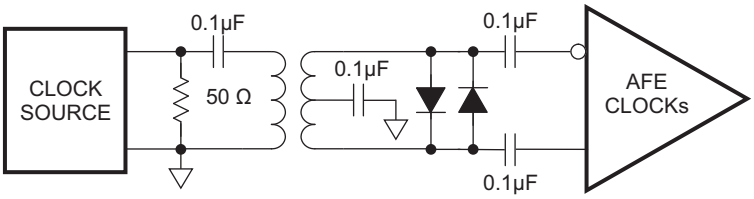
The AFE5809 can accept differential LVDS, LVPECL, and other differential clock inputs as well as single-ended CMOS clock. An internally generated VCM of 2.5V is applied to CW clock inputs, that is CLKP_16X/ CLKM_16X and CLKP_1X/ CLKM_1X. Since this 2.5 V VCM is different from the one used in standard LVDS or LVPECL clocks, AC coupling is required between clock drivers and the AFE5809 CW clock inputs. When CMOS clock is used, CLKM_1X and CLKM_16X should be tied to ground. Common clock configurations are illustrated in Figure 105. Appropriate termination is recommended to achieve good signal integrity.



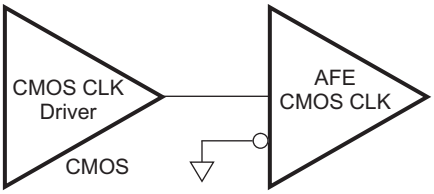
(a) LVPECL Configuration



(b) LVDS Configuration



(c) Transformer Based Configuration



(d) CMOS Configuration

S0503-01

Figure 105. Clock Configurations

The combination of the clock noise and the CW path noise can degrade the CW performance. The internal clocking circuit is designed for achieving excellent phase noise required by CW operation. The phase noise of the AFE5809 CW path is better than 155dBc/Hz at 1KHz offset. Consequently the phase noise of the mixer clock inputs needs to be better than 155 dBc/Hz.

In the 16/8/4×fcw operations modes, low phase noise clock is required for 16, 8, 4 × f_{cw} clocks (that is CLKP_16X/ CLKM_16X pins) in order to maintain good CW phase noise performance. The 1 × f_{cw} clock (that is CLKP_1X/ CLKM_1X pins) is only used to synchronize the multiple AFE5809 chips and is not used for demodulation. Thus 1×fcw clock's phase noise is not a concern. However, in the 1 × $f$cw operation mode, low phase noise clocks are required for both CLKP_16X/ CLKM_16X and CLKP_1X/ CLKM_1X pins since both of them are used for mixer demodulation. In general, higher slew rate clock has lower phase noise; thus, clocks with high amplitude and fast slew rate are preferred in CW operation. In the CMOS clock mode, 5 V CMOS clock can achieve the highest slew rate.

Clock phase noise can be improved by a divider as long as the divider's phase noise is lower than the target phase noise. The phase noise of a divided clock can be improved approximately by a factor of 20logN dB where N is the dividing factor of 16, 8, or 4. If the target phase noise of mixer LO clock 1×fcw is 160dBc/Hz at 1KHz off carrier, the 16×fcw clock phase noise should be better than 160-20log16=136dBc/Hz. TI's jitter cleaners LMK048X/CDCM7005/CDCE72010 exceed this requirement and can be selected for the AFE5809. In the 4X/1X modes, higher quality input clocks are expected to achieve the same performance since N is smaller. Thus the 16X mode is a preferred mode since it reduces the phase noise requirement for system clock design. In addition, the phase delay accuracy is specified by the internal clock divider and distribution circuit. Note in the 16X operation mode, the CW operation range is limited to 8 MHz due to the 16X CLK. The maximum clock frequency for the 16X CLK is 128 MHz. In the 8X, 4X, and 1X modes, higher CW signal frequencies up to 15 MHz can be supported with small degradation in performance, e.g. the phase noise is degraded by 9 dB at 15 MHz, compared to 2 MHz.

As the channel number in a system increases, clock distribution becomes more complex. It is not preferred to use one clock driver output to drive multiple AFEs since the clock buffer's load capacitance increases by a factor of N. As a result, the falling and rising time of a clock signal is degraded. A typical clock arrangement for multiple AFE5809s is illustrated in Figure 106. Each clock buffer output drives one AFE5809 in order to achieve the best signal integrity and fastest slew rate, that is better phase noise performance. When clock phase noise is not a concern, e.g. the 1 × $f$cw clock in the 16, 8, 4 × $f$cw operation modes, one clock driver output may excite more than one AFE5809s. Nevertheless, special considerations should be applied in such a clock distribution network design. In typical ultrasound systems, it is preferred that all clocks are generated from a same clock source, such as 16 × $f$cw , 1 × $f$cw clocks, audio ADC clocks, RF ADC clock, pulse repetition frequency signal, frame clock and so on. By doing this, interference due to clock asynchronization can be minimized

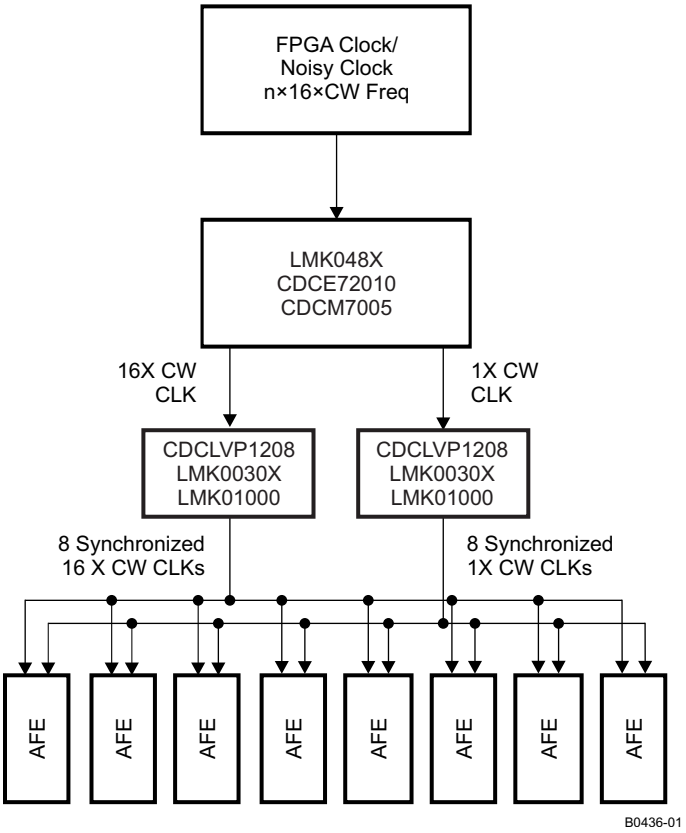


Figure 106. CW Clock Distribution

CW Supporting Circuits

As a general practice in CW circuit design, in-phase and quadrature channels should be strictly symmetrical by using well matched layout and high accuracy components.

In systems, additional high-pass wall filters (20 Hz to 500 Hz) and low-pass audio filters (10 KHz to 100 KHz) with multiple poles are usually needed. Since CW Doppler signal ranges from 20 Hz to 20 KHz, noise under this range is critical. Consequently low noise audio operational amplifiers are suitable to build these active filters for CW post-processing, that is OPA1632 or OPA2211. More filter design techniques can be found from www.ti.com. The TI active filter design tool http://focus.ti.com/docs/toolsw/folders/print/filter-designer.html

The filtered audio CW I/Q signals are sampled by audio ADCs and processed by DSP or PC. Although CW signal frequency is from 20 Hz to 20 KHz, higher sampling rate ADCs are still preferred for further decimation and SNR enhancement. Due to the large dynamic range of CW signals, high resolution ADCs (≥ 16bit) are required, such as ADS8413 (2MSPS, 16it, 92dBFS SNR) and ADS8472 (1MSPS/16bit/95dBFS SNR). ADCs for in-phase and quadature-phase channels must be strictly matched, not only amplitude matching but also phase matching, in order to achieve the best I/Q matching,. In addition, the in-phase and quadrature ADC channels must be sampled simultaneously.

LOW FREQUENCY SUPPORT

In addition, the signal chain of the AFE5809 can handle signal frequency lower than 100 KHz, which enables the AFE5809 to be used in both sonar and medical applicaitons. The PGA intergrator has to be turned off in order to enable the low frequency support. Meanwhile, a large capacitor like 1 µF can be used for setting low corner frequency of the LNA DC offset correction circuit as shown in Figure 77. AFE5809's low frequency response can be found in Figure 60.

ADC OPERATION

ADC Clock Configurations

To ensure that the aperture delay and jitter are the same for all channels, the AFE5809 uses a clock tree network to generate individual sampling clocks for each channel. The clock, for all the channels, are matched from the source point to the sampling circuit of each of the eight internal ADCs. The variation on this delay is described in the aperture delay parameter of the output interface timing. Its variation is given by the aperture jitter number of the same table.

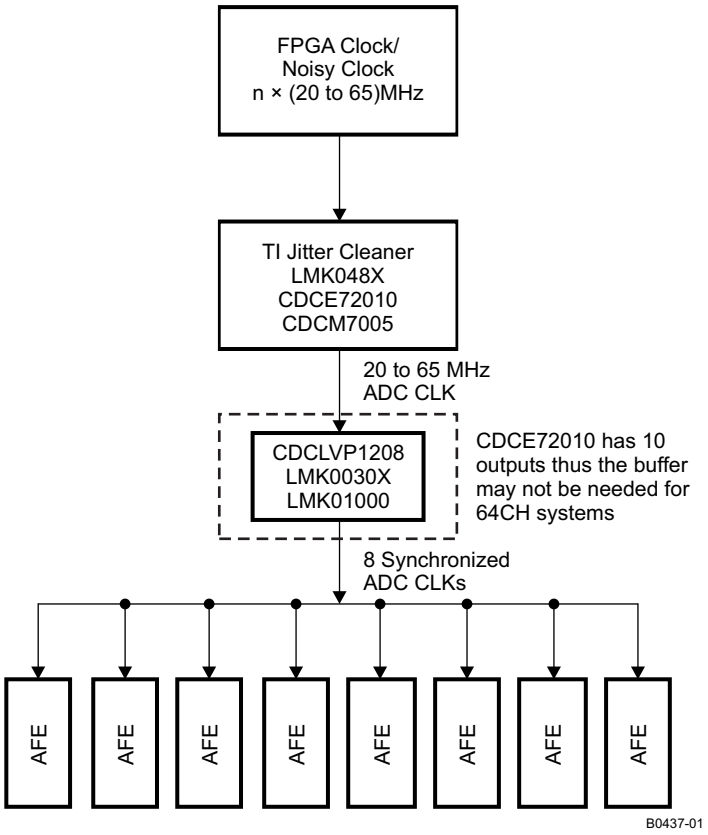


Figure 107. ADC Clock Distribution Network

The AFE5809 ADC clock input can be driven by differential clocks (sine wave, LVPECL or LVDS) or singled clocks (LVCMOS) similar to CW clocks as shown in Figure 105. In the single-end case, it is recommended that the use of low jitter square signals (LVCMOS levels, 1.8V amplitude). See TI document SLYT075 for further details on the theory.

The jitter cleaner CDCM7005 or CDCE72010 is suitable to generate the AFE5809's ADC clock and ensure the performance for the14bit ADC with 77dBFS SNR. A clock distribution network is shown in Figure 107.

ADC Reference Circuit

The ADC's voltage reference can be generated internally or provided externally. When the internal reference mode is selected, the REFP/M becomes output pins and should be floated. When 3[15] =1 and 1[13]=1, the device is configured to operate in the external reference mode in which the VREF_IN pin should be driven with a 1.4 V reference voltage and REFP/M must be left open. Since the input impedance of the VREF_IN is high, no special drive capability is required for the 1.4 V voltage reference

The digital beam-forming algorithm in an ultrasound system relies on gain matching across all receiver channels. A typical system would have about 12 octal AFEs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the AFEs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures that the reference voltages are well-matched across different chips. When the external reference mode is used, a solid reference plane on a printed circuit board can ensure minimal voltage variation across devices. More information on voltage reference design can be found in the document SLYT339.

The dominant gain variation in the AFE5809 comes from the VCA gain variation. The gain variation contributed by the ADC reference circuit is much smaller than the VCA gain variation. Hence, in most systems, using the ADC internal reference mode is sufficient to maintain good gain matching among multiple AFE5809s. In addition, the internal reference circuit without any external components achieves satisfactory thermal noise and phase noise performance."

POWER MANAGEMENT

Power/Performance Optimization

The AFE5809 has options to adjust power consumption and meet different noise performances. This feature would be useful for portable systems operated by batteries when low power is more desired. Please refer to characteristics information listed in the table of electrical characteristics as well as the typical characteristic plots.

Power Management Priority

Power management plays a critical role to extend battery life and ensure long operation time. The AFE5809 has fast and flexible power down/up control which can maximize battery life. The AFE5809 can be powered down/up through external pins or internal registers. Table 27 indicates the affected circuit blocks and priorities when the power management is invoked. The higher priority controls can overwrite the lower priority controls.

In the device, all the power down controls are logically ORed to generate final power down for different blocks. The higher priority controls can cover the lower priority controls.

The digital demoduator also has 4 power down controls, PWRDWN_VCA_BYPASS, PWRDWN_ADC_BYPASS, PWRDWN_DIG_BYPASS, and PWRDWN_LVDS_BYPASS. Their priority is lower the controls listed inTable 27.

Table 27. Power Management Priority

	Name	Blocks	Priority
Pin	PDN_GLOBAL	All	High
Pin	PDN_VCA	LNA + VCAT+ PGA	Medium
Register	VCA_PARTIAL_PDN	LNA + VCAT+ PGA	Low
Register	VCA_COMPLETE_PDN	LNA + VCAT+ PGA	Medium
Pin	PDN_ADC	ADC	Medium
Register	ADC_PARTIAL_PDN	ADC	Low
Register	ADC_COMPLETE_PDN	ADC	Medium
Register	PDN_VCAT_PGA	VCAT + PGA	Lowest
Register	PDN_LNA	LNA	Lowest

Partial Power-Up/Down Mode

The partial power up/down mode is also called as fast power up/down mode. In this mode, most amplifiers in the signal path are powered down, while the internal reference circuits remain active as well as the LVDS clock circuit, that is the LVDS circuit still generates its frame and bit clocks.

The partial power down function allows the AFE5809 to be wake up from a low-power state quickly. This configuration ensures that the external capacitors are discharged slowly; thus a minimum wake-up time is needed as long as the charges on those capacitors are restored. The VCA wake-up response is typically about 2 µs or 1% of the power down duration whichever is larger. The longest wake-up time depends on the capacitors connected at INP and INM, as the wake-up time is the time required to recharge the caps to the desired operating voltages. For 0.1 µF at INP and 15 nF at INM can give a wake-up time of 2.5 ms. For larger capacitors this time will be longer. The ADC wake-up time is about 1 µs. Thus the AFE5809 wake-up time is more dependent on the VCA wake-up time. This also assumes that the ADC clock has been running for at least 50 µs before normal operating mode resumes. The power-down time is instantaneous, less than 1 µs.

This fast wake-up response is desired for portable ultrasound applications in which the power saving is critical. The pulse repetition frequency of a ultrasound system could vary from 50KHz to 500 Hz, while the imaging depth (that is the active period for a receive path) varies from 10 µs to hundreds of us. The power saving can be pretty significant when a system's PRF is low. In some cases, only the VCA would be powered down while the ADC keeps running normally to ensure minimal impact to FPGAs.

In the partial power-down mode, the AFE5809 typically dissipates only 26mW/ch, representing an 80% power reduction compared to the normal operating mode. This mode can be set using either pins (PDN_VCA and PDN_ADC) or register bits (VCA_PARTIAL_PDN and ADC_PARTIAL_PDN).

Complete Power-Down Mode

To achieve the lowest power dissipation of 0.7 mW/CH, the AFE5809 can be placed into a complete power-down mode. This mode is controlled through the registers ADC_COMPLETE_PDN, VCA_COMPLETE_PDN or PDN_GLOBAL pin. In the complete power-down mode, all circuits including reference circuits within the AFE5809 are powered down; and the capacitors connected to the AFE5809 are discharged. The wake-up time depends on the time needed to recharge these capacitors. The wake-up time depends on the time that the AFE5809 spends in shutdown mode. 0.1 µF at INP and 15 nF at INM can give a wake-up time close to 2.5 ms

Power Saving in CW Mode

Usually only half the number of channels in a system are active in the CW mode. Thus the individual channel control through ADC_PDN_CH <7:0> and VCA_PDN_CH <7:0> can power down unused channels and save power consumption greatly. Under the default register setting in the CW mode, the voltage controlled attenuator, PGA, and ADC are still active. During the debug phase, both the PW and CW paths can be running simultaneously. In real operation, these blocks need to be powered down manually.

TEST MODES

The AFE5809 includes multiple test modes to accelerate system development. The ADC test modes have been discussed in the register description section.

The VCA has a test mode in which the CH7 and CH8 PGA outputs can be brought to the CW pins. By monitoring these PGA outputs, the functionality of VCA operation can be verified. The PGA outputs are connected to the virtual ground pins of the summing amplifier (CW_IP_AMPINM/P, CW_QP_AMPINM/P) through 5KΩ resistors. The PGA outputs can be monitored at the summing amplifier outputs when the LPF capacitors C_{EXT} are removed. Please note that the signals at the summing amplifier outputs are attenuated due to the 5 KΩ resistors. The attenuation coefficient is $R_{INT/EXT}$/5 KΩ

If users would like to check the PGA outputs without removing CEXT, an alternative way is to measure the PGA outputs directly at the CW_IP_AMPINM/P and CW_QP_AMPINM/P when the CW summing amplifier is powered down

Some registers are related to this test mode. PGA Test Mode Enable: Reg59[9]; Buffer Amplifier Power Down Reg59[8]; and Buffer Amplifier Gain Control Reg54[4:0]. Based on the buffer amplifier configuration, the registers can be set in different ways:

- Configuration 1
  - In this configuration, the test outputs can be monitored at CW_AMPINP/M
  - Reg59[9]=1 ;Test mode enabled
  - Reg59[8]=0 ;Buffer amplifier powered down
- Configuration 2

– In this configuration, the test outputs can be monitored at CW_OUTP/M
– Reg59[9]=1 ;Test mode enabled
– Reg59[8]=1 ;Buffer amplifier powered on
– Reg54[4:0]=10H; Internal feedback 2K resistor enabled. Different values can be used as well

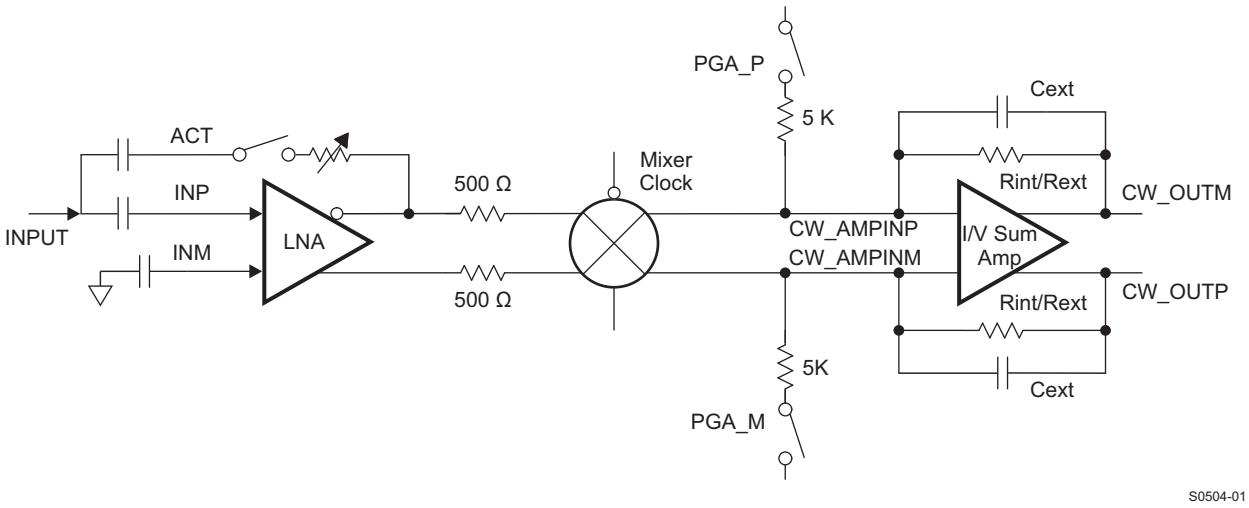


Figure 108. AFE5809 PGA Test Mode

POWER SUPPLY, GROUNDING AND BYPASSING

In a mixed-signal system design, power supply and grounding design plays a significant role. The AFE5809 distinguishes between two different grounds: AVSS(Analog Ground) and DVSS(digital ground). In most cases, it should be adequate to lay out the printed circuit board (PCB) to use a single ground plane for the AFE5809. Care should be taken that this ground plane is properly partitioned between various sections within the system to minimize interactions between analog and digital circuitry. Alternatively, the digital (DVDD) supply set consisting of the DVDD and DVSS pins can be placed on separate power and ground planes. For this configuration, the AVSS and DVSS grounds should be tied together at the power connector in a star layout. In addition, optical isolator or digital isolators, such as ISO7240, can separate the analog portion from the digital portion completely. Consequently they prevent digital noise to contaminate the analog portion. Table 27 lists the related circuit blocks for each power supply.

Table 28. Supply vs Circuit Blocks

Power Supply	Ground	Circuit Blocks
AVDD (3.3VA)	AVSS	LNA, attenuator, PGA with clamp and BPF, reference circuits, CW summing amplifier, CW mixer, VCA SPI
AVDD_5V (5VA)	AVSS	LNA, CW clock circuits, reference circuits
AVDD_ADC (1.8VA)	AVSS	ADC analog and reference circuits
DVDD (1.8VD)	DVSS	LVDS and ADC SPI

All bypassing and power supplies for the AFE5809 should be referenced to their corresponding ground planes. All supply pins should be bypassed with 0.1 µF ceramic chip capacitors (size 0603 or smaller). In order to minimize the lead and trace inductance, the capacitors should be located as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition, larger bipolar decoupling capacitors 2.2 µF to 10 µF, effective at lower frequencies) may also be used on the main supply pins. These components can be placed on the PCB in proximity (< 0.5 in or 12.7 mm) to the AFE5809 itself.

The AFE5809 has a number of reference supplies needed to be bypassed, such CM_BYP, VHIGH, and VREF_IN. These pins should be bypassed with at least 1µF; higher value capacitors can be used for better low-frequency noise suppression. For best results, choose low-inductance ceramic chip capacitors (size 0402, > 1 µF) and place them as close as possible to the device pins.

High-speed mixed signal devices are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffer/drivers. For the AFE5809, care has been taken to ensure that the interaction between the analog and digital supplies within the device is kept to a minimal amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each of the supply and ground connections. Smaller effective inductance of the supply and ground pins leads to improved noise suppression. For this reason, multiple pins are used to connect each supply and ground sets. It is important to maintain low inductance properties throughout the design of the PCB layout by use of proper planes and layer thickness.

BOARD LAYOUT

Proper grounding and bypassing, short lead length, and the use of ground and power-supply planes are particularly important for high-frequency designs. Achieving optimum performance with a high-performance device such as the AFE5809 requires careful attention to the PCB layout to minimize the effects of board parasitics and optimize component placement. A multilayer PCB usually ensures best results and allows convenient component placement. In order to maintain proper LVDS timing, all LVDS traces should follow a controlled impedance design. In addition, all LVDS trace lengths should be equal and symmetrical; it is recommended to keep trace length variations less than 150mil (0.150 in or 3.81 mm).

To avoid noise coupling through supply pins, it is recommended to keep sensitive input pins, such as INM, INP, ACT pins aways from the AVDD 3.3 V and AVDD_5V planes. For example, either the traces or vias connected to these pins should not be routed across the AVDD 3.3 V and AVDD_5V planes. In addition, appropriate delay matching should be considered for the CW clock path, especially in systems with high channel count. For example, if clock delay is half of the 16x clock period, a phase error of 22.5°C could exist. Thus the timing delay difference among channels contributes to the beamformer accuracy.

Additional details on BGA PCB layout techniques can be found in the Texas Instruments Application Report MicroStar BGA Packaging Reference Guide (SSYZ015B), which can be downloaded from www.ti.com.

REVISION HISTORY

Changes from Original (September 2012) to Revision A **Page**

- 已将器件状态从：产品预览改为：生产 1

Changes from Revision A (September 2012) to Revision B **Page**

- Deleted 特性：“可编程数字 I/Q 解调器” 1
- Changed 特性：噪声、功率优化（无数字解调器）从：1.1nV/rtHz，40MSPS 时为 99mW/CH 改为：1.1nV/rtHz，40MSPS 时为 101mW/CH 1
- Changed 特性：出色的器件到器件增益匹配从：±0.5dB（典型值）和 ±0.9dB（最大值）改为：±0.5dB（典型值）和 ±1dB（最大值） 1
- Changed Gain matching values From MIN = -0.9 dB to MIN = -1 dB and From: MAX = 0.9 dB to MAX = 1 dB 9
- Added a note to PGA_CLAMP_LEVEL: "in the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0" 36
- Added Note: "In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0" 62

Changes from Revision B (September 2012) to Revision C **Page**

- Changed 'SIN' to '-SIN' and 'C8' to 'Cn' in Figure 2 3
- Added a note "The above timing data can be applied to 12-bit or 16-bit LVDS rates" 24
- Changed SPI pull down resistors from "100kΩ" to "20kΩ". 27
- Added a note to register 0x3[14:13] "Make sure the settings aligning with the demod register 0x3[14:13]" 31
- Added Note to PGA_CLAMP_LEVEL: "The maximum PGA output level can exceed 2Vpp with the clamp circuit enabled.". 36
- Changed List item From: "The internal 32 bit filter output" To: The internal 36 bit filter output" 49
- Changed text following Table 21From: "the block index, from 0 to (-1)" To: "the block index, from 0 to (M-1) 51
- Changed from "For RF mode (passing 14 bits only)... 0xC3[14:13] to ‘00’ " to "...0xC3[14:13] to ‘10’ " in LVDS Serialization Factor 51
- Added "The maximum PGA output level can be above 2Vpp even with the clamp circuit enabled" in the PGA description. 62
- Added a note "The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH " 63
- Changed "10Ω" to "10-15Ω " in Figure 82 64
- Added a NOTE "The digital demodulator is based on a conventional down converter, that is, -sin(ω_0t) is used for Q phase. 70
- Added text "It is recommended that $V_{CNTLM/P}$ noise is below 25 nV/rtHz at 1KHz and 5 nV/rtHz at 50 KHz. " 79
- Added a note "The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH " 83
- Added "AVDD_5V needs to be away from sensitive input pins" 91

Changes from Revision C (January 2013) to Revision D **Page**

- 将特性从：抽取滤波器因数 M = 1 至 64 改为：。。。M = 1 至 32 1
- 已添加针对全新芯片特性的注释。 2
- Changed pin description of CLKM_16X from "In the 1X CW clock mode, this pin becomes the quadrature-phase 1X CLKM for the CW mixer" to "... in-phase 1X CLKM for the CW mixer" 5
- Changed pin description of CLKP_16X from "In the 1X CW clock mode, this pin becomes the quadrature-phase 1X CLKP for the CW mixer" to "... in-phase 1X CLKP for the CW mixer" 5
- Changed pin description of CLKM_1X from "In the 1X CW clock mode, this pin becomes the in-phase 1X CLKP for the CW mixer" to "... quadrature-phase 1X CLKP for the CW mixer" 5
- Changed pin description of CLKP_1X from "In the 1X CW clock mode, this pin becomes the in-phase 1X CLKP for

the CW mixer" to "... quadrature-phase 1X CLKP for the CW mixer" 5
- Corrected AVDD_5V current from 16.5mA to 26mA 11
- Changed 64X decimation factor to 32X decimation factor in DIGITAL DEMODULATOR ELECTRICAL CHARACTERISTICS 12
- Changed 64X decimation factor to 32X decimation factor in DIGITAL DEMODULATOR ELECTRICAL CHARACTERISTICS 12
- Corrected a typo in Reg0x2[15:13], i.e. changed 0x2[15:3] to 0x2[15:13] 30
- Added a note in the Reg 51[3:1] description,"Please note: 0x3D[14], i.e. 5MHz LPF, should be set a 0. " 36
- Added a note in the Reg 57[7:5] description,"Note: Reg.61[15] should be set as 0; otherwise PGA_CLAMP_LEVEL is determined by Reg. 61[15]." 36
- Added Reg 61[15:13] description. 38
- Added a note for Reg0x1F[5:0] "it is from 1 to 32." 46
- Changed "0x521" to "0x121F" inRF Mode 52
- Changed "MODULATE_BYPASS=1" to "MODULATE_BYPASS=0" inRF Mode 52
- Added "FIR Filter Delay vs. TX_TRIG Timing" and "Expression of Decimation Filter Response" 54

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE5809ZCF	ACTIVE	NFBGA	ZCF	135	160	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 85	AFE5809	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

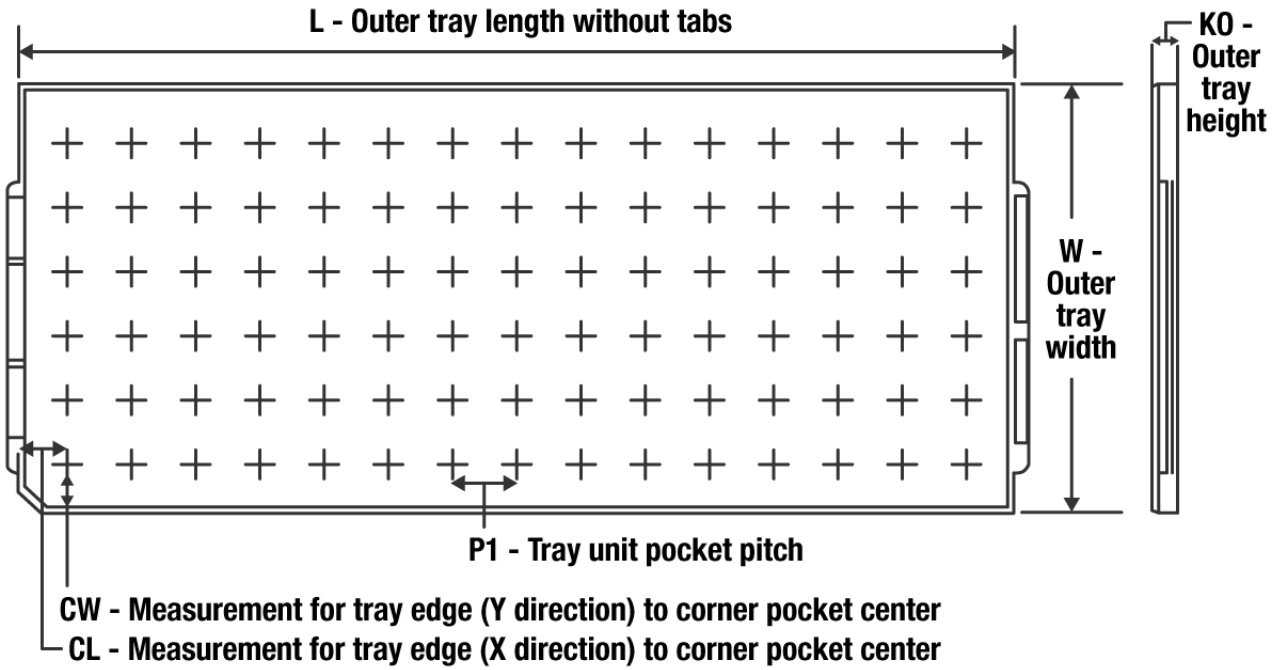
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY

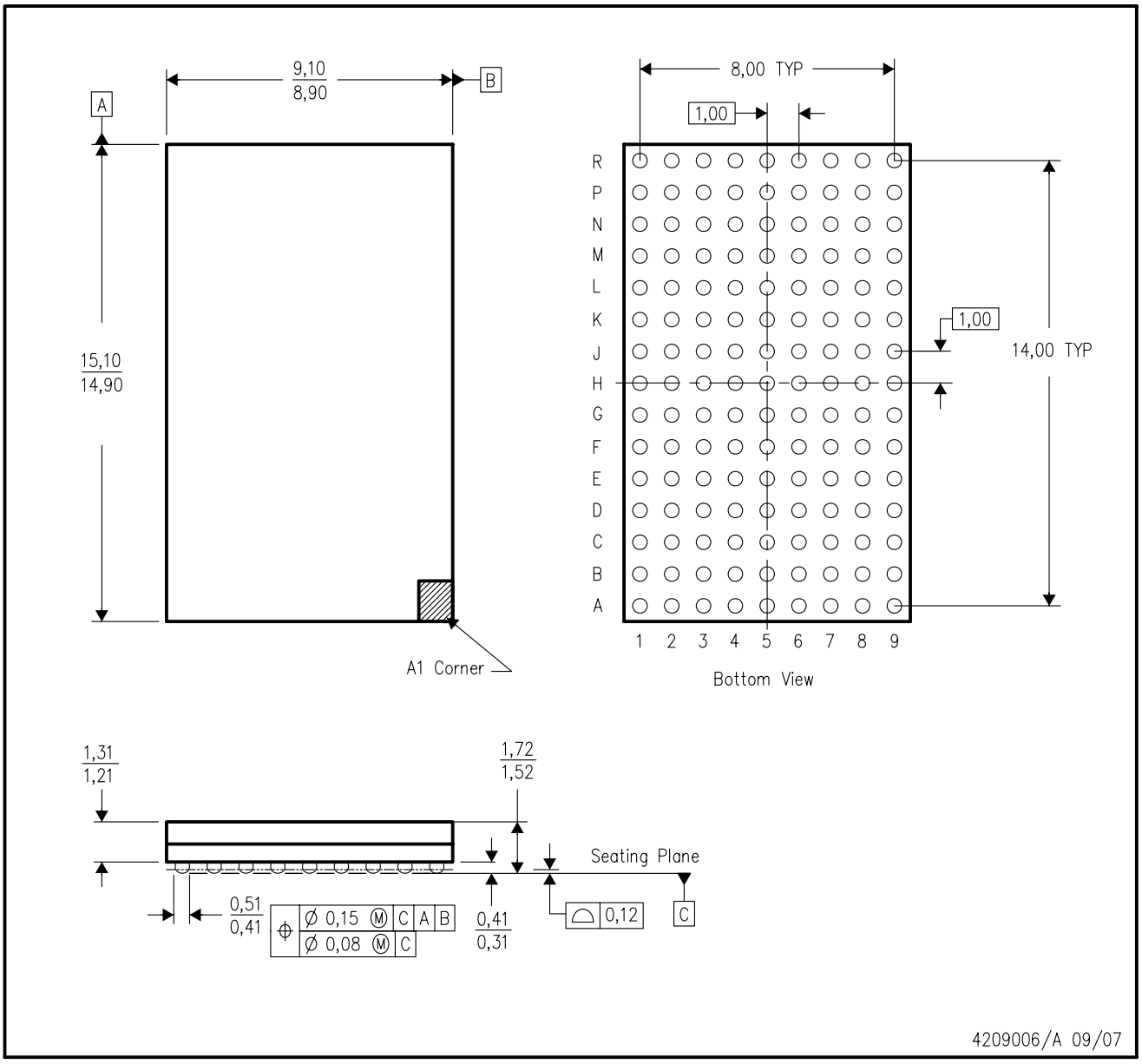


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE5809ZCF	ZCF	NFBGA	135	160	10 x 16	150	315	135.9	7620	19.2	13.5	10.35

ZCF (R–PBGA–N135) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994 .
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265