

AWR1443 单芯片 77 和 79GHz FMCW 雷达传感器

1 器件概述

1.1 特性

- FMCW 收发器
 - 集成式 PLL、发送器、接收器、基带和 A2D
 - 76 至 81GHz 覆盖范围，具有 4GHz 的可用带宽
 - 四个接收通道
 - 三个发送通道（可以同时使用两个通道）
 - 基于分数 N PLL 的超精确线性调频脉冲引擎
 - TX 功率：12dBm
 - RX 噪声系数：
 - 14dB（76 至 77GHz）
 - 15dB（77 至 81GHz）
 - 1MHz 时的相位噪声：
 - -94dBc/Hz（76 至 77GHz）
 - -91dBc/Hz（77 至 81GHz）
- 内置的校准和自检
 - ARM® Cortex® 基于 ARM® Cortex®-R4F 的无线电控制系统
 - 内置的固件 (ROM)
 - 针对频率和温度进行自校准的系统
- 适用于嵌入式用户应用的片上可编程内核
 - 计时频率为 200MHz 的集成 Cortex®-R4F 微控制器
 - 片上引导加载程序支持自主模式（从 QSPI 闪存加载用户应用）
 - 集成外设
 - 具有 ECC 的内部存储器
 - 雷达硬件加速器（FFT、对数幅度计算等）
 - 集成计时器（看门狗以及多达四个 32 位计时器或两个 64 位计时器）
- I2C（支持主模式和从模式）
- 两个 SPI 端口
- CAN 端口
- 多达六个通用 ADC 端口
- 支持分布式应用（即中间数据）的高速数据接口
- 主机接口
 - 通过 SPI 与外部处理器进行控制连接
 - 用于故障报告的中断
- 符合 AECQ100 标准
- AWR1443 高级特性
 - 嵌入式自监控，无需使用主机处理器
 - 复基带架构
 - 嵌入式干扰检测功能
- 电源管理
 - 内置的 LDO 网络，可增强 PSRR
 - I/O 支持双电压 3.3V/1.8V
- 时钟源
 - 支持外部驱动、频率为 40MHz 的时钟（方波/正弦波）
 - 支持 40MHz 晶体与负载电容器相连接
- 轻松的硬件设计
 - 0.65mm 间距、161 引脚 10.4mm × 10.4mm 覆晶 BGA 封装，可实现轻松组装和低成本 PCB 设计
 - 小尺寸解决方案
- 支持汽车运行温度范围

1.2 应用

- 邻近感测
- 泊车辅助
- 占位检测
- 简单手势识别
- 车门开启器应用

1.3 说明

AWR1443 器件是一款能够在 76 至 81GHz 频带中运行的集成式单芯片 FMCW 雷达传感器。该器件采用 TI 的低功耗 45nm RFCMOS 工艺构建，具有一个集成式 ARM R4F 处理器和一个硬件加速器，用于进行雷达数据处理，该解决方案在极小的封装中实现了前所未有的集成度。AWR1443 是适用于汽车领域中的低功耗、自监控、超精确雷达系统的理想解决方案。

AWR1443 器件是一种自包含 FMCW 雷达传感器单芯片解决方案，能够简化 76 至 81GHz 频带中的汽车雷达传感器实施。它实现了一个具有内置 PLL 和模数转换器的单片实施 3TX、4RX 系统。简单编程模型更改可支持各种传感器实施（近距离、中距离和远距离），并且能够进行动态重新配置，从而实现多模式传感器。此外，该器件作为完整的平台解决方案进行提供，该解决方案包括硬件参考设计、软件驱动程序、样例配置、API 指南以及用户文档。



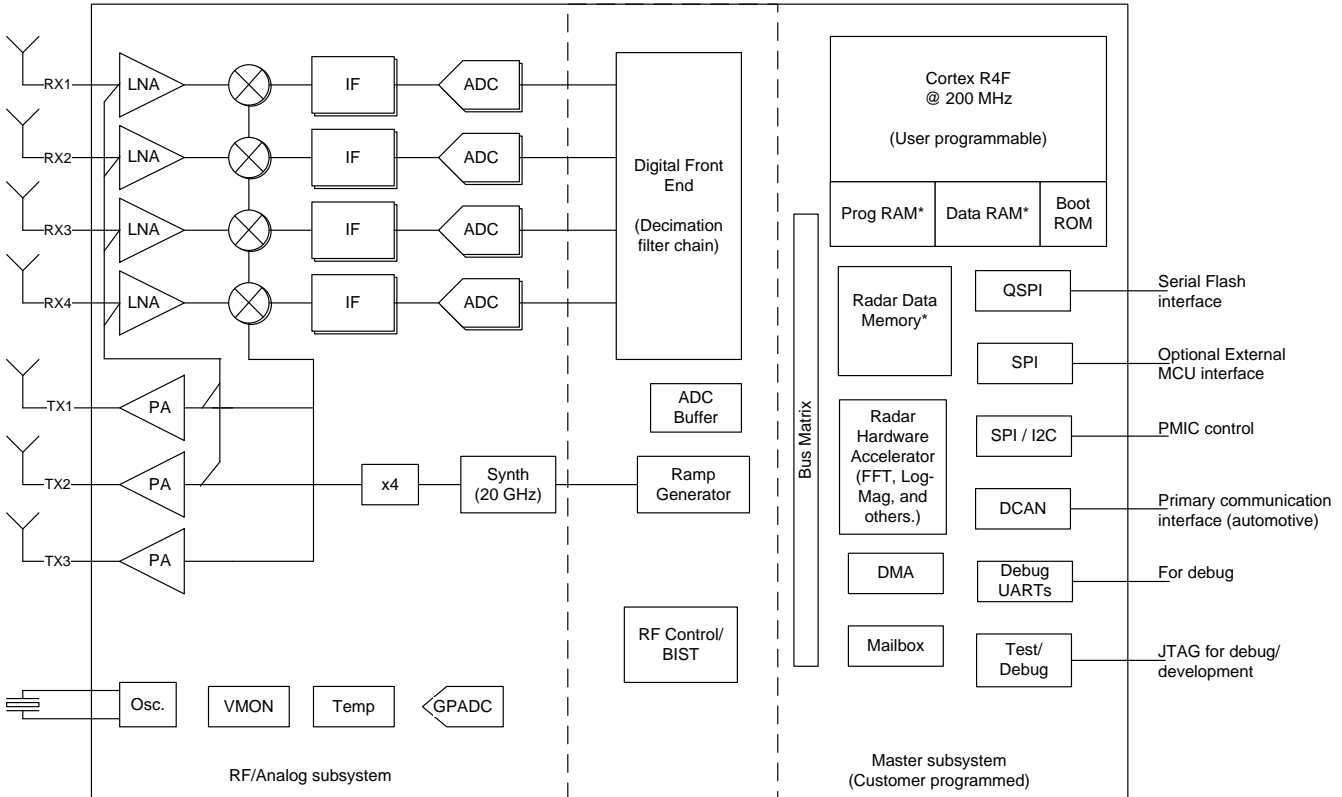
不同的应用在雷达数据存储立方体、处理能力和功能安全监控方面，对雷达器件的要求各不相同。电源的需求。在这种背景之下，可以将 AWR1443 视为适用于入门级雷达应用的 77GHz 片上雷达 解决方案。

器件信息⁽¹⁾

| 器件编号 | 封装 | 封装尺寸 |
|-----------------------|-------------|-----------------|
| AWR1443FQIGABLQ1 (托盘) | FCBGA (161) | 10.4mm x 10.4mm |
| AWR1443FQIGABLRQ1 (卷) | | |

(1) 更多信息请参见 节 9，机械封装和可订购产品信息。

1.4 功能框图



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内容

| | | | | | |
|----------|---|---------------------------|----------|---|---------------------------|
| 1 | 器件概述 | 1 | 6.2 | Functional Block Diagram | 46 |
| 1.1 | 特性 | 1 | 6.3 | External Interfaces | 47 |
| 1.2 | 应用 | 1 | 6.4 | Subsystems | 47 |
| 1.3 | 说明 | 1 | 6.5 | Accelerators and Coprocessors | 53 |
| 1.4 | 功能框图 | 2 | 6.6 | Other Subsystems | 54 |
| 2 | 修订历史记录 | 4 | 6.7 | Identification | 56 |
| 3 | Device Comparison | 5 | 6.8 | Boot Modes | 56 |
| 3.1 | Related Products | 6 | 7 | Applications, Implementation, and Layout | 59 |
| 4 | Terminal Configuration and Functions | 7 | 7.1 | Application Information | 59 |
| 4.1 | Pin Diagram | 7 | 7.2 | Short-Range Radar | 59 |
| 4.2 | Signal Descriptions | 12 | 7.3 | Blind Spot Detector and Ultrasonic Upgrades | 60 |
| 4.3 | Pin Multiplexing | 15 | 7.4 | Reference Schematic | 60 |
| 5 | Specifications | 20 | 7.5 | Layout | 62 |
| 5.1 | Absolute Maximum Ratings | 20 | 8 | Device and Documentation Support | 67 |
| 5.2 | ESD Ratings | 20 | 8.1 | Device Nomenclature | 67 |
| 5.3 | Power-On Hours (POH) | 20 | 8.2 | Tools and Software | 68 |
| 5.4 | Recommended Operating Conditions | 21 | 8.3 | Documentation Support | 68 |
| 5.5 | Power Supply Specifications | 21 | 8.4 | Community Resources | 69 |
| 5.6 | Power Consumption Summary | 22 | 8.5 | 商标 | 69 |
| 5.7 | RF Specification | 23 | 8.6 | 静电放电警告 | 69 |
| 5.8 | Thermal Resistance Characteristics for FCBGA Package [ABL0161] | 24 | 8.7 | Export Control Notice | 69 |
| 5.9 | Timing and Switching Characteristics | 24 | 8.8 | Glossary | 69 |
| 6 | Detailed Description | 46 | 9 | Mechanical, Packaging, and Orderable Information | 70 |
| 6.1 | Overview | 46 | 9.1 | Packaging Information | 70 |

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| Changes from May 1, 2017 to October 31, 2018 (from * Revision (May 2017) to A Revision) | Page |
|---|--------------------|
| • 将 RX 噪声系数从“15dB (76 至 77GHz)”更新成了“14dB (76 至 77GHz)” | 1 |
| • 将 RX 噪声系数从“16dB (77 至 81GHz)”更新成了“15dB (77 至 81GHz)” | 1 |
| • 更新/更改了时钟源子项目 | 1 |
| • 在“器件信息”中添加了新的可订购部件号 | 2 |
| • 更新了功能方框图中的 RX 和 TX 连接 | 2 |
| • Added AWR1243P to Device Features Comparison | 5 |
| • Updated/Changed Device Features Comparison ASIL for AWR1243P, AWR1243, and AWR1642 from "B-Capable" to "B-Targeted" | 5 |
| • Added "Max complex sampling rate (MSPS)" to Device Features Comparison | 5 |
| • Changed AWR1243 and AWR1443 Product status from AI to PD | 5 |
| • Corrected A10 pin to "VOUT_14APLL" | 8 |
| • Added DEFAULT PULL STATUS column to Signal Descriptions | 12 |
| • Added text to SYNC_IN Description in Signal Descriptions table | 12 |
| • Updated/Changed CLKP and CLKM descriptions in <i>Signal Descriptions</i> | 13 |
| • Deleted all rows after RS232_TX in <i>Pin Multiplexing</i> | 19 |
| • Changed HBM ESD value from ± 1000 V to ± 2000 V and CDM ESD value from ± 250 V to ± 500 V | 20 |
| • Added footnote to $V_{(ESD)}$ | 20 |
| • Completely updated Recommended Operating Conditions | 21 |
| • Added footnote to Power Supply Rails Characteristics | 21 |
| • Added footnote to Maximum Current Ratings at Power Terminals | 22 |
| • Updated footnote to Maximum Current Ratings at Power Terminals | 22 |
| • Updated Average Power Consumption at Power Terminals | 22 |
| • Updated RF Specification | 23 |
| • Updated footnote in RF Specification | 24 |
| • Removed 1v4 signal from Device Wakeup | 25 |
| • Updated Device Wake-up Sequence | 25 |
| • Updated Synchronized Frame Triggering text | 26 |
| • Added Synchronized Frame Triggering subsection | 26 |
| • Removed T_{Lag} from Frame Trigger Timing table | 26 |
| • Updated Crystal Implementation note | 27 |
| • Updated/Changed f_p Parallel resonance crystal frequency from "40, 50" to "40" | 27 |
| • Updated/Changed Frequency tolerance from "-50 and 50" to "-200 to 200" | 27 |
| • Added External Clock Mode Specifications | 27 |
| • Completely updated External Clock Mode Specifications | 27 |
| • Updated SPI Slave Mode Timing Requirements | 33 |
| • Added LVDS Interface Configuration | 36 |
| • Updated LVDS Interface Lane Config image | 36 |
| • Updated Timing Parameters | 36 |
| • Updated LVDS Electrical Characteristics | 37 |
| • Updated Timing Requirements for QSPI Input (Read) Timings | 42 |
| • Updated QSPI Switching Characteristics | 43 |
| • Updated/Changed <i>Clock Subsystem</i> diagram | 48 |
| • Removed sentence from Transmit Subsystem | 49 |
| • Updated/Changed Recieve Subsystem text from "...cutoff frequencies above 350 kHz..." to "...cutoff frequencies above 175 kHz..." | 49 |
| • Updated/Changed <i>ADC Channels (Service) for User Application</i> text from "...for ADC channel mapped to B12..." to "...for ADC channel mapped to C14..." | 54 |
| • Deleted "ADC supply/reference voltage" from <i>GP-ADC Parameter</i> | 54 |

3 Device Comparison

Table 3-1. Device Features Comparison

| FUNCTION | AWR1243P | AWR1243 | AWR1443 | AWR1642 |
|---|---|------------|---------|------------|
| Number of receivers | 4 | 4 | 4 | 4 |
| Number of transmitters | 3 ⁽¹⁾ | 3 | 3 | 2 |
| On-chip memory | — | — | 576KB | 1.5MB |
| ASIL | B-Targeted | B-Targeted | — | B-Targeted |
| Max I/F (Intermediate Frequency) (MHz) | 15 | 15 | 5 | 5 |
| Max real sampling rate (Msps) | 37.5 | 37.5 | 12.5 | 12.5 |
| Max complex sampling rate (Msps) | 18.75 | 18.75 | 6.25 | 6.25 |
| Processor | | | | |
| MCU (R4F) | — | — | Yes | Yes |
| DSP (C674x) | — | — | — | Yes |
| Peripherals | | | | |
| Serial Peripheral Interface (SPI) ports | 1 | 1 | 1 | 2 |
| Quad Serial Peripheral Interface (QSPI) | — | — | Yes | Yes |
| Inter-Integrated Circuit (I ² C) interface | — | — | 1 | 1 |
| Controller Area Network (DCAN) interface | — | — | Yes | Yes |
| CAN FD | — | — | — | Yes |
| Trace | — | — | — | Yes |
| PWM | — | — | — | Yes |
| Hardware In Loop (HIL/DMM) | — | — | — | Yes |
| GPADC | — | — | Yes | Yes |
| LVDS/Debug | Yes | Yes | Yes | Yes |
| CSI2 | Yes | Yes | — | — |
| Hardware accelerator | — | — | Yes | — |
| 1-V bypass mode | Yes | Yes | Yes | Yes |
| Cascade (20-GHz sync) | Yes | — | — | — |
| JTAG | — | — | Yes | Yes |
| Number of Tx that can be simultaneously used | 3 | 2 | 2 | 2 |
| Per chirp configurable Tx phase shifter | Yes | — | — | — |
| Product status ⁽²⁾ | PRODUCT PREVIEW (PP), ADVANCE INFORMATION (AI), or PRODUCTION DATA (PD) | AI | PD | PD |

(1) 3 Tx Simultaneous operation is supported only in AWR1243P with 1V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin.

(2) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

3.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave Sensors TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for automotive applications.

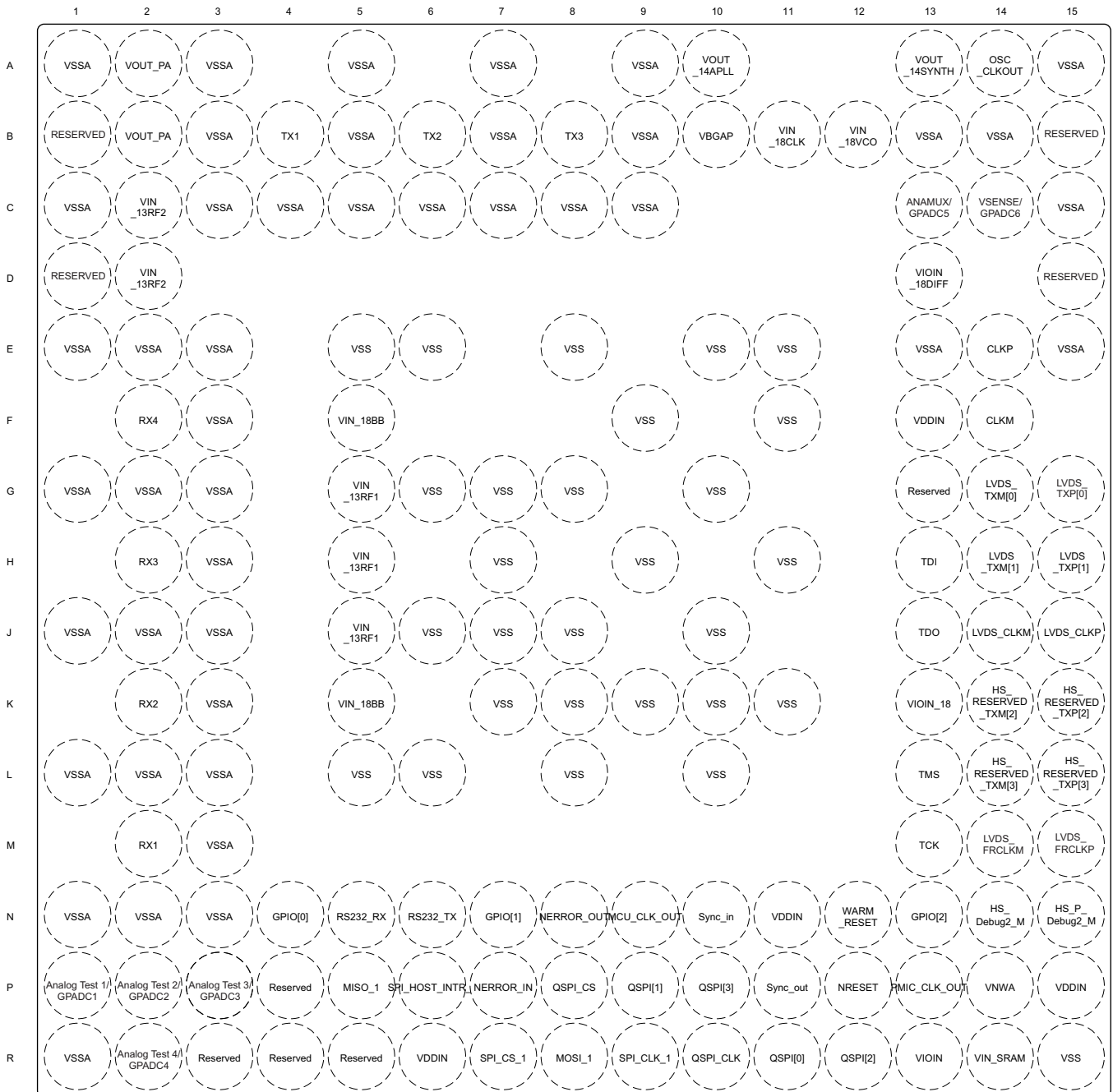
Automotive mmWave Sensors TI's automotive mmWave sensor portfolio offers high-performance radar front end to ultra-high resolution, small and low-power single-chip radar solutions. TI's scalable sensor portfolio enables design and development of ADAS system solution for every performance, application and sensor configuration ranging from comfort functions to safety functions in all vehicles.

Companion Products for AWR1443 Review products that are frequently purchased or used in conjunction with this product.

4 Terminal Configuration and Functions

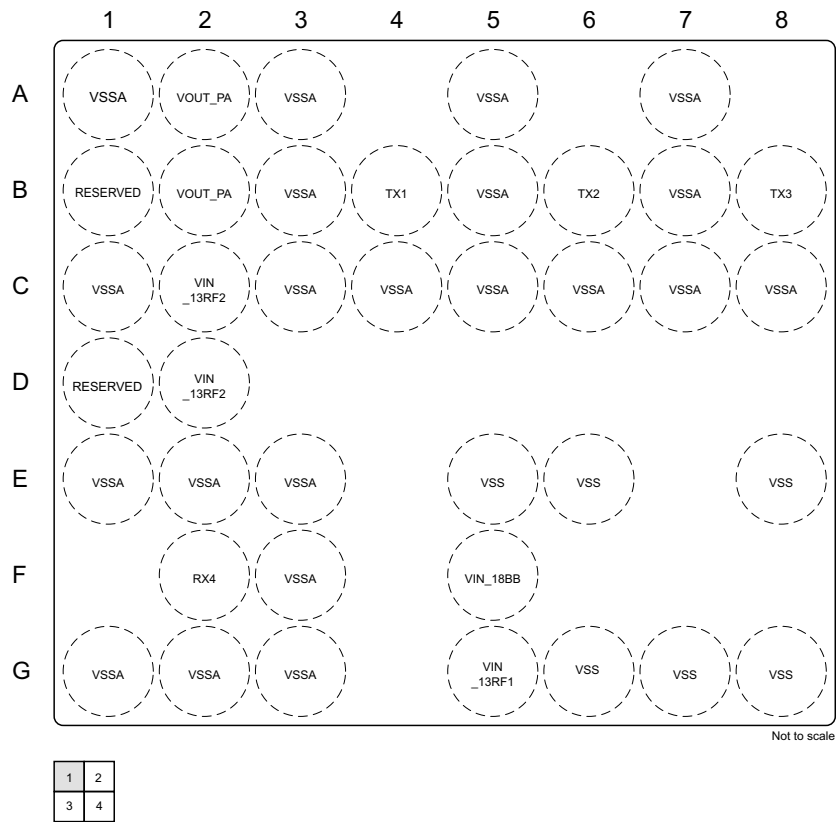
4.1 Pin Diagram

Figure 4-1 shows the pin locations for the 161-pin FCBGA package. Figure 4-2, Figure 4-3, Figure 4-4, and Figure 4-5 show the same pins, but split into four quadrants.



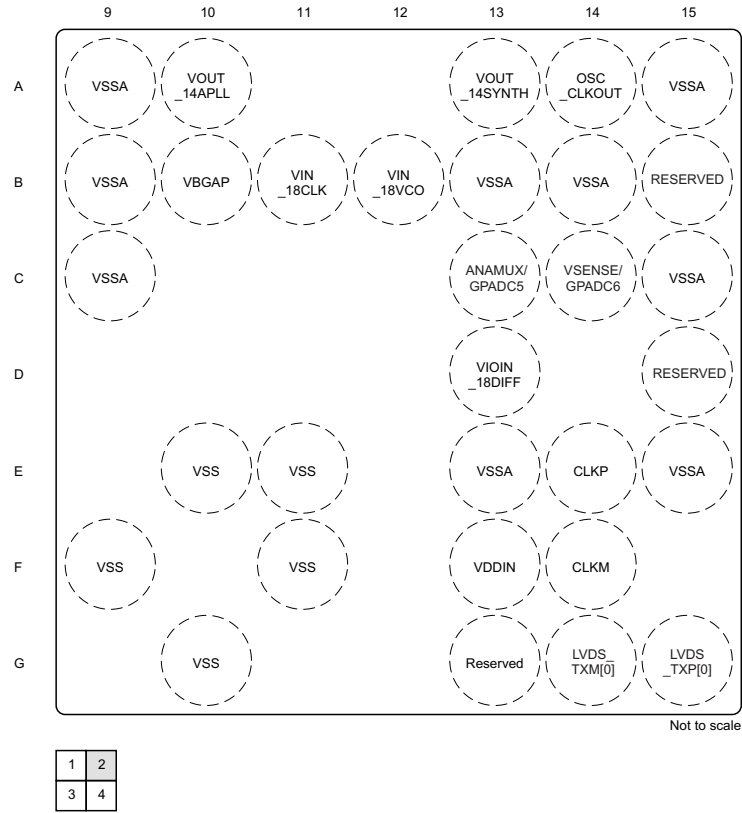
Not to scale
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Figure 4-1. Pin Diagram



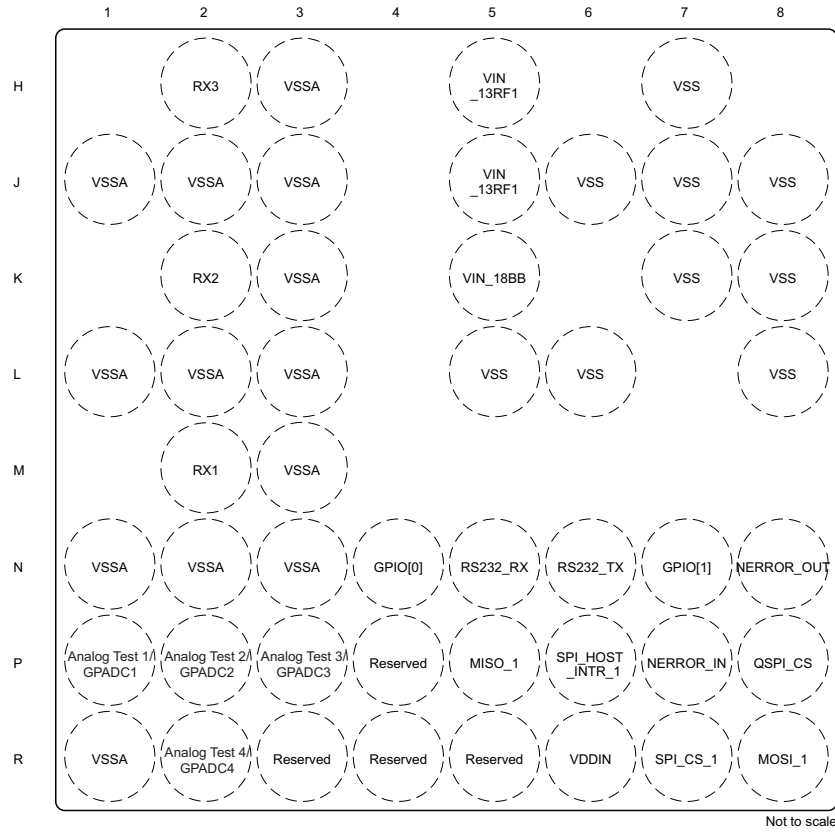
Not to scale

Figure 4-2. Top Left Quadrant



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Figure 4-3. Top Right Quadrant

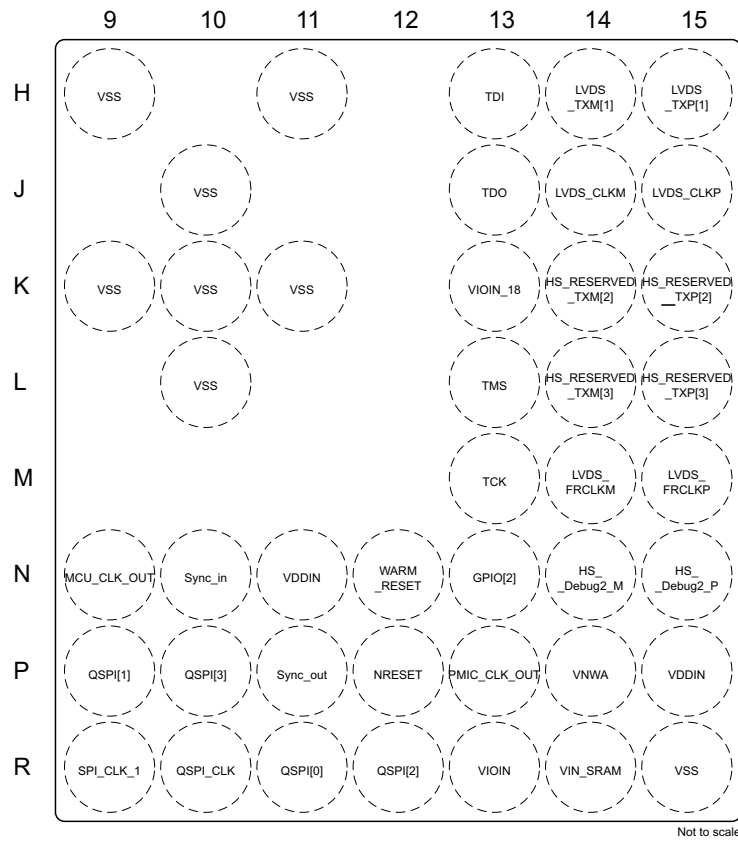


Not to scale

| | |
|---|---|
| 1 | 2 |
| 3 | 4 |

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Figure 4-4. Bottom Left Quadrant



Not to scale

| | |
|---|---|
| 1 | 2 |
| 3 | 4 |

Figure 4-5. Bottom Right Quadrant

4.2 Signal Descriptions

Table 4-1. Signal Descriptions

| FUNCTION | SIGNAL NAME | PIN NUMBER | PIN TYPE | DEFAULT PULL STATUS ⁽¹⁾ | DESCRIPTION |
|--|---------------------|------------------|----------|------------------------------------|--|
| Transmitters | TX1 | B4 | O | — | Single-ended transmitter1 o/p |
| | TX2 | B6 | O | — | Single-ended transmitter2 o/p |
| | TX3 | B8 | O | — | Single-ended transmitter3 o/p |
| Receivers | RX1 | M2 | I | — | Single-ended receiver1 i/p |
| | RX2 | K2 | I | — | Single-ended receiver2 i/p |
| | RX3 | H2 | I | — | Single-ended receiver3 i/p |
| | RX4 | F2 | I | — | Single-ended receiver4 i/p |
| LVDS TX | LVDS_TXP[0] | G15 | O | — | Differential data Out – Lane 0 |
| | LVDS_TXM[0] | G14 | O | — | |
| | LVDS_CLKP | J15 | O | — | Differential clock Out |
| | LVDS_CLKM | J14 | O | — | |
| | LVDS_TXP[1] | H15 | O | — | Differential data Out – Lane 1 |
| | LVDS_TXM[1] | H14 | O | — | |
| | HS_RESERVED_TX P[2] | K15 | O | — | Differential data Out – Lane 2 |
| | HS_RESERVED_TX M[2] | K14 | O | — | |
| | HS_RESERVED_TX P[3] | L15 | O | — | Differential data Out – Lane 3 |
| | HS_RESERVED_TX M[3] | L14 | O | — | |
| | LVDS_FRCLKP | M15 | O | — | Differential debug port 1 |
| | LVDS_FRCLKM | M14 | O | — | |
| | HS_DEBUG2_P | N15 | O | — | Differential debug port 2 |
| HS_DEBUG2_M | N14 | O | — | | |
| | RESERVED | B1, B15, D1, D15 | | — | |
| Reference clock | OSC_CLKOUT | A14 | O | — | Reference clock output from clocking subsystem after cleanup PLL. Can be used by slave chip in multichip cascading |
| System synchronization | SYNC_OUT | P11 | O | Pull Down | Low-frequency frame synchronization signal output. Can be used by slave chip in multichip cascading |
| | SYNC_IN | N10 | I | Pull Down | Low-frequency frame synchronization signal input. This signal could also be used as a hardware trigger for frame start |
| SPI control interface from external MCU (default slave mode) | SPI_CS_1 | R7 | I | Pull Up | SPI chip select |
| | SPI_CLK_1 | R9 | I | Pull Down | SPI clock |
| | MOSI_1 | R8 | I | Pull Up | SPI data input |
| | MISO_1 | P5 | O | Pull Up | SPI data output |
| | SPI_HOST_INTR_1 | P6 | O | Pull Down | SPI interrupt to host |
| | RESERVED | R3, R4, R5, P4 | | — | |
| Reset | NRESET | P12 | I | Open Drain | Power on reset for chip. Active low |
| | WARM_RESET | N12 | IO | Open Drain | Open-drain fail-safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset. |

(1) Status of PULL structures associated with the IO after device POWER UP.

Table 4-1. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NUMBER | PIN TYPE | DEFAULT PULL STATUS ⁽¹⁾ | DESCRIPTION |
|----------------------|--------------|--|----------|------------------------------------|---|
| Safety | NERROR_OUT | N8 | O | Open Drain | Open-drain fail-safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset. |
| | NERROR_IN | P7 | I | Open Drain | Fail-safe input to the device. Error output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by firmware |
| JTAG | TMS | L13 | I | Pull Up | JTAG port for standard boundary scan |
| | TCK | M13 | I | Pull Down | |
| | TDI | H13 | I | Pull Up | |
| | TDO | J13 | O | — | |
| Reference oscillator | CLKP | E14 | I | — | In XTAL mode: Differential port for reference crystal In External clock mode: Single ended input reference clock port (Output CLKM is grounded in this case) |
| | CLKM | F14 | O | — | |
| Band-gap voltage | VBGAP | B10 | O | — | |
| Power supply | VDDIN | F13,N11,P15,R6 | POW | — | 1.2-V digital power supply |
| | VIN_SRAM | R14 | POW | — | 1.2-V power rail for internal SRAM |
| | VNWA | P14 | POW | — | 1.2-V power rail for SRAM array back bias |
| | VIOIN | R13 | POW | — | I/O supply (3.3-V or 1.8-V): All CMOS I/Os would operate on this supply. |
| | VIOIN_18 | K13 | POW | — | 1.8-V supply for CMOS IO |
| | VIN_18CLK | B11 | POW | — | 1.8-V supply for clock module |
| | VIOIN_18DIFF | D13 | POW | — | 1.8-V supply for high speed interface port |
| | Reserved | G13 | POW | — | No connect |
| | VIN_13RF1 | G5,J5,H5 | POW | — | 1.3-V Analog and RF supply,VIN_13RF1 and VIN_13RF2 could be shorted on the board |
| | VIN_13RF2 | C2,D2 | POW | — | |
| | VIN_18BB | K5,F5 | POW | — | 1.8-V Analog baseband power supply |
| | VIN_18VCO | B12 | POW | — | 1.8-V RF VCO supply |
| | VSS | E5,E6,E8,E10,E11,F9,F11,G6,G7,G8,G10,H7,H9,H11,J6,J7,J8,J10,K7,K8,K9,K10,K11,L5,L6,L8,L10,R15 | GND | — | Digital ground |
| | VSSA | A1,A3,A5,A7,A9,A15,B3,B5,B7,B9,B13,B14,C1,C3,C4,C5,C6,C7,C8,C9,C15,E1,E2,E3,E13,E15,F3,G1,G2,G3,H3,J1,J2,J3,K3,L1,L2,L3,M3,N1,N2,N3,R1 | GND | — | Analog ground |

Table 4-1. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NUMBER | PIN TYPE | DEFAULT PULL STATUS ⁽¹⁾ | DESCRIPTION |
|---|-----------------------|------------|----------|------------------------------------|---|
| Internal LDO output/inputs | VOUT_14APLL | A10 | O | — | |
| | VOUT_14SYNTH | A13 | O | — | |
| | VOUT_PA | A2,B2 | O | — | |
| External clock out | PMIC_CLK_OUT | P13 | O | — | Dithered clock input to PMIC |
| | MCU_CLK_OUT | N9 | O | — | Programmable clock given out to external MCU or the processor |
| General-purpose I/Os | GPIO[0] | N4 | IO | Pull Down | General-purpose IO |
| | GPIO[1] | N7 | IO | Pull Down | General-purpose IO |
| | GPIO[2] | N13 | IO | Pull Down | General-purpose IO |
| QSPI for Serial Flash | QSPI_CS | P8 | O | Pull Up | Chip-select output from the device. Device is a master connected to serial flash slave. |
| | QSPI_CLK | R10 | O | Pull Down | Clock output from the device. Device is a master connected to serial flash slave. |
| | QSPI[0] | R11 | IO | Pull Down | Data IN/OUT |
| | QSPI[1] | P9 | IO | Pull Down | Data IN/OUT |
| | QSPI[2] | R12 | IO | Pull Up | Data IN/OUT |
| | QSPI[3] | P10 | IO | Pull Up | Data IN/OUT |
| Flash programming and RS232 UART ⁽²⁾ | RS232_TX | N6 | O | Pull Down | UART pins for programming external flash in preproduction/debug hardware. |
| | RS232_RX | N5 | I | Pull Up | |
| Test and Debug output for preproduction phase. Can be pinned out on production hardware for field debug | Analog Test1 / GPADC1 | P1 | IO | — | GP ADC channel 1 |
| | Analog Test2 / GPADC2 | P2 | IO | — | GP ADC channel 2 |
| | Analog Test3 / GPADC3 | P3 | IO | — | GP ADC channel 3 |
| | Analog Test4 / GPADC4 | R2 | IO | — | GP ADC channel 4 |
| | ANAMUX / GPADC5 | C13 | IO | — | GP ADC channel 5 |
| | VSENSE / GPADC6 | C14 | IO | — | GP ADC channel 6 |

(2) This option is for development/debug in preproduction phase. Can be disabled by firmware pin mux setting.

4.3 Pin Multiplexing

Table 4-2. Pin Multiplexing

| REGISTER ADDRESS ⁽¹⁾ | PIN NAME | PIN | DIGITAL PIN MUX CONFIG VALUE [Bits3:0] | FUNCTION | | | PAD STATE nReset = 0 [ASSERTED] | |
|---------------------------------|-----------|-----|--|----------------|---|-------------|------------------------------------|--------------------------|
| | | | | SIGNAL NAME | SIGNAL DESCRIPTION | SIGNAL TYPE | STATE | INTERNAL WEAK PULL STATE |
| EA00h | GPIO_12 | P6 | 0 | GPIO_12 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | SPI_HOST1_INTR | General Purpose IO [AWR14xx] | O | | |
| EA04h | GPIO_0 | N4 | 0 | GPIO_13 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | GPIO_0 | General Purpose IO | IO | | |
| | | | 2 | PMIC_CLKOUT | Dithered Clock Output for PMIC | O | | |
| EA08h | GPIO_1 | N7 | 0 | GPIO_16 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | GPIO_1 | General Purpose IO | IO | | |
| | | | 2 | SYNC_OUT | Low Frequency Synchronization Signal output | O | | |
| EA0Ch | MOSI_1 | R8 | 0 | GPIO_19 | General Purpose IO | IO | Hi-Z | Weak Pull Up |
| | | | 1 | MOSI_1 | SPI Channel#1 Data Input | IO | | |
| | | | 2 | CAN_RX | CAN Interface | I | | |
| EA10h | MISO_1 | P5 | 0 | GPIO_20 | General Purpose IO | IO | Hi-Z | Weak Pull Up |
| | | | 1 | MISO_1 | SPI Channel#1 Data Output | IO | | |
| | | | 2 | CAN_TX | CAN Interface | O | | |
| EA14h | SPI_CLK_1 | R9 | 0 | GPIO_3 | General Purpose IO | IO | Hi-Z | Weak Pull Up |
| | | | 1 | SPI_CLK_1 | SPI Channel#1 Clock | IO | | |
| | | | | RCOSC_CLK | | O | | |
| EA18h | SPI_CS_1 | R7 | 0 | GPIO_30 | General Purpose IO | IO | Hi-Z | Weak Pull Up |
| | | | 1 | SPI_CS_1 | SPI Channel#1 Chip Select | IO | | |
| | | | | RCOSC_CLK | | O | | |
| EA1Ch | MOSI_2 | R3 | 0 | GPIO_21 | General Purpose IO | IO | Hi-Z | |
| | | | 1 | MOSI_2 | SPI Channel#2 Data Input | IO | | |
| | | | 2 | I2C_SDA | I2C Data | IO | | |
| EA20h | MISO_2 | P4 | 0 | GPIO_22 | General Purpose IO | IO | Hi-Z | |
| | | | 1 | MISO_2 | SPI Channel#2 Data Output | IO | | |
| | | | 2 | I2C_SCL | I2C Clock | IO | | |

(1) Register addresses are of the form FFFF XXXXh, where XXXX is listed here.

Table 4-2. Pin Multiplexing (continued)

| REGISTER ADDRESS ⁽¹⁾ | PIN NAME | PIN | DIGITAL PIN MUX CONFIG VALUE [Bits3:0] | FUNCTION | | | PAD STATE nReset = 0 [ASSERTED] | |
|---------------------------------|-----------|-----|--|--------------|--|-------------|------------------------------------|--------------------------|
| | | | | SIGNAL NAME | SIGNAL DESCRIPTION | SIGNAL TYPE | STATE | INTERNAL WEAK PULL STATE |
| EA24h | SPI_CLK_2 | R5 | 0 | GPIO_5 | General Purpose IO | IO | Hi-Z | |
| | | | 1 | SPI_CLK_2 | SPI Channel#2 Clock | IO | | |
| | | | | MSS_UARTA_RX | | IO | | |
| | | | 6 | MSS_UARTB_TX | Debug: Firmware Trace | O | | |
| | | | 7 | BSS_UART_TX | Debug: Firmware Trace | O | | |
| EA28h | SPI_CS_2 | R4 | 0 | GPIO_4 | General Purpose IO | IO | Hi-Z | |
| | | | 1 | SPI_CS_2 | SPI Channel#2 Chip Select | IO | | |
| | | | | MSS_UARTA_TX | | IO | | |
| | | | 6 | MSS_UARTB_TX | Debug: Firmware Trace | O | | |
| | | | 7 | BSS_UART_TX | Debug: Firmware Trace | O | | |
| EA2Ch | QSPI[0] | R11 | 0 | GPIO_8 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | QSPI[0] | QSPI Data IN/OUT | IO | | |
| | | | 2 | MISO_2 | SPI Channel#1 Data Output | IO | | |
| EA30h | QSPI[1] | P9 | 0 | GPIO_9 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | QSPI[1] | QSPI Data IN/OUT | IO | | |
| | | | 2 | MOSI_2 | SPI Channel#2 Data Input | IO | | |
| EA34h | QSPI[2] | R12 | 0 | GPIO_10 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | QSPI[2] | QSPI Data IN/OUT | IO | | |
| EA38h | QSPI[3] | P10 | 0 | GPIO_11 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | QSPI[3] | QSPI Data IN/OUT | I | | |
| EA3Ch | QSPI_CLK | R10 | 0 | GPIO_7 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | QSPI_CLK | QSPI Clock output from the device. Device operates as a master with the serial flash being a slave | O | | |
| | | | 2 | SPI_CLK_2 | SPI Channel#2 Clock | IO | | |
| EA40h | QSPI_CS | P8 | 0 | GPIO_6 | General Purpose IO | IO | Hi-Z | Weak Pull Up |
| | | | 1 | QSPI_CS | QSPI Chip Select output from the device. Device operates as a master with the serial flash being a slave | O | | |
| | | | 2 | SPI_CS_2 | SPI Channel#2 Chip Select | IO | | |

Table 4-2. Pin Multiplexing (continued)

| REGISTER ADDRESS ⁽¹⁾ | PIN NAME | PIN | DIGITAL PIN MUX CONFIG VALUE [Bits3:0] | FUNCTION | | | PAD STATE nReset = 0 [ASSERTED] | |
|---------------------------------|------------|-----|--|--------------|---|-------------|------------------------------------|--------------------------|
| | | | | SIGNAL NAME | SIGNAL DESCRIPTION | SIGNAL TYPE | STATE | INTERNAL WEAK PULL STATE |
| | NERROR_IN | P7 | | NERROR_IN | Failsafe input to the device. Nerror output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by Firmware | I | Hi-Z | |
| | WARM_RESET | N12 | | WARM_RESET | Open drain fail safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset. | IO | Hi-Z Input | Open Drain |
| | NERROR_OUT | N8 | | NERROR_OUT | Open drain fail safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset. | O | Hi-Z | Open Drain |
| EA50h | TCK | M13 | 0 | GPIO_17 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | TCK | JTAG Clock | I | | |
| | | | 2 | MSS_UARTB_TX | Debug: Firmware Trace | O | | |
| | | | 6 | BSS_UART_RX | Debug: Firmware Trace | I | | |
| EA54h | TMS | L13 | 0 | GPIO_18 | General Purpose IO | IO | Hi-Z | Weak Pull Up |
| | | | 1 | TMS | JTAG Test Mode Select | IO | | |
| | | | 2 | BSS_UART_TX | Debug: Firmware Trace | O | | |
| EA58h | TDI | H13 | 0 | GPIO_23 | General Purpose IO | IO | Hi-Z | Weak Pull Up |
| | | | 1 | TDI | JTAG Test Data In | I | | |
| | | | | MSS_UARTA_RX | | IO | | |
| EA5Ch | TDO | J13 | 0 | GPIO_24 | General Purpose IO | IO | Hi-Z | |
| | | | 1 | TDO | JTAG Test Data Out | O | | |
| | | | | MSS_UARTA_TX | | IO | | |
| | | | 6 | MSS_UARTB_TX | Debug: Firmware Trace | O | | |
| | | | 7 | BSS_UART_TX | Debug: Firmware Trace | O | | |
| | | | | SOP0 | Sense On Power [Reset] Line Impacts boot mode | I | | |

Table 4-2. Pin Multiplexing (continued)

| REGISTER ADDRESS ⁽¹⁾ | PIN NAME | PIN | DIGITAL PIN MUX CONFIG VALUE [Bits3:0] | FUNCTION | | | PAD STATE nReset = 0 [ASSERTED] | |
|---------------------------------|-------------|-----|--|--------------|---|-------------|------------------------------------|--------------------------|
| | | | | SIGNAL NAME | SIGNAL DESCRIPTION | SIGNAL TYPE | STATE | INTERNAL WEAK PULL STATE |
| EA60h | MCU_CLKOUT | N9 | 0 | GPIO_25 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | MCU_CLKOUT | Programmable clock given out to external MCU or the processor | O | | |
| | | | 10 | BSS_UART_RX | Debug: Firmware Trace | I | | |
| EA64h | GPIO_2 | N13 | 0 | GPIO_26 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | GPIO_2 | General Purpose IO | IO | | |
| | | | 7 | MSS_UARTB_TX | Debug: Firmware Trace | O | | |
| | | | 8 | BSS_UART_TX | Debug: Firmware Trace | O | | |
| | | | 9 | SYNC_OUT | Low frequency Synchronization signal output | O | | |
| | | | 10 | PMIC_CLKOUT | Dithered clock input to PMIC | O | | |
| EA68h | PMIC_CLKOUT | P13 | 0 | GPIO_27 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | PMIC_CLKOUT | Dithered Clock Output for PMIC | O | | |
| | | | | SOP2 | Sense On Power [Reset] Line Impacts boot mode | I | | |
| EA6Ch | SYNC_IN | N10 | 0 | GPIO_28 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | SYNC_IN | Low frequency Synchronization signal input | I | | |
| | | | 6 | MSS_UARTB_RX | Debug: Firmware Trace | I | | |
| EA70h | SYNC_OUT | P11 | 0 | GPIO_29 | General Purpose IO | IO | Hi-Z | Weak Pull Down |
| | | | 1 | SYNC_OUT | Low frequency Synchronization signal output | O | | |
| | | | | RCOSC_CLK | | O | | |
| | | | | SOP1 | Sense On Power [Reset] Line Impacts boot mode | I | | |
| EA74h | RS232_RX | N5 | 0 | GPIO_15 | General Purpose IO | IO | Hi-Z | Weak Pull Up |
| | | | 1 | RS232_RX | Debug: Firmware load to RAM | IO | | |
| | | | 2 | MSS_UARTA_RX | FLASH Programming Bootloader Controlled | I | | |
| | | | 6 | BSS_UART_TX | Debug: Firmware Trace | O | | |
| | | | 7 | MSS_UARTB_RX | Debug: Firmware Trace | I | | |

Table 4-2. Pin Multiplexing (continued)

| REGISTER ADDRESS ⁽¹⁾ | PIN NAME | PIN | DIGITAL PIN MUX CONFIG VALUE [Bits3:0] | FUNCTION | | | PAD STATE nReset = 0 [ASSERTED] | |
|---------------------------------|----------|-----|--|--------------|---|-------------|------------------------------------|--------------------------|
| | | | | SIGNAL NAME | SIGNAL DESCRIPTION | SIGNAL TYPE | STATE | INTERNAL WEAK PULL STATE |
| EA78h | RS232_TX | N6 | 0 | GPIO_14 | General Purpose IO | IO | | |
| | | | 1 | RS232_TX | Debug: Firmware load to RAM | IO | | |
| | | | 5 | MSS_UARTA_TX | FLASH Programming Bootloader Controlled | O | | |
| | | | 6 | MSS_UARTB_TX | Debug: Firmware Trace | O | | |
| | | | 7 | BSS_UART_TX | Debug: Firmware Trace | O | | |

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | MIN | MAX | UNIT |
|--------------------------------|---|--|-------------|------|
| VDDIN | 1.2 V digital power supply | -0.5 | 1.4 | V |
| VIN_SRAM | 1.2 V power rail for internal SRAM | -0.5 | 1.4 | V |
| VNWA | 1.2 V power rail for SRAM array back bias | -0.5 | 1.4 | V |
| VIOIN | I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply. | -0.5 | 3.8 | V |
| VIOIN_18 | 1.8 V supply for CMOS IO | -0.5 | 2 | V |
| VIN_18CLK | 1.8 V supply for clock module | -0.5 | 2 | V |
| VIN_13RF1 | 1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board. | -0.5 | 1.45 | V |
| VIN_13RF2 | | | | |
| VIN_13RF1 | 1-V Internal LDO bypass mode. Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed. | -0.5 | 1.4 | V |
| VIN_13RF2 | | | | |
| VIN_18BB | 1.8-V Analog baseband power supply | -0.5 | 2 | V |
| VIN_18VCO supply | 1.8-V RF VCO supply | -0.5 | 2 | V |
| Input and output voltage range | Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State) | -0.3V | VIOIN + 0.3 | V |
| | Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input | VIOIN + 20% up to 20% of signal period | | |
| CLKP, CLKM | Input ports for reference crystal | -0.5 | 2 | V |
| Clamp current | Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O. | -20 | 20 | mA |
| T _J | Operating junction temperature range | -40 | 125 | °C |
| T _{STG} | Storage temperature range after soldered onto PC board | -55 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V_{SS}, unless otherwise noted.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 |
| | | Charged-device model (CDM), per AEC Q100-011 ⁽²⁾ | ±500 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) Corner pins are rated as ±750 V

5.3 Power-On Hours (POH)⁽¹⁾

| JUNCTION TEMPERATURE (T _J) | OPERATING CONDITION | NOMINAL CVDD VOLTAGE (V) | POWER-ON HOURS [POH] (HOURS) |
|--|---------------------|--------------------------|------------------------------|
| -40°C | 100% duty cycle | 1.2 | 600 (6%) |
| 75°C | | | 2000 (20%) |
| 95°C | | | 6500 (65%) |
| 125°C | | | 900 (9%) |

- (1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|-------------|-----|-----------|------|
| VDDIN | 1.2 V digital power supply | 1.14 | 1.2 | 1.32 | V |
| VIN_SRAM | 1.2 V power rail for internal SRAM | 1.14 | 1.2 | 1.32 | V |
| VNWA | 1.2 V power rail for SRAM array back bias | 1.14 | 1.2 | 1.32 | V |
| VIOIN | I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply. | 3.15 | 3.3 | 3.45 | V |
| | | 1.71 | 1.8 | 1.89 | |
| VIOIN_18 | 1.8 V supply for CMOS IO | 1.71 | 1.8 | 1.9 | V |
| VIN_18CLK | 1.8 V supply for clock module | 1.71 | 1.8 | 1.9 | V |
| VIN_13RF1 | 1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board | 1.23 | 1.3 | 1.36 | V |
| VIN_13RF2 | | | | | |
| VIN_13RF1 (1-V Internal LDO bypass mode) | | 0.95 | 1 | 1.05 | V |
| VIN_13RF2 (1-V Internal LDO bypass mode) | | | | | |
| VIN18BB | 1.8-V Analog baseband power supply | 1.71 | 1.8 | 1.9 | V |
| VIN_18VCO | 1.8V RF VCO supply | 1.71 | 1.8 | 1.9 | V |
| V _{IH} | Voltage Input High (1.8 V mode) | 1.17 | | | V |
| | Voltage Input High (3.3 V mode) | 2.25 | | | |
| V _{IL} | Voltage Input Low (1.8 V mode) | | | 0.3*VIOIN | V |
| | Voltage Input Low (3.3 V mode) | | | 0.62 | |
| V _{OH} | High-level output threshold (I _{OH} = 6 mA) | VIOIN – 450 | | | mV |
| V _{OL} | Low-level output threshold (I _{OL} = 6 mA) | | | | 450 |
| NRESET SOP[2:0] | V _{IL} (1.8V Mode) | | | 0.2 | V |
| | V _{IH} (1.8V Mode) | 0.96 | | | |
| | V _{IL} (3.3V Mode) | | | 0.3 | |
| | V _{IH} (3.3V Mode) | 1.57 | | | |

5.5 Power Supply Specifications

Table 5-1 describes the four rails from an external power supply block of the AWR1443 device.

Table 5-1. Power Supply Rails Characteristics

| SUPPLY | DEVICE BLOCKS POWERED FROM THE SUPPLY | RELEVANT IOS IN THE DEVICE |
|---|---|---|
| 1.8 V | Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, LVDS | Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL |
| 1.3 V (or 1 V in internal LDO bypass mode) ⁽¹⁾ | Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution | Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA |
| 3.3 V (or 1.8 V for 1.8 V I/O mode) | Digital I/Os | Input VIOIN |
| 1.2 V | Core Digital and SRAMs | Input: VDDIN, VIN_SRAM |

(1) Three simultaneous transmitter operation is supported only in 1-V LDO bypass mode.

The 1.3V (1.0V) and 1.8V power supply ripple specifications mentioned in are defined to meet a target spur level of -105dBc (RF Pin = -15dBm) at the RX. The spur and ripple levels have a dB to dB relationship, for example, a 1dB increase in supply ripple leads to a $\sim 1\text{dB}$ increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

5.6 Power Consumption Summary

Table 5-2 and Table 5-3 summarize the power consumption at the power terminals.

Table 5-2. Maximum Current Ratings at Power Terminals

| PARAMETER | SUPPLY NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---------------------|--|---|-----|-----|------|------|
| Current consumption | VDDIN, VIN_SRAM, VNWA | Total current drawn by all nodes driven by 1.2V rail | | | 500 | mA |
| | VIN_13RF1, VIN_13RF2 | Total current drawn by all nodes driven by 1.3V rail ⁽¹⁾ | | | 2000 | |
| | VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO | Total current drawn by all nodes driven by 1.8V rail | | | 850 | |
| | VIOIN | Total current drawn by all nodes driven by 3.3V rail | | | 50 | |

(1) 3 Transmitters can simultaneously be deployed only in AWR1243P device with 1V / LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin. In this case the peak 1V supply current goes up to 2500 mA.

Table 5-3. Average Power Consumption at Power Terminals

| PARAMETER | CONDITION | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---------------------------|---------------------------------|----------|-------------|-----|------|-----|------|
| Average power consumption | 1.0-V internal LDO bypass mode | 1TX, 4RX | | | 1.72 | | W |
| | | 2TX, 4RX | | | 1.89 | | |
| | 1.3-V internal LDO enabled mode | 1TX, 4RX | | | 1.9 | | |
| | | 2TX, 4RX | | | 2.1 | | |

5.7 RF Specification

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT | |
|--------------------|---|------------------|--|------|---------------|--------|
| Receiver | Noise figure | 76 to 77 GHz | 14 | | dB | |
| | | 77 to 81 GHz | 15 | | | |
| | 1-dB compression point (Out Of Band) ⁽¹⁾ | | | -8 | | dBm |
| | Maximum gain | | | 48 | | dB |
| | Gain range | | | 24 | | dB |
| | Gain step size | | | 2 | | dB |
| | Image Rejection Ratio (IMRR) | | | 30 | | dB |
| | IF bandwidth ⁽²⁾ | | | | 5 | MHz |
| | A2D sampling rate (real) | | | | 12.5 | MSPS |
| | A2D sampling rate (complex) | | | | 6.25 | MSPS |
| | A2D resolution | | | 12 | | Bits |
| | Return loss (S11) | | | <-10 | | dB |
| | Gain mismatch variation (over temperature) | | | ±0.5 | | dB |
| | Phase mismatch variation (over temperature) | | | ±3 | | ° |
| | Receiver | In-band IIP2 | RX gain = 30dB IF = 1.5, 2 MHz at -12 dBFS | 16 | | dBm |
| | | Out-of-band IIP2 | RX gain = 24dB IF = 10 kHz at -10dBm, 1.9 MHz at -30 dBm | 24 | | dBm |
| Idle Channel Spurs | | | -90 | | dBFS | |
| Transmitter | Output power | | 12 | | dBm | |
| | Amplitude noise | | | -145 | | dBc/Hz |
| Clock subsystem | Frequency range | | 76 | | 81 GHz | |
| | Ramp rate | | | | 100 MHz/μs | |
| | Phase noise at 1-MHz offset | 76 to 77 GHz | | -95 | | dBc/Hz |
| 77 to 81 GHz | | | -93 | | | |

- (1) 1-dB Compression Point (Out Of Band) is measured by feed a Continuous wave Tone below the lowest HPF cut-off frequency (50 kHz).
 (2) The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

| | |
|--|----------------------|
| Available HPF Corner Frequencies (kHz) | |
| HPF1 | HPF2 |
| 175, 235, 350, 700 | 350, 700, 1400, 2800 |

The filtering performed by the digital baseband chain is targeted to provide:

- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

Figure 5-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

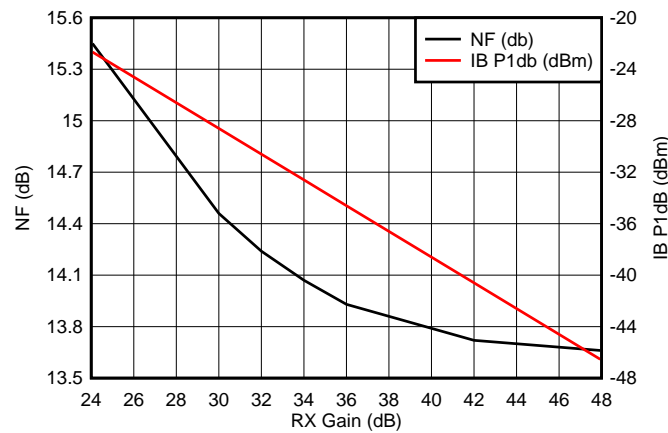


Figure 5-1. Noise Figure, In-band P1dB vs Receiver Gain

5.8 Thermal Resistance Characteristics for FCBGA Package [ABL0161]⁽¹⁾

| THERMAL METRICS ⁽²⁾ | | °C/W ^{(3) (4)} |
|--------------------------------|-------------------------|-------------------------|
| R θ_{JC} | Junction-to-case | 4.92 |
| R θ_{JB} | Junction-to-board | 6.57 |
| R θ_{JA} | Junction-to-free air | 22.3 |
| R θ_{JMA} | Junction-to-moving air | N/A ⁽¹⁾ |
| Psi $_{JT}$ | Junction-to-package top | 4.92 |
| Psi $_{JB}$ | Junction-to-board | 6.4 |

(1) N/A = not applicable

(2) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(3) °C/W = degrees Celsius per watt.

(4) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

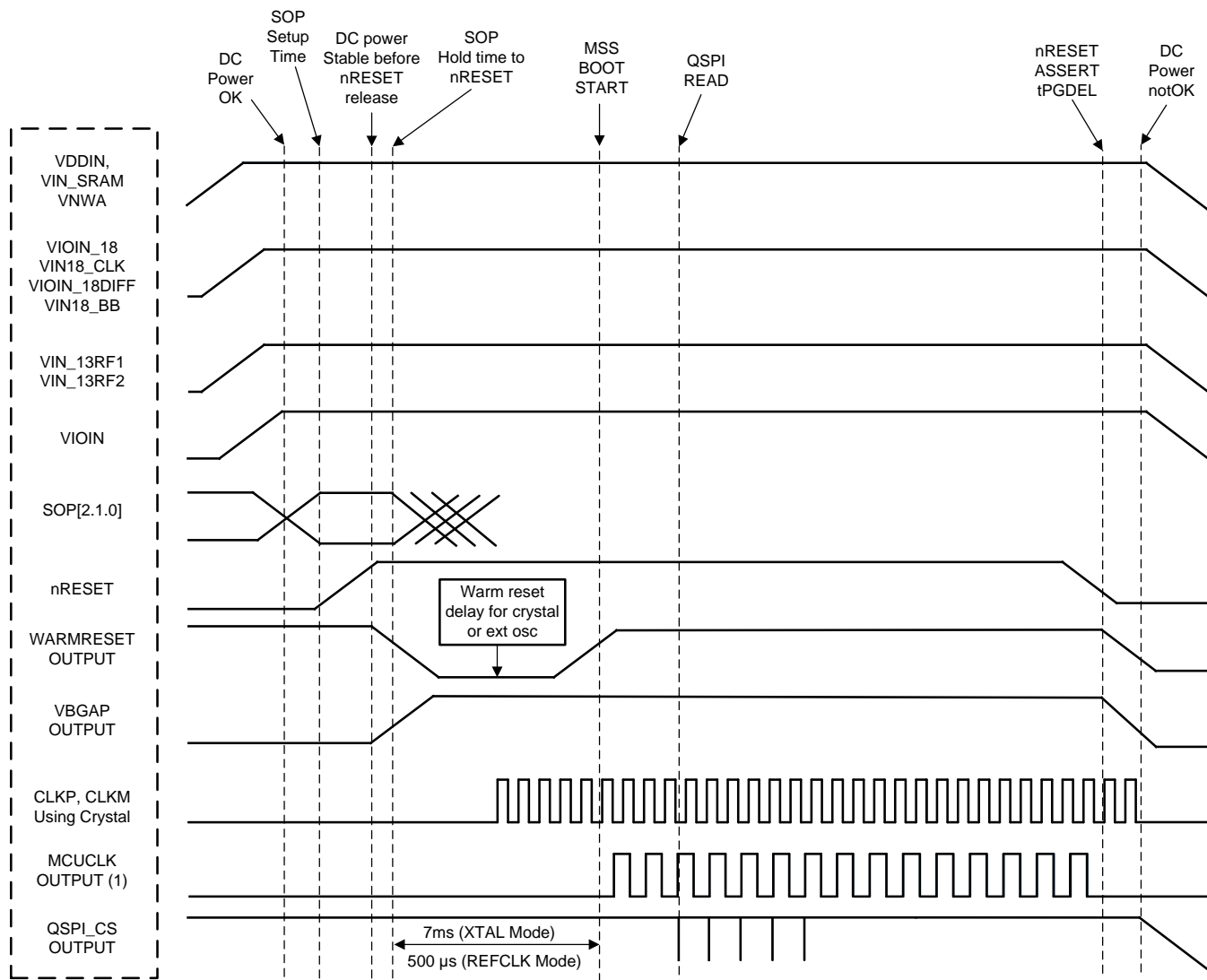
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

A junction temperature of 125°C is assumed.

5.9 Timing and Switching Characteristics

5.9.1 Power Supply Sequencing and Reset Timing

The AWR1443 device expects all external voltage rails to be stable before reset is deasserted. Figure 5-2 describes the device wake-up sequence.



(1) MCU_CLK_OUT in autonomous mode, where AWR1443 application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

Figure 5-2. Device Wake-up Sequence

5.9.2 Synchronized Frame Triggering

The AWR1443 device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC_IN signal to start radar frames. The typical time difference between the rising edge of the external pulse and the frame transmission on air (Tlag) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time.

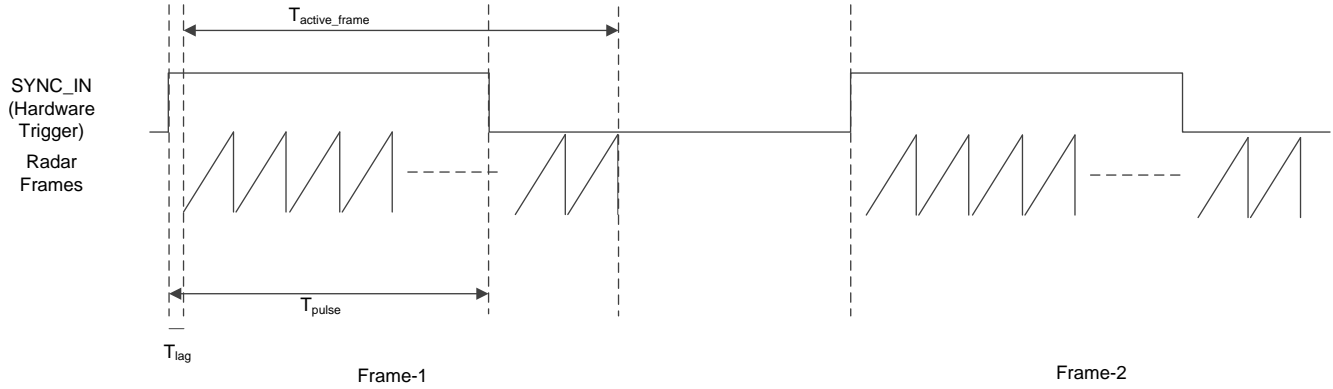


Figure 5-3. Sync In Hardware Trigger

Table 5-4. Frame Trigger Timing

| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---------------------|-----------------------|--------------|-----------------------|------|
| T_{active_frame} | Active frame duration | User defined | | ns |
| T_{pulse} | | 25 | $< T_{active_frame}$ | |

5.9.3 Input Clocks and Oscillators

5.9.3.1 Clock Specifications

An external crystal is connected to the device pins. Figure 5-4 shows the crystal implementation.

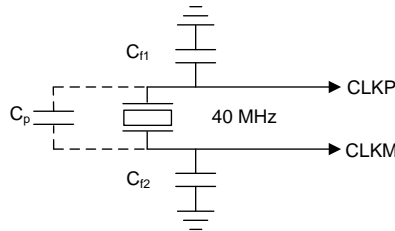


Figure 5-4. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 5-4, should be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins. Note that C_{f1} and C_{f2} include the parasitic capacitances due to PCB routing.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

Table 5-5 lists the electrical characteristics of the clock crystal.

Table 5-5. Crystal Electrical Characteristics (Oscillator Mode)

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---------------------|---|------|-----|-----|--------------------|
| f_p | Parallel resonance crystal frequency | | 40 | | MHz |
| C_L | Crystal load capacitance | 5 | 8 | 12 | pF |
| ESR | Crystal ESR | | | 50 | Ω |
| Temperature range | Expected temperature range of operation | -40 | | 150 | $^{\circ}\text{C}$ |
| Frequency tolerance | Crystal frequency tolerance ⁽¹⁾⁽²⁾ | -200 | | 200 | ppm |
| Drive level | | | 50 | 200 | μW |

(1) The crystal manufacturer's specification must satisfy this requirement.

(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

Table 5-6. External Clock Mode Specifications

| PARAMETER | SPECIFICATION | | | UNIT | |
|---|----------------------------|-----|-----|------|---------|
| | MIN | TYP | MAX | | |
| Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40 MHz | Frequency | | 40 | | MHz |
| | AC-Amplitude | 700 | | 1200 | mV (pp) |
| | DC- $t_{\text{rise/fall}}$ | | | 10 | ns |
| | Phase Noise at 1 kHz | | | -132 | dBc/Hz |
| | Phase Noise at 10 kHz | | | -143 | dBc/Hz |
| | Phase Noise at 100 kHz | | | -152 | dBc/Hz |
| | Phase Noise at 1 MHz | | | -153 | dBc/Hz |
| | Duty Cycle | 35 | | 65 | % |
| | Freq Tolerance | -50 | | 50 | ppm |

5.9.4 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

5.9.4.1 Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format.
- SPI I/Os not used in the communication can be used as digital input/output signals

5.9.4.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 256 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

[Table 5-8](#) to assume the operating conditions stated in [Table 5-7](#).

Table 5-7. SPI Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input rise time | 1 | | 3 | ns |
| t_F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C_{LOAD} | Output load capacitance | 2 | | 15 | pF |

Table 5-8. SPI Master Mode Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------|----------------------|--|--|--|--------------------------------|------|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK ⁽⁴⁾ | 25 | | $256t_{c(VCLK)}$ | ns |
| 2 ⁽⁴⁾ | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 3 ⁽⁴⁾ | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 4 ⁽⁴⁾ | $t_{d(SPCH-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0) | $0.5t_{c(SPC)M} - 3$ | | | ns |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1) | $0.5t_{c(SPC)M} - 3$ | | | |
| 5 ⁽⁴⁾ | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0) | $0.5t_{c(SPC)M} - 10.5$ | | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1) | $0.5t_{c(SPC)M} - 10.5$ | | | |
| 6 ⁽⁵⁾ | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | CSHOLD = 0 | $(C2TDELAY+2)*t_{c(VCLK)} - 7.5$ | $(C2TDELAY+2)*t_{c(VCLK)} + 7$ | ns |
| | | | CSHOLD = 1 | $(C2TDELAY+3)*t_{c(VCLK)} - 7.5$ | $(C2TDELAY+3)*t_{c(VCLK)} + 7$ | |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | CSHOLD = 0 | $(C2TDELAY+2)*t_{c(VCLK)} - 7.5$ | $(C2TDELAY+2)*t_{c(VCLK)} + 7$ | |
| | | | CSHOLD = 1 | $(C2TDELAY+3)*t_{c(VCLK)} - 7.5$ | $(C2TDELAY+3)*t_{c(VCLK)} + 7$ | |
| 7 ⁽⁵⁾ | $t_{T2CDELAY}$ | Hold time, SPICLK low until CS inactive (clock polarity = 0) | $0.5*t_{c(SPC)M} + (T2CDELAY + 1)*t_{c(VCLK)} - 7$ | $0.5*t_{c(SPC)M} + (T2CDELAY + 1)*t_{c(VCLK)} + 7.5$ | ns | |
| | | Hold time, SPICLK high until CS inactive (clock polarity = 1) | $0.5*t_{c(SPC)M} + (T2CDELAY + 1)*t_{c(VCLK)} - 7$ | $0.5*t_{c(SPC)M} + (T2CDELAY + 1)*t_{c(VCLK)} + 7.5$ | | |
| 8 ⁽⁴⁾ | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 0) | 5 | | | ns |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 1) | 5 | | | |
| 9 ⁽⁴⁾ | $t_{h(SPCL-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0) | 3 | | | ns |
| | $t_{h(SPCH-SOMI)M}$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1) | 3 | | | |

- (1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
- (2) $t_{c(MSS_VCLK)}$ = master subsystem clock time = $1 / f_{(MSS_VCLK)}$. For more details, see the [Technical Reference Manual](#).
- (3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(MSS_VCLK)} \geq 25ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25ns$.
- (4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
- (5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

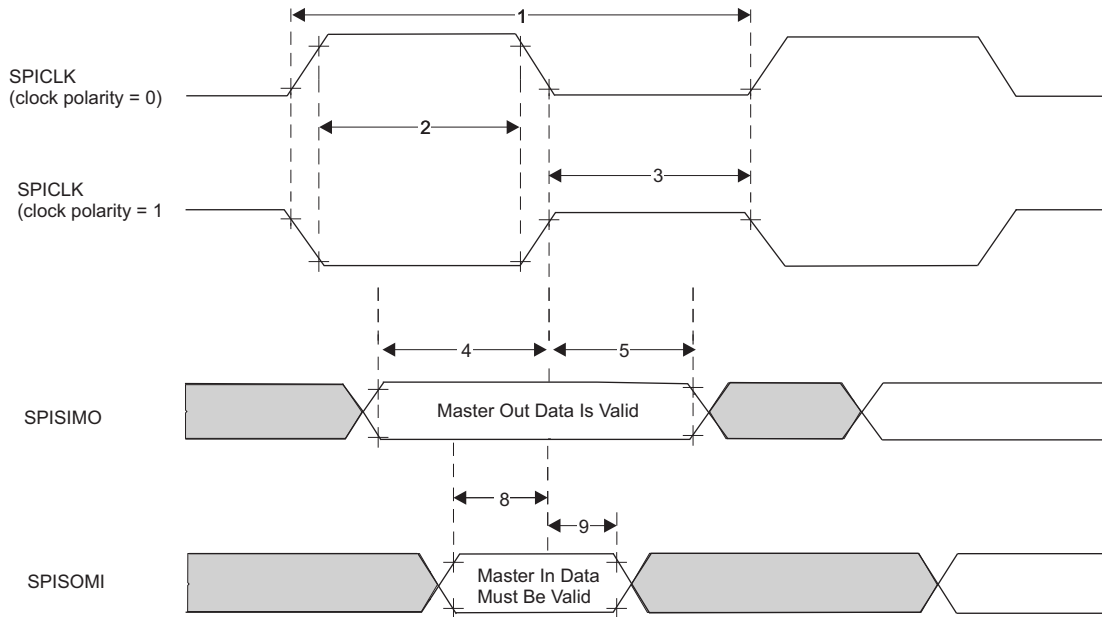


Figure 5-5. SPI Master Mode External Timing (CLOCK PHASE = 0)

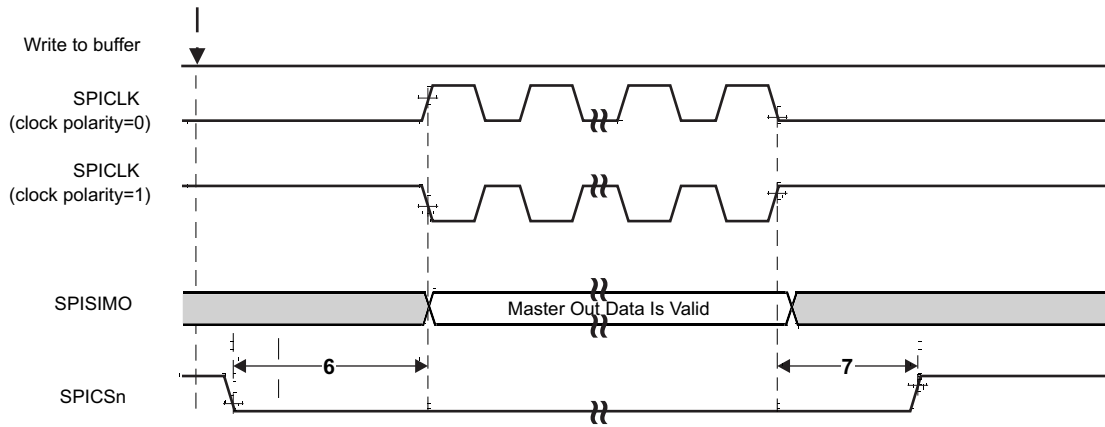


Figure 5-6. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

Table 5-9. SPI Master Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------|----------------------|--|--------------------------------------|--|--|------|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK ⁽⁴⁾ | 25 | | $256t_{c(VCLK)}$ | ns |
| 2 ⁽⁴⁾ | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 3 ⁽⁴⁾ | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 4 ⁽⁴⁾ | $t_{d(SPCH-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0) | $0.5t_{c(SPC)M} - 3$ | | | ns |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1) | $0.5t_{c(SPC)M} - 3$ | | | |
| 5 ⁽⁴⁾ | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0) | $0.5t_{c(SPC)M} - 10.5$ | | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1) | $0.5t_{c(SPC)M} - 10.5$ | | | |
| 6 ⁽⁵⁾ | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | CSHOLD = 0 | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} - 7$ | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} + 7.5$ | ns |
| | | | CSHOLD = 1 | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} - 7$ | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} + 7.5$ | |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | CSHOLD = 0 | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} - 7$ | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} + 7.5$ | |
| | | | CSHOLD = 1 | $0.5 * t_{c(SPC)M} + (C2TDELAY + 3) * t_{c(VCLK)} - 7$ | $0.5 * t_{c(SPC)M} + (C2TDELAY + 3) * t_{c(VCLK)} + 7.5$ | |
| 7 ⁽⁵⁾ | $t_{T2CDELAY}$ | Hold time, SPICLK low until CS inactive (clock polarity = 0) | $(T2CDELAY + 1) * t_{c(VCLK)} - 7.5$ | $(T2CDELAY + 1) * t_{c(VCLK)} + 7$ | ns | |
| | | Hold time, SPICLK high until CS inactive (clock polarity = 1) | $(T2CDELAY + 1) * t_{c(VCLK)} - 7.5$ | $(T2CDELAY + 1) * t_{c(VCLK)} + 7$ | | |
| 8 ⁽⁴⁾ | $t_{su(SOMI-SPCL)M}$ | Setup time, SPISOMI before SPICLK low (clock polarity = 0) | 5 | | | ns |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPISOMI before SPICLK high (clock polarity = 1) | 5 | | | |
| 9 ⁽⁴⁾ | $t_h(SPCL-SOMI)M$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0) | 3 | | | ns |
| | $t_h(SPCH-SOMI)M$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1) | 3 | | | |

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set (where x = 0 or 1).
(2) $t_{c(MSS_VCLK)}$ = master subsystem clock time = $1 / f_{(MSS_VCLK)}$. For more details, see the [Technical Reference Manual](#).
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

5.9.4.3 SPI Slave Mode I/O Timings

Table 5-10. SPI Slave Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------|----------------------|--|-----|-----|-----|------|
| 1 | $t_{c(SPC)}S$ | Cycle time, SPICLK ⁽⁴⁾ | 25 | | | ns |
| 2 ⁽⁵⁾ | $t_{w(SPCH)}S$ | Pulse duration, SPICLK high (clock polarity = 0) | 10 | | | ns |
| | $t_{w(SPCL)}S$ | Pulse duration, SPICLK low (clock polarity = 1) | 10 | | | |
| 3 ⁽⁵⁾ | $t_{w(SPCL)}S$ | Pulse duration, SPICLK low (clock polarity = 0) | 10 | | | ns |
| | $t_{w(SPCH)}S$ | Pulse duration, SPICLK high (clock polarity = 1) | 10 | | | |
| 4 ⁽⁵⁾ | $t_{d(SPCH-SOMI)}S$ | Delay time, SPISOMI valid after SPICLK high (clock polarity = 0) | | | 10 | ns |
| | $t_{d(SPCL-SOMI)}S$ | Delay time, SPISOMI valid after SPICLK low (clock polarity = 1) | | | 10 | |
| 5 ⁽⁵⁾ | $t_{h(SPCH-SOMI)}S$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0) | 2 | | | ns |
| | $t_{h(SPCL-SOMI)}S$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1) | 2 | | | |
| 4 ⁽⁵⁾ | $t_{d(SPCH-SOMI)}S$ | Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | | | 10 | ns |
| | $t_{d(SPCL-SOMI)}S$ | Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | | | 10 | |
| 5 ⁽⁵⁾ | $t_{h(SPCH-SOMI)}S$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | 2 | | | ns |
| | $t_{h(SPCL-SOMI)}S$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | 2 | | | |
| 6 ⁽⁵⁾ | $t_{su(SIMO-SPCL)}S$ | Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | 3 | | | ns |
| | $t_{su(SIMO-SPCH)}S$ | Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | 3 | | | |
| 7 ⁽⁵⁾ | $t_{h(SPCL-SIMO)}S$ | Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | 1 | | | ns |
| | $t_{h(SPCL-SIMO)}S$ | Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | 1 | | | |

(1) The MASTER bit (SPIGCRx.0) is cleared (where x = 0 or 1).

(2) The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.

(3) $t_{c(MSS_VCLK)}$ = master subsystem clock time = $1 / f_{(MSS_VCLK)}$. For more details, see the [Technical Reference Manual](#).

(4) When the SPI is in Slave mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)}S \geq (PS + 1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)}S = 2t_{c(MSS_VCLK)} \geq 25$ ns.

(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

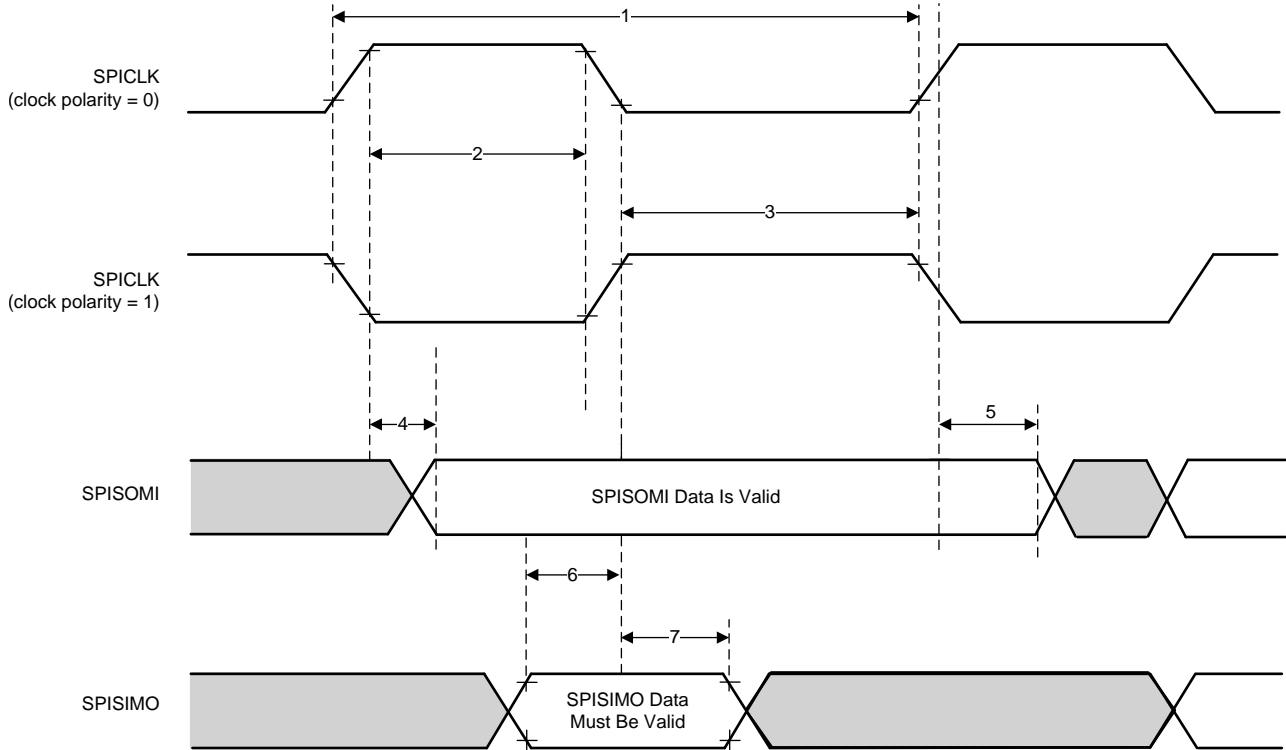


Figure 5-9. SPI Slave Mode External Timing (CLOCK PHASE = 0)

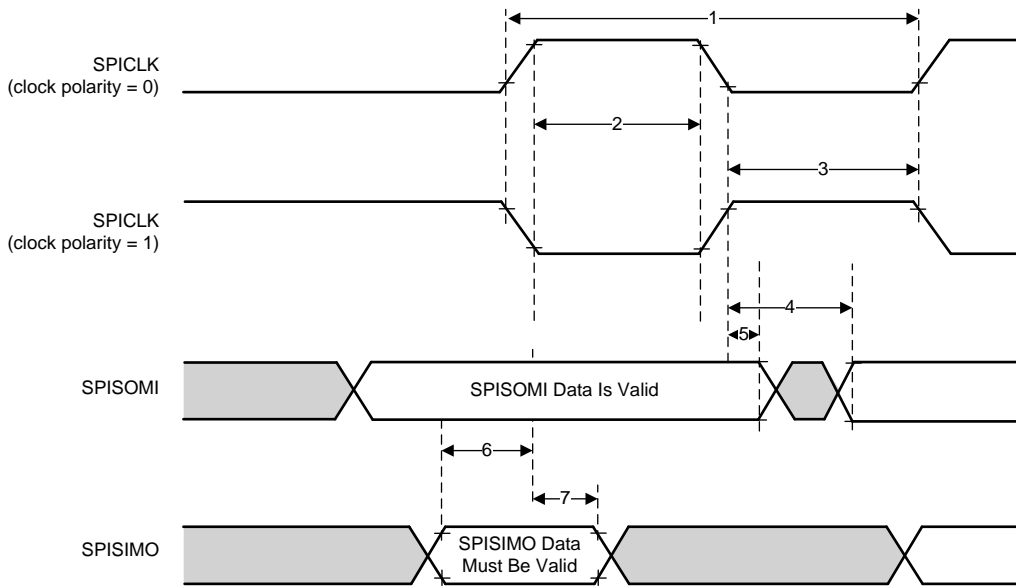


Figure 5-10. SPI Slave Mode External Timing (CLOCK PHASE = 1)

5.9.4.4 Typical Interface Protocol Diagram (Slave Mode)

1. Host should ensure that there is a delay of two SPI clocks between CS going low and start of SPI clock.
2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

Figure 5-11 shows the SPI communication timing of the typical interface protocol.

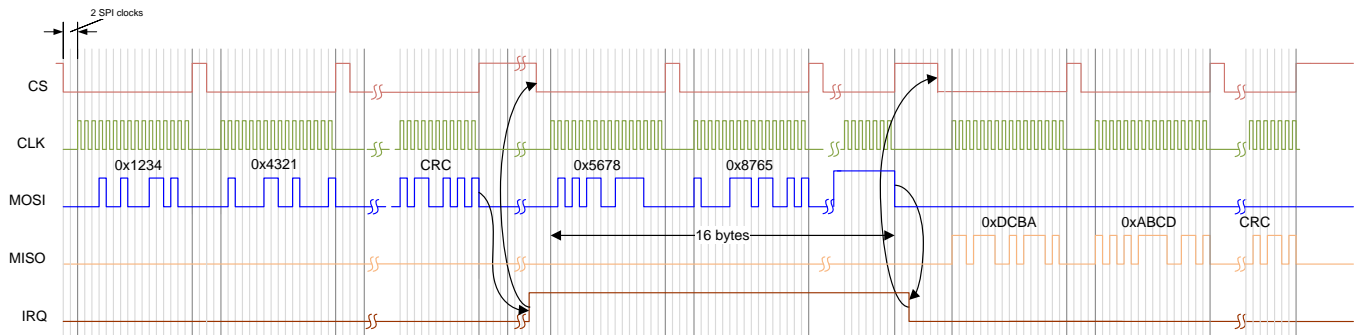


Figure 5-11. SPI Communication

5.9.5 LVDS Interface Configuration

The AWR1443 supports seven differential LVDS IOs/Lanes. The lane configuration supported is four Data lanes (LVDS_TXP/M), one Bit Clock lane (LVDS_CLKP/M) and one Frame clock lane (LVDS_FRCLKP/M), and one HS_DEBUG LVDS pair. The LVDS interface is used for debugging. The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

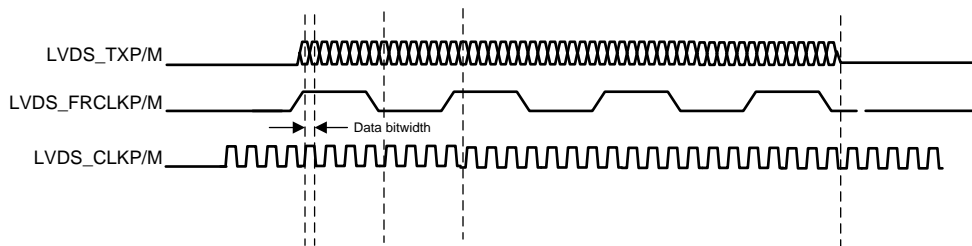


Figure 5-12. LVDS Interface Lane Configuration And Relative Timings

5.9.5.1 LVDS Interface Timings

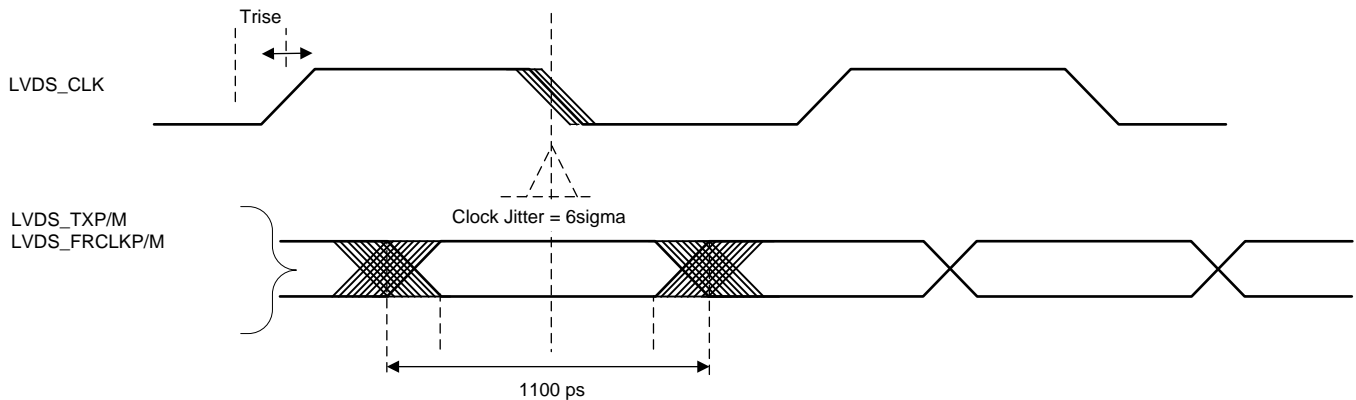


Figure 5-13. Timing Parameters

Table 5-11. LVDS Electrical Characteristics

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|---|------|-----|------|------|
| Duty Cycle Requirements | max 1 pF lumped capacitive load on LVDS lanes | 48% | | 52% | |
| Output Differential Voltage | peak-to-peak single-ended with 100 Ω resistive load between differential pairs | 250 | | 450 | mV |
| Output Offset Voltage | | 1125 | | 1275 | mV |
| Trise and Tfall | 20%-80%, 900 Mbps | | 330 | | ps |
| Jitter (pk-pk) | 900 Mbps | | 80 | | ps |

5.9.6 General-Purpose Input/Output

Table 5-12 lists the switching characteristics of output timing relative to load capacitance.

Table 5-12. Switching Characteristics for Output Timing versus Load Capacitance (C_L)⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITIONS | VIOIN = 1.8V | VIOIN = 3.3V | UNIT | |
|-----------|---------------|------------------|---------------|--------------|------|----|
| t_r | Max rise time | Slew control = 0 | $C_L = 20$ pF | 2.8 | 3.0 | ns |
| | | | $C_L = 50$ pF | 6.4 | 6.9 | |
| | | | $C_L = 75$ pF | 9.4 | 10.2 | |
| t_f | Max fall time | | $C_L = 20$ pF | 2.8 | 2.8 | ns |
| | | | $C_L = 50$ pF | 6.4 | 6.6 | |
| | | | $C_L = 75$ pF | 9.4 | 9.8 | |
| t_r | Max rise time | Slew control = 1 | $C_L = 20$ pF | 3.3 | 3.3 | ns |
| | | | $C_L = 50$ pF | 6.7 | 7.2 | |
| | | | $C_L = 75$ pF | 9.6 | 10.5 | |
| t_f | Max fall time | | $C_L = 20$ pF | 3.1 | 3.1 | ns |
| | | | $C_L = 50$ pF | 6.6 | 6.6 | |
| | | | $C_L = 75$ pF | 9.6 | 9.6 | |

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).

(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

5.9.7 Controller Area Network Interface (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for applications operating in noisy and harsh environments that require reliable serial communication or multiplexed wiring.

The DCAN has the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 Mbps
- Configurable Message objects
- Individual identifier masks for each message object
- Programmable FIFO mode for message objects
- Suspend mode for debug support
- Programmable loop-back modes for self-test operation
- Direct access to Message RAM in test mode
- Supports two interrupt lines - Level 0 and Level 1
- Automatic Message RAM initialization

Table 5-13. Dynamic Characteristics for the DCANx TX and RX Pins

| PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------|--|-----|-----|-----|------|
| $t_{d(CAN_tx)}$ | Delay time, transmit shift register to CAN_tx pin ⁽¹⁾ | | | 15 | ns |
| $t_{d(CAN_rx)}$ | Delay time, CAN_rx pin to receive shift register ⁽¹⁾ | | | 10 | ns |

(1) These values do not include rise/fall times of the output buffer.

5.9.8 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Two external pins: RS232_RX and RS232_TX

Table 5-14. SCI Timing Requirements

| | | MIN | TYP | MAX | UNIT |
|---------|------------------------------|-----|-------|-----|------|
| f(baud) | Supported baud rate at 20 pF | | 921.6 | | kHz |

5.9.9 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multimaster communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I²C-bus™. This module will support any slave or master I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
 - Bit/Byte format transfer
 - 7-bit and 10-bit device addressing modes
 - General call
 - START byte
 - Multi-master transmitter/ slave receiver mode
 - Multi-master receiver/ slave transmitter mode
 - Combined master transmit/receive and receive/transmit mode
 - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

NOTE

This I2C module does not support:

- High-speed (HS) mode
 - C-bus compatibility mode
 - The combined format in 10-bit address mode (the I2C sends the slave address second byte every time it sends the slave address first byte)
-

Table 5-15. I2C Timing Requirements⁽¹⁾

| | | STANDARD MODE | | FAST MODE | | UNIT |
|---------------------|---|---------------|---------------------|-----------|-----|---------------|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | μs |
| $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | μs |
| $t_{h(SCLL-SDAL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | μs |
| $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | μs |
| $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | μs |
| $t_{su(SDA-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | μs |
| $t_{h(SCLL-SDA)}$ | Hold time, SDA valid after SCL low | 0 | 3.45 ⁽¹⁾ | 0 | 0.9 | μs |
| $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | μs |
| $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | μs |
| $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| $C_b^{(2)(3)}$ | Capacitive load for each bus line | | 400 | | 400 | pF |

- (1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
- (2) The maximum $t_h(SDA-SCLL)$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_w(SCLL)$) of the SCL signal.
- (3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

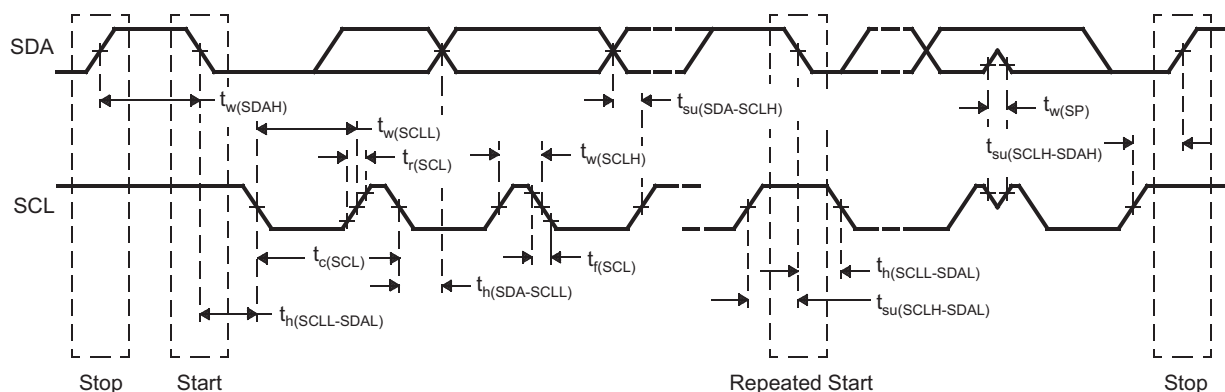


Figure 5-14. I2C Timing Diagram

NOTE

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_h(SDA-SCLL)$ has only to be met if the device does not stretch the LOW period ($t_w(SCLL)$) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r \max + t_{su(SDA-SCLH)}$.

5.9.10 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI™) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a master only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Support for 3-, 4-, or 6-pin SPI interface
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Table 5-17 and Table 5-18 assume the operating conditions stated in Table 5-16.

Table 5-16. QSPI Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input rise time | 1 | | 3 | ns |
| t_F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C_{LOAD} | Output load capacitance | 2 | | 15 | pF |

Table 5-17. Timing Requirements for QSPI Input (Read) Timings⁽¹⁾⁽²⁾

| | | MIN | TYP | MAX | UNIT |
|------------------|---|-----------------|-----|-----|------|
| $t_{su(D-SCLK)}$ | Setup time, d[3:0] valid before falling sclk edge (Q12) | 7.3 | | | ns |
| $t_{h(SCLK-D)}$ | Hold time, d[3:0] valid after falling sclk edge (Q13) | 1.5 | | | ns |
| $t_{su(D-SCLK)}$ | Setup time, final d[3:0] bit valid before final falling sclk edge | $7.3 - P^{(3)}$ | | | ns |
| $t_{h(SCLK-D)}$ | Hold time, final d[3:0] bit valid after final falling sclk edge | $1.5 + P^{(3)}$ | | | ns |

(1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.

(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.

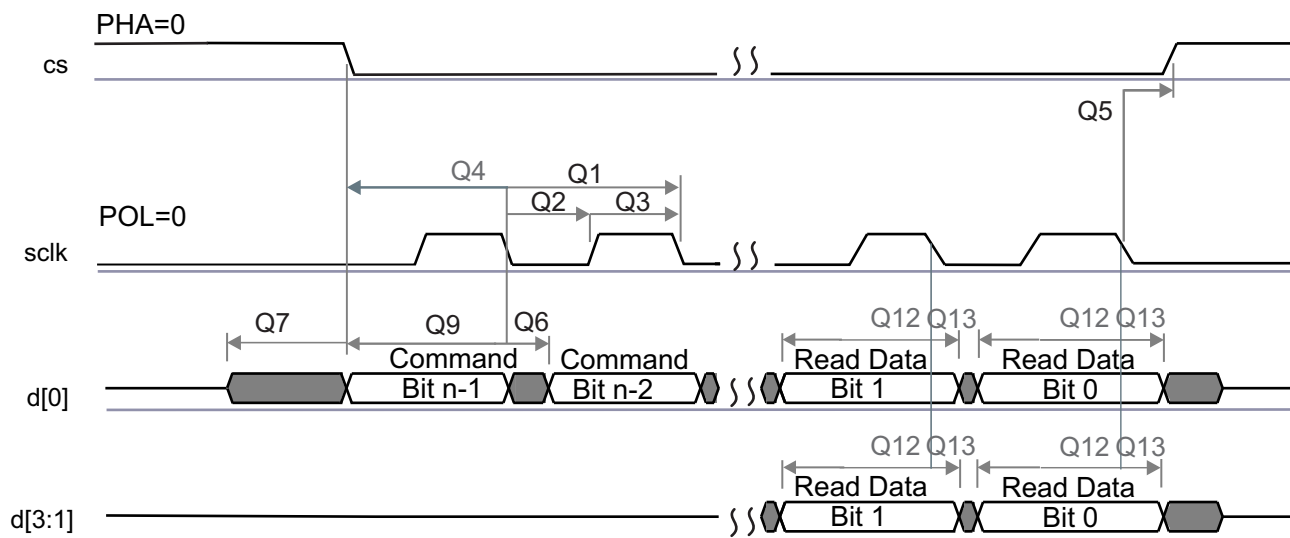
(3) P = SCLK period in ns.

Table 5-18. QSPI Switching Characteristics

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|--------------------|---|---------------------|-----|----------------------|------|
| Q1 | $t_{c(SCLK)}$ | Cycle time, sclk | 25 | | | ns |
| Q2 | $t_{w(SCLKL)}$ | Pulse duration, sclk low | $0.5 * P - 3^{(1)}$ | | | ns |
| Q3 | $t_{w(SCLKH)}$ | Pulse duration, sclk high | $0.5 * P - 3$ | | | ns |
| Q4 | $t_{d(CS-SCLK)}$ | Delay time, sclk falling edge to cs active edge | $-M * P - 1^{(2)}$ | | $-M * P + 2.5^{(2)}$ | ns |
| Q5 | $t_{d(SCLK-CS)}$ | Delay time, sclk falling edge to cs inactive edge | $N * P - 1^{(2)}$ | | $N * P + 2.5^{(2)}$ | ns |
| Q6 | $t_{d(SCLK-D1)}$ | Delay time, sclk falling edge to d[0] transition | -3.5 | | 7 | ns |
| Q7 | $t_{ena(CS-D1LZ)}$ | Enable time, cs active edge to d[0] driven (lo-z) | $-P - 4^{(2)}$ | | $-P + 1^{(2)}$ | ns |
| Q8 | $t_{dis(CS-D1Z)}$ | Disable time, cs active edge to d[0] tri-stated (hi-z) | $-P - 4^{(2)}$ | | $-P + 1^{(2)}$ | ns |
| Q9 | $t_{d(SCLK-D1)}$ | Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only) | $-3.5 - P^{(2)}$ | | $7 - P^{(2)}$ | ns |

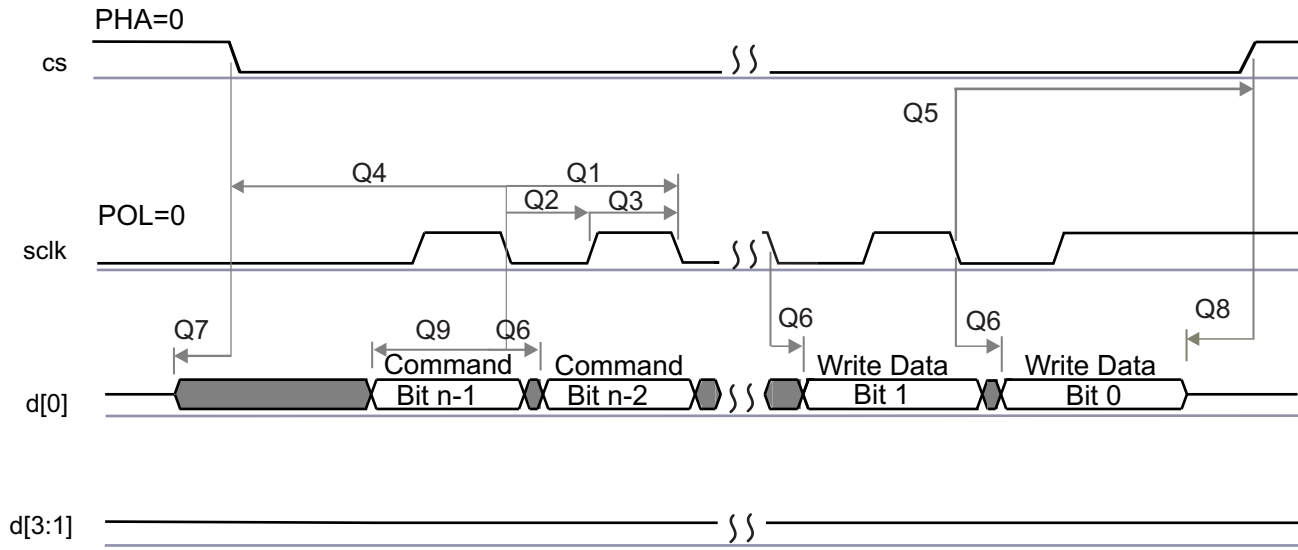
(1) P = SCLK period in ns.

(2) M = QSPI_SPI_DC_REG.DDx + 1, N = 2



SPRS85v_TIMING_OSP11_02

Figure 5-15. QSPI Read (Clock Mode 0)



SPRS85v_TIMING_OSP11_04

Figure 5-16. QSPI Write (Clock Mode 0)

5.9.11 JTAG Interface

Table 5-20 and Table 5-21 assume the operating conditions stated in Table 5-19.

Table 5-19. JTAG Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input rise time | 1 | | 3 | ns |
| t_F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C_{LOAD} | Output load capacitance | 2 | | 15 | pF |

Table 5-20. Timing Requirements for IEEE 1149.1 JTAG

| NO. | | | MIN | TYP | MAX | UNIT |
|-----|-------------------|---|-------|-----|-----|------|
| 1 | $t_c(TCK)$ | Cycle time TCK | 66.66 | | | ns |
| 1a | $t_w(TCKH)$ | Pulse duration TCK high (40% of t_c) | 26.67 | | | ns |
| 1b | $t_w(TCKL)$ | Pulse duration TCK low(40% of t_c) | 26.67 | | | ns |
| 3 | $t_{su}(TDI-TCK)$ | Input setup time TDI valid to TCK high | 2.5 | | | ns |
| | $t_{su}(TMS-TCK)$ | Input setup time TMS valid to TCK high | 2.5 | | | ns |
| 4 | $t_h(TCK-TDI)$ | Input hold time TDI valid from TCK high | 18 | | | ns |
| | $t_h(TCK-TMS)$ | Input hold time TMS valid from TCK high | 18 | | | ns |

Table 5-21. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|------------------|----------------------------------|-----|-----|-----|------|
| 2 | $t_d(TCKL-TDOV)$ | Delay time, TCK low to TDO valid | 0 | | 25 | ns |

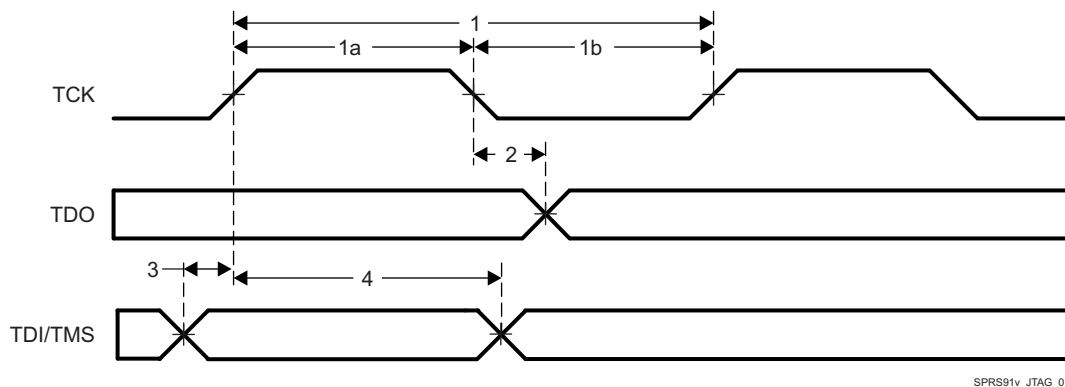


Figure 5-17. JTAG Timing

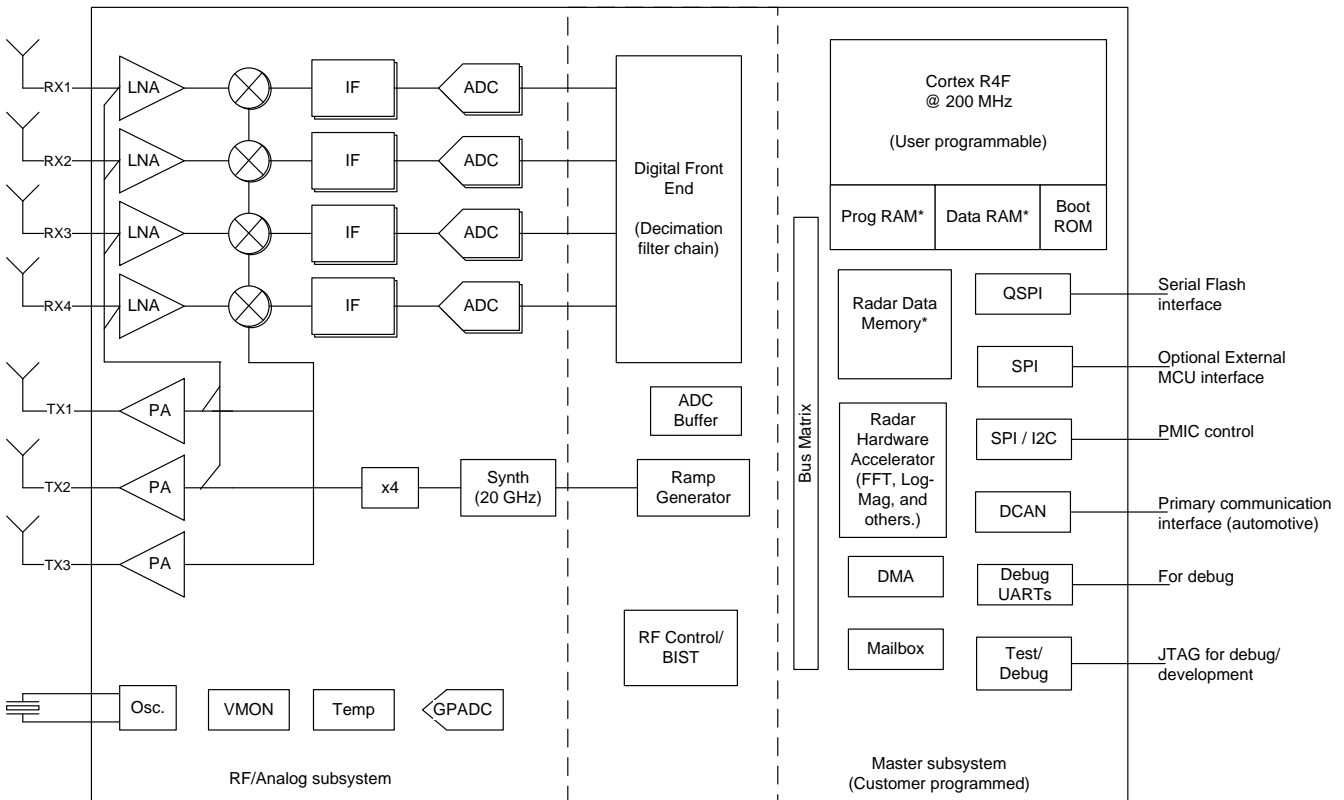
6 Detailed Description

6.1 Overview

The AWR1443 device includes the entire millimeter wave blocks and analog baseband signal chain for three transmitters (two usable at the same instance) and four receivers, as well as a customer-programmable MCU with a hardware accelerator for radar signal processing. This device is applicable as a radar-on-a-chip in use-cases with modest requirements for memory, processing capacity and application code size. These could be cost-sensitive automotive applications that are evolving from 24 GHz narrowband implementation and some emerging simple ultra-short-range radar applications. Typical application examples for this device include basic Blind Spot Detect, Parking Assist, and so forth.

In terms of scalability, the AWR1443 device could be paired with a low-end external MCU, to address more complex applications that might require additional memory for larger application software footprint and faster interfaces. Because the AWR1443 device also provides high speed data interfaces, it is suitable for interfacing with more capable external processing blocks. Here system designers can choose the AWR1443 to provide raw ADC data or use the on-chip Hardware Accelerator for partial processing viz. first stage Fast Fourier Transform.

6.2 Functional Block Diagram



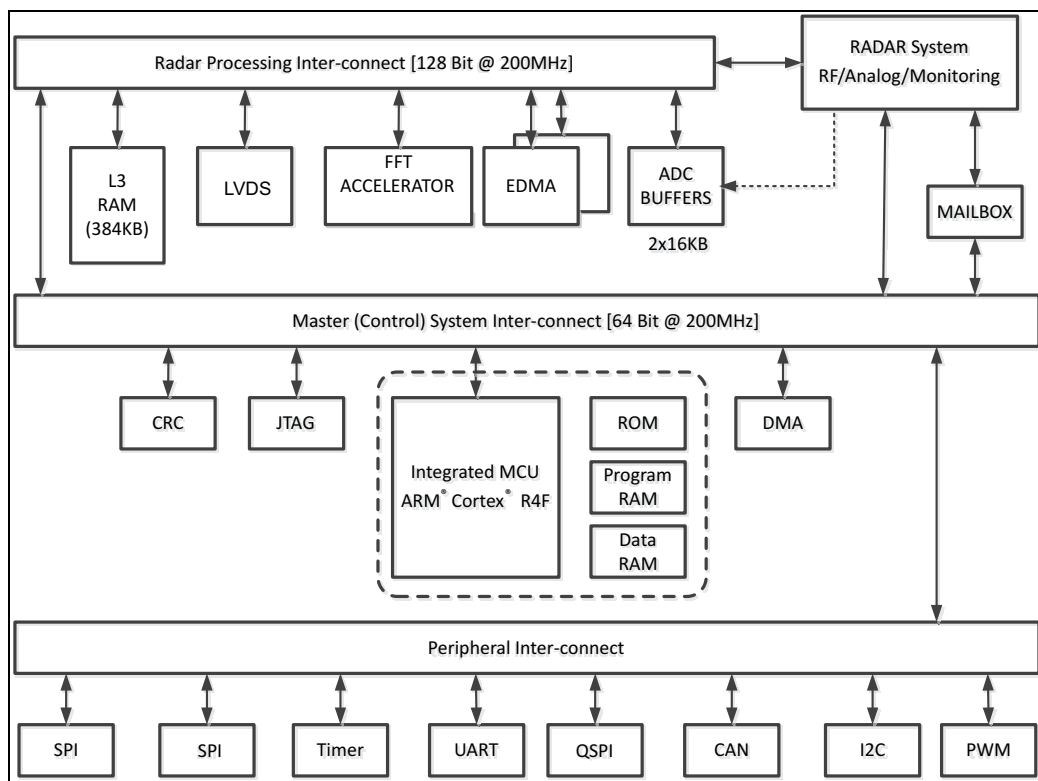
* Total RAM available in Master subsystem is 576KB (for Cortex-R4F Program RAM, Data RAM, and Radar Data Memory)

6.3 External Interfaces

The AWR1443 device provides the following external interfaces:

- Reference Clock – Reference clock available for Host Processor after device wakeup.
- Low speed control information
 - Up to two 4-line standard SPI interface
 - One I²C interface (Pin multiplexed with one of the SPI ports)
- One Controller Area Network (CAN) Port for Automotive Interfacing
- Reset – Active Low reset for device wakeup from host General Purpose IOs
- Error Signaling – Used for notifying the host in case the Radio Controller detects a fault

The AWR1443 device comprises of three main blocks – Radar (or the Millimeter Wave) System, Master (or the Control) System and Processing System.



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Figure 6-1. System Interconnect

6.4 Subsystems

6.4.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated up to a maximum of two at a time (simultaneously) for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

6.4.1.1 Clock Subsystem

The AWR1443 clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 6-2 describes the clock subsystem.

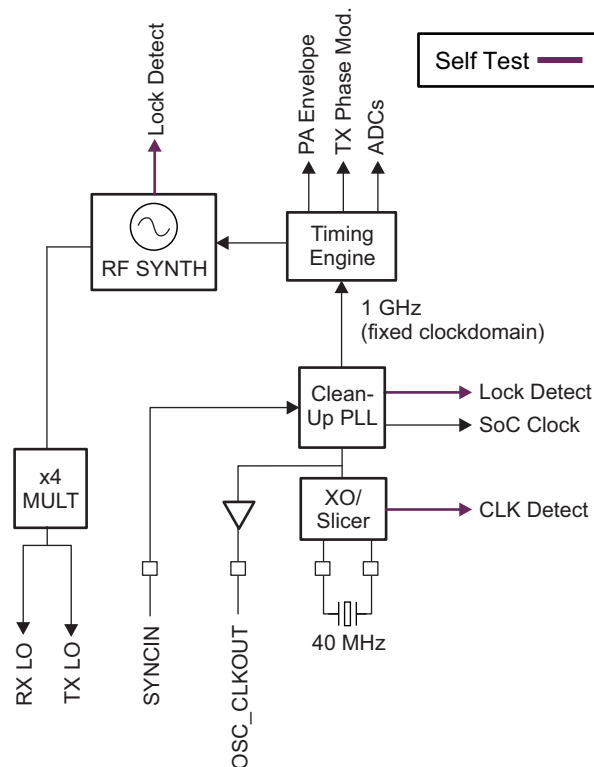


Figure 6-2. Clock Subsystem

6.4.1.2 Transmit Subsystem

The AWR1443 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. A maximum of 2 transmit chains can be operational at the same time. However all 3 chains can be operated together in a time multiplexed fashion. The device supports binary phase modulation for MIMO radar and interference mitigation.

Each transmit chain can deliver a maximum of 12 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization.

Figure 6-3 describes the transmit subsystem.

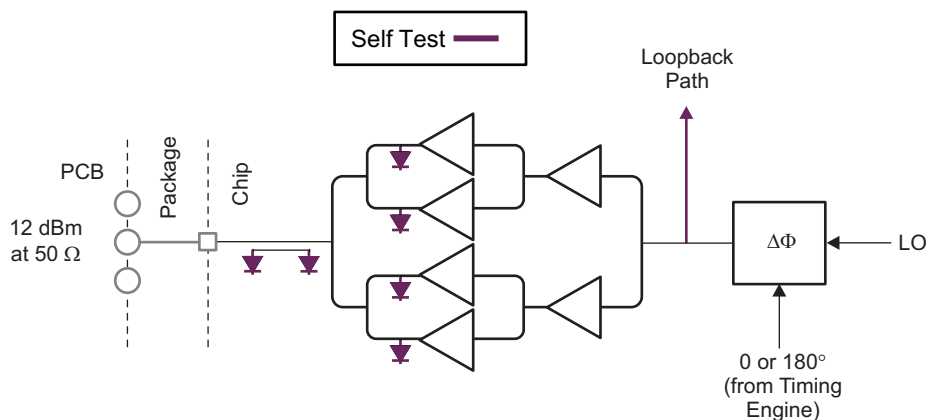


Figure 6-3. Transmit Subsystem (Per Channel)

6.4.1.3 Receive Subsystem

The AWR1443 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, A2D conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the AWR1443 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The AWR1443 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 5 MHz.

Figure 6-4 describes the receive subsystem.

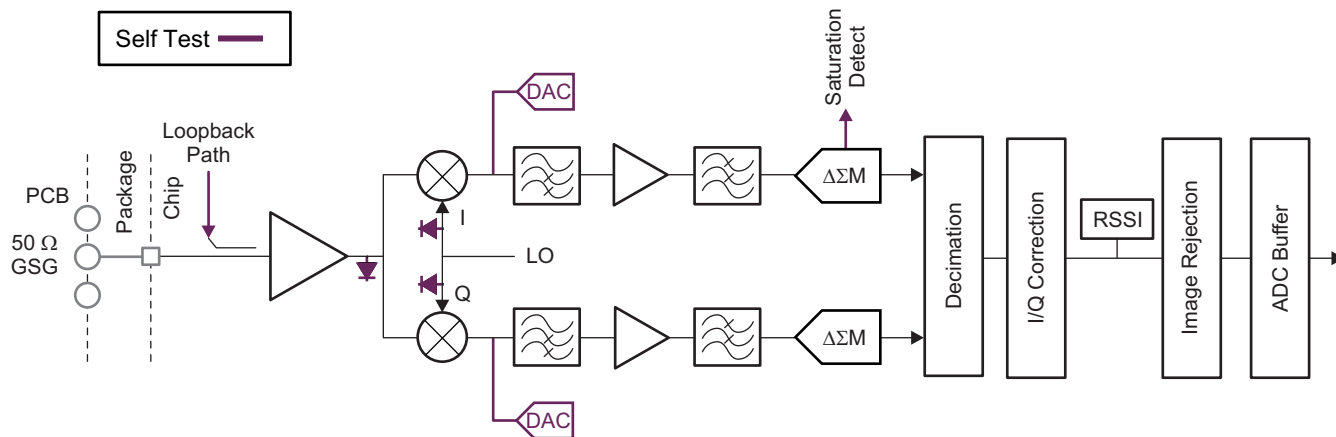


Figure 6-4. Receive Subsystem (Per Channel)

6.4.1.4 Radio Processor Subsystem

The Radio Processor subsystem (also referred to as BIST Subsystem in this document) includes the digital front-end, the ramp generator and an internal processor for control / configuration of the low-level RF/analog and ramp generator registers. The Radar Processor also schedules periodic monitoring tasks. User applications, running on

Master (Control) System, do not have direct access to Radar System; access is based on well-defined API messages (over a hardware channel) from the master subsystem.

NOTE

This radio processor is programmed by TI and takes care of RF calibration and self-test/monitoring functions (BIST). This processor is not available directly for customer use/application.

The digital front-end takes care of filtering and decimating the raw sigma-delta ADC output and provides the final ADC data samples at a programmable sampling rate.

6.4.2 Master (Control) System

The Master (Control) System includes ARM's automotive grade Cortex-R4F processor clocked at 200 MHz, which is user programmable. User applications executing on this processor control the overall operation of the device, including Radar Control via well-defined API messages, radar signal processing (assisted by the radar hardware accelerator) and peripherals for external interface.

The Master (Control) System plays a big role in enabling autonomous operation of AWR1443 as a radar-on-a-chip sensor. The device includes a quad serial peripheral interface (QSPI) which can be used to download customer code directly from a serial flash. A (classic) CAN interface is included that can be used to communicate directly from the device to a CAN bus. An SPI/I2C interface is available for power management IC (PMIC) control when the AWR1443 is used as an autonomous sensor.

For more complex applications, the device can operate under the control of an external MCU, which can communicate with AWR1443 device over an SPI interface. In this case, it is possible to use the AWR14xx as a radar sensor, providing raw detected objects to the external MCU. External MCU could reduce the application code complexity residing in the device and makes more memory available for radar data cube inside the AWR1443. This configuration also eliminates the need for a separate serial flash to be connected to the AWR1443.

Furthermore, the external MCU can provide faster interfaces, such as CAN-FD or Ethernet, for the radar sensor to connect to a central processing unit (CPU). In such a distributed configuration, multiple AWR1443 devices mounted around the vehicle can connect to the CPU, providing a surround view. The external MCU itself is low-cost, because the low-level radar signal processing is accomplished inside the AWR1443, using the hardware accelerator, while the higher-layer intelligence and complex algorithms reside in the common CPU, making the overall solution cost-effective.

Note that although four interfaces – one CAN, one I2C and two SPI interfaces – are present in the AWR1443 device for external communication and PMIC control, only two of these interfaces are usable at any point in time.

The total memory (RAM) available in the master subsystem is 576 KB. This is partitioned between the R4F program RAM, R4F data RAM and radar data memory. The maximum usable size for R4F is 448 KB and this is partitioned between the R4F's tightly coupled interfaces TCMA (320 KB) and TCMB (128 KB). Although the complete 448 KB is unified memory and can be used for program or data, typical applications use TCMA as program and TCMB as data memory.

The remaining memory, starting at a minimum of 128 KB, is available to be used as radar data memory for storing the 'radar data cube'. It is possible to increase the radar data memory size in 64 KB increments, at the cost of corresponding reduction in R4F program or data RAM size. The maximum size of radar data memory possible is 384 KB. A few example configurations supported are listed in [Table 6-1](#).

Table 6-1. R4F RAM⁽¹⁾

| OPTION | R4F PROGRAM RAM | R4F DATA RAM | RADAR DATA MEMORY |
|--------|-----------------|--------------|-------------------|
| 1 | 320KB | 128KB | 128KB |
| 2 | 256KB | 128KB | 192KB |
| 3 | 256KB | 64KB | 256KB |
| 4 | 128KB | 64KB | 384KB |

(1) For AWR1443 ES version 1.0, available RAM is 448 KB instead of 576KB.

The Master Subsystem, Cortex-R4F memory map is shown in [Table 6-2](#).

Table 6-2. Master System Memory Map

| Name | Frame Address (Hex) | | Size | Description |
|------------------------------------|---------------------|--------------|--------|--|
| | Start | End | | |
| CPU Tightly Coupled Memories | | | | |
| TCMA ROM | 0x0000_0000 | 0x0001_FFFF | 96KiB | Program ROM |
| TCM RAM-A | 0x0020_0000 | 0x0023_FFFF | 128KiB | 256/512KB based on Variant |
| TCM RAM-B | 0x0800_0000 | 0x0802_FFFF | 64KiB | Data RAM |
| System Peripherals | | | | |
| Mail Box MSS<->RADARSS | 0xF060_1000 | 0xF060_17FF | 2KiB | RADARSS to MSS mailbox memory space |
| | 0xF060_2000 | 0xF060_27FF | 2KiB | MSS to RADARSS mailbox memory space |
| | 0xF060_8000 | 0xF060_80FF | 188B | MSS to RADARSS mailbox Configuration Registers |
| | 0xF060_8060 | 0xF060_86FF | 188B | RADARSS to MSS mailbox Configuration Registers |
| PRCM & Control Module | 0xFFFF_E100 | 0xFFFF_E2FF | 756B | TOP Level Reset, Clock management registers |
| | 0xFFFF_FF00 | 0xFFFF_FFFF | 256B | MSS Reset, Clock management registers |
| | 0xFFFF_EA00 | 0xFFFF_EBFF | 512KiB | IO Mux module registers |
| | 0xFFFF_F800 | 0xFFFF_FBFF | 352B | General-purpose control registers |
| | 0x5000_0400 | | 584B | TPCC,TPTC,ADC buffer configuration, status registers |
| GIO | 0xFFFF7_BC00 | 0xFFFF7_BDFF | 180B | GIO module configuration registers |
| DMA | 0xFFFF7_F000 | 0xFFFF7_F3FF | 1KiB | DMA-1 module configuration registers |
| VIM | 0xFFFF7_FD00 | 0xFFFF7_FEFF | 512B | VIM module configuration registers |
| RTI-A | 0xFFFF7_FC00 | 0xFFFF7_FCFF | 192B | RTI-A module |
| RTI-B | 0xFFFF7_EE00 | 0xFFFF7_EEFF | 192B | RTI-B module register space |
| Serial Interfaces and Connectivity | | | | |
| QSPI | 0xC000_0000 | 0xC07F_FFFF | 8MB | QSPI –Flash Memory space |
| | 0xC080_0000 | 0xC0FF_FFFF | 116B | QSPI module configuration registers |
| MIBSPI | 0xFFFF7_F400 | 0xFFFF7_F5FF | 512B | MIBSPI-A module configuration registers |
| SPI | 0xFFFF7_F600 | 0xFFFF7_F7FF | 512B | SPI module configuration registers |
| SCI-A/UART | 0xFFFF7_E500 | 0xFFFF7_E5FF | 148B | SCI-A module configuration registers |
| SCI-B/UART | 0xFFFF7_E700 | 0xFFFF7_E7FF | 148B | SCI-B module configuration registers |
| CAN | 0xFFFF7_DC00 | 0xFFFF7_DDFF | 512B | CAN module configuration registers |
| I2C | 0xFFFF7_D400 | 0xFFFF7_D4FF | 112B | I2C module configuration registers |
| ADC Buffer | 0x5200_0000 | | 16KiB | ADC ping pong buffer memory space |
| CBUF_FIFO | 0x5202_0000 | | 16KiB | Common buffer memory space |

Table 6-2. Master System Memory Map (continued)

| Name | Frame Address (Hex) | | Size | Description |
|---|---------------------|--------------|--------|--|
| | Start | End | | |
| Hardware FFT accelerator | 0x5008_0000 | 0x5008_07FF | 512B | FFT Accelerator PARAM memory |
| | 0x5008_0800 | 0x5008_0FFF | 264B | FFT accelerator Configuration registers |
| | 0x5008_1000 | | 4KiB | FFT accelerator Window registers |
| | 0x5203_0000 | 0x5203_7FFF | 32KiB | FFT accelerator Memory -1 space |
| | 0x5203_8000 | | 32KiB | FFT accelerator Memory -2 space |
| L3 Memory | | | | |
| L3 Shared Memory | 0x5100_0000 | | 384KiB | L3 Shared memory space |
| Interconnects | | | | |
| PCR | 0xFFFF7_8000 | 0xFFFF7_87FF | 1KiB | PCR-1 interconnect configuration port |
| PCR-2 | 0xFCFF_1000 | 0xFCFF_17FF | 1KiB | PCR-2 interconnect configuration port |
| 128 bit SCR | 0x5207_0000 | | 128B | 128 bit SCR configuration port |
| Safety Modules | | | | |
| CRC | 0xFE00_0000 | 0xFEFF_FFFF | 16KiB | CRC module configuration registers |
| PBIST | 0xFFFF_E400 | 0xFFFF_E5FF | 464B | PBIST module configuration registers |
| STC | 0xFFFF_E600 | 0xFFFF_E7FF | 284B | STC module configuration registers |
| DCC-A | 0xFFFF_EC00 | 0xFFFF_ECFE | 44B | DCC-A module configuration registers |
| DCC-B | 0xFFFF_F400 | 0xFFFF_F4FF | 44B | DCC-B module configuration registers |
| ESM | 0xFFFF_F500 | 0xFFFF_F5FF | 156B | ESM module configuration registers |
| CCMR4 | 0xFFFF_F600 | 0xFFFF_F6FF | 136B | CCMR4 module configuration registers |
| Peripheral Memories (System & Non System) | | | | |
| CAN RAM | 0xFF1E_0000 | 0xFF1F_FFFF | 128KB | CAN RAM memory space |
| DMA RAM | 0xFFF8_0000 | 0xFFF8_0FFF | 4KB | DMA RAM memory space |
| VIM RAM | 0xFFF8_2000 | 0xFFF8_2FFF | 2KB | VIM RAM memory space |
| MIBSPIA-TX RAM | 0xFF0E_0000 | 0xFF0E_01FF | 0.5KB | MIBSPIA-TX RAM memory space |
| MIBSPIA- RX RAM | 0xFF0E_0200 | 0xFF0E_03FF | 0.5KB | MIBSPIA- RX RAM memory space |
| Debug Modules | | | | |
| Debug Sub System | 0xFFA0_0000 | 0xFFAF_FFFF | 244KiB | Debug subsystem memory space and registers |

6.4.3 Host Interface

The AWR1443 device communicates with the host radar processor over the following main interfaces:

- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (slave) for host control. All radio control commands (and response) flow through this interface.
- Reset – Active-low reset for device wakeup from host
- Out-of-band interrupt
- Error – Used for notifying the host in case the radio controller detects a fault

6.5 Accelerators and Coprocessors

The Processing System in the AWR1443 device is an accelerator for FFT operations. The Radar Hardware Accelerator is an IP that enables off-loading the burden of certain frequently used computations in FMCW radar signal processing from the main processor. It is well-known that FMCW radar signal processing involves the use of FFT and Log-Magnitude computations in order to obtain a radar image across the range, velocity and angle dimensions. Some of the frequently used functions in FMCW radar signal processing can be done within the Radar Hardware Accelerator, while still retaining the flexibility of implementing other proprietary algorithms in the Master System processor.

Key features of the Radar Processing Accelerator are:

- FFT computation, with programmable FFT sizes (powers of 2) up to 1024-pt complex FFT
- Internal FFT bit-width of 24 bits (each for I and Q) for good SQNR performance, with fully programmable butterfly scaling at every radix-2 stage for user flexibility
- Built-in capabilities for simple pre-FFT processing – specifically, programmable windowing, basic interference zeroing-out and basic BPM removal
- Magnitude (absolute value) and Log-Magnitude computation capability
- Flexible data flow and data sample arrangement to support efficient multi-dimensional FFT operations and transpose accesses as required
- Chaining and Looping mechanism to sequence a set of accelerator operations one-after-another with minimal intervention from the main processor
- CFAR-CA detector support (linear and logarithmic)
- Miscellaneous other capabilities of the accelerator
 - Stitching two or four 1024-point FFTs to get the equivalent of 2048-point or 4096-point FFT for industrial level sensing applications where large FFT sizes are required
 - Slow DFT mode, with resolution equivalent to 16K size FFT, for FFT peak interpolation (eg. range interpolation) purpose
 - Complex Vector Multiplication and Dot product capability for vectors of size up to 512

6.6 Other Subsystems

6.6.1 ADC Channels (Service) for User Application

The AWR1443 device includes provision for an ADC service for user application, where the

GPADC engine present inside the device can be used to measure up to six external voltages. The ADC1, ADC2, ADC3, ADC4, ADC5, and ADC6 pins are used for this purpose.

- ADC itself is controlled by TI firmware running inside the BIST subsystem and access to it for customer's external voltage monitoring purpose is via 'monitoring API' calls routed to the BIST subsystem. This API could be linked with the user application running on the Master R4.
- BIST subsystem firmware will internally schedule these measurements along with other RF and Analog monitoring operations. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings will be reported for each of the monitored voltages.

GPADC Specifications:

- 625 Ksps SAR ADC
- 0 to 1.8V input range
- 10-bit resolution
- For 5 out of the 6 inputs, an optional internal buffer is available. Without the buffer, the ADC has a switched capacitor input load modeled with 5pF of sampling capacitance and 12pF parasitic capacitance (GPADC channel 6, the internal buffer is not available).

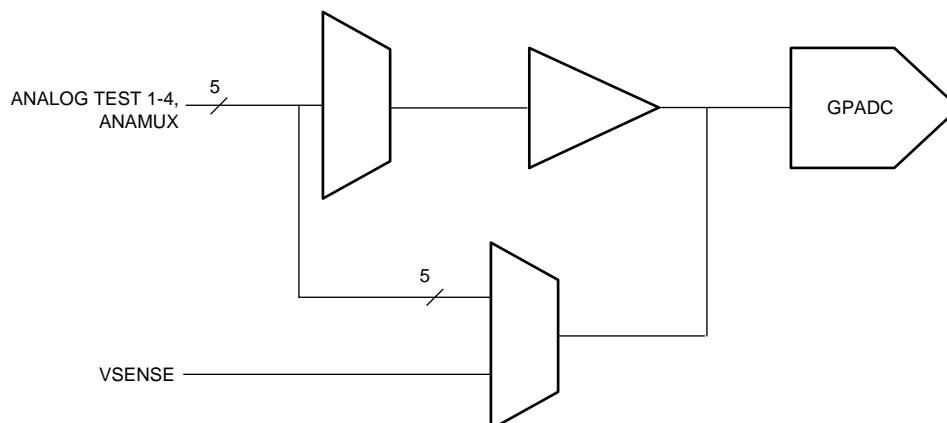


Figure 6-5. ADC Path

Table 6-3. GP-ADC Parameter

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|-------------------------|-------------------------|------|-----|-----|------|
| ADC input voltage range | | 0 | | 1.8 | V |
| ADC resolution | | | 10 | | bit |
| ADC | 100 kHz input frequency | 47 | | | dB |
| ADC offset error | | -5 | | 5 | LSB |
| ADC gain error | | -5 | | 5 | LSB |
| ADC DNL | | -1 | | 3.5 | LSB |
| ADC INL | | -2.5 | | 2.5 | LSB |
| ADC sample rate | | | 625 | | Ksps |
| ADC sampling time | | | 400 | | ns |

Table 6-3. GP-ADC Parameter (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|-----------|-----|-----|-----|------|
| ADC internal capacitance | sampling | | 7 | | pF |
| | parasitic | | 12 | | |
| ADC leakage current | | | 3 | | μA |
| Input buffer input range ⁽¹⁾ | | 0.4 | | 1.4 | V |
| Input buffer input capacitance | | | 0.5 | | pF |

(1) Outside of given range, the buffer output will become nonlinear.

6.7 Identification

The JTAG identification code for this device is the same as the device ICEPick Identification code. [Table 6-4](#) captures the JTAG ID code per silicon revision.

Table 6-4. Device Identification

| Silicon Revision | ID |
|------------------|------------|
| ES1.0 | 0x0BB1F02F |

Table 6-5. JTAG Interface

| Signal | SoC Pin | Name | Type | Function |
|--------|---------|------------------|--------|---|
| TCK | M13 | Test Clock | Input | Free Running clock when used with emulators viz. Spectrum Digital's XDS200 or TI's XDS110 |
| TMS | L13 | Test Mode Select | Input | Directs the next state of the JTAG state machine |
| TDI | H13 | Test Data Input | Input | Scan Data Input to the device |
| TDO | J13 | Test Data Output | Output | Scan Data Output of the device |

6.8 Boot Modes

As soon as device reset is de-asserted, the R4F processor of the Master (Control) system starts executing its bootloader from an on-chip ROM memory.

The bootloader of the Master system operates in two basic modes and these are specified on the user hardware (Printed Circuit Board) by configuring what are termed as “Sense on Power” (SOP) pins. These pins on the device boundary are scanned by the bootloader firmware and choice of mode for bootloader operation is made.

[Table 6-6](#) enumerates the relevant SOP combinations and how these map to bootloader operation.

Table 6-6. SOP Combinations

| SOP2 (P13) | SOP1 (P11) | SOP0 (J13) | BOOTLOADER MODE AND OPERATION |
|------------|------------|------------|--|
| 0 | 0 | 1 | Functional Mode Device Bootloader loads user application from QSPI Serial Flash to internal RAM and switches the control to it |
| 1 | 0 | 1 | Flashing Mode Device Bootloader spins in loop to allow flashing of user application (or device firmware patch – Supplied by TI) to the serial flash |
| 0 | 1 | 1 | Debug Mode Bootloader is bypassed and R4F processor is halted. This allows user to connect emulator at a known point |

6.8.1 Flashing Mode

In Flashing Mode, the Master System’s bootloader enables the UART driver and expects a data stream comprising of User Application (Binary Image) and Device Firmware (referred to as Device Firmware Patch or Service Pack) from an external flashing utility. Figure 6-6 shows the flashing utility executing on a PC platform, but the protocol can be accomplished on an embedded platform as well.

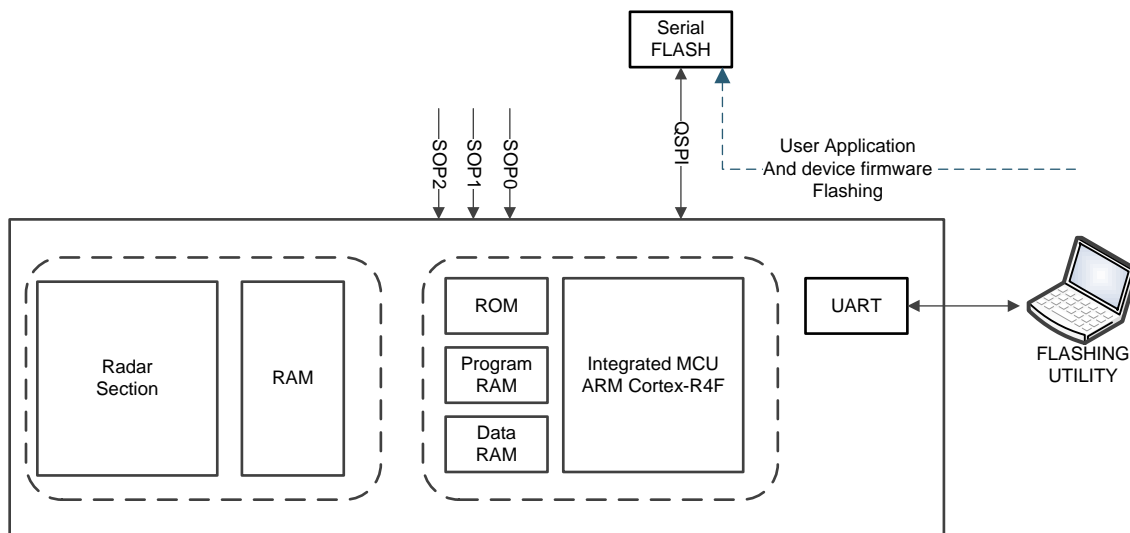


Figure 6-6. Figure 5. Bootloader Flashing Mode

6.8.2 Functional Mode

In Functional Mode, the Master System's bootloader looks for a valid image in the serial flash memory, interfaced over the QSPI port. If a valid image is found, the bootloader transfers the same to Master System's memory subsystem. If the device firmware image is found, it gets transferred to the Radar section's memory subsystem.

If a valid image (or the QSPI Serial Flash is not found), the bootloader initializes the SPI port and awaits for the image transfer. This operation comes handy for configurations where the AWR1443 is interfaced to an external processor which has its own nonvolatile storage hence can store the user application and the AWR1443 device's firmware image.

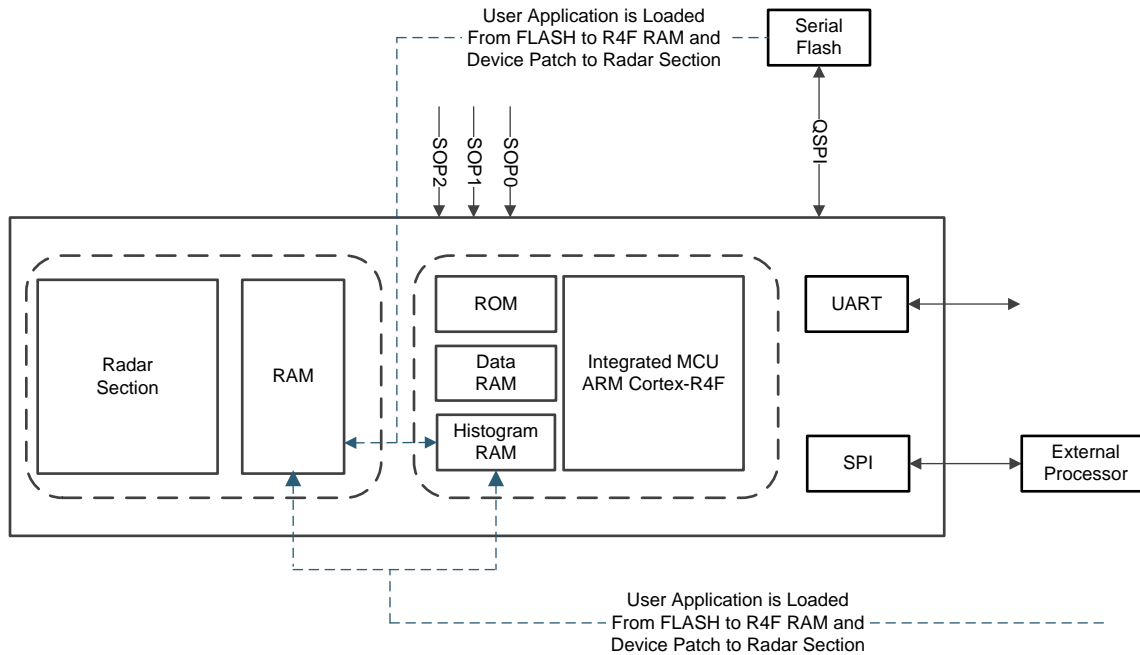


Figure 6-7. Bootloader's Functional Mode

7 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

Key device features driving the following applications are:

- Integration of Radar Front End and Programmable MCU
- On-chip Hardware Accelerator for Radar Data Processing
- Flexible boot modes: Autonomous Application boot using a serial flash or external boot over SPI.

7.2 Short-Range Radar

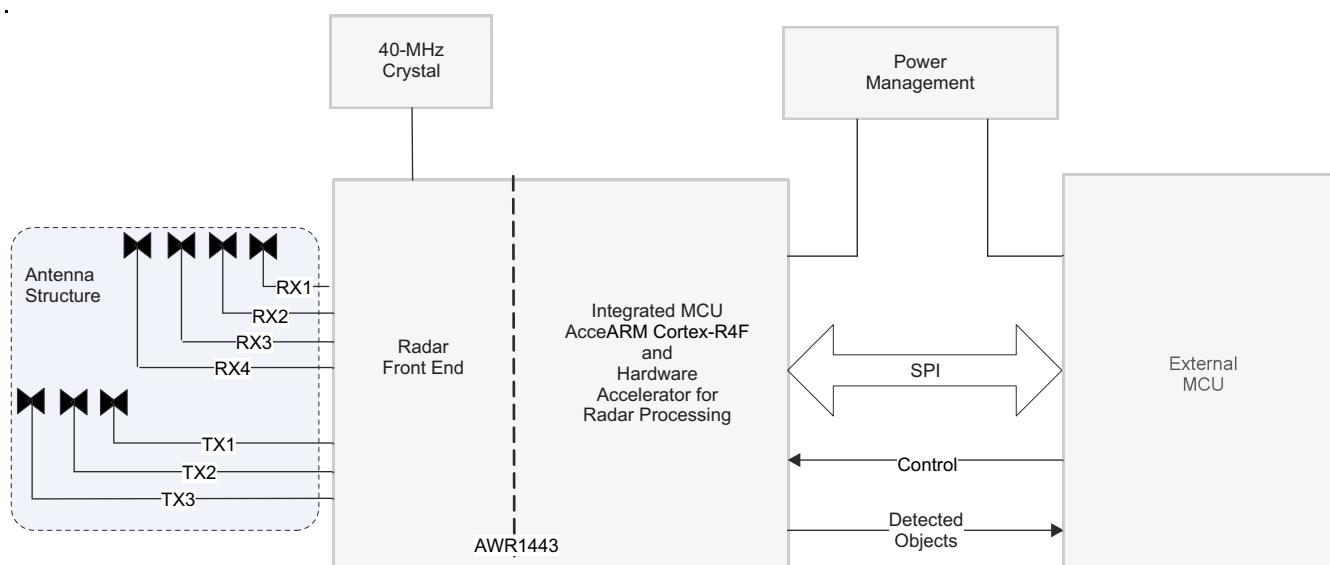
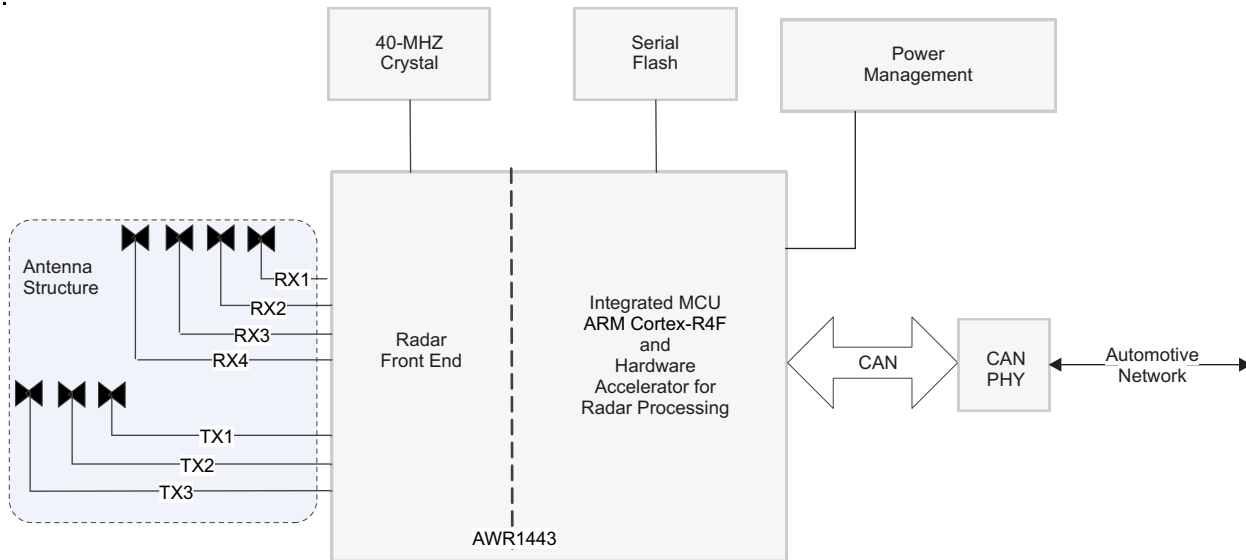


Figure 7-1. Short-Range Radar

7.3 Blind Spot Detector and Ultrasonic Upgrades



7.4 Reference Schematic

Figure 7-2 and show the reference schematic and low-noise LDO circuitry for the AWR1443 device.

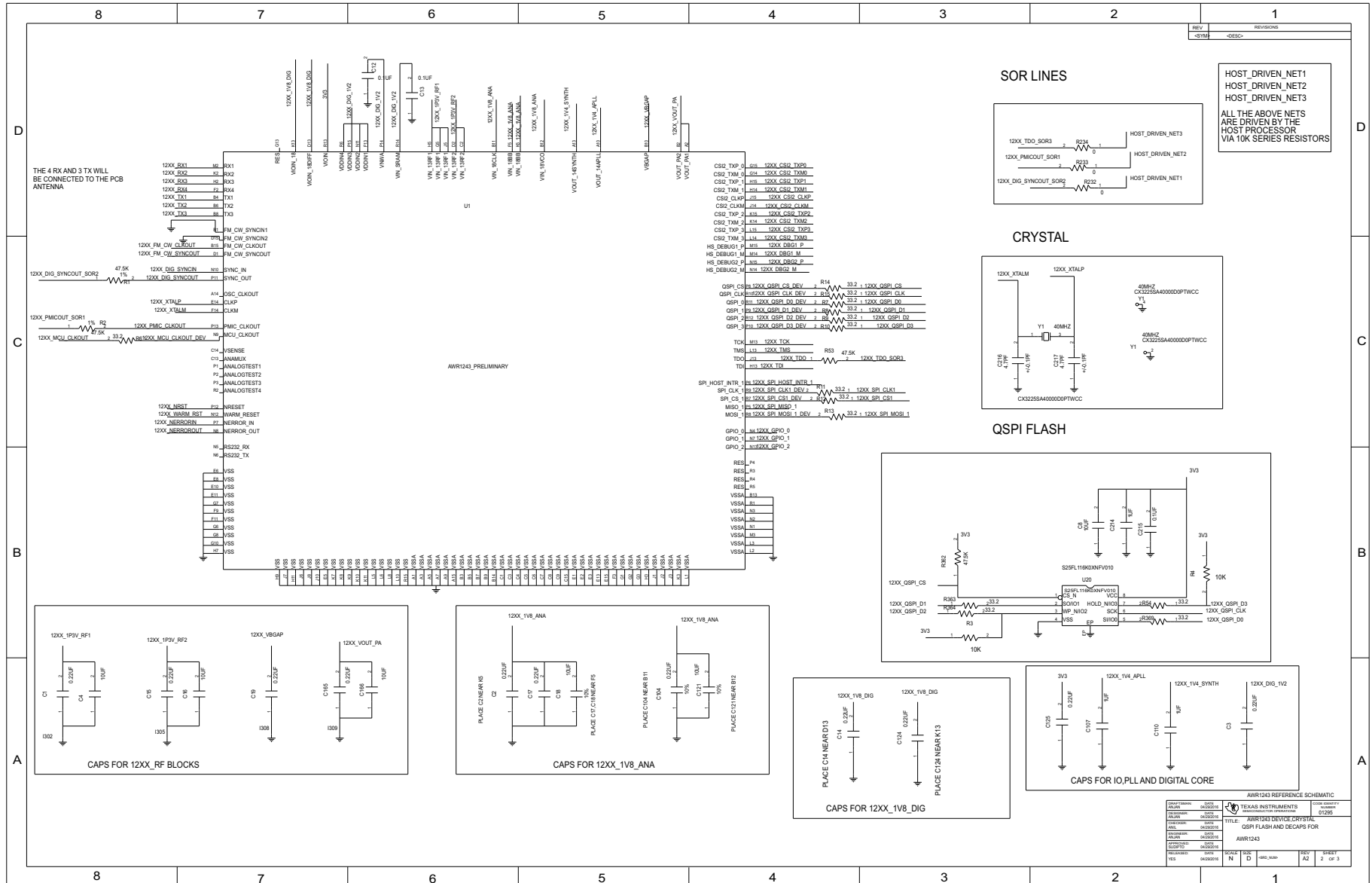


Figure 7-2. AWR1443 Reference Schematic

7.5 Layout

The top layer routing, top layer closeup, and bottom layer routing are shown in [Figure 7-3](#), [Figure 7-4](#), and [Figure 7-5](#), respectively.

7.5.1 Layout Guidelines

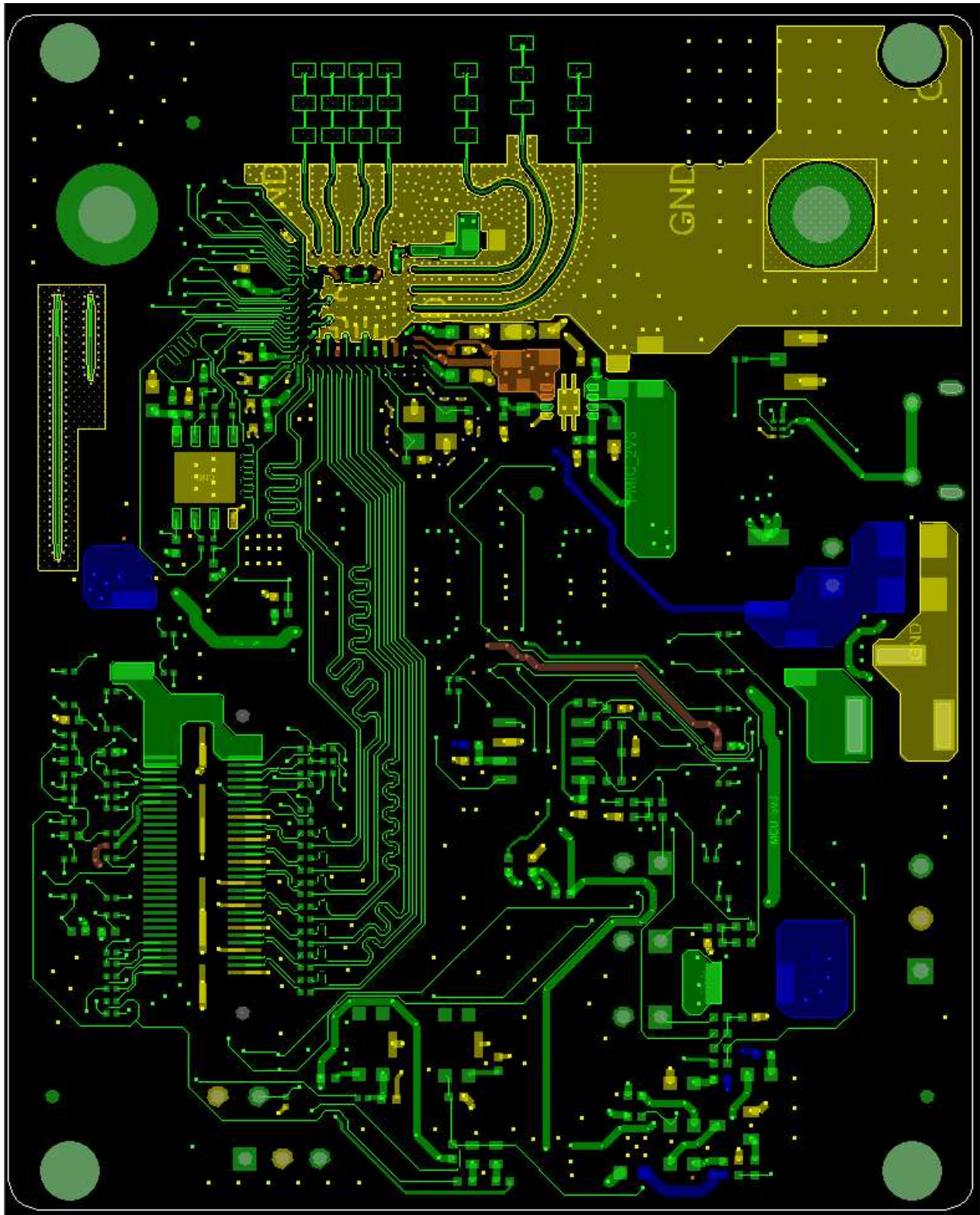


Figure 7-3. Top Layer Routing

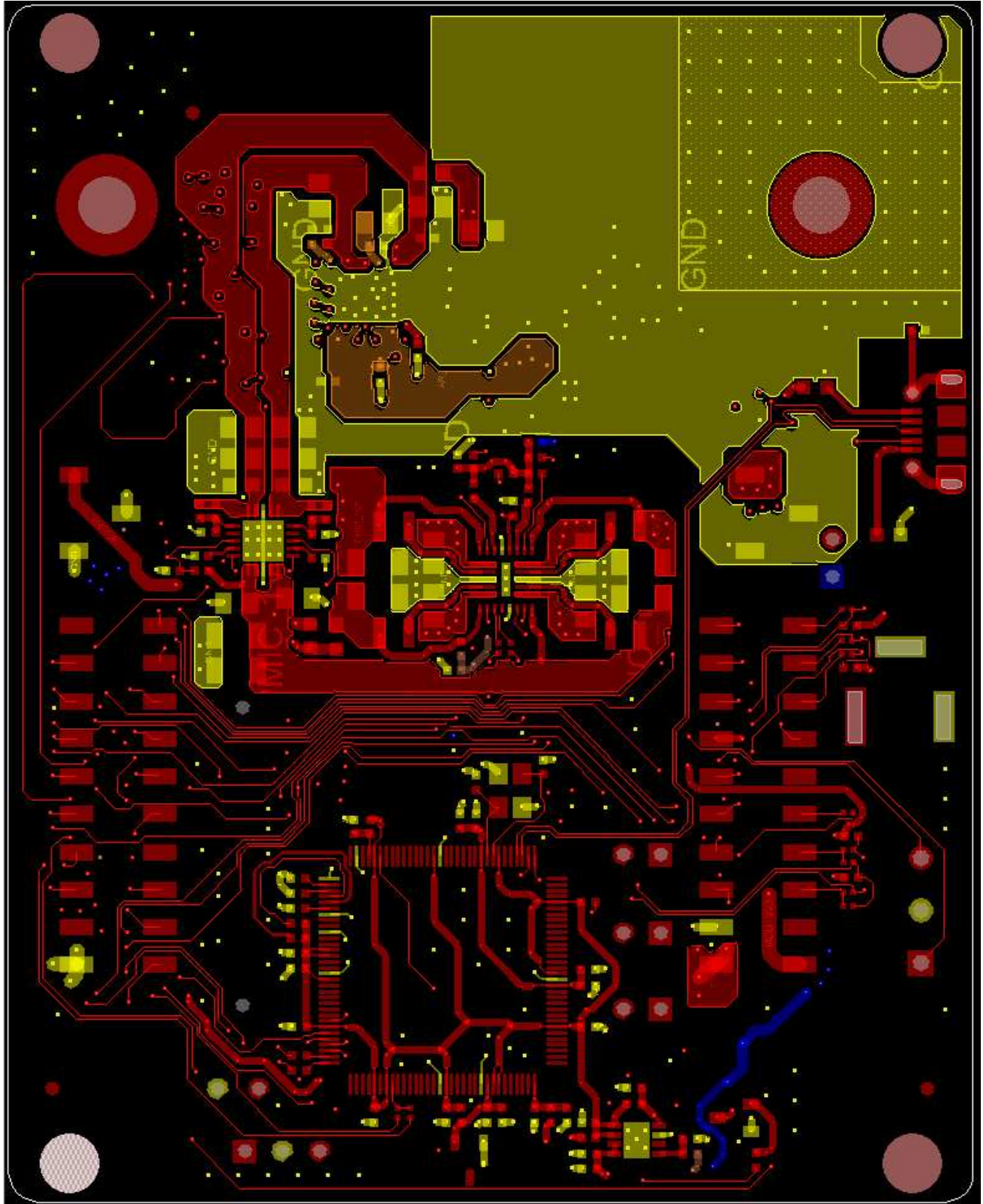
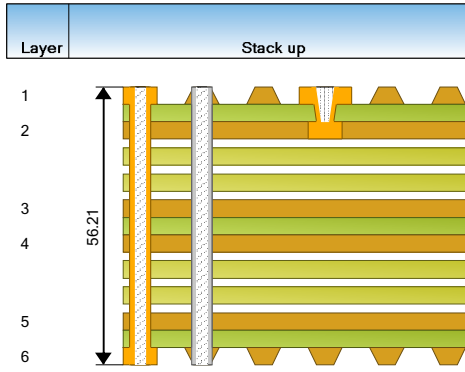


Figure 7-5. Bottom Layer Routing

7.5.2 Stackup Details



| Layer | Stack up | Description | Type | Base Thickness | Processed Thickness | ϵ_r | Copper Coverage |
|-------|----------|----------------------------------|-------------|----------------|---------------------|--------------|-----------------|
| 1 | | Rogers 4835 4mil coreH/1 Low Pro | Rogers 4835 | 0.689 | 2.067 | | 100.000 |
| 2 | | | | 4.000 | 4.000 | 3.480 | |
| | | | | 1.260 | 1.260 | | 73.000 |
| | | Iteq IT 180A Prepreg 1080 | Dielectric | 4.195 | 2.830 | 3.700 | |
| | | Iteq IT 180A Prepreg 1080 | Dielectric | 4.195 | 2.830 | 3.700 | |
| 3 | | | | 1.260 | 1.260 | | 69.000 |
| | | Iteq IT 180A 28 mil core 1/1 | FR4 | 28.000 | 28.000 | 4.280 | |
| 4 | | | | 1.260 | 1.260 | | 48.000 |
| | | Iteq IT 180A Prepreg 1080 | Dielectric | 4.195 | 2.691 | 3.700 | |
| | | Iteq IT 180A Prepreg 1080 | Dielectric | 4.195 | 2.691 | 3.700 | |
| 5 | | | | 1.260 | 1.260 | | 72.000 |
| | | Iteq IT 180A 4 mil core 1/H | FR4 | 4.000 | 4.000 | 3.790 | |
| 6 | | | | 0.689 | 2.067 | | 100.000 |

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *AWR1443*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL0161), the temperature range (for example, blank is the default commercial temperature range). [Figure 8-1](#) provides a legend for reading the complete device name for any *AWR1443* device.

For orderable part numbers of *AWR1443* devices in the ABL0161 package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the [AWR1443 Device Errata Silicon Revision 1.0 and 2.0](#).

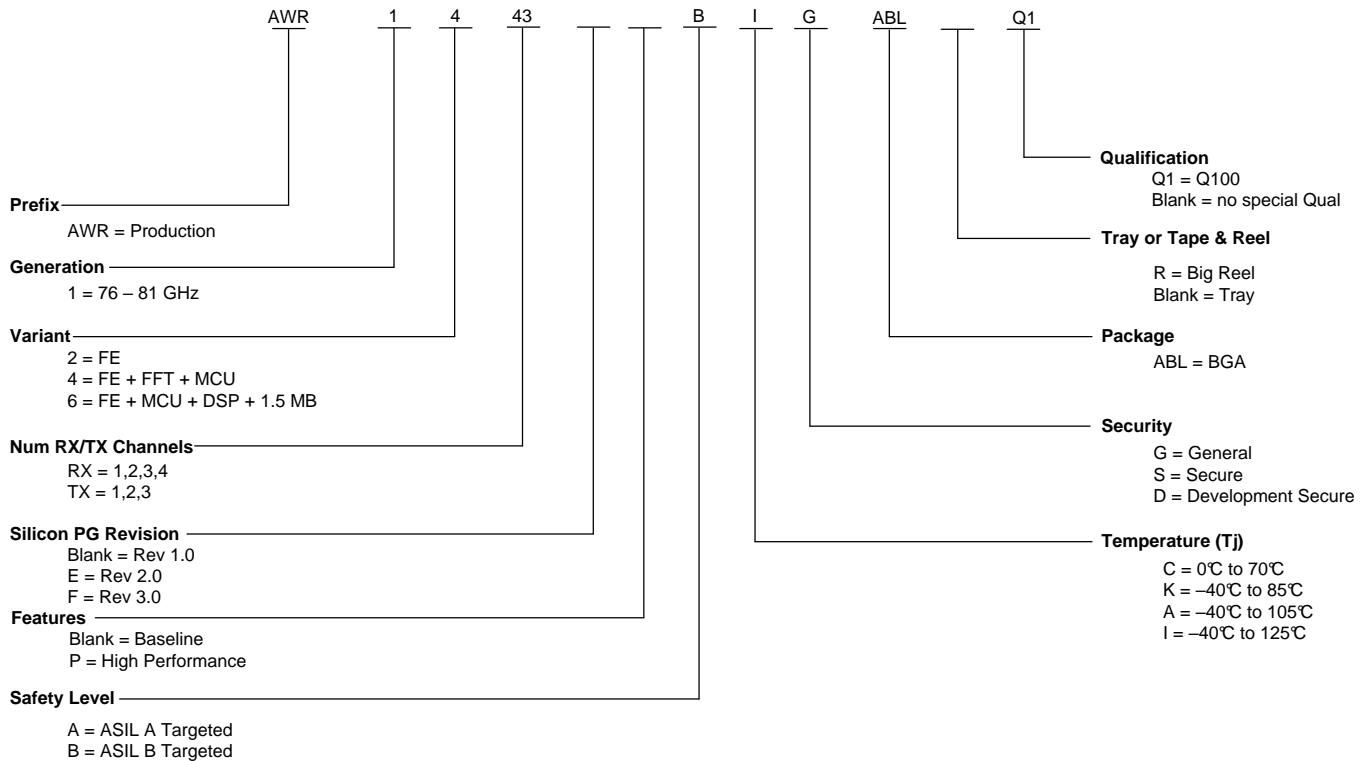


Figure 8-1. Device Nomenclature

8.2 Tools and Software

Models

AWR1443 BSDL Model Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

AWR1x43 IBIS Model IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

AWR1443 Checklist for Schematic Review, Layout Review, Bringup/Wakeup A set of steps in spreadsheet form to select system functions and pinmux options. Specific EVM schematic and layout notes to apply to customer engineering. A bringup checklist is suggested for customers.

8.3 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (AWR1443). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

Errata

AWR1443 Device Errata Describes known advisories, limitations, and cautions on silicon and provides workarounds.

8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

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8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information



9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

CAUTION

The following package information is subject to change without notice.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| AWR1443FQIGABLRQ1 | ACTIVE | FCCSP | ABL | 161 | 176 | RoHS & Green | Call TI | Level-3-260C-168 HR | -40 to 125 | AWR1443 IG 964FC |  |
| AWR1443FQIGABLRQ1 | ACTIVE | FCCSP | ABL | 161 | 1000 | RoHS & Green | Call TI | Level-3-260C-168 HR | -40 to 125 | AWR1443 IG 964FC |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

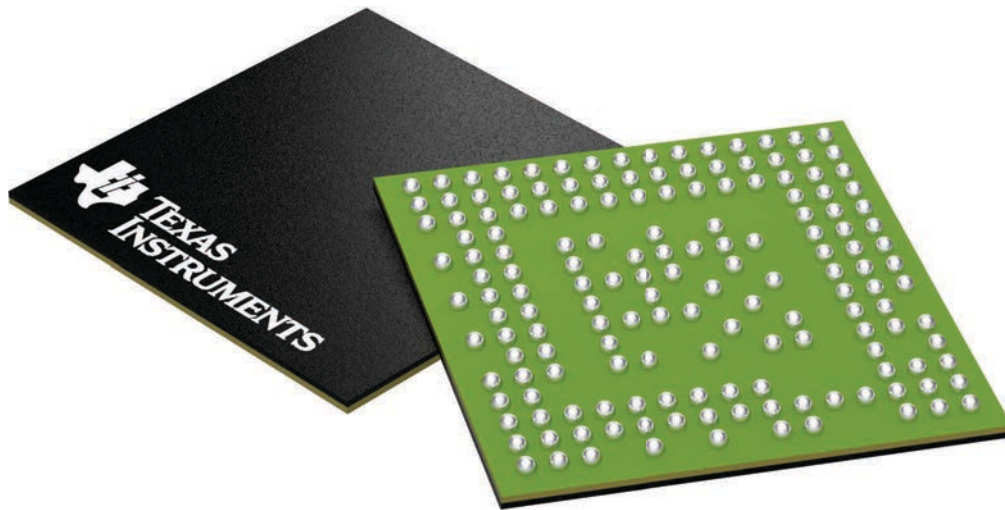
ABL 161

FCBGA - 1.17 mm max height

10.4 x 10.4, 0.65 mm pitch

PLASTIC BALL GRID ARRAY

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225978/A

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