ADS794x 超低功耗、12/10/8 位双通道 SAR ADC

1 特性

- 采样率：2MSPS
- 引脚兼容系列：12/10/8 位
- 高分辨率、高吞吐量：
  - ADS7947：12 位、2.1MSPS
  - ADS7948：10 位、2.57MSPS
  - ADS7949：8 位、3MSPS
- 出色的性能：
  - 无丢码
  - INL：1LSB（最大值）
  - SNR：72dB（最小值）
- 低功耗：
  - 以 2MSPS 运行时为 7.5mW
  - 低速时自动断电：
    - 500kSPS 时为 3.8mW
    - 100kSPS 时为 0.8mW
    - 20kSPS 时为 0.16mW
- 宽电源电压范围：
  - 模拟：2.7V 至 5.5V
  - 数字：1.65V 至 AVDD
- SPI 兼容串行接口
- 工作温度范围：-40°C 至 +125°C
- 微型封装尺寸：3mm × 3mm WQFN

2 应用

- 通信系统
- 光纤网络
- 医疗仪器
- 电池供电类设备
- 数据采集系统

3 说明

ADS7947、ADS7948 和 ADS7949 分别是具有引脚兼容性的 12/10/8 位 2MSPS 模数转换器 (ADC)。这些器件以 2MSPS 采样率和标准 16 时钟数据帧运行。此外，ADS7947（12 位）、ADS7948（10 位）和 ADS7949（8 位）可以分别以 2.1MSPS、2.57MSPS 和 3MSPS 运行，并使用针对时钟周期数量进行了优化的短数据帧，足以在丝毫不影响性能的情况下完成转换。这些器件具有出色的直流精度和动态性能。此系列器件具有引脚兼容性，包含一个双通道输入多路复用器和一个低功耗逐次逼近寄存器 (SAR) ADC。

ADS7947、ADS7948 和 ADS7949 支持宽模拟电源电压范围，因此支持最高 5V 的满量程输入范围。利用简单的 SPI 数字接口以及可在电压低至 1.65V 时运行的数字电源，可轻松连接到各种数字控制器。低速运行时，可以启用自动断电功能以大幅降低功耗。

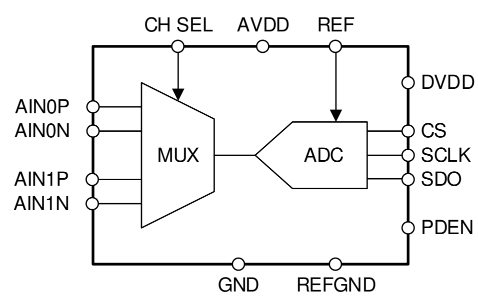
ADS7947、ADS7948 和 ADS7949 采用微型 3mm × 3mm WQFN 封装，其额定工作温度范围为 -40°C 至 +125°C，适用于多种将高性能、低功耗和小尺寸视为主要考虑因素的数据采集 应用 。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS794x	WQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

ADS794x 方框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (September 2010) to Revision A **Page**

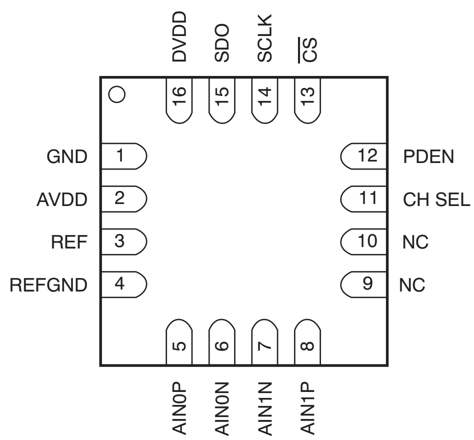
- 已添加 *器件信息* 表、*ESD 额定值* 表、*建议运行条件* 表、*开关特性* 表、*功能方框图* 部分特性 *说明* 部分、*器件功能模式* 部分、*编程* 部分、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 已更改 更改了文档标题 ... 1
- 已更改 将整个文档中的 QFN 更改为 WQFN ... 1
- 已添加 *高分辨率*、*高吞吐量*：“特性” 项目中的子项目 ... 1
- 已更改 将温度范围 特性 项目符号从*额定温度范围* 更改为*工作温度范围* ... 1
- 已更改 *更改了说明* 部分的内容（为了清晰起见）并将*具有固有采样保持 (S/H) 输入级的 ADC* 更改为 *ADC* ... 1
- 已更改 更改了第 1 页的图片并添加了标题 ... 1
- Changed title of *Family and Ordering Information* to *Device Comparison Table* ... 3
- Changed thermal symbols for $R_{\theta JA}$, $R_{\theta JC(top)}$, $R_{\theta JB}$, and $R_{\theta JC(bot)}$ ... 5
- Deleted *Full-scale input span*, *Absolute input range*, *External Reference*, *AVDD*, and *DVDD* parameters and *Temperature Range* section from *Electrical Characteristics: ADS7947 (12-Bit)* table ... 5
- Deleted *Full-scale input span*, *Absolute input range*, *External Reference*, *AVDD*, and *DVDD* parameters and *Temperature Range* section from *Electrical Characteristics: ADS7948 (10-Bit)* table ... 7
- Deleted *Full-scale input span*, *Absolute input range*, *External Reference*, *AVDD*, and *DVDD* parameters and *Temperature Range* section from *Electrical Characteristics: ADS7949 (8-Bit)* table ... 9
- Changed *Timing Requirements* table: added section titles, moved switching parameters into *Switching Characteristics* table ... 10
- Changed symbol for *Pulse duration, SCLK low* parameter from t_{W1} to t_{WL} ... 10
- Added symbol to *SCLK frequency* parameter ... 10
- Changed title of *PCB Layout/Schematic Guidelines* to *Layout* and changed format of section ... 30
- Changed *Recommended ADC Schematic* figure ... 30

5 Device Comparison Table

PRODUCT	RESOLUTION (Bits)	INPUT	SAMPLE RATE (MSPS)
ADS7947	12	Unipolar, pseudo-differential	2
ADS7948	10	Unipolar, pseudo-differential	2
ADS7949	8	Unipolar, pseudo-differential	2

6 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN NO.	PIN NAME	FUNCTION	DESCRIPTION
1	GND	Analog/digital	Power supply ground; all analog and digital signals are referred with respect to this pin.
2	AVDD	Analog	ADC power supply.
3	REF	Analog	ADC positive reference input; decouple this pin with REFGND.
4	REFGND	Analog	Reference return; short to analog ground plane.
5	AIN0P	Analog input	Positive analog input, channel 0.
6	AIN0N	Analog input	Negative analog input, channel 0. The allowable signal swing on this pin is ±0.2V; this pin can be grounded.
7	AIN1N	Analog input	Negative analog input, channel 1. The allowable signal swing on this pin is ±0.2V; this pin can be grounded.
8	AIN1P	Analog input	Positive analog input, channel 1.
9	NC	—	Not connected internally, TI recommends externally shorting this pin to GND.
10	NC	—	Not connected internally, TI recommends externally shorting this pin to GND.
11	CH SEL	Digital input	This pin selects the analog input channel. Low = channel 0, high = channel 1. TI recommends changing the channel within a window of one clock; from half a clock after the $\overline{\text{CS}}$ falling edge. This change ensures the settling on the multiplexer output before the sample start.
12	PDEN	Digital input	This pin enables a power-down feature if this pin is high at the $\overline{\text{CS}}$ rising edge.
13	$\overline{\text{CS}}$	Digital input	Chip-select signal; active low.
14	SCLK	Digital input	Serial SPI clock.
15	SDO	Digital output	Serial data out.
16	DVDD	Digital	Digital I/O supply.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
AINxP to GND or AINxN to GND		–0.3	AVDD + 0.3	V
AVDD to GND or DVDD to GND		–0.3	7	V
Digital input voltage to GND		–0.3	DVDD + 0.3	V
Digital output to GND		–0.3	DVDD + 0.3	V
Temperature	Operating	–40	125	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions: ADS794x (12-, 10-, 8-Bit)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage		2.7	3.3	5.5	V
DVDD	Digital supply voltage		1.65	3.3	AVDD	V
REFERENCE INPUT						
V_{REF}	External reference input		2.5		AVDD	V
ANALOG INPUTS						
FSR	Full-scale input span(1)	AINxP – AINxN	0		V_{REF}	V
V_{IN}	Absolute input range	AIN0P, AIN1P	–0.2		AVDD + 0.2	V
		AIN0N, AIN1M	–0.2		0.2	
TEMPERATURE RANGE						
	Temperature range for specified performance		–40		125	°C

(1) Ideal input span; does not include gain or offset error.

7.4 Thermal Information

THERMAL METRIC[1]		ADS794x RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: ADS7947 (12-Bit)

minimum and maximum values at AVDD = 2.7 V to 5.5 V, DVDD = 1.65 V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2 MSPS (unless otherwise noted); typical values at AVDD = 3 V, DVDD = 1.8 V, T_A = +25°C, and f_{SAMPLE} = 2 MSPS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Input capacitance[1]			32		pF
Input leakage current	At +125°C		1.5		nA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No missing codes		12			Bits
Integral linearity		–1	±0.3	1	LSB[2]
Differential linearity		–1	±0.3	1	LSB
Offset error[3]		–1	±0.3	1	LSB
Gain error		–1	±0.3	1	LSB
Transition noise				25	μV_{RMS}
Power-supply rejection			60		dB
SAMPLING DYNAMICS					
Conversion time				13.5	SCLK
Acquisition time		80			ns
Maximum sample rate (throughput rate)	34-MHz SCLK with a 16-clock frame			2	MSPS
	34-MHz SCLK and $\overline{CS}$ low for 13.5 clocks			2.1	MSPS
Aperture delay				5	ns
Aperture jitter			10		ps
Step response			80		ns
Overvoltage recovery			80		ns
DYNAMIC CHARACTERISTICS					
Total harmonic distortion (THD)[4]	100kHz		–85		dB
Signal-to-noise ratio (SNR)	100 kHz	72	73		dB
Signal-to-noise and distortion ratio (SINAD)	100 kHz		72.75		dB
Spurious-free dynamic range (SFDR)	100 kHz		86		dB
Full-power bandwidth	At –3 dB		15		MHz
DIGITAL INPUT/OUTPUT					
Logic family	CMOS				

(1) See Figure 40 for sampling circuit details.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input.
(4) Calculated on the first nine harmonics of the input frequency.

Electrical Characteristics: ADS7947 (12-Bit) (continued)

minimum and maximum values at AVDD = 2.7 V to 5.5 V, DVDD = 1.65 V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2 MSPS (unless otherwise noted); typical values at AVDD = 3 V, DVDD = 1.8 V, T_A = +25°C, and f_{SAMPLE} = 2 MSPS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic level	V_{IH}		0.7DVDD			V
	V_{IL}				0.3DVDD	V
	V_{OH}	I_{SOURCE} = 200 µA	DVDD – 0.2			V
	V_{OL}	I_{SINK} = 200 µA	0.4			V
Input leakage current	I_{IH}, I_{IL}	0 < V_{IN} < DVDD		±20		nA
POWER-SUPPLY REQUIREMENTS						
AVDD supply current	$I_{DYNAMIC}$	AVDD = 3.3 V, f_{SAMPLE} = 2 MSPS		2.5		mA
		AVDD = 5 V, f_{SAMPLE} = 2 MSPS		3	3.5	mA
	I_{STATIC}	AVDD = 3.3 V, SCLK off		1.8		mA
		AVDD = 5 V, SCLK off		1.9	2.5	mA
DVDD supply current(5)		DVDD = 3.3 V, SCLK = 34 MHz, SDO load 20 pF		500		µA
Power-down state AVDD supply current	$I_{PD\text{-}DYNAMIC}$	SCLK = 34 MHz			550	µA
	$I_{PD\text{-}STATIC}$	SCLK off			2.5	µA
Power-up time					1	µs

(5) DVDD consumes only dynamic current. $I_{DVDD} = C_{LOAD} \times DVDD \times$ number of 0→1 transitions in SDO × f_{SAMPLE}. This current is load-dependent and there is no DVDD current when the output is not toggling.

7.6 Electrical Characteristics: ADS7948 (10-Bit)

minimum and maximum values at AVDD = 2.7 V to 5.5 V, DVDD = 1.65 V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2 MSPS (unless otherwise noted); typical values at AVDD = 3 V, DVDD = 1.8 V, T_A = +25°C, and f_{SAMPLE} = 2 MSPS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
Input capacitance[1]				32		pF
Input leakage current		At +125°C		1.5		nA
SYSTEM PERFORMANCE						
Resolution				10		Bits
No missing codes			10			Bits
Integral linearity			–0.5	±0.15	0.5	LSB[2]
Differential linearity			–0.5	±0.15	0.5	LSB
Offset error[3]			–0.5	±0.15	0.5	LSB
Gain error			–0.5	±0.15	0.5	LSB
Transition noise					25	μV_{RMS}
Power-supply rejection				60		dB
SAMPLING DYNAMICS						
Conversion time					10.5	SCLK
Acquisition time			80			ns
Maximum sample rate (throughput rate)		34-MHz SCLK in 16-clock frame			2	MSPS
		34-MHz SCLK and $\overline{CS}$ low for 10.5 clocks			2.57	MSPS
Aperture delay					5	ns
Aperture jitter				10		ps
Step response				80		ns
Overvoltage recovery				80		ns
DYNAMIC CHARACTERISTICS						
Total harmonic distortion (THD)[4]		100kHz		–80		dB
Signal-to-noise ratio (SNR)		100 kHz	61			dB
Signal-to-noise and distortion ratio (SINAD)		100 kHz		61		dB
Spurious-free dynamic range (SFDR)		100 kHz		81		dB
Full-power bandwidth		At –3 dB		15		MHz
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7DVDD			V
	V_{IL}				0.3DVDD	V
	V_{OH}	I_{SOURCE} = 200 µA	DVDD – 0.2			V
	V_{OL}	I_{SINK} = 200 µA			0.4	V
Input leakage current	I_{IH}, I_{IL}	0 < V_{IN} < DVDD		±20		nA

(1) See Figure 40 for sampling circuit details.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input.
(4) Calculated on the first nine harmonics of the input frequency.

Electrical Characteristics: ADS7948 (10-Bit) (continued)

minimum and maximum values at AVDD = 2.7 V to 5.5 V, DVDD = 1.65 V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2 MSPS (unless otherwise noted); typical values at AVDD = 3 V, DVDD = 1.8 V, T_A = +25°C, and f_{SAMPLE} = 2 MSPS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS						
AVDD supply current	$I_{DYNAMIC}$	AVDD = 3.3 V, f_{SAMPLE} = 2 MSPS		2.5		mA
		AVDD = 5 V, f_{SAMPLE} = 2 MSPS		3	3.5	mA
	I_{STATIC}	AVDD = 3.3 V, SCLK off		1.8		mA
		AVDD = 5 V, SCLK off		1.9	2.5	mA
DVDD supply current[(5)]		DVDD = 3.3 V, SCLK = 34 MHz, SDO load 20 pF		500		µA
Power-down state AVDD supply current	$I_{PD-DYNAMIC}$	SCLK = 34 MHz			550	µA
	$I_{PD-STATIC}$	SCLK off			2.5	µA
Power-up time					1	µs

(5) DVDD consumes only dynamic current. $I_{DVDD} = C_{LOAD}$ × DVDD × number of 0→1 transitions in SDO × f_{SAMPLE}. This current is load-dependent and there is no DVDD current when the output is not toggling.

7.7 Electrical Characteristics: ADS7949 (8-Bit)

minimum and maximum values at AVDD = 2.7 V to 5.5 V, DVDD = 1.65 V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2 MSPS (unless otherwise noted); typical values at AVDD = 3 V, DVDD = 1.8 V, T_A = +25°C, and f_{SAMPLE} = 2 MSPS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
Input capacitance[1]				32		pF
Input leakage current		At +125°C		1.5		nA
SYSTEM PERFORMANCE						
Resolution				8		Bits
No missing codes			8			Bits
Integral linearity			–0.3	±0.06	0.3	LSB[2]
Differential linearity			–0.3	±0.06	0.3	LSB
Offset error[3]			–0.3	±0.06	0.3	LSB
Gain error			–0.3	±0.06	0.3	LSB
Transition noise					25	μV_{RMS}
Power-supply rejection				60		dB
SAMPLING DYNAMICS						
Conversion time					8.5	SCLK
Acquisition time			80			ns
Maximum sample rate (throughput rate)		34-MHz SCLK in 16-clock frame			2	MSPS
		34-MHz SCLK and $\overline{CS}$ low for 8.5 clocks			3	MSPS
Aperture delay					5	ns
Aperture jitter				10		ps
Step response				80		ns
Overvoltage recovery				80		ns
DYNAMIC CHARACTERISTICS						
Total harmonic distortion (THD)[4]		100 kHz		–80		dB
Signal-to-noise ratio (SNR)		100 kHz	49			dB
Signal-to-noise and distortion ratio (SINAD)		100 kHz		49		dB
Spurious-free dynamic range (SFDR)		100 kHz		81		dB
Full-power bandwidth		At –3 dB		15		MHz
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7DVDD			V
	V_{IL}				0.3DVDD	V
	V_{OH}	I_{SOURCE} = 200 µA	DVDD – 0.2			V
	V_{OL}	I_{SINK} = 200 µA	0.4			V
Input leakage current	I_{IH}, I_{IL}	0 < V_{IN} < DVDD		±20		nA

(1) See Figure 40 for sampling circuit details.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input.
(4) Calculated on the first nine harmonics of the input frequency.

Electrical Characteristics: ADS7949 (8-Bit) (continued)

minimum and maximum values at AVDD = 2.7 V to 5.5 V, DVDD = 1.65 V to AVDD, T_A = –40°C to +125°C, and f_{SAMPLE} = 2 MSPS (unless otherwise noted); typical values at AVDD = 3 V, DVDD = 1.8 V, T_A = +25°C, and f_{SAMPLE} = 2 MSPS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS						
AVDD supply current	$I_{DYNAMIC}$	AVDD = 3.3 V, f_{SAMPLE} = 2 MSPS		2.5		mA
		AVDD = 5 V, f_{SAMPLE} = 2 MSPS		3	3.5	mA
	I_{STATIC}	AVDD = 3.3 V, SCLK off		1.8		mA
		AVDD = 5 V, SCLK off		1.9	2.5	mA
DVDD supply current(5)		DVDD = 3.3 V, SCLK = 34 MHz, SDO load 20 pF		500		µA
Power-down state AVDD supply current	$I_{PD-DYNAMIC}$	SCLK = 34 MHz			550	µA
	$I_{PD-STATIC}$	SCLK off			2.5	µA
Power-up time					1	µs

(5) DVDD consumes only dynamic current. $I_{DVDD} = C_{LOAD}$ × DVDD × number of 0→1 transitions in SDO × f_{SAMPLE}. This current is load-dependent and there is no DVDD current when the output is not toggling.

7.8 Timing Requirements

at DVDD(1) = 1.65 V to AVDD (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C, typical values at T_A = 25°C

			MIN	NOM	MAX	UNIT
CONVERSION CYCLE						
f_{SAMPLE}	Sample rate (throughput rate)	SCLK = 34 MHz, 16 clock frame			2	MSPS
	$f_{SAMPLE\ MAX} = 1 / (t_{CONV\ MAX} + t_{ACQ\ MIN})$	ADS7947 (12 bit), SCLK = 34 MHz			2.1	MSPS
		ADS7948 (10 bit), SCLK = 34 MHz			2.57	
		ADS7949 (8 bit), SCLK = 34 MHz			3	
t_{ACQ}	Acquisition time		80			ns
POWER DOWN						
t_{PDSU}	Setup time, PDEN high to $\overline{CS}$ rising edge (see Figure 45 and Figure 46)		2			ns
t_{PDH}	Hold time, $\overline{CS}$ rising edge to PDEN falling edge (see Figure 45)		20			ns
SPI INTERFACE TIMINGS						
t_{W1}	Pulse duration, $\overline{CS}$ high		25			ns
t_{SU1}	Setup time, $\overline{CS}$ low to first rising edge of SCLK	DVDD = 1.8 V	3.5			ns
		DVDD = 3 V	3.5			
		DVDD = 5 V	3.5			
t_{D4}	Delay time, $\overline{CS}$ rising edge from conversion end (see the t_{CONV} specification for conversion time)		10			ns
t_{WH}	Pulse duration, SCLK high		11			ns
t_{WL}	Pulse duration, SCLK low		11			ns
f_{SCLK}	SCLK frequency		0.4	34	40	MHz

(1) 1.8-V specifications apply from 1.65 V to 2 V; 3-V specifications apply form 2.7 V to 3.6 V; 5-V specifications apply from 4.75 V to 5.25 V.

7.9 Switching Characteristics

at DVDD = 1.65 V to AVDD (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C, typical values at T_A = 25°C

PARAMETER			TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time	ADS7947 (12 bit)				13.5	SCLK
		ADS7948 (10 bit)				10.5	
		ADS7949 (8 bit)				8.5	
t_{D1}	Delay time, $\overline{CS}$ low to first data (D0-15) out		DVDD = 1.8 V			14.5	ns
			DVDD = 3 V			12.5	
			DVDD = 5 V			8.5	
t_{D2}(2)	Delay time, SCLK falling to SDO		DVDD = 1.8 V			11	ns
			DVDD = 3 V			9	
			DVDD = 5 V			7.1	
t_{H1}	Hold time, SCLK falling to data valid		DVDD = 1.8 V	4			ns
			DVDD = 3 V	3			
			DVDD = 5 V	2			
t_{D3}	Delay time, $\overline{CS}$ high to SDO 3-state		DVDD = 1.8 V			15	ns
			DVDD = 3 V			12.5	
			DVDD = 5 V			8.5	

(1) 1.8-V specifications apply from 1.65 V to 2 V; 3-V specifications apply form 2.7 V to 3.6 V; 5-V specifications apply from 4.75 V to 5.25 V.
(2) With 50-pF load.

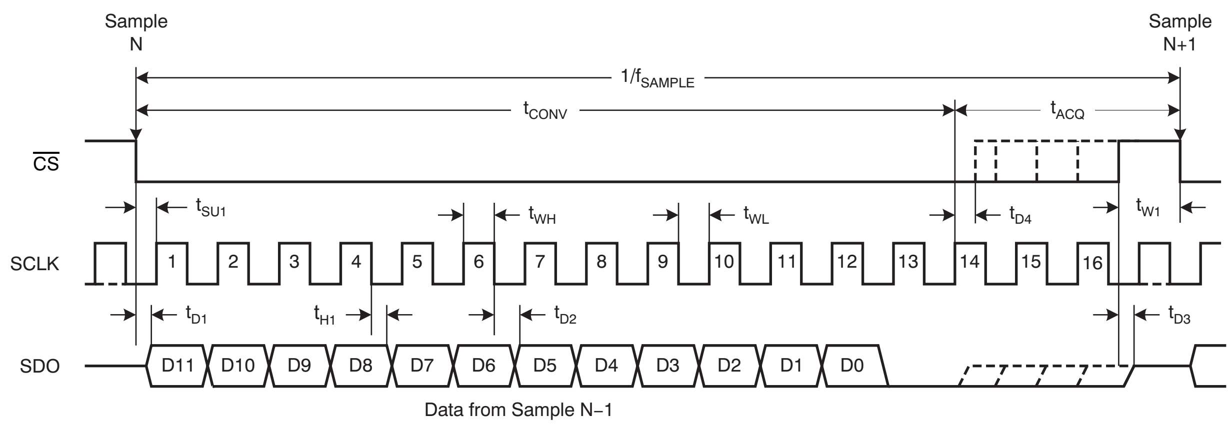


Figure 1. Timing Diagram

7.10 Typical Characteristics: ADS7947, ADS7948, ADS7949

at T_A = 25°C, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS (unless otherwise noted)

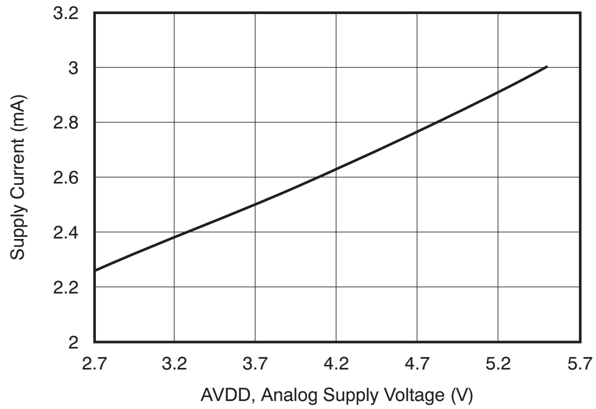


Figure 2. Supply Current vs Analog Supply Voltage

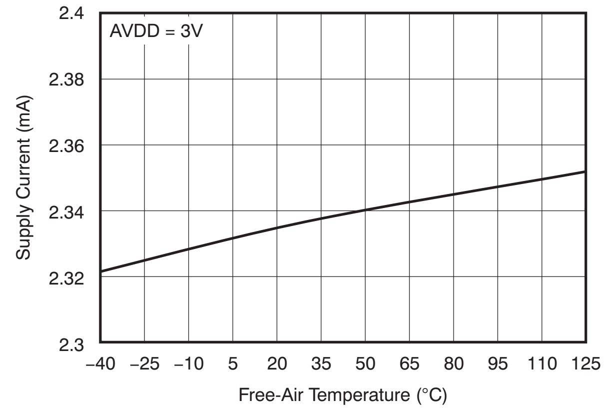


Figure 3. Supply Current vs Temperature

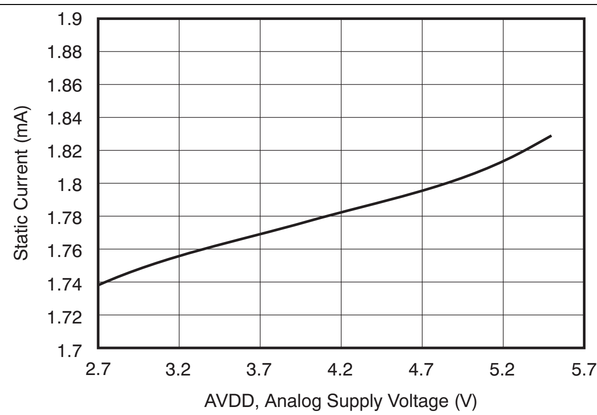


Figure 4. Static Current vs Analog Supply Voltage

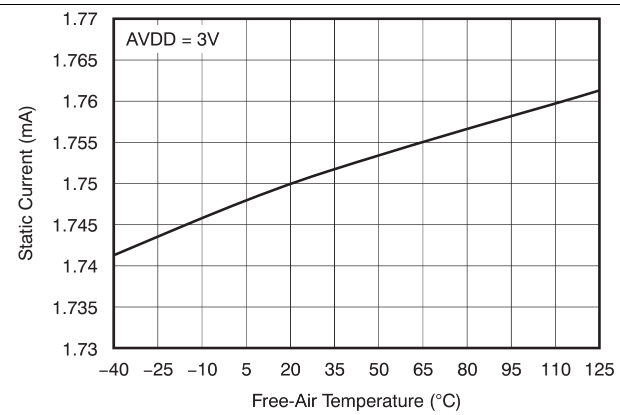


Figure 5. Static Current vs Free-Air Temperature

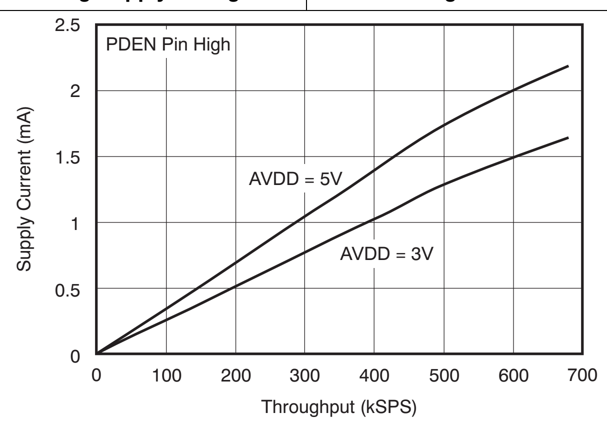


Figure 6. Supply Current vs Throughput

7.11 Typical Characteristics: ADS7947 (12-Bit)

At T_A = 25°C, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS (unless otherwise noted)

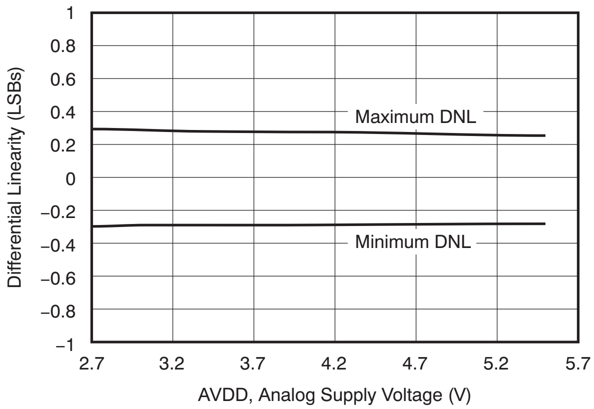


Figure 7. Differential Linearity vs Analog Supply Voltage

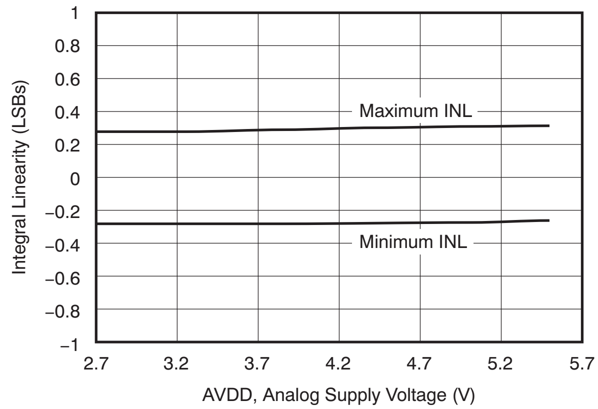


Figure 8. Integral Linearity vs Analog Supply Voltage

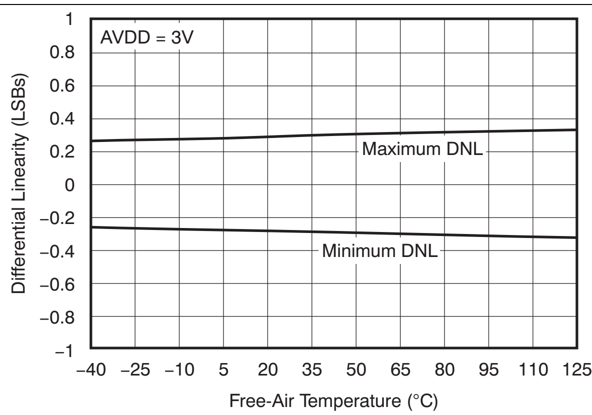


Figure 9. Differential Linearity vs Temperature

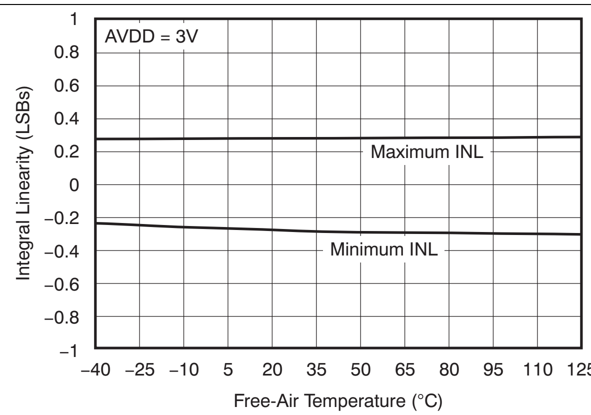


Figure 10. Integral Linearity vs Temperature

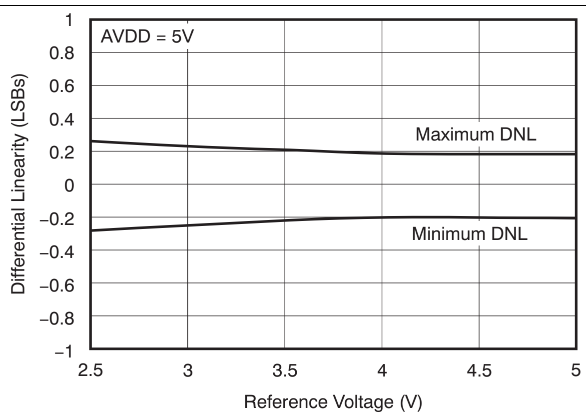


Figure 11. Differential Linearity vs Reference Voltage

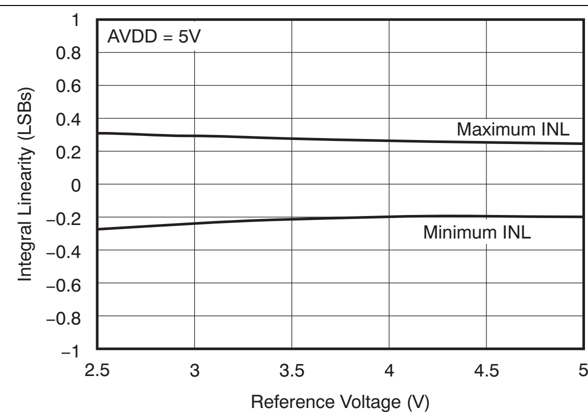


Figure 12. Integral Linearity vs Reference Voltage

Typical Characteristics: ADS7947 (12-Bit) (continued)

At T_A = 25°C, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS (unless otherwise noted)

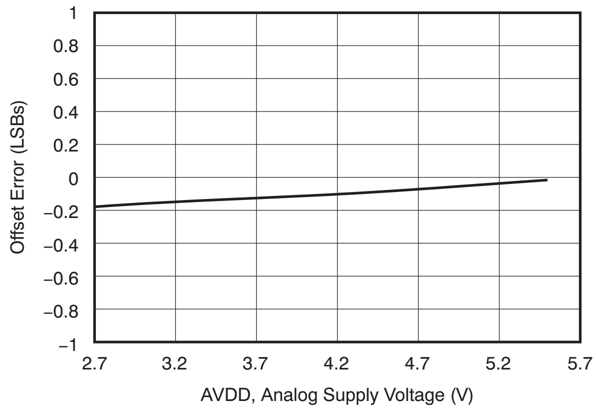


Figure 13. Offset Error vs Analog Supply Voltage

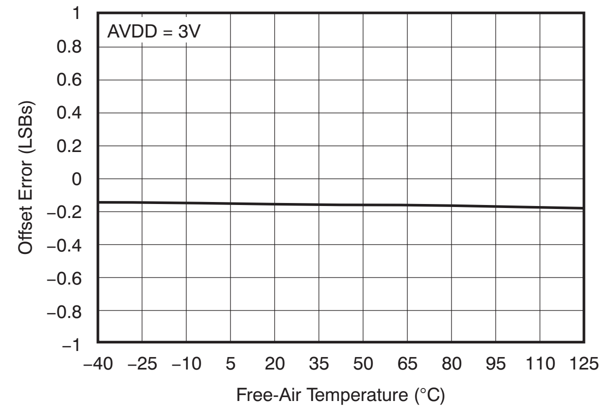


Figure 14. Offset Error vs Temperature

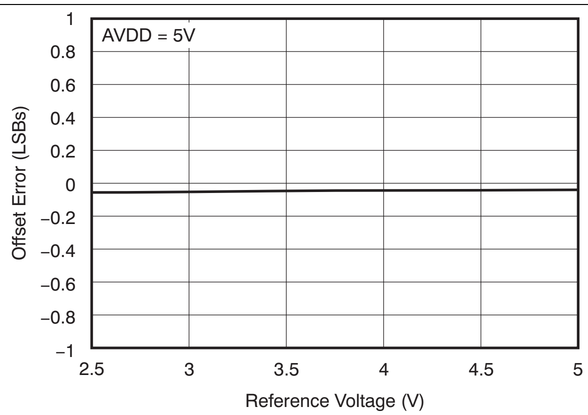


Figure 15. Offset Error vs Reference Voltage

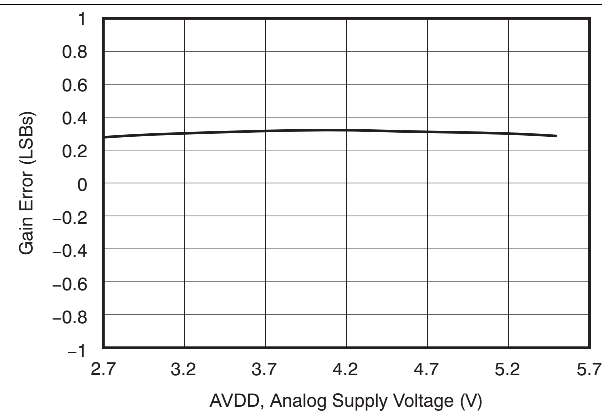


Figure 16. Gain Error vs Analog Supply Voltage

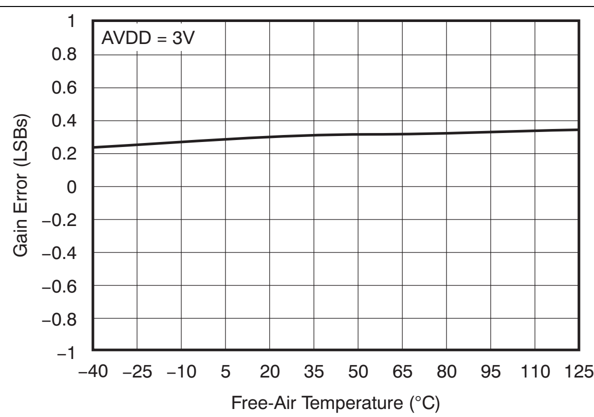


Figure 17. Gain Error vs Temperature

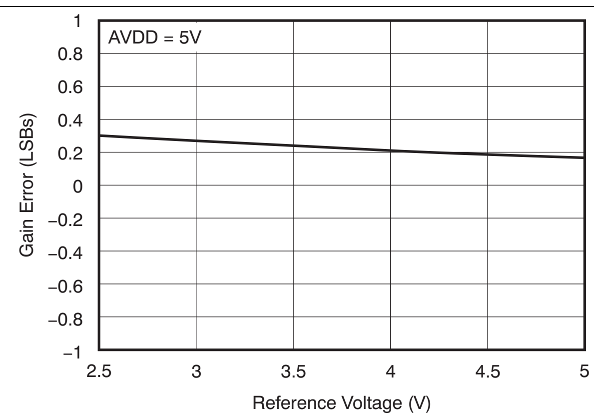


Figure 18. Gain Error vs Reference Voltage

Typical Characteristics: ADS7947 (12-Bit) (continued)

At T_A = 25°C, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS (unless otherwise noted)

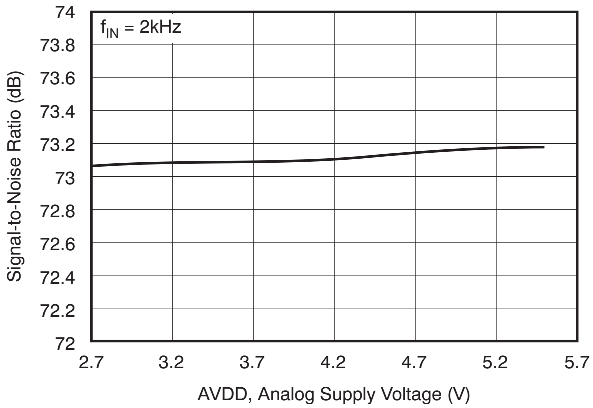


Figure 19. SNR vs Analog Supply Voltage

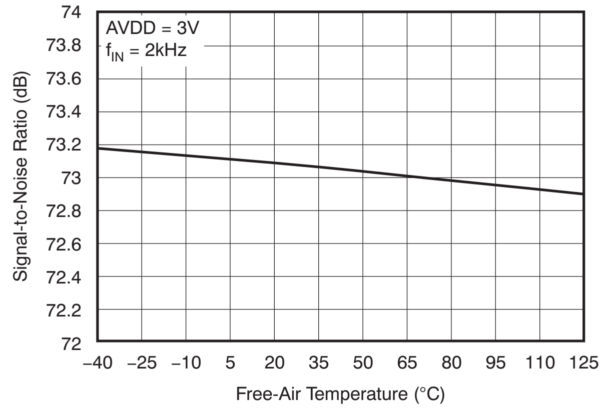


Figure 20. SNR vs Temperature

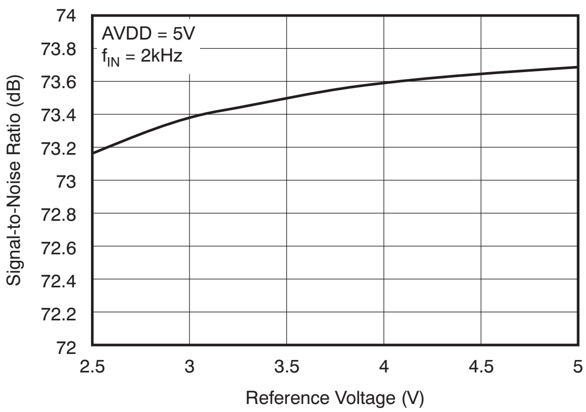


Figure 21. SNR vs Reference Voltage

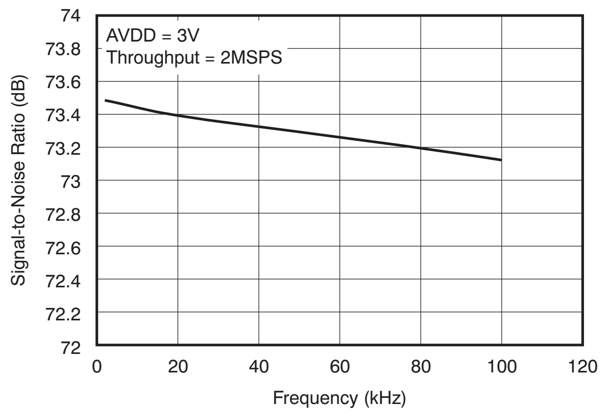


Figure 22. SNR vs Input Frequency

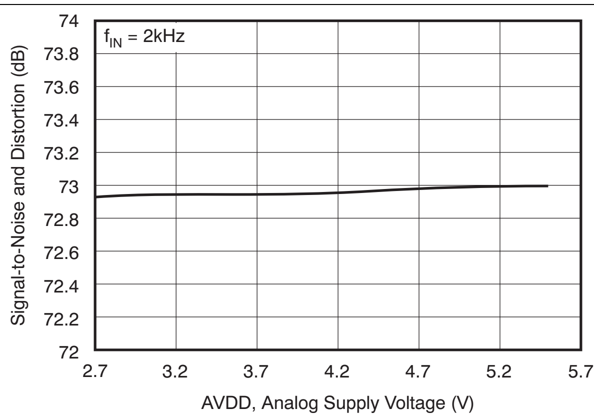


Figure 23. SINAD vs Analog Supply Voltage

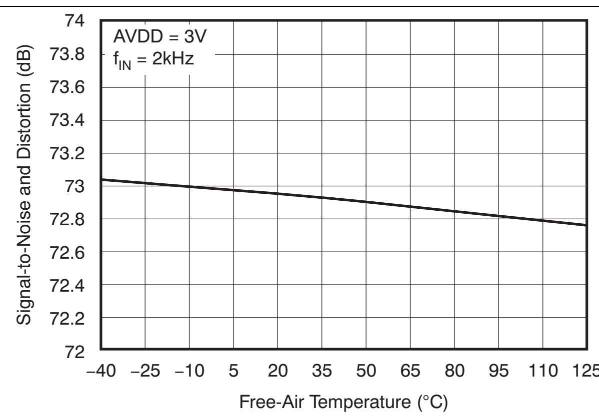


Figure 24. SINAD vs Temperature

Typical Characteristics: ADS7947 (12-Bit) (continued)

At T_A = 25°C, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS (unless otherwise noted)

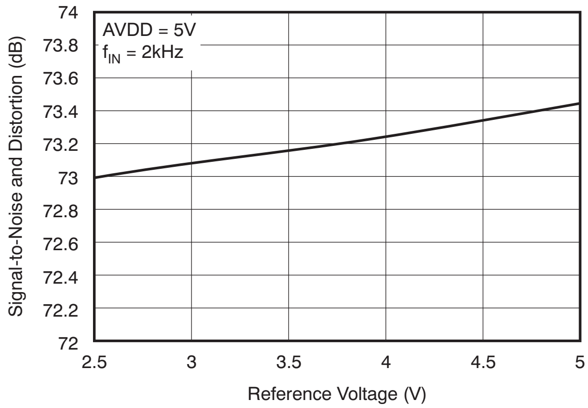


Figure 25. SINAD vs Reference Voltage

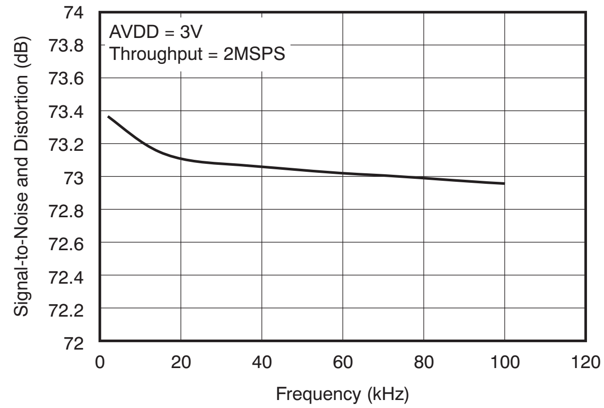


Figure 26. SINAD vs Input Frequency

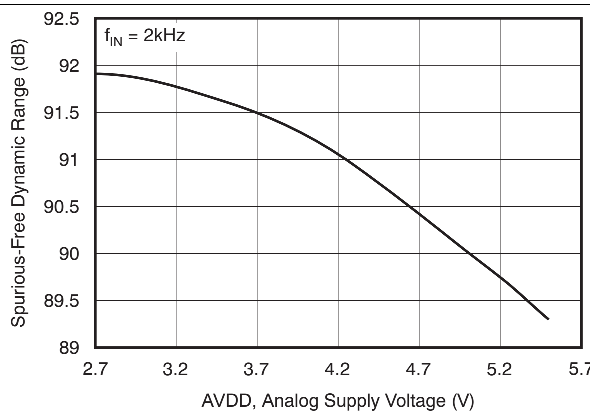


Figure 27. SFDR vs AVDD

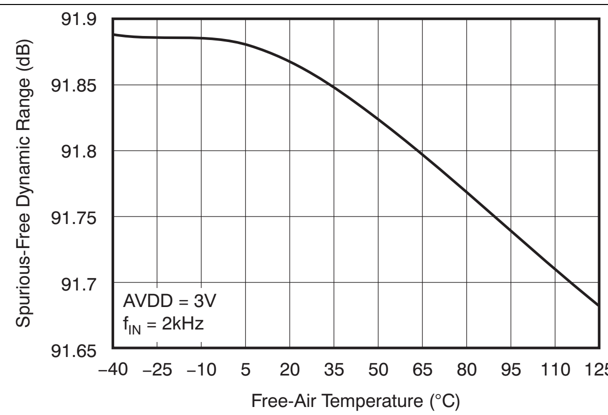


Figure 28. SFDR vs Temperature

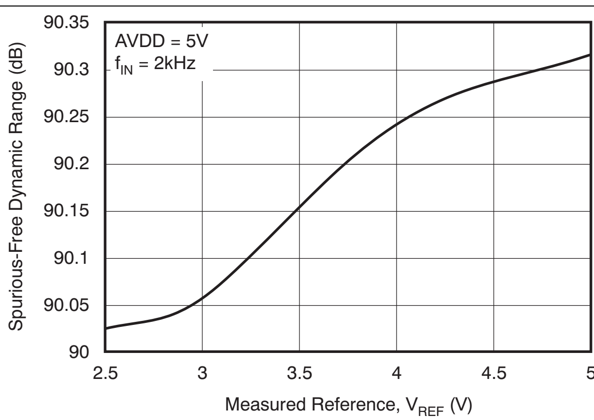


Figure 29. SFDR vs Reference Voltage

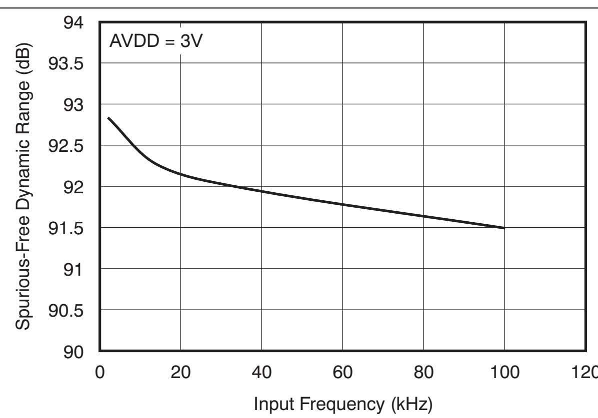


Figure 30. SFDR vs Input Frequency

Typical Characteristics: ADS7947 (12-Bit) (continued)

At T_A = 25°C, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS (unless otherwise noted)

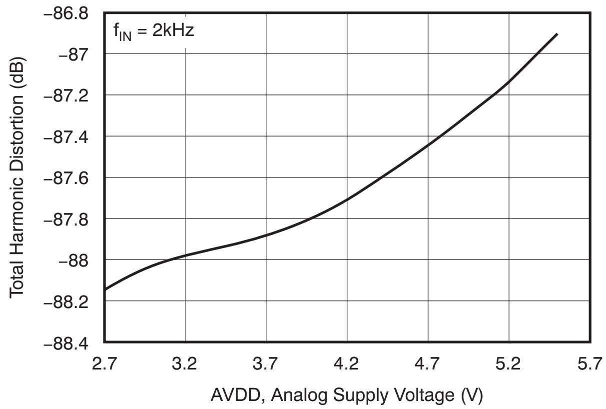


Figure 31. SFDR vs AVDD

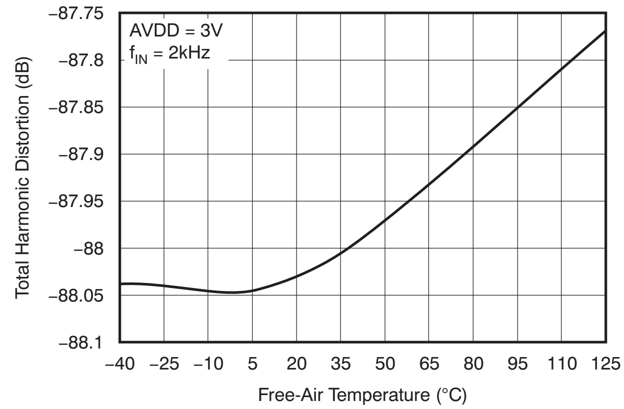


Figure 32. SFDR vs Temperature

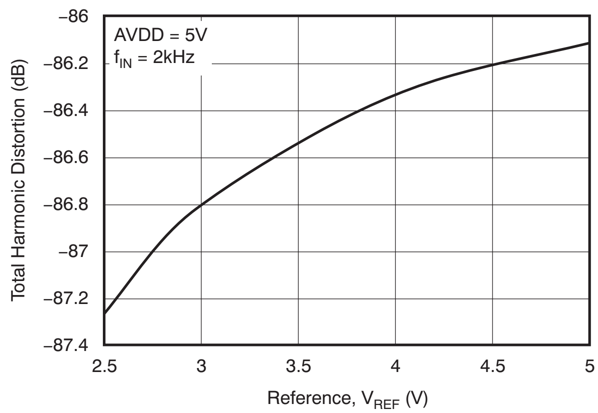


Figure 33. THD vs Reference Voltage

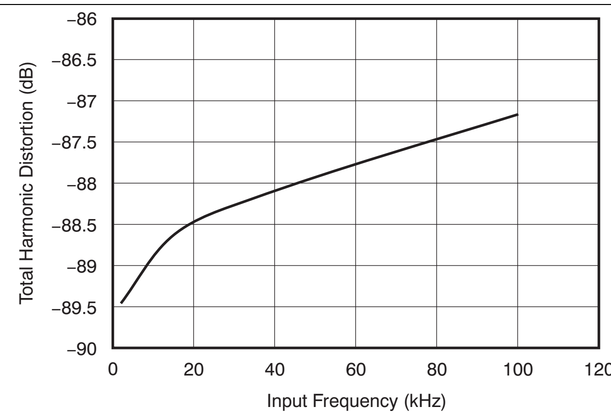
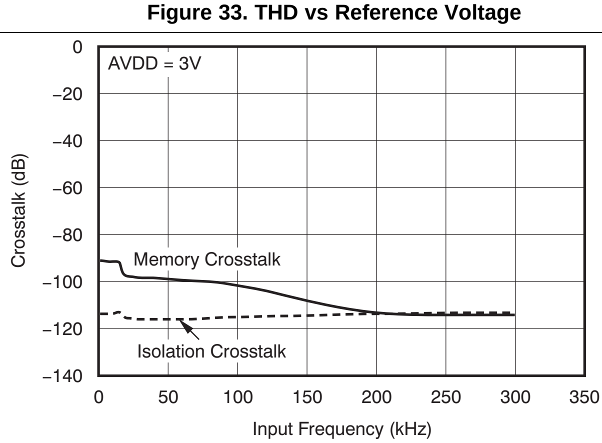


Figure 34. THD vs Input Frequency



Memory crosstalk is the effect of the last converted channel on the current converted channel data. Isolation crosstalk is the effect on the channel being converted that is coming from the signal on the channel that is off.

Figure 35. Crosstalk vs Input Frequency

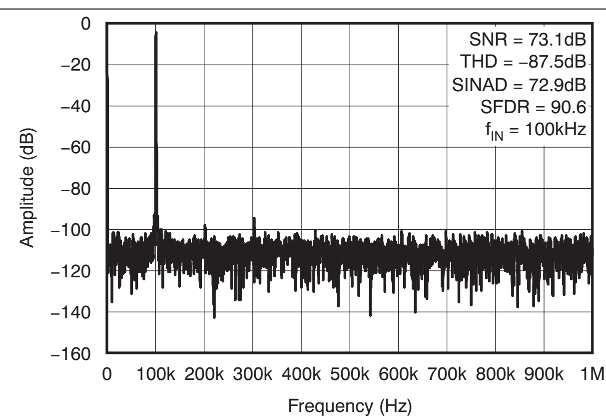


Figure 36. Spectral Response (8192-Point FFT)

Typical Characteristics: ADS7947 (12-Bit) (continued)

At T_A = 25°C, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS (unless otherwise noted)

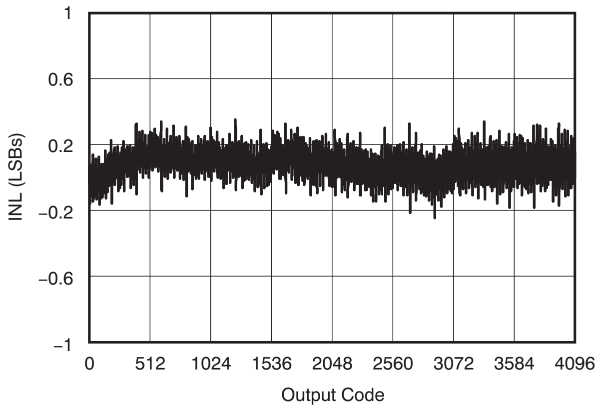


Figure 37. Typical INL

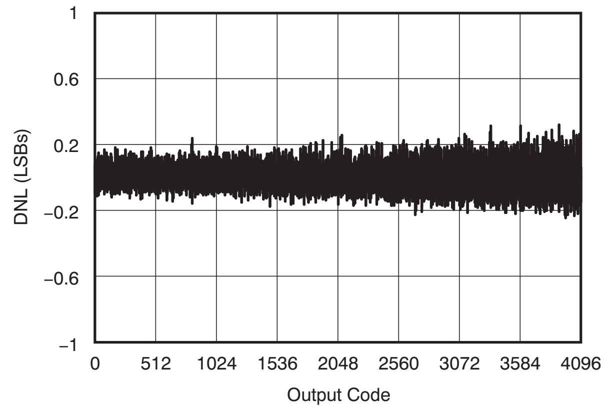


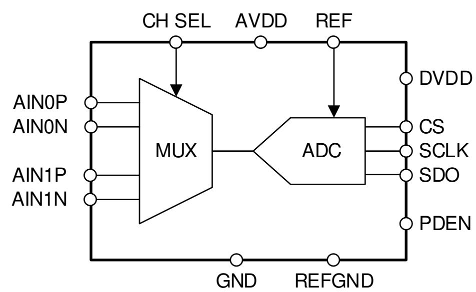
Figure 38. Typical DNL

8 Detailed Description

8.1 Overview

The ADS7947 is 12-bit, miniature, dual-channel, low-power successive-approximation register (SAR) analog-to-digital converter (ADC). The ADS7948 and ADS7949 are 10-bit and 8-bit devices, respectively, from the same product family. These devices feature low-power consumption at full-speed. The PDEN pin enables an auto power-down mode that further reduces power consumption at lower speeds.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Multiplexer and ADC Input

The devices feature pseudo-differential inputs with a double-pole, double-throw multiplexer. The negative inputs (AINxN) can accept swings of ±0.2 V; the positive inputs (AINxP) allow signals in the range of 0 V to V_{REF} over the negative input. The ADC converts the difference in voltage: $V_{AINxP} – V_{AINxN}$. This feature can be used in multiple ways.

Two signals can be connected from different sensors with unequal ground potentials (within ±0.2 V) to a single ADC. The pseudo-differential ADC rejects common-mode offset and noise. This feature also allows the use of a single-supply op amp. The signal and the AINxN input can be offset by +0.2 V, which provides the ground clearance needed for a single-supply op amp.

Feature Description (continued)

Figure 39 shows the electrostatic discharge (ESD) diodes to supply and ground at every analog input. Make sure that these diodes do not turn on by keeping the supply voltage within the specified input range.

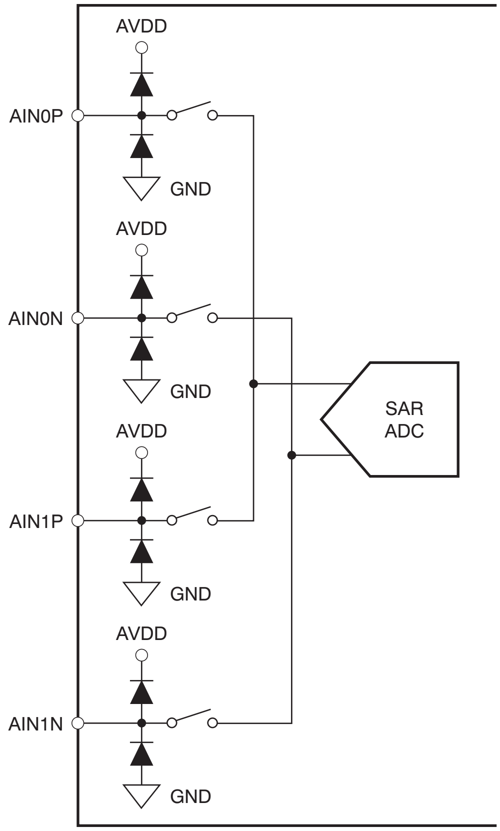


Figure 39. Analog Inputs

Figure 40 shows an equivalent circuit of the multiplexer and ADC sampling stage. The positive and negative inputs are separately sampled on 32-pF sampling capacitors. The multiplexer and sampling switches are represented by an ideal switch in series with a 12-Ω resistance. During sampling, the devices connect the 32-pF sampling capacitor to the ADC driver. This connection creates a glitch at the device input. TI recommends connecting a capacitor across the AINxP and AINxN terminals to reduce this glitch. A driving circuit must have sufficient bandwidth to settle this glitch within the acquisition time.

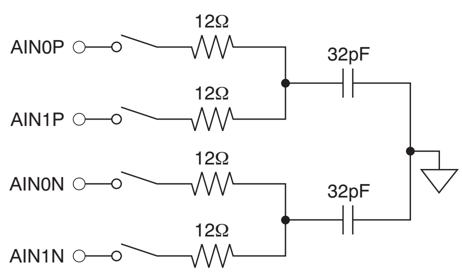
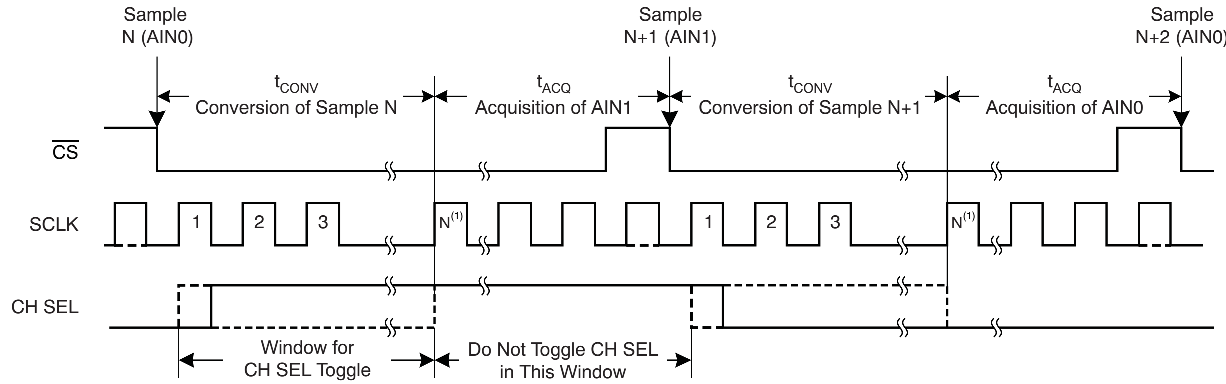


Figure 40. Input Sampling Stage Equivalent Circuit
(See the *Application Information* section for details on the driving circuit.)

Feature Description (continued)

Figure 41 shows a timing diagram for the ADC analog input channel selection. As shown in Figure 41, the CH SEL signal selects the analog input channel to the ADC. CH SEL = 0 selects channel 0 (AIN0P – AIN0N) and CH SEL = 1 selects channel 1 (AIN1P – AIN1N). It is recommended not to toggle the CH SEL signal during an ADC acquisition phase until the device detects the first valid SCLK rising edge after the device samples the analog input. If CH SEL is toggled during this period, an erroneous output code can result because the device might detect an unsettled analog input.

CH SEL can be toggled at any time during the window specified in Figure 41; however, TI recommends selecting the desired channel after the first SCLK rising edge and before the second SCLK rising edge. This timing ensures that the multiplexer output is settled before the ADC starts acquisition of the analog input.



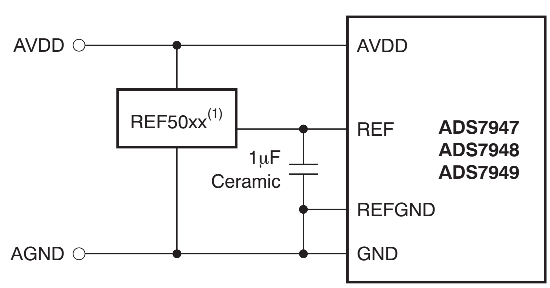
(1) *N* indicates the 14th SCLK rising edge for the ADS7947 (12 bit), the 11th rising edge for the ADS7948 (10 bit), and the ninth rising edge for the ADS7949 (8 bit).

Figure 41. ADC Analog Input Channel Selection

8.3.2 Reference

The ADS7947, ADS7948, and ADS7949 use an external reference voltage during the conversion of a sampled signal. The devices switch the capacitors used in the conversion process to the reference terminal during conversion. The switching frequency is the same as the SCLK frequency. The REF terminal must be decoupled to REFGND with a 1-µF ceramic capacitor in order to get the best noise performance from the device. The capacitor must be placed closest to these pins. The reference input can be driven with the REF50xx series precision references from TI. Figure 42 shows a typical reference driving circuit.

For convenience, AVDD can be used as a reference. The ADS794x allow reference ranges up to AVDD. However, make sure that AVDD is well-bypassed and that there is a separate bypass capacitor between REF and REFGND.



(1) Select the appropriate device as described by the required reference value. For example, select the REF5040 for a 4-V reference, the REF5030 for a 3-V reference, and the REF5025 for a 2.5-V reference. Ensure that (AVDD – REF) > 0.2 V so that the REF50xx functions properly.

Figure 42. Typical Reference Driving Circuit

Feature Description (continued)

8.3.3 Clock

The ADS794x use SCLK for conversions (typically 34 MHz). A lower frequency SCLK can be used for applications requiring sample rates less than 2 MSPS. However, using a 34-MHz SCLK and slowing down the device speed by choosing a lower frequency for $\overline{CS}$ is better, which allows more acquisition time. This configuration relaxes constraints on the output impedance of the driving circuit. See the *Application Information* section for a calculation of the driving circuit output impedance.

8.3.4 ADC Transfer Function

The ADS7947 (12 bit), ADS7948 (10 bit), and ADS7949 (8 bit) devices are unipolar, pseudo-differential input devices. The ADC output is in straight binary format. Figure 43 shows ideal characteristics for this family of devices. Here, FSR is the full-scale range for the ADC input (AINxP – AINxN) and is equal to the reference input voltage to the ADC (V_{REF}). 1 LSB is equal to (V_{REF} / 2^N) where *N* is the resolution of the ADC (for example, N = 12 for the ADS7947).

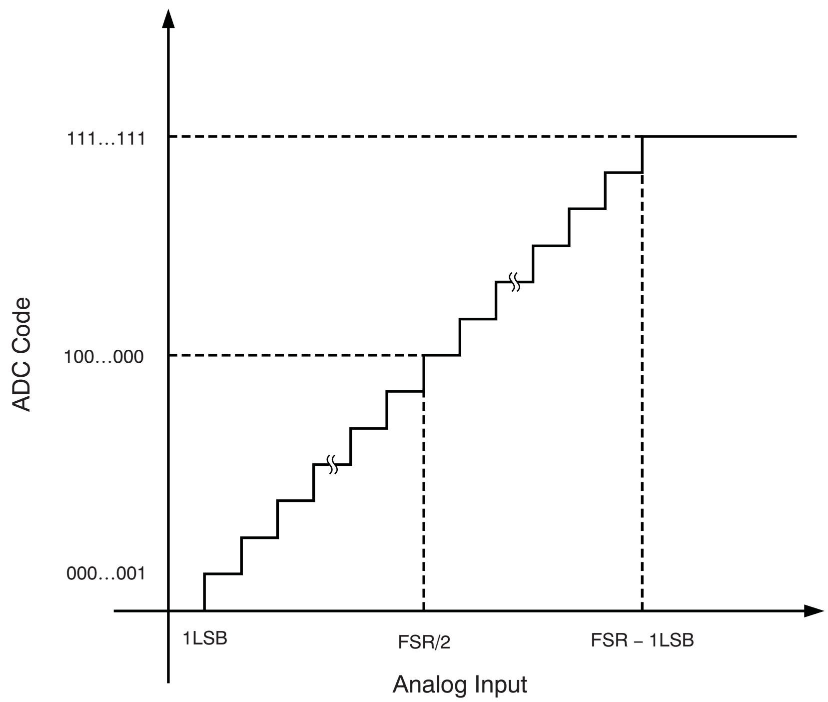


Figure 43. ADS7947, ADS7948, and ADS7949 Transfer Characteristics

8.3.5 Power-Down

The ADS7947, ADS7948, and ADS7949 family of devices offers an easy-to-use power-down feature available through a dedicated PDEN pin (pin 12). A high level on PDEN at the $\overline{CS}$ rising edge enables the power-down mode for that particular cycle. Figure 44 to Figure 46 illustrate device operation with power-down in both 32-clock and 16-clock mode.

Many applications must slow device operation. For speeds below approximately 500 kSPS, the 32-clock mode can be used with power-down. This capability results in considerable power savings.

As illustrated in Figure 44, PDEN is held at a logic '1' level. The device observes the PDEN status only at the $\overline{CS}$ rising edge; however, for continuous low-speed operation, continuously hold PDEN = 1. The devices detect power-down mode on the $\overline{CS}$ rising edge with PDEN = 1.

Feature Description (continued)

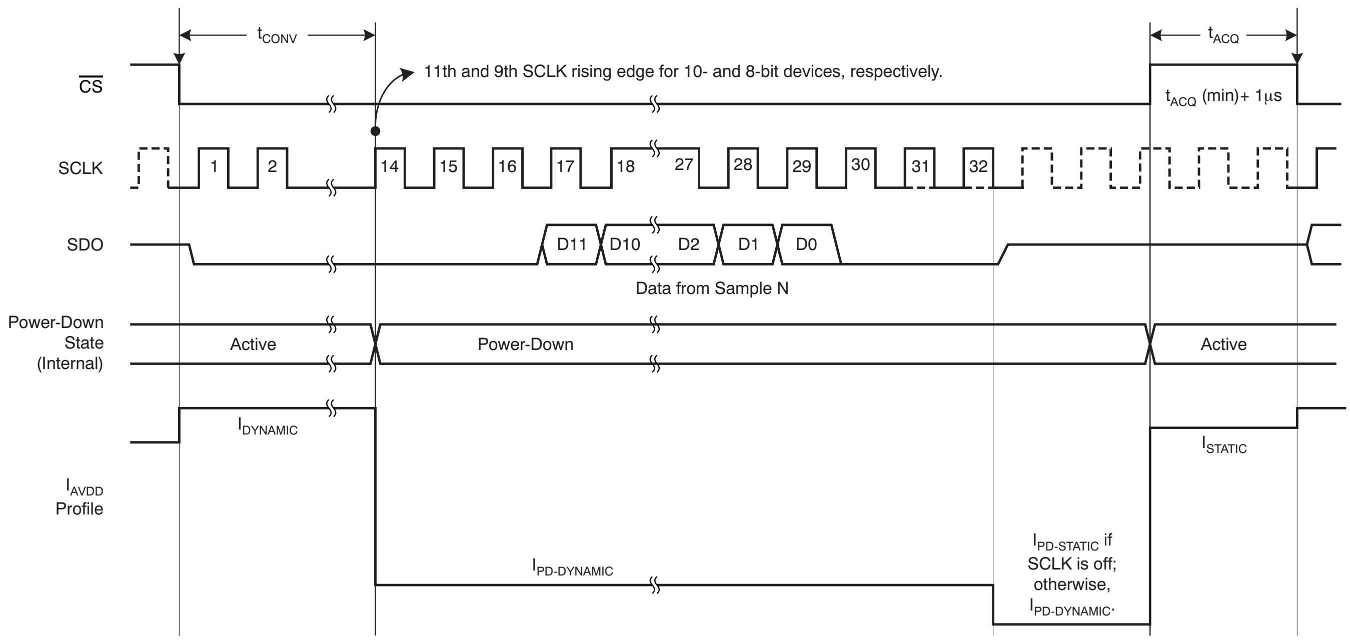


Figure 44. Operation With a 32-Clock Frame in Power-Down Mode (PDEN = 1)

On the $\overline{CS}$ falling edge, the devices start normal operation as previously described. The devices complete conversions on the 14th SCLK rising edge. (Conversions complete on the 11th and ninth SCLK rising edge for 10-bit and 8-bit devices, respectively.) The devices enter the power-down state immediately after conversions complete. However, the devices can still output data as per the timings described previously. The devices consume dynamic power-down current ($I_{PD\text{-}DYNAMIC}$) during data out operations. TI recommends stopping the clock after the 32nd SCLK falling edge to further save power down to the *static power-down current* level ($I_{PD\text{-}STATIC}$). The devices power up again on the SCLK rising edge. However, they require an extra 1µs to power up completely. $\overline{CS}$ must be high for the 1µs + t_{ACQ} (min) period.

In some applications, data collection is accomplished in burst mode. The system powers down after data collection. 16-clock mode is convenient for these applications. Figure 45 and Figure 46 detail power saving in 16-clock burst mode.

As illustrated in Figure 45, the two frames capturing the *N–1* and *Nth* samples are normal 16-clock frames. Keeping PDEN = 1 prior to the $\overline{CS}$ rising edge in the next frame ensures that the devices detect the power-down mode. Data from the Nth sample are read during this frame. The Nth sample represents the last data of interest in the burst of conversions. The devices enter power-down state after the end of conversions. This state is the 14th, 11th, or ninth SCLK rising edge for the 12-, 10-, and 8-bit devices, respectively. The clock can be stopped after the 14th SCLK falling edge; however, TI still recommends stopping the clock after the 16th SCLK falling edge. There must be no more than 29 SCLK falling edges during the $\overline{CS}$ low period. This limitation ensures that the devices remain in 16-clock mode.

The devices remain in a power-down state as long as $\overline{CS}$ is low. A $\overline{CS}$ rising edge with PDEN = 0 brings the devices out of the power-down state. Ensure that the $\overline{CS}$ high time for the first sample after power up is more than 1 µs + t_{ACQ} (min).

Feature Description (continued)

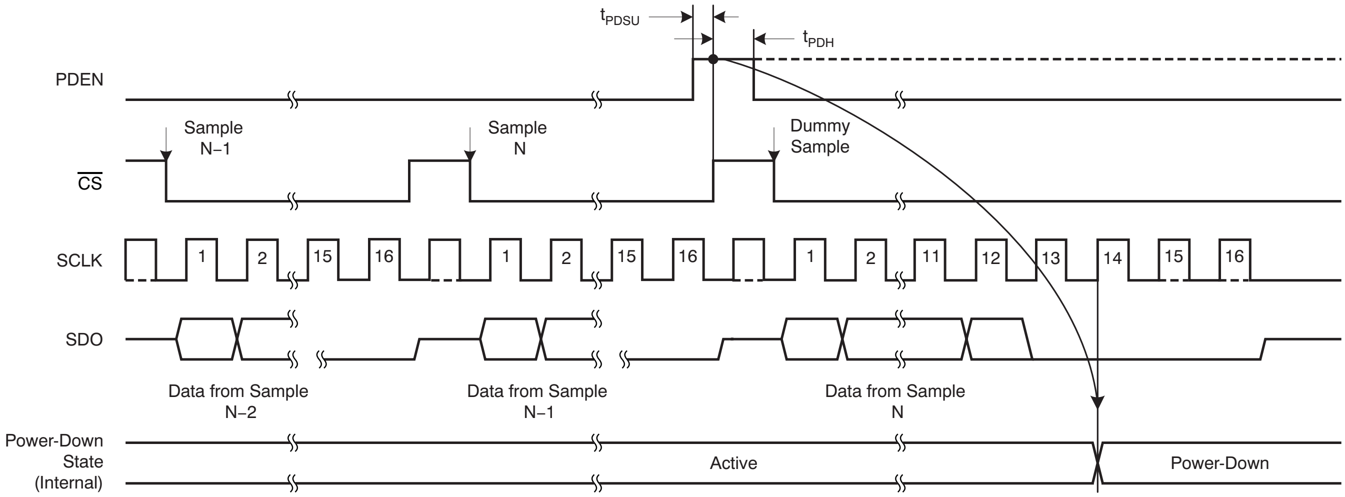


Figure 45. Entry Into Power-Down With 16-Clock Burst Mode

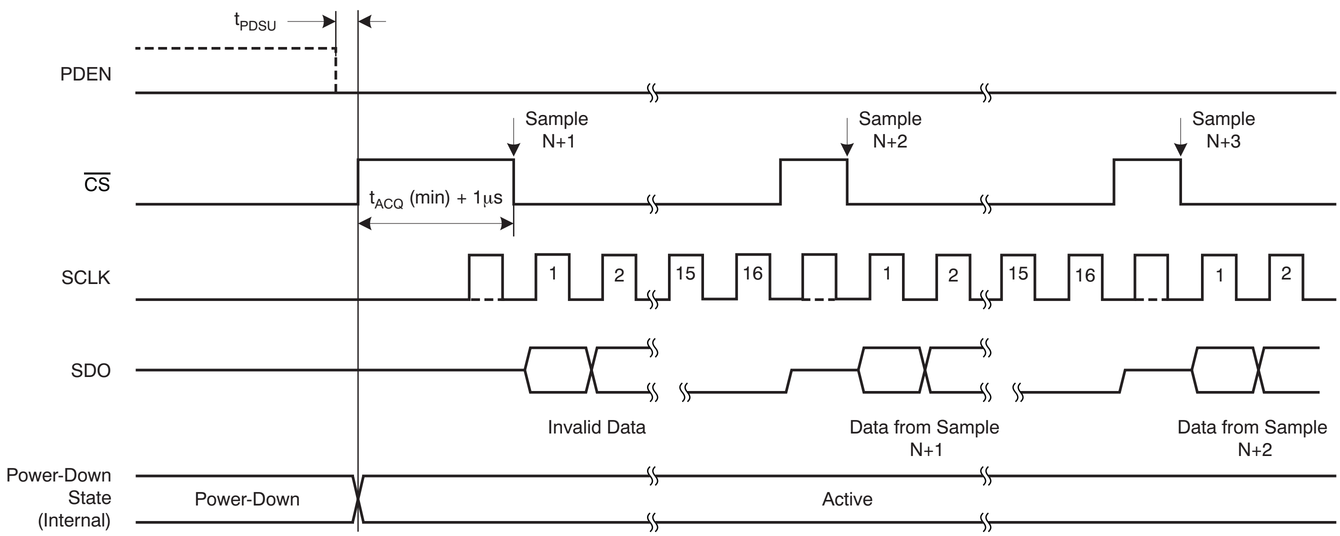


Figure 46. Exit From Power-Down With 16-Clock Burst Mode

8.4 Device Functional Modes

8.4.1 Device Operation

The ADS7947, ADS7948, and ADS7949 are typically operated with either a 16-clock frame or 32-clock frame for ease of interfacing with the host processor.

8.5 Programming

8.5.1 16-Clock Frame

Figure 47 through Figure 49 illustrate the devices operating in 16-clock mode. This mode is the fastest mode for device operation. In this mode, the devices output data from previous conversions while converting the recently sampled signal.

As shown in Figure 47, the ADS7947 starts acquisition of the analog input from the 14th rising edge of SCLK. The device samples the input signal on the CS falling edge. SDO comes out of 3-state and the device outputs the MSB on the CS falling edge. The device outputs the next lower SDO bits on every SCLK falling edge after the SCLK rising edge. The data correspond to the sample and conversion completed in the previous frame. During a CS low period, the device converts the recently sampled signal and uses SCLK for conversions. The number of clocks needed for a conversion for 12-bit and 8-bit devices are different. For the ADS7947, conversion is complete on the 14th SCLK rising edge. CS can be high at any time after the 14th SCLK rising edge. The CS rising edge after the 14th SCLK rising edge and before the 29th SCLK falling edge keeps the device in the 16-clock data frame. The device output goes to 3-state with CS high.

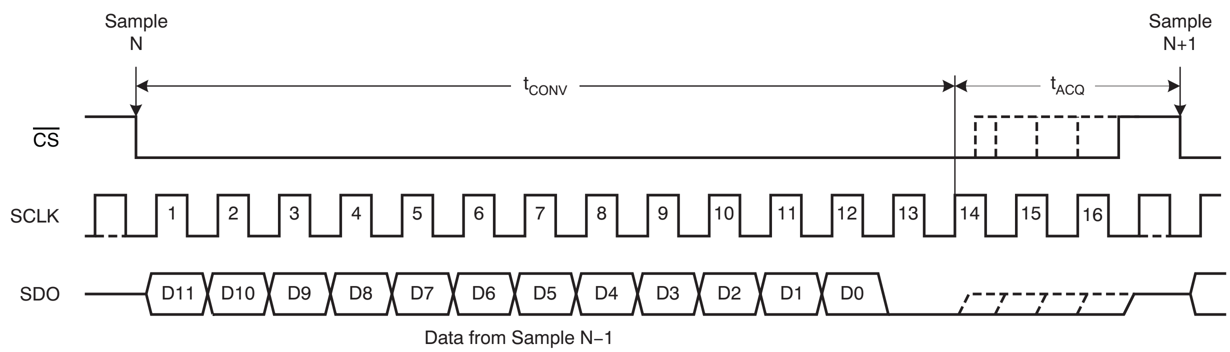


Figure 47. ADS7947 Operating in 16-Clock Mode Without Power-Down (PDEN = 0)

SCLK can also be stopped after the 14th SCLK rising edge.

Figure 48 and Figure 49 illustrate the 16-clock mode operation for the ADS7948 and ADS7949, respectively. The operation for these 10-bit and 8-bit devices is identical to the ADS7947 except that the conversion ends on different edges of SCLK. For the ADS7948, the conversion ends and acquisition starts on the 11th SCLK rising edge. For the ADS7949, the device uses the ninth SCLK rising edge for the conversion end and acquisition start. Similar to the ADS7947, CS can go high and SCLK can be stopped when the device enters acquisition.

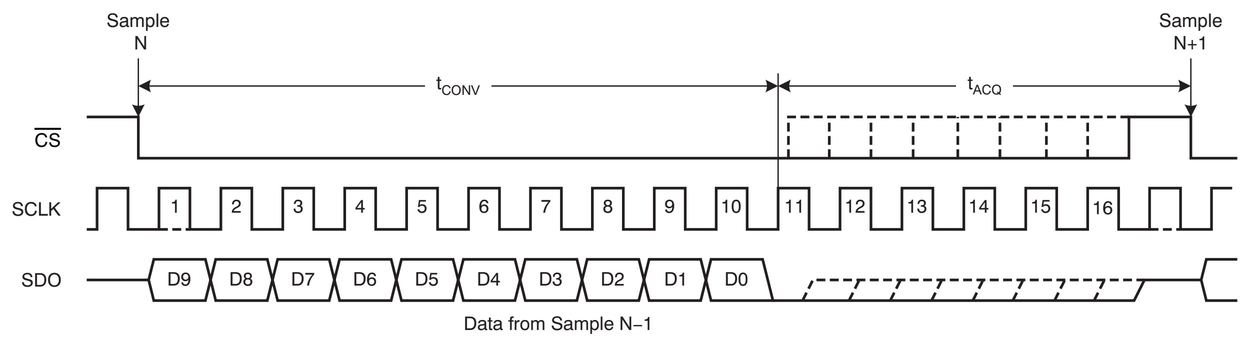


Figure 48. ADS7948 Operating in 16-Clock Mode Without Power-Down (PDEN = 0)

Programming (continued)

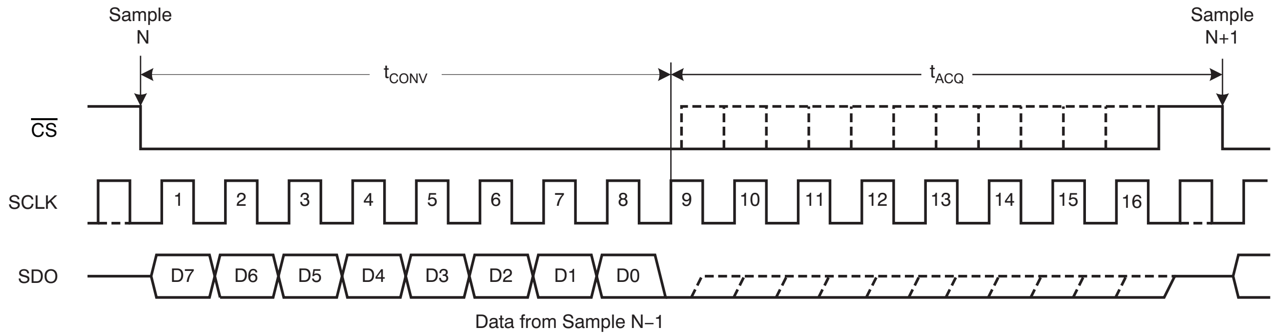


Figure 49. ADS7949 Operating in 16-Clock Mode Without Power-Down (PDEN = 0)

8.5.2 32-Clock Frame

Figure 50 through Figure 52 illustrate the devices operating in 32-clock mode. In this mode, the devices convert and output the data from the most recent sample before taking the next sample.

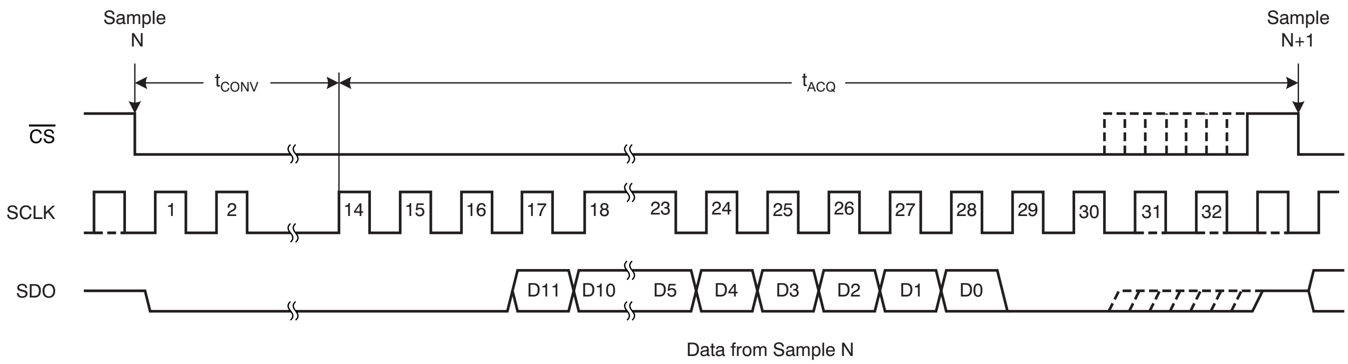


Figure 50. ADS7947 Operation in 32-Clock Frame Without Power-Down (PDEN = 0)

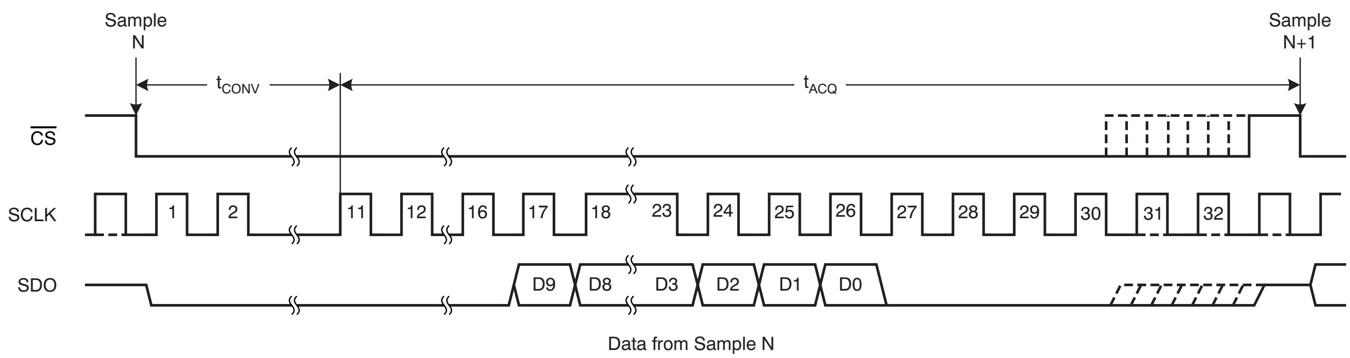


Figure 51. ADS7948 Operating in 32-Clock Frame Without Power-Down (PDEN = 0)

Programming (continued)

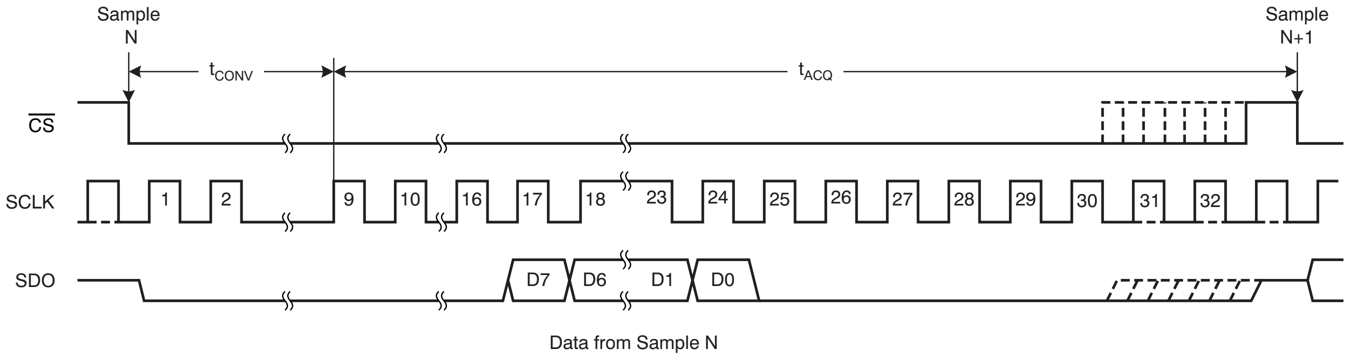


Figure 52. ADS7949 Operating in 32-Clock Frame Without Power-Down (PDEN = 0)

$\overline{CS}$ can be held low past the 16th falling edge of SCLK. The device continues to output recently converted data starting with the 16th SCLK falling edge. If $\overline{CS}$ is held low until the 30th SCLK falling edge, then the device detects 32-clock mode. The device data from recent conversions are already out with no latency before the 30th SCLK falling edge. When 32-clock mode is detected, the device outputs 16 zeros during the next conversion (in fact, for the first 16 clocks), unlike 16-clock mode where the device outputs the previous conversion result. SCLK can be stopped after the device has seen the 30th falling edge with $\overline{CS}$ low.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device employs a sample-and-hold stage at the input; see Figure 40 for a typical equivalent circuit of a sample-and-hold stage. The device connects a 32-pF sampling capacitor during sampling. This configuration results in a glitch at the input terminals of the device at the start of the sample. The external circuit must be designed in such a way that the input can settle to the required accuracy during the sampling time chosen. Figure 53 shows a typical driving circuit for the analog inputs.

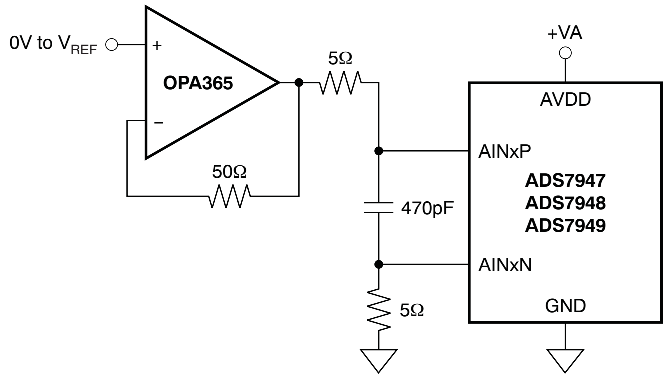


Figure 53. Typical Input Driving Circuit

Application Information (continued)

The 470-pF capacitor across the AINxP and AINxN terminals decouples the driving op amp from the sampling glitch. Splitting the series resistance of the input filter in two equal values is recommended, as shown in Figure 53. Both input terminals are recommended to have the same impedance from the external circuit. The low-pass filter at the input limits noise bandwidth of the driving op amp. Select the filter bandwidth so that the full-scale step at the input can settle to the required accuracy during the sampling time. Equation 1, Equation 2, and Equation 3 are useful for filter component selection.

$$\text{Filter Time Constant } (t_{AU}) = \frac{\text{Sampling Time}}{\text{Settling Resolution} \times \ln(2)}$$

Where:

Settling resolution is the accuracy in LSB to which the input needs to settle. A typical settling resolution for the 12-bit device is 13 or 14. (1)

$$\text{Filter Time Constant } (t_{AU}) = R \times C \quad (2)$$

$$\text{Filter Bandwidth} = \frac{1}{2 \times \pi \times t_{AU}} \quad (3)$$

Also, make sure the driving op amp bandwidth does not limit the signal bandwidth below filter bandwidth. In many applications, signal bandwidth can be much lower than filter bandwidth. In this case, an additional low-pass filter can be used at the input of the driving op amp. This signal filter bandwidth can be selected in accordance with the input signal bandwidth.

9.1.1 Driving an ADC Without a Driving Op Amp

There are some low input signal bandwidth applications, such as battery power monitoring or mains monitoring. For these applications, an ADC does not have to be operated at high sampling rates and, preferrably, avoid using a driving op amp from a cost perspective. In this case, the ADC input observes the impedance of the signal source (such as a battery or mains transformer). This section elaborates the effects of source impedance on sampling frequency.

Equation 1 can be rewritten as Equation 4:

$$\text{Sampling Time} = \text{Filter Time Constant} \times \text{Settling Resolution} \times \ln(2) \quad (4)$$

As shown in Figure 54, use a bypass capacitor across the positive and negative ADC input terminals.

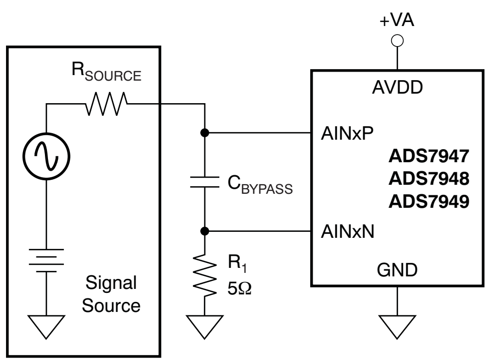


Figure 54. Driving an ADC Without a Driving Op Amp

Source impedance ($R_{SOURCE} + R_1$) with ($C_{BYPASS} + C_{SAMPLE}$) acts as a low-pass filter with Equation 5:

$$\text{Filter Time Constant} = (R_{SOURCE} + R_1) \times (C_{BYPASS} + C_{SAMPLE})$$

Where:

C_{SAMPLE} is the internal sampling capacitance of the ADC (equal to 32 pF). (5)

Table 1 lists the recommended bypass capacitor values and the filter time constant for different source resistances. Use a 10-pF bypass capacitor, at minimum.

Application Information (continued)

Table 1. Filter Time Constant versus Source Resistance

R_{SOURCE} (Ω)	R_{SOURCE} + R_1	APPROXIMATE C_{BYPASS} (pF)	C_{BYPASS} + C_{SAMPLE} (pF)	FILTER TIME CONSTANT (ns)
15	20	370	400	8
25	30	235	267	8
50	55	115	145	8
100	105	44	76	8
180	185	10	43.2	8
250	255	10	42	10.7
1000	1005	10	42	42.2
5000	5005	10	42	210.2

Typically, settling resolution is selected as (ADC resolution + 2). For the ADS7947 (12-bit) the ideal settling resolution is 14. Using equations Equation 2 and Equation 3, the sampling time can be easily determined for a given source impedance. This resolution allows 80 ns of sampling time for a 12-bit ADC with 8 ns of filter time constant, which matches the ADS7947 specifications. For source impedances above 180 Ω, the filter time constant continues to increase beyond the 8 ns required for an 80-ns sampling time. This incrementation increases the minimum permissible sampling time for the 12-bit settling and the device must be operated at a lower sampling rate.

The device sampling rate can be maximized by using a 34-MHz clock even for lower throughputs. Table 2 shows typical calculations for the ADS7947(12-bit).

Table 2. Sampling Frequency versus Source Impedance for the ADS7947 (12-Bit)

R_{SOURCE} (Ω)	C_{BYPASS} (pF)	SAMPLING TIME, t_{ACQ} (ns)	CONVERSION TIME, t_{CONV} (ns)	CYCLE TIME, t_{ACQ} + t_{CONV} (ns)	SAMPLING RATE (MSPS)
180	10	80	397 (with 34MHz clock)	477	2
250	10	107	397 (with 34MHz clock)	504	1.98
1000	10	422	397 (with 34MHz clock)	819	1.2
5000	10	2102	397 (with 34MHz clock)	2499	0.4

An 1000-ns additional sampling time must be allowed over what is shown in Table 2 if PDEN (pin 12) is set high.

10 Power Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges. Decouple the AVDD and DVDD pins individually with 1-µF ceramic decoupling capacitors. The decoupling capacitors must be placed as close as possible to the device.

11 Layout

11.1 Layout Guidelines

ADCs are mixed-signal devices. For maximum performance, proper decoupling, grounding, and proper termination of digital signals is essential. Figure 55 shows the essential components around the ADC. All capacitors shown are ceramic. These decoupling capacitors must be placed close to the respective signal pins.

There is a 47-Ω *source series termination* resistor shown on the SDO signal. This resistor must be placed as close to pin 15 as possible. Series terminations for SCLK and $\overline{CS}$ must be placed close to the host.

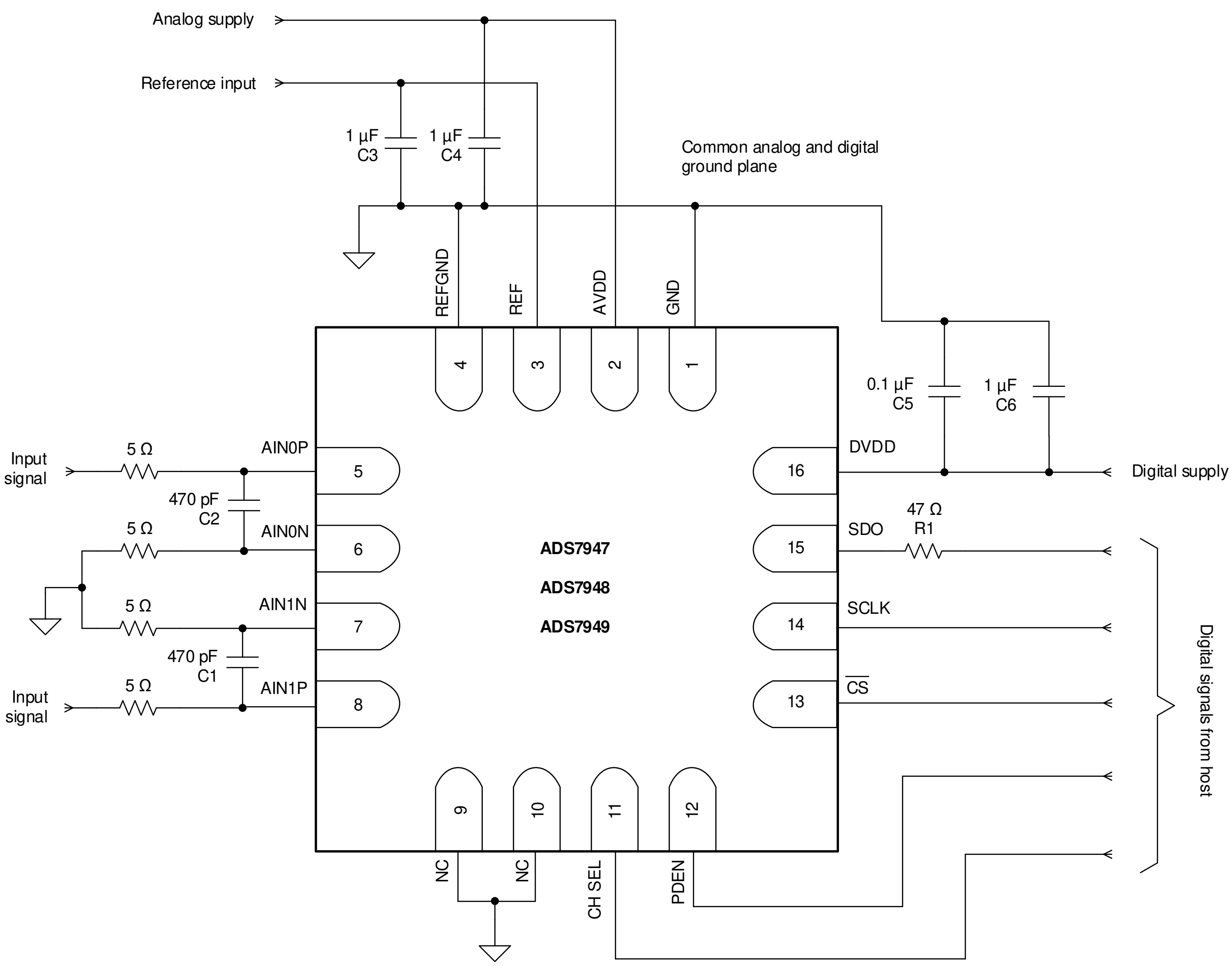


Figure 55. Recommended ADC Schematic

11.2 Layout Example

A common ground plane for both analog and digital often gives better results. Typically, the second PCB layer is the ground plane. The ADC ground pins are returned to the ground plane through multiple vias (PTH). Good practice is to place analog components on one side and digital components on other side of the ADC (or ADCs). All signals must be routed, assuming there is a split ground plane for analog and digital. Furthermore, splitting the ground initially during layout is better. Route all analog and digital traces so that the traces see the respective ground all along the second layer. Then short both grounds to form a common ground plane. Figure 56 shows a typical layout around the ADC.

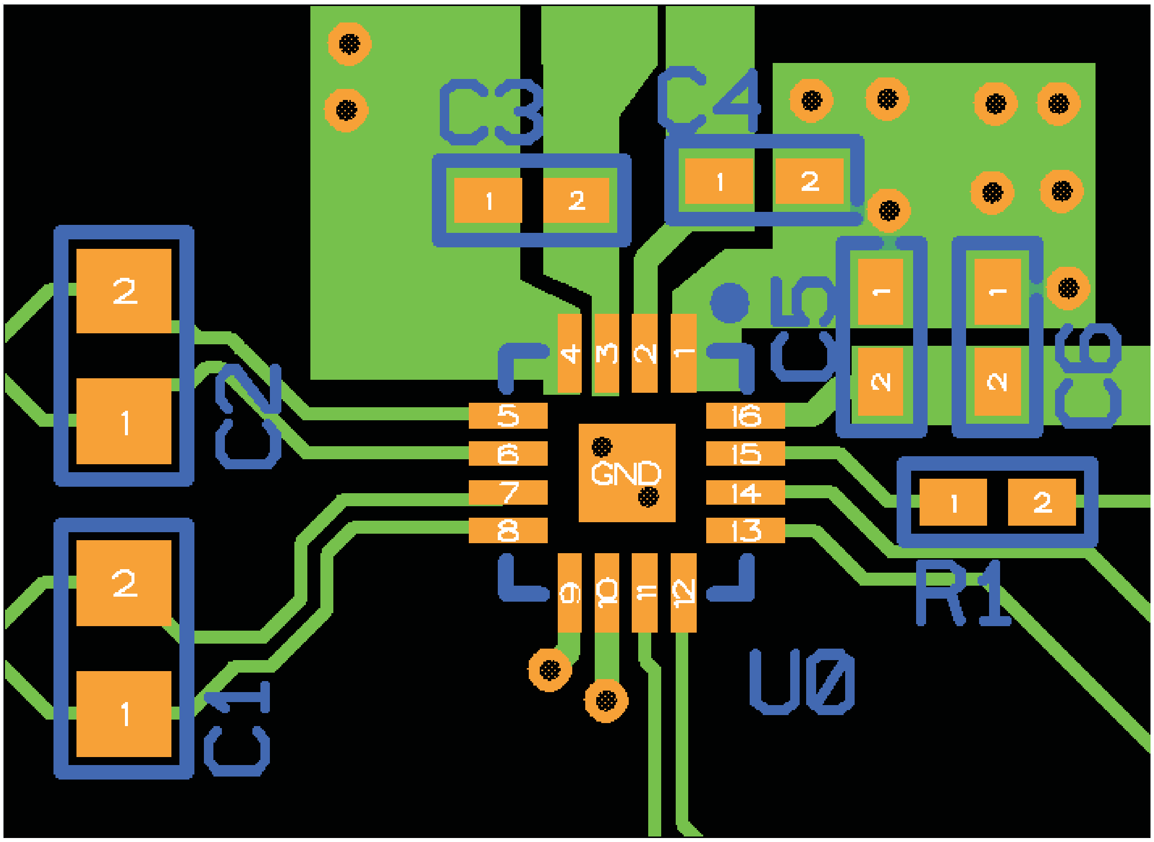


Figure 56. Recommended ADC Layout
(Only top layer is shown, second layer is common ground for analog and digital)

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 **3.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
ADS7947	单击此处	单击此处	单击此处	单击此处	单击此处
ADS7948	单击此处	单击此处	单击此处	单击此处	单击此处
ADS7949	单击此处	单击此处	单击此处	单击此处	单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 商标

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12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7947SRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7947	Samples
ADS7947SRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7947	Samples
ADS7948SRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7948	Samples
ADS7948SRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7948	Samples
ADS7949SRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7949	Samples
ADS7949SRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7949	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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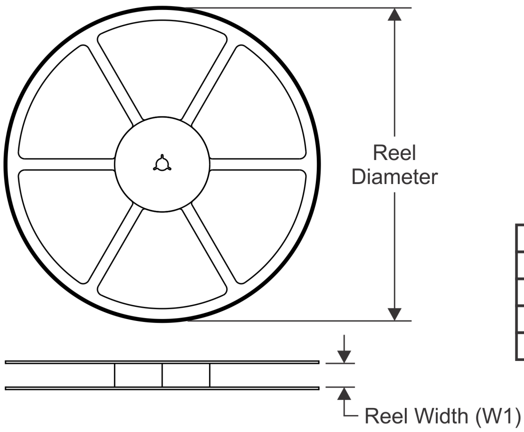
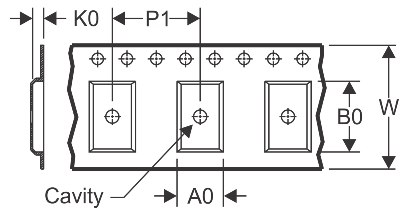
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

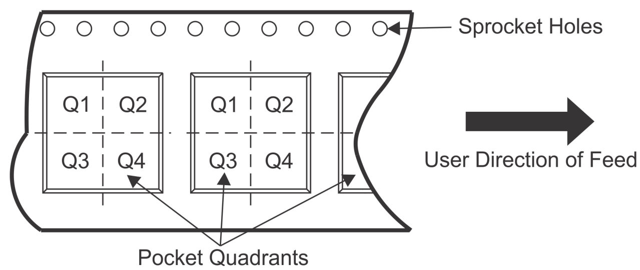


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

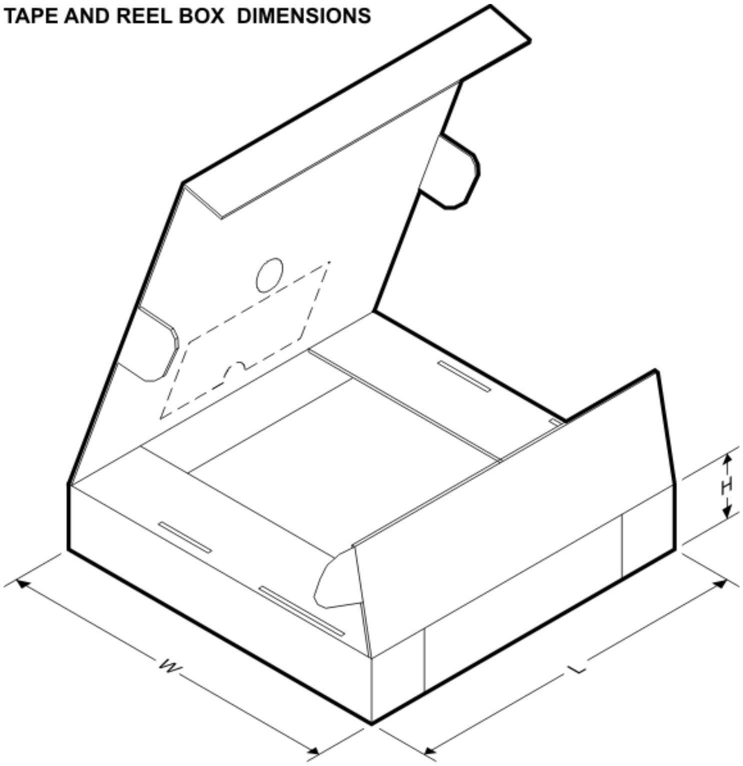
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7947SRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7947SRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7948SRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7948SRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7949SRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7949SRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7947SRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7947SRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS7948SRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7948SRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS7949SRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7949SRTET	WQFN	RTE	16	250	210.0	185.0	35.0

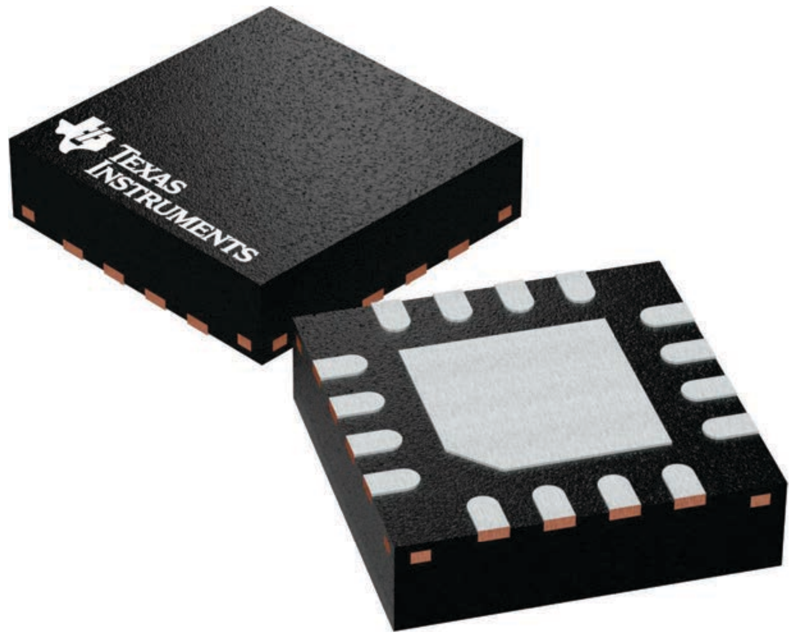
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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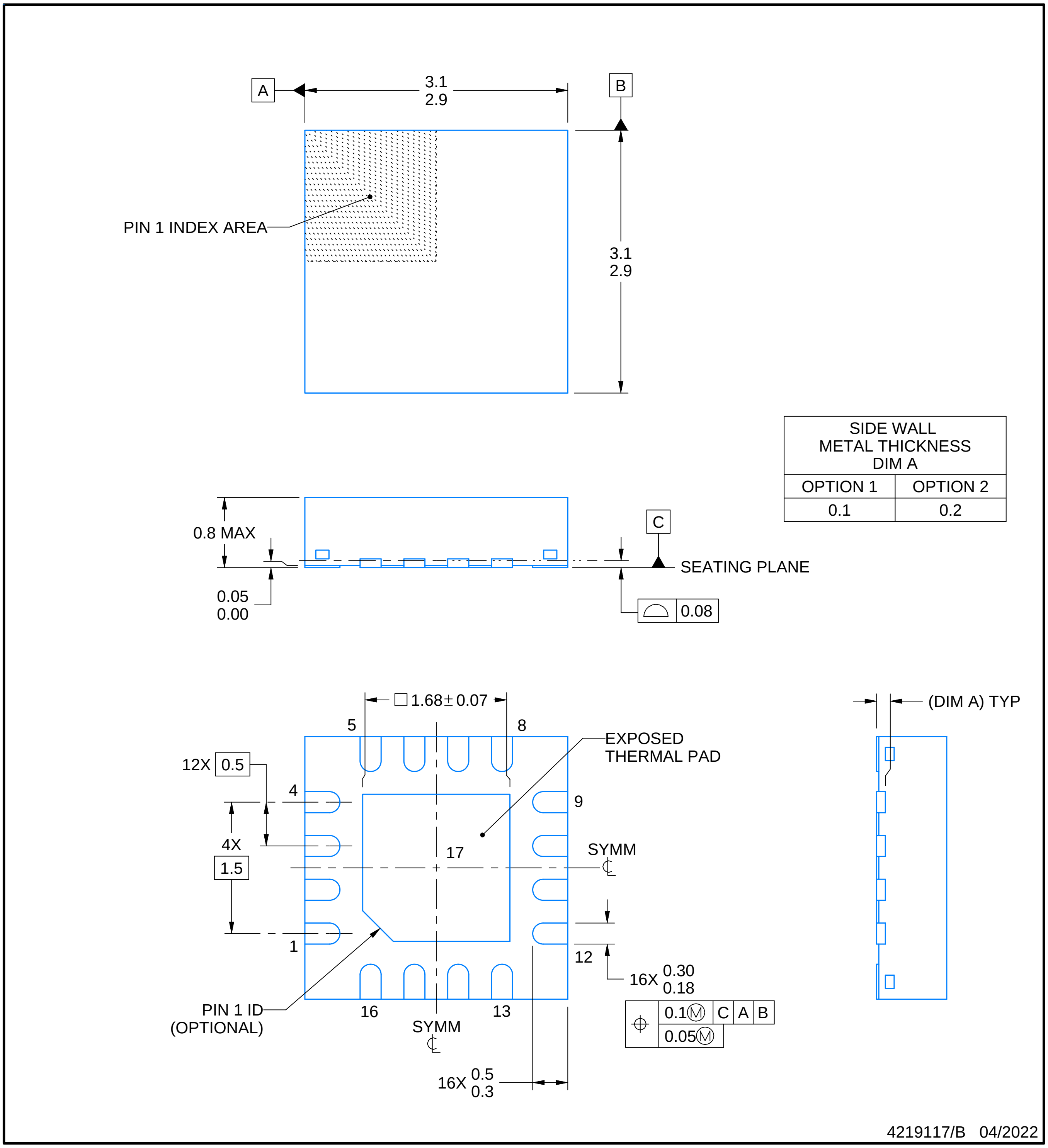
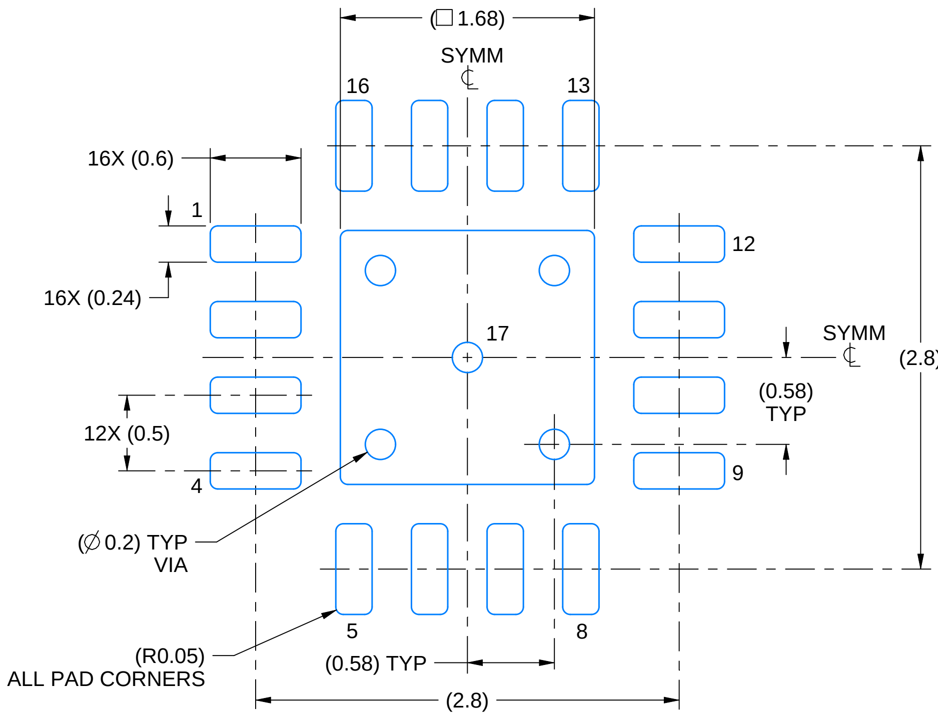
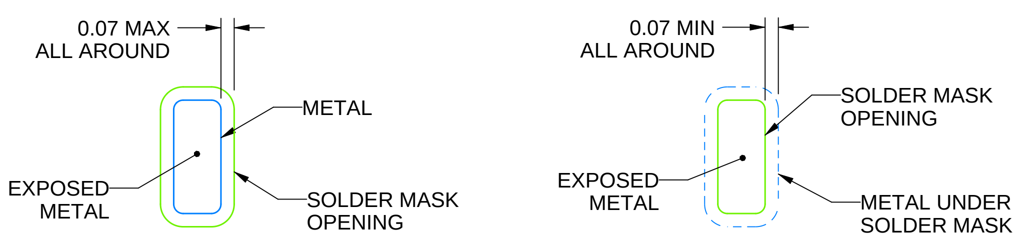


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

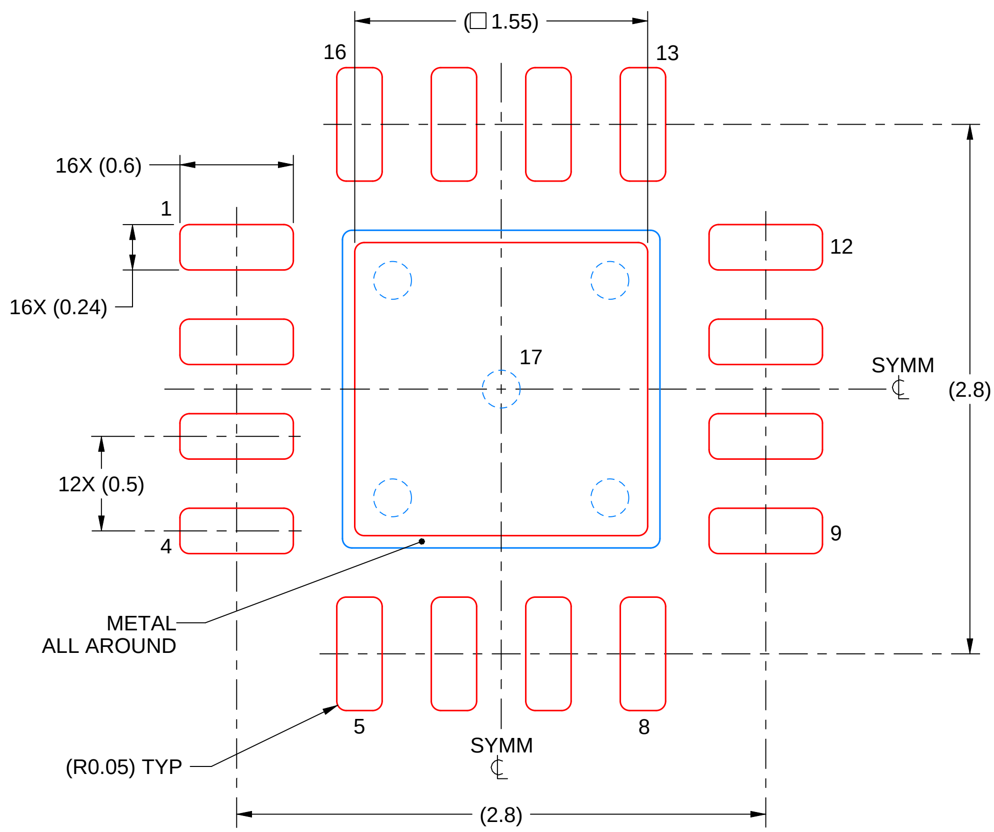
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265