

## TPS65295 完整 DDR4 存储器电源解决方案

### 1 特性

- 同步降压转换器 (VDDQ)
  - 输入电压范围: 4.5V 至 18V
  - 输出电压固定为 1.2V
  - D-CAP3™模式控制, 用于快速瞬态响应
  - 持续输出电流: 8A
  - 高级 Eco-mode™脉冲跳跃
  - 集成 22mΩ 和 8.6mΩ  $R_{DS(on)}$  内部电源开关
  - 600kHz 开关频率
  - 内部软启动: 1.6ms
  - 逐周期过流保护
  - 锁存输出 OV 和 UV 保护
- 同步降压转换器 (VPP)
  - 输入电压范围: 3V 至 5.5V
  - 输出电压固定为 2.5V
  - D-CAP3™模式控制, 用于快速瞬态响应
  - 持续输出电流: 1A
  - 高级 Eco-mode™脉冲跳跃
  - 集成 150mΩ 和 120mΩ  $R_{DS(on)}$  内部电源开关
  - 580kHz 开关频率
  - 内部软启动: 1ms
  - 逐周期过流保护
  - 锁存输出 OV 和 UV 保护
- 1A LDO (VTT)
  - 1A 持续灌电流和拉电流
  - 仅需 10μF 的陶瓷输出电容
  - 在 S3 状态下支持高阻态输出
  - ±30mV VTT 输出精度 (直流 + 交流)
- 缓冲基准 (VTTREF)
  - 经缓冲的低噪声 ±10mA 功能
  - 0.8% 输出精度
- 低静态电流: 150μA
- 电源正常指示器
- 输出放电功能
- 加电和断电排序控制
- 非锁存 OT 和 UVLO 保护
- 18 引脚 3.0mm × 3.0mm HotRod™VQFN 封装

### 2 应用

- DDR4 存储器电源
- 笔记本电脑、台式机和服务器
- 超极本、平板电脑
- 单板计算机、模块化计算机

### 3 说明

TPS65295 器件能够以最低的总成本和最小的空间为 DDR4 存储器系统提供完整的电源解决方案。它符合 JEDEC 标准中的 DDR4 加电和断电顺序要求。TPS65295 将两个同步降压转换器 (VPP 和 VDDQ) 与 1A 灌电流和拉电流跟踪 LDO (VTT) 以及缓冲低噪声基准 (VTTREF) 集成在一起。TPS65295 采用耦合了 600kHz 开关频率的 D-CAP3™模式, 此模式可在无需外部补偿电路的情况下实现易于使用的快速瞬变并支持陶瓷输出电容器。

VTTREF 跟踪  $\frac{1}{2}$  VDDQ 的精度优于 0.8%。VTT 可同时提供 1A 持续灌电流和拉电流功能, 而仅需 10μF 的陶瓷输出电容。

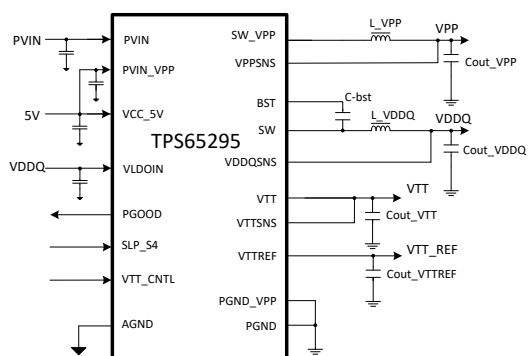
TPS65295 可提供丰富的功能和卓越的电源性能。它支持灵活功耗状态控制, 将 VTT 置于高阻抗状态 (处于 S3) 并在 S4/S5 状态下对 VDDQ、VTT 和 VTTREF 进行放电。另外还提供 OVP、UVP、OCP、UVLO 和热关断保护。此器件采用热增强型 18 引脚 HotRod™VQFN 封装, 额定结温范围为 -40°C 至 125°C。

#### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPS65295	VQFN (18)	3.00mm × 3.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

#### 典型应用



## 目录

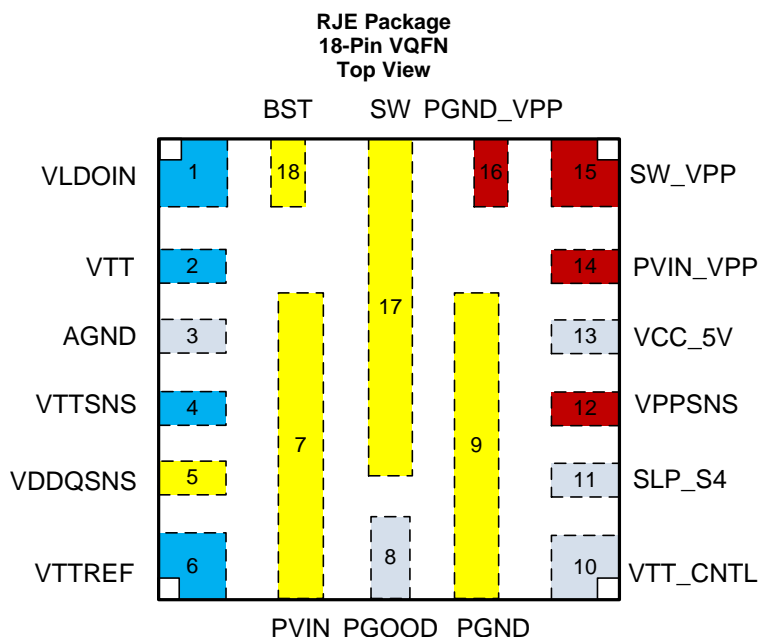
<b>1</b>	<b>特性</b> .....	<b>1</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>18</b>
<b>2</b>	<b>应用</b> .....	<b>1</b>	8.1	Application Information.....	18
<b>3</b>	<b>说明</b> .....	<b>1</b>	8.2	Typical Application .....	18
<b>4</b>	<b>修订历史记录</b> .....	<b>2</b>	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>25</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>10</b>	<b>Layout</b> .....	<b>26</b>
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	10.1	Layout Guidelines .....	26
6.1	Absolute Maximum Ratings .....	4	10.2	Layout Example .....	26
6.2	ESD Ratings .....	4	<b>11</b>	<b>器件和文档支持</b> .....	<b>27</b>
6.3	Recommended Operating Conditions .....	4	11.1	器件支持 .....	27
6.4	Thermal Information .....	5	11.2	接收文档更新通知 .....	27
6.5	Electrical Characteristics .....	5	11.3	社区资源 .....	27
6.6	Typical Characteristics .....	8	11.4	商标 .....	27
<b>7</b>	<b>Detailed Description</b> .....	<b>13</b>	11.5	静电放电警告 .....	27
7.1	Overview .....	13	11.6	术语表 .....	27
7.2	Functional Block Diagram .....	14	<b>12</b>	<b>机械、封装和可订购信息</b> .....	<b>27</b>
7.3	Feature Description .....	15	12.1	Package Option Addendum .....	28
7.4	Device Functional Modes .....	17			

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 2 月	*	初始发行版。

## 5 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
VLDOIN	1	P	Power supply input for VTT LDO. Connect VDDQ in typical application.
VTT	2	O	VTT 1-A LDO output. Recommend to connect to 10- $\mu$ F or larger capacitance for stability.
AGND	3	G	Signal ground.
VTTSENS	4	I	VTT output voltage feedback.
VDDQSNS	5	I	VDDQ output voltage feedback.
VTTREF	6	O	Buffered VTT reference output. Recommend to connect to 0.22- $\mu$ F or larger capacitance for stability.
PVIN	7	P	Input power supply for VDDQ buck.
PGOOD	8	O	Power good signal open-drain output. PGOOD goes high when VPP and VDDQ output voltage are within the target range.
PGND	9	G	Power ground for VDDQ buck.
VTT_CNTL	10	I	VTT_CNTL signal input for VTT LDO enable control. For detail control setup, please refer to <a href="#">表 1</a> .
SLP_S4	11	I	SLP_S4 signal input for VDDQ buck and VPP buck enable control. For detail control setup, please refer to <a href="#">表 1</a> .
VPPSNS	12	I	VPP output voltage feedback.
VCC_5V	13	P	Power supply for VPP and VDDQ buck converter control logic circuit.
PVIN_VPP	14	P	Input power supply for VPP buck.
SW_VPP	15	O	VPP switching node connection to the inductor and bootstrap capacitor.
PGND_VPP	16	G	Power ground for VPP buck.
SW	17	O	VDDQ switching node connection to the inductor and bootstrap capacitor.
BST	18	I	High-side MOSFET gate driver bootstrap voltage input for VDDQ buck. Connect a capacitor between the BST pin and the SW pin.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage	PVIN	-0.3	20	V
	VBST	-0.3	25	V
	VBST-SW	-0.3	6	V
	VTT_CNTL, SLP_S4, VCC_5V, PVIN_VPP, VLDOIN, VDDQSNS, VTTSNS, VPPSNS	-0.3	6	V
	PGND, AGND, PGND_VPP	-0.3	0.3	V
Output voltage	SW DC	-0.3	20	V
	SW (20-ns transient)	-3	22	V
	SW_VPP DC	-0.3	7	V
	SW_VPP (20-ns transient)	-3	8	V
	PGOOD, VTT, VTTREF	-0.3	6	V
T <sub>J</sub>	Operating junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22- V C101 <sup>(2)</sup>	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	PVIN	4.5	18	V
	VBST	-0.3	23	V
	VBST-SW	-0.3	5.5	V
	VTT_CNTL, SLP_S4, VCC_5V, PVIN_VPP, VLDOIN, VDDQSNS, VTTSNS, VPPSNS	-0.3	5.5	V
	PGND, AGND, PGND_VPP	-0.3	0.3	V
Output voltage	SW DC	-0.3	18	V
	SW (20-ns transient)	-3	20	V
	SW_VPP DC	-0.3	5.5	V
	SW_VPP (20-ns transient)	-3	6.5	V
	PGOOD, VTT, VTTREF	-0.3	5.5	V
I <sub>VDDQOUT</sub>	VDDQ Output current		8	A
T <sub>J</sub>	Operating junction temperature	-40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS65295	UNIT
		RJE (VQFN)	
		18 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	58.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	26.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	17.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	17.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

T<sub>J</sub> = -40°C to 125°C, V<sub>PVIN</sub> = 12V, V<sub>PVIN\_VPP</sub> = 5V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT SUPPLY VOLTAGE</b>					
I <sub>VCC_5V</sub>	V <sub>S4</sub> = V <sub>TT_CNTL</sub> = 0 V		5		μA
	V <sub>S4</sub> = 5 V, V <sub>TT_CNTL</sub> = 0 V, no load		110		μA
	V <sub>S4</sub> = V <sub>TT_CNTL</sub> = 5 V, no load		150		μA
V <sub>IN</sub>	PVIN input voltage range	4.5		18	V
<b>UVLO</b>					
UVLO	Wake up VCC_5V voltage		4.1	4.5	V
	Shut down VCC_5V voltage	3.3	3.6		V
	Hysteresis VCC_5V voltage		500		mV
<b>VDDQ</b>					
V <sub>VDDQSNS</sub>	VDDQ sense voltage	1.188	1.2	1.212	V
I <sub>VDDQSNS</sub>	VDDQSNS input current		40		μA
I <sub>VDDQDIS</sub>	VDDQ discharge current		12		mA
t <sub>VDDQSS</sub>	VDDQ soft-start time		1.6	2.65	ms
t <sub>VDDQDLY</sub>	VDDQ ramp up delay time		2		ms
R <sub>DSONH</sub>	High-side switch resistance		22		mΩ
R <sub>DSONL</sub>	Low-side switch resistance		8.6		mΩ
I <sub>VDDQOCL</sub>	Low-side valley current limited	8.2	9.8	11.5	A
f <sub>sw</sub>	VDDQ switching frequency		600		kHz
t <sub>OFF(MIN)</sub>	Minimum off time		198		ns
<b>PGOOD (VDDQ, VPP)</b>					
V <sub>THPG</sub>	VDDQSNS / VPPSNS falling (Fault)		87		%
	VDDQSNS / VPPSNS rising (Good)		93		%
	VDDQSNS / VPPSNS rising (Fault)		115		%
	VDDQSNS / VPPSNS falling (Good)		110		%
I <sub>PGMAX</sub>	PG sink current		46		mA
t <sub>PGDLY</sub>	PG start-up delay		1		ms
<b>VPP</b>					
V <sub>VPPSNS</sub>	VPP sense voltage	2.45	2.5	2.55	V
I <sub>VPPSNS</sub>	VPPSNS input current		20		μA

### Electrical Characteristics (continued)

T<sub>J</sub> = -40°C to 125°C, V<sub>PVIN</sub> = 12V, V<sub>PVIN\_VPP</sub> = 5V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
I <sub>VPPDIS</sub>	VPP discharge current	V <sub>SLP_S4</sub> = V <sub>VTT_CNTL</sub> = 0 V, V <sub>VPPSNS</sub> = 0.5 V		12	mA		
t <sub>VPPSS</sub>	VPP soft-start time		1.0	2	ms		
R <sub>DSONH</sub>	High-side switch resistance	T <sub>J</sub> = 25°C, V <sub>PVIN_VPP</sub> = 5V, V <sub>VCC_5V</sub> = 5V		150	mΩ		
R <sub>DSONL</sub>	Low-side switch resistance	T <sub>J</sub> = 25°C, V <sub>PVIN_VPP</sub> = 5V, V <sub>VCC_5V</sub> = 5V		120	mΩ		
I <sub>VPOCL</sub>	Low-side valley current limited	V <sub>OUT</sub> = 2.5 V, L = 4.7 μH		1.05	A		
f <sub>sw</sub>	VPP switching frequency		580		kHz		
t <sub>OFF(MIN)</sub>	Minimum off time		195		ns		
t <sub>OOA</sub>	OOA mode operation period	V <sub>VPPSNS</sub> = 2.5 V		31	μs		
<b>OVP AND UVP (VDDQ, VPP)</b>							
V <sub>OVP</sub>	OVP threshold voltage	OVP detect voltage		120	125	130	%
V <sub>UVP1</sub>	UVP threshold voltage	UVP detect voltage		55	60	65	%
t <sub>OVPDLY</sub>	OVP delay		20				μs
t <sub>UVPDLY</sub>	UVP delay		250				μs
<b>VTTREF OUTPUT</b>							
V <sub>VTTREF</sub>	Output voltage			1/2* V <sub>VDDQSNS</sub>			V
V <sub>VTTREF</sub>	Output voltage tolerance to VDDQ	T <sub>J</sub> = 25°C,  I <sub>VTTREF</sub>   ≤ 100 μA, V <sub>VDDQSNS</sub> = 1.2 V		49.2		50.8	%
		T <sub>J</sub> = 25°C,  I <sub>VTTREF</sub>   ≤ 10mA, V <sub>VDDQSNS</sub> = 1.2 V		49		51	
I <sub>VTTREFOCLSRC</sub>	Source current limit	V <sub>VDDQSNS</sub> = 1.2 V, V <sub>VTTREF</sub> = 0 V		10	18		mA
I <sub>VTTREFOCLSnk</sub>	Sink current limit	V <sub>VDDQSNS</sub> = 1.2 V, V <sub>VTTREF</sub> = 1.2 V		10	18		mA
I <sub>VTTREFDIS</sub>	VTTREF discharge current	T <sub>J</sub> = 25°C, V <sub>SLP_S4</sub> = V <sub>VTT_CNTL</sub> = 0 V, V <sub>VTTREF</sub> = 0.5 V		0.8	1.3		mA
<b>VTT OUTPUT</b>							
V <sub>VTT</sub>	Output voltage			V <sub>VTTREF</sub>			V
V <sub>VTTTOL</sub>	Output voltage tolerance	I <sub>VTT</sub>   ≤ 10 mA, V <sub>VDDQSNS</sub> = 1.2 V, I <sub>VTTREF</sub> = 0 A		-20		20	mV
		T <sub>J</sub> = 25°C,  I <sub>VTT</sub>   ≤ 1A, V <sub>VDDQSNS</sub> = 1.2 V, I <sub>VTTREF</sub> = 0 A		-30		30	
I <sub>VTTOCLSRC</sub>	Source current limit	V <sub>VDDQSNS</sub> = 1.2 V, V <sub>VTT</sub> = V <sub>VTTSNS</sub> = 0.5 V, I <sub>VTTREF</sub> = 0 A		1	1.7		A
I <sub>VTTOCLSnk</sub>	Sink current limit	V <sub>VDDQSNS</sub> = 1.2 V, V <sub>VTT</sub> = V <sub>VTTSNS</sub> = 0.7 V, I <sub>VTTREF</sub> = 0 A		1	1.7		A
I <sub>VTTLK</sub>	Leakage current	T <sub>J</sub> = 25°C, V <sub>SLP_S4</sub> = 5 V, V <sub>VTT_CNTL</sub> = 5 V, V <sub>VTT</sub> = V <sub>VTTREF</sub>				5	μA
I <sub>VTTSNSBIAS</sub>	VTTSNS input bias current	V <sub>SLP_S4</sub> = 5 V, V <sub>VTT_CNTL</sub> = 5 V, V <sub>VTT</sub> = V <sub>VTTREF</sub>		-0.5	0	0.5	
I <sub>VTTSNSLK</sub>	VTTSNS leakage current	V <sub>SLP_S4</sub> = 5 V, V <sub>VTT_CNTL</sub> = 0 V, V <sub>VTT</sub> = V <sub>VTTREF</sub>		-1	0	1	
I <sub>VTTDLY</sub>	VTT output delay relative to VTT_CNTL					35	us
I <sub>VTTDIS</sub>	VTT discharge current	T <sub>J</sub> = 25°C, V <sub>SLP_S4</sub> = V <sub>VTT_CNTL</sub> = 0 V, V <sub>VDDQSNS</sub> = 1.2 V, V <sub>VTT</sub> = 0.5V, I <sub>VTTREF</sub> = 0 A			5.7		mA
<b>SLP_S4, VTT_CNTL LOGIC THRESHOLD</b>							
V <sub>IH</sub>	SLP_S4/VTT_CNTL high-level voltage		1.6				V

**Electrical Characteristics (continued)**
 $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{PVIN} = 12\text{V}$ ,  $V_{PVIN\_VPP} = 5\text{V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL}$	SLP_S4/VTT_CNTL low-level voltage				0.5	V
$R_{TOGND}$	SLP_S4/VTT_CNTL resistance to GND			500		$k\Omega$
<b>THERMAL PROTECTION</b>						
$T_{OTP}$	OTP trip threshold			150		$^{\circ}\text{C}$
$T_{OTPHSY}$	OTP hysteresis			20		$^{\circ}\text{C}$

## 6.6 Typical Characteristics

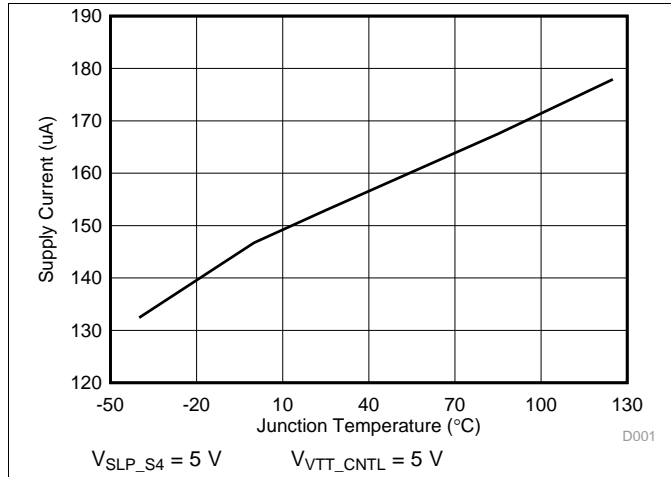


图 1. VCC\_5V Supply Current vs Junction Temperature

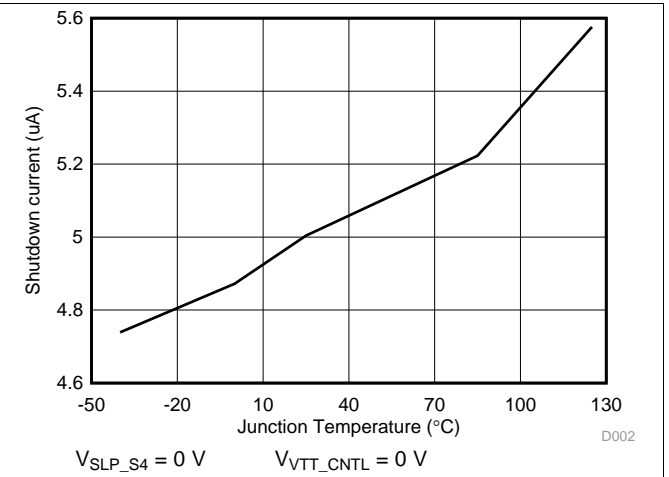


图 2. VCC\_5V Shutdown Current vs Temperature

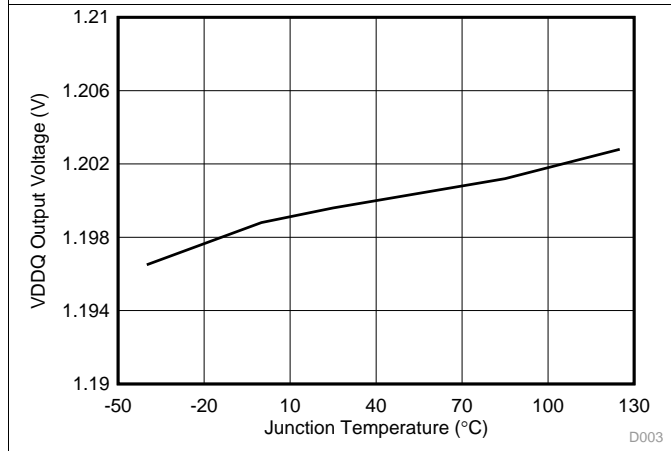


图 3. VDDQ Output Voltage vs Junction Temperature

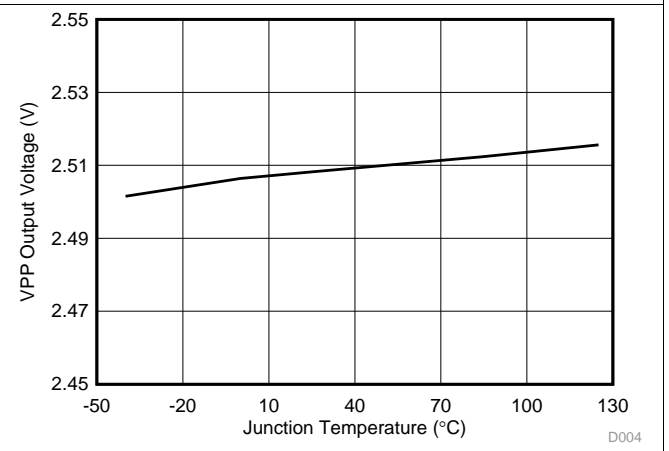


图 4. VPP Output Voltage vs Junction Temperature

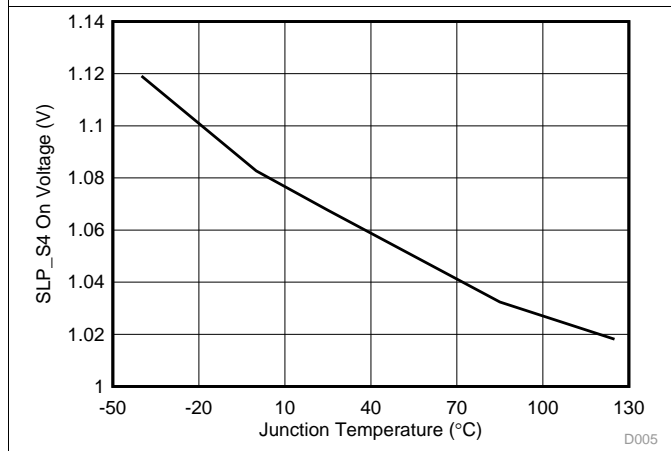


图 5. Enable On Voltage (SLP\_S4) vs Junction Temperature

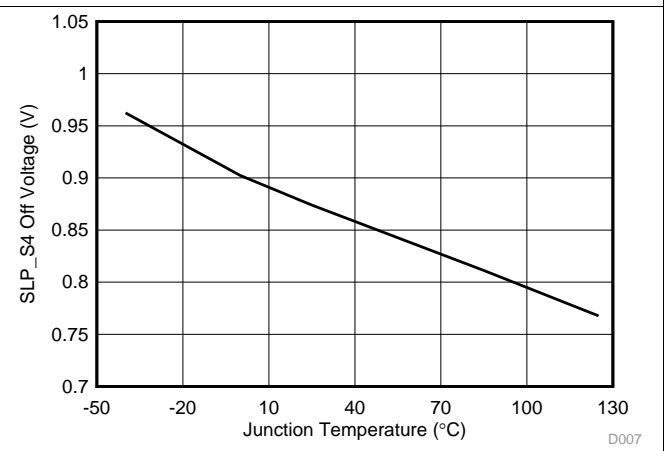
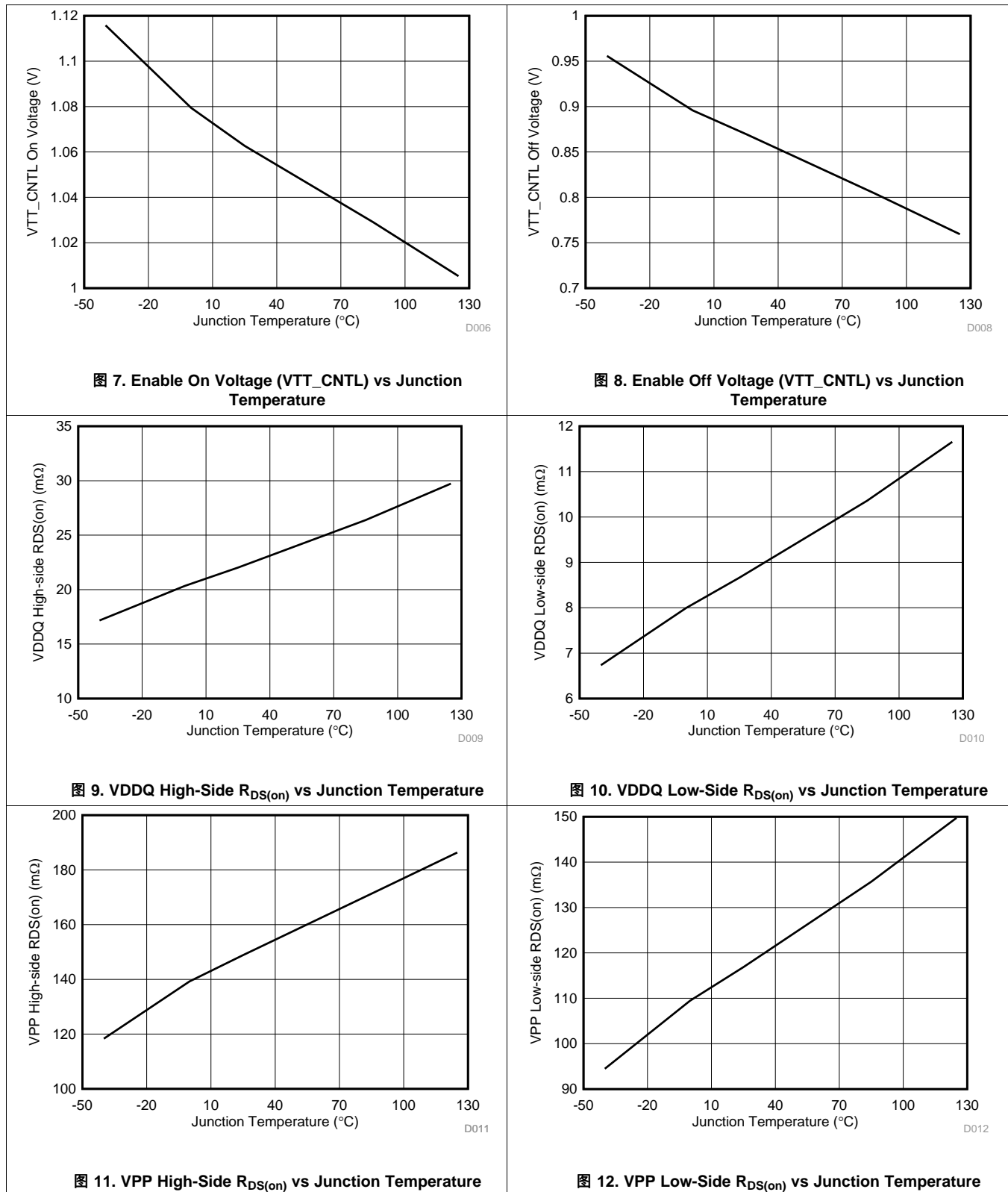


图 6. Enable Off Voltage (SLP\_S4) vs Junction Temperature



Typical Characteristics (接下页)



Typical Characteristics (接下页)

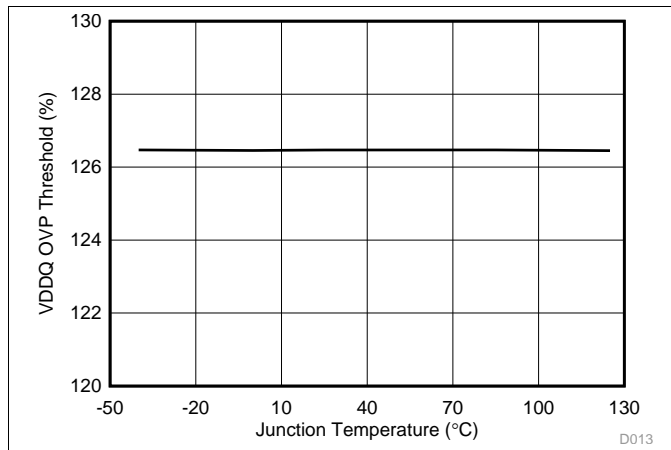


图 13. VDDQ OVP Threshold vs Junction Temperature

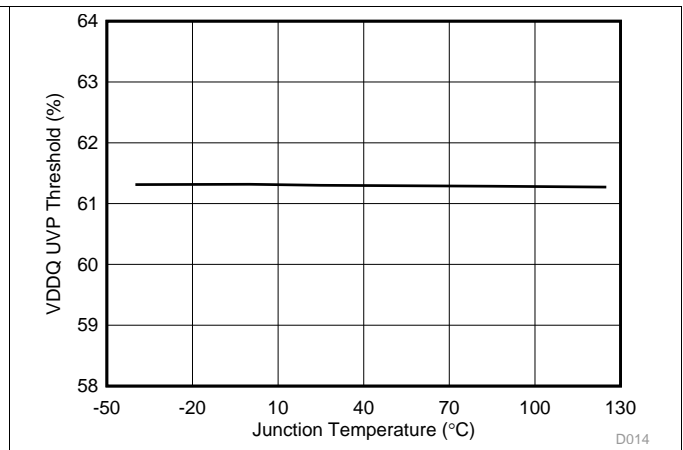


图 14. VDDQ UVP Threshold vs Junction Temperature

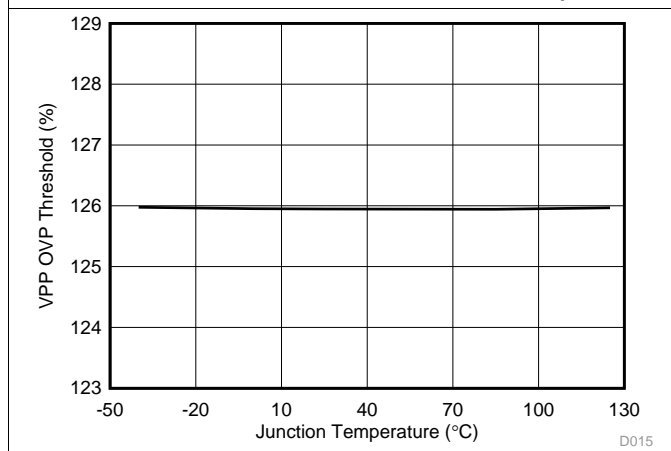


图 15. VPP OVP Threshold vs Junction Temperature

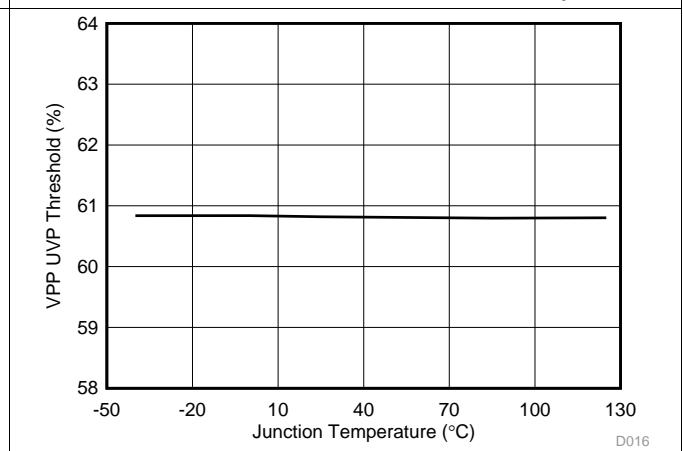


图 16. VPP UVP Threshold vs Junction Temperature

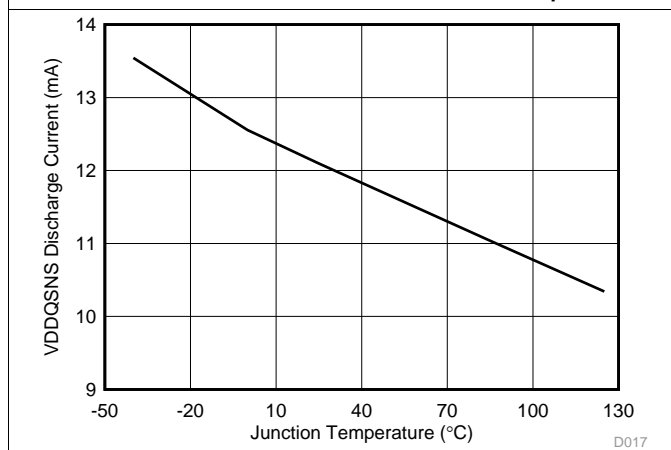


图 17. VDDQSNS Discharge Current vs Junction Temperature

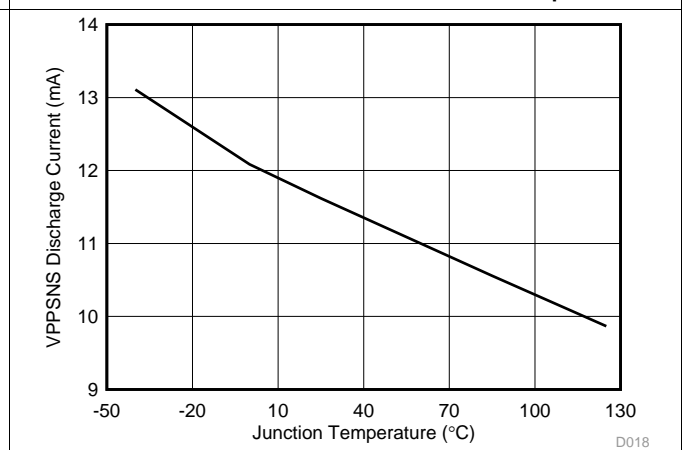
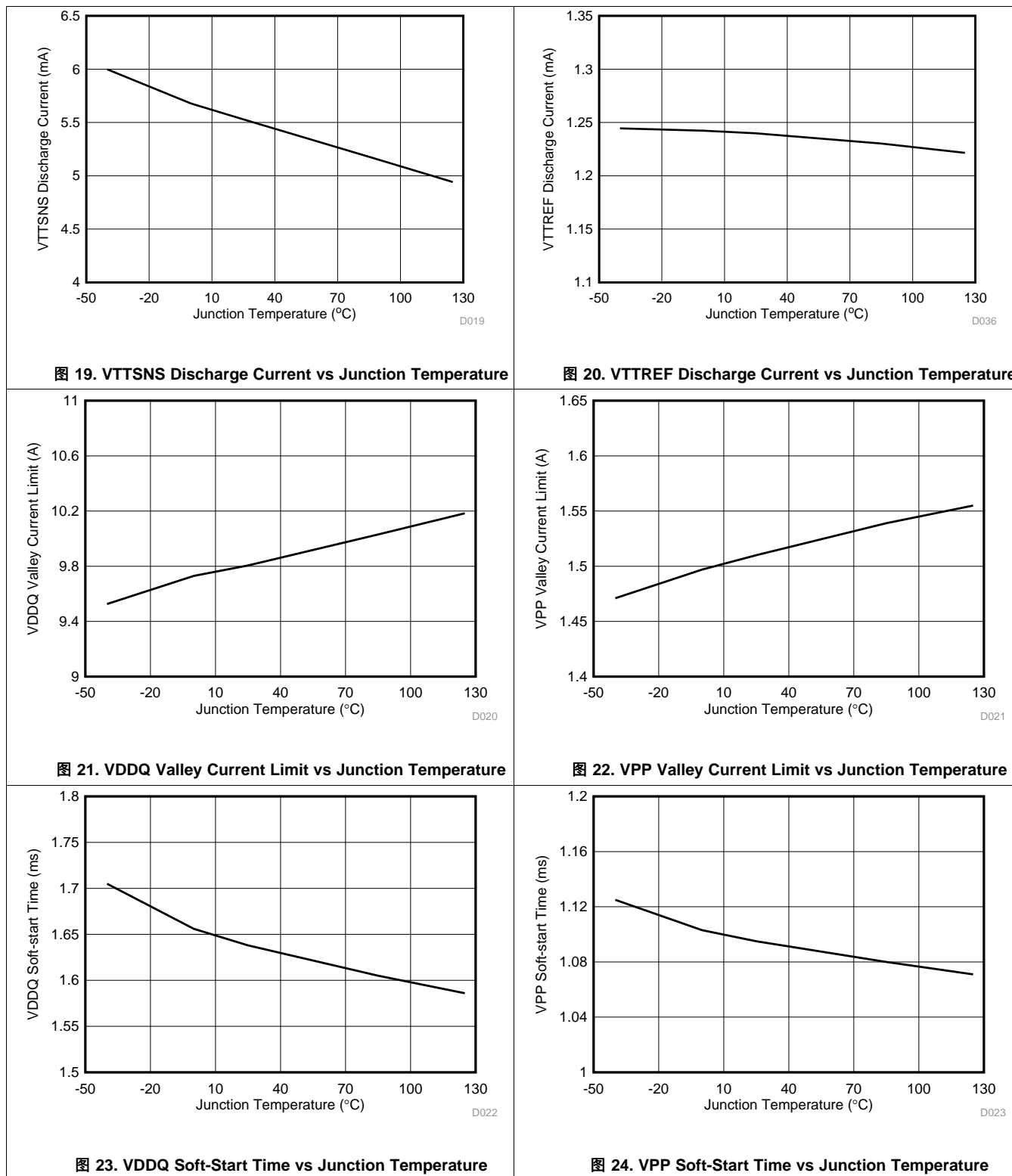


图 18. VPPSNS Discharge Current vs Junction Temperature

Typical Characteristics (接下页)



Typical Characteristics (接下页)

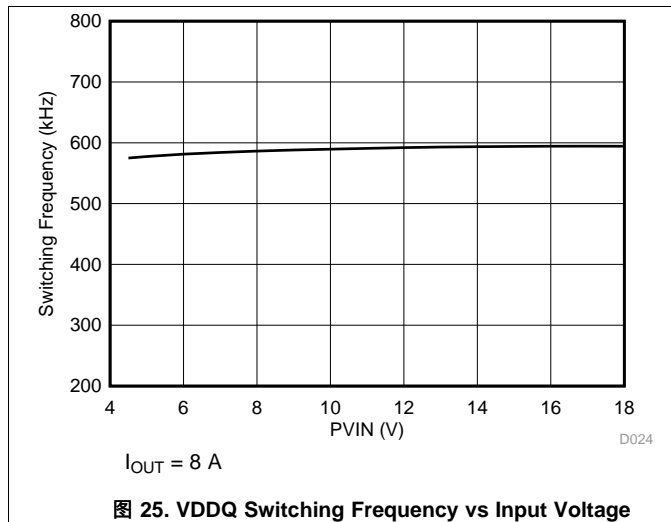


图 25. VDDQ Switching Frequency vs Input Voltage

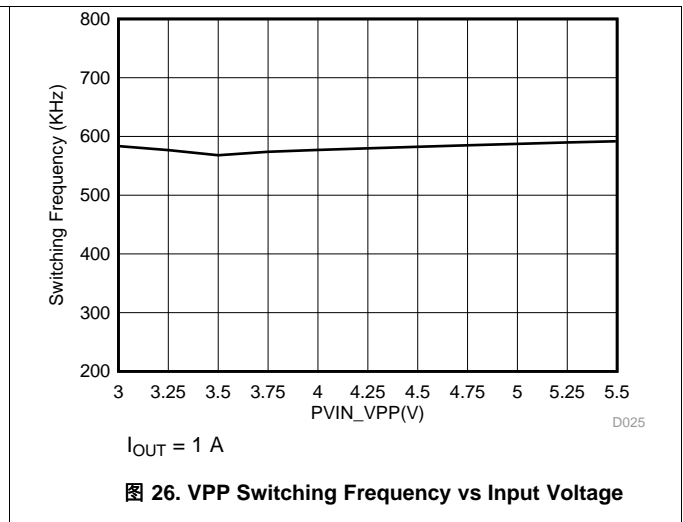


图 26. VPP Switching Frequency vs Input Voltage

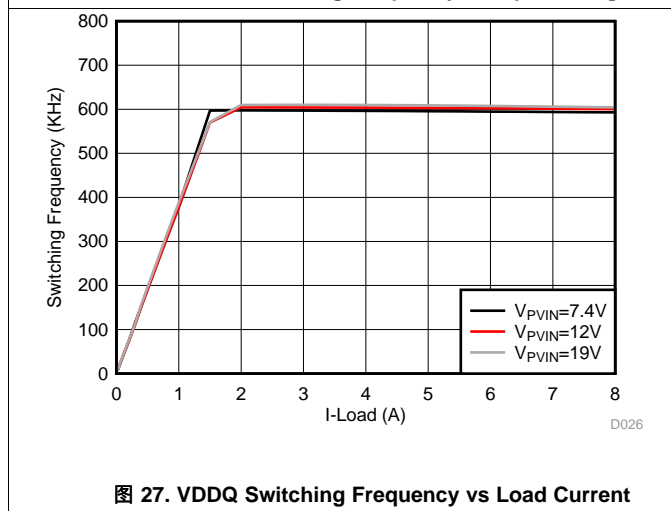


图 27. VDDQ Switching Frequency vs Load Current

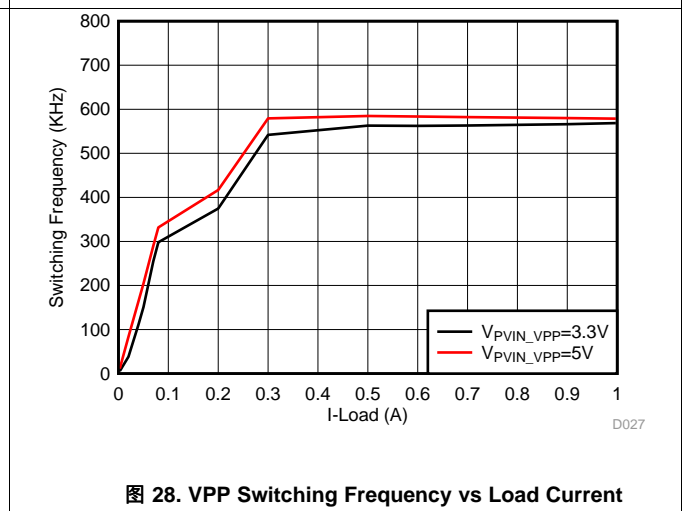


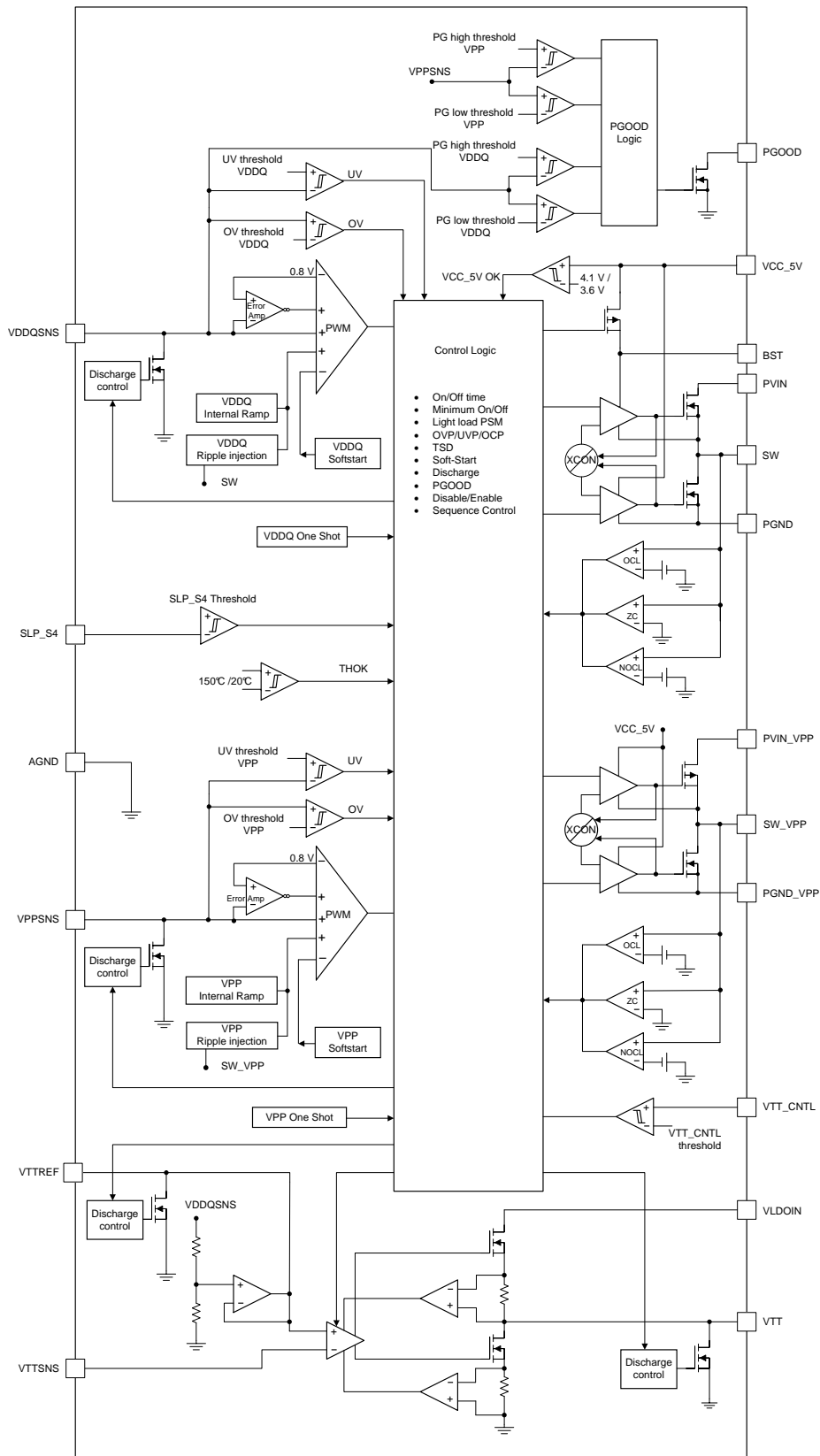
图 28. VPP Switching Frequency vs Load Current

## 7 Detailed Description

### 7.1 Overview

The TPS65295 integrates two synchronous step-down buck converters and two LDOs to support complete DDR4 power solution. The VDDQ buck converter has the fixed 1.2-V output and supports continuous 8-A output current, and it can operate from 4.5-V to 18-V PVIN input voltage. The VPP buck converter has the fixed 2.5-V output and supports continuous 1-A output current, and can operate from 3-V to 5.5-V PVIN\_VPP input voltage. The VTTREF LDO tracks the  $\frac{1}{2}$  VDDQ output and has about 10-mA both sink and source current capability. The VTT LDO tracks the VTTREF output and has continuous 1-A both sink and source current capability.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 PWM Operation and D-CAP3™ Control

The main control loop of the two bucks is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3™ mode control. The DCAP3™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS65295 also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the converter input voltage,  $V_{IN}$ , and is inversely proportional to the output voltage,  $V_O$ , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage for emulating the output ripple, this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3™ control topology.

Both VDDQ buck and VPP buck include an error amplifier that makes the output voltage very accurate. For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS65295 is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in [公式 1](#).

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the internal output set-point resistor divider network and the internal gain of the TPS65295. The low-frequency L-C double pole has a 180 degree in phase. At the output filter frequency, the gain rolls off at a  $-40$  dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from  $-40$  dB to  $-20$  dB per decade and increases the phase to 90 degree one decade above the zero frequency. The internal ripple injection high-frequency zero is related to the switching frequency. The inductor and capacitor selected for the output filter must be such that the double pole is placed close enough to the high-frequency zero, so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-fifth of the switching frequency ( $F_{SW}$ ).

### 7.3.2 Advanced Eco-mode™ Control

The VDDQ buck and VPP buck are designed with advanced Eco-mode™ control schemes to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode, so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The light load current where the transition to Eco-mode™ operation happens ( $I_{OUT(LL)}$ ) can be calculated from [公式 2](#).

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance ( $L_{OUT}$ ) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the  $I_{OUT(max)}$  (peak current in the application). It is also important to size the inductor properly so that the valley current does not hit the negative low-side current limit.

## Feature Description (接下页)

### 7.3.3 Soft Start and Prebiased Soft Start

The VDDQ buck has an internal 1.6-ms soft start and VPP buck has an internal 1-ms soft start. Provide the voltage supply to PVIN, PVIN\_VPP and VCC\_5V before asserting SLP\_S4 to be high, when the SLP\_S4 pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is prebiased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage. This scheme ensures that the converters ramp up smoothly into regulation point.

### 7.3.4 Power Good

The Power Good (PGOOD) pin is an open-drain output. Once the VDDQSNS and VPPSNS pins voltage are between 90% and 110% of the target output voltage, the PGOOD is deasserted and floats after a 1-ms de-glitch time. A pullup resistor of 100 k $\Omega$  is recommended to pull the voltage up to VCC\_5V. The PGOOD pin is pulled low when:

- the VDDQSNS pin voltage or VPPSNS pin voltage is lower than 85% or greater than 115% of the target output voltage
- in an OVP, UVP, or thermal shutdown event
- during the soft-start period.

### 7.3.5 Overcurrent Protection and Undervoltage Protection

Both VDDQ and VPP bucks have the overcurrent protection and undervoltage protection, and the implementation is same. The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by  $V_{in}$ ,  $V_{out}$ , the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current  $I_{OUT}$ . If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. When the load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it, the output will be discharged and latched after a wait time of 256  $\mu$ s. When the overcurrent condition is removed, the output voltage is latched till the SLP\_S4 is toggled or repower the VCC\_5V power input.

### 7.3.6 Overvoltage Protection

Both VDDQ and VPP bucks have the overvoltage protection feature and have the same implementation. When the output voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high, and then the output will be discharged and latched after a wait time of 20  $\mu$ s. When the over current condition is removed, the output voltage is latched till the SLP\_S4 is toggled or repower the VCC\_5V power input.

### 7.3.7 UVLO Protection

Undervoltage Lockout protection (UVLO) monitors the VCC\_5V power input. When the voltage is lower than UVLO threshold voltage, the device is shut off and outputs are discharged. This is a non-latch protection.

### 7.3.8 Output Voltage Discharge

The VPP buck, VDDQ buck, VTT LDO, and VTTREF LDO block all have the discharge function by using internal MOSFETs, which are connected to the corresponding output terminals VPPSNS, VDDQSNS, VTT, and VTTREF. The discharge is slow due to the lower current capability of these MOSFETs.



## Feature Description (接下页)

### 7.3.9 Thermal Shutdown

The TPS65295 monitors the internal die temperature. If the temperature exceeds the threshold value (typically 150°C), the device is shut off and the output will be discharged. This is a non-latch protection. The device restarts switching when the temperature goes below the thermal shutdown recover threshold.

## 7.4 Device Functional Modes

### 7.4.1 Light Load Operation for VDDQ Buck and VPP Buck

When the load is light on the VDDQ or VPP output, the buck enters pulse skip mode after the inductor current crosses zero. This is the Eco-mode™ which improves the efficiency at light load with a lower switching frequency. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VDDQSNS or VPPSNS voltage falls below the Eco-mode™ threshold voltage. As the output current decreases, the period time between switching pulses increases.

### 7.4.2 Output State Control

The TPS65295 has two enable input pins, SLP\_S4 and VTT\_CNTL, to provide simple control scheme of output state. All of VPP, VDDQ, VTTREF and VTT are turned on at S0 state (SLP\_S4=VTT\_CNTL=high). In S3 state (VTT\_CNTL=low, SLP\_S4=high), VPP, VDDQ, and VTTREF voltages are kept on while VTT is turned off and left at high impedance state (high-Z). The VTT output floats and does not sink or source current in this state. In S4/S5 states (SLP\_S4=VTT\_CNTL =low), all of the three outputs are turned off and discharged to GND. Each state code represents as follow: S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF (see 表 1).

表 1. VTT\_CNTL and SLP\_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

### 7.4.3 Output Sequence Control

There are specific sequencing requirements for the DDR4 VDDQ and VPP rails. The TPS65295 follows the DDR4 power rail sequence requirements as shown in 图 29 and 图 30. VPP is greater than VDDQ at all times during ramp up, operating, and ramp down. The VTT output ramp and stable within 35 μs after VTT\_CNTL asserted.

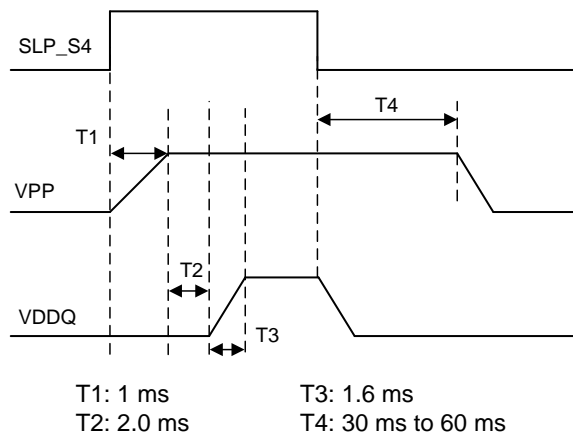


图 29. Power Sequence, VPP and VDDQ vs SLP\_S4

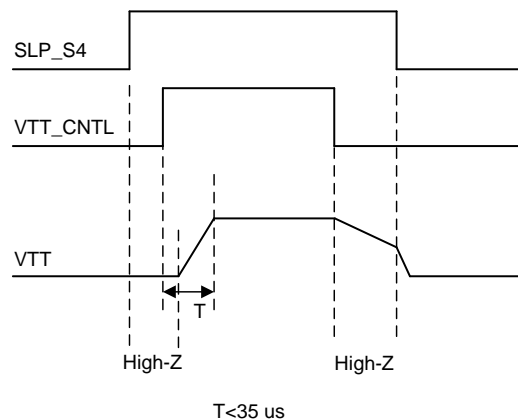


图 30. Power Sequence, VTT vs VTT\_CNTL

## 8 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The schematic of 图 31 shows a typical application for TPS65295. For VDDQ buck, the PVIN supports 4.5-V to 18-V input range with 1.2-V VDDQ output, the continuous current capability is 8 A. Usually the PVIN\_VPP and VCC\_5V can share one 5-V power input and supports 2.5-V VPP output with 1-A continuous current capability, of course the PVIN\_VPP can be lowered down to a 3.3-V power supply. The VLDOIN power input usually is connected to VDDQ output, while also it can be connected to external 1.2-V power supply input. The VTTREF output voltage will follow the 1/2 VDDQSNS voltage, and VTT output voltage will follow the VTTREF output voltage, this is required by DDR4 power supply standard.

### 8.2 Typical Application

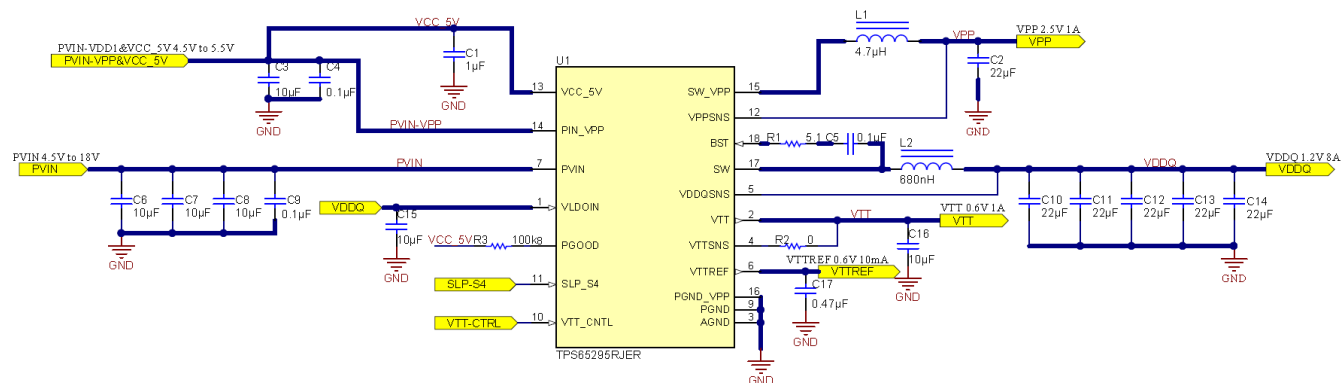


图 31. Application Schematic

#### 8.2.1 Design Requirements

表 2 lists the design parameters for this example.

表 2. Design Parameters

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>VDDQ OUTPUT</b>					
V <sub>OUT</sub>	Output voltage		1.2		V
I <sub>OUT</sub>	Output current		8		A
ΔV <sub>OUT</sub>	Transient response		±60		mV
V <sub>IN</sub>	Input voltage	4.5	12	18	V
V <sub>OUT(ripple)</sub>	Output voltage ripple		40		mV <sub>(P-P)</sub>
F <sub>SW</sub>	Switching frequency		600		kHz
<b>VPP OUTPUT</b>					
V <sub>OUT</sub>	Output voltage		2.5		V
I <sub>OUT</sub>	Output current		1		A
ΔV <sub>OUT</sub>	Transient response		±125		mV
V <sub>IN</sub>	Input voltage	3	5	5.5	V

**Typical Application (接下页)**
**表 2. Design Parameters (接下页)**

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT(ripple)}$	Output voltage ripple			40		mV <sub>(P-P)</sub>
$F_{SW}$	Switching frequency			580		kHz
<b>OTHERS</b>						
$V_{VCC\_5V}$	Start VCC_5V input voltage	VCC_5V Input voltage rising		Internal UVLO		V
	Stop VCC_5V input voltage	VCC_5V Input voltage falling		Internal UVLO		V
	Light load operating mode			ECO		
$T_A$	Ambient temperature			25		°C

**8.2.2 Detailed Design Procedure**
**8.2.2.1 External Component Selection**
**8.2.2.1.1 Inductor Selection**

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See 表 3 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using 公式 3 and 公式 4. It is important that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{\left( I_{OUT}^2 + \frac{1}{12} \times \left( \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_{OUT} \times F_{SW}} \right)^2 \right)} \quad (3)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (4)$$

During transient and short-circuit conditions, the inductor current can increase up to the current limit of the device so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

**8.2.2.1.2 Output Capacitor Selection**

After selecting the inductor the output capacitor needs to be optimized. In DCAP3, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in 表 3.

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than  $V_{OUT(ripple)}/I_{OUT(ripple)}$ .

**表 3. Recommended Component Values**

$V_{OUT}$ (V)	$F_{SW}$ (kHz)	$L_{OUT}$ (μH)	$C_{OUT(min)}$ (μF)	$C_{OUT(max)}$ (μF)
1.2	600	0.68	88	132
	600	0.56	88	132
	600	0.47	88	132
2.5	580	6.8	20	66
	580	4.7	20	66
	580	3.3	20	66

For VTT output, high quality X5R or X7R 10-μF capacitor is recommended and a 0.47 μF is recommended for VTTREF output.

### 8.2.2.1.3 Input Capacitor Selection

The TPS65295 requires input decoupling capacitors on both power supply input PVIN and PVIN\_VPP, and the bulk capacitors are needed depending on the application. The minimum input capacitance required is given in 公式 5.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \tag{5}$$

TI recommends using a high-quality X5R or X7R input decoupling capacitors of 30 μF on the VDDQ buck input voltage pin PVIN, and 10 μF on the VPP buck input voltage pin PVIN\_VPP. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by 公式 6:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \tag{6}$$

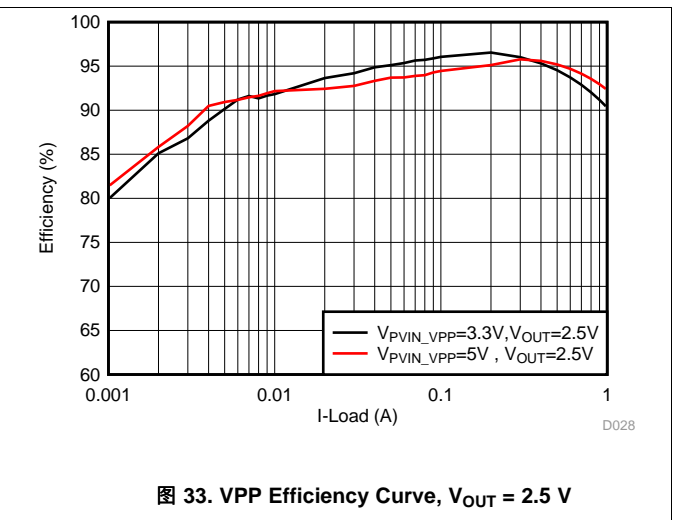
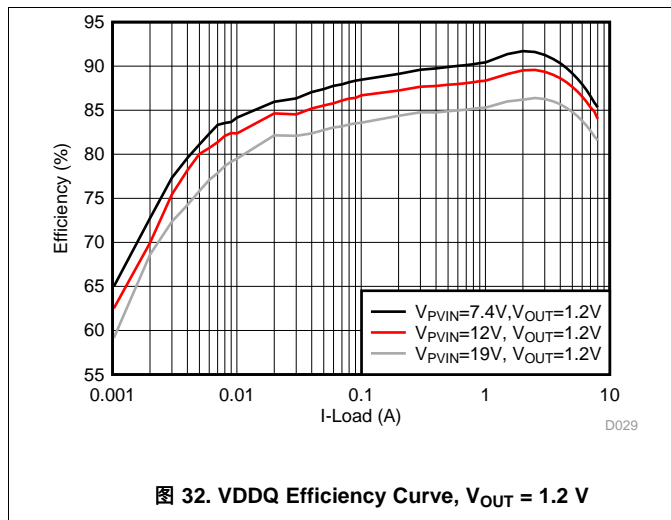
An additional 0.1-μF capacitor from PVIN to ground and from PVIN\_VPP to ground is optional to provide additional high frequency filtering. One ceramic capacitor of 10 μF is recommended for the decoupling capacitor on VLDOIN pin for providing stable power on VTT LDO block. A 1-μF ceramic capacitor is needed for the decoupling capacitor on VCC\_5V input.

### 8.2.2.1.4 Bootstrap Capacitor and Resistor Selection

A 0.1-μF ceramic capacitor serialized with a 5.1-Ω resistor is recommended between the BST and SW pin for proper operation. TI recommends using a ceramic capacitor.

## 8.2.3 Application Curves

图 32 through 图 60 apply to the circuit of 图 31.  $V_{IN} = 12\text{ V}$ .  $T_A = 25^\circ\text{C}$  unless otherwise specified.



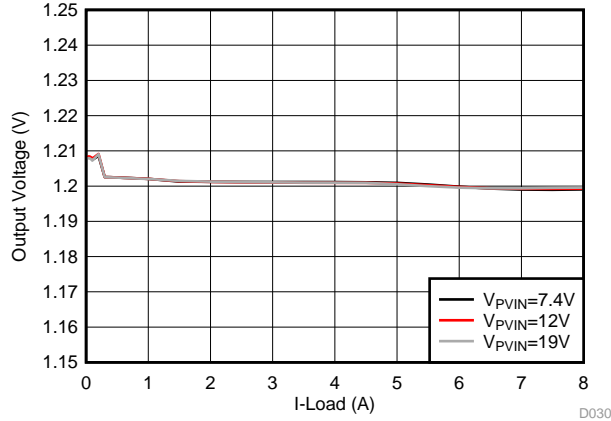


图 34. VDDQ Load Regulation,  $V_{OUT} = 1.2\text{ V}$

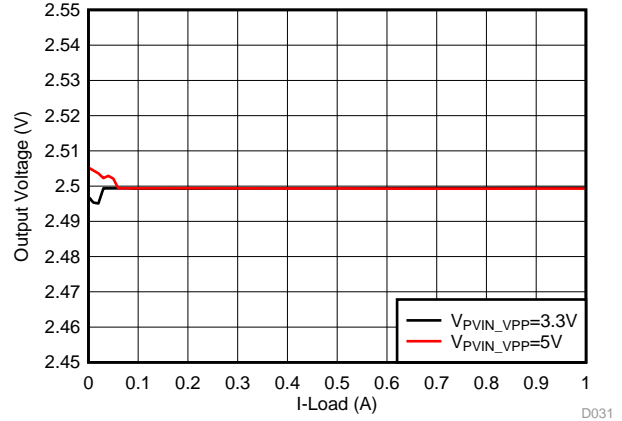


图 35. VPP Load Regulation,  $V_{OUT} = 2.5\text{ V}$

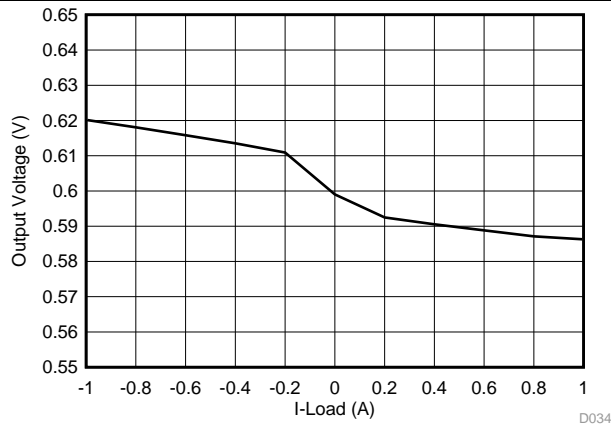


图 36. VTT Load Regulation,  $V_{OUT} = 0.6\text{ V}$

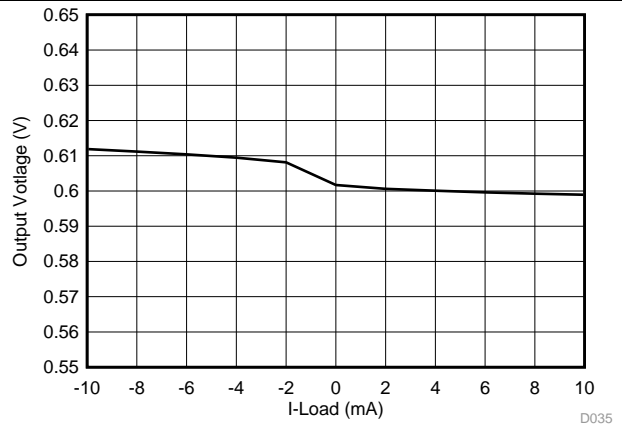


图 37. VTTREF Load Regulation,  $V_{OUT} = 0.6\text{ V}$

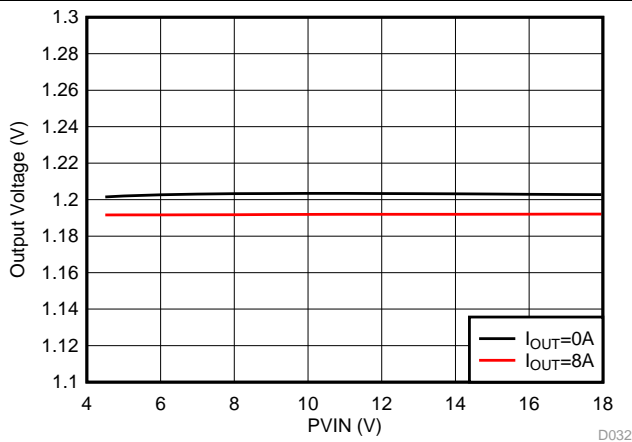


图 38. VDDQ Line Regulation,  $V_{OUT} = 1.2\text{ V}$

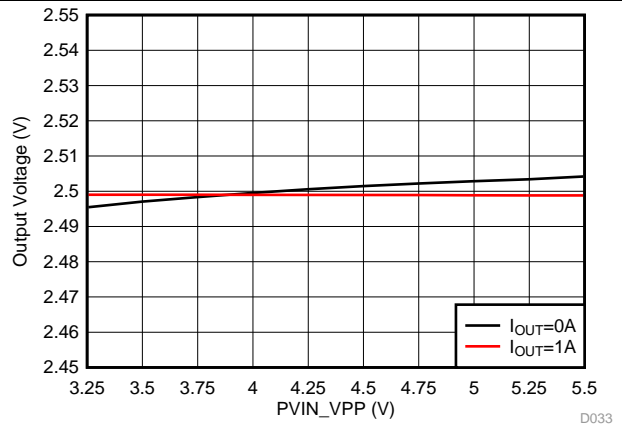


图 39. VPP Line Regulation,  $V_{OUT} = 2.5\text{ V}$

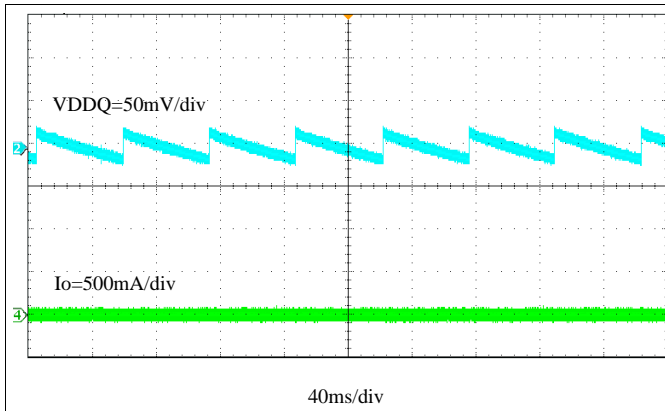


图 40. VDDQ Output Voltage Ripple,  $I_{OUT} = 0\text{ A}$

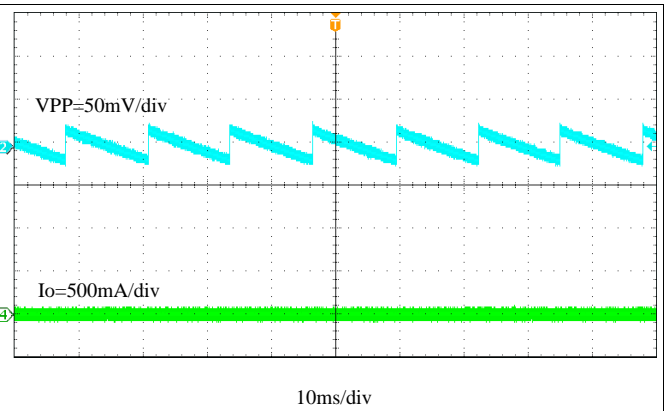


图 41. VPP Output Voltage Ripple,  $I_{OUT} = 0\text{ A}$

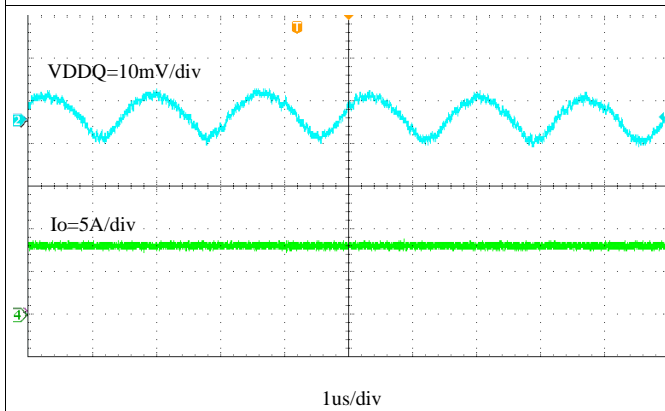


图 42. VDDQ Output Voltage Ripple,  $I_{OUT} = 8\text{ A}$

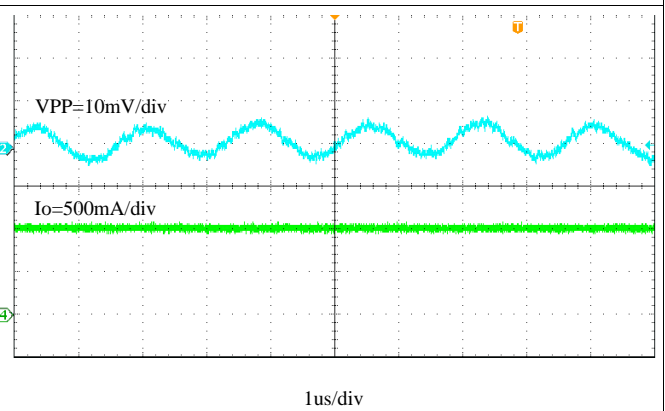


图 43. VPP Output Voltage Ripple,  $I_{OUT} = 1\text{ A}$

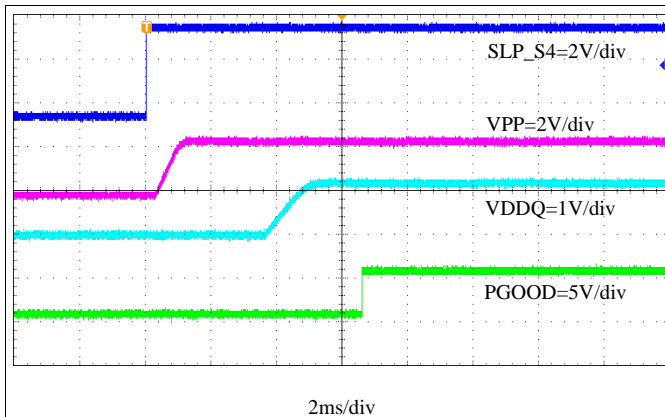


图 44. Start-Up Through SLP\_S4,  $I_{VPPOUT} = 0\text{ A}$ ,  $I_{VDDQOUT} = 0\text{ A}$

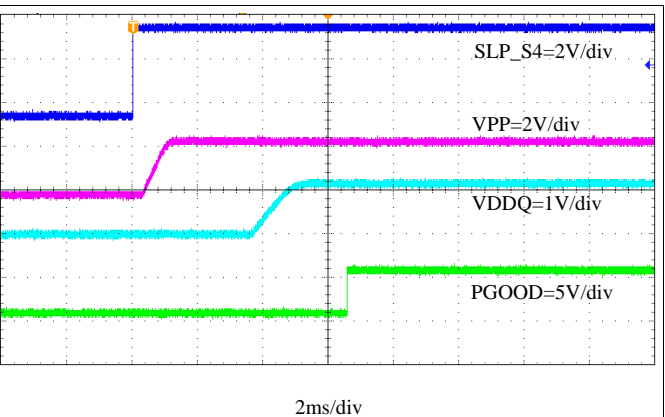
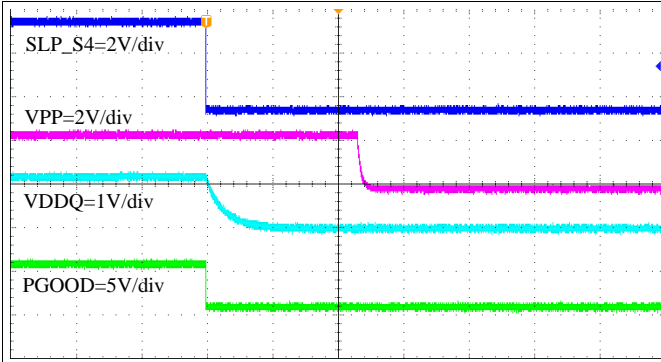
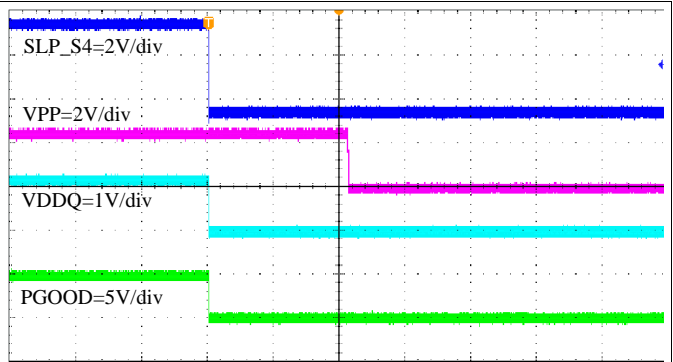


图 45. Start-Up Through SLP\_S4,  $I_{VPPOUT} = 1\text{ A}$ ,  $I_{VDDQOUT} = 8\text{ A}$



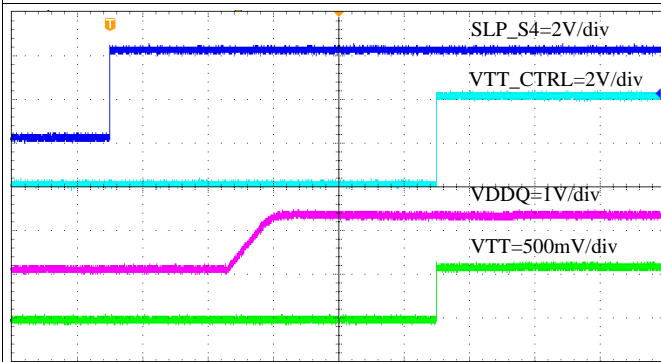
20ms/div

图 46. Shutdown Through SLP\_S4,  $I_{VPP\text{OUT}} = 0 \text{ A}$ ,  $I_{VDD\text{QOUT}} = 0 \text{ A}$



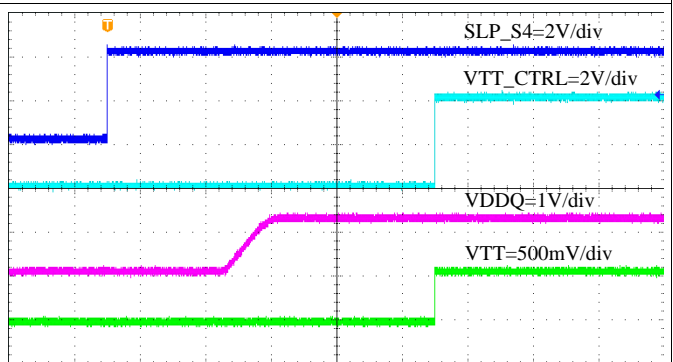
20ms/div

图 47. Shutdown Through SLP\_S4,  $I_{VPP\text{OUT}} = 1 \text{ A}$ ,  $I_{VDD\text{QOUT}} = 8 \text{ A}$



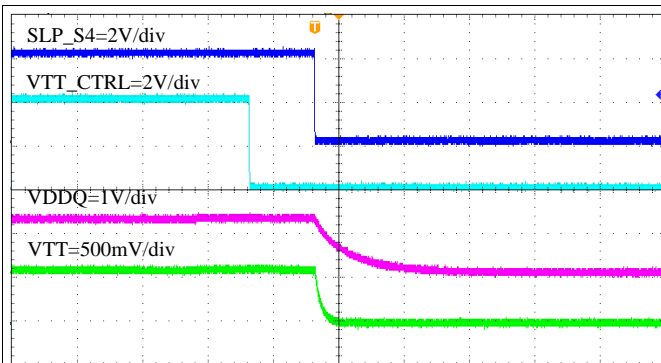
$I_{VDD\text{QOUT}} = 0 \text{ A}$       2ms/div  
 $I_{VTT} = 0 \text{ A}$        $I_{VTT\text{REF}} = 0 \text{ A}$

图 48. VTT Start-Up Through VTT\_CTRL



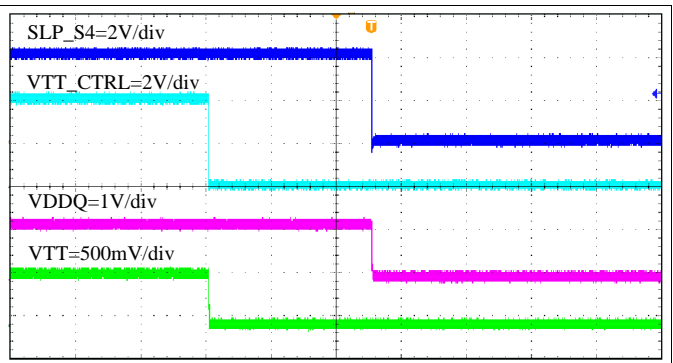
$I_{VDD\text{QOUT}} = 8 \text{ A}$       2ms/div  
 $I_{VTT} = 1 \text{ A}$        $I_{VTT\text{REF}} = 10 \text{ mA}$

图 49. VTT Start-Up Through VTT\_CTRL



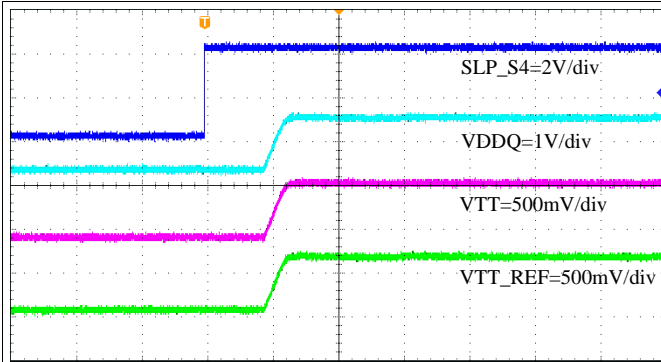
$I_{VDD\text{QOUT}} = 0 \text{ A}$       10ms/div  
 $I_{VTT} = 0 \text{ A}$        $I_{VTT\text{REF}} = 0 \text{ A}$

图 50. VTT Shutdown Through VTT\_CTRL



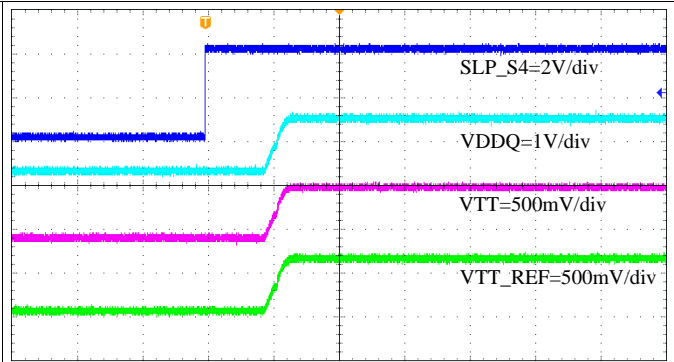
$I_{VDD\text{QOUT}} = 8 \text{ A}$       4ms/div  
 $I_{VTT} = 1 \text{ A}$        $I_{VTT\text{REF}} = 10 \text{ mA}$

图 51. VTT Shutdown Through VTT\_CTRL



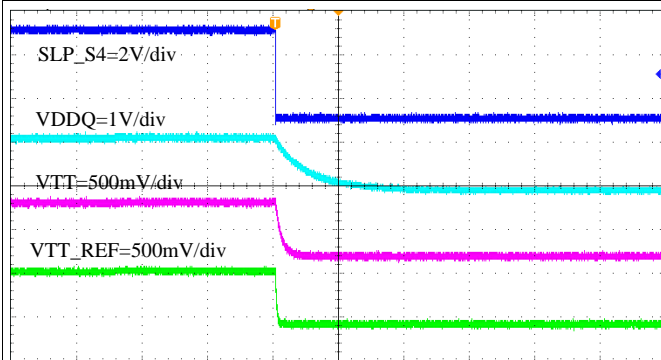
$I_{VDDQOUT} = 0\text{ A}$       4ms/div       $I_{VTT} = 0\text{ A}$        $I_{VTTREF} = 0\text{ A}$

图 52. VTT Start-Up Through SLP\_S4



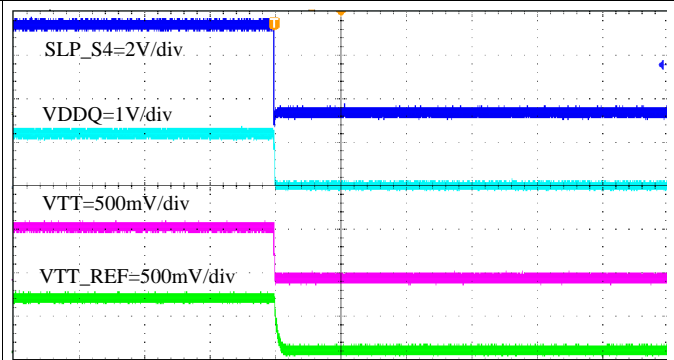
$I_{VDDQOUT} = 8\text{ A}$       4ms/div       $I_{VTT} = 1\text{ A}$        $I_{VTTREF} = 10\text{ mA}$

图 53. VTT Start-Up Through SLP\_S4



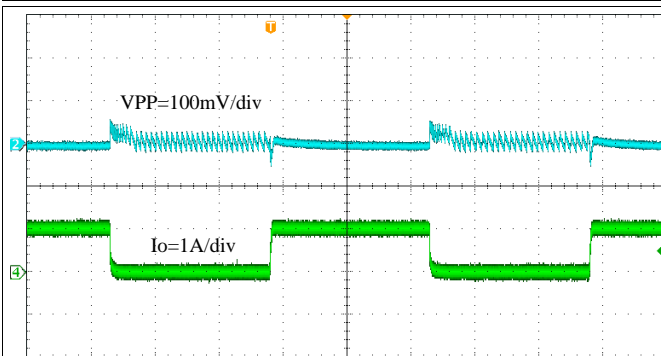
$I_{VDDQOUT} = 0\text{ A}$       10ms/div       $I_{VTT} = 0\text{ A}$        $I_{VTTREF} = 0\text{ A}$

图 54. VTT Shutdown Through SLP\_S4



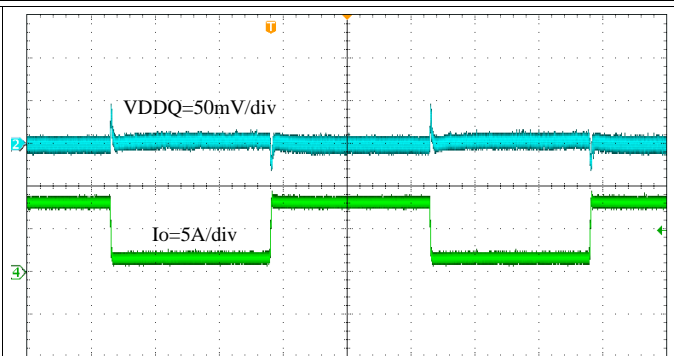
$I_{VDDQOUT} = 8\text{ A}$       4ms/div       $I_{VTT} = 1\text{ A}$        $I_{VTTREF} = 10\text{ mA}$

图 55. VTT Shutdown Through SLP\_S4



Slew Rate=2.5A/us      400us/div

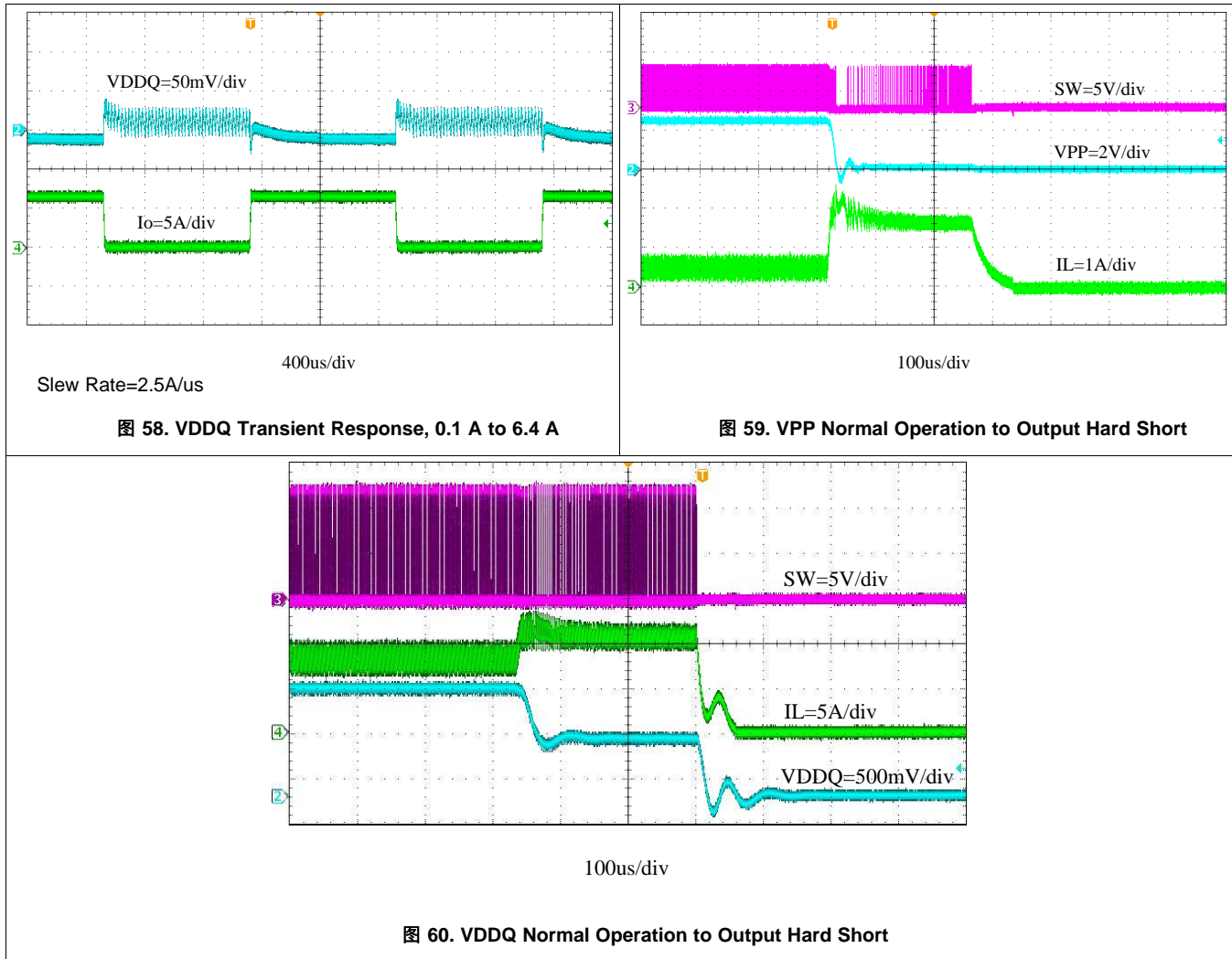
图 56. VPP Transient Response, 0 A to 1 A



Slew Rate=2.5A/us      400us/div

图 57. VDDQ Transient Response, 1.6 A to 8 A





## 9 Power Supply Recommendations

TPS65295 is designed for DDR4 complete power solution. PVIN is the power input for VDDQ buck, PVIN\_VPP is the power input for VPP buck, VLDOIN input is for VTT LDO power supply, VCC\_5V is power supply for internal control logic. Below lists the power on sequence scenarios.

- SLP\_S4 is high before PVIN or PVIN\_VPP has the power input, VCC\_5V power supply must be provided after or same time with PVIN or PVIN\_VPP, otherwise the output will be latched, this latch can be recovered by toggling the SLP\_S4 pin or re-power the VCC\_5V
- SLP\_S4 is low before PVIN and PVIN\_VPP has the power input, then there is no power supply input sequence requirement for VCC\_5V, PVIN and PVIN\_VPP.

## 10 Layout

### 10.1 Layout Guidelines

- Recommend a four-layer PCB for good thermal performance and with maximum ground plane. 3-inch x 3-inch, four-layer PCB with 2-oz. copper used as example.
- Place the decoupling capacitors right across PVIN, PVIN\_VPP, and VLDOIN as close as possible.
- Place output inductors and capacitors with IC at the same layer, SW routing should be as short as possible to minimize EMI, and should be a width plane to carry big current, enough vias should be added to the PGND connection of output capacitor and also as close to the output pin as possible. Reserve some space between VDDQ choke and VPP choke, just minimize radiation crosstalk.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane, >15 mil width trace is recommended to reduce line parasitic inductance.
- VPPSNS/VDDQSNS/VTTSNS could be 10 mil and must be routed away from the switching node, BST node or other high efficiency signal.
- PVIN and PVIN\_VPP trace must be wide to reduce the trace impedance and provide enough current capability.
- Output capacitors for VTT and VTTREF should be put as close as output pin.

### 10.2 Layout Example

图 61 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in 图 31.

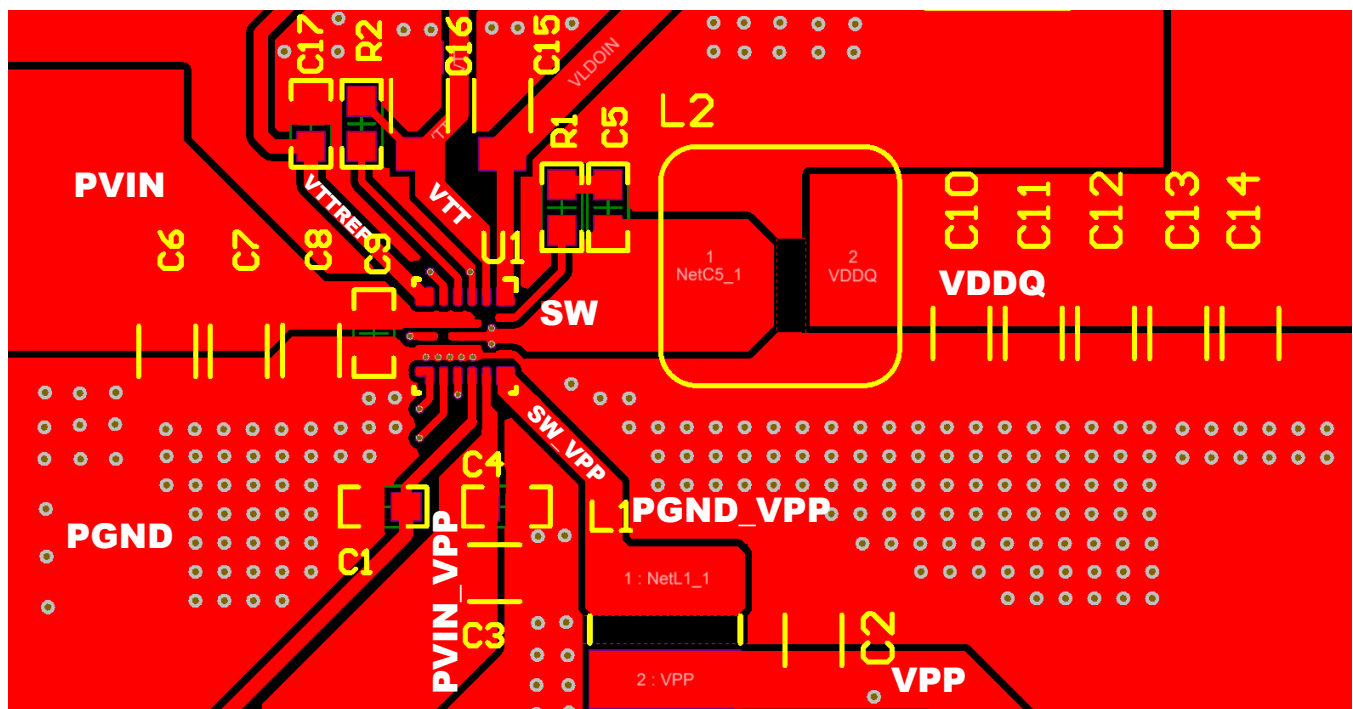


图 61. Top-Side Layout

## 11 器件和文档支持

### 11.1 器件支持

#### 11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

#### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的 *通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 商标

D-CAP3, Eco-mode, HotRod, DCAP3, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.6 术语表

**SLYZ022** — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

## 12.1 Package Option Addendum

### 12.1.1 Packaging Information

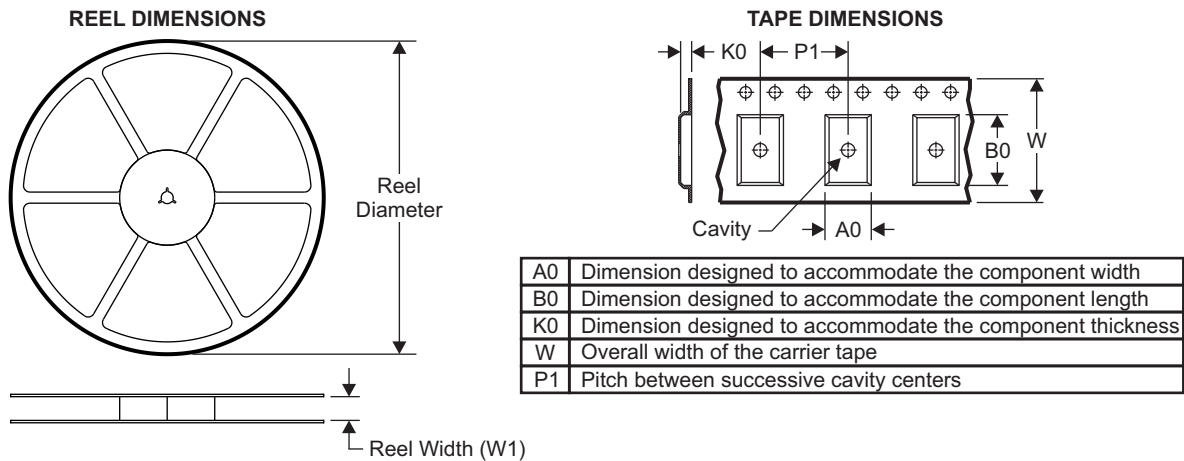
Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish <sup>(3)</sup>	MSL Peak Temp <sup>(4)</sup>	Op Temp (°C)	Device Marking <sup>(5)(6)</sup>
TPS65295RJER	PRE_PROD	VQFN-HR	RJE	18	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65295
TPS65295RJET	PRE_PROD	VQFN-HR	RJE	18	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65295

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

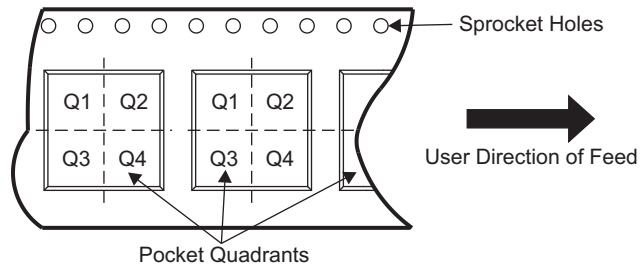
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

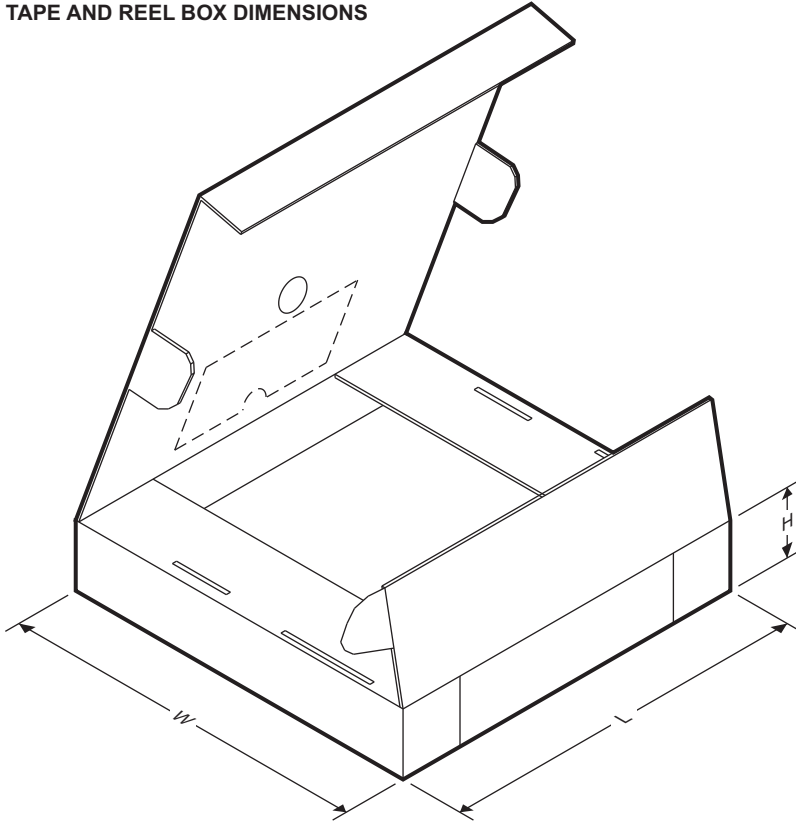
12.1.2 Tape and Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65295RJER	VQFN-HR	RJE	18	3000	330	12.4	3.3	3.3	1.1	8	12	Q2
TPS65295RJET	VQFN-HR	RJE	18	250	180	12.4	3.3	3.3	1.1	8	12	Q2

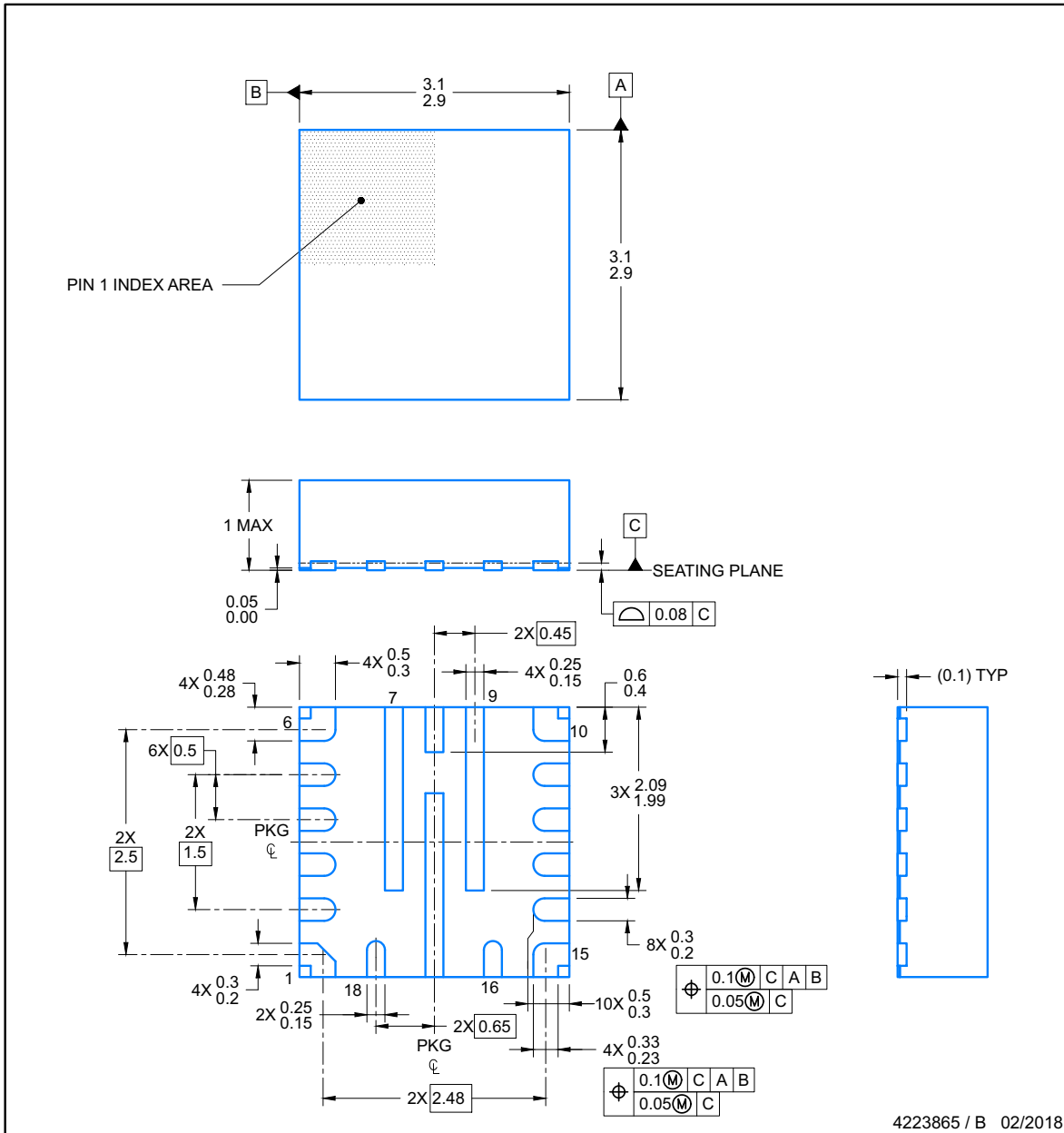
**TAPE AND REEL BOX DIMENSIONS**


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65295RJER	VQFN-HR	RJE	18	3000	367	367	35
TPS65295RJET	VQFN-HR	RJE	18	250	210	185	35

**PACKAGE OUTLINE**  
**VQFN-HR - 1 mm max height**

**RJE0018B**

PLASTIC QUAD FLATPACK- NO LEAD



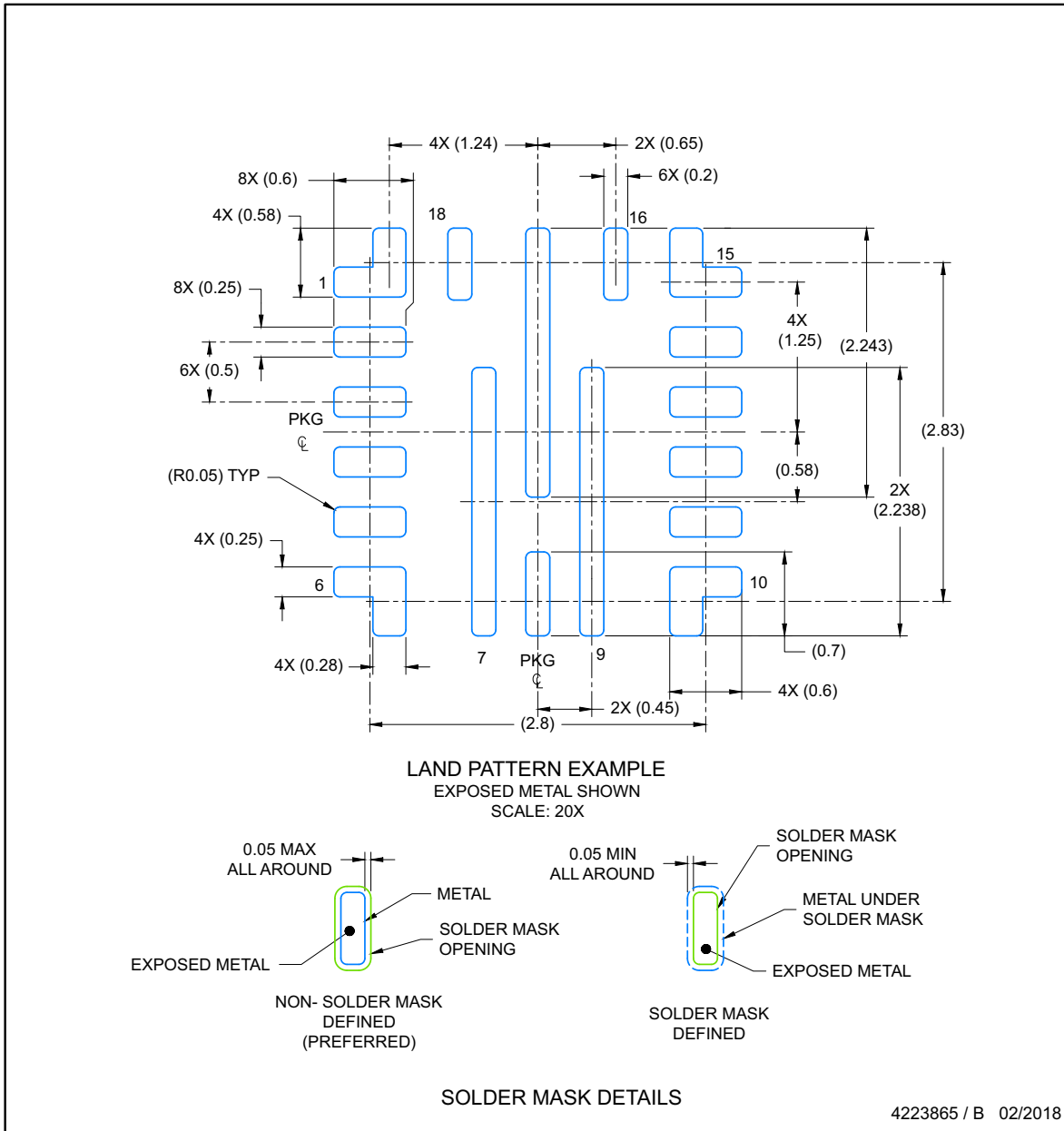
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

**EXAMPLE BOARD LAYOUT**  
**VQFN-HR - 1 mm max height**

**RJE0018B**

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

- For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)) .
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

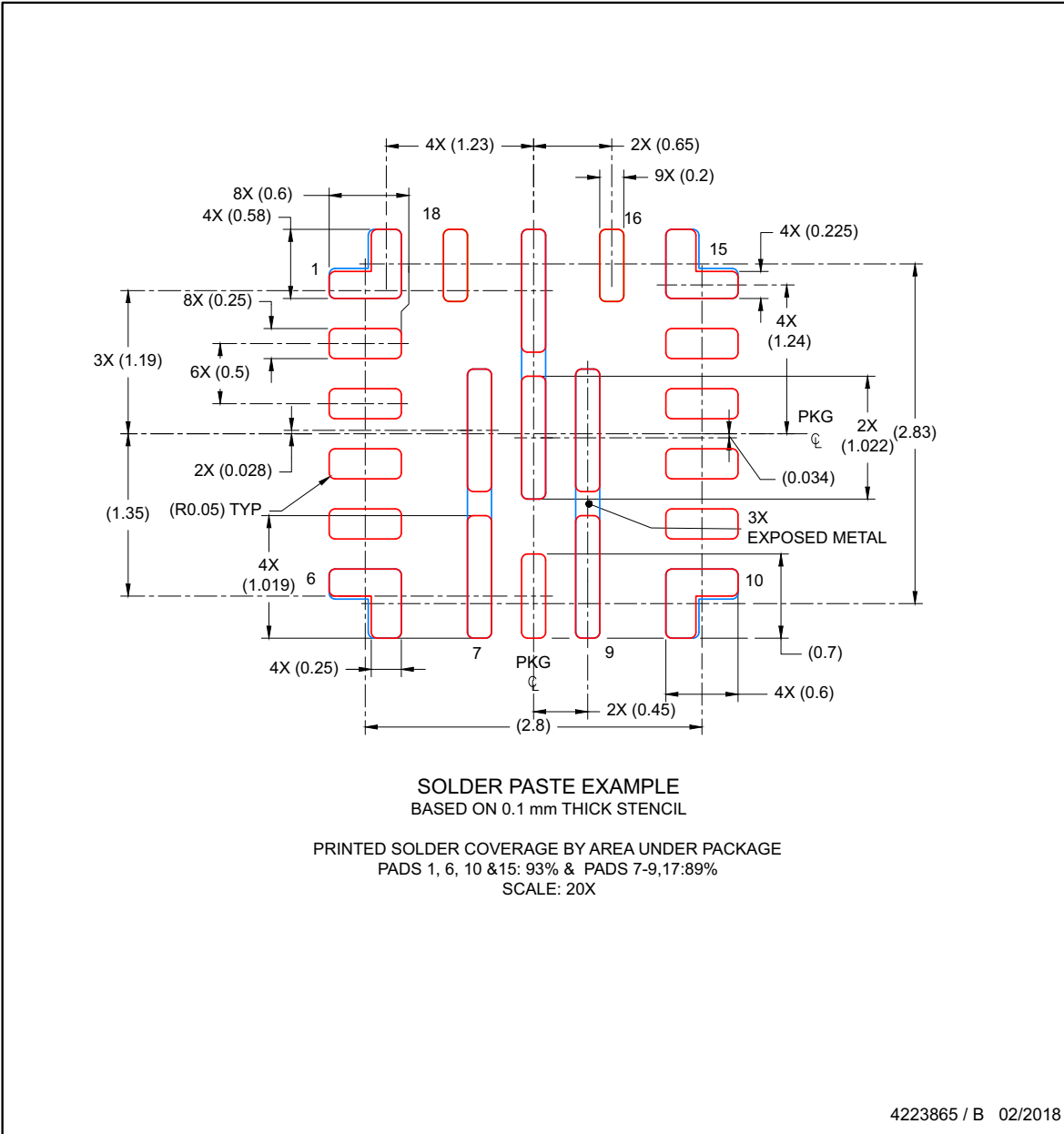


EXAMPLE STENCIL DESIGN

RJE0018B

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65295RJER	ACTIVE	VQFN-HR	RJE	18	3000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	65295	Samples
TPS65295RJET	ACTIVE	VQFN-HR	RJE	18	250	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	65295	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

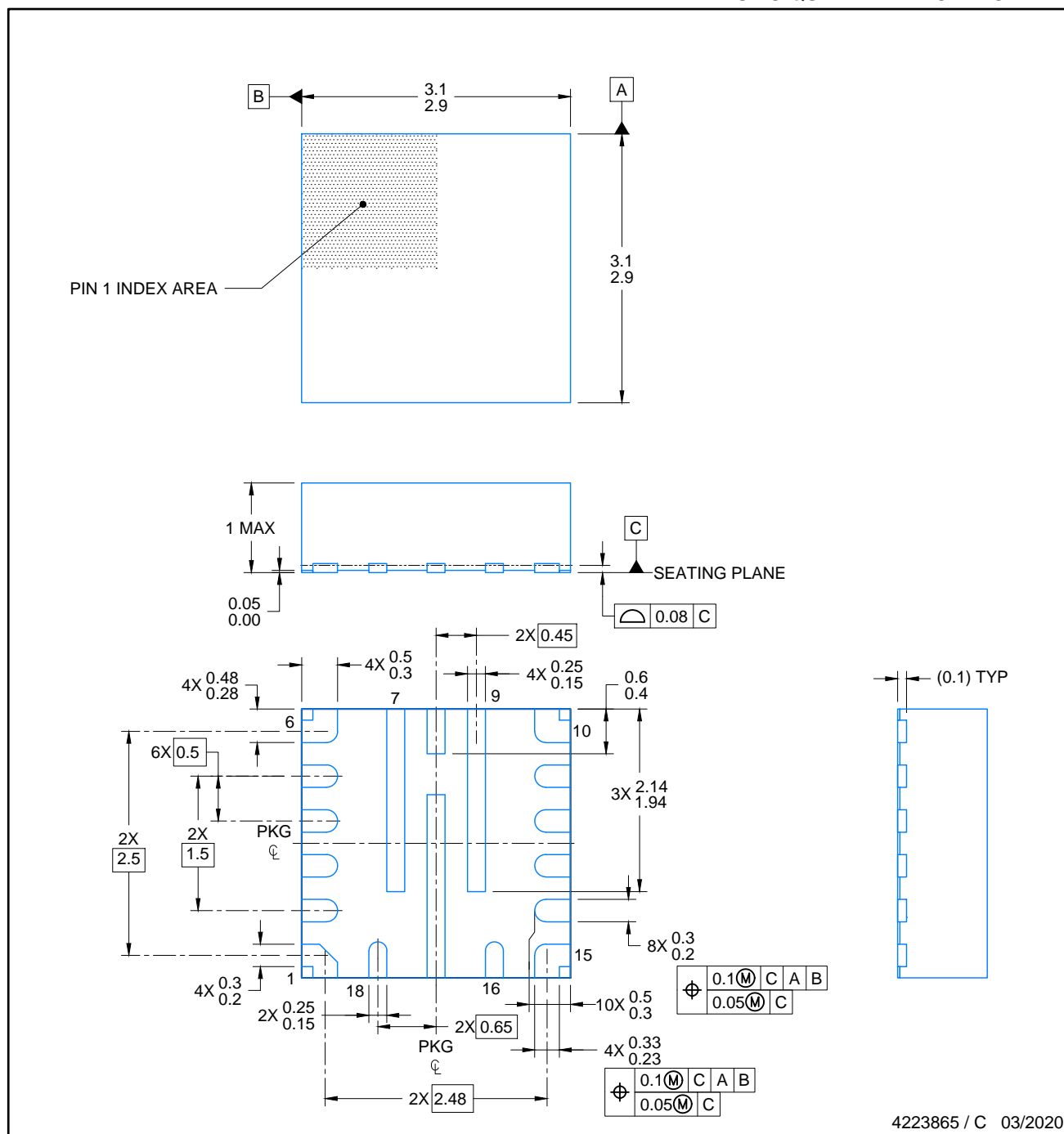
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

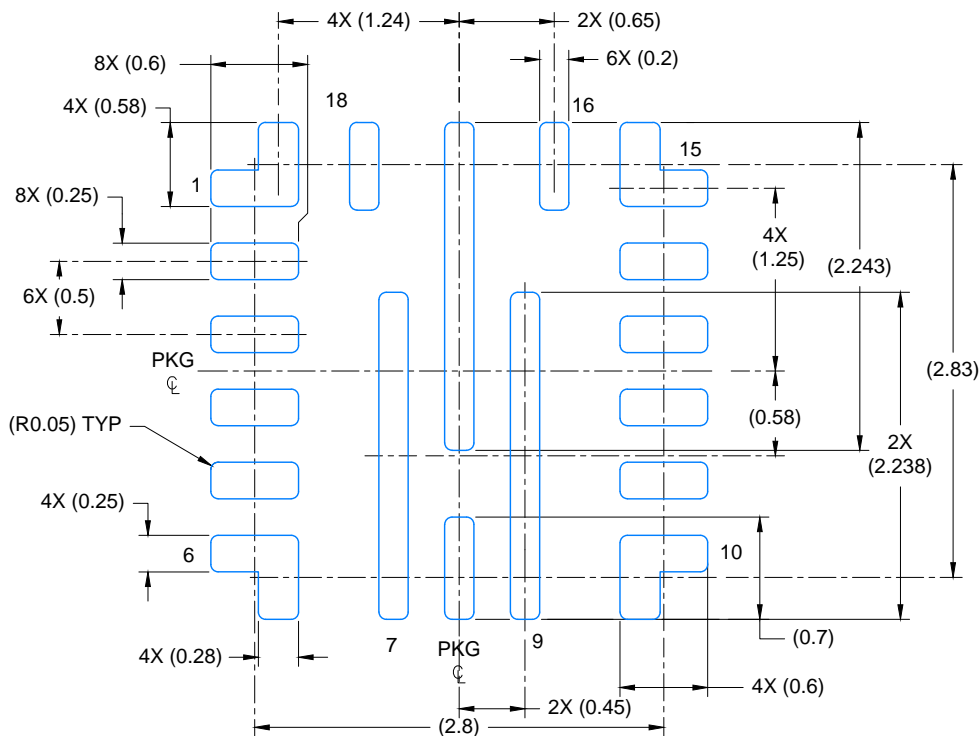
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



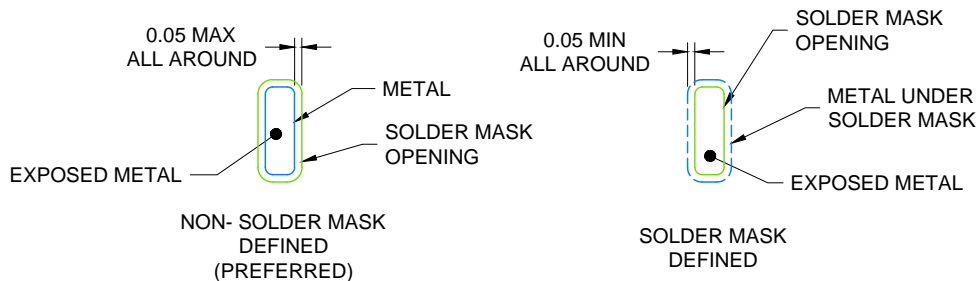


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

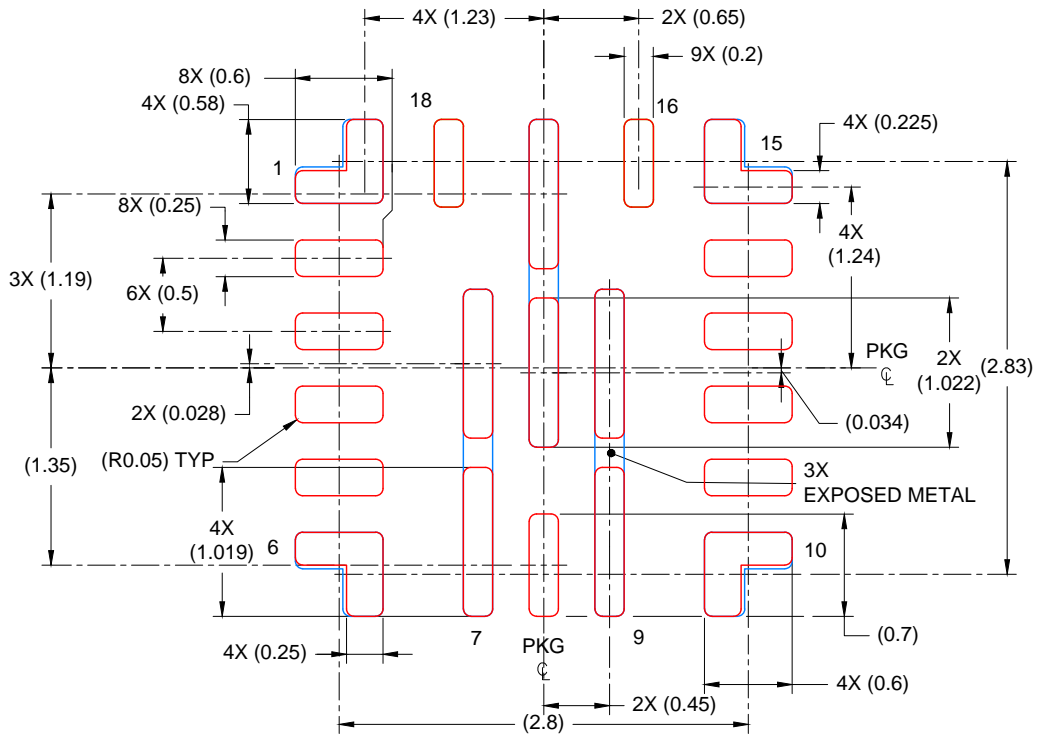


SOLDER MASK DETAILS

4223865 / C 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 PADS 1, 6, 10 & 15: 93% & PADS 7-9, 17: 89%  
 SCALE: 20X

4223865 / C 03/2020

NOTES: (continued)

- 5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司