带有集成场效应晶体管 (FET) (SWIFT™) 的 2.2V 至 4V，14A 输出同步降压脉宽调制 (PWM) 开关

查询样品: TPS54010-EP

特性

- 单独的低压电源总线
- **14A** 持续输出时，用于实现高效率的 **8mΩ** 金属氧化物半导体场效应晶体管 **(MOSFET)** 开关
- 输出电压可调低至 **0.9V**
- 具有 **1%** 内部基准精度的外部补偿
- 快速瞬态响应
- 宽 **PWM** 频率：可在 **280kHz** 至 **700kHz** 之间调节
- 受到峰值电流限制和热关断保护的负载
- 集成解决方案减少了电路板面积和总体成本
- **SWIFT** 文档，操作说明书和设计软件，请见：**www.ti.com/swift**

应用范围

- 可在 **2.5V**，**3.3V** 上配电的低压、高密度系统
- 针对高性能数字信号处理器 **(DSP)**、现场可编程栅极阵列 **(FPGA)**、特定用途集成电路 **(ASIC)**、和微处理器的负载点调节
- 宽带、网络互联及光纤通信基础设施

支持国防、航空航天、和医疗应用

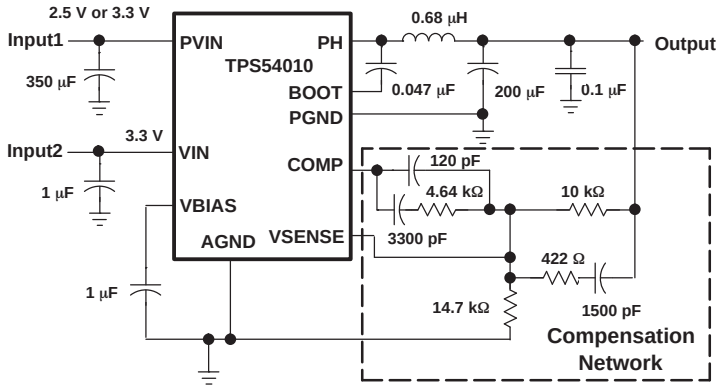
- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 支持军用（**-55°C** 至 **125°C**）温度范围
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

说明

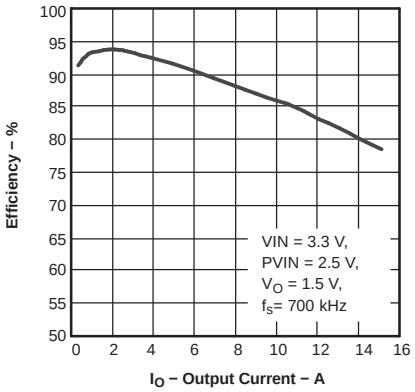
作为 SWIFT ™ 系列 dc/dc 稳压器产品的一员，TPS54010 低输入电压、高输出电流同步降压 PWM 转换器集成了所需的全部有源组件。 基板上包含了一款具有所列特性的真正高性能电压误差放大器，此放大器可实现瞬态条件下的最大性能并在输出滤波器 L 和 C 组件选择方面提供很大的灵活性；一个欠压闭锁电路在 VIN 输出电压达到 3V 前防止启动；一个内部和外部缓启动设定电路课可限制涌入电流；而一个电源正常输出用于处理器/逻辑电路复位、故障信号发送和电源排序。

TPS54010 采用耐热增强型 28 引脚薄型小尺寸 (TSSOP)(PWP) PowerPAD™ 封装，这种封装免除了对大型散热装置的需要。

SIMPLIFIED SCHEMATIC



EFFICIENCY VS OUTPUT CURRENT



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	OUTPUT VOLTAGE	PACKAGE	ORDERABLE PART NUMBER	VID NUMBER
–55°C to 125°C	Adjustable down to 0.9 V	Plastic HTSSOP (PWP)	TPS54010MPWPREP	V62/13604-01XE
			TPS54010MPWPEP	V62/13604-01XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			TPS54010	UNIT
V_I	Input voltage range	SS/ENA, SYNC	–0.3 to 7	V
		RT	–0.3 to 6	
		VSENSE	–0.3 to 4	
		PVIN, VIN	–0.3 to 4.5	
		BOOT	–0.3 to 10	
V_O	Output voltage range	VBIAS, COMP, PWRGD	–0.3 to 7	V
		PH	–0.6 to 6	
V_O	Source current	PH	Internally limited	
		COMP, VBIAS	6	mA
I_S	Sink current	PH	25	A
		COMP	6	mA
		SS/ENA, PWRGD	10	
	Voltage differential	AGND to PGND	±0.3	V
T_J	Junction temperature range		–55 to 150	°C
T_{stg}	Storage temperature range		–65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C
	Electrostatic Discharge (ESD) ratings	Human body model (HBM)	1.5	kV
		CDM	750	V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage, VIN	3		4	V
	Power Input voltage, PVIN	2.2		4	V
T_J	Operating junction temperature	–55		125	°C

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54010 PWP 28 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	30.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	13.5	
θ_{JB}	Junction-to-board thermal resistance(4)	11.6	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	11.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.9	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

ELECTRICAL CHARACTERISTICS

T_J = -55°C to 125°C, VIN = 3 V to 4 V, PVIN = 2.2 V to 4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN							
V_I	Input voltage, VIN			3		4	V
	Supply voltage range, PVIN		Output = 1.8 V	2.2		4	V
I_Q	Quiescent current	VIN	f_s = 350 kHz, RT open, PH pin open, PVIN = 2.5 V, SYNC = 0 V		6.3	10	mA
			f_s = 550 kHz, RT open, PH pin open, SYNC ≥ 2.5 V, PVIN = 2.5 V		8.3	13	mA
			SHUTDOWN, SS/ENA = 0 V, PVIN = 2.5 V		1	1.4	mA
		PVIN	f_s = 350 kHz, RT open, PH pin open, PVIN = 3.3 V, SYNC = 0 V		6	8	mA
			f_s = 550 kHz, RT open, PH pin open, SYNC ≥ 2.5 V, PVIN = 2.5 V, VIN = 3.3 V		6	10	mA
			SHUTDOWN, SS/ENA = 0 V, VIN = 3.3 V		<140		µA
UNDERVOLTAGE LOCKOUT (VIN)							
	Start threshold voltage, UVLO				2.95	3	V
	Stop threshold voltage, UVLO			2.7	2.8		V
	Hysteresis voltage, UVLO				0.11		V
	Rising and falling edge deglitch, UVLO(1)				2.5		µs
BIAS VOLTAGE							
	Output voltage, VBIAS		$I_{(VBIAS)}$ = 0	2.7	2.8	2.95	V
	Output current, VBIAS(2)					100	µA
CUMULATIVE REFERENCE							
V_{ref}	Accuracy			0.879	0.891	0.903	V

(1) Specified by design from -40°C to 125°C
(2) Static resistive loads only

ELECTRICAL CHARACTERISTICS (continued)

T_J = -55°C to 125°C, VIN = 3 V to 4 V, PVIN = 2.2 V to 4 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REGULATION					
Line regulation(3) (4)	I_L = 7 A, f_s = 350 kHz, T_J = 85°C		0.05		%/V
Load regulation(3) (4)	I_L = 0 A to 14 A, f_s = 350 kHz, T_J = 85°C PVIN = 2.5 V, VIN = 3.3 V		0.013		%/A
OSCILLATOR					
Internally set—free running frequency	RT open, SYNC ≤ 0.8 V	225	350	455	kHz
	RT open, SYNC ≥ 2.5 V	435	550	660	
Externally set—free running frequency range	RT = 180 kΩ (1% resistor to AGND)(3)	252	280	308	kHz
	RT = 100 kΩ (1% resistor to AGND)	432	500	540	
	RT = 68 kΩ (1% resistor to AGND)(3)	663	700	762	
High-level threshold voltage, SYNC		2.5			V
Low-level threshold voltage, SYNC				0.8	V
Pulse duration, SYNC(3)		50			ns
Frequency range, SYNC		300		700	kHz
Ramp valley(3)			0.75		V
Ramp amplitude (peak-to-peak)(3)			1		V
Minimum controllable on time(3)				200	ns
Maximum duty cycle(3)		90%			
ERROR AMPLIFIER					
Error amplifier open-loop voltage gain	1 kΩ COMP to AGND(3)	90	110		dB
Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(3)	3	5		MHz
Error amplifier common mode input voltage range	Powered by internal LDO(3)	0		VBIAS	V
Input bias current, VSENSE	VSENSE = V_{ref}		60	300	nA
Output voltage slew rate (symmetric), COMP			1.4		V/µs
PWM COMPARATOR					
PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive(3)		70	85	ns
SLOW-START/ENABLE					
Enable threshold voltage, SS/ENA		0.82	1.2	1.4	V
Enable hysteresis voltage, SS/ENA(3)			0.03		V
Falling edge deglitch, SS/ENA(3)			2.5		µs
Internal slow-start time		2.1	3.35	4.1	ms
Charge current, SS/ENA	SS/ENA = 0 V	2	5	8.3	µA
Discharge current, SS/ENA	SS/ENA = 0.2 V, VIN = 2.7 V, PVIN = 2.5 V	1.3	2.3	4	mA
POWER GOOD					
Power-good threshold voltage	VSENSE falling		93		%V_{ref}
Power-good hysteresis voltage(3)			3		%V_{ref}
Power-good falling edge deglitch(3)			35		µs
Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
Leakage current, PWRGD	VIN = 3.3 V, PVIN = 2.5 V			1	µA
CURRENT LIMIT					
Current limit	VIN = 3.3 V, PVIN = 2.5 V (3), Output shorted	14.5	21		A
Current limit leading edge blanking time(3)			100		ns
Current limit total response time(3)			200		ns
THERMAL SHUTDOWN					
Thermal shutdown trip point(3)		135	165		°C
Thermal shutdown hysteresis(3)			10		°C

(3) Specified by design from -40°C to 125°C
(4) Specified by the circuit used in Figure 12

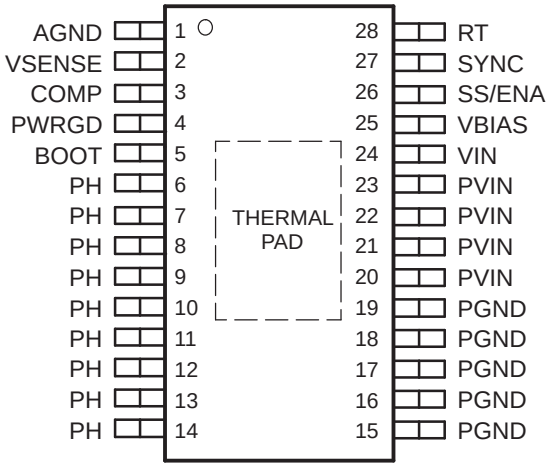
ELECTRICAL CHARACTERISTICS (continued)

T_J = -55°C to 125°C, VIN = 3 V to 4 V, PVIN = 2.2 V to 4 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT POWER MOSFETS					
$r_{DS(on)}$ Power MOSFET switches	VIN = 3 V, PVIN = 2.5 V		8	21	mΩ
	VIN = 3.6 V, PVIN = 2.5 V		8	18	

DEVICE INFORMATION

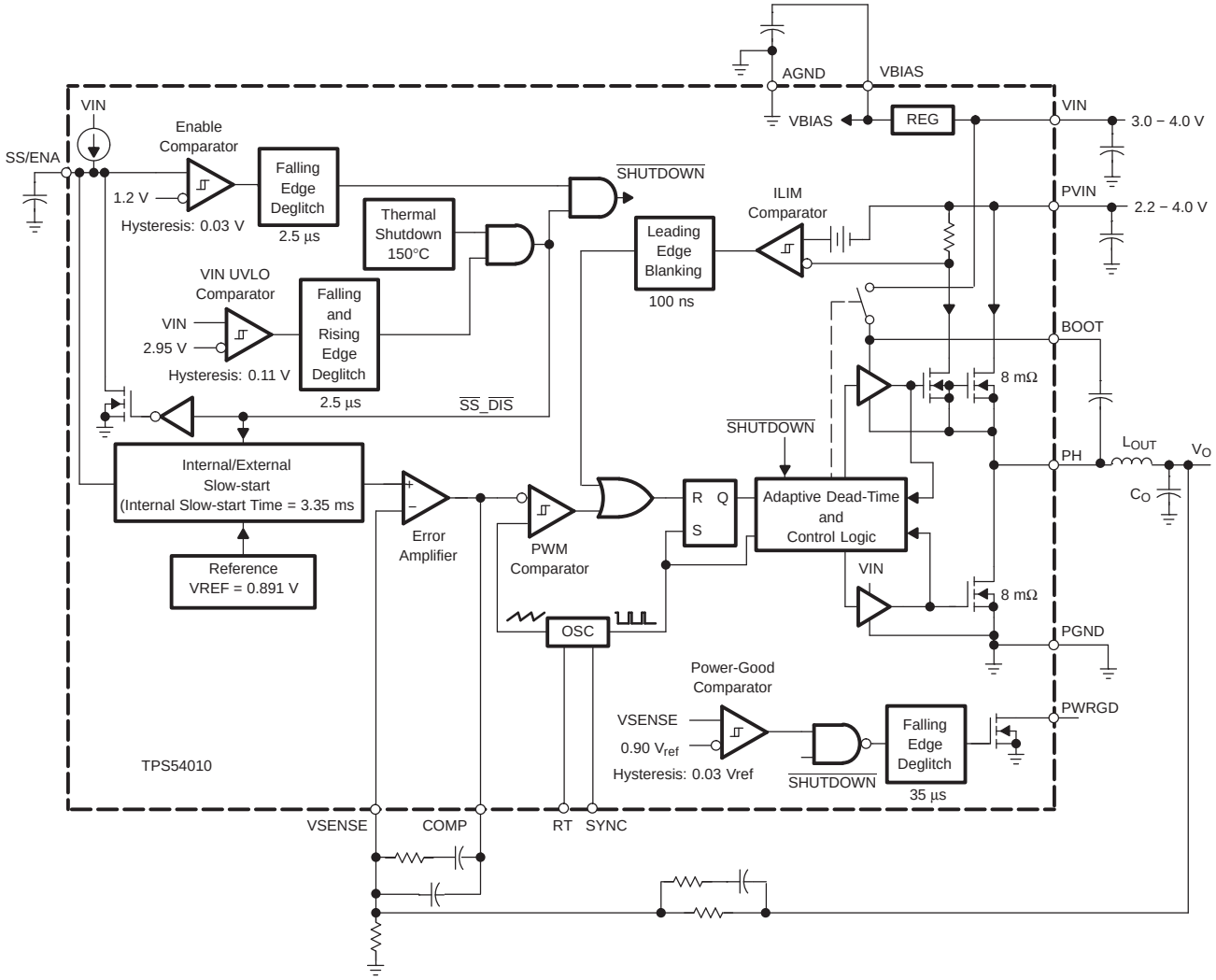
PWP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

PIN NAME	PIN NUMBER	DESCRIPTION
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, and RT resistor. If using the PowerPAD, connect it to AGND. See the *Application Information* section for details.
BOOT	5	Bootstrap output. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
PGND	15, 16, 17, 18, 19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6-14	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PVIN	20, 21, 22, 23	Input supply for the power MOSFET switches and internal bias regulator. Bypass the PVIN pins to the PGND pins close to device package with a high-quality, low-ESR 10-µF ceramic capacitor.
PWRGD	4	Power-good open-drain output. High when VSENSE > 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s.
SS/ENA	26	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	27	Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high-quality, low-ESR 0.1-µF to 1.0-µF ceramic capacitor.
VIN	24	Input supply for the internal control circuits. Bypass the VIN pin to the PGND pins close to device package with a high-quality, low-ESR 1-µF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

Figure 1. FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

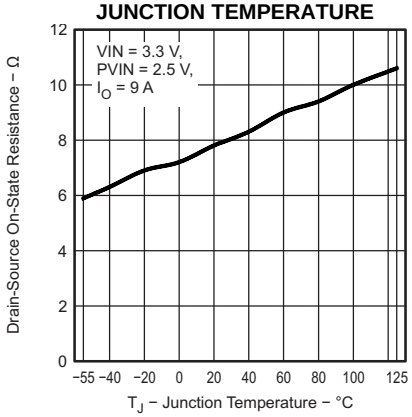


Figure 2.

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

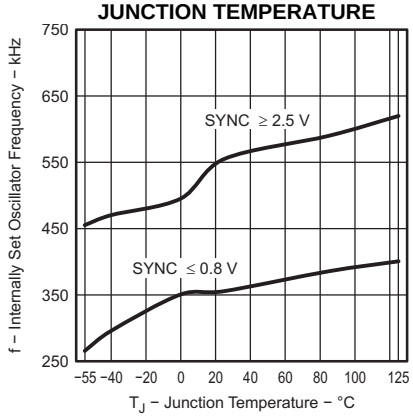


Figure 3.

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

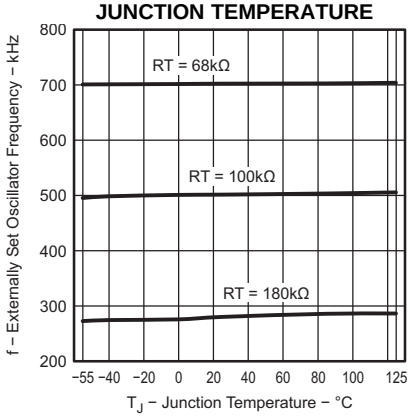


Figure 4.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

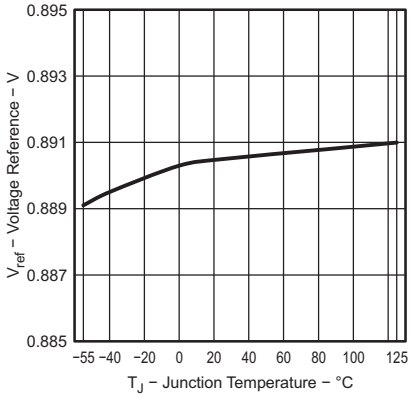


Figure 5.

DEVICE POWER DISSIPATION vs OUTPUT CURRENT

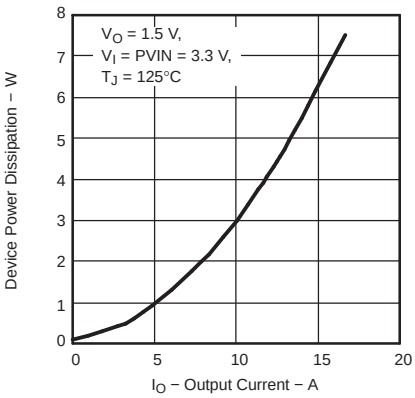


Figure 6.

REFERENCE VOLTAGE vs INPUT VOLTAGE

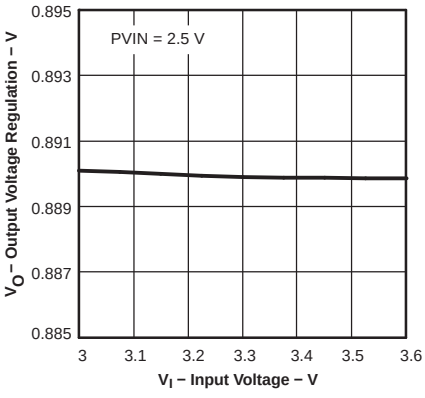


Figure 7.

ERROR AMPLIFIER OPEN-LOOP RESPONSE

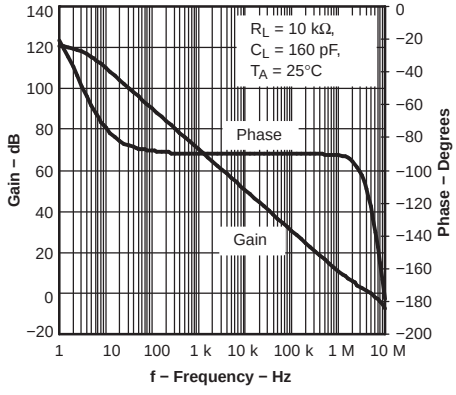


Figure 8.

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

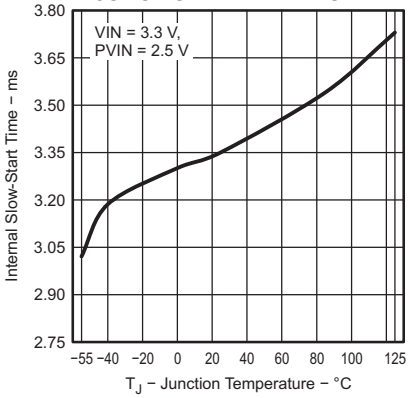


Figure 9.

APPLICATION INFORMATION

PCB LAYOUT

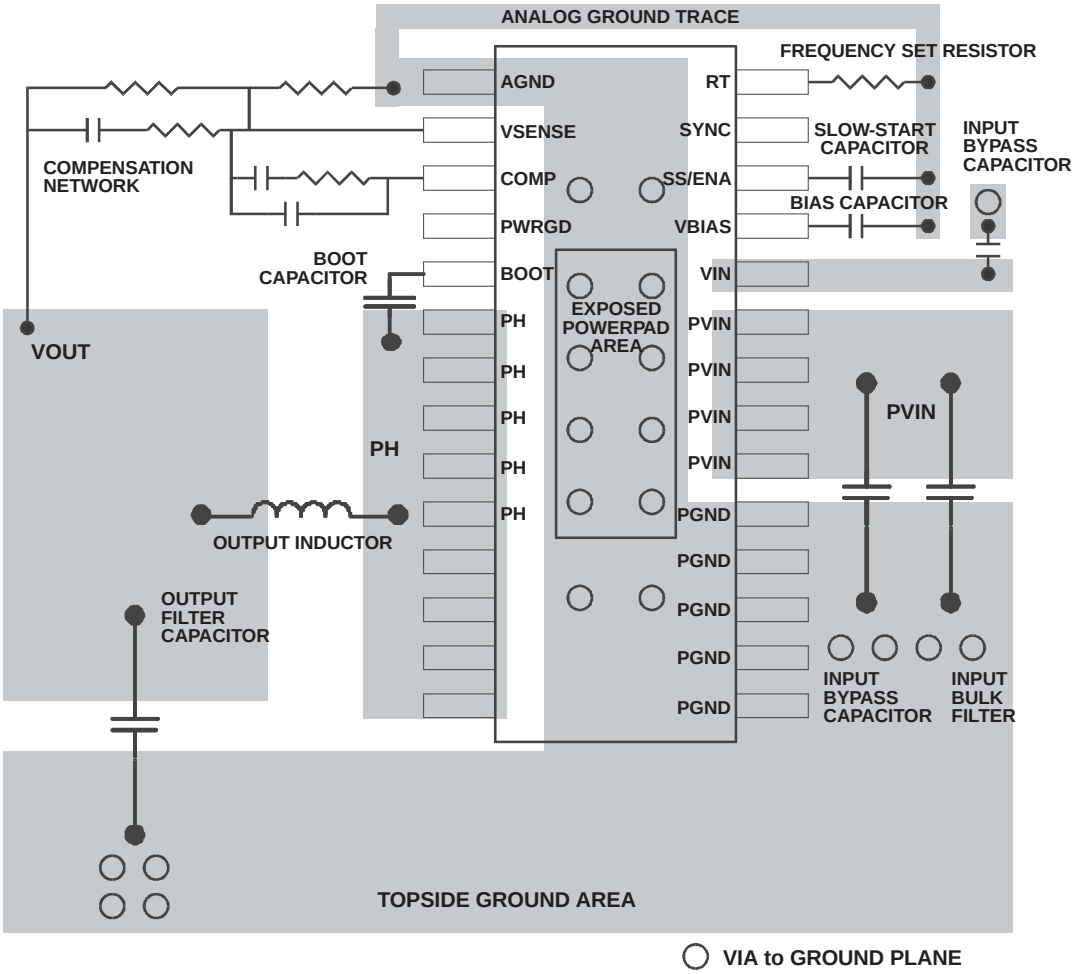


Figure 10. TPS54010 Layout

The PVIN pins are connected together on the printed-circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the TPS54010 ground pins. The minimum recommended bypass capacitance is a 10-µF ceramic capacitor with a X5R or X7R dielectric. The optimum placement is as close as possible to the PVIN pins, the AGND, and PGND pins. See Figure 10 for an example of a board layout. If the VIN is connected to a separate source supply, it is bypassed with its own capacitor. There is an area of ground on the top layer of the PCB, directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors. The AGND and PGND pins are tied to the PCB ground by connecting them to the ground area under the device as shown in Figure 10.

Use a separate wide trace for the analog ground signal path. This analog ground is used for the voltage set point divider, timing resistor RT, slow-start capacitor, and bias capacitor grounds. The PH pins are tied together and routed to the output inductor. Because the PH connection is the switching node, an inductor is located close to the PH pins, and the area of the PCB conductor is minimized to prevent excessive capacitive coupling. Connect the boot capacitor between the phase node and the BOOT pin as shown in Figure 10. Keep the boot capacitor close to the IC, and minimize the conductor trace lengths. Connect the output filter capacitor(s) between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, Lout, Cout, and PGND as small as is practical. Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pinout, they must be routed

close, but maintain as much separation as possible while keeping the layout compact. Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If a slow-start capacitor or RT resistor is used, or if the SYNC pin is used to select 350-kHz operating frequency, connect them to this trace.

For operation at full rated load current, the analog ground plane must provide an adequate heat-dissipating area. A 3-inch by 3-inch plane of 1-ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD must be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available must be used when 6-A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer must be made using 0.013-inch diameter vias to avoid solder wicking through the vias.

Eight vias must be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the twelve recommended that enhance thermal performance must be included in areas not under the device package.

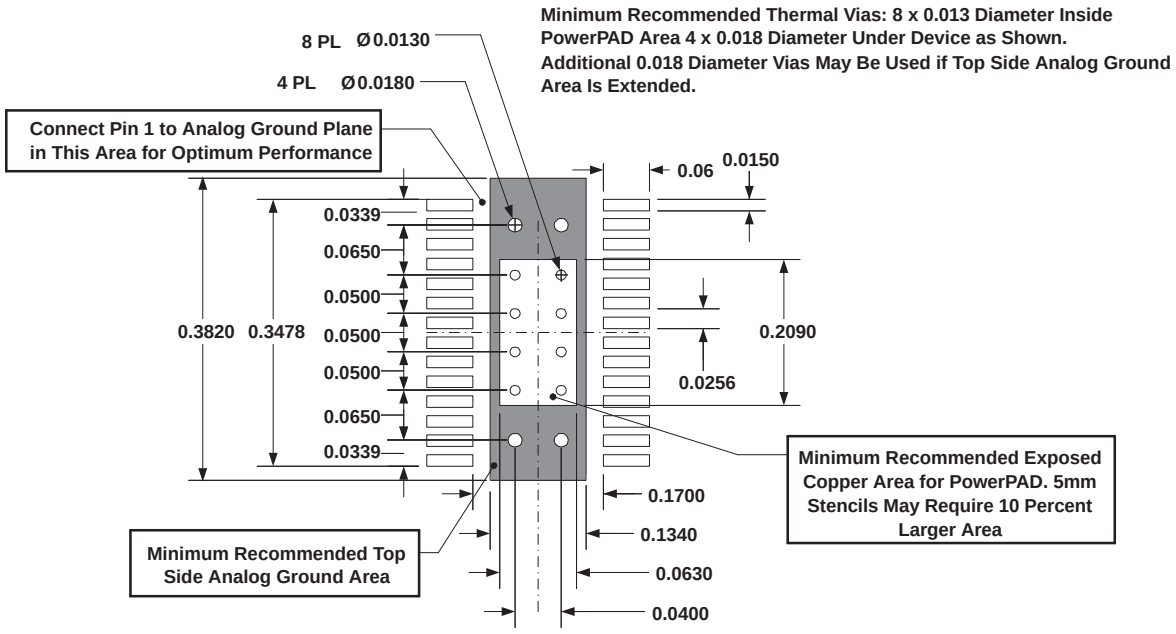


Figure 11. Recommended Land Pattern for 28-Pin PWP PowerPAD

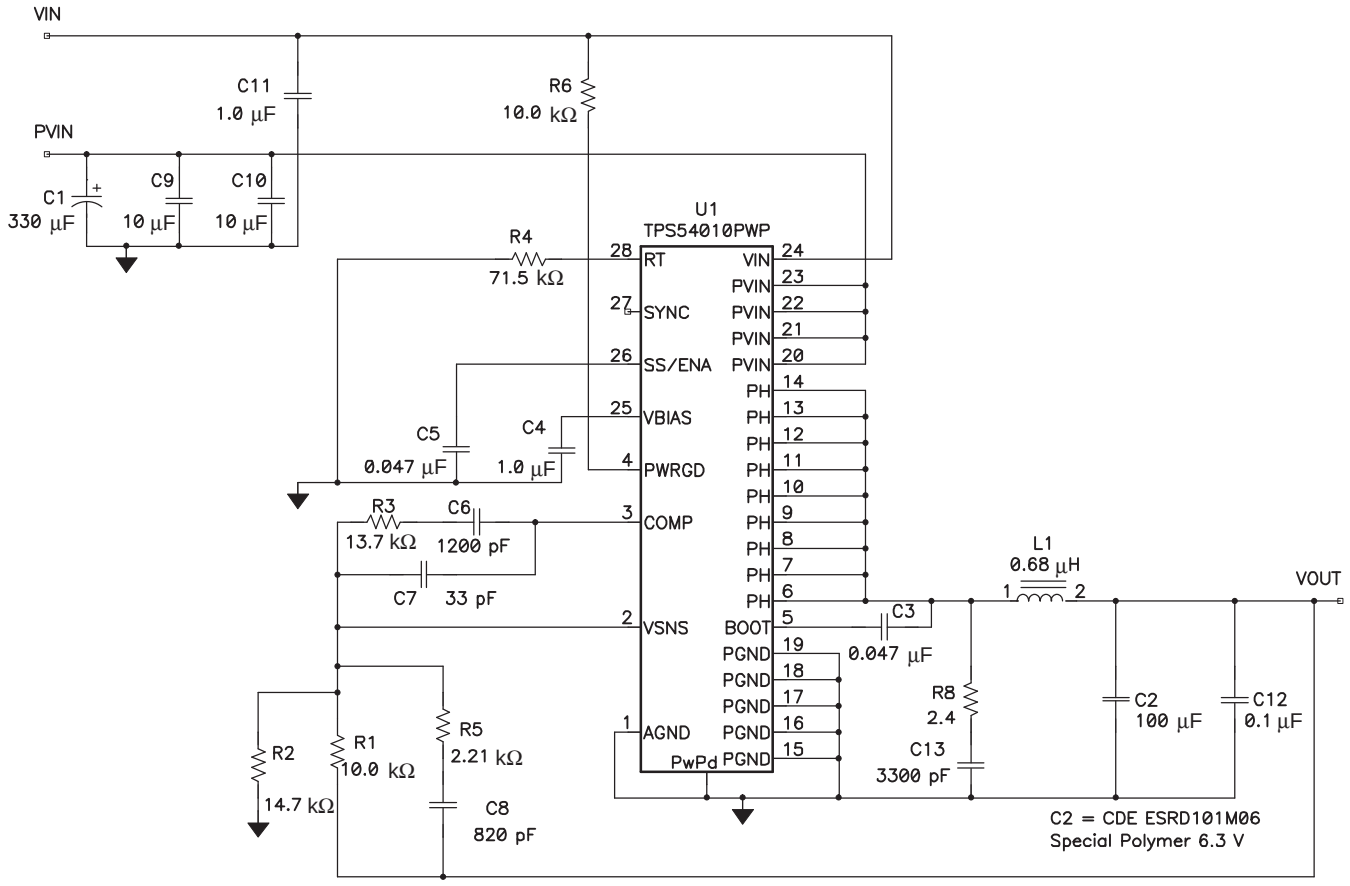


Figure 12. Application Circuit, 2.5 V to 1.5 V

Figure 12 shows the schematic for a typical TPS54010 application. The TPS54010 can provide up to 14-A output current at a nominal output voltage of 1.5 V. Nominal input voltages are 2.5 V for PVIN and 3.3 V for VIN. For proper thermal performance, the exposed PowerPAD underneath the device must be soldered down to the printed-circuit board.

DESIGN PROCEDURE

The following design procedure can be used to select component values for the TPS54010. Alternately, the SWIFT Designer Software may be used to generate a complete design. The SWIFT Designer Software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

DESIGN PARAMETERS

To begin the design process, a few parameters must be decided. The designer needs to know:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

For this design example, use the following as the input parameters:

Table 1.

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (VIN)	3.3 V
Input voltage range (PVIN)	2.2 to 3.5 V
Output voltage	1.5 V
Input ripple voltage	300 mV
Output ripple voltage	50 mV
Output current rating	14 A
Operating frequency	700 kHz

SWITCHING FREQUENCY

The switching frequency can be set to either one of two internally programmed frequencies or set to a externally programmed frequency. With the RT pin open, setting the SYNC pin at or above 2.5 V selects 550-kHz operation, whereas grounding or leaving the

SYNC pin open selects 350-kHz operation. For this design, the switching frequency is externally programmed using the RT pin. By connecting a resistor (R4) from RT to AGND, any frequency in the range of 250 to 700 kHz can be set. Use Equation 1 to determine the proper value of RT.

$$R4(k\Omega) = \frac{500\ kHz}{f_S(kHz)} \times 100\ k\Omega \quad (1)$$

In this example circuit, R4 is calculated to be 71.5 kΩ and the switching frequency is set at 700 kHz.

INPUT CAPACITORS

The TPS54010 requires an input de-coupling capacitor and, depending on the application, a bulk input capacitor. The minimum value for the de-coupling capacitor, C9, is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. Additionally, some bulk capacitance may be needed, especially if the TPS54010 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable.

This input ripple voltage can be approximated by Equation 2:

$$\Delta V_{PVIN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum load current.

The TPS54010 requires an input de-coupling capacitor and, depending on the application, a bulk input capacitor. f_{sw} is the switching frequency, $C_{(BULK)}$ is the bulk capacitor value and ESR_{MAX} is the maximum series resistance of the bulk capacitor.

The maximum RMS ripple current also needs to be checked. For worst-case conditions, this can be approximated by Equation 3:

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (3)$$

In this case, the input ripple voltage would be 155 mV and the RMS ripple current would be 7 A. The maximum voltage across the input capacitors would be Vin max plus delta Vin/2. The chosen bulk capacitor, a Sanyo POSCAP 6TPD330M is rated for 6.3 V and 4.4 A of ripple current; two bypass capacitors, TDK C3225X5R1C106M are each rated for 16 V, and the ripple current capacity is greater than 3 A at the operating frequency of 700 kHz. Total ripple current handling is in excess of 10.4 A. It is important that the maximum ratings for voltage and current are not exceeded under any circumstance.

OUTPUT FILTER COMPONENTS

Two components need to be selected for the output filter, L1 and C2. Because the TPS54010 is an externally compensated device, a wide range of filter component types and values can be supported.

Inductor Selection

To calculate the minimum value of the output inductor, use Equation 4

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{in(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{sw}} \quad (4)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. For designs using low ESR output capacitors such as ceramics, use K_{IND} = 0.3. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.2 to keep the inductor ripple current small. The minimum inductor value is calculated to be 0.44 µH.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 5:

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left[V_{OUT} \times \frac{\left(V_{in(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{sw} \times 0.8}\right]^2} \quad (5)$$

and the peak inductor current can be found from Equation 6

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{in(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{sw}} \quad (6)$$

For this design, the RMS inductor current is 15.4 A, and the peak inductor current is 15.1 A. For this design, a Vishay IHLP2525CZ-01 style output inductor is specified. The largest value greater than 0.44 µH that meets these current requirements is 0.68 µH. Increasing the inductor value decreases the ripple current and the corresponding output ripple voltage. The inductor value can be decreased if more margin in the RMS current is required. In general, inductor values for use with the TPS54010 falls in the range of 0.47 to 2.2 µH.

Capacitor Requirements

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed-loop crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the closed-loop crossover frequency at less than 1/5 of the switching frequency. With high switching frequencies such as the 500 kHz frequency of this design, internal circuit limitations of the TPS54010 limit the practical maximum crossover frequency to about 70 kHz. To allow for adequate phase gain in the compensation network, the LC corner frequency should be about one decade or so below the closed-loop crossover frequency. This limits the minimum capacitor value for the output filter to:

$$C_{OUT(MIN)} = \frac{1}{L_{OUT}} \times \left(\frac{K}{2\pi \ f_{CO}} \right)^2 \quad (7)$$

Where K is the frequency multiplier for the spread between f_{LC} and f_{CO}. K should be between 5 and 15, typically 10 for one decade difference. For a desired crossover of 100-kHz and a 0.68-µH inductor, the minimum value for the output capacitor is 93 µF using a minimum K factor of 5. Increasing the K factor would require using a larger capacitance as 100 kHz is approaching the maximum practical closed-loop crossover frequency for this device. The selected output capacitor must be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any de-rating amount must also be included. The maximum RMS ripple current in the output capacitors is given by Equation 8:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{PVIN(MAX)} - V_{OUT} \right)}{V_{PVIN(MAX)} \times L_{OUT} \times F_{sw}} \right) \quad (8)$$

The calculated RMS ripple current is 780 mA in the output capacitors.

The maximum ESR of the output capacitor is determined by the amount of allowable output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter; therefore, the maximum specified ESR as listed in the capacitor data sheet is given by Equation 9 :

$$ESR_{MAX} = N_C \times \left(\frac{V_{IN(MAX)} \times L_{OUT} \times F_{sw} \times 0.8}{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)} \right) \times \Delta V_{P-P(MAX)} \quad (9)$$

and the maximum ESR required is 22.2 mΩ. A capacitor that meets these requirements is a Cornell Dubilier Special Polymer (SP) ESRD101M06 rated at 6.3 V with a maximum ESR of 0.015 Ω and a ripple current rating of 2 A. An additional small 0.1-µF ceramic bypass capacitor C13 is a also used.

Other capacitor types work well with the TPS54010, depending on the needs of the application.

Compensation Components

The external compensation used with the TPS54010 allows for a wide range of output filter configurations. A large range of capacitor values and types of dielectric are supported. The design example uses Type-3 compensation consisting of R1, R3, R5, C6, C7, and C8. Additionally, R2 along with R1 forms a voltage divider network that sets the output voltage. These component reference designators are the same as those used in the SWIFT Designer Software. There are a number of different ways to design a compensation network. This procedure outlines a relatively simple procedure that produces good results with most output filter combinations. Use the SWIFT Designer Software for designs with unusually high closed-loop crossover frequencies, low value, low ESR output capacitors such as ceramics or if you are unsure about the design procedure.

When designing compensation networks for the TPS54010, a number of factors need to be considered. The gain of the compensated error amplifier should not be limited by the open-loop amplifier gain characteristics and should not produce excessive gain at the switching frequency. Also, the closed-loop crossover frequency should be set less than one-fifth of the switching frequency, and the phase margin at crossover must be greater than 45 degrees. The general procedure outlined here produces results consistent with these requirements without going into great detail about the theory of loop compensation.

First, calculate the output filter LC corner frequency using Equation 10:

$$f_{LC} = \frac{1}{2\pi \sqrt{L_{OUT} C_{OUT}}} \quad (10)$$

For the design example, f_{LC} = 19.3 kHz.

The closed-loop crossover frequency should be chosen to be greater than f_{LC} and less than one-fifth of the switching frequency. Also, the crossover frequency should not exceed 150 kHz, as the error amplifier may not provide the desired gain. For this design, a crossover frequency of 100 kHz was chosen. This value is chosen for comparatively wide loop bandwidth while still allowing for adequate phase boost to insure stability.

Next, calculate the R2 resistor value for the output voltage of 1.5 V using Equation 11:

$$R2 = \frac{R1 \times 0.891}{V_{OUT} - 0.891} \quad (11)$$

For any TPS54010 design, start with an R1 value of 10 kΩ. R2 is 14.7 kΩ.

Now, the values for the compensation components that set the poles and zeros of the compensation network can be calculated. Assuming that R1 >> than R5 and C6 >> C7, the pole and zero locations are given by Equation 12 through Equation 18:

$$f_{Z1} = \frac{1}{2\pi R3C6} \quad (12)$$

$$f_{Z2} = \frac{1}{2\pi R1C8} \quad (13)$$

$$f_{P1} = \frac{1}{2\pi R5C8} \quad (14)$$

$$f_{P2} = \frac{1}{2\pi R3C7} \quad (15)$$

Additionally, there is a pole at the origin, which has unity gain at a frequency:

$$f_{INT} = \frac{1}{2\pi R1C6} \quad (16)$$

This pole is used to set the overall gain of the compensated error amplifier and determines the closed-loop crossover frequency. Because R1 is given as 1 kΩ and the crossover frequency is selected as 100 kHz, the desired f_{INT} can be calculated from Equation 17:

$$f_{INT} = \frac{f_{CO}}{V_{IN(MAX)} \times 2} \quad (17)$$

And the value for C6 is given by Equation 18:

$$C6 = \frac{1}{2\pi R1 f_{INT}} \quad (18)$$

The first zero, f_{Z1} is located at one-half the output filter LC corner frequency; so, R3 can be calculated from:

$$R3 = \frac{1}{\pi C6 f_{LC}} \quad (19)$$

The second zero, f_{Z2} is located at the output filter LC corner frequency; so, C8 can be calculated from:

$$C8 = \frac{1}{2\pi R1 f_{LC}} \quad (20)$$

The first pole, f_{P1} is located to coincide with output filter ESR zero frequency. This frequency is given by:

$$f_{ESR0} = \frac{1}{2\pi R_{ESR} C_{OUT}} \quad (21)$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

In this case, the ESR zero frequency is 88.4 kHz, and R5 can be calculated from:

$$R5 = \frac{1}{2\pi C8 f_{ESR}} \quad (22)$$

The final pole is placed at a frequency above the closed-loop crossover frequency high enough to not cause the phase to decrease too much at the crossover frequency while still providing enough attenuation so that there is little or no gain at the switching frequency. The f_{P2} pole location for this circuit is set to 3.5 times the closed-loop crossover frequency and the last compensation component value C7 can be derived:

$$C7 = \frac{1}{7\pi R3 f_{CO}} \quad (23)$$

Note that capacitors are only available in a limited range of standard values, so the nearest standard value has been chosen for each capacitor. The measured closed-loop response for this design is shown in Figure 5.

BIAS AND BOOTSTRAP CAPACITORS

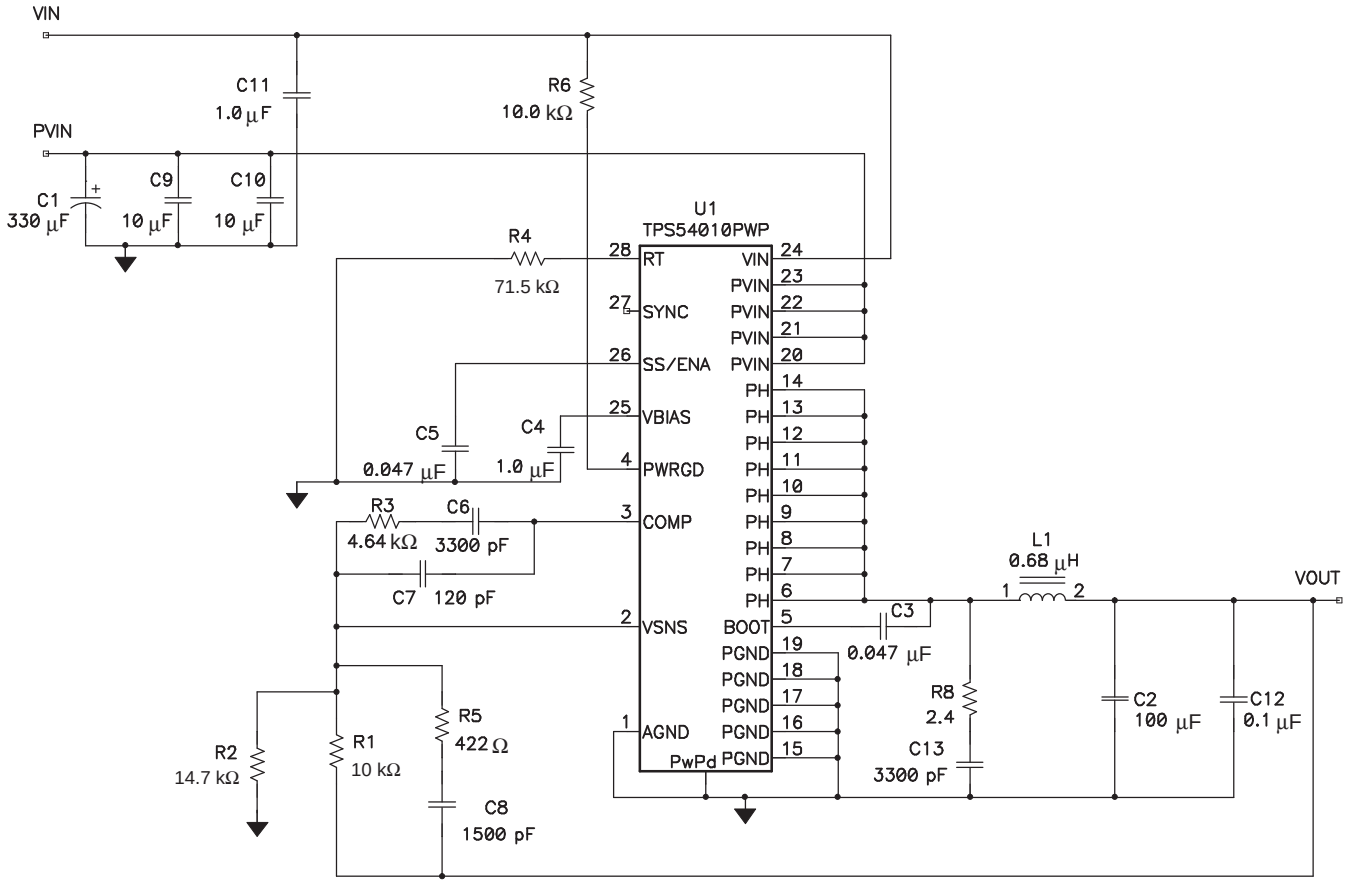
Every TPS54010 design requires a bootstrap capacitor, C3, and a bias capacitor, C4. The bootstrap capacitor must be a 0.1 µF. The bootstrap capacitor is located between the PH pins and BOOT. The bias capacitor is connected between the VBIAS pin and AGND. The value should be 1.0 µF. Both capacitors should be high-quality ceramic types with X7R or X5R grade dielectric for temperature stability. They should be placed as close to the device connection pins as possible.

POWER GOOD

The TPS54010 is provided with a power-good output pin PWRGD. This output is an open-drain output and is intended to be pulled up to a 3.3-V or 5-V logic supply. A 10-kΩ pullup works well in this application.

SNUBBER CIRCUIT

R10 and C11 of the application schematic comprise a snubber circuit. The snubber is included to reduce overshoot and ringing on the phase node when the internal high-side FET turns on. Because the frequency and amplitude of the ringing depends to a large degree on parasitic effects, it is best to choose these component values based on actual measurements of any design layout. See literature number SLUP100 for more detailed information on snubber design.



The following part numbers are used for test purposes:

C1 = T520D337M0O4ASE015 (Kemet)

C2 = TDK C3225X5R0J107M ceramic 6.3 V X5R

L1 = IHLP2525CZ−01 0.68 µH (Vishay Dale)

Figure 13. 1.5-V Power Supply With Ceramic Output Capacitors

Figure 13 shows an application where all ceramic capacitors, including the main output filter capacitor, are used. The compensation network components were calculated using SWIFT Designer Software. See Figure 22 through Figure 30 for loop response, performance graphs, and switching waveforms for this circuit.

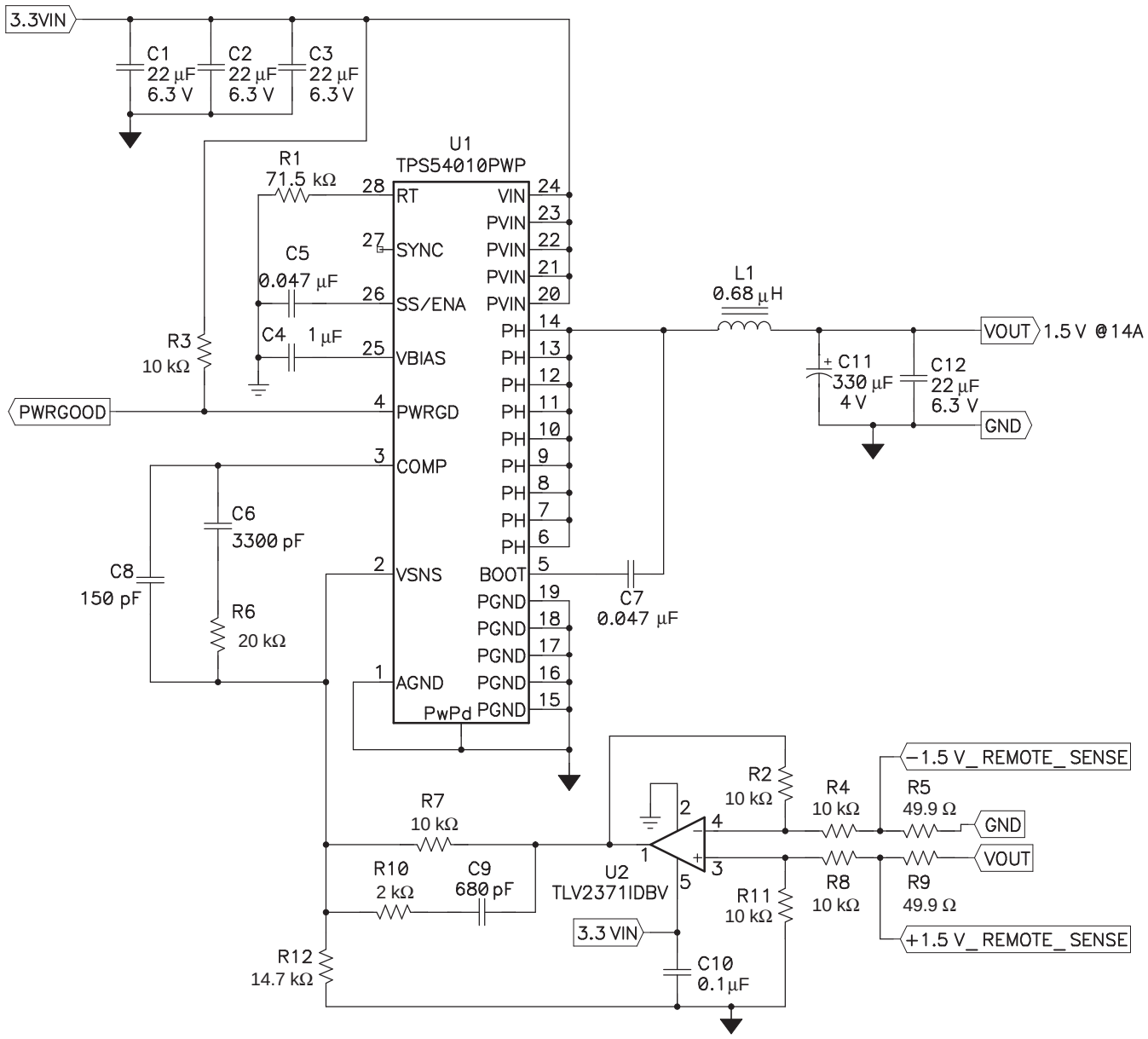


Figure 14. 1.5-V Power Supply With Remote Sense

With an output current of 14 A, if the load is located far from the dc/dc converter circuit, it may be beneficial to include a remote sense capability. Figure 14 is an example of a power supply incorporating active differential remote sensing. As the TPS54010 only has a positive VSENSE input, this circuit compensates for voltage drops in both the output voltage rail and the return (GND). The difference amplifier of U2 forces the output of the TPS54010 to generate an output voltage that maintains a constant 1.5-V difference between +1.5V_REMOTE_SENSE and -1.5V_REMOTE_SENSE.

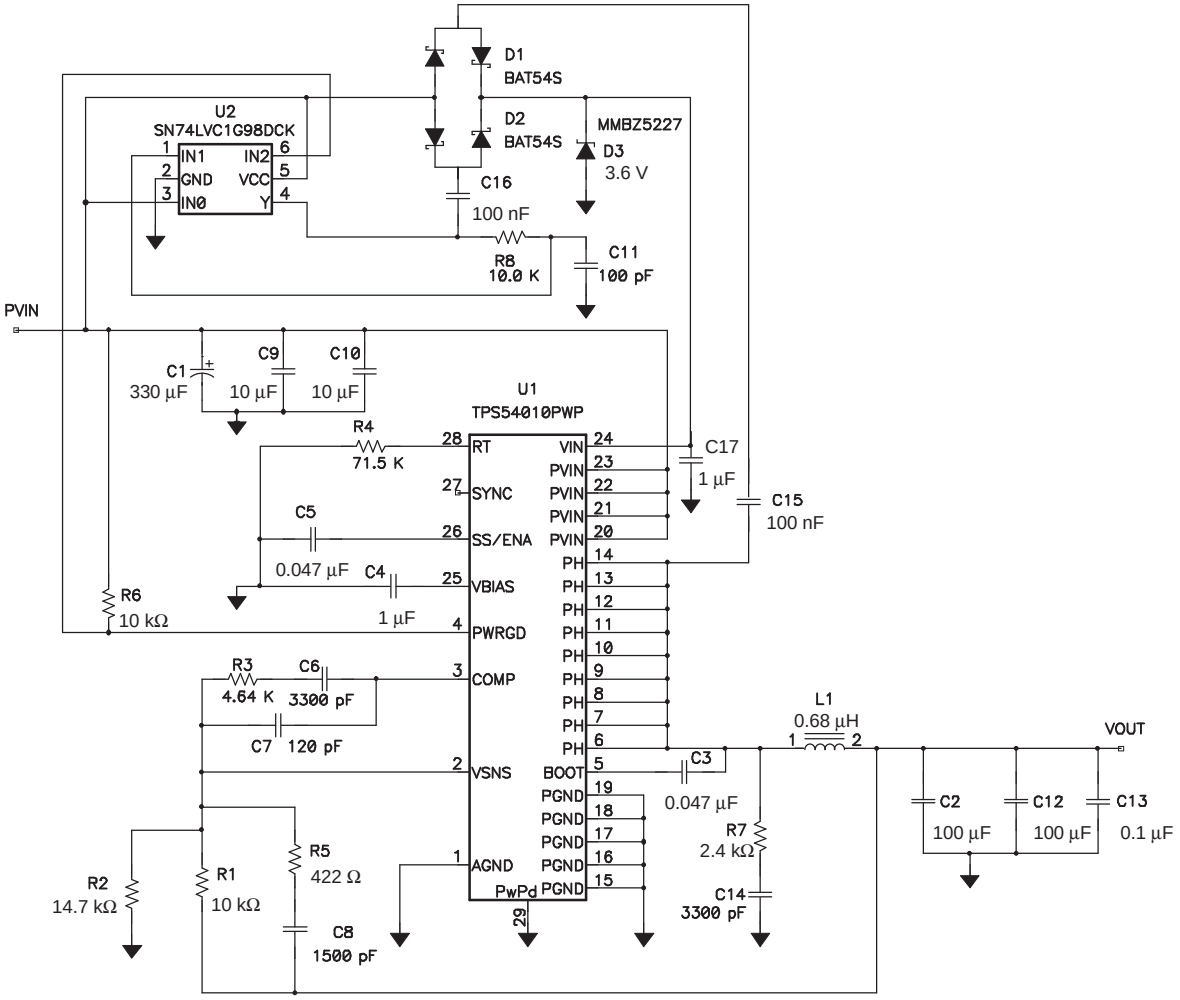


Figure 15. 2.5 V to 1.5 V Power Supply with Charge Pump

If a suitable 3-V to 4-V source is not available for the VIN supply, a charge pump may be used to boost the PVIN voltage. In this circuit, the charge pump is used to boost a 2.5-V source to a nominal 3.6 V.

PERFORMANCE GRAPHS

The performance data for Figure 16 through Figure 24 are for the circuit in Figure 12. Conditions are PVIN = 2.5 V, VIN = 3.3 V, V_O = 1.5 V, f_s = 700 kHz, and I_O = 7 A, T_A = 25°C, unless otherwise specified.

MEASURED LOOP RESPONSE VS FREQUENCY

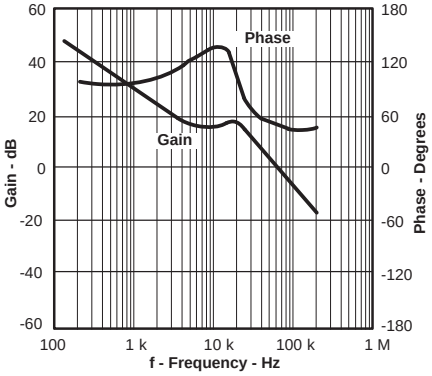


Figure 16.

LOAD REGULATION VS OUTPUT CURRENT

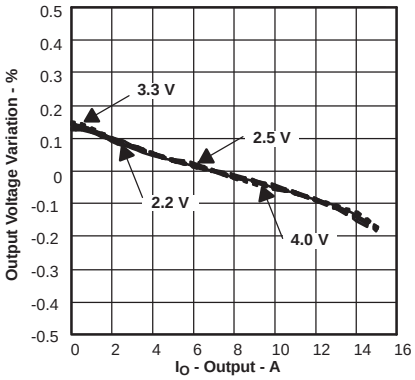


Figure 17.

LINE REGULATION VS INPUT VOLTAGE

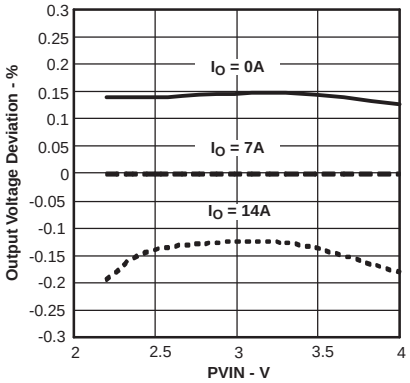


Figure 18.

EFFICIENCY VS OUTPUT CURRENT

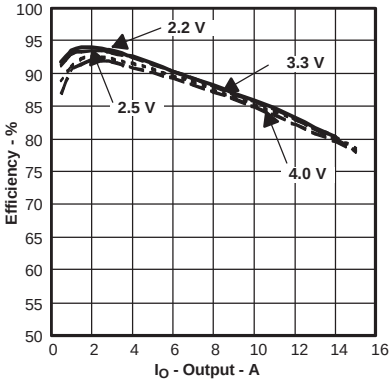


Figure 19.

INPUT RIPPLE VOLTAGE

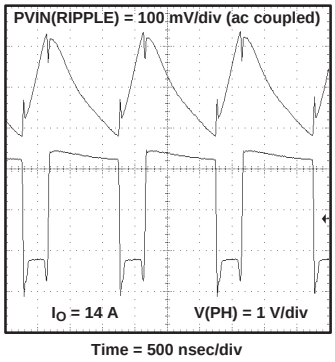


Figure 20.

OUTPUT VOLTAGE RIPPLE

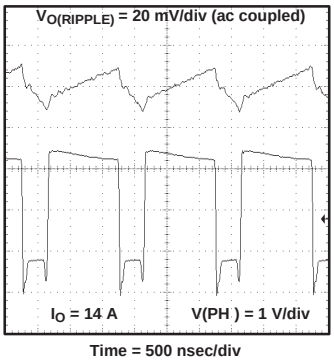


Figure 21.

LOAD TRANSIENT RESPONSE

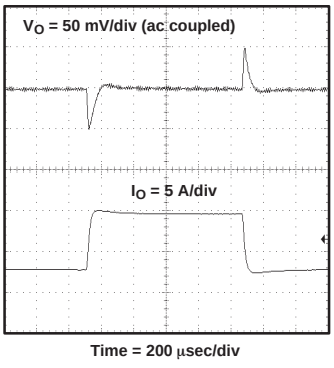


Figure 22.

START-UP WAVEFORM OUTPUT VOLTAGE RELATIVE TO ENABLE

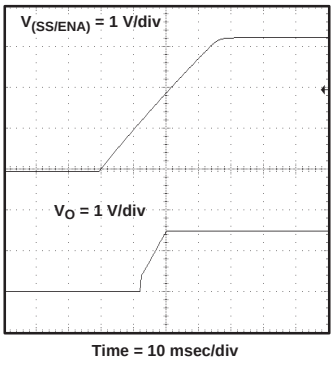


Figure 23.

START-UP WAVEFORM OUTPUT VOLTAGE RELATIVE TO VIN

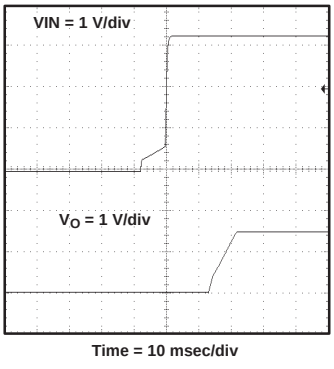
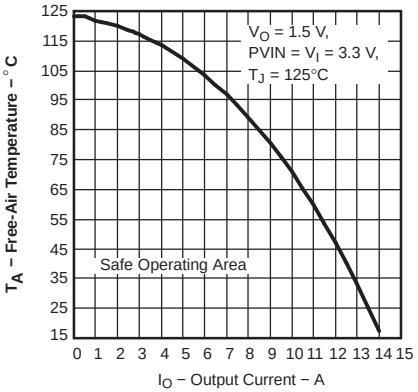


Figure 24.

PERFORMANCE GRAPHS

The performance data for Figure 25 through Figure 34 are for the circuit in Figure 13. Conditions are PVIN = 2.5 V, VIN = 3.3 V, V_O = 1.5 V, f_s = 700 kHz, and I_O = 7 A, T_A = 25°C, unless otherwise specified.

FREE-AIR TEMPERATURE VS MAXIMUM OUTPUT CURRENT



Note: Figure 25 applies to the application circuit (Figure 13) installed on a 3 inch x 3 inch x 0.062 inch four-layer PCB.

Figure 25.

MEASURED LOOP RESPONSE VS FREQUENCY

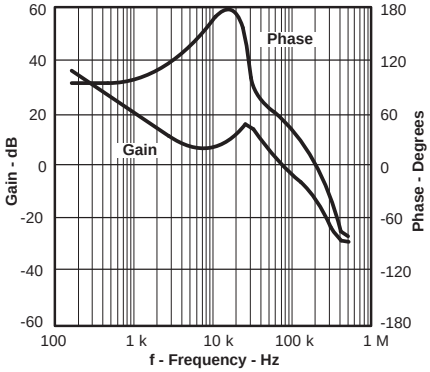


Figure 26.

LOAD REGULATION VS OUTPUT CURRENT

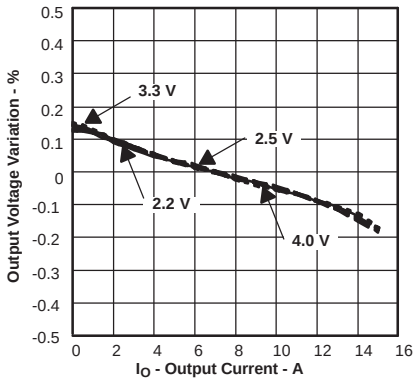


Figure 27.

LINE REGULATION VS PVIN

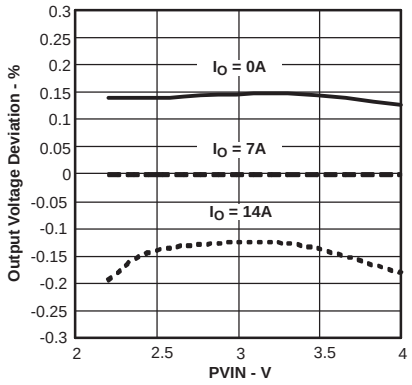


Figure 28.

EFFICIENCY VS OUTPUT CURRENT

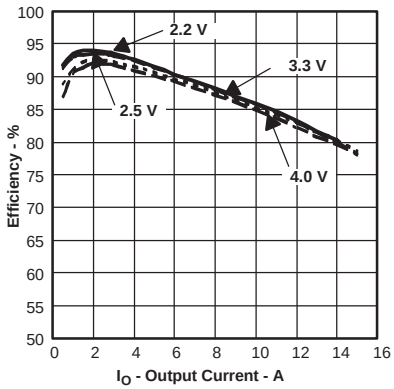


Figure 29.

INPUT RIPPLE VOLTAGE

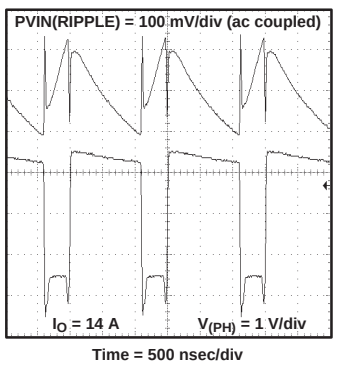


Figure 30.

PERFORMANCE GRAPHS (continued)

OUTPUT VOLTAGE RIPPLE

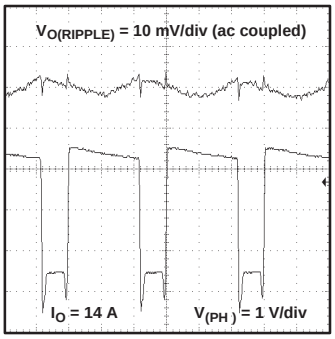


Figure 31.

LOAD TRANSIENT RESPONSE

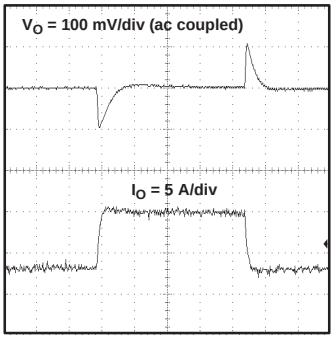


Figure 32.

START-UP WAVEFORM OUTPUT VOLTAGE RELATIVE TO ENABLE

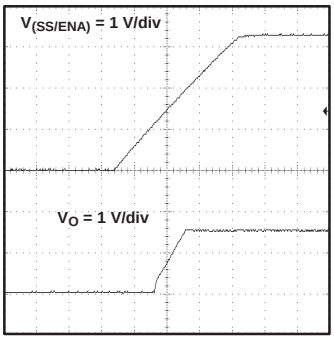


Figure 33.

START-UP WAVEFORM OUTPUT VOLTAGE RELATIVE TO ENABLE

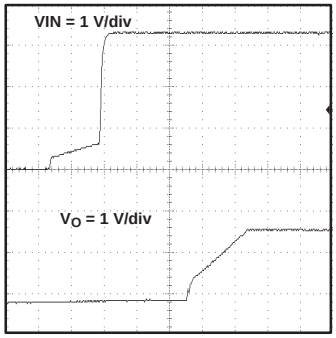


Figure 34.

DETAILED DESCRIPTION

OPERATING WITH SEPARATE PVIN

The TPS54010 is designed to operate with the power stage (high-side and low-side MOSFETs) and the PVIN input connected to a separate power source from VIN. The primary intended application has VIN connected to a 3.3-V bus and PVIN connected to a 2.5-V bus. The TPS54010 cannot be damaged by any sequencing of these voltages. However, the UVLO (see detailed description section) is referenced to the VIN input. Some conditions may cause undesirable operation.

If PVIN is absent when the VIN input is high, the slow-start is released, and the PWM circuit goes to maximum duty factor. When the PVIN input ramps up, the output of the TPS54010 follows the PVIN input until enough voltage is present to regulate to the proper output value.

NOTE

If the PVIN input is controlled via a fast bus switch, it results in a hard-start condition and may damage the load (i.e., whatever is connected to the regulated output of the TPS54010). If a power-good signal is not available from the 2.5-V power supply, one can be generated using a comparator and hold the SS/ENA pin low until the 2.5-V bus power is good. An example of this is shown in Figure 35. This circuit can also be used to prevent the TPS54010 output from following the PVIN input while the PVIN power supply is ramping up.

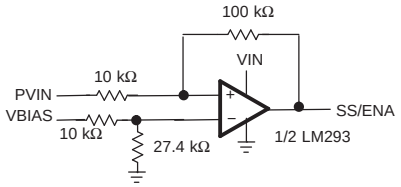


Figure 35. Undervoltage Lockout Circuit for PVIN Using Open-Collector or Open-Drain Comparator

PVIN and VIN can be tied together for 3.3-V bus operation.

MAXIMUM OUTPUT VOLTAGE

The maximum attainable output voltage is limited by the minimum voltage at the PVIN pin. Nominal maximum duty cycle is limited to 90% in the TPS54010; so, maximum output voltage is:

$$V_{O(max)} = PVIN_{(min)} \times 0.9 \quad (24)$$

Care must be taken while operating when nominal conditions cause duty cycles near 90%. Load transients can require momentary increases in duty cycle. If the required duty cycle exceeds 90%, the output may fall out of regulation.

GROUNDING AND PowerPAD LAYOUT

The TPS54010 has two internal grounds (analog and power). Inside the TPS54010, the analog ground ties to all of the noise-sensitive signals, whereas the power ground ties to the noisier power signals. The PowerPAD must be tied directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54010, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground planes are recommended. These two planes must tie together directly at the IC to reduce noise between the two grounds. The only components that must tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54010.

UNDERVOLTAGE LOCKOUT (UVLO)

The TPS54010 incorporates an undervoltage-lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-ms rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN. UVLO is with respect to VIN and not PVIN, see the *Application Information* section.

SLOW-START/ENABLE (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-ms falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \quad (25)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \quad (26)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high-quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.7 V, and external loads on VBIAS with ac or digital-switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits. VBIAS is derived from the VIN pin; see the functional block diagram of this data sheet.

VOLTAGE REFERENCE

The voltage reference system produces a precise V_{ref} signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high-precision regulation of the TPS54010, because it cancels offset errors in the scale and error amplifier circuits.

OSCILLATOR AND PWM RAMP

The oscillator frequency is set to an internally fixed value of 350 kHz. The oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin to ground. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ k\Omega}{R} \times 500\ [kHz] \quad (27)$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 700 kHz by driving a synchronization signal into SYNC and connecting a resistor from RT to AGND. Choose a resistor between the RT and AGND which sets the free running frequency to 80% of the synchronization signal. The following table summarizes the frequency selection configurations:

SWITCHING FREQUENCY	SYNC PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	≥ 2.5 V	Float
Externally set 280 kHz to 700 kHz	Float	R = 180 kΩ to 68 kΩ
Externally synchronized frequency	Synchronization signal	R = RT value for 80% of external synchronization frequency

ERROR AMPLIFIER

The high-performance, wide bandwidth, voltage error amplifier sets the TPS54010 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type-2 or Type-3 compensation can be employed using external compensation components.

PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control-logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp. During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54010 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turn-on times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, whereas the high-side driver is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

OVERCURRENT PROTECTION

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading-edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the slow-start circuit, heating up due to the fault condition, and then shutting down on reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

POWER-GOOD (PWRGD)

The power-good circuit monitors for undervoltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low. When VIN, UVLO threshold, SS/ENA, enable threshold, and VSENSE > 90% of Vref, the open-drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35-µs falling-edge deglitch circuit prevent tripping of the power-good comparator due to high-frequency noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54010MPWPEP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	TPS54010M	Samples
TPS54010MPWPREP	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	TPS54010M	Samples
V62/13604-01XE	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	TPS54010M	Samples
V62/13604-01XE-T	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	TPS54010M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

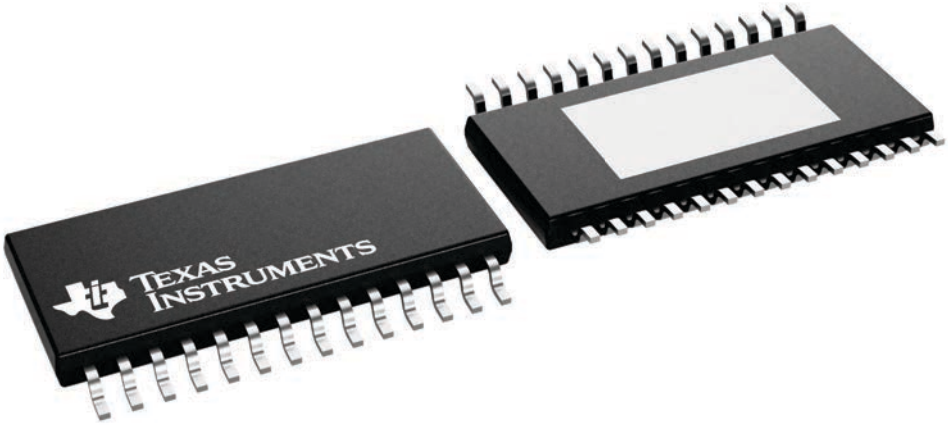
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

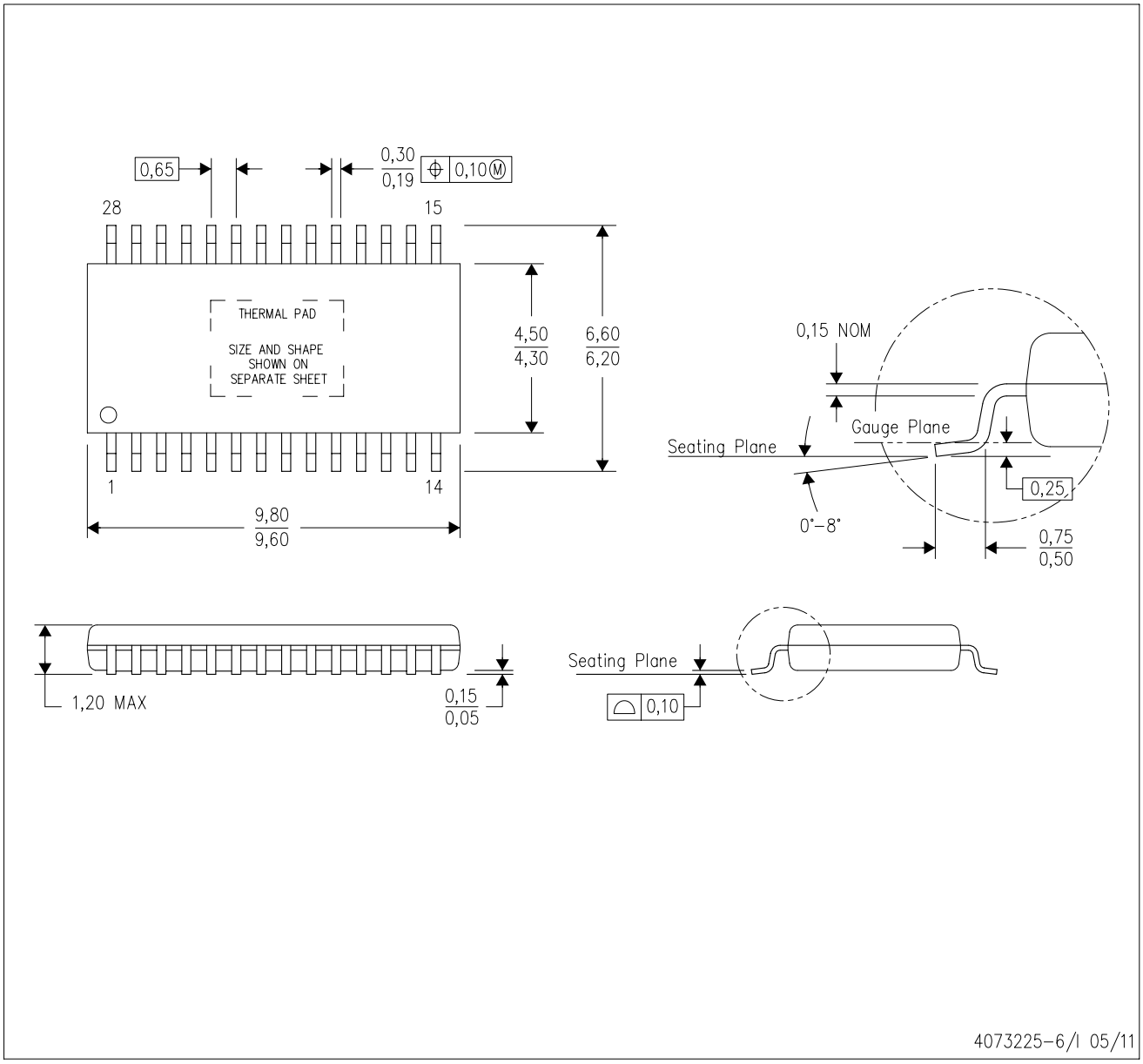
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

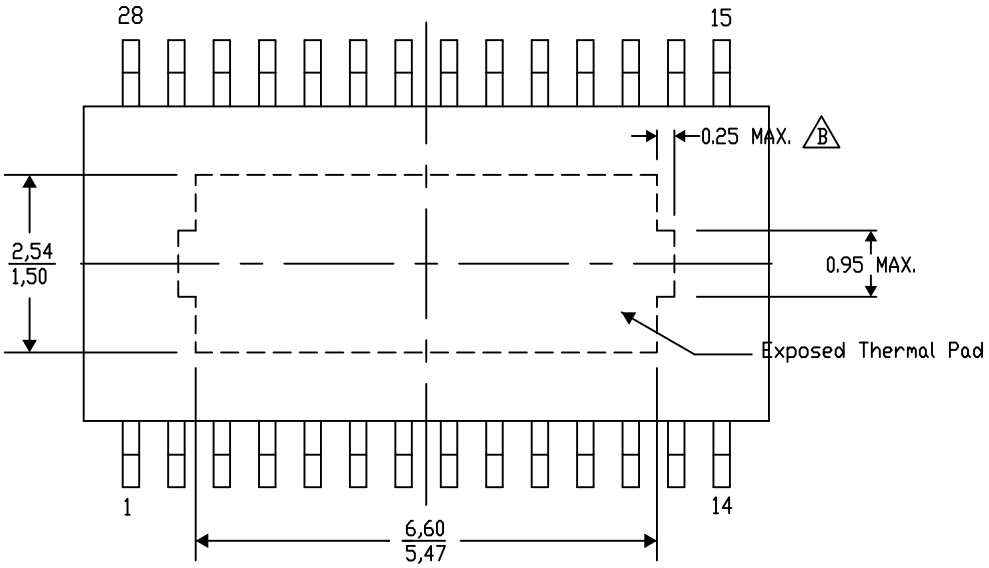
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–40/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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