TEXAS INSTRUMENTS

DAC11001A, DAC91001, DAC81001

ZHCSKD4A –OCTOBER 2019–REVISED DECEMBER 2019

DACx1001 20 位、18 位和 16 位的低噪声、超低谐波失真、快速趋稳、高电压输出数模转换器 (DAC)

1 特性

- 20 位单调性：1-LSB DNL（最大值）
- 积分线性：4-LSB INL（最大值）
- 低噪声：7nV/√Hz
- 独立于代码的低干扰：1nV-s
- 出色的 THD：1kHz f_{OUT} 时为 -105 dB
- 快速趋稳：1μs
- 灵活的输出范围：V_{REFPF} 至 V_{REFNF}
- 集成式精密反馈电阻器
- 50MHz、4 线 SPI 兼容接口
  - 读回
  - 菊花链
- 温度范围：-40°C 至 +125°C
- 封装：48 引脚 TQFP

2 应用

- 实验室和现场仪表
- 光谱仪
- 模拟输出模块
- 电池测试
- 半导体测试
- 任意波形发生器 (AWG)
- MRI
- X 射线系统
- 专业音频放大器（机架式）

3 说明

20 位 DAC11001A、18 位 DAC91001 和 16 位 DAC81001 (DACx1001) 是高精度、低噪声、电压输出、单通道数模转换器 (DAC)。DACx1001 根据设计具有单调性，可以在所有范围内提供低于 4LSB（最大值）的出色线性度。

非缓冲电压输出可提供低噪声性能 (7nV/√Hz) 和快速稳定时间 (1μs)，因此这款器件非常适合低噪声、快速控制环路和波形生成 应用中的数字输入 D 类音频放大器。DACx1001 兼具增强型抗尖峰脉冲电路以及独立于代码的超低干扰 (1nV-s)，可实现干净的波形斜升和超低总谐波失真 (THD)。

DACx1001 器件包含上电复位电路，因此 DAC 能够使用寄存器中的已知值供电。使用外部基准，可以实现 V_{REFPF} 到 V_{REFNF} 的 DAC 输出，包括非对称输出范围。

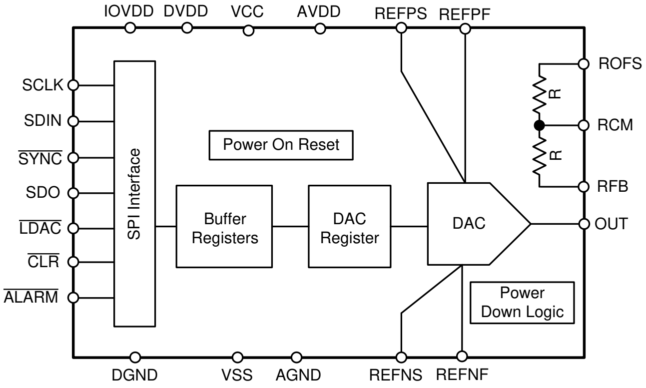
DACx1001 使用一个在高达 50MHz 的时钟频率下运行的通用 4 线串行接口。DACx1001 的额定工业工作温度范围为 -40°C 至 +125°C。

器件信息(1)

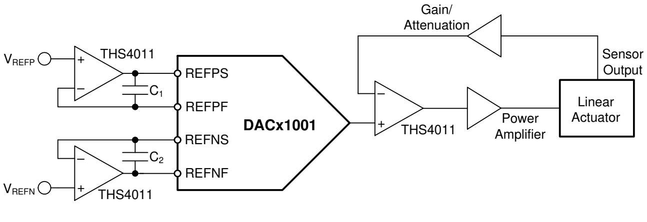
器件型号	封装	封装尺寸（标称值）
DAC11001	TQFP (48)	7.00mm × 7.00mm
DAC91001（预发布）		
DAC81001（预发布）		

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

功能方框图



高精度控制环路电路



English Data Sheet: SLASEL0

目录

4 修订历史记录

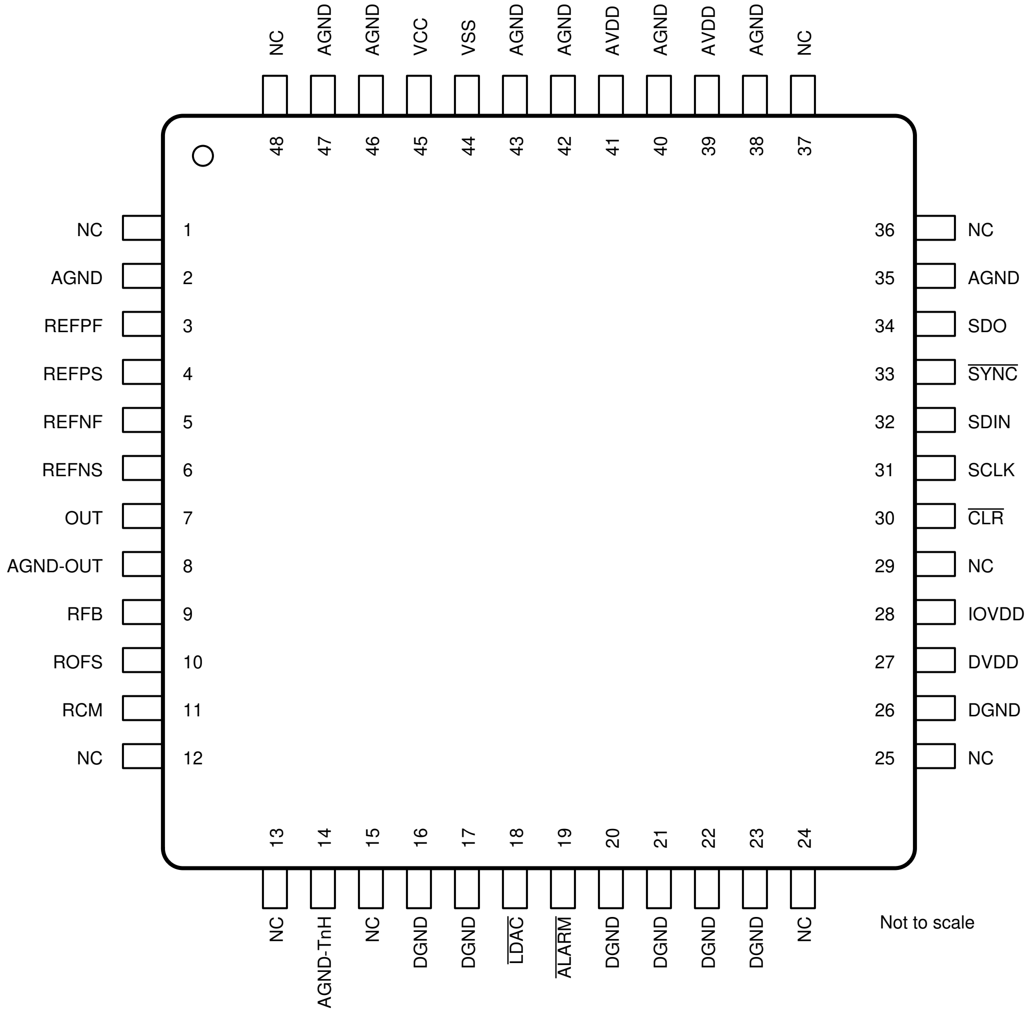
Changes from Original (October 2019) to Revision A	**Page**
• 已更改 将 DAC11001A 器件从“预告信息（预发布）”更改为“生产数据（正在供货）”	1

5 Device Comparison Table

DEVICE	RESOLUTION
DAC11001A	20-bit
DAC91001 (preview)	18-bit
DAC81001 (preview)	16-bit

6 Pin Configuration and Functions

PFB Package
48-Pin TQFP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	2, 35, 38, 40, 42, 43, 46, 47	Analog ground	Connect to 0 V.
AGND-OUT	8	Analog ground	Connect to 0 V. Measure DAC output voltage with respect to this node.
AGND-TnH	14	Analog ground	Connect to 0 V. Integrated deglitcher clock ground..
$\overline{\text{ALARM}}$	19	Output	Alarm output
AVDD	39, 41	Power	Positive low voltage analog power supply
$\overline{\text{CLR}}$	30	Input	DAC registers clear pin, active low
DGND	16, 17, 20, 21, 22, 23, 26	Digital ground	Connect to 0 V.
DVDD	27	Power	Digital power supply pin
RFB	9	Input	Integrated precision resistor feedback node
IOVDD	28	Power	Interface power supply pin
$\overline{\text{LDAC}}$	18	Input	Load DAC pin, active low
NC	1, 12, 13, 15, 24, 25, 29, 36, 37, 48	—	No connection, leave floating
OUT	7	Output	Unbuffered voltage output
RCM	11	Input	Integrated precision resistor common-mode node
REFNF	5	Input	External negative reference input. Connect to 0 V for unipolar DAC output.
REFNS	6	Input	External negative reference sense node
REFPF	3	Input	External positive reference input
REFPS	4	Input	External positive reference sense node
ROFS	10	Input	Integrated precision resistor offset node
SCLK	31	Input	Serial clock input of serial peripheral interface (SPI). Schmitt-trigger logic input. Data are transferred at rates of up to 50 MHz.
SDIN	32	Input	Serial data input. Schmitt-trigger logic input. Data are clocked into the input shift register on the falling edge of the serial clock input.
SDO	34	Output	Serial data output. Data are valid on the falling edge of SCLK.
$\overline{\text{SYNC}}$	33	Input	SPI bus chip select input (active low). Data bits are not clocked into the serial shift register unless $\overline{\text{SYNC}}$ is low. When $\overline{\text{SYNC}}$ is high, the SDO pin is in high-impedance status.
VCC	45	Power	Analog positive power supply
VSS	44	Power	Analog negative power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Positive supply voltage	AV_{DD} to AGND	–0.3	7	V
		V_{CC} to V_{SS}	–0.3	40	
		V_{CC} to AGND	–0.3	40	
	Negative supply voltage	V_{SS} to AGND	–19	0.3	V
	Positive reference voltage	V_{REFPF} to V_{REFNF}	–0.3	40	V
		V_{REFPF} to V_{CC}	–0.3	V_{CC} + 0.3	
		V_{REFPF} to AGND	–0.3	40	
	Negative reference voltage	V_{REFNF} to AGND	–19	0.3	V
		V_{REFNF} to V_{SS}	V_{SS} – 0.3	0.3	
	Digital and IO power supply	DV_{DD}, IOV_{DD} to DGND	–0.3	7	V
	Digital input(s) to DGND		DGND – 0.3	IOV_{DD} + 0.3	V
	V_{OUT}, V_{RFB}, V_{RCM}, V_{ROFS}	to AGND (V_{SS} = AGND)	V_{SS}	V_{CC}	V
		to V_{SS}	0	V_{CC}	
	Alarm pin voltage, $\overline{\text{ALARM}}$ to DGND		–0.3	DV_{DD} + 0.3	V
	Digital output, SDO to DGND		–0.3	DV_{DD} + 0.3	V
	Current into any pin		–10	10	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	AV_{DD} to AGND	4.5		5.5	V
	V_{SS} to AGND	–18		–3	V
	V_{CC} to AGND	8		33	V
	V_{CC} to V_{SS}	11		36	V
	DV_{DD} to DGND	2.7		5.5	V
	IOV_{DD} to DGND	1.7		5.5	V
	AGND to DGND	–0.3		0.3	V
	V_{IH} digital input high voltage	0.7 × IOV_{DD}			V
	V_{IL} digital input low voltage			0.3 × IOV_{DD}	V
	V_{REFPF} to AGND	3		15	V
	V_{REFNF} to AGND	–15		0	V
	V_{REFPF} to V_{REFNF}	3		30	V
T_A	Operating temperature	–40		125	°C

7.4 Thermal Information Package

THERMAL METRIC[1]		DAC11001A, DAC91001, DAC81001	UNIT
		PFB (TQFP)	
		48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = –40°C to +125°C, V_{CC} = +15 V, V_{SS} = –15 V, AV_{DD} = 5.5 V, DV_{DD} = 3.3 V, IOV_{DD} = 1.8 V, see note(1) for V_{REFPF} and V_{REFNF}, 20-bit orderable used, OUT pin buffered with unity gain OPA827, ROFS, RCM, RFB unconnected, and all typical specifications at T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	DAC11001A	20			Bits
		DAC91001	18			
		DAC81001	16			
INL	Relative accuracy(2)		–4		4	LSB
	Relative accuracy(2)(3)(4)		–2.6		2.6	
	Relative accuracy(2)(4)	DACx1001A T_A = 25°C	–2		2	
	Relative accuracy drift over time(2)	T_A = 25°C, 1000 hrs		0.1		LSB
DNL	Differential nonlinearity(2)(3)		–1		1	LSB
	Zero code error(4)	T_A = 0°C to 70°C, code 0d into DAC, unipolar ranges only	–4		4	LSB
		T_A = –40°C to +125°C, code 0d into DAC, unipolar ranges only	–4		4	
		T_A = 25°C, unipolar ranges only		±2		
	Zero code error temperature coefficient	T_A = 0°C to 70°C, code 0d into DAC, unipolar ranges only		±0.04		ppm FSR/°C
		T_A = –40°C to +125°C, code 0d into DAC, unipolar ranges only		±0.04		
	Gain error(2)(4)	T_A = 0°C to 70°C	–8		8	ppm of FSR
		T_A = 0°C to 70°C, V_{REFPF} = 3 V, V_{REFNF} = –10 V	–8		8	
		T_A = –40°C to +125°C	–10		10	
		T_A = 25°C		±2		
	Gain error temperature coefficient	T_A = 0°C to 70°C		±0.04		ppm FSR/°C
		T_A = 0°C to 70°C, V_{REFPF} = 3 V, V_{REFNF} = –10 V		±0.04		
		T_A = –40°C to +125°C		±0.04		
	Positive full-scale error(4)	T_A = 0°C to 70°C, code 1048575d into DAC	–8		8	LSB
		T_A = 0°C to 70°C, code 1048575d into DAC, V_{REFPF} = 3 V, V_{REFNF} = –10 V	–6		6	
		T_A = –40°C to +125°C, code 1048575d into DAC	–10		10	
		T_A = 25°C		±2		
	Full-scale error temperature coefficient	T_A = 0°C to 70°C		±0.04		ppm FSR/°C
		T_A = 0°C to 70°C, V_{REFPF} = 3 V, V_{REFNF} = –10 V		±0.04		
		T_A = –40°C to +125°C		±0.04		
OUTPUT CHARACTERISTICS						
	Headroom	From V_{REFPF} to V_{CC}	3			V
	Footroom	From V_{REFNF} to V_{SS}	3			V
	DC impedance	From ROFS to RCM		5		kΩ
		From RCM to RFB		5		
Z_O	DC output impedance			2.5		kΩ

(1) Specified for the following pairs: V_{REFPF} = 5 V and V_{REFNF} = 0 V; V_{REFPF} = 10 V and V_{REFNF} = 0 V; V_{REFPF} = +5 V and V_{REFNF} = –5 V; V_{REFPF} = +10 V and V_{REFNF} = –10 V.
(2) Calculated between code 0d to 1048575d.
(3) With device temperature calibration mode enabled and used.
(4) Specified by design, not production tested.

Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{CC} = +15 V, V_{SS} = –15 V, AV_{DD} = 5.5 V, DV_{DD} = 3.3 V, IOV_{DD} = 1.8 V, see note(1) for V_{REFPF} and V_{REFNF}, 20-bit orderable used, OUT pin buffered with unity gain OPA827, ROFS, RCM, RFB unconnected, and all typical specifications at T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio (dc)	T_A = 25°C, V_{CC} = 15 V ± 20%, V_{SS} = –15 V		1.5		µV/V
		T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V ± 20%		1		
VOLTAGE REFERENCE INPUT						
	Reference input impedance (REFPF)	DAC at midscale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		5.5		kΩ
	Reference input impedance (REFNF)	DAC at midscale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		7		
DYNAMIC PERFORMANCE						
t_s	Output voltage settling time(5)	V_{REFPF} = 10 V, V_{REFNF} = 0 V, full-scale settling to 0.1%FSR		1		µs
		V_{REFPF} = 10 V, V_{REFNF} = 0 V, full-scale settling to ±1 LSB		2.5		
		V_{REFPF} = 10 V, V_{REFNF} = 0 V, 1-mV step settling to ±1 LSB		2.5		
SR	Slew rate	V_{REFPF} = 10 V, V_{REFNF} = 0 V, full-scale step, measured at OUT pin		50		V/µs
	Power-on glitch magnitude	Measured at unbuffered DAC voltage output, V_{REFPF} = 10 V, V_{REFNF} = 0 V		–0.2		V
V_n	Output noise	0.1-Hz to 10-Hz, DAC at midscale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		0.4		µVpp
		100-kHz bandwidth, DAC at midscale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		3		µVrms
	Output noise density	Measured at 1 kHz, 10 kHz, 100 kHz, DAC at mid scale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		7		$nV/\sqrt{Hz}$
SFDR	Spurious free dynamic range	DAC update rate = 400 kHz, f_{OUT} = 1 kHz, V_{OUTPP} = 0 V to 10 V		–105		dB
		DAC update rate = 400 kHz, f_{OUT} = 1 kHz, V_{OUTPP} = 3 V to –10 V		–105		dB
THD	Total harmonic distortion	DAC update rate = 400 kHz, f_{OUT} = 1 kHz, V_{OUTPP} = 0 V to 10 V		–105		dB
		DAC update rate = 400 kHz, f_{OUT} = 1 kHz, V_{OUTPP} = 3 V to –10 V		–105		dB
	Power supply rejection ratio (ac)	200-mV 50-Hz or 60-Hz sine wave superimposed on $V_{SS,}$ V_{CC} = 15 V		95		dB
		200-mV 50 Hz or 60 Hz sine wave superimposed on $V_{CC,}$ V_{SS} = –15 V		95		dB
	Code change glitch impulse	±1 LSB change around mid code (including feedthrough), V_{REFPF} = 10 V, V_{REFNF} = 0 V, measured at output of buffer op amp		1		nV-s
	Code change glitch impulse magnitude	±1 LSB change around mid code (including feedthrough), V_{REFPF} = 10 V, V_{REFNF} = 0 V, measured at output of buffer op amp		5		mV
	Reference feedthrough	V_{REFPF} = 10 V ± 10%, V_{REFNF} = 0 V, frequency = 100 Hz, DAC at zero scale		–90		dB
	Reference feedthrough	V_{REFNF} = –10 V ± 10%, V_{REFPF} = 10 V, frequency = 100 Hz, DAC at full scale		–90		dB

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(5) Adaptive TnH mode. TnH action is disabled for large code steps. For small steps, TnH action happens with a hold time of 1.2µs.

Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{CC} = +15 V, V_{SS} = –15 V, AV_{DD} = 5.5 V, DV_{DD} = 3.3 V, IOV_{DD} = 1.8 V, see note(1) for V_{REFPF} and V_{REFNF}, 20-bit orderable used, OUT pin buffered with unity gain OPA827, ROFS, RCM, RFB unconnected, and all typical specifications at T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Digital feedthrough	At SCLK = 1 MHz, DAC output static at midscale, 10-V range		1		nV-s
DIGITAL INPUTS						
	Hysteresis voltage			0.4		V
	Input current			±5		µA
	Pin capacitance	Per pin		10		pF
DIGITAL OUTPUTS						
V_{OL}	Output low voltage	sinking 200 µA			0.4	V
V_{OH}	Output high voltage	sourcing 200 µA	IOV_{DD} – 0.5			V
	High impedance leakage			±5		µA
	High impedance output capacitance			10		pF
POWER						
I_{AVDD}	Current flowing into AV_{DD}	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code			1.5	mA
I_{VCC}	Current flowing into V_{CC}	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code			7	mA
I_{VSS}	Current flowing into V_{SS}	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code			7	mA
I_{DVDD}	Current flowing into DV_{DD}	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code		0.5		mA
I_{IOVDD}	Current flowing into IOV_{DD}	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code, all digital input pins static at IOV_{DD}		0.1		mA
I_{REFPF}	Reference input current (V_{REFPF})	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code			5	mA
I_{REFNF}	Reference input current (V_{REFNF})	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code			5	mA

7.6 Timing Requirements: Write, 4.5 V ≤ DV_{DD} ≤ 5.5 V

all input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20 pF, and T_A = –40°C to +125°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency, 1.7 V ≤ IOV_{DD} < 2.7 V			33	MHz
	SCLK frequency, 2.7 V ≤ IOV_{DD} ≤ 5.5 V			50	
$t_{SCLKHIGH}$	SCLK high time, 1.7 V ≤ IOV_{DD} < 2.7 V	15			ns
	SCLK high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	10			
$t_{SCLKLOW}$	SCLK low time, 1.7 V ≤ IOV_{DD} < 2.7 V	15			ns
	SCLK low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	10			
t_{SDIS}	SDI setup, 1.7 V ≤ IOV_{DD} < 2.7 V	13			ns
	SDI setup, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	8			
t_{SDIH}	SDI hold, 1.7 V ≤ IOV_{DD} < 2.7 V	13			ns
	SDI hold, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	8			
t_{CSS}	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V	23			ns
	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	18			
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge, 1.7 V ≤ IOV_{DD} < 2.7 V	15			ns
	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	10			
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time, 1.7 V ≤ IOV_{DD} < 2.7 V	55			ns
	$\overline{\text{SYNC}}$ high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	50			
$t_{CSIGNORE}$	SCLK falling edge to $\overline{\text{SYNC}}$ ignore, 1.7 V ≤ IOV_{DD} < 2.7 V	10			ns
	SCLK falling edge to $\overline{\text{SYNC}}$ ignore, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	5			
t_{LDACSL}	Synchronous update: $\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V	50			ns
	Synchronous update: $\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	50			
t_{LDACW}	$\overline{\text{LDAC}}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V	20			ns
	$\overline{\text{LDAC}}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			
t_{CLRW}	$\overline{\text{CLR}}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V	20			ns
	$\overline{\text{CLR}}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			

7.7 Timing Requirements: Write, 2.7 V ≤ DV_{DD} < 4.5 V

all input signals are specified with t_R = t_F = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20 pF, and T_A = –40°C to +125°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency, 1.7 V ≤ IOV_{DD} < 2.7 V			20	MHz
	SCLK frequency, 2.7 V ≤ IOV_{DD} ≤ 5.5 V			25	
$t_{SCLKHIGH}$	SCLK high time, 1.7 V ≤ IOV_{DD} < 2.7 V	25			ns
	SCLK high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			
$t_{SCLKLOW}$	SCLK low time, 1.7 V ≤ IOV_{DD} < 2.7 V	25			ns
	SCLK low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			
t_{SDIS}	SDI setup, 1.7 V ≤ IOV_{DD} < 2.7 V	21			ns
	SDI setup, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	16			
t_{SDIH}	SDI hold, 1.7 V ≤ IOV_{DD} < 2.7 V	21			ns
	SDI hold, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	16			
t_{CSS}	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V	41			ns
	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	36			
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge, 1.7 V ≤ IOV_{DD} < 2.7 V	25			ns
	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time, 1.7 V ≤ IOV_{DD} < 2.7 V	100			ns
	$\overline{\text{SYNC}}$ high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	100			
$t_{CSIGNORE}$	SCLK falling edge to $\overline{\text{SYNC}}$ ignore, 1.7 V ≤ IOV_{DD} < 2.7 V	10			ns
	SCLK falling edge to $\overline{\text{SYNC}}$ ignore, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	5			
t_{LDACSL}	Synchronous update: $\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V	100			ns
	Synchronous update: $\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	100			
t_{LDACW}	$\overline{\text{LDAC}}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V	40			ns
	$\overline{\text{LDAC}}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	40			
t_{CLRW}	$\overline{\text{CLR}}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V	40			ns
	$\overline{\text{CLR}}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	40			

7.8 Timing Requirements: Read and Daisy-Chain Write, 4.5 V ≤ DV$_{DD}$ ≤ 5.5 V

all input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV$_{DD}$) and timed from a voltage level of ($V_{IL} + V_{IH}$) / 2, SDO loaded with 20 pF, and T_A = –40°C to +125°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency	1.7 V ≤ IOV$_{DD}$ < 2.7 V, FSDO = 0			10	MHz
		1.7 V ≤ IOV$_{DD}$ < 2.7 V, FSDO = 1			20	
		2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V, FSDO = 0			15	
		2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V, FSDO = 1			30	
$t_{SCLKHIGH}$	SCLK high time	1.7 V ≤ IOV$_{DD}$ < 2.7 V, FSDO = 0	50			ns
		1.7 V ≤ IOV$_{DD}$ < 2.7 V, FSDO = 1	25			
		2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V, FSDO = 0	33			
		2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V, FSDO = 1	16			
$t_{SCLKLOW}$	SCLK low time	1.7 V ≤ IOV$_{DD}$ < 2.7 V, FSDO = 0	50			ns
		1.7 V ≤ IOV$_{DD}$ < 2.7 V, FSDO = 1	25			
		2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V, FSDO = 0	33			
		2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V, FSDO = 1	16			
t_{SDIS}	SDI setup, 1.7 V ≤ IOV$_{DD}$ < 2.7 V		13			ns
	SDI setup, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V		8			
t_{SDIH}	SDI hold, 1.7 V ≤ IOV$_{DD}$ < 2.7 V		13			ns
	SDI hold, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V		8			
t_{CSS}	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge, 1.7 V ≤ IOV$_{DD}$ < 2.7 V		30			ns
	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V		20			
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge, 1.7 V ≤ IOV$_{DD}$ < 2.7 V		15			ns
	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V		10			
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time, 1.7 V ≤ IOV$_{DD}$ < 2.7 V		55			ns
	$\overline{\text{SYNC}}$ high time, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V		50			
$t_{CSIGNORE}$	SCLK falling edge to $\overline{\text{SYNC}}$ ignore, 1.7 V ≤ IOV$_{DD}$ < 2.7 V		10			ns
	SCLK falling edge to $\overline{\text{SYNC}}$ ignore, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V		5			
t_{LDACSL}	Synchronous update: $\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge, 1.7 V ≤ IOV$_{DD}$ < 2.7 V		50			ns
	Synchronous update: $\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V		50			
t_{LDACW}	$\overline{\text{LDAC}}$ low time, 1.7 V ≤ IOV$_{DD}$ < 2.7 V		20			ns
	$\overline{\text{LDAC}}$ low time, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V		20			
t_{CLRW}	$\overline{\text{CLR}}$ low time, 1.7 V ≤ IOV$_{DD}$ < 2.7 V		20			ns
	$\overline{\text{CLR}}$ low time, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V		20			
t_{SDODLY}	SCLK rising edge to SDO valid data, 1.7 V ≤ IOV$_{DD}$ < 2.7 V, FSDO = 0		0		35	ns
	SCLK rising edge to SDO valid data, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V, FSDO = 0		0		25	
	SCLK falling edge to SDO valid data, 1.7 V ≤ IOV$_{DD}$ < 2.7 V, FSDO = 1		0		35	
	SCLK falling edge to SDO valid data, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V, FSDO = 1		0		25	
t_{SDOZ}	$\overline{\text{SYNC}}$ rising edge to SDO HiZ, 1.7 V ≤ IOV$_{DD}$ < 2.7 V		0		20	ns
	$\overline{\text{SYNC}}$ rising edge to SDO HiZ, 2.7 V ≤ IOV$_{DD}$ ≤ 5.5 V		0		20	

7.9 Timing Requirements: Read and Daisy-Chain Write, 2.7 V ≤ DV_{DD} < 4.5 V

all input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of ($V_{IL} + V_{IH}$) / 2, SDO loaded with 20 pF, and T_A = –40°C to +125°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency	1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0			8	MHz
		1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1			16	
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0			10	
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1			20	
$t_{SCLKHIGH}$	SCLK high time	1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0	62			ns
		1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1	31			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0	50			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1	25			
$t_{SCLKLOW}$	SCLK low time	1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0	62			ns
		1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1	31			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0	50			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1	25			
t_{SDIS}	SDI setup, 1.7 V ≤ IOV_{DD} < 2.7 V		21			ns
	SDI setup, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		16			
t_{SDIH}	SDI hold, 1.7 V ≤ IOV_{DD} < 2.7 V		21			ns
	SDI hold, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		16			
t_{CSS}	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V		41			ns
	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		36			
t_{CSH}	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge, 1.7 V ≤ IOV_{DD} < 2.7 V		25			ns
	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		20			
t_{CSHIGH}	$\overline{\text{SYNC}}$ high time, 1.7 V ≤ IOV_{DD} < 2.7 V		100			ns
	$\overline{\text{SYNC}}$ high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		100			
$t_{CSIGNORE}$	SCLK falling edge to $\overline{\text{SYNC}}$ ignore, 1.7 V ≤ IOV_{DD} < 2.7 V		10			ns
	SCLK falling edge to $\overline{\text{SYNC}}$ ignore, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		5			
t_{LDACSL}	Synchronous update: $\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V		100			ns
	Synchronous update: $\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		100			
t_{LDACW}	$\overline{\text{LDAC}}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V		40			ns
	$\overline{\text{LDAC}}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		40			
t_{CLRW}	$\overline{\text{CLR}}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V		40			ns
	$\overline{\text{CLR}}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		40			
t_{SDODLY}	SCLK rising edge to SDO valid data, 1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0		0		40	ns
	SCLK rising edge to SDO valid data, 2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0		0		30	
	SCLK rising edge to SDO valid data, 1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1		0		40	
	SCLK rising edge to SDO valid data, 2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1		0		30	
t_{SDOZ}	$\overline{\text{SYNC}}$ rising edge to SDO HiZ, 1.7 V ≤ IOV_{DD} < 2.7 V		0		20	ns
	$\overline{\text{SYNC}}$ rising edge to SDO HiZ, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		0		20	

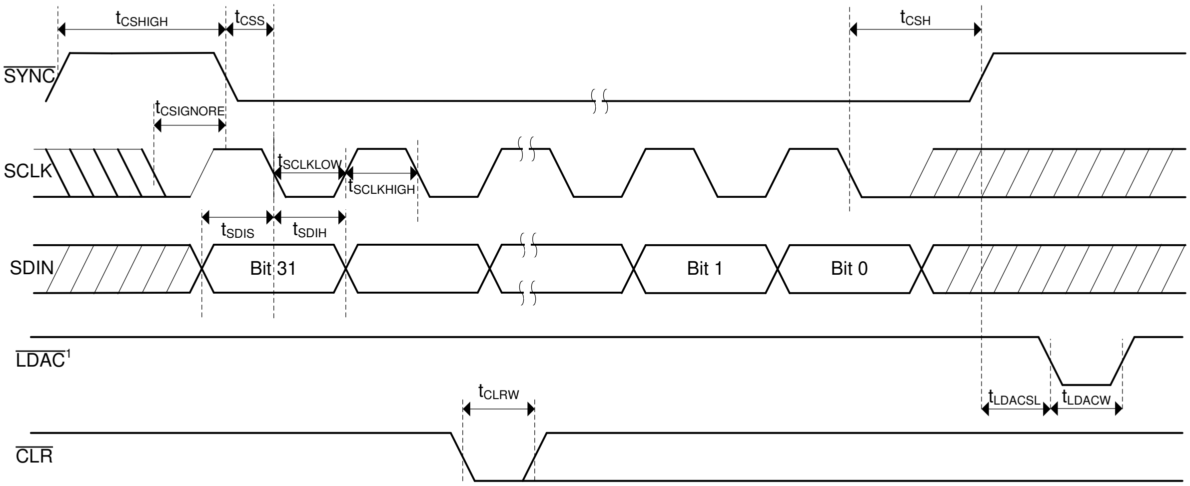


图 1. Serial Interface Write Timing: Standalone Mode

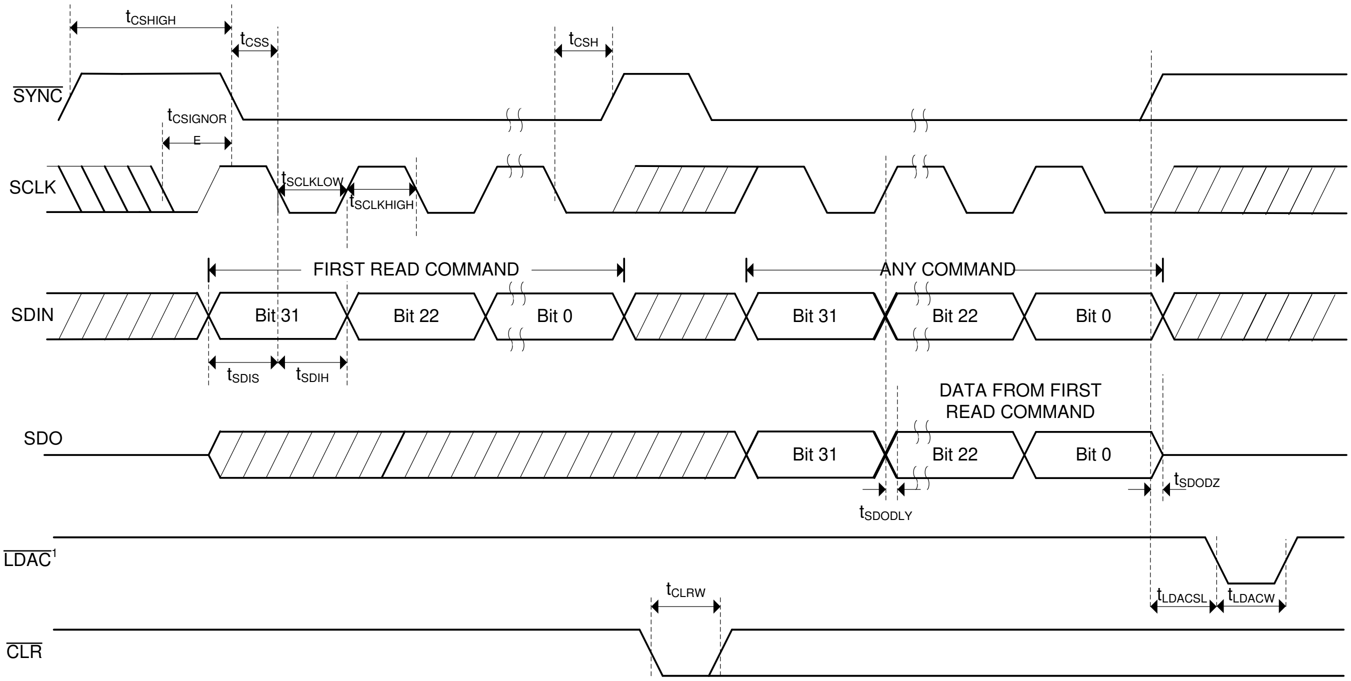


图 2. Serial Interface Read and Write Timing: Daisy-Chain Mode

7.10 Typical Characteristics

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as output and reference amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)

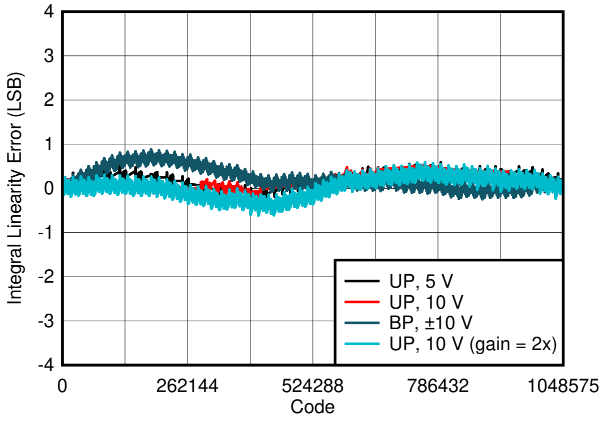


图 3. . Integral Linearity Error vs Digital Input Code

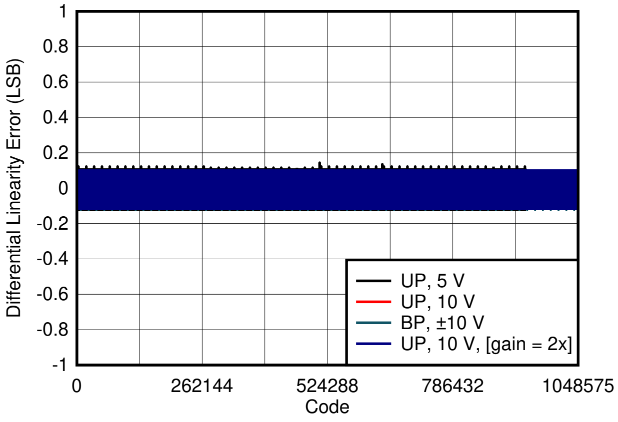


图 4. Differential Linearity Error vs Digital Input Code

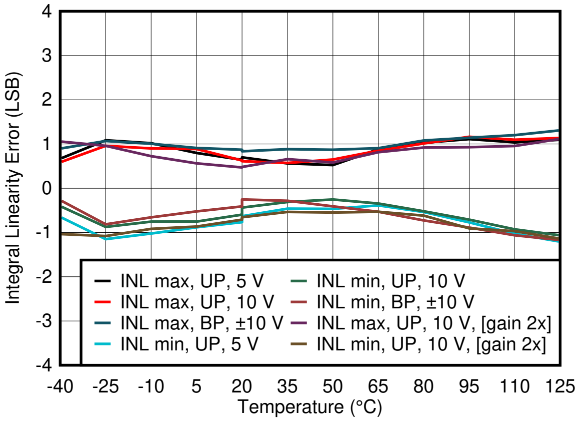
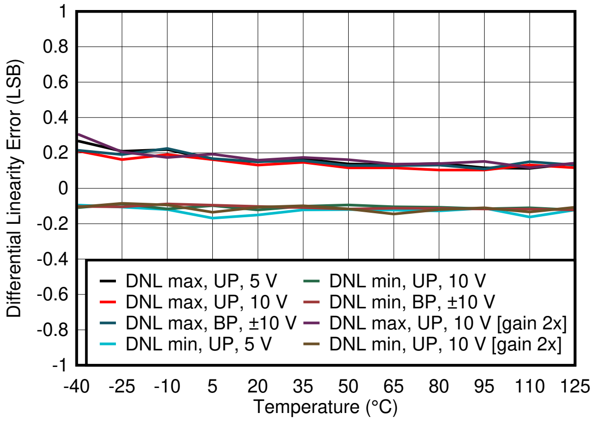
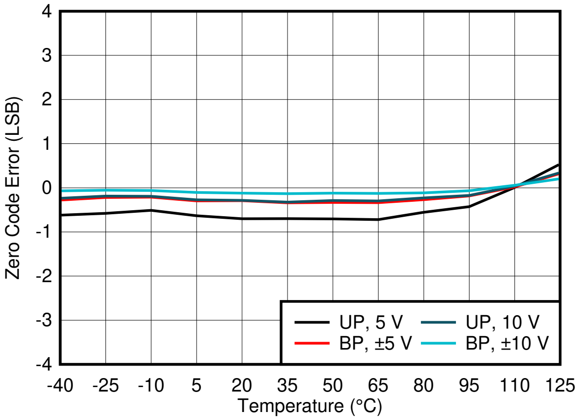


图 5. Integral Linearity Error vs Temperature



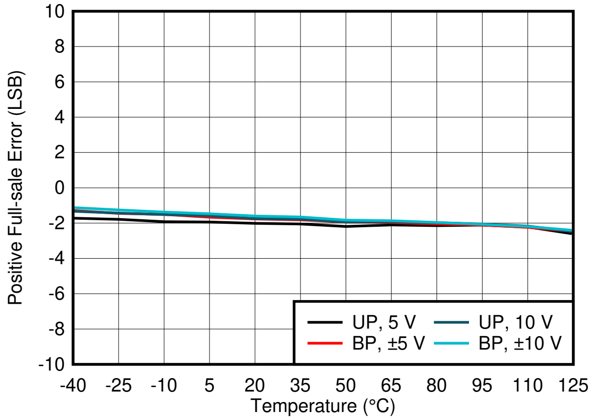
Temperature calibration enabled

图 6. Differential Linearity Error vs Temperature



Temperature calibration enabled

图 7. Zero Code Error vs Temperature

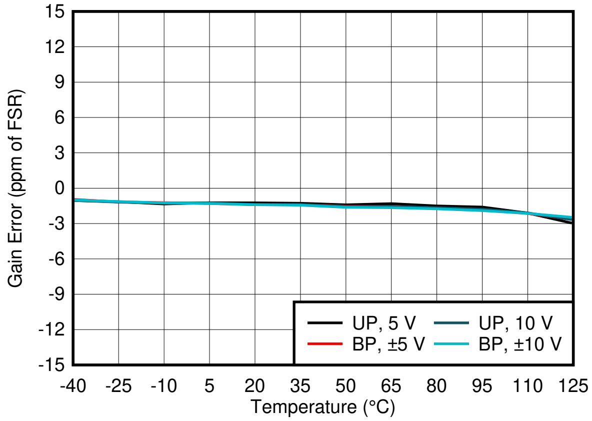


Temperature calibration enabled

图 8. Positive Full-Scale Error vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as output and reference amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



Temperature calibration enabled

图 9. Gain Error vs Temperature

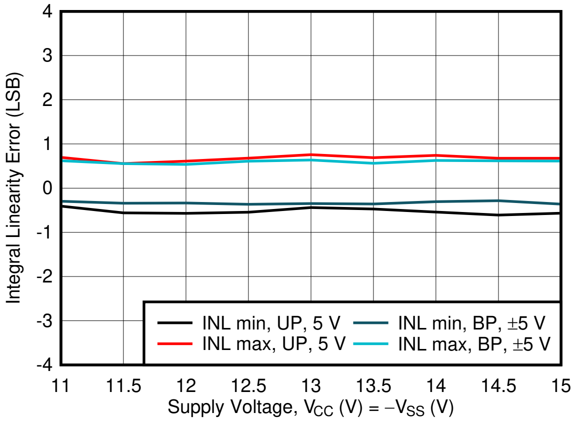


图 10. Integral Linearity Error vs Supply Voltage

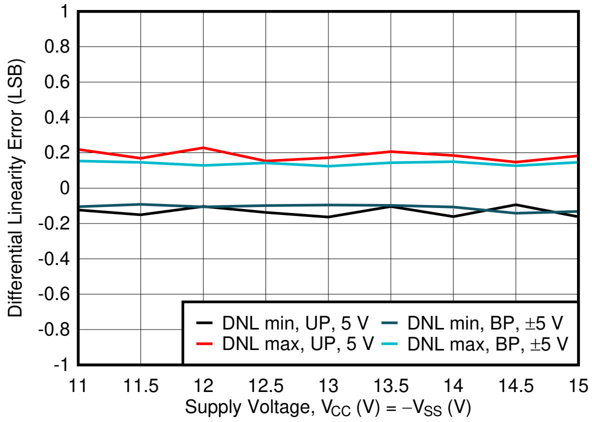


图 11. Differential Linearity Error vs Supply Voltage

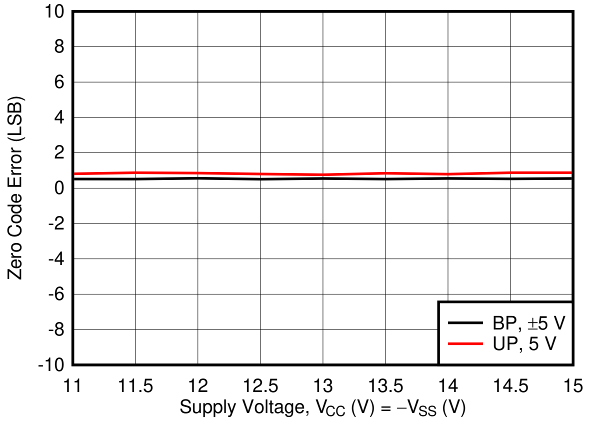


图 12. Zero Code Error vs Supply Voltage

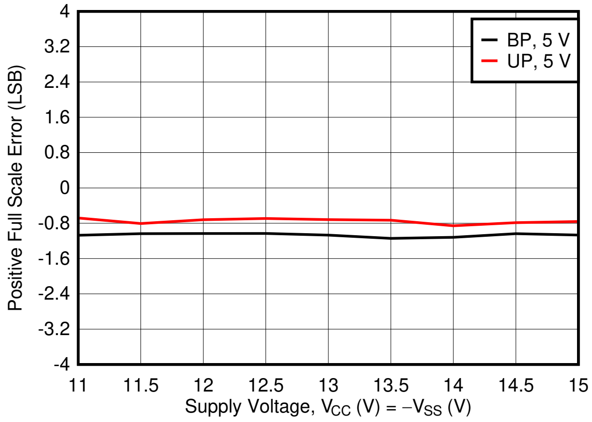


图 13. Positive Full-Scale Error vs Supply Voltage

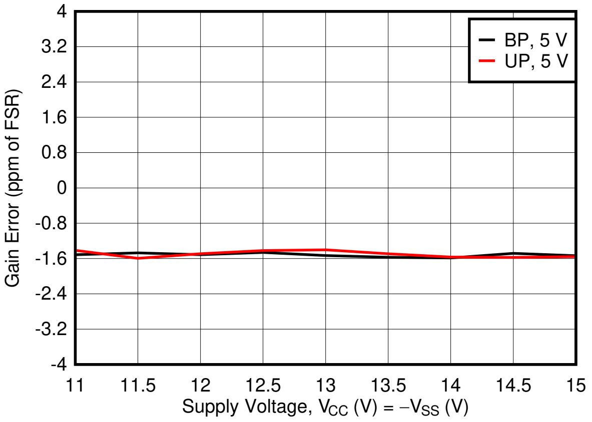


图 14. Gain Error vs Supply Voltage

Typical Characteristics (接下页)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as output and reference amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)

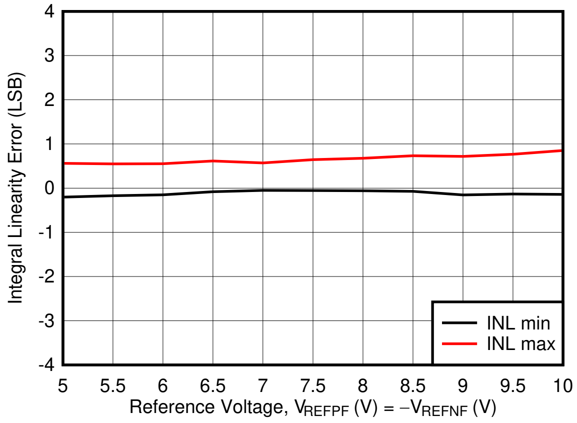


图 15. Integral Linearity Error vs Reference Voltage

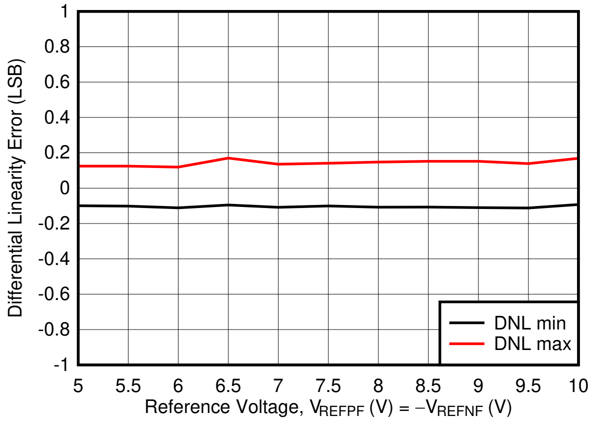


图 16. Differential Linearity Error vs Reference Voltage

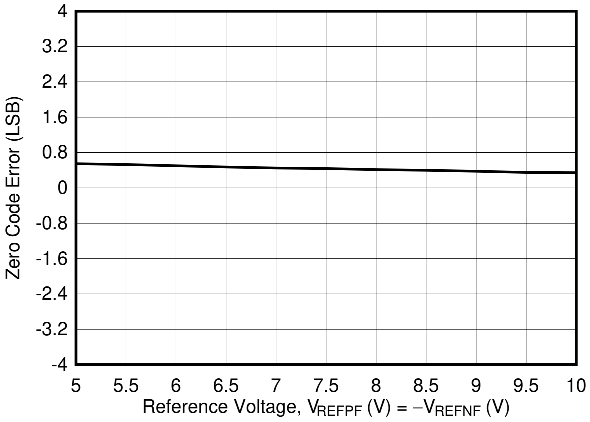


图 17. Zero Code Error vs Reference Voltage

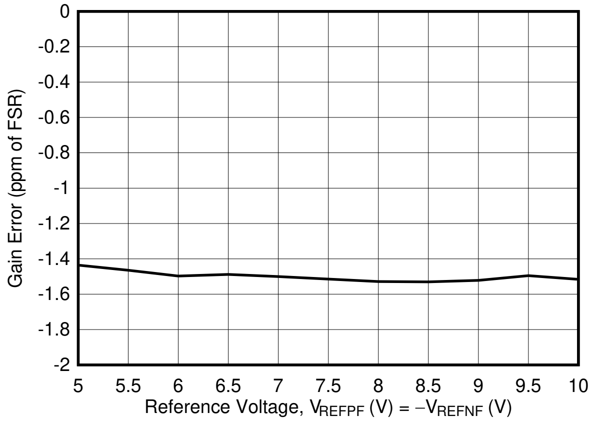


图 18. Gain Error vs Reference Voltage

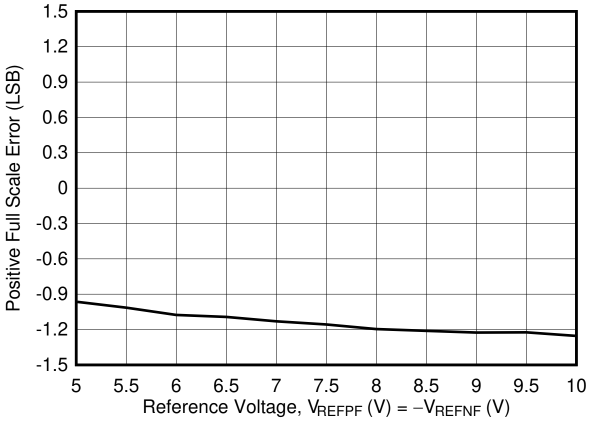
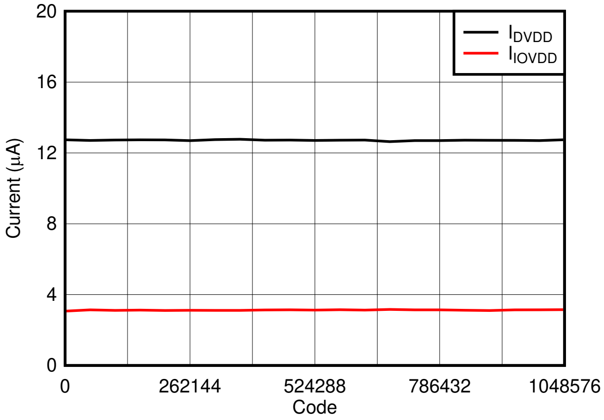


图 19. Positive Full-Scale Error vs Reference Voltage

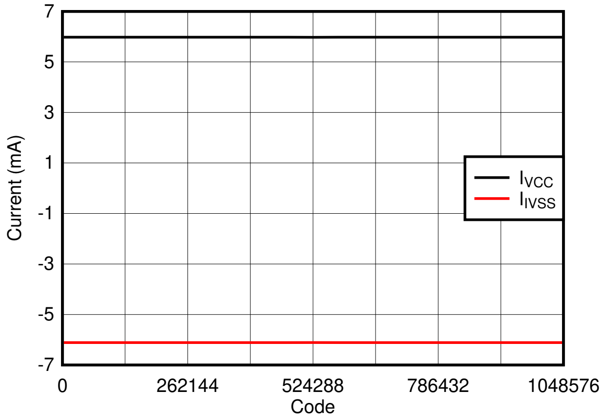


V_{REFPF} = 10 V, V_{REFNF} = 0 V

图 20. Supply Current (DV_{DD} and IOV_{DD}) vs Digital Input Code

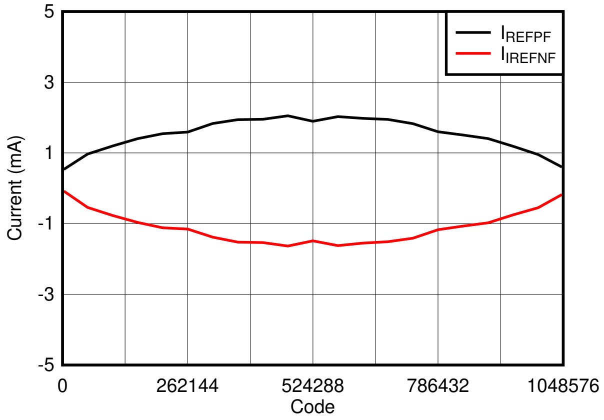
Typical Characteristics (接下页)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as output and reference amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



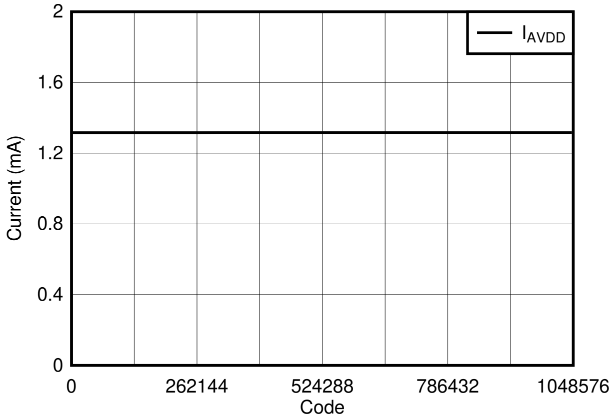
V_{REFPF} = 10 V, V_{REFNF} = 0 V

图 21. Supply Current (V_{CC} and V_{SS}) vs Digital Input Code



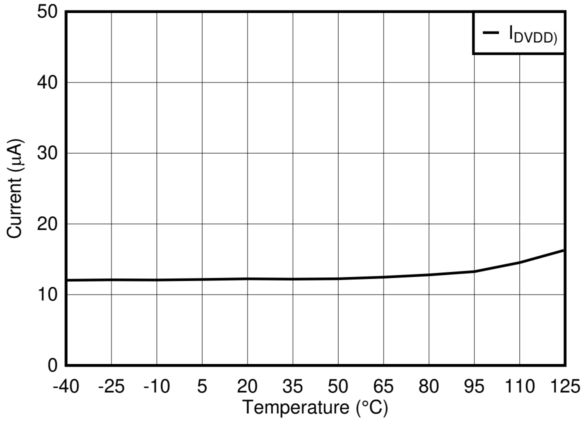
V_{REFPF} = 10 V, V_{REFNF} = 0 V

图 22. Reference Current (V_{REFPF} and V_{REFNF}) vs Digital Input Code



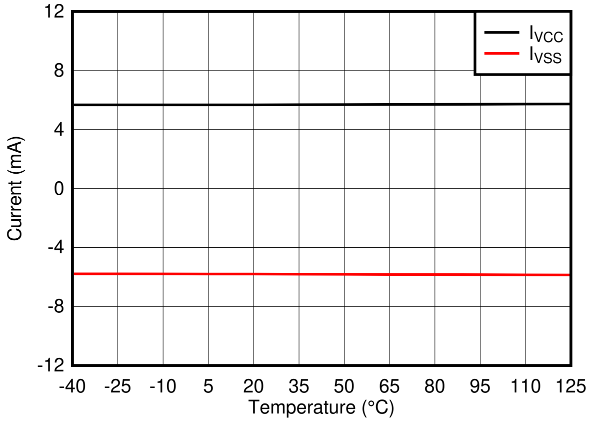
V_{REFPF} = 10 V, V_{REFNF} = 0 V

图 23. Supply Current (AV_{DD}) vs Digital Input Code



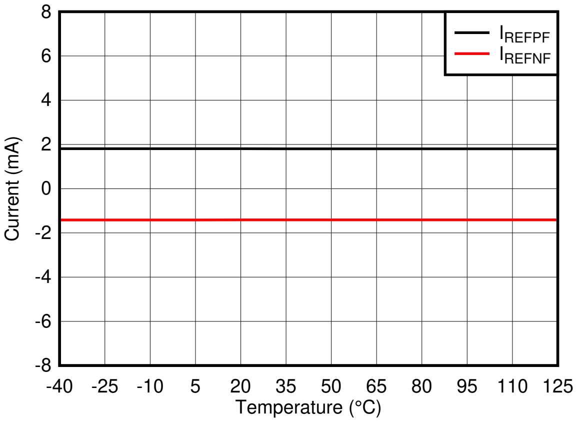
V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

图 24. Supply Current (DV_{DD}) vs Temperature



V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

图 25. Supply Current (V_{CC} and V_{SS}) vs Temperature

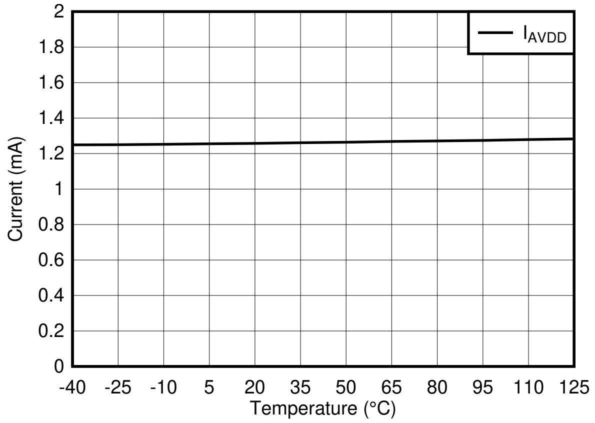


V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

图 26. Reference Current (V_{REFPF} and V_{REFNF}) vs Temperature

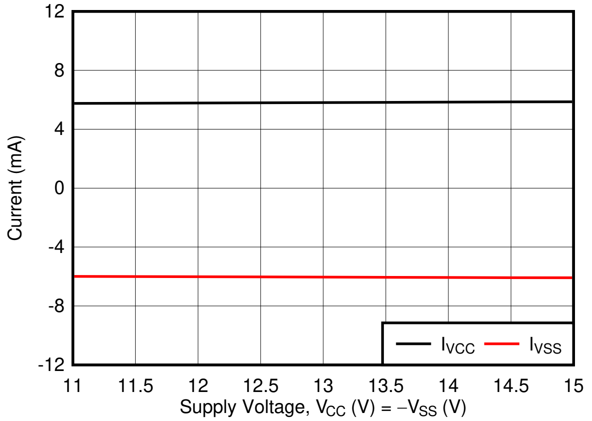
Typical Characteristics (接下页)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as output and reference amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



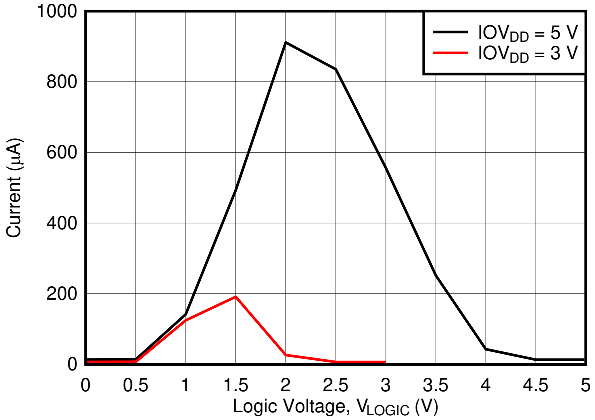
V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

图 27. Supply Current (AV_{DD}) vs Temperature



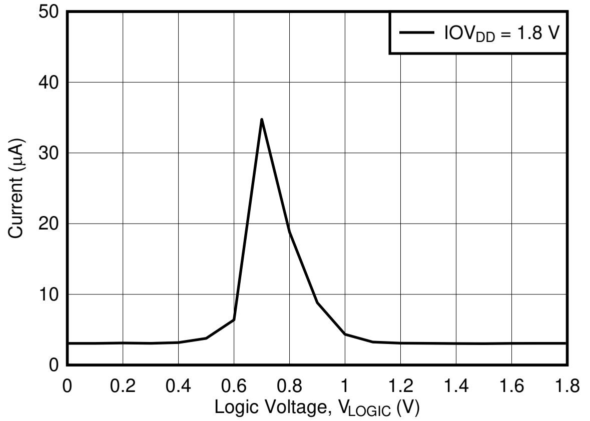
V_{REFPF} = 5 V, V_{REFNF} = 0 V, DAC at midcode

图 28. Supply Current (V_{CC} and V_{SS}) vs Supply Voltage



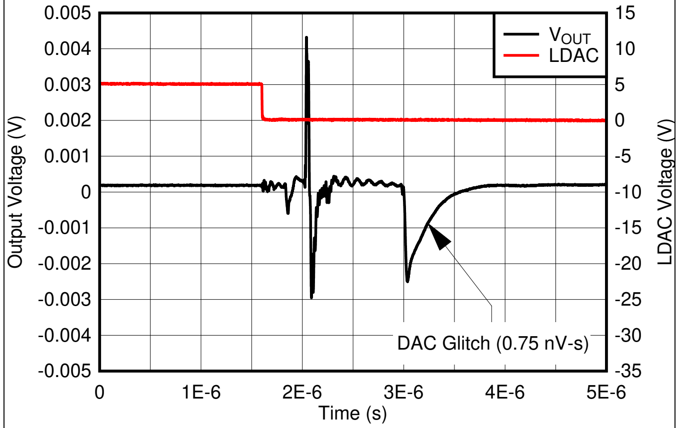
V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

图 29. Supply Current (IOV_{DD}) vs Input Pin Logic Level



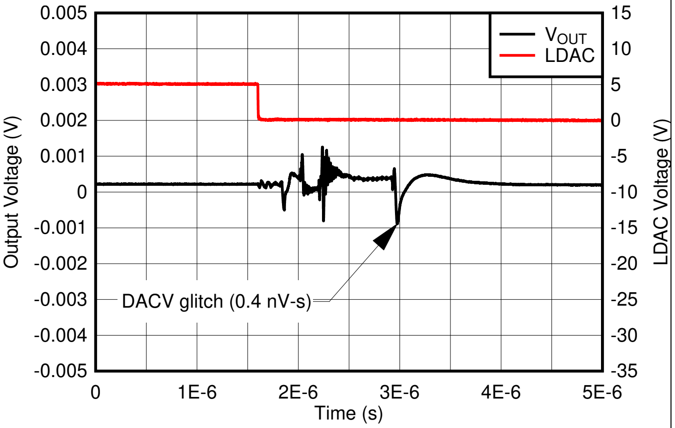
V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

图 30. Supply Current (IOV_{DD} = 1.8 V) vs Input Pin Logic Level



V_{REFPF} = 10 V, V_{REFNF} = –10 V, DAC transition midcode – 1 to midcode

图 31. Glitch Impulse, Rising Edge, 1-LSB Step

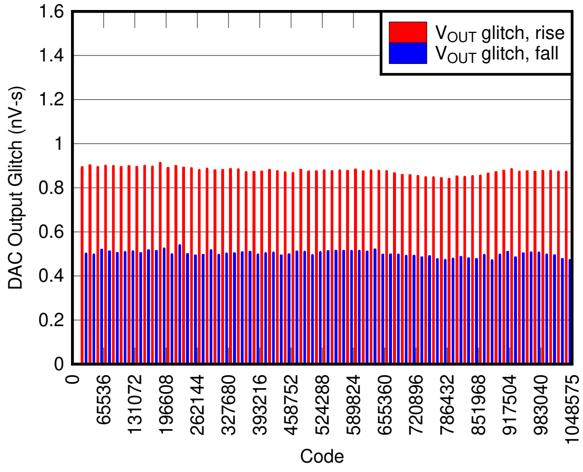


V_{REFPF} = 10 V, V_{REFNF} = –10 V, DAC transition midcode to midcode – 1

图 32. Glitch Impulse, Falling Edge, 1-LSB Step

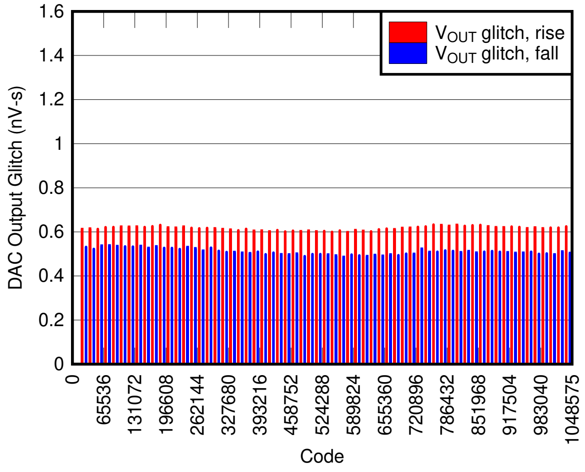
Typical Characteristics (接下页)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as output and reference amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



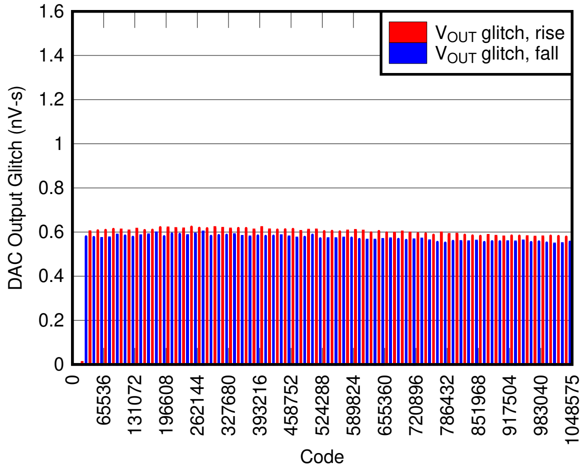
V_{REFPF} = 10 V, V_{REFNF} = –10 V

图 33. Segment Glitch Impulse, 1-LSB Step



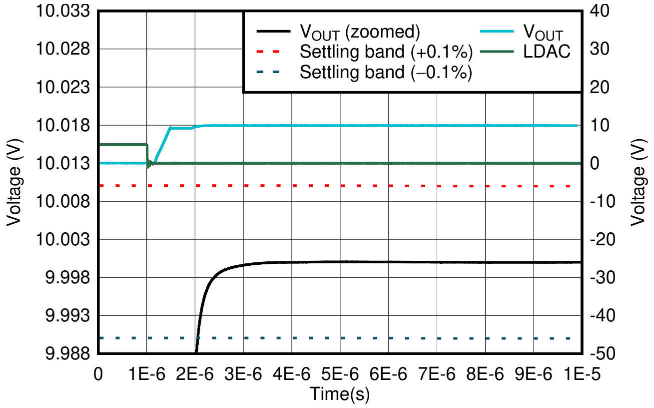
V_{REFPF} = 10 V, V_{REFNF} = 0 V

图 34. Segment Glitch Impulse, 1-LSB Step



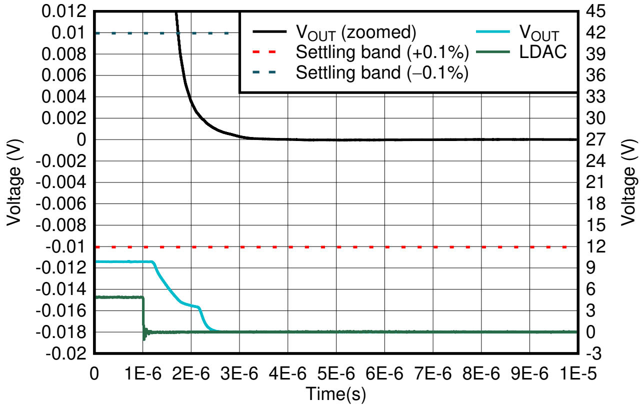
V_{REFPF} = 5 V, V_{REFNF} = 0 V

图 35. Segment Glitch Impulse, 1-LSB Step



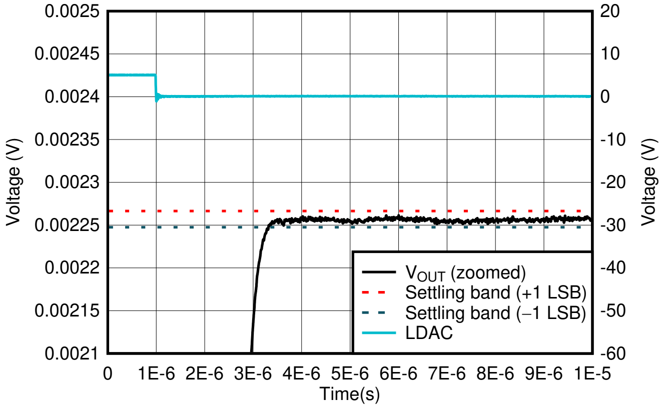
V_{REFPF} = 10 V, V_{REFNF} = 0 V

图 36. Full-Scale Settling Time, Rising Edge



V_{REFPF} = 10 V, V_{REFNF} = 0 V

图 37. Full-Scale Settling Time, Falling Edge

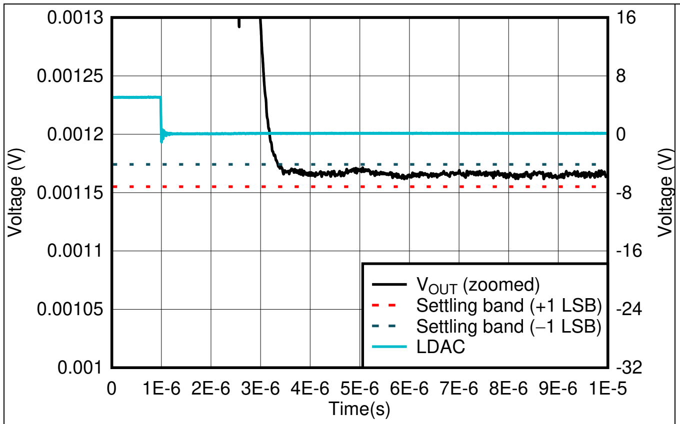


V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC transitions 100 codes around midscale

图 38. 100 Codes Settling Time, Rising Edge

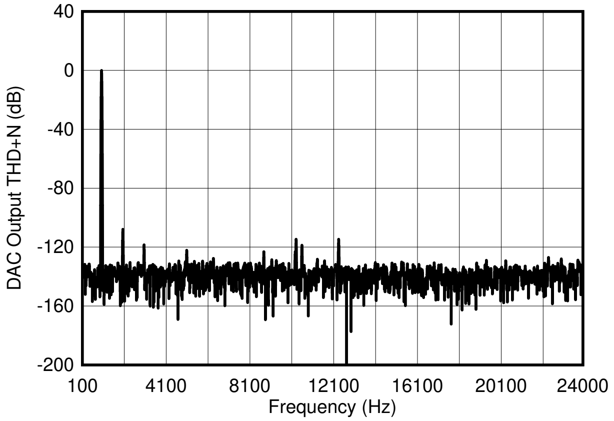
Typical Characteristics (接下页)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as output and reference amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



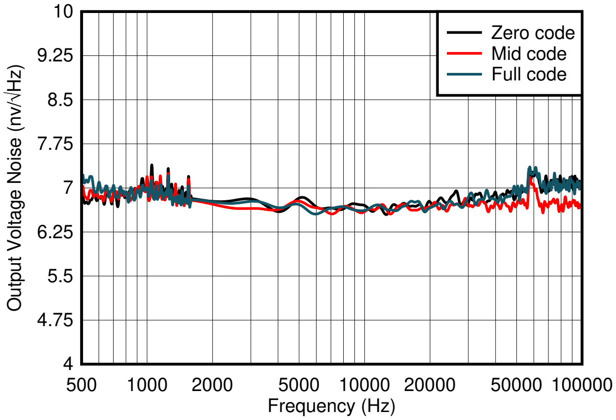
V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC transitions 100 codes around midscale

图 39. 100 Codes Settling Time, Falling Edge



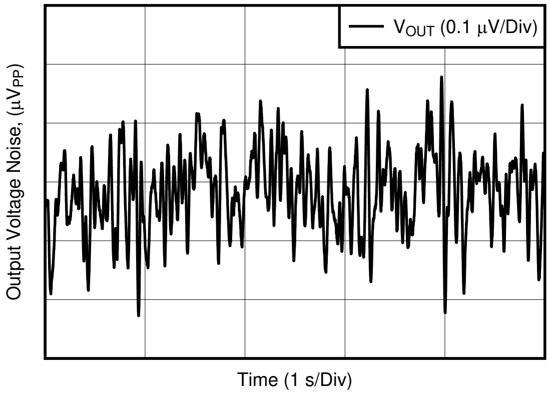
V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC output frequency = 1 kHz, DAC update rate = 400 kHz

图 40. Total Harmonic Distortion (THD + N) vs Frequency



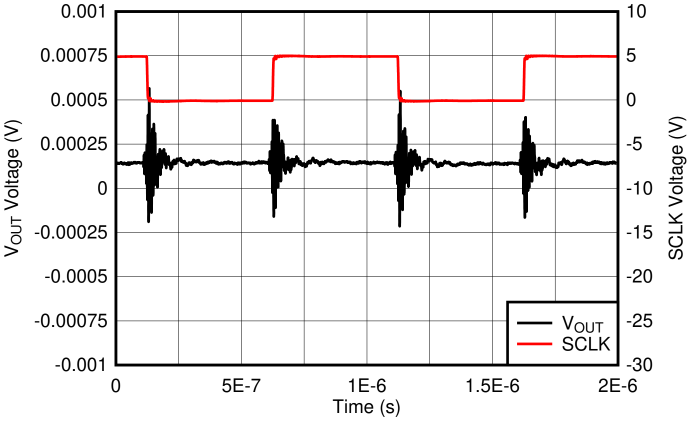
V_{REFPF} = 10 V, V_{REFNF} = 0 V, measured at DAC output

图 41. DAC Output Noise Spectral Density



V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode, measured at DAC output pin

图 42. DAC Output Noise: 0.1 Hz to 10 Hz



V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode, measured at DAC output pin

图 43. Clock Feedthrough

8 Detailed Description

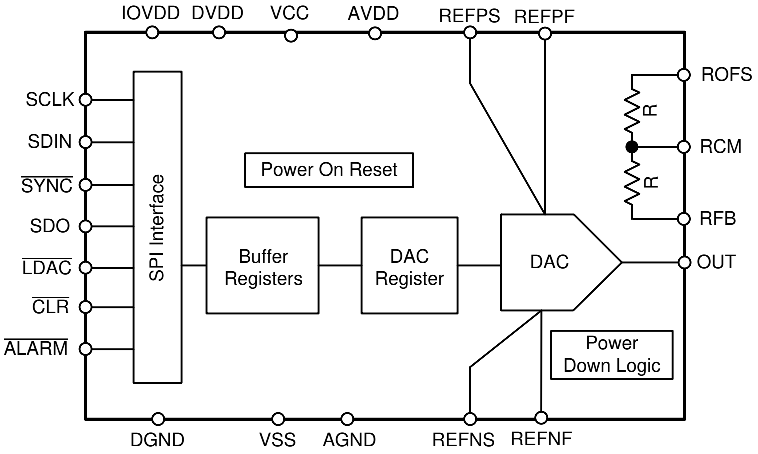
8.1 Overview

The 20-bit DAC11001A, 18-bit DAC91001, and 16-bit DAC81001 (DACx1001) are single-channel DACs. The unbuffered DAC output architecture is based on an R2R ladder that is designed to provide monotonicity over wide reference and temperature ranges (1-LSB DNL). This architecture provides a very low-noise (7 nV/$\sqrt{\text{Hz}}$) and fast-settling (1 µs) output. The DACx1001 also implement a deglitch circuit that enables low, code-independent glitch at the DAC output. This is extremely useful for creating ultra low harmonic distortion waveform generation.

The DACx1001 requires external reference voltages on REFPF and REFNF pins. The output of the DAC ranges from V_{REFNF} to V_{REFPF}. See the *Recommended Operating Conditions* for V_{REFPF} and V_{REFNF} voltage ranges.

The DACx1001 also includes precision matched gain setting pins (ROFS, RCM, and RFB), Using these pins and an external op amp, the DAC output can be scaled. The DACx1001 incorporate a power-on-reset circuit that makes sure that the DAC output powers up at zero scale, and remains at zero scale until a valid DAC command is issued. The DACx1001 use a 4-wire serial interface that operates at clock rates of up to 50 MHz.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital-to-Analog Converter Architecture

The DACx1001 provide 20-bit monotonic outputs using an R2R ladder architecture. The DAC output ranges between VREFNF and VREFPF based on the 20-bit DAC data, as described in 公式 1:

$$V_{OUT} = (V_{REFPF} - V_{REFNF}) \times \frac{CODE}{2^N} + V_{REFNF}$$

where

- CODE is the decimal equivalent of the DAC-DATA loaded to the DAC.
- N is the bits of resolution; 20 for DAC1101A, 18 for DAC91001, 16 for DAC81001.
- V_{REF}PF, V_{REF}NF is the reference voltage (positive and negative). (1)

Feature Description (接下页)

8.3.2 External Reference

The DACx1001 require external references (REFPF and REFNF) to operate. See the *Recommended Operating Conditions* for V_{REFPF} and V_{REFNF} voltage ranges.

The DACx1001 also contain dedicated sense pins, REFPS for REFPF and REFNS for REFNF. The reference pins are unbuffered; therefore, use a reference driver circuit for these pins. Set the VREFVAL bits (address 02h) as per a reference span equal to (V_{REFPF} – V_{REFNF}). For example, the VREFVAL bits must be set to 0100 for V_{REFPF} = 5 V and V_{REFNF} = –5 V.

图 44 shows an example reference drive circuit for DACx1001. 表 1 shows the op-amp options for the reference driver circuit.

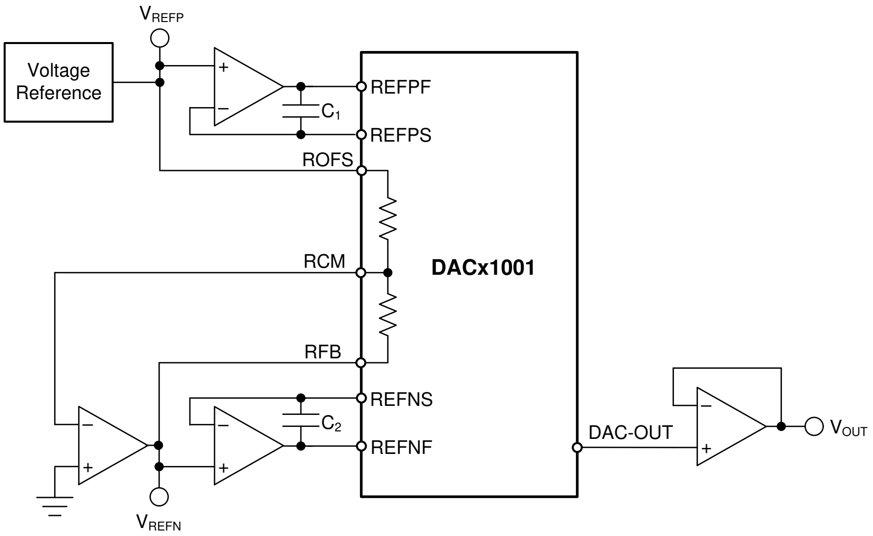


图 44. Reference Drive Circuit

表 1. Reference Op Amp Options

SELECTION PARAMETERS	OP AMPS
Low voltage and current noise	OPA211, OPA827, OPA828
Low offset and drift	OPA189

8.3.3 Output Buffers

The DACx1001 outputs are unbuffered. Use an external op amp to buffer the DAC output. The DAC output voltage ranges from V_{REFPF} to V_{REFNF}. Two gain-setting resistors are integrated in the DACx1001. These resistors are used to scale the DAC output, minimize the bias current mismatch of the external op amp, and generate a negative reference for the REFNF pin. See the *Embedded Resistor Configurations* section for more information. 表 2 shows the op amp options for the output drive circuit.

表 2. Output Op Amp Options

SELECTION PARAMETERS	OP AMPS
Low bias current	OPA827, OPA828
Low noise	OPA211, OPA828
Low offset and drift	OPA189
Fast settling and low THD	OPA827, OPA828, OPA1612, THS4011

8.3.4 Internal Power-On Reset (POR)

The DACx1001 incorporate two internal POR circuits for the DV_{DD}, AV_{DD}, IOV_{DD}, V_{CC}, and V_{SS} supplies. The POR signals are ANDed together, so that all supplies must be at the minimal specified values for the device to *not* be in a reset condition. These POR circuits initialize internal registers, as well as set the analog outputs to a known state while the device supplies are ramping. All registers are reset to default values. The DACx1001 power on with the DAC registers set to zero scale. The DAC can be powered down by writing 1 to PDN (bit 4, address 02h). Typically, the POR function can be ignored as long as the device supplies power up and maintain the specified minimum voltage levels. However, in the case of supply drop or brownout, the DACx1001 can have an internal POR reset event. 图 45 represents the internal POR threshold levels for the DV_{DD}, AV_{DD}, IOV_{DD}, V_{CC}, and V_{SS} supplies.

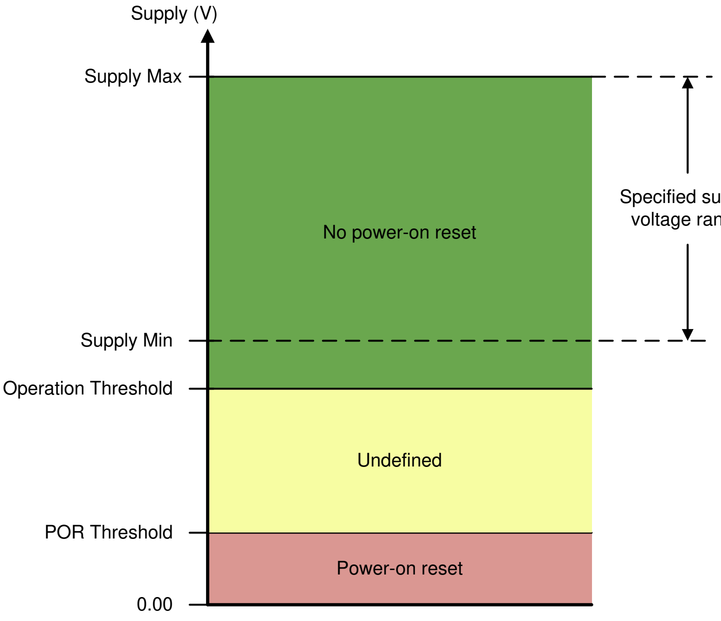


图 45. Relevant Voltage Levels for the POR Circuit

For the DV_{DD} supply, no internal POR occurs for nominal supply operation from 2.7 V (supply minimum) to 5.5 V (supply maximum). For a DV_{DD} supply region between 2.5 V (undefined operation threshold) and 1.6 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For a DV_{DD} supply less than 1.6 V (POR threshold), the internal POR resets as long as the supply voltage is less than 1.6 V for approximately 1 ms.

For the AV_{DD} supply, no internal POR occurs for nominal supply operation from 4.5 V (supply minimum) to 5.5 V (supply maximum). For an AV_{DD} supply region between 4.1 V (undefined operation threshold) and 3.3 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For an AV_{DD} supply less than 3.3 V (POR threshold), the internal POR resets as long as the supply voltage is less than 3.3 V for approximately 1 ms.

For the V_{CC} supply, no internal POR occurs for nominal supply operation from 8 V (supply minimum) to 36 V (supply maximum). For V_{CC} supply voltages between 7.5 V (undefined operation threshold) to 6 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For a V_{CC} supply less than 6 V (POR threshold), the internal POR resets as long as the supply voltage is less than 6 V for approximately 1 ms.

For the V_{SS} supply, no internal POR occurs for nominal supply operation from –3 V (supply minimum) to –18 V (supply maximum). For V_{SS} supply voltages between –2.7 V (undefined operation threshold) to –1.8 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For a V_{SS} supply greater than –1.8 V (POR threshold), the internal POR resets as long as the supply voltage is higher than –1.8 V for approximately 1 ms.

For the IOV_{DD} supply, no internal POR occurs for nominal supply operation from 1.8 V (supply minimum) to 5.5 V (supply maximum). For IOV_{DD} supply voltages between 1.5 V (undefined operation threshold) and 0.8 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For an IOV_{DD} supply less than 0.8 V (POR threshold), the internal POR resets as long as the supply voltage is less than 0.8 V for approximately 1 ms.

In case the DV_{DD}, AV_{DD}, IOV_{DD}, V_{CC}, or V_{SS} supply drops to a level where the internal POR signal is indeterminate, power cycle the device followed using a software reset.

8.3.5 Temperature Drift and Calibration

The DACx1001 includes a calibration circuit that significantly reduces the temperature drift on integrated and differential nonlinearities. By default, this feature is disabled. Enable the temperature calibration feature by writing 1 to the EN_TMP_CAL bit (address 02h, B23). After the EN_TMP_CAL bit is set, issue a calibration cycle by writing 1 to RCLTMP (address 04h, B8). At this point, the device enters a calibration cycle. Do not issue any DAC update command during this period. The device has the capability to indicate the end of calibration using two methods:

1. Read the status bit ALM (address 05h, B12) using SPI.
2. Issue an alarm on the $\overline{\text{ALARM}}$ pin by setting logic 0. To enable this feature, write 1 to ENALMP bit (address 02h, B12).

After the calibration cycle completes, update the DAC code to observe the impact at the DAC output. If the environmental temperature changes after calibration, then recalibrate the device.

8.3.6 DAC Output Deglitch Circuit

The DACx1001 include a deglitch (track-and-hold) circuit at the output. This circuit is enabled by default. The deglitch circuit minimizes the code-to-code glitch at the DAC output at the expense of the DAC update rate. This circuit is disabled by writing 1 to DIS_TNH (bit 7, address 06h). Disable this circuit to enable faster update of the DAC output, but with higher code-to-code glitches.

8.4 Device Functional Modes

8.4.1 Fast-Settling Mode and THD

The DACx1001 R2R ladder and deglitch circuit reduce the harmonic distortion for waveform generation applications. The fast settling bit (FSET, bit 10, address 02h) is set to 1 by default, so that the DAC is configured for enhanced THD performance. The FSET bit can be reset to 0 using an SPI write to enable fast-settling mode. In this mode, the DAC deglitcher circuit can be configured using TNH_MASK (bits 19:18, address 02h). These bits disable the deglitch circuit for code changes specified in 表 7. These bits are only writable when FSET = 0 (fast settling enabled) and DIS_TNH = 0 (deglitch circuit enabled).

8.4.2 DAC Update Rate Mode

The DACx1001 maximum update rate can be configured up to 1 MHz by using UP_RATE (bits 6:4, address 06h). These bits change the hold timing of the deglitch circuit. The bits are set to a 0.5-MHz DAC update rate by default for enhanced THD performance. Changing the maximum update rate of the DAC impacts THD performance.

8.5 Programming

The DACx1001 family of devices is controlled through a flexible four-wire serial interface that is compatible with serial interfaces used on many microcontrollers and DSP controllers. The interface provides read and write access to all registers of the DACx1001 devices. Additionally, the interface can be configured to daisy-chain multiple devices for write operations.

Each serial interface access cycle is exactly 32 bits long, as shown in 图 46. A frame is initiated by asserting SYNC pin low. The frame ends when the SYNC pin is deasserted high. The first bit is read/write bit B31. A write is performed when this bit is set to 0, and a read is performed when this bit is set to 1. The next 7 bits are address bits B30 to B24. The next 20 bits are data. For all writes, data are clocked on the falling edge of SCLK. As 图 47 shows, for read access and daisy-chain operation, the data are clocked out on the SDO terminal on the rising edge of SCLK.

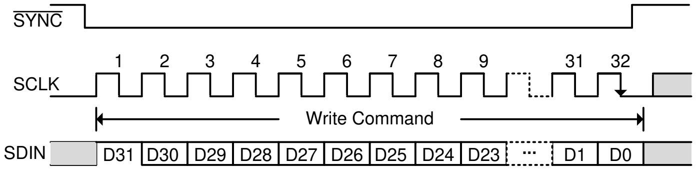


图 46. Serial Interface Write Bus Cycle: Standalone Mode

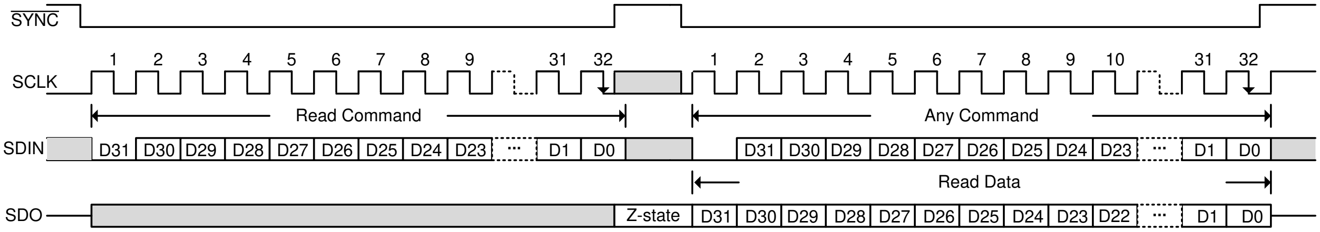


图 47. Serial Interface Read Bus Cycle

8.5.1 Daisy-Chain Operation

For systems that contain several DACx1001 devices, the SDO pin is used to daisy-chain the devices together. The daisy-chain feature is useful in reducing the number of serial interface lines. The first falling edge on the SYNC pin starts the operation cycle, as shown in 图 48. SCLK is continuously applied to the input shift register while the SYNC pin is kept low. The DAC is updated with the data on rising edge of SYNC pin.

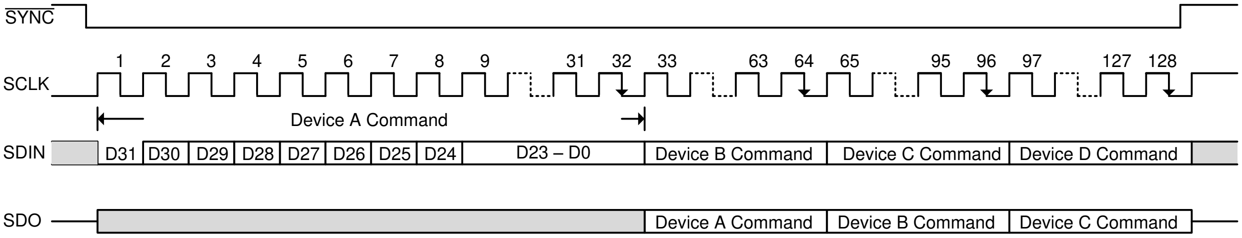


图 48. Serial Interface Daisy-Chain Write Cycle

If more than 32 clock pulses are applied, the data ripple out of the shift register and appear on the SDO line. These data are clocked out on the rising edge of SCLK and are valid on the falling edge. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 32 clock pulses.

Programming (接下页)

As a result, the total number of clock cycles must be equal to 32 × N, where N is the total number of devices in the daisy-chain. When the serial transfer to all devices is complete the SYNC signal is taken high. This action transfers the data from the SPI shift registers to the internal register of each device in the daisy-chain and prevents any further data from being clocked into the input shift register. The DACx1001 implement a bit that enables higher speeds for clocking out data from the SDO pin. Enable this feature by setting FSDO (bit 13, address 02h) to 1. See Timing Requirements: Read and Daisy-Chain Write, 2.7 V ≤ DV_{DD} < 4.5 V and for more information.

8.5.2 CLR Pin Functionality and Software Clear

The CLR pin is an asynchronous input pin to the DAC. When activated, this level-sensitive pin clears the DAC buffers and DAC latches to the DAC-CLEAR-DATA bits (address 03h). The device exits clear mode on the SYNC rising edge of the next valid write to the device. If the CLR pin receives a logic 0 during a write sequence during normal operation, the clear mode is activated and the buffer and DAC registers are immediately cleared. The DAC registers can also be cleared using the SCLR bit (address 04h, B5); the contents are cleared at the rising edge of SYNC.

8.5.3 Output Update (Synchronous and Asynchronous)

The DACx1004 devices offer both a software and hardware simultaneous update and control function. The DAC double-buffered architecture has been designed so that new data can be entered for the DAC without disturbing the analog output. Data updates can be performed either in synchronous or in asynchronous mode, depending on the status of LDAC-MODE bit (address 02h, B14).

8.5.3.1 Synchronous Update

In synchronous mode (LDACMODE = 1), the LDAC pin is used as an active-low signal for simultaneous DAC updates. Data buffers must be loaded with the desired data before an LDAC low pulse. After an LDAC low pulse, the DAC is updated with the last contents of the corresponding data buffers. If the content of a data buffer is not changed, the DAC output remains unchanged after the LDAC pin is pulsed low.

8.5.3.2 Asynchronous Update

In asynchronous mode (LDACMODE = 0), data are updated with the rising edge of the SYNC (when daisy-chain mode is enabled, DSDO = 0), or at the 32nd falling edge of SCLK (When daisy-chain mode is disabled, DSDO = 1). For asynchronous updates, the LDAC pin is not required, and it must be connected to 0 V permanently.

8.5.4 Software Reset Mode

The DACx1001 implements a software reset feature. The software reset function uses the SRST bit (address 04h, B6). When this bit is set to 1, the device resets to the default state.

8.6 Register Map

表 3. Register Map

REGISTER NAME	BIT																						
	31	**30-24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3-0**
NOP	$\overline{\text{W}}$	00h	NOP																				0h
DAC-DATA	R/$\overline{\text{W}}$	01h	DAC-DATA (20 bits, 18 bits, or 16 bits, left-justified)																				0h
CONFIG1	R/$\overline{\text{W}}$	02h	EN_ TMP_ CAL	0h			TNH_MASK		0h			LDAC MODE	FSDO	ENALMP	DSDO	FSET	VREFVAL				0	PDN	0h
DAC-CLEAR-DATA	R/$\overline{\text{W}}$	03h	DAC-CLEAR-DATA (8 bits left justified)								000h												0h
TRIGGER	R/$\overline{\text{W}}$	04h	0000h															RCLTMP	0	SRST	SCLR	0	0h
STATUS	R	05h	000h											ALM	00h								0h
CONFIG2	R/$\overline{\text{W}}$	06h	0000h																DIS_TNH	TNH_SETTING			0h

表 4. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

8.6.1 NOP Register (address = 00h) [reset = 0x000000h]

图 49. NOP Register Format

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>Read/ Write</td><td colspan="7">Address</td><td colspan="8">NOP</td></tr>
<tr><td>$\overline{\text{W}}$</td><td colspan="7">W</td><td colspan="8">W</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="12">NOP</td><td colspan="4">0h</td></tr>
<tr><td colspan="12">W</td><td colspan="4">W</td></tr>
</table>

表 5. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Write	W	N/A	Write when set to 0
30:24	Address	W	N/A	00h
23:4	NOP	W	00000h	No operation - Write 00000h
3:0	0h	W	N/A	N/A

8.6.2 DAC-DATA Register (address = 01h) [reset = 0x000000h]

图 50. DAC-DATA Register Format

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>Read/ Write</td><td colspan="7">Address</td><td colspan="8">DAC-DATA (20-bit, 18-bit, or 16-bit, left justified)</td></tr>
<tr><td>R/$\overline{\text{W}}$</td><td colspan="7">W</td><td colspan="8">R/W</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="12">DAC-DATA (20-bit, 18-bit, or 16-bit, left justified)</td><td colspan="4">0h</td></tr>
<tr><td colspan="12">R/W</td><td colspan="4">W</td></tr>
</table>

表 6. DAC-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	R/$\overline{\text{W}}$	N/A	Read when set to 1 or write when set to 0
30:24	Address	W	N/A	01h
23:4	DAC-DATA[19:0]	R/W	0h	Stores the 20-bit, 18-bit, or 16-bit data to be loaded to DAC in MSB aligned straight binary format. Data follows the format below: DAC1101A: { DAC-DATA[19:0] } DAC91001: { DAC-DATA[17:0], 0, 0 } DAC81001: { DAC-DATA[15:0], 0, 0, 0, 0}
3:0	0h	W	N/A	N/A

8.6.3 CONFIG1 Register (address = 02h) [reset = 004C80h for bits [23:0]]

图 51. CONFIG1 Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							EN_ TMP_ CAL	0h			TNH_MASK		0h	
R/$\overline{W}$	W							R/W	W			R/W		W	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0h	LDAC MODE	FSDO	ENALMP	DSDO	FSET	VREFVAL				0h	PDN	0h			
W	R/W									W	R/W	W			

表 7. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	R/$\overline{W}$	N/A	Read when set to 1 or write when set to 0
30:24	Address	W	N/A	02h
23	EN_TMP_CAL	R/W	0h	Enables and disables the temperature calibration feature 0 : Temperature calibration feature disabled (default) 1 : Temperature calibration feature enabled
22:20	0h	W	N/A	N/A
19-18	TNH_MASK	R/W	0h	Mask track and hold (TNH) circuit. This bit is writable only when FSET = 0 [fast-settling mode] and DIS_TNH = 0 [track-and-hold enabled] 00: TNH masked for code jump > 2^14 (default) 01: TNH masked for code jump > 2^15 10: TNH masked for code jump > 2^13 11: TNH masked for code jump > 2^12
17:15	0h	W	N/A	N/A
14	LDACMODE	R/W	1	Synchronous or asynchronous mode select bit 0 : DAC output updated on $\overline{\text{SYNC}}$ rising edge 1 : DAC updated on $\overline{\text{LDAC}}$ falling edge (default)
13	FSDO	R/W	0h	Enable Fast SDO 0 : Fast SDO disabled (Default) 1 : Fast SDO enabled
12	ENALMP	R/W	0h	Enable $\overline{\text{ALARM}}$ pin to be pulled low, end of temperature calibration cycle 0 : No alarm on the $\overline{\text{ALARM}}$ pin 1 : Indicates end of temperature calibration cycle. $\overline{\text{ALARM}}$ pin pulled low.
11	DSDO	R/W	1h	Enable SDO (for readback and daisy-chain) 1 : SDO enabled (default) 0 : SDO disabled
10	FSET	R/W	1h	Fast-settling vs enhanced THD mode 0 : Fast settling 1 : Enhanced THD (default)
9:6	VREFVAL	R/W	2h	Reference span value bits 0000: Invalid 0001: Invalid 0010: Reference span = 5 V ± 1.25 V (default) 0011: Reference span = 7.5 V ± 1.25 V 0100: Reference span = 10 V ± 1.25 V 0101: Reference span = 12.5 V ± 1.25 V 0110: Reference span = 15 V ± 1.25 V 0111: Reference span = 17.5 V ± 1.25 V 1000: Reference span = 20 V ± 1.25 V 1001: Reference span = 22.5 V ± 1.25 V 1010: Reference span = 25 V ± 1.25 V 1011: Reference span = 27.5 V± 1.25 V 1100: Reference span = 30 V ± 1.25 V
5	0	W	N/A	N/A
4	PDN	R/W	0h	Powers down and power up the DAC 0 : DAC power up (default) 1 : DAC power down
3:0	0000	R/W	N/A	N/A

8.6.4 DAC-CLEAR-DATA Register (address = 03h) [reset = 000000h for bits [23:0]]

图 52. DAC-CLEAR-DATA Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							DAC-CLEAR-DATA (8 bits, left justified)							
R/$\overline{\text{W}}$	W							R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
000h												0h			
W												W			

表 8. DAC-CLEAR-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	R/$\overline{\text{W}}$	N/A	Read when set to 1 or write when set to 0
30:24	Address	W	N/A	03h
23:16	DAC-CLEAR-DATA	R/W	00h	Stores the 8-bit data to be loaded to DAC in left-justified, straight-binary format. DAC data registers updated with this value when $\overline{\text{CLR}}$ pin asserted low
15:0	000h	W	N/A	N/A

8.6.5 TRIGGER Register (address = 04h) [reset = 000000h for bits [23:0]]

图 53. TRIGGER Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							00h							
R/$\overline{\text{W}}$	W							W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h							RCLTMP	0h	SRST	SCLR	0h	0h			
W							R/W	W	R/W	R/W	W	W			

表 9. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	R/$\overline{\text{W}}$	N/A	Read when set to 1 or write when set to 0
30:24	Address	W	N/A	04h
23:9	0000h	W	N/A	Unused
8	RCLTMP	R/W	0h	Trigger temperature recalibration DAC Codes 0 : No temperature recalibration (default) 1 : DAC codes recalibrated, $\overline{\text{ALARM}}$ pin is pulled low (if ENALMP = 1) and ALM bit (Address 05) is set 1 upon calibration completion. Subsequent DAC codes will use latest calibrated coefficients.
7	0h	W	N/A	NA
6	SRST	R/W	0h	Software reset 0 : No software reset (default) 1 : Software reset initiated, device in default state
5	SCLR	R/W	0h	Software clear 0 : No software clear (default) 1 : Software clear initiated, DAC registers in clear mode, DAC code set by clear select register (address 03h). DAC output clears on 32nd SCLK falling (DSDO = 1) or $\overline{\text{SYNC}}$ rising edge (DSDO = 0)
4	0h	W	N/A	N/A
3:0	0h	W	N/A	N/A

8.6.6 STATUS Register (address = 05h) [reset = 000000h for bits [23:0]]

图 54. STATUS Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							00h							
R	W							W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0h			ALM	00h								0h			
W			R	W								W			

表 10. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	R	N/A	Read when set to 1 , read only
30:24	Address	W	N/A	05h
23:13	000h	W	N/A	N/A
12	ALM	R	0	Alarm indicator bit, This bit is not masked by ENALMP bit 0 :Temperature recalibration in progress 1 : DAC codes recalibrated, $\overline{\text{ALARM}}$ pin is pulled low (if ENALMP = 1) Subsequent DAC codes will use latest calibrated coefficients. Reading back this register resets $\overline{\text{ALARM}}$ pin to 1 status.
11:4	00h	W	N/A	N/A
3:0	0h	W	N/A	N/A

8.6.7 CONFIG2 Register (address = 06h) [reset = 000040h for bits [23:0]]

图 55. CONFIG2 Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							00h							
R/$\overline{W}$	W							W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h								DIS_TNH	UP_RATE			0h			
W								R/W	R/W			W			

表 11. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	R/$\overline{W}$	N/A	Read when set to 1 or write when set to 0
30:24	Address	W	N/A	06h
23:8	0000h	W	N/A	N/A
7	DIS_TNH	R/W	0h	Disable track and hold: 0 : Track and hold enabled (default) 1 : Track and hold disabled
6-4	UP_RATE	R/W	4h	DAC output max update rate: 000: 1 MHz with 38-MHz SCLK 001: 0.9 MHz with 34-MHz SCLK 010: 0.8 MHz with 31-MHz SCLK 011: 1.2 MHz with 45-MHz SCLK 100: 0.5 MHz with 21-MHz SCLK, (default) 101: 0.45 MHz with 18-MHz SCLK 110: 0.4 MHz with 16-MHz SCLK 111: 0.6 MHz with 24-MHz SCLK
3:0	0h	W	N/A	N/A

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DACx1001 family of DACs are targeted for high-precision applications where ultra-high dc accuracy, ultra-low noise, fast settling, or high total harmonic distortion (THD) is required. The DACx1001 provides 20-bit monotonic resolution. This device finds application in high-performance source measure unit (SMU), battery test equipment (BTE), arbitrary waveform generation (AWG), and closed-loop control applications such as microelectromechanical system (MEMS) actuators, linear actuators, precision motor control, lens autofocus control in precision microscopy, lens control in mass spectrometer, beam control in electron beam lithography, and so on.

9.2 Typical Application

9.2.1 Source Measure Unit (SMU)

A source measure unit (SMU) is a common building block in memory and semiconductor test equipment and bench-top source measure units. A DAC is used in an SMU to force a desired voltage or a current to a device-under-test (DUT). 图 56 provides a simplified circuit diagram of the force-DAC in an SMU.

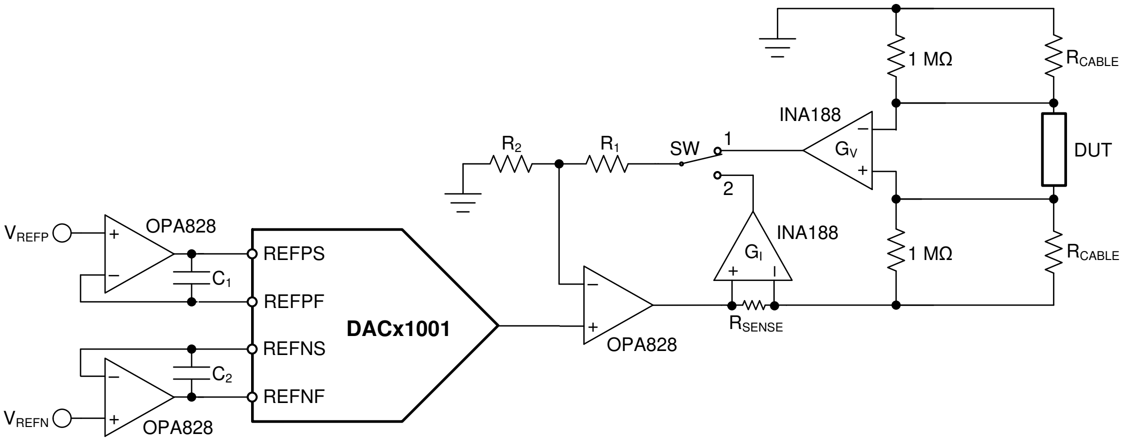


图 56. Source Measure Unit

9.2.1.1 Design Requirements

- Force voltage range: ±10 V
- Force current range: ±20 mA

9.2.1.2 Detailed Design Procedure

The DAC11001A is an excellent choice for this application to meet the 20-bit resolution requirement. Switch SW is used to toggle between force-voltage and force-current modes, as shown in 图 56. The OPA828 is a high-precision amplifier that provides a good balance between dc and ac performance, and can supply ±30-mA output current. The INA188 is a zero-drift instrumentation amplifier with gain selected with an external resistor. The external resistor is not shown in the drawing for simplicity. The gain resistor is not required for a gain of 1. 公式 2 shows the calculation of the voltage gain when switch SW is in position 1.

$$A_V = \frac{1}{G_V} \times \left(1 + \frac{R_1}{R_2}\right) \tag{2}$$

Typical Application (接下页)

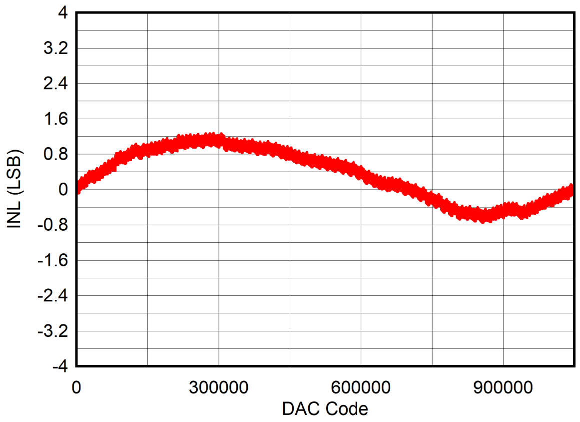
Precision reference sources are available at 5 V or less. Use a ±5-V reference with a 2x gain configuration to get an output of ±10 V. The DAC output amplifier sets the gain at 2, assuming G_V = 1, as shown in 公式 3. R_1 and R_2 are 1-kΩ each. 公式 3 shows the calculation for the current gain when the switch is in the position 2.

$$A_V = \frac{1}{R_{SENSE} x G_I} x \left(1 + \frac{R_1}{R_2}\right) \tag{3}$$

In order to get ±20-mA output current range with R_1 = R_2, R_{SENSE}x G_I must be 500. Choose G_I as 50 so that R_{SENSE} can be 10-Ω. For a ±20mA output current, the voltage drop across R_{SENSE} is ±200-mV. Choose a higher value for G_I and a smaller resistance value for R_{SENSE} in case the design requires a lower voltage headroom.

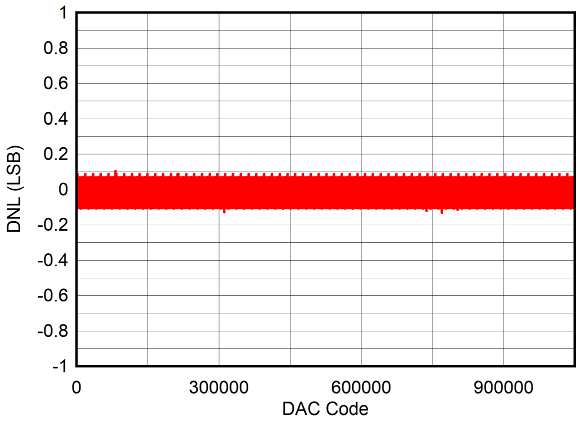
There is no equation to select C_1 and C_2. The values of C_1 and C_2 depend on the stability criteria of the reference buffers when driving the reference inputs of DACx1001. The values are obtained through simulation. For the OPA828, use C_1 = C_2 = 100 pF. The 1-MΩ resistors in the circuit are used for making sure the amplifiers are not left in open loop.

9.2.1.3 Application Curves



Measured on BP-DAC11001EVM, external 10-V reference source

图 57. INL at ±10-V Output



Measured on BP-DAC11001EVM, external 10-V reference source

图 58. DNL at ±10-V Output

Typical Application (接下页)

9.2.2 Battery Test Equipment (BTE)

Battery test equipment is used for lithium-ion battery formation, end-of-line testing, and diagnostics. For battery diagnostics, high-precision DACs, such as the DACx1001, are required to maintain a highly stable voltage over temperature and time.

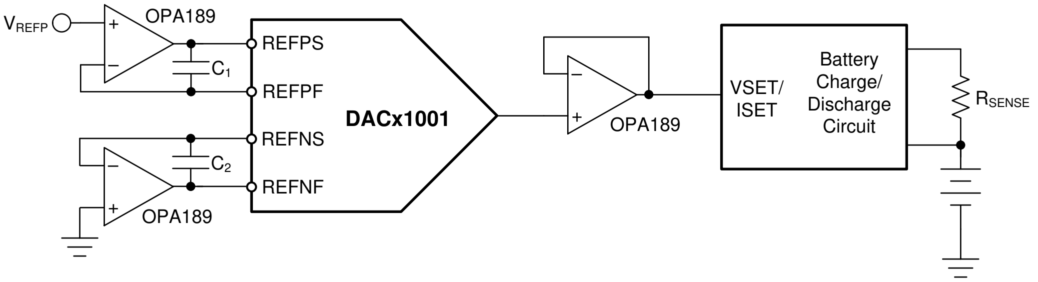


图 59. Battery Test Equipment

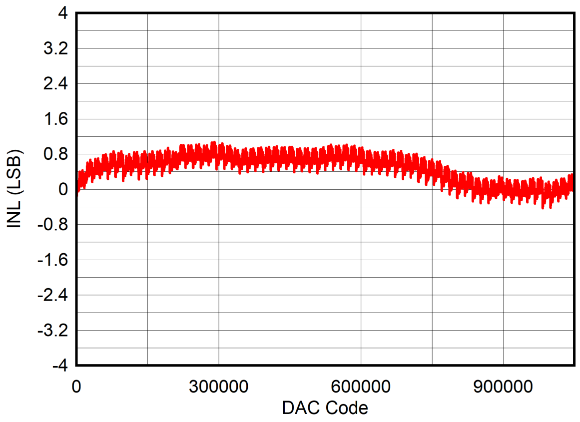
9.2.2.1 Design Requirements

- Output range: 0 V to 5 V
- System level temperature drift: ±2 ppm/°C

9.2.2.2 Detailed Design Procedure

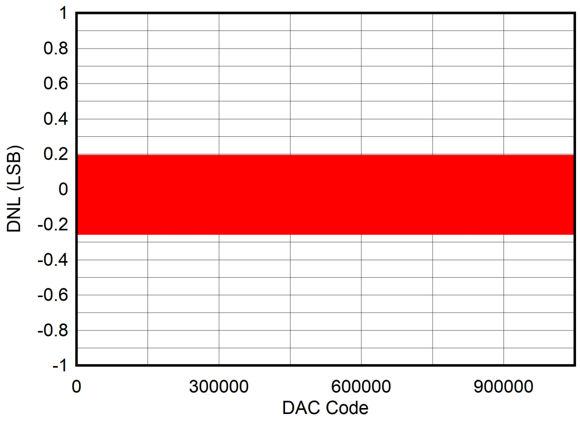
To get unipolar output from DACx1001, connect the negative reference input to ground as shown in 图 59. The OPA189 is a zero-drift amplifier with ±0.02 ppm/°C. The DACx1001 has a temperature drift of offset error of ±0.04 ppm/°C. The temperature drifts of the DAC and amplifier might be neglected when compared to the temperature drift of the reference source. The best reference sources offer temperature drifts of the order of ±2.5 ppm/°C to ±3 ppm/°C. A temperature calibration is needed for the voltage reference to achieve the goal of ±2 ppm/°C.

9.2.2.3 Application Curves



Measured on BP-DAC11001EVM, REF6250 onboard reference source (5 V)

图 60. INL at 0-V to 5-V Output



Measured on BP-DAC11001EVM, REF6250 onboard reference source (5 V)

图 61. DNL at 0-V to 5-V Output

Typical Application (接下页)

9.2.3 High-Precision Control Loop

High-precision control loops are used in precision motion-control applications, such as linear actuator control, servo motor control, galvanometer control, and more. The key requirements for such applications is resolution, monotonicity, settling time, and code-to-code glitch. 图 62 provides a simplified circuit of a linear actuator control circuit, wherein the DACx1001 commands the set point and an analog loop controls the actuator.

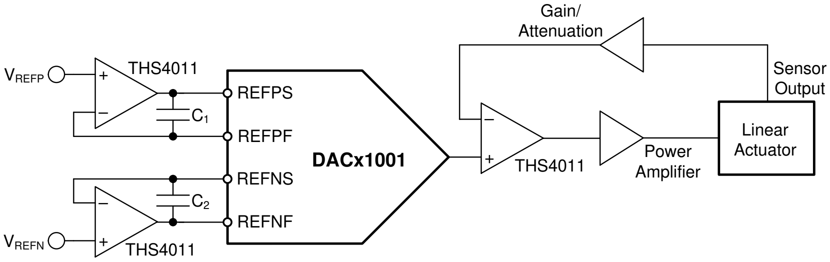


图 62. High-Precision Control Loop

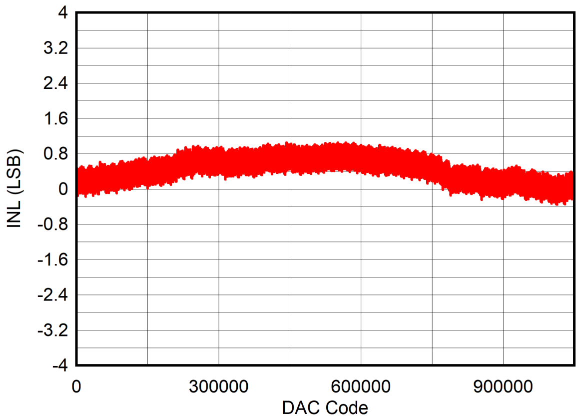
9.2.3.1 Design Requirements

- DNL: ±1 LSB max at 20-bits
- Settling time: < 2 µs
- Code-to-code Glltch: < 2 nV-s

9.2.3.2 Detailed Design Procedure

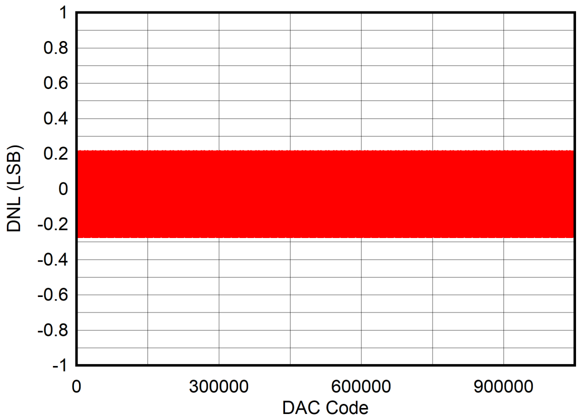
The DACx1001 provides 20-bit monotonic resolution at < ±1 LSB DNL. The device provides < 2 µs setting time and < 2 nV-s code-to-code glitch for major carry transition. The reference and output buffer used for this design is the THS4011, a high-speed amplifier with a 90-ns settling time. For the best settling response, use C_1 and C_2 between 10 pF to 50 pF.

9.2.3.3 Application Curves



Measured on BP-DAC11001EVM, REF6250 onboard reference source (5 V)

图 63. INL at ±5-V Output



Measured on BP-DAC11001EVM, REF6250 onboard reference source (5 V)

图 64. DNL at ±5-V Output

Typical Application (接下页)

9.2.4 Arbitrary Waveform Generation (AWG)

Arbitrary waveform generation circuits are common in memory and semiconductor test equipment. These circuits are used to generate reference ac waveforms to test semiconductor devices. The key performance parameters of such circuits are THD, SNR, and the update rate. 图 65 shows the basic building block example of an AWG circuit using the DACx1001.

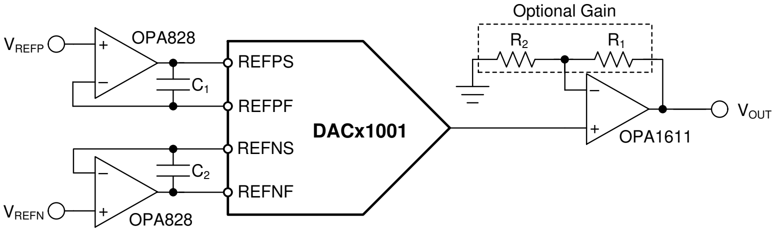


图 65. Arbitrary Waveform Generation

9.2.4.1 Design Requirements

- THD at 1 kHz: > –105 dB
- Update rate: 100 kHz

9.2.4.2 Detailed Design Procedure

The DACx1001 provides a THD of –105 dB at 1 kHz. The device provides update rates of up to 1 MHz, with marginal degradation in THD at higher frequencies. The OPA828 provides the best balance between the voltage and current noise densities, and is therefore an excellent choice to use as reference buffers. The OPA1611 is a low-distortion amplifier for high-THD applications.

9.2.4.3 Application Curves

The test conditions for the THD values in the graph of 图 66 are a ±3-V reference input on the BP-DAC11001EVM, and an external 3x gain at the DAC output. The THD calculation considers 11 harmonics; the even harmonics are omitted. When two DACs are used in a differential output mode, the even harmonics are cancelled to a large extent. 图 66 shows an ideal scenario, when the even harmonics are completely cancelled out.

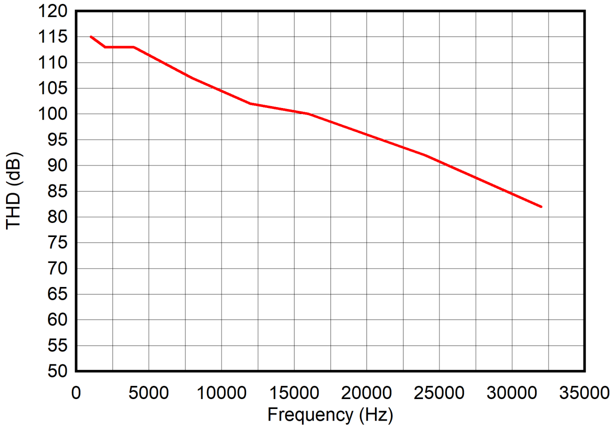


图 66. THD vs Frequency

9.3 System Examples

This section provides details on the digital interface and the embedded resistor configurations.

9.3.1 Interfacing to a Processor

The DACx1001 family of DACs works with a 4-wire SPI interface. The digital interface of the DACx1001 to a processor is shown in 图 67. The DACx1001 has an LDAC input option for synchronous output update. In ac-signal generation applications, the jitter in the LDAC signal contributes to signal-to-noise ratio (SNR). Therefore, the LDAC signal must be generated from a low-jitter timer in the processor. The CLR and ALARM pins are static signals, and therefore can be connected to general-purpose input-output (GPIO) pins on the processor. All active-low signals (SYNC, LDAC, CLR, and ALARM) must be pulled up to IOVDD using 10-kΩ resistors. ALARM is an output pin from the DAC, so the corresponding GPIO on the processor must be configured as an input. Either poll the GPIO, or configured the GPIO as an interrupt to detect any failure alarm from the DAC. When using a high SCLK frequency, use source termination resistors, as shown in Interfacing to a Processor. Typically, 33-Ω resistors work on printed circuit boards (PCBs) with a 50-Ω trace impedance.

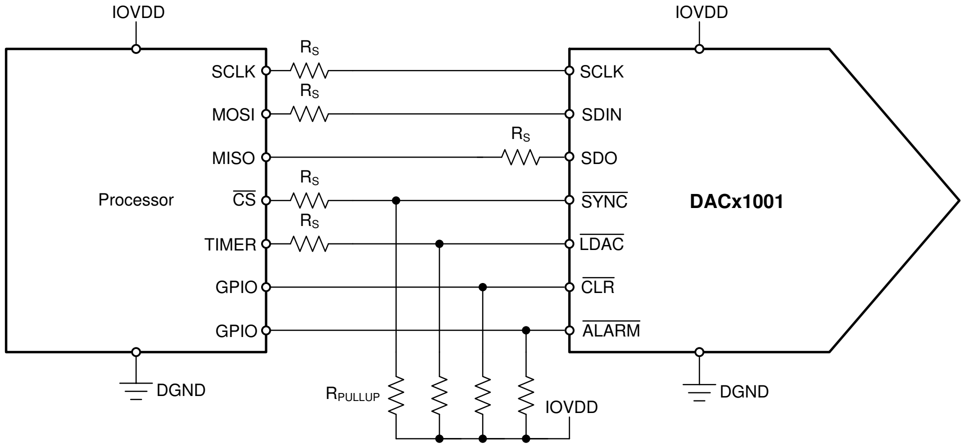


图 67. Interfacing to a Processor

9.3.2 Interfacing to a Low-Jitter LDAC Source

When the processor is not able to provide a low-jitter source for the LDAC signal, an external low-jitter LDAC source can be used, as shown in 图 68. The processor can take the LDAC signal as an interrupt and trigger the SPI frame synchronously.

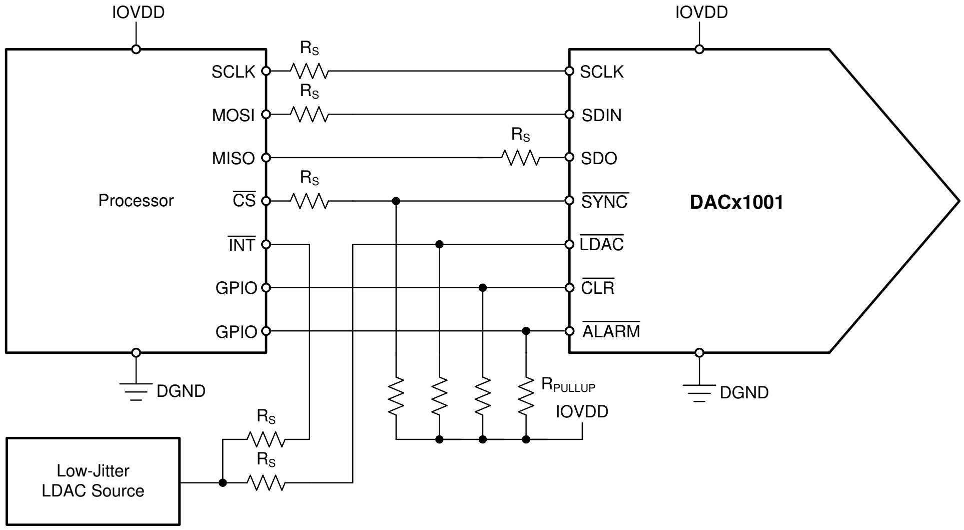


图 68. Interfacing to an External LDAC Source

System Examples (接下页)

9.3.3 Embedded Resistor Configurations

The DACx1001 provides two embedded resistors with values is double the value of the output impedance of the R2R ladder. These resistors can be used in various configurations, as shown in the following subsections.

9.3.3.1 Minimizing Bias Current Mismatch

The bias current mismatch in the output amplifier can lead to offset error at the output. To minimize mismatch, the amplifier must have a matching resistor to that of the R2R output impedance on the feedback path. The feedback resistors are used in parallel for this purpose, as shown in 图 69. Some amplifiers may become unstable with a feedback resistor in the buffer configuration. Therefore, a compensation capacitor (C_{COMP}) might be needed, as shown. The typical value of this capacitor is in the range of 22 pF to 100 pF, depending on the amplifier.

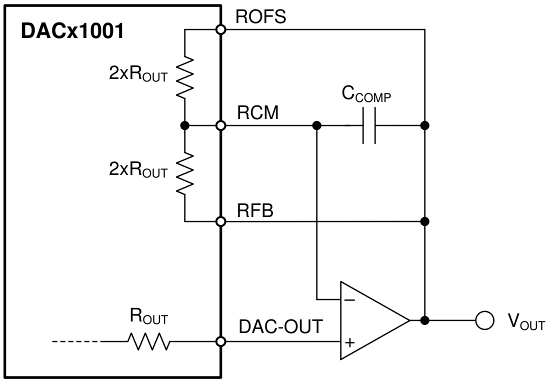


图 69. Minimizing Bias Current Mismatch

9.3.3.2 2x Gain configuration

The circuit of 图 69 can be configured for 2x gain by connecting one of the resistor ends to ground, as shown in 图 70.

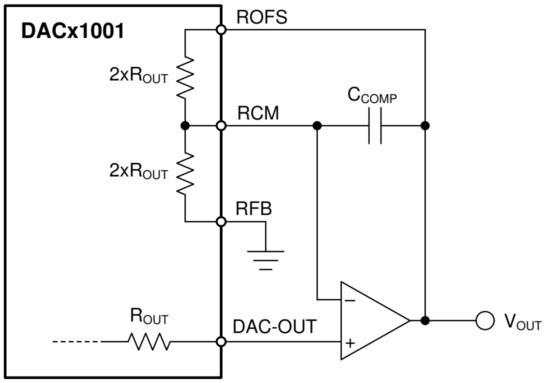


图 70. 2x Gain Configuration

System Examples (接下页)

9.3.3.3 Generating Negative Reference

Generating a negative reference is a challenge because of the fact that the circuit needs an inverting amplifier involving resistors. The resistor mismatch and temperature drift can lead to inaccuracy. The embedded, matched resistors in DACx1001 can be used as shown in 图 71, the inverting amplifier configuration, to generate an accurate negative reference voltage.

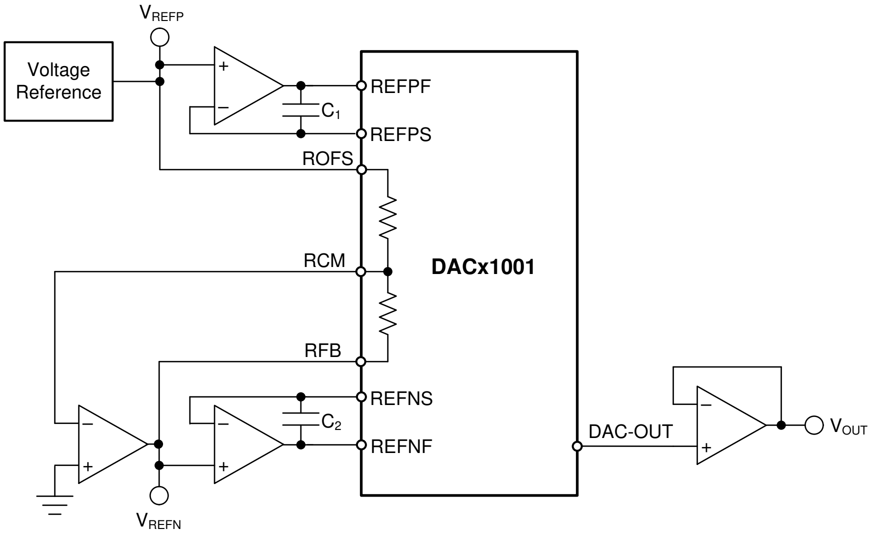


图 71. Generating Negative Reference

9.4 What to Do and What Not to Do

9.4.1 What to Do

- Follow recommended grounding, decoupling, and layout schemes for achieving best accuracy.
- Use a low-jitter $\overline{\text{LDAC}}$ source for best ac performance.
- Choose the appropriate amplifiers depending on the application requirements as explained in above sections.

9.4.2 What Not to Do

- Do not apply the reference before the DAC power supplies are powered on.
- Do not use the reference source directly with the DAC reference inputs without using buffers. or else the accuracy drastically degrades.

9.5 Initialization Set Up

The following text shows the pseudocode to get started with the DACx1001:

```
//SPI Settings
//Mode: Mode-1 (CPOL: 0, CPHA: 1)
//CS Type: Active Low, Per Packet
//Frame length: 32
//SYNTAX: WRITE <REGISTER (HEX ADDRESS>, <HEX DATA>
//Select VREF, TnH mode (Good THD), LDAC mode and power-up the DAC
WRITE CONFIG (0x02), 0x004C80
//Write zero code to the DAC
WRITE DACDATA (0x01), 0x000000
//Write mid code to the DAC
WRITE DACDATA (0x01), 0x7FFFF0
//Write full code to the DAC
WRITE DACDATA (0x01), 0xFFFFF0
```

10 Power Supply Recommendations

To get the best performance out of the DACx1001, the power supply, grounding, and decoupling are very important. Use a PCB with a ground-plane reference, which helps in confining the digital return currents. A low mutual inductance path is created just beneath the high-frequency digital traces causing the return currents to follow the respective signal traces, thus minimizing crosstalk. On the other hand, dc signals spread over the ground plane without being confined below the signal trace. Therefore, in precision dc applications, limiting the common-impedance coupling is very difficult unless the ground planes are physically separated. 图 72 shows a method to divide the grounds so that there is no common-mode current flow between the grounds, while maintaining the same dc potential across all grounds. This circuit assumes that the REFGND and LOAD-GND are provided from isolated power sources, therefore, there is no common-mode current flow through the reference or the load.

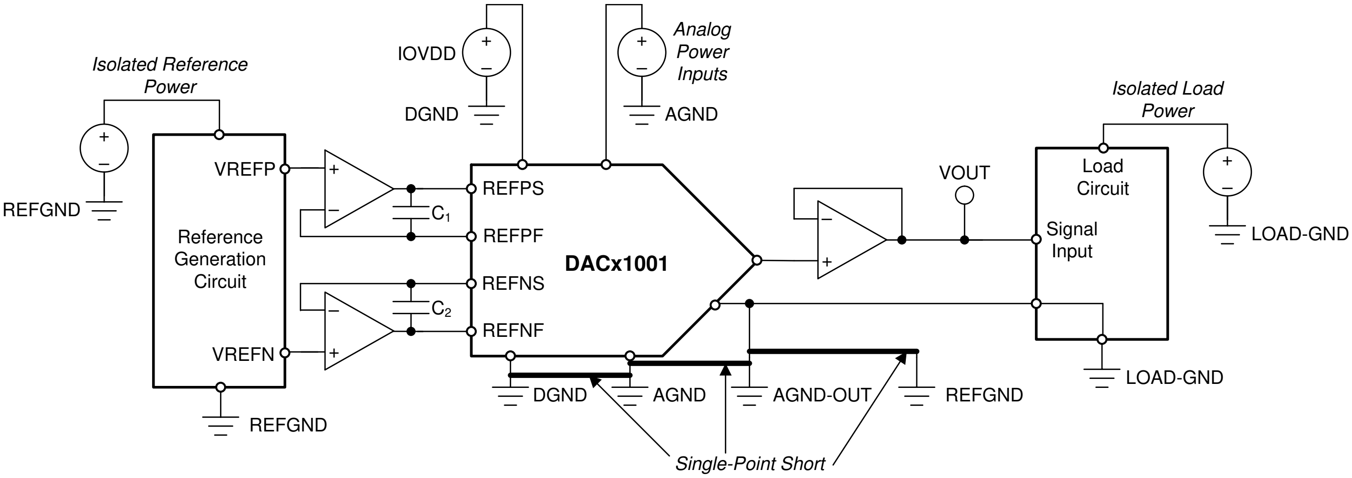


图 72. Power and Signal Grounding

When the load circuit is powered from a source referenced to AGND, and the LOAD-GND is shorted to AGND at the far end, the AGND-OUT must no longer be shorted to AGND locally near the DAC. The local shorting creates a ground loop, otherwise. The resulting connection that avoids the ground loop is shown in 图 73.

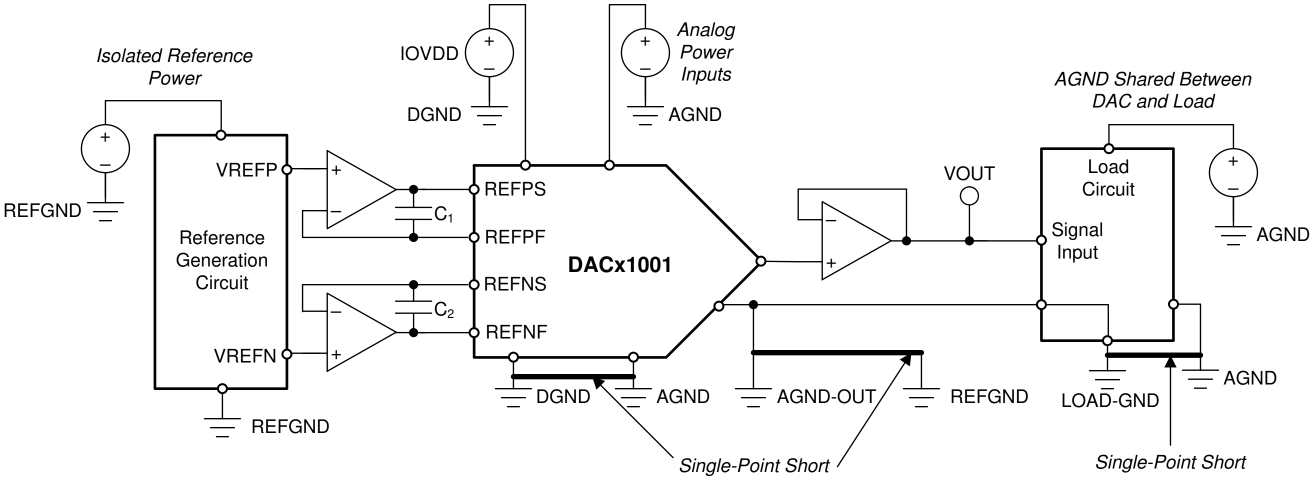


图 73. Grounding Scheme When AGND is Load Ground

When the reference source is powered from a power source with AGND as the ground, there is a possibility of common-impedance coupling causing a code-dependent shift in the reference voltage. To avoid undesired coupling, drive REFGND using a buffer that maintains the reference ground potential equals to that of AGND-OUT, as shown in 图 74.

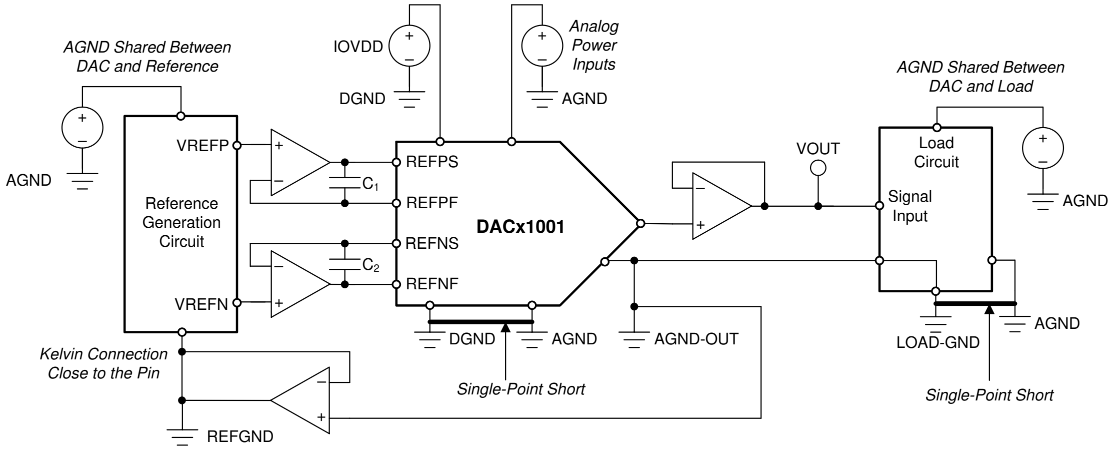


图 74. Connecting the Reference Ground

Channel-to-channel dc crosstalk is a major concern in multichannel applications, such as battery test equipment. While the DACx1001 is single-channel, the crosstalk problem can appear at a system level when using multiple DACx1001 devices. The problem becomes severe when the grounds of the loads are shorted together creating a possible ground loop. In such cases, avoid the local short between AGND and AGND-OUT. Use a single short between AGND and DGND for all the DACs. If the PCB layout allows for the digital signal and analog power supplies to be kept separate, DGND and AGND can be combined to a single ground plane. 图 75 shows an example circuit for minimizing dc crosstalk across DAC channels in a system.

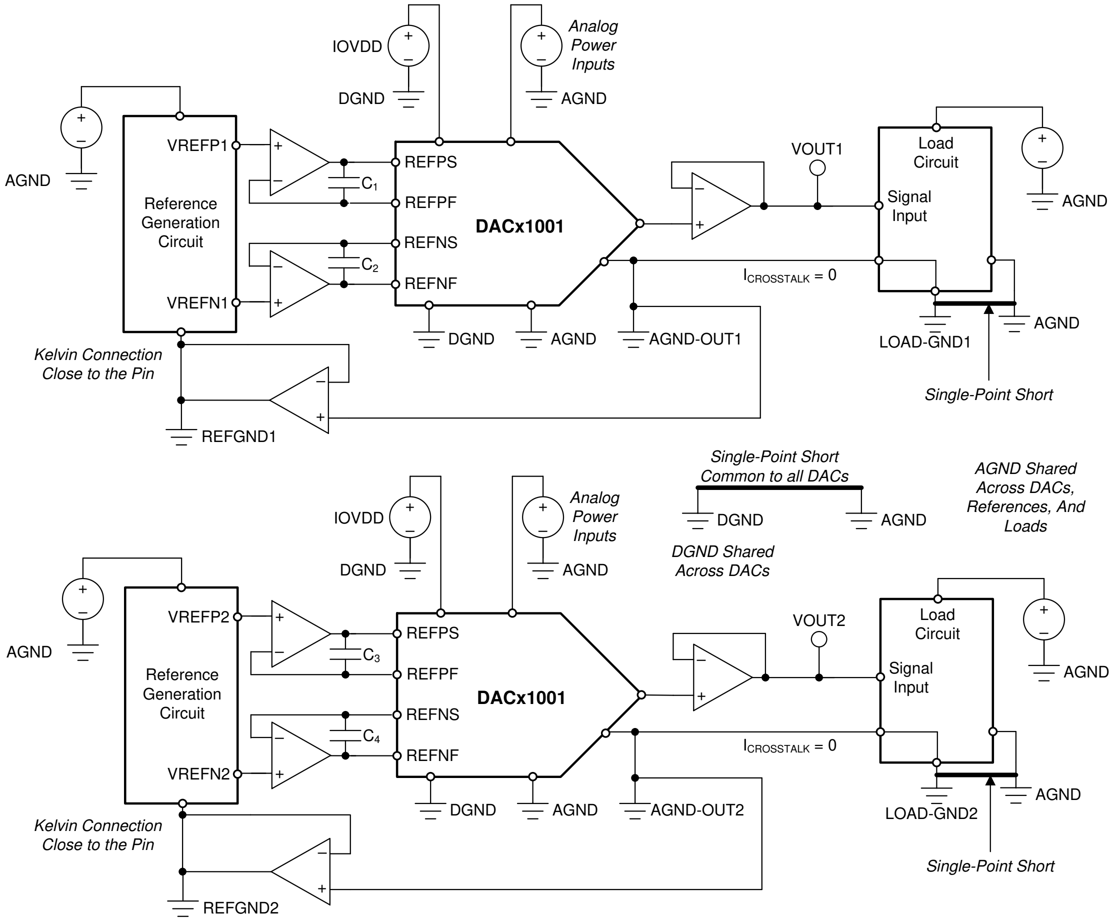


图 75. Minimizing Multichannel DC Crosstalk

Power-supply bypassing and decoupling is key to keep power supply noise, switching transients, and common-mode currents away from the DAC output. There are three main objective of power-supply bypassing:

- *Filtering*: Filter out noise and ripple from power supplies
- *Bypassing*: Supply switching or load transient currents locally by avoiding trace inductances
- *Decoupling*: Stop local transient currents from impacting other circuits

To achieve these objectives, use the following 3-element scheme. Place a decoupling capacitor close to every power supply pin to provide the local current path for load and circuit switching transients. This capacitor must be referenced to the respective load ground for best load transient suppression. Use a 0.1-µF to 1-µF, X7R, multilayer ceramic capacitor (MLCC) for this purpose. For analog power supplies, a 10-Ω series resistor provides the best decoupling. For filtering the power supply noise and ripple, 10-µF capacitors work best when placed at the power entry point of the board. An example decoupling scheme is shown in 图 76.

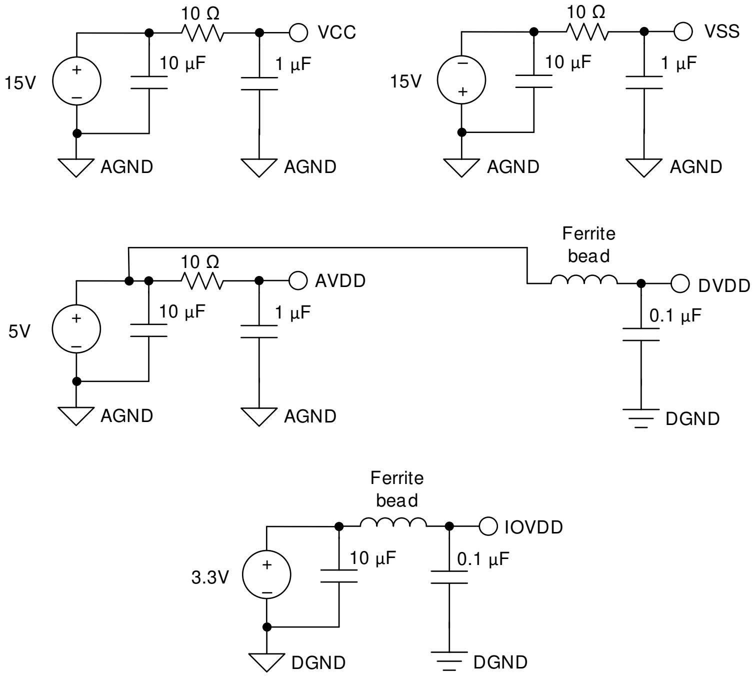


图 76. Power-Supply Decoupling

10.1 Power-Supply Sequencing

The DACx1001 do not require any power-supply sequence. However, the power supplies to the AVDD pin must be capable of providing 30-mA of current if V_{SS} ramps before AV_{DD}. This current is derived from the AVDD pin, and flows out of the VSS pin. This condition is transient, and the device stops consuming this current when the power supplies are ramped up. To avoid this condition, make sure to ramp AV_{DD} before V_{SS}.

11 Layout

11.1 Layout Guidelines

PCB layout plays a significant role for achieving desired ac and dc performance from the DACx1001. The DACx1001 has a pinout that supports easy splitting of the noisy and quiet grounds. The digital signals are available on two adjacent sides of the device; whereas, the power and analog signals are available separate sides. 图 77 shows an example layout, where the different ground planes have been clearly demarcated. The figure also shows the best positions for the single-point shorts between the ground planes. For best power-supply bypassing, place the bypass capacitors close to the respective power pins as shown. Provide unbroken ground reference planes for the digital signal traces, especially for the SPI and LDAC signals.

11.2 Layout Example

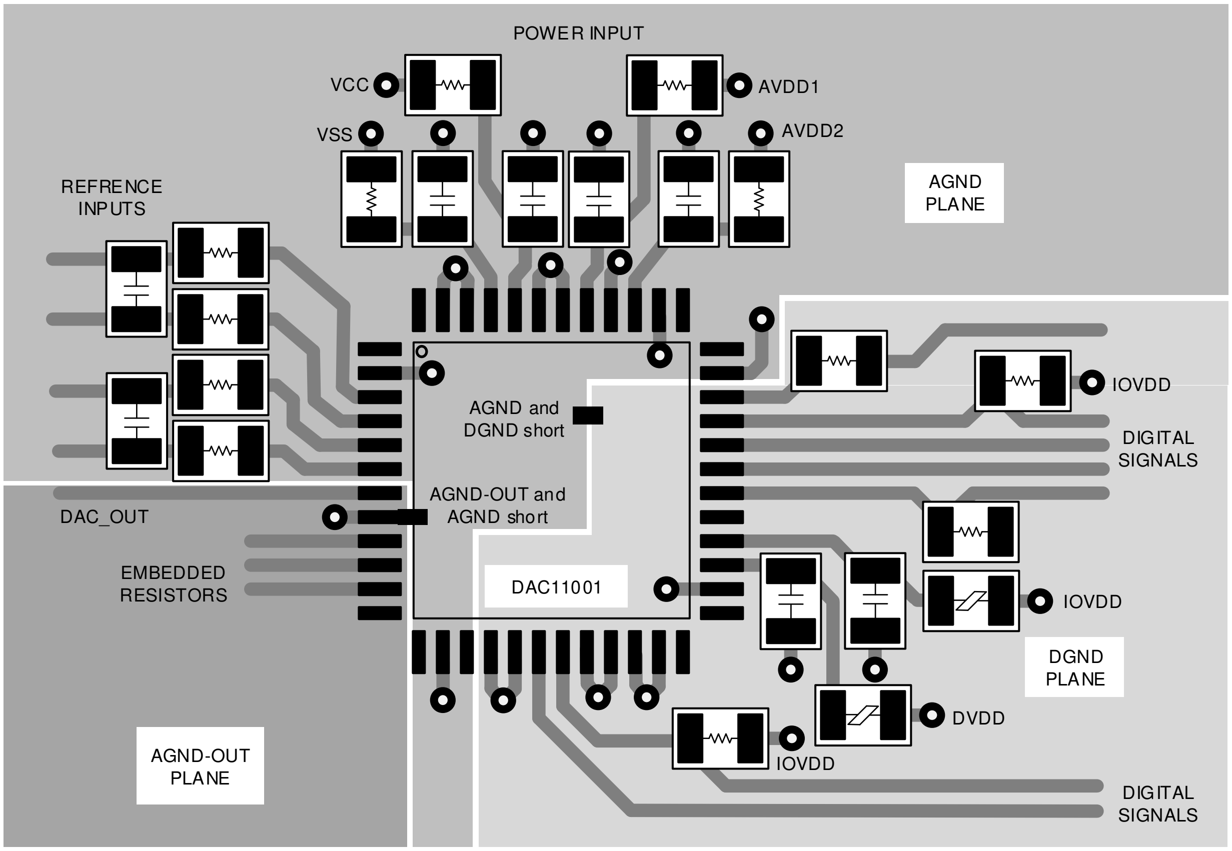


图 77. Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

BP-DAC11001 评估模块

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《BP-DAC11001EVM 用户指南》*
- 德州仪器 (TI)，*《代码对代码干扰在精密 应用 中产生的影响》*应用简介

12.3 相关链接

表 12 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具与软件，以及立即订购快速访问。

表 **12.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
DAC11001A	单击此处	单击此处	单击此处	单击此处	单击此处
DAC91001	单击此处	单击此处	单击此处	单击此处	单击此处

12.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.5 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC11001APFBR	ACTIVE	TQFP	PFB	48	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	DAC11001A	Samples
DAC11001APFBT	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	DAC11001A	Samples
DAC81001PFBR	ACTIVE	TQFP	PFB	48	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	DAC81001	Samples
DAC81001PFBT	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	DAC81001	Samples
DAC91001PFBR	ACTIVE	TQFP	PFB	48	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	DAC91001	Samples
DAC91001PFBT	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	DAC91001	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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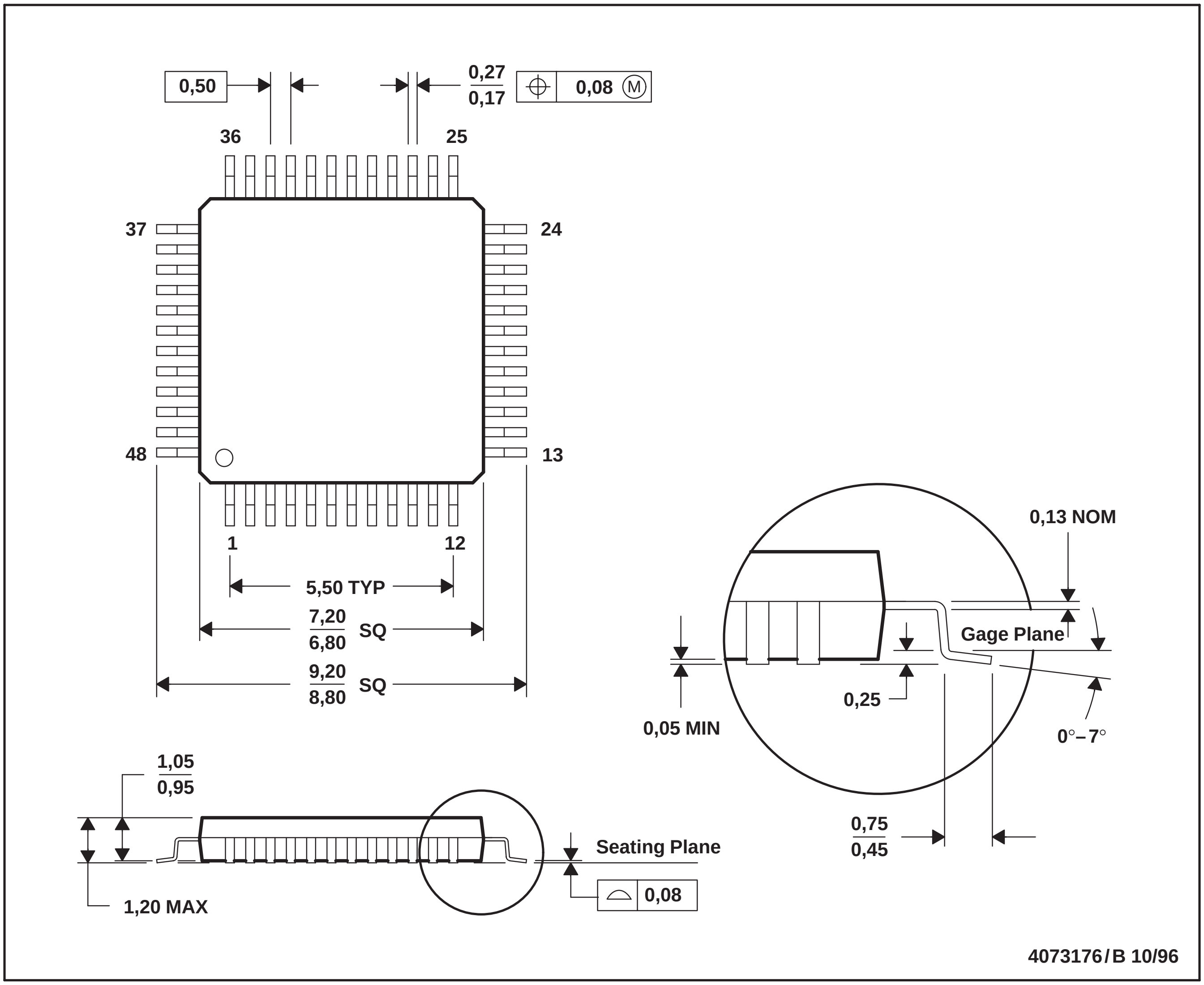

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026

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