

TPS65835

与联合 MSP430 的先进的 PMU 用于有源快门3D 眼镜

Data Manual



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查询样品: [TPS65835](#)

1 介绍

1.1 特性

- 电源管理内核
 - 线性充电器
 - 三个充电阶段: 预充电、快速充电和充电终止
 - 用于电源状态良好和充电器状态指示的 **LED** 电流吸收器
 - **LDO** 电源用于为外部模块和集成型 **MSP430** 供电
 - 升压转换器
 - 可调输出电压: **8 V 至 16 V**
 - 全 **H** 桥模拟开关
 - 由 **MSP430** 内核进行内部控制以实现系统功能
- **MSP430** 内核
 - 超低功耗
 - 运行模式: **280µA** (在 **1MHz** 频率和 **2.2V** 电压条件下)
 - 待机模式: **0.5µA**
 - 关断模式 (**RAM** 保持): **0.1µA**
- **5** 种节能模式
- **16** 位 **RISC** 架构
- **16 kB** 闪存
- 具有 **3** 个捕获/比较寄存器的两个 **16** 位 **Timer_A** 模块
- 带内部基准、采样与保持以及自动扫描功能的 **10** 位 **200-ksps** 模数 (**A/D**) 转换器
- 通用串行通信接口, 支持 **IrDA** 编码/解码的同步 **SPI**
 - 增强型 **UART** 可支持自动波特率检测 (**LIN**)
 - **IrDA** 编码器和解码器
 - 同步 **SPI**
 - **I²C™**
- 串行板上编程
 - 无需从外部进行电压编程
 - 利用安全熔丝 (**Security Fuse**) 实现可编程代码保护
- 如需了解完整的模块说明, 请查阅 **MSP430x2xx** 系列用户指南 (文献编号 [SLAU144](#))

1.2 说明

TPS65835 是一款用于有源快门 3D 眼镜的电源管理单元 (PMU), 包括一个电源管理内核和一个 MSP430 微控制器。电源管理内核具有集成型电源通路、线性充电器、LDO、升压转换器以及用于在一副有源快门 3D 眼镜中实现左右快门操作的全 H 桥模拟开关。MSP430 内核支持通过集成型通用串行通信和定时器接口从一个 IR、RF 或其他通信模块实现同步及通信, 以支持电源管理内核上的 H 桥开关的操作。



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1.3 方框图

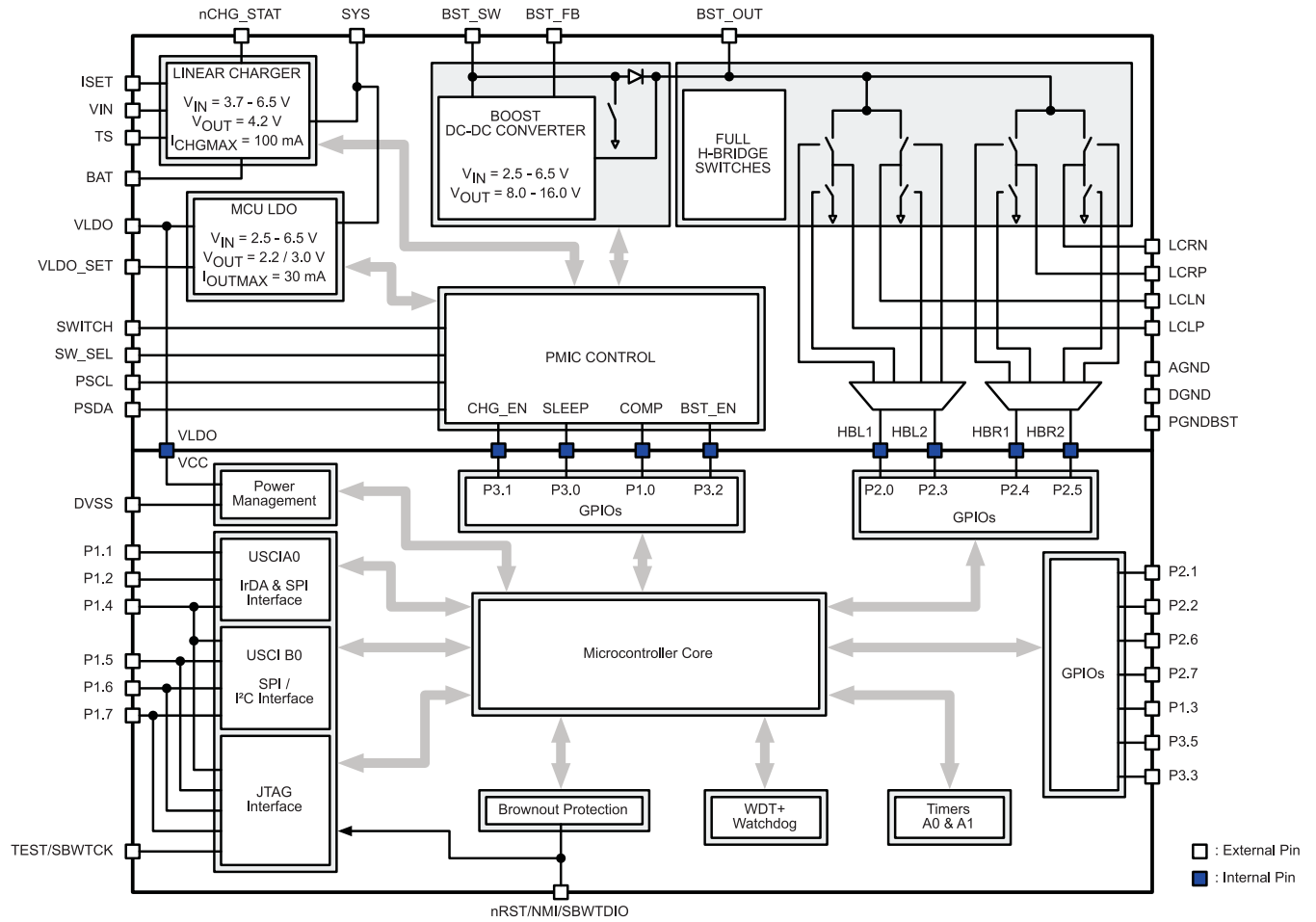


图 1-1. TPS65835 的简化原理框图

1.4 引脚说明

表 1-1. 引脚说明

引脚名称	I/O	引脚序号	说明
电源管理内核 (PMIC)			
VIN	I	26	AC 或 USB 适配器输入
ISET	I/O	18	快速充电电流设定电阻器
TS	I	19	Pin for 10 kΩ NTC Thermistor Connection FLOAT IF THERMISTOR / TS FUNCTION IS NOT USED
nCHG_STAT	O	38	Open-drain Output, Charger Status Indication CONNECT TO GROUND IF FUNCTION IS NOT USED
BAT	I/O	22	充电器功率级输出和电池电压感测输入
SYS	O	23	至系统的输出端
VLDO	O	27	LDO 输出
VLDO_SET	I	28	Sets LDO Output Voltage (see 表 2-2)
开关	I	33	用于器件接通/关断的开关输入
SW_SEL	I	35	Selects Type of Switch Connected to SWITCH Pin (see 表 2-6)
BST_SW	I	12	升压开关节点
BST_FB	I	15	升压反馈节点
BST_OUT	O	11	升压输出
LCRN	O	8	用于右 LC 快门的 H 桥输出, “负(-)”端子
LCRP	O	7	用于右 LC 快门的 H 桥输出, “正(+)”端子
LCLN	O	6	用于左 LC 快门的 H 桥输出, “负(-)”端子
LCLP	O	5	用于左 LC 快门的 H 桥输出, “正(+)”端子
PSCL	I/O	37	I ² C Clock Pin (only used for TI debug and test) GROUND PIN IN APPLICATION
PSDA	I/O	36	I ² C Data Pin (only used for TI debug and test) GROUND PIN IN APPLICATION
PGNDBST	-	14	PMIC 升压电源地 ⁽¹⁾
AGND	-	29	PMIC 模拟地 ⁽¹⁾
DGND	-	4	PMIC 数字地 ⁽¹⁾
MSP430 微控制器			
P1.1/ TA0.0/ UCA0RXD/ UCA0SOMI/ A1/ CA1	I/O	30	General-purpose digital I/O pin Timer0_A, capture: CCI0A input, compare: Out0 output USCI_A0 receive data input in UART mode USCI_A0 slave data out/master in SPI mode ADC10 analog input A1 Comparator_A+, CA1 input
P1.2/ TA0.1/ UCA0TXD/ UCA0SIMO/ A2/ CA2	I/O	31	General-purpose digital I/O pin Timer0_A, capture: CCI1A input, compare: Out1 output USCI_A0 transmit data output in UART mode USCI_A0 slave data in/master out in SPI mode ADC10 analog input A2 Comparator_A+, CA2 input
P1.3/ ADC10CLK/ A3 VREF-/VEREF-/ CA3/ CAOUT	I/O	32	General-purpose digital I/O pin ADC10, conversion clock output ADC10 analog input A3 ADC10 negative reference voltage Comparator_A+, CA3 input Comparator_A+, output
P1.4/ SMCLK/ UCB0STE UCA0CLK/ A4 VREF+/VEREF+/ CA4 TCK	I/O	34	General-purpose digital I/O pin SMCLK signal output USCI_B0 slave transmit enable USCI_A0 clock input/output ADC10 analog input A4 ADC10 positive reference voltage Comparator_A+, CA4 input JTAG test clock, input terminal for device programming and test

(1) MSP430 的地与 PMIC (电源管理内核) 的地在内部连接。

表 1-1. 引脚说明 (continued)

引脚名称	I/O	引脚序号	说明
P1.5/ TA0.0/ UCB0CLK/ UCA0STE/ A5/ CA5/ TMS	I/O	39	General-purpose digital I/O pin Timer0_A, compare: Out0 output USCI_B0 clock input/output USCI_A0 slave transmit enable ADC10 analog input A5 Comparator_A+, CA5 input JTAG test mode select, input terminal for device programming and test
P1.6/ TA0.1/ A6/ CA6/ UCB0SOMI/ UCB0SCL/ TDI/TCLK	I/O	13	General-purpose digital I/O pin Timer0_A, compare: Out1 output ADC10 analog input A6 Comparator_A+, CA6 input USCI_B0 slave out/master in SPI mode USCI_B0 SCL I2C clock in I2C mode JTAG test data input or test clock input during programming and test
P1.7/ A7/ CA7/ CAOUT/ UCB0SIMO/ UCB0SDA/ TDO/TDI	I/O	16	General-purpose digital I/O pin ADC10 analog input A7 Comparator_A+, CA7 input Comparator_A+, output USCI_B0 slave in/master out in SPI mode USCI_B0 SDA I2C data in I2C mode JTAG test data output terminal or test data input during programming and test ⁽²⁾
P2.1/ TA1.1	I/O	1	General-purpose digital I/O pin Timer1_A, capture: CC1A input, compare: Out1 output
P2.2/ TA1.1	I/O	2	General-purpose digital I/O pin Timer1_A, capture: CC1B input, compare: Out1 output
P2.6/ XIN/ TA0.1	I/O	24	General-purpose digital I/O pin XIN, Input terminal of crystal oscillator TA0.1, Timer0_A, compare: Out1 output
P2.7/ XOUT	I/O	21	General-purpose digital I/O pin Output terminal of crystal oscillator ⁽³⁾
P3.3/ TA1.2	I/O	3	General-purpose digital I/O pin Timer1_A, compare: Out2 output
P3.5/ TA0.1	I/O	9	General-purpose digital I/O pin Timer0_A, compare: Out0 output
nRST/ NMI/ SBWTDIO	I/O	17	Reset Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTKK	I	20	选择针对端口 1 上的 JTAG 引脚的测试模式。器件保护熔丝连接至 TEST。 编程及测试期间的两线式 JTAG (Spy-Bi-Wire) 测试时钟输入
DVSS	-	25	MSP430 接地参考 ⁽⁴⁾
MISC. 及封装			
Thermal PAD	-	41	在裸露散热焊盘与器件的 AGND 接地引脚之间布设了一根内部电气连接线。散热焊盘必须连接至与印刷电路板上的 AGND 引脚相同的电位。不要将散热焊盘用作器件的主要接地输入。AGND 引脚必须始终连接至地。
悬空	-	10, 40	所有的悬空 (N/C) 引脚在内部均未连接 (封装至晶片)。应把它们连接至主系统地。

(2) TDO 或 TDI 通过 JTAG 指令来选择。

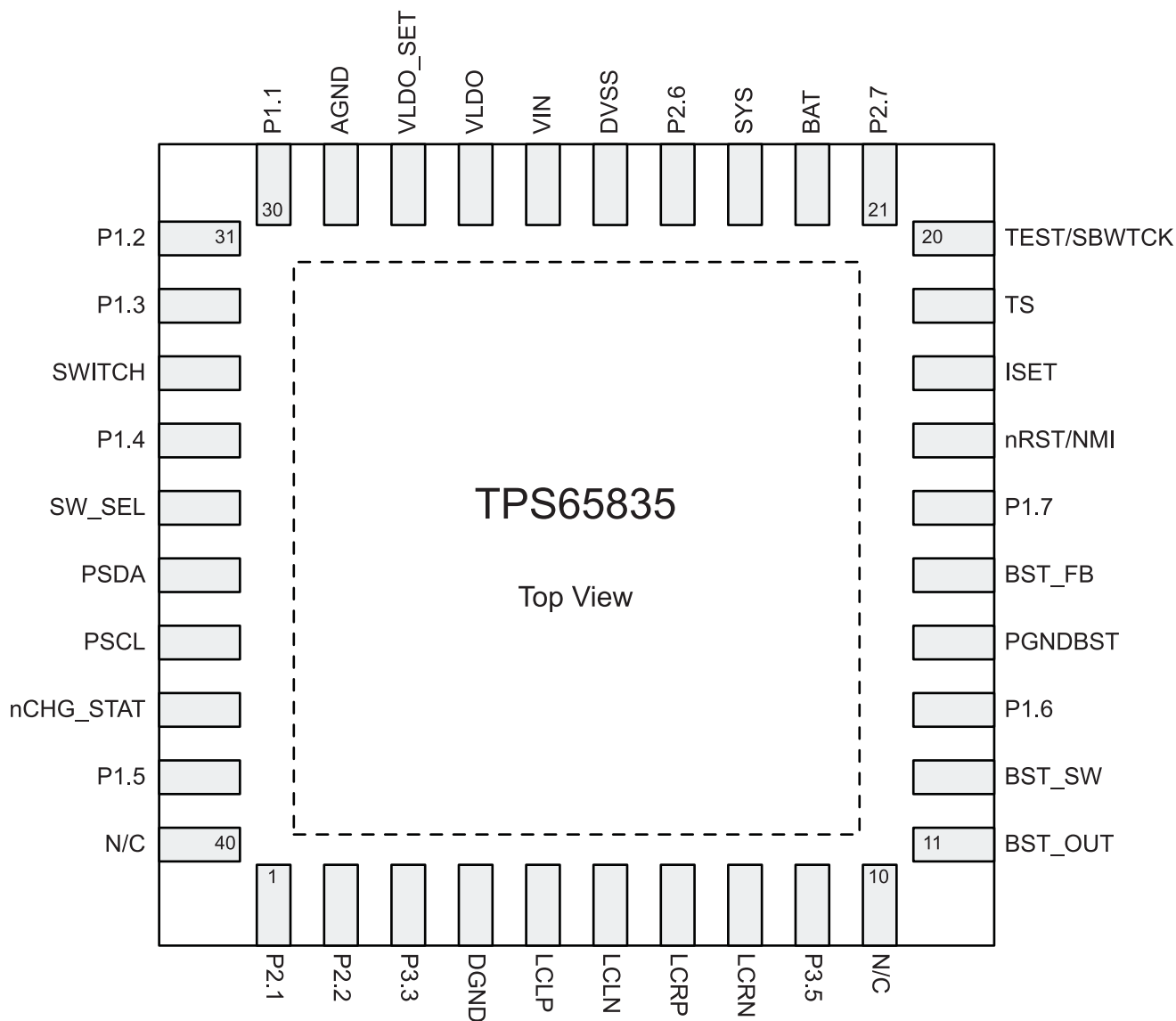
(3) 如果 P2.7 用作一个输入, 则将产生过大的电流, 直到 P2SEL.7 被清除为止。这是由于复位之后振荡器输出驱动器连接至该焊盘所致。

(4) MSP430 的地与 PMIC (电源管理内核) 的地在内部连接。

表 1-2. 引脚的最大绝对额定值

引脚	数值/单位
所有引脚 (VIN、BST_OUT、BST_SW、BST_FB、VLDO、LCLP、LCLN、LCRP、LCRN、AGND、DGND、PGNDBS T 及 MSP430 内核引脚除外) 的输入电压范围均以 AGND 为基准	-0.3 V 至 7.0 V
VIN (相对于 AGND)	-0.3 V 至 28.0 V
BST_OUT、BST_SW (相对于 PGNDBST)	-0.3 V 至 18.0 V
BST_FB (相对于 PGNDBST), VLDO (相对于 DGND)	-0.3 V 至 3.6 V
MSP430 内核引脚	-0.3 V 至 4.1 V

1.5 封装引脚分布



Pins 10 & 40 = N/C. No internal connection, connect to main system ground.

图 1-2. TPS65835 封装引脚分布

2 POWER MANAGEMENT CORE

2.1 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

SUBSYSTEM AND PARAMETER		MIN	NOM	MAX	UNIT
CHARGER / POWER PATH					
V _{VIN}	Voltage range at charger input pin	3.7		28 ⁽¹⁾	V
I _{VIN}	Input current at VIN pin			200	mA
C _{VIN}	Capacitor on VIN pin	0.1	2.2	10	μF
L _{VIN}	Inductance at VIN pin	0		2	μH
V _{SYS}	Voltage range at SYS pin	2.5		6.4	V
I _{SYS(OUT)}	Output current at SYS pin			100	mA
C _{SYS}	Capacitor on SYS pin	0.1	4.7	10	μF
V _{BAT}	Voltage range at BAT pin	2.5		6.4	V
C _{BAT}	Capacitor on BAT pin	4.7		10	μF
R _{EXT(nCHG_STAT)}	Resistor connected to nCHG_STAT pin to limit current into pin	320			Ω
BOOST CONVERTER / H-BRIDGE SWITCHES					
V _{IN(BST_SW)}	Input voltage range for boost converter	2.5		6.5	V
V _{BST_OUT}	Output voltage range for boost converter	8		16	V
C _{BST_OUT}	Boost output capacitor	3.3	4.7	10	μF
L _{BST_SW} ⁽²⁾	Inductor connected between SYS and BST_SW pins	4.7		10 ⁽³⁾	μH
LDO					
C _{VLDO}	External decoupling cap on pin VLDO	1		10	μF
POWER MANAGEMENT CORE CONTROL (LOGIC LEVELS FOR GPIOs)					
V _{IL(PMIC)}	GPIO low level (BST_EN, CHG_EN, SW_SEL, VLDO_SET and to switch H-Bridge inputs to a low, 0, level)			0.4	V
V _{IH(PMIC)}	GPIO high level (BST_EN, CHG_EN, SW_SEL, VLDO_SET and to switch H-Bridge inputs to a high, 1, level)	1.2			V

(1) VIN pin has 28 V ESD protection

(2) See [节 2.9](#) for information on boost converter inductor selection.

(3) Design optimized for boost operation with 10 μH inductor

2.2 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MINIMUM	MAXIMUM	UNITS
Operating free-air temperature, T _A	0	60	°C
Max Junction Temperature, T _J , Electrical Characteristics Guaranteed	0	85	°C
Max Junction temperature, T _J , Functionality Guaranteed ⁽¹⁾	0	105	°C

(1) Device has a thermal shutdown feature implemented that shuts down at 105 °C

2.3 Thermal Information

THERMAL METRIC		TPS65835	UNITS
		RKP	
		40 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽¹⁾	31.9	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽²⁾	22.7	
θ_{JB}	Junction-to-board thermal resistance ⁽³⁾	6.2	
Ψ_{JT}	Junction-to-top characterization parameter ⁽⁴⁾	0.3	
Ψ_{JB}	Junction-to-board characterization parameter ⁽⁵⁾	6.1	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁶⁾	1.4	

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter, Ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter, Ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

2.4 Quiescent Current

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q(SLEEP)}$	Power management core quiescent current in sleep mode	@ 25° C $V_{BAT} = 3.6$ V $V_{VIN} = 0$ V No load on LDO CHG_EN, BST_EN grounded BST_FB = 300 mV Power management core in sleep mode / device 'off'		8.6	10.5	μA
$I_{Q(ACTIVE)}$	Power management core quiescent current in active mode	@ 25° C $V_{BAT} = 3.6$ V $V_{VIN} = 0$ V Boost enabled but not switching, H-bridge in grounded state No load on LDO Power management core in active mode		39	53.5	μA

2.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER POWER PATH						
$V_{UVLO(VIN)}$	Undervoltage lockout at power path input, VIN pin	$V_{VIN}: 0$ V → 4 V	3.2	3.3	3.45	V
$V_{HYS-UVLO(VIN)}$	Hysteresis on UVLO at power path input, VIN pin	$V_{VIN}: 4$ V → 0 V	200		300	mV
V_{IN-DT}	Input power detection threshold	Input power detected if: ($V_{VIN} > V_{BAT} + V_{IN-DT}$); $V_{BAT} = 3.6$ V $V_{VIN}: 3.5$ V → 4 V	40		140	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT}	$V_{BAT} = 3.6$ V $V_{VIN}: 4$ V → 3.5 V	20			mV

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OVP}	Input over-voltage protection threshold	V _{VIN} : 5 V → 7 V	6.4	6.6	6.8	V
V _{HYS-OVP}	Hysteresis on OVP	V _{VIN} : 11 V → 5 V		105		mV
V _{DO(VIN-SYS)}	VIN pin to SYS pin dropout voltage V _{VIN} – V _{SYS}	I _{SYS} = 150 mA (including I _{BAT}) V _{VIN} = 4.35 V V _{BAT} = 3.6 V			350	mV
V _{DO(BAT-SYS)}	BAT pin to SYS pin dropout voltage V _{BAT} – V _{SYS}	I _{SYS} = 100 mA V _{VIN} = 0 V V _{BAT} > 3 V			150	mV
I _{VIN(MAX)}	Maximum power path input current at pin VIN	V _{VIN} = 5 V		200		mA
V _{SUP(ENT)}	Enter battery supplement mode			V _{SYS} ≤ (V _{BAT} - 40 mV)		V
V _{SUP(EXIT)}	Exit battery supplement mode			V _{SYS} ≥ (V _{BAT} - 20 mV)		V
V _{SUP(SC)}	Output short-circuit limit in supplement mode			250		mV
V _{O(SC)}	Output short-circuit detection threshold, power-on			0.9		V
BATTERY CHARGER						
I _{CC}	Active supply current into VIN pin	V _{VIN} = 5 V No load on SYS pin V _{BAT} > V _{BAT(REG)}			2	mA
I _{BAT(SC)}	Source current for BAT pin short-circuit detection			1		mA
V _{BAT(SC)}	BAT pin short-circuit detection threshold		1.6	1.8	2.0	V
V _{BAT(REG)}	Battery charger output voltage		-1%	4.20	1%	V
V _{LOWV}	Pre-charge to fast-charge transition threshold		2.9	3.0	3.1	V
I _{CHG}	Charger fast charge current range I _{CHG} = K _{ISET} / R _{ISET}	V _{VIN} = 5 V V _{BAT(REG)} > V _{BAT} > V _{LOWV}		5	100	mA
K _{ISET}	Battery fast charge current set factor I _{CHG} = K _{ISET} / R _{ISET}	V _{VIN} = 5 V I _{VIN(MAX)} > I _{CHG} I _{CHG} = 100 mA No load on SYS pin, thermal loop not active.	-20%	450	20%	AΩ
I _{PRECHG}	Pre-charge current		0.07 × I _{CHG}	0.10 × I _{CHG}	0.15 × I _{CHG}	mA
I _{TERM}	Charge current value for termination detection threshold	I _{CHG} = 100 mA	7	10	15	mA
V _{RCH}	Recharge detection threshold	V _{BAT} below nominal charger voltage, V _{BAT(REG)}	55	100	170	mV
I _{BAT(DET)}	Sink current for battery detection			1		mA
t _{CHG}	Charge safety timer (18000 seconds = 5 hours)			18000		s
t _{PRECHG}	Pre-charge timer (1800 seconds = 30 minutes)			1800		s
V _{DPPM}	DPPM threshold			V _{BAT} + 100 mV		V
I _{LEAK(nCHG)}	Leakage current for nCHG_STAT pin	V _{nCHG_STAT} = 4.2 V CHG_EN = LOW (Charger disabled)			100	nA
R _{DSON(nCHG)}	On resistance for nCHG_STAT MOSFET switch			20	60	Ω

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{MAX(nCHG)}$	Maximum input current to nCHG_STAT pin				50	mA
BATTERY CHARGER NTC MONITOR						
I_{TSBIAS}	TS pin bias current			75		μ A
V_{COLD}	0°C charge threshold for 10k Ω NTC ($\beta = 3490$)			2100		mV
$V_{HYS(COLD)}$	Low temperature threshold hysteresis	Battery charging and battery / NTC temperature increasing		300		mV
V_{HOT}	50°C charge threshold for 10k Ω NTC ($\beta = 3490$)			300		mV
$V_{HYS(HOT)}$	High temperature threshold hysteresis	Battery charging and battery / NTC temperature decreasing		30		mV
BATTERY CHARGER THERMAL REGULATION						
$T_{J(REG_LOWER)}$	Charger lower thermal regulation limit			75		°C
$T_{J(REG_UPPER)}$	Charger upper thermal regulation limit			95		°C
$T_{J(OFF)}$	Charger thermal shutdown temperature			105		°C
$T_{J(OFF-HYS)}$	Charger thermal shutdown hysteresis			20		°C
LDO						
$I_{MAX(LDO)}$	Maximum LDO output current, $V_{VLDO} = 2.2$ V	$V_{SYS} = 4.2$ V $V_{VIN} = 0$ V $VLDO_SET = 0$ V		30		mA
	Maximum LDO output current, $V_{VLDO} = 3.0$ V	$V_{SYS} = 4.2$ V $V_{VIN} = 0$ V $VLDO_SET = V_{SYS}$		30		mA
$I_{SC(LDO)}$	Short circuit current limit		30		100	mA
V_{VLDO}	LDO output voltage	$VLDO_SET = LOW$ ($VLDO_SET$ pin connected to DGND) 3.7 V $\leq V_{VIN} \leq 6.5$ V $I_{LOAD(LDO)} = -10$ mA	2.13	2.2	2.27	V
V_{VLDO}	LDO output voltage	$VLDO_SET = HIGH$ ($V_{VLDO_SET} = V_{SYS}$) 3.7 V $\leq V_{VIN} \leq 6.5$ V $I_{LOAD(LDO)} = -10$ mA	2.91	3.0	3.09	V
$V_{DO(LDO)}$	LDO Dropout voltage	$V_{VIN} - V_{LDO}$ when in dropout $I_{LOAD(LDO)} = -10$ mA			200	mV
	Line regulation	3.7 V $\leq V_{VIN} \leq 6.5$ V $I_{LOAD(LDO)} = -10$ mA	-1		1	%
	Load regulation	$V_{VIN} = 3.5$ V 0.1 mA $\leq I_{LOAD(LDO)} \leq -10$ mA	-2		2	%
PSRR	Power supply rejection ratio	@20 KHz, $I_{LOAD(LDO)} = 10$ mA $V_{DO(LDO)} = 0.5$ V $C_{VLDO} = 10$ μ F		45		dB
BOOST CONVERTER						
$I_{Q(BST)}$	Boost operating quiescent current	Boost Enabled, $BST_EN = High$ $I_{OUT(BST)} = 0$ mA (boost is not switching) $V_{BAT} = 3.6$ V		2	4.5	μ A
$R_{DS(on)(BST)}$	Boost MOSFET switch on-resistance	$V_{IN(BST)} = 2.5$ V $I_{SW(MAIN)} = 200$ mA		0.8	1.2	Ω

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LKG(BST_SW)}$	Leakage into BST_SW pin (includes leakage into analog h-bridge switches)	BST_EN signal = LOW (Boost disabled) $V_{BST_SW} = 4.2\text{ V}$ No load on BST_OUT pin			90	nA
$I_{SWLIM(BST)}$	Boost MOSFET switch current limit		100	150	200	mA
$V_{DIODE(BST)}$	Voltage across integrated boost diode during normal operation	BST_EN signal = HIGH $V_{BST_SW} = 16.0\text{ V}$ $I_{BST_OUT} = -2\text{ mA}$			1.0	V
$V_{REF(BST)}$	Boost reference voltage on BST_FB pin		1.17	1.2	1.23	V
$V_{REFHYS(BST)}$	Boost reference voltage hysteresis on BST_FB pin		2	2.5	3.2	%
$T_{ON(BST)}$	Maximum on time detection threshold		5	6.5	8	μs
$T_{OFF(BST)}$	Minimum off time detection threshold		1.4	1.75	2.1	μs
$T_{SHUT(BST)}$	Boost thermal shutdown threshold			105		$^{\circ}\text{C}$
$T_{SHUT-HYS(BST)}$	Boost thermal shutdown threshold hysteresis			20		$^{\circ}\text{C}$
FULL H-BRIDGE ANALOG SWITCHES						
$I_{Q(HSW)}$	Operating quiescent current for h-bridge switches				5	μA
$R_{DS(on)(HSW)}$	H-bridge switches on resistance			20	40	Ω
$T_{DELAY(HSW-H)}$	H-bridge switch propagation delay, input switched from low to high state.	$V_{HBxy} = 0\text{ V} \rightarrow V_{VLDO}$		100		ns
$T_{DELAY(HSW-L)}$	H-bridge switch propagation delay, input switched from high to low state.	$V_{HBxy} = V_{VLDO} \rightarrow 0\text{ V}$		100		ns
POWER MANAGEMENT CORE CONTROLLER						
$V_{IL(PMIC)}$	Low logic level for logic signals on power management core (BST_EN, CHG_EN, SLEEP, HBR1, HBR2, HBL1, HBL2)	IO logic level decreasing: $V_{SYS} \rightarrow 0\text{ V}$ $I_{IN} = 1\text{ mA}$			0.4	V
$V_{IH(PMIC)}$	High logic level for signals on power management core (BST_EN, CHG_EN, SLEEP, HBR1, HBR2, HBL1, HBL2)	IO logic level increasing: $0\text{ V} \rightarrow V_{SYS}$ $I_{IN} = 1\text{ mA}$	1.2			V
$V_{GOOD(LDO)}$	Power fault detection threshold	V_{VLDO} decreasing			1.96	V
$V_{GOOD_HYS(LDO)}$	Power fault detection hysteresis	V_{VLDO} increasing		50		mV
$V_{BATCOMP}$	COMP pin voltage (scaled down battery voltage)	$V_{BAT} = 4.2\text{ V}$ $V_{VLDO} = 2.2\text{ V}$		1.85		V
		$V_{BAT} = 2.5\text{ V}$ $V_{VLDO} = 2.2\text{ V}$		1.10		V
		$V_{BAT} = 4.2\text{ V}$ $V_{VLDO} = 3.0\text{ V}$		1.90		V
		$V_{BAT} = 3.3\text{ V}$ $V_{VLDO} = 3.0\text{ V}$		1.50		V

2.6 System Operation

The system must complete the power up routine before it enters normal operating mode. The specific system operation depends on the setting defined by the state of the SW_SEL pin. The details of the system operation for each configuration of the SW_SEL pin are contained in this section.

2.6.1 System Power Up

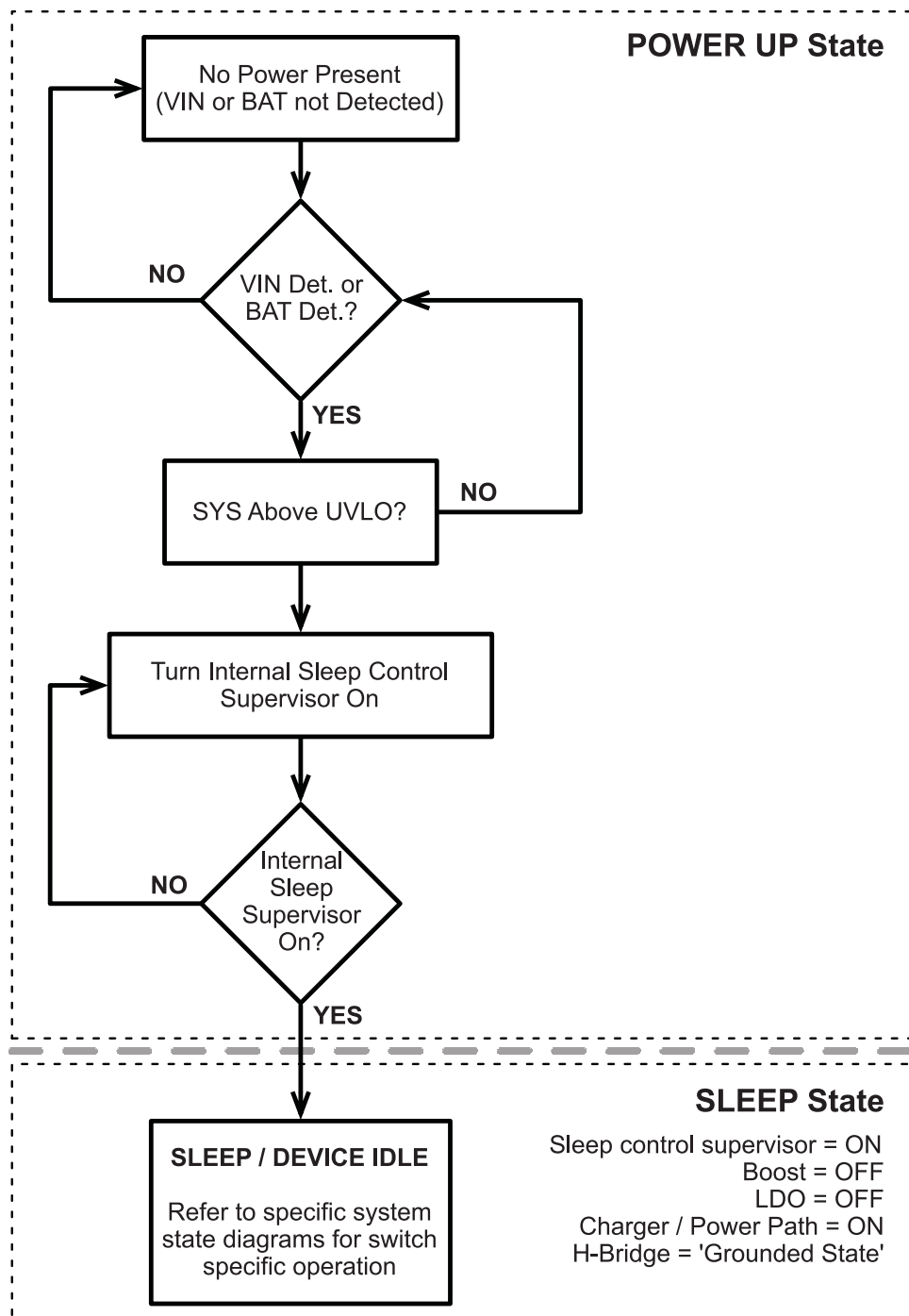


图 2-1. System Power Up State Diagram

2.6.2 System Operation Using Push Button Switch

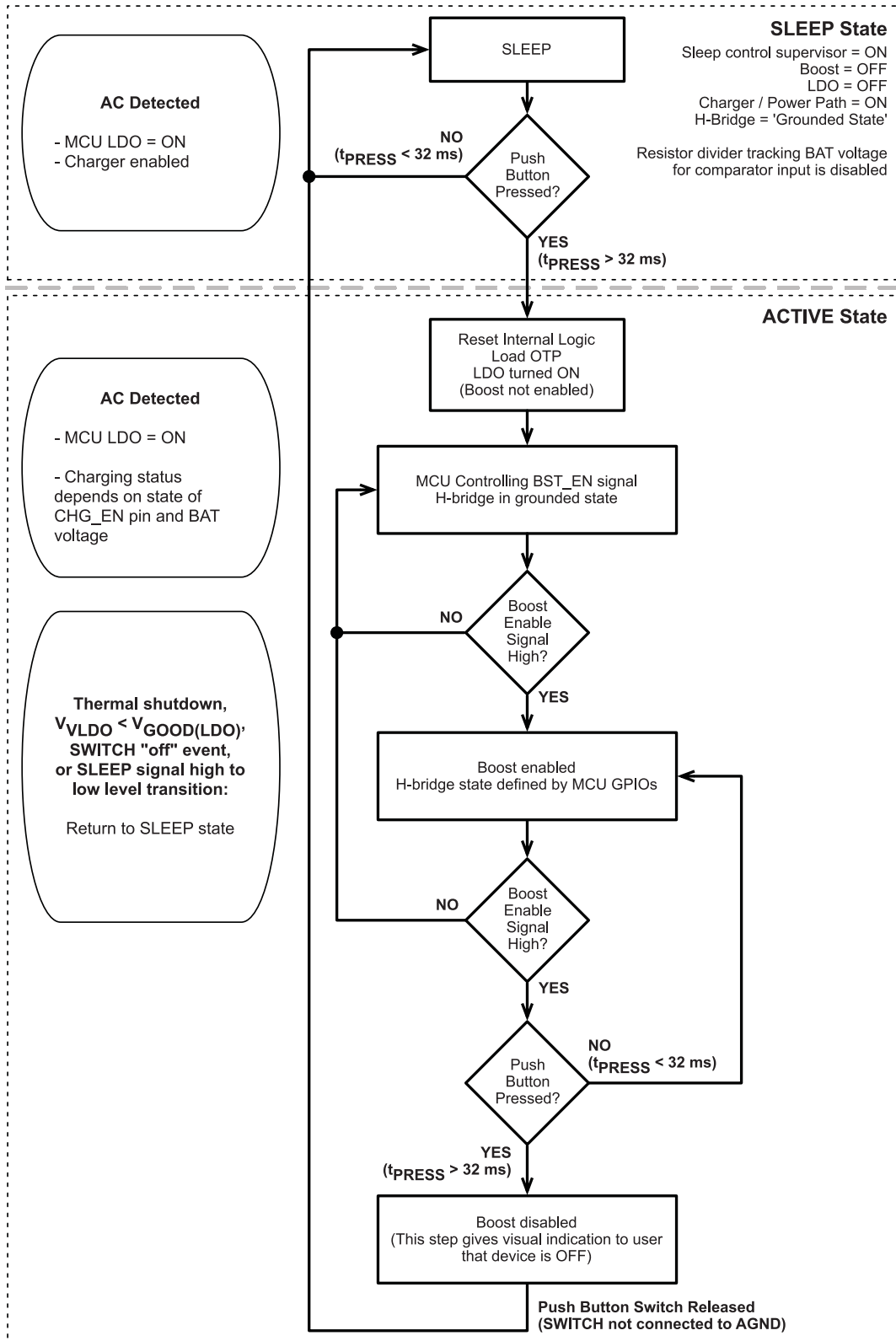


图 2-2. Push Button State Diagram

2.6.3 System Operation Using Slider Switch

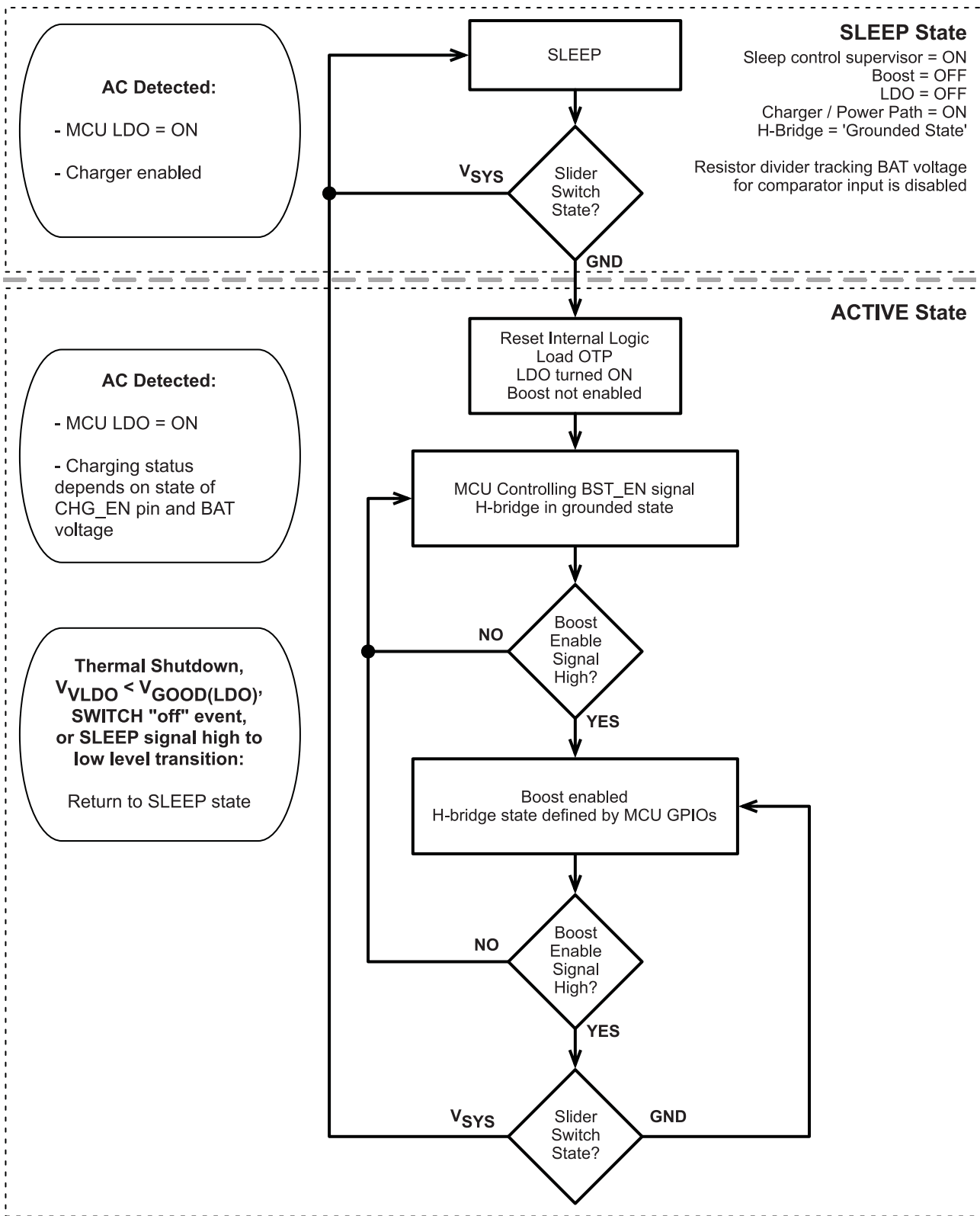


图 2-3. System Operation Using Slider Switch

2.7 Linear Charger Operation

This device has an integrated Li-Ion battery charger and system power path management feature targeted at space-limited portable applications. The architecture powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination, and enables the system to run with a defective or absent battery pack. It also allows instant system turn-on even with a totally discharged battery.

The input power source for charging the battery and running the system can be an AC adapter or USB port connected to the VIN pin as long as the input meets the device operating conditions outlined in this datasheet. The power-path management feature automatically reduces the charging current if the system load increases. Note that the charger input, VIN, has voltage protection up to 28 V.

2.7.1 Battery and TS Detection

To detect and determine between a good or damaged battery, the device checks for a short circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage on the BAT pin. While sourcing this current if the BAT pin voltage exceeds $V_{BAT(SC)}$, a battery has been detected. If the voltage stays below the $V_{BAT(SC)}$ level, the battery is presumed to be damaged and not safe to charge.

The device will also check for the presence of a 10 kΩ NTC thermistor attached to the TS pin of the device. The check for the NTC thermistor on the TS pin is done much like the battery detection feature described previously. The voltage on the TS pin is compared against a defined level and if it is found to be above the threshold, the NTC thermistor is assumed to be disconnected or not used in the system. To reduce the system quiescent current, the NTC thermistor temperature sensing function is only enabled when the device is charging and when the thermistor has been detected.

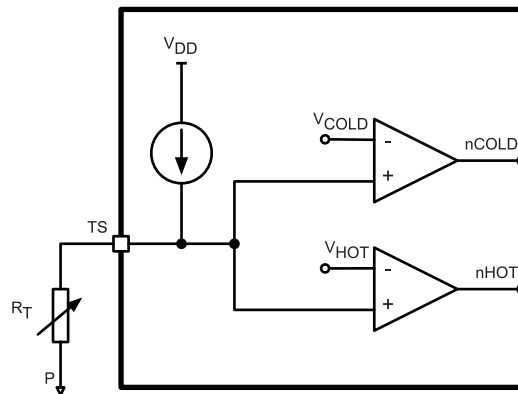


图 2-4. Thermistor Detection and Circuit

2.7.2 Battery Charging

The battery is charged in three phases: conditioning pre-charge, constant-current fast charge (current regulation), and a constant-voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. 图 2-5 shows what happens in each of the three charge phases:

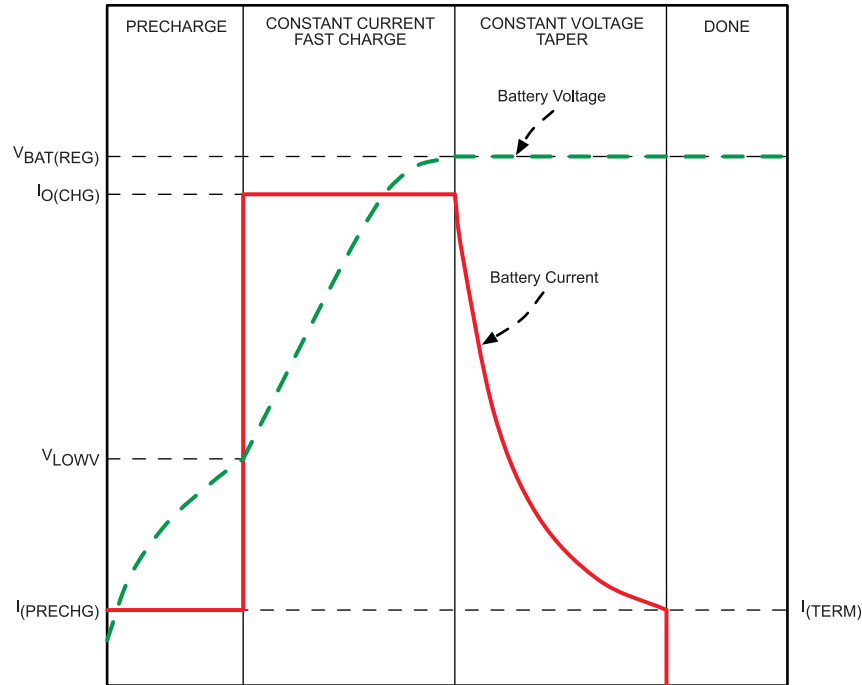


图 2-5. Battery Charge Phases

In the pre-charge phase, the battery is charged with the pre-charge current that is scaled to be 10% of the fast-charge current set by the resistor connected to the ISET pin. Once the battery voltage crosses the V_{LOWV} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{TERM} , the charger indicates charging is done by making the nCHG_STAT pin high impedance. Note that termination detection is disabled whenever the charge rate is reduced from the set point because of the actions of the thermal loop, the DPM loop, or the $V_{IN(LOWV)}$ loop.

2.7.2.1 Pre-charge

The value for the pre-charge current is set to be 10% of the charge current that is set by the external resistor, R_{ISET} . Pre-charge current is scaled to lower currents when the charger is in thermal regulation.

2.7.2.2 Charge Termination

In the fast charge state, once $V_{BAT} \geq V_{BAT(REG)}$, the charger enters constant voltage mode. In constant voltage mode, the charge current will taper until termination when the charge current falls below the $I_{(TERM)}$ threshold (typically 10% of the programmed fast charge current). Termination current is not scaled when the charger is in thermal regulation. When the charging is terminated, the nCHG_STAT pin will be high impedance (effectively turning off any LED that is connected to this pin).

2.7.2.3 Recharge

Once a charge cycle is complete and termination is reached, the battery voltage is monitored. If $V_{BAT} < V_{BAT(REG)} - V_{RCH}$, the device determines if the battery has been removed. If the battery is still present, then the recharge cycle begins and will end when $V_{BAT} \geq V_{BAT(REG)}$.

2.7.2.4 Charge Timers

The charger in this device has internal safety timers for the pre-charge and fast charge phases to prevent potential damage to either the battery or the system. The default values for these timers are found as follows: Pre-charge timer = 0.5 hours (30 minutes) and Fast charge timer = 5 hours (300 minutes).

During the fast charge phase, the following events may increase the timer durations:

1. The system load current activates the DPM loop which reduces the available charging current
2. The input current is reduced because the input voltage has fallen to $V_{IN(Low)}$
3. The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$

During each of these events, the internal timers are slowed down proportionately to the reduction in charging current.

If the pre-charge timer expires before the battery voltage reaches V_{LOWV} , the charger indicates a fault condition.

2.7.3 Charger Status (nCHG_STAT Pin)

The nCHG_STAT pin is used to indicate the charger status by an externally connected resistor and LED circuit. The pin is an open drain input and the internal switch is controlled by the logic inside of the charger. This pin may also be connected to a GPIO of the system MCU to indicate charging status. The table below details the status of the nCHG_STAT pin for various operating states of the charger.

表 2-1. nCHG_STAT Functionality

Charging Status	nCHG_STAT FET / LED
Pre-charge / Fast Charge / Charge Termination	ON
Recharge	OFF
OVP	OFF
SLEEP	OFF

2.8 LDO Operation

The power management core has a low dropout linear regulator (LDO) with variable output voltage capability. This LDO is used for supplying the microcontroller and may be used to supply either an external IR or RF module, depending on system requirements. The LDO can supply a continuous current of up to 30 mA.

The output voltage (V_{VLDO}) of the LDO is set by the state of the VLDO_SET pin. See 表 2-2 for details on setting the LDO output voltage.

表 2-2. VLDO_SET Functionality

VLDO_SET State	VLDO Output Voltage (V_{VLDO})
Low ($VLDO_SET < V_{IL(PMIC)}$)	2.2 V
High ($VLDO_SET > V_{IH(PMIC)}$)	3.0 V

2.8.1 LDO Internal Current Limit

The internal current limit feature helps to protect the LDO regulator during fault conditions. During current limit, the output sources a fixed amount of current that is defined in the electrical specification table. The voltage on the output in this stage can not be regulated and will be $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The pass transistor integrated into the LDO will dissipate power, $(V_{IN} - V_{OUT}) \times I_{LIMIT}$, until the device enters thermal shutdown. In thermal shutdown the device will enter the "SLEEP / POWER OFF" state which means that the LDO will then be disabled and shut off.

2.9 Boost Converter Operation

The boost converter in this device is designed for the load of active shutter 3D glasses. This load is typically a light load where the average current is 2 mA or lower and the peak current out of a battery is limited in operation. This asynchronous boost converter operates with a minimum off time / maximum on time for the integrated low side switch, these values are specified in the electrical characteristics table of this datasheet.

The peak output voltage from the boost converter is adjustable and set by using an external resistor divider connected between BST_OUT, the BST_FB pin, and ground. The peak output voltage is set by choosing resistors for the feedback network such that the voltage on the BST_FB pin is $V_{REF(BST)} = 1.2\text{ V}$. See 节 4.2 for more information on calculating resistance values for this feedback network.

The efficiency curves for various input voltages over the typical 3D glasses load range (2 mA and lower) are shown below. All curves are for a target V_{OUT} of 16 V. For output voltages less than 16 V, a higher efficiency at each operating input voltage should be expected. Note that efficiency is dependent upon the external boost feedback network resistances, the inductor used, and the type of load connected.

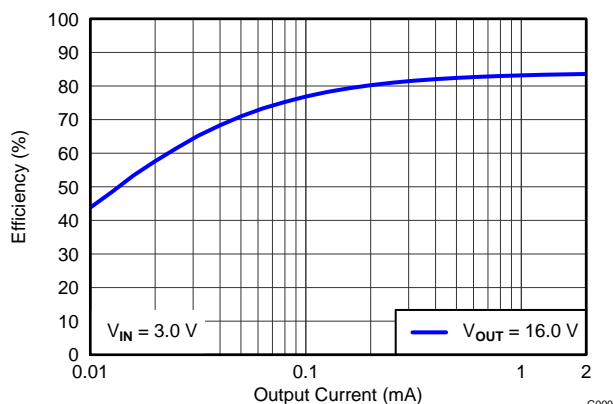


图 2-6. Boost Efficiency vs. I_{OUT} , $V_{IN} = 3.0\text{ V}$, $V_{OUT} = 16\text{ V}$

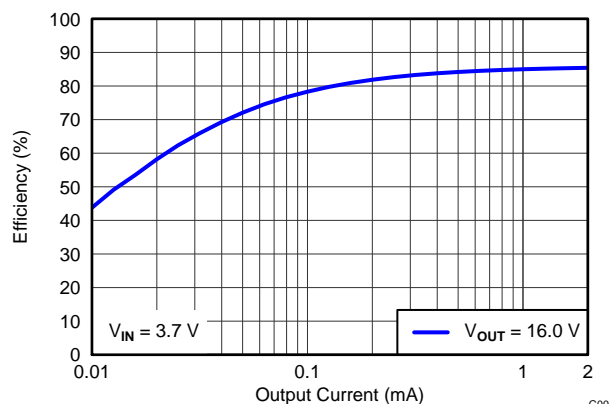


图 2-7. Boost Efficiency vs. I_{OUT} , $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 16\text{ V}$

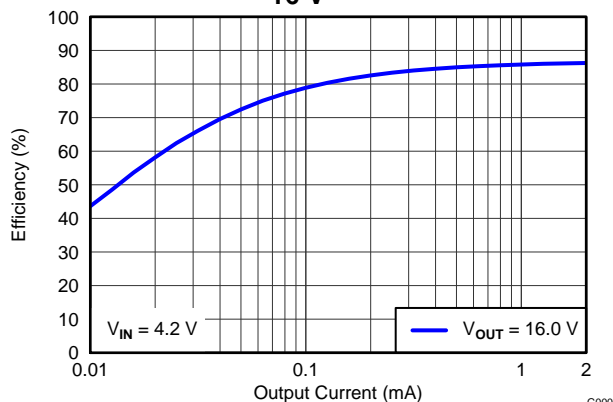


图 2-8. Boost Efficiency vs. I_{OUT} , $V_{IN} = 4.2\text{ V}$, $V_{OUT} = 16\text{ V}$

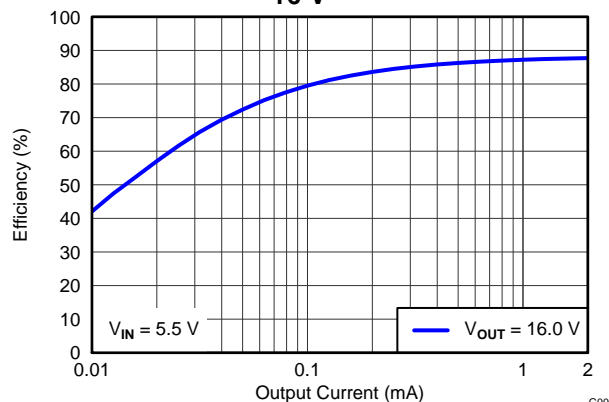


图 2-9. Boost Efficiency vs. I_{OUT} , $V_{IN} = 5.5\text{ V}$, $V_{OUT} = 16\text{ V}$

2.9.1 Boost Thermal Shutdown

An internal thermal shutdown mode is implemented in the boost converter that shuts down the device if the typical junction temperature of 105°C is exceeded. If the device is in thermal shutdown mode, the main switch of the boost is open and the device enters the "SLEEP / POWER OFF" state.

2.9.2 Boost Load Disconnect

When the boost is disabled (BST_EN = LOW), the H-bridge is automatically placed into the OFF state. In the OFF state the high side H-bridge switches are open and the low side switches of the H-bridge are closed. The OFF state grounds and discharges the load, potentially prolonging the life of the LC shutters by eliminating any DC content (see 节 2.10.1 for more information regarding the H-bridge states). The disconnection of the load is done with the H-Bridge and can be seen in the next figure (图 2-10).

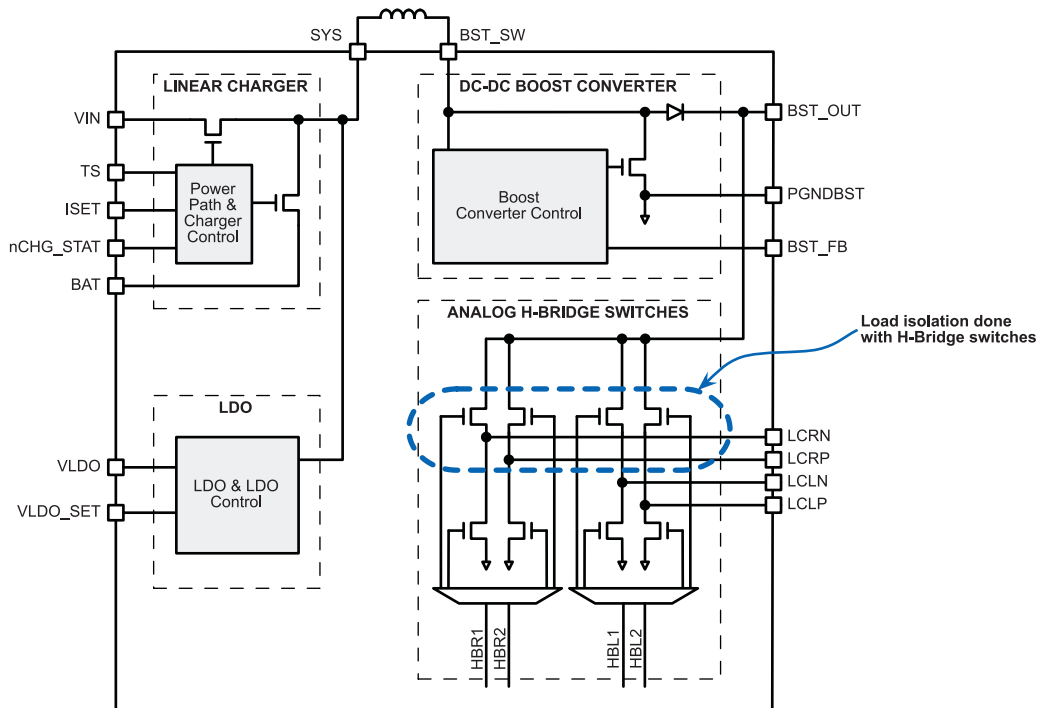


图 2-10. Boost Load Disconnect

An advantage to this topology for disconnecting the load is that the boost output capacitor is charged to approximately the SYS voltage level, specifically $V_{SYS} - V_{DIODE(BST)}$, when the boost is disabled. This design ensures that there is not a large in-rush current into the boost output capacitor when the boost is enabled. The boost operation efficiency is also increased because there is no load disconnect switch in the boost output path, such a switch would decrease efficiency because of the resistance that it would introduce.

2.10 Full H-Bridge Analog Switches

The TPS65835 has two integrated full H-bridge analog switches that are connected to GPIO ports on the MSP430 and can be controlled by the MSP430 core for various system functions. There is an internal level shifter that takes care of the input signals to the H-Bridge switches.

2.10.1 H-Bridge Switch Control

The H-Bridge switches are controlled by the MSP430 core for system operation - specifically to control charge polarity on the LCD shutters. Depending on the state of the signals from the MSP430 core, the H-Bridge will be put into 4 different states. These states are:

- **OPEN:** All Switches Opened
- **CHARGE+:** Boost Output Voltage Present on Pins LCLP or LCRP
- **CHARGE-:** Boost Output Voltage Present on Pins LCLN or LCRN
- **GROUNDED:** High side switches are opened and low side switches are closed

If CHARGE+ state is followed by the CHARGE- state, the voltage across the capacitor connected to the H-Bridge output terminals will be reversed. The system is automatically put into the GROUNDED state when the boost is disabled by the BST_EN pin - for more details see 节 2.6.

表 2-3. H-Bridge States from Inputs

HBx2 [HBL2 & HBR2]	HBx1 [HBL1 & HBR1]	H-Bridge State
0	0	OPEN
0	1	CHARGE +
1	0	CHARGE -
1	1	GROUNDED

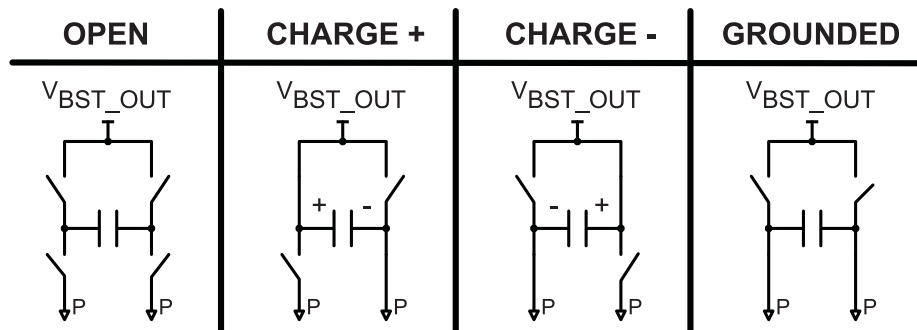


图 2-11. H-Bridge States

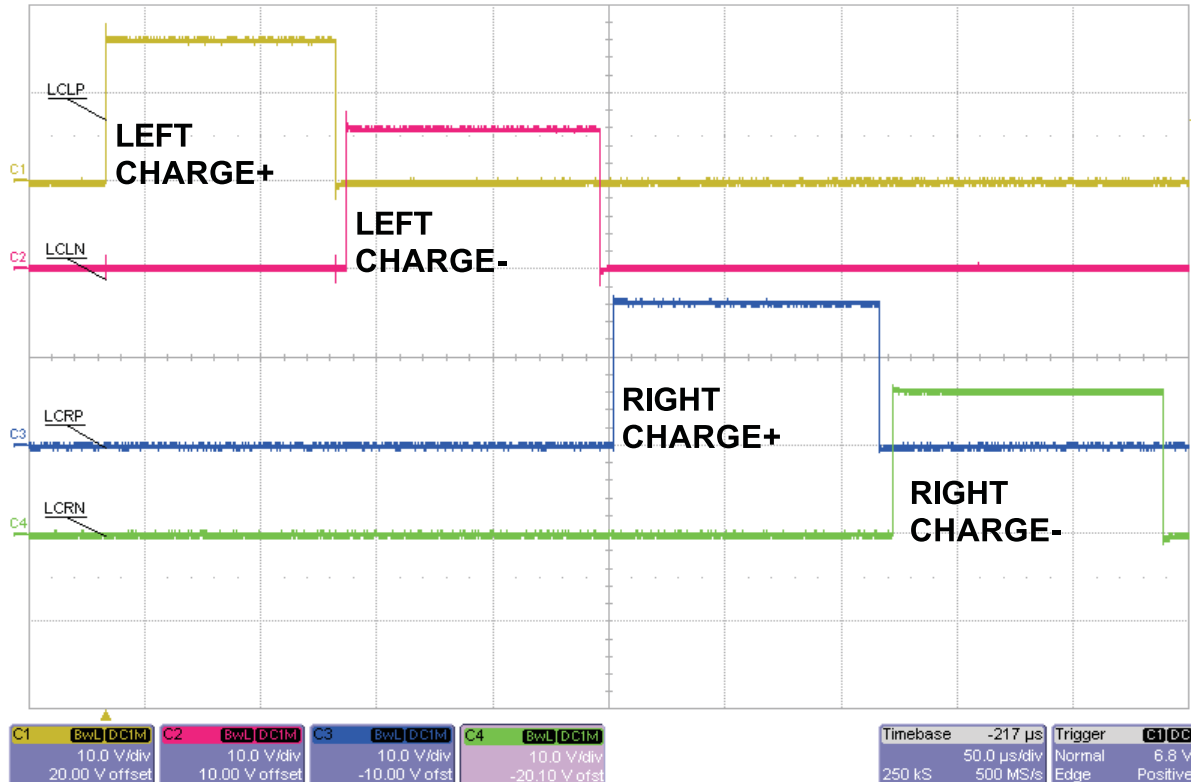


图 2-12. H-Bridge States from Oscilloscope

2.11 Power Management Core Control

The power management core is controlled with external pins that can set system behavior by their status along with internal connections to GPIOs from the MSP430 that can be modified depending on the code implemented in the MSP430.

2.11.1 SLEEP / Power Control Pin Function

The internal SLEEP signal between the power management device and the MSP430 can be used to control the power down behavior of the device. This has multiple practical applications such as a watchdog implementation for the communication between the sender (TV) and the 3D glasses (receiver) or different required system on and off times; typically when the push-button press timing for an off event is a few seconds in length, programmable by software in the system MCU.

If there is a requirement that the push-button press for system on and off events are different, the SLEEP signal must be set to a logic high value ($V_{SLEEP} > V_{IH(PMIC)}$) upon system startup. This implementation allows the device to power down the system on the falling edge of the SLEEP signal (when: $V_{SLEEP} < V_{IL(PMIC)}$).

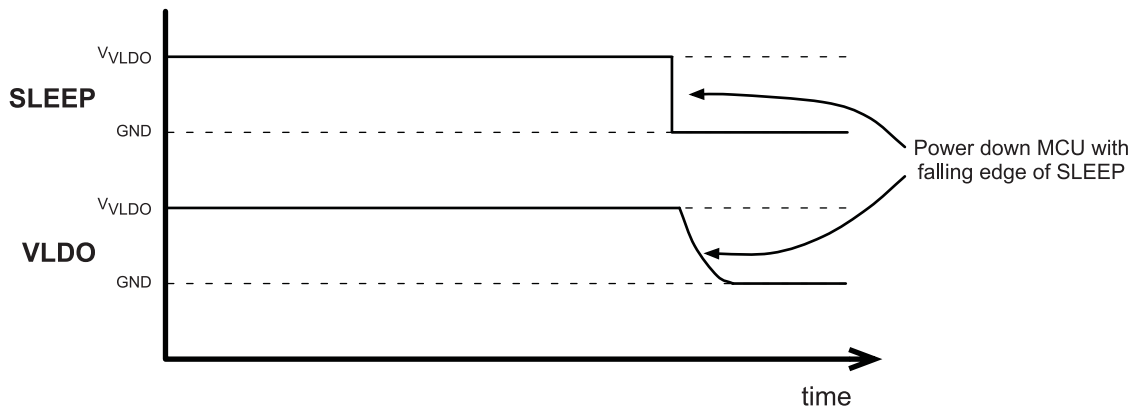


图 2-13. SLEEP Signal to Force System Power Off

2.11.2 COMP Pin Functionality

The COMP pin is used to output a scaled down voltage level related to the battery voltage for input to the comparator of the MSP430. Applications for this COMP feature could be to generate an interrupt on the MSP430 when the battery voltage drops under a threshold and the device can then be shut down or indicate to the end user with an LED that the battery requires charging.

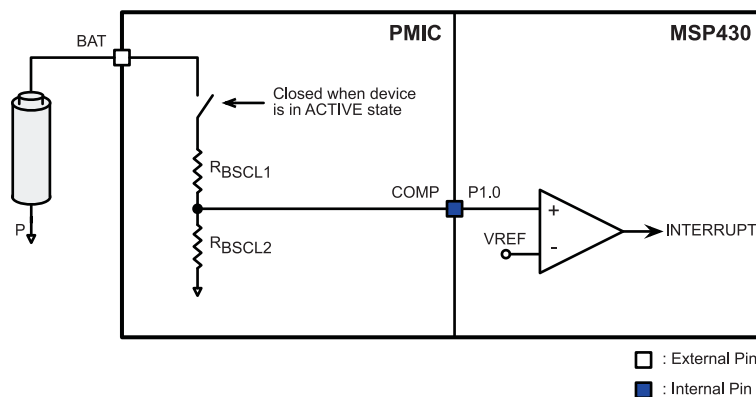


图 2-14. COMP Pin Internal Connection

表 2-4. Scaling Resistors for COMP Pin Function ($V_{VLDO} = 2.2\text{ V}$)

Scaling Resistors for COMP Pin Function	Value
R_{BSC1}	3.0 M Ω
R_{BSC2}	2.36 M Ω

表 2-5. Scaling Resistors for COMP Pin Function ($V_{VLDO} = 3.0\text{ V}$)

Scaling Resistors for COMP Pin Function	Value
R_{BSC1}	3.0 M Ω
R_{BSC2}	2.48 M Ω

Using the designed values in 表 2-4 or 表 2-5, the voltage on the COMP pin will be: $V_{COMP} = 0.5 \times V_{VLDO} + 300\text{ mV}$. This assures that the COMP pin voltage will be close to half of the LDO output voltage plus the LDO dropout voltage of the device. The COMP pin can also be used as an input to ADC channel A0 of the integrated MSP430 microcontroller. This is useful if greater measurement accuracy or increased functionality is desired from this function.

2.11.3 SW_SEL Pin Functionality

The SW_SEL pin is used to select what type of switch is connected to the SWITCH pin of the device. Selection between a push-button and a slider switch can be made based on the state of this pin.

表 2-6. SW_SEL Settings

SW_SEL State	Type of Switch Selected
Low ($V_{SW_SEL} < V_{IL(PMIC)}$)	Slider Switch
High ($V_{SW_SEL} > V_{IH(PMIC)}$)	Push-button

When the push button switch type is selected, the device will debounce the SWITCH input with a 32 ms timer for both the ON and OFF events and either power on or off the device. Using the push-button switch function, the ON and OFF timings are equal; $t_{ON} = t_{OFF}$. If the system requirements are such that the on and off timings should be different, $t_{ON} \neq t_{OFF}$, then refer to the following section for the correct system setup: 节 4.3. When the slider switch operation is selected, the SWITCH pin must be externally pulled up to the SYS voltage with a resistor and the output connected to the slider switch. When the SWITCH pin is pulled to ground, the device will turn on and enter the power up sequence.

2.11.4 SWITCH Pin

The SWITCH pin behavior is defined by the SW_SEL pin (节 2.11.3) which defines the type of switch that is connected to the system; either a slider switch or push-button.

2.11.5 Slider Switch Behavior

If a slider switch is connected in the system then the system power state and VLDO output (which powers the internal MSP430) is defined by the state of the slider switch. If the slider is in the "off" position than the SWITCH pin should be connected to the SYS pin. If the slider is in the "on" position than the SWITCH pin should be connected to ground. 图 2-15 details the system operation using the slider switch configuration.

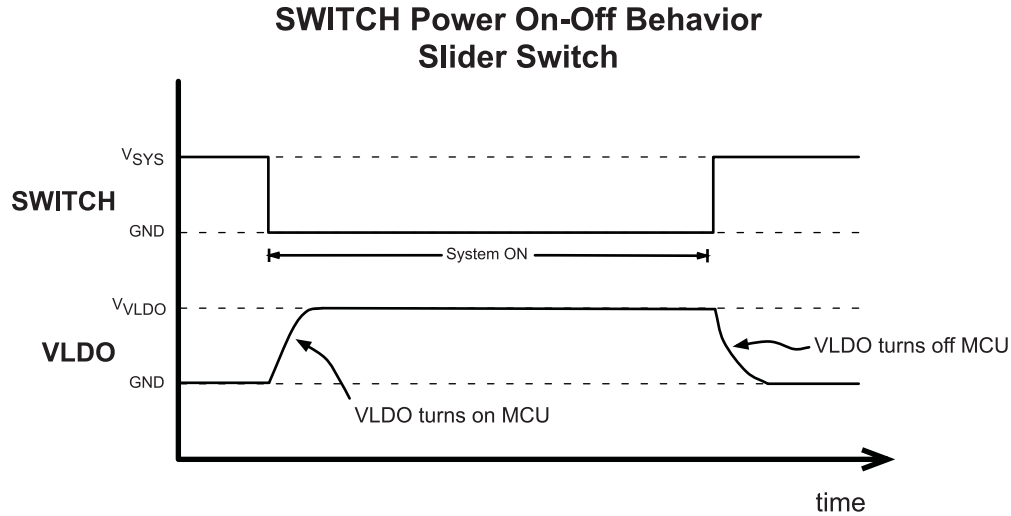


图 2-15. SWITCH, Slider Power On-Off Behavior

2.11.6 Push-Button Switch Behavior

The system is powered on or off by a push-button press after a press that is greater than 32 ms. The following figures (图 2-16 and 图 2-17) show the system behavior and the expected VLDO output during the normal push-button operation where the ON and OFF press timings are the same value, $t_{ON} = t_{OFF}$.

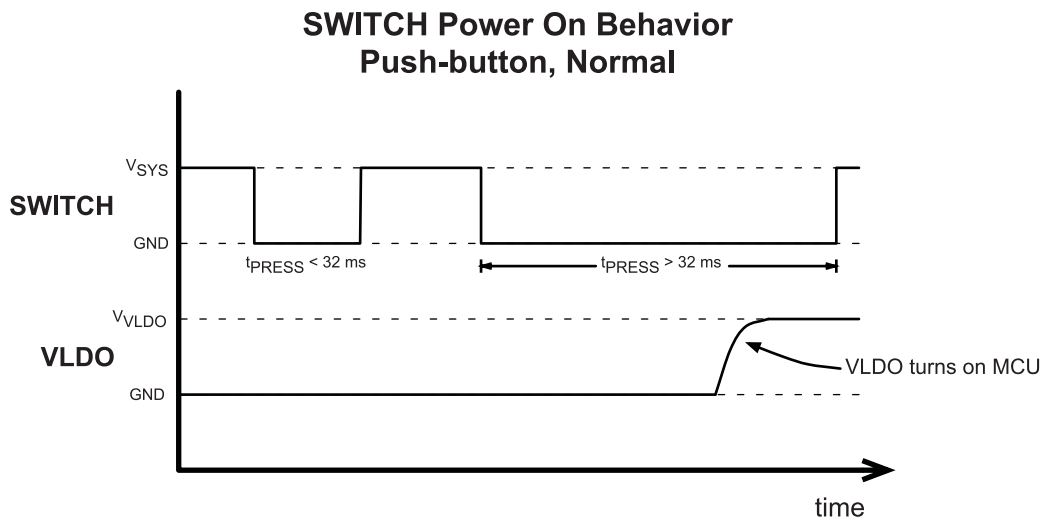


图 2-16. SWITCH, Push-button Power On Behavior

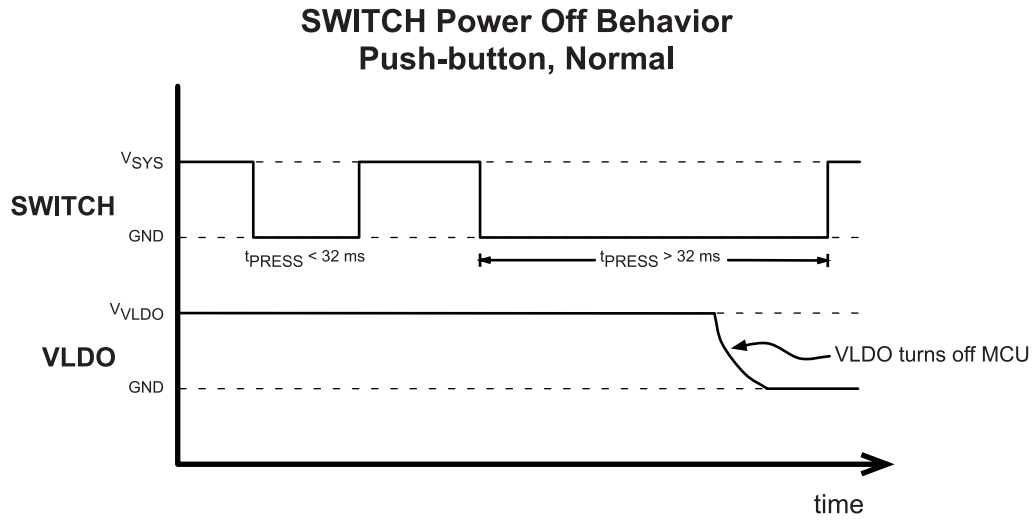


图 2-17. SWITCH, Push-button Power Off Behavior

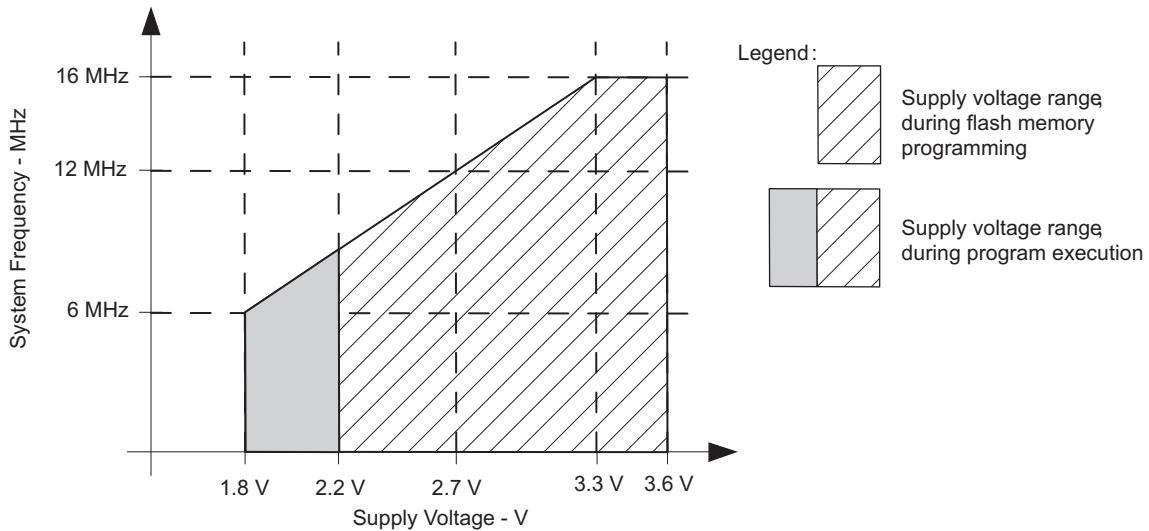
3 MSP430 CORE

3.1 MSP430 Electrical Characteristics

3.1.1 MSP430 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage	During program execution		1.8	3.6	V
		During flash programming/erase		2.2	3.6	
V _{SS}	Supply voltage	0			V	
f _{SYSTEM}	Processor frequency (maximum MCLK frequency using the USART module) ⁽¹⁾⁽²⁾	V _{CC} = 1.8 V, Duty cycle = 50% ± 10%		dc	6	MHz
		V _{CC} = 2.7 V, Duty cycle = 50% ± 10%		dc	12	
		V _{CC} = 3.3 V, Duty cycle = 50% ± 10%		dc	16	

- (1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
- (2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

图 3-1. Safe Operating Area

3.1.2 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾⁽⁴⁾

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
I _{AM,1MHz}	Active mode (AM) current at 1 MHz		2.2 V	230		420	μA
			3 V	330			

- (3) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
- (4) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

3.1.3 Typical Characteristics, Active Mode Supply Current (Into V_{CC})

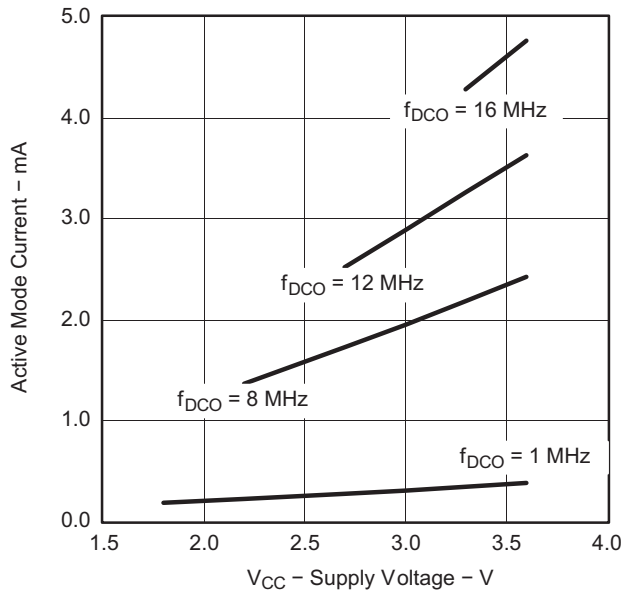


图 3-2. Active Mode Current vs V_{CC} , $T_A = 25^\circ\text{C}$

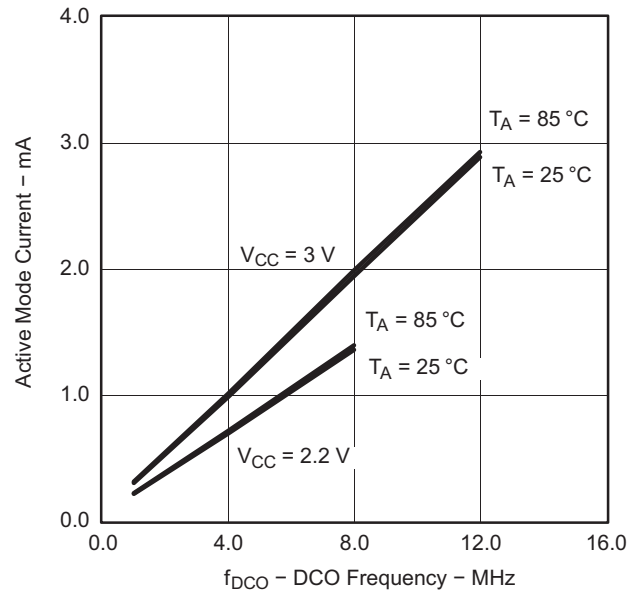


图 3-3. Active Mode Current vs DCO Frequency

3.1.4 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$ Low-power mode 0 (LPM0) current ⁽¹⁾	$f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO} = 1$ MHz, $f_{ACLK} = 32768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	25°C	2.2 V		56		μA
I_{LPM2} Low-power mode 2 (LPM2) current ⁽²⁾	$f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{DCO} = 1$ MHz, $f_{ACLK} = 32768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		22		μA
$I_{LPM3,LFXT1}$ Low-power mode 3 (LPM3) current ⁽²⁾	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32768$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.7	1.5	μA
$I_{LPM3,VLO}$ Low-power mode 3 current, (LPM3) ⁽²⁾	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.5	0.7	μA
I_{LPM4} Low-power mode 4 (LPM4) current ⁽³⁾	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 0$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	2.2 V		0.1	0.5	μA
		85°C			0.8	1.7	

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
- (1) Current for brownout and WDT clocked by SMCLK included.
- (2) Current for brownout and WDT clocked by ACLK included.
- (3) Current for brownout included.

3.1.5 Typical Characteristics, Low-Power Mode Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

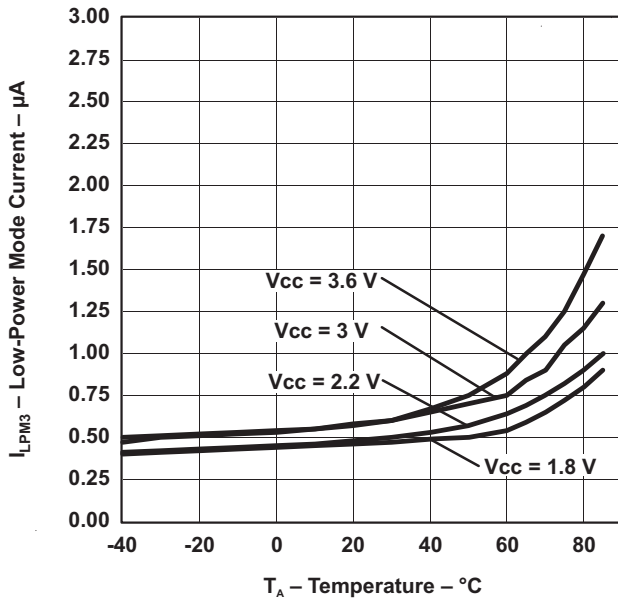


图 3-4. LPM3 Current vs Temperature

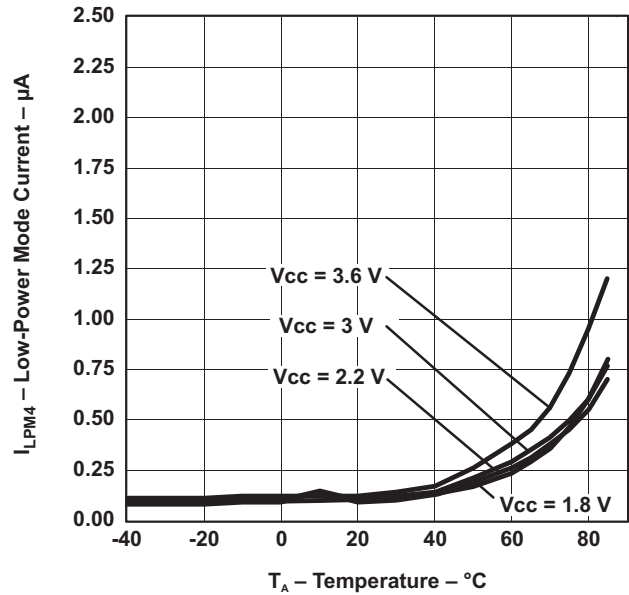


图 3-5. LPM4 Current vs Temperature

3.1.6 Schmitt-Trigger Inputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	3 V	0.45 V _{CC}	0.75 V _{CC}	2.25	V
			1.35			
V _{IT-}	Negative-going input threshold voltage	3 V	0.25 V _{CC}	0.55 V _{CC}	1.65	V
			0.75			
V _{hys}	Input voltage hysteresis (V _{IT+} – V _{IT-})	3 V	0.3		1	V
R _{Pull}	Pullup/pulldown resistor	3 V	20	35	50	kΩ
C _I	Input capacitance	V _{IN} = V _{SS} or V _{CC}		5		pF

3.1.7 Leakage Current, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
I _{lkg(Px.y)}	(1) (2)	3 V		±50	nA

- (1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
- (2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

3.1.8 Outputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _(OHmax) = –6 mA ⁽¹⁾	3 V		V _{CC} – 0.3		V
V _{OL}	I _(OLmax) = 6 mA ⁽¹⁾	3 V		V _{SS} + 0.3		V

- (1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

3.1.9 Output Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{Px,y}	Port output frequency (with load) Px,y, C _L = 20 pF, R _L = 1 kΩ ⁽¹⁾ (2)	3 V		12		MHz
f _{Port_CLK}	Clock output frequency Px,y, C _L = 20 pF ⁽²⁾	3 V		16		MHz

- (1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

3.1.10 Typical Characteristics, Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

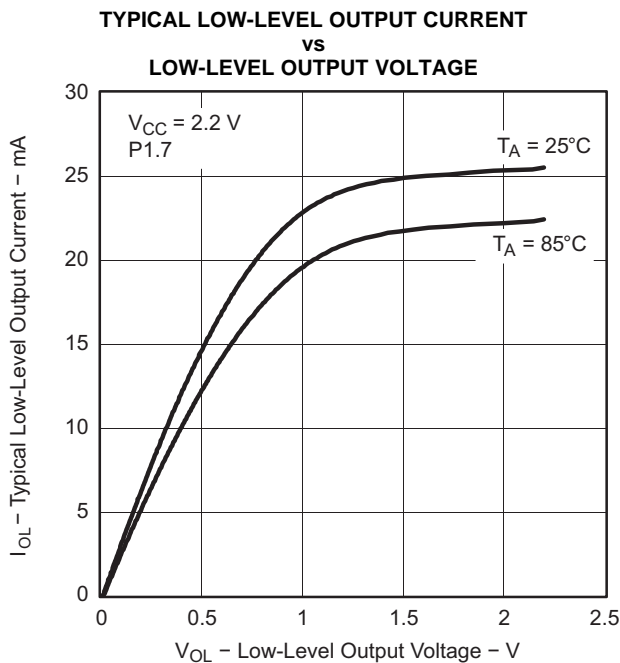


图 3-6.

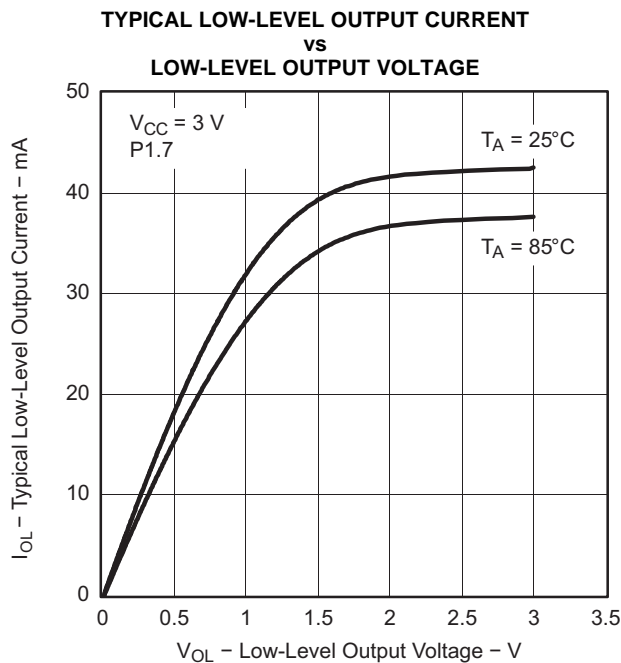


图 3-7.

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

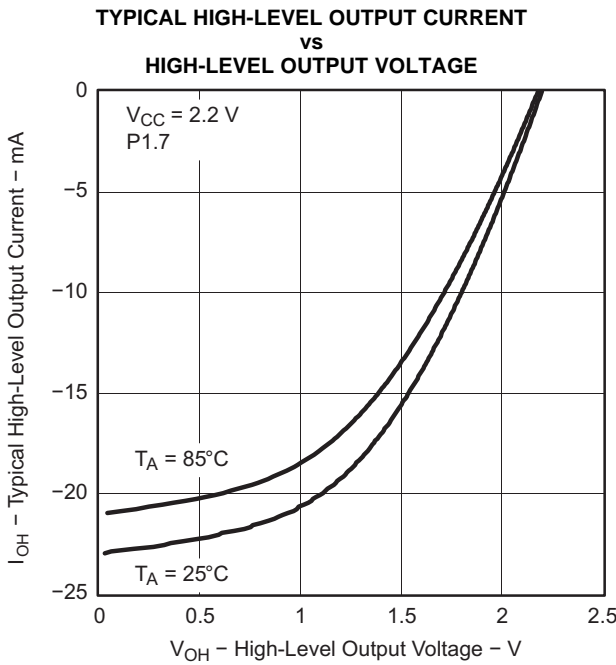


图 3-8.

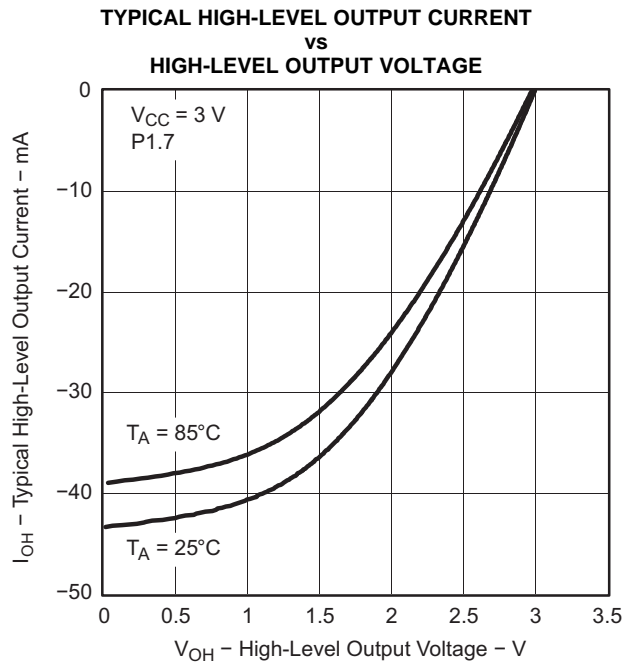


图 3-9.

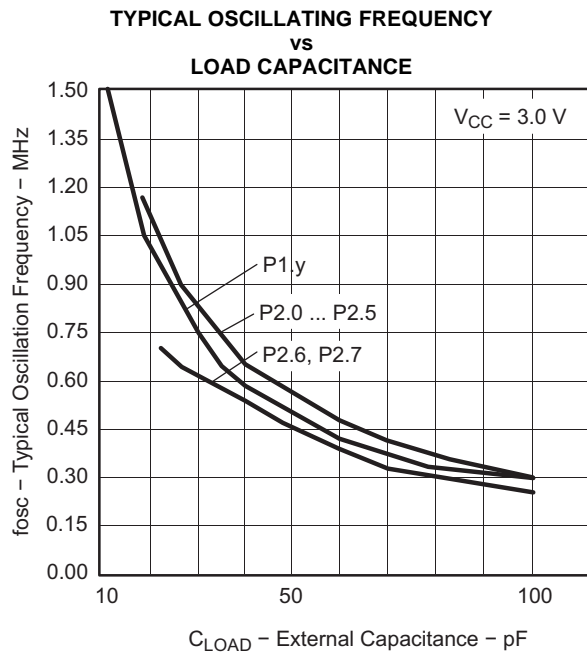
3.1.11 Pin-Oscillator Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{OP1,x}	Port output oscillation frequency	P1.y, C _L = 10 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾	3 V	1400			kHz
		P1.y, C _L = 20 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾		900			
f _{OP2,x}	Port output oscillation frequency	P2.0 to P2.5, C _L = 10 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾	3 V	1800			kHz
		P2.0 to P2.5, C _L = 20 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾		1000			
f _{OP2,6/7}	Port output oscillation frequency	P2.6 and P2.7, C _L = 20 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾	3 V	700			kHz
f _{OP3,x}	Port output oscillation frequency	P3.y, C _L = 10 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾		1800			kHz
		P3.y, C _L = 20 pF, R _L = 100 kΩ ⁽¹⁾⁽²⁾		1000			

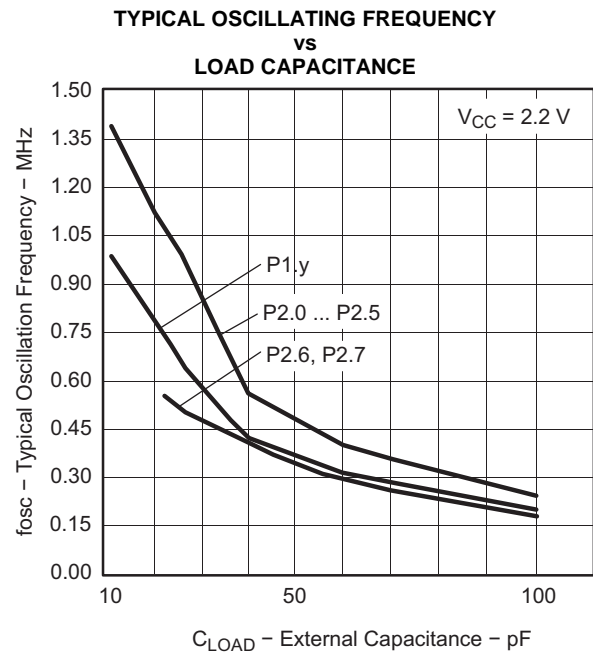
- (1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

3.1.12 Typical Characteristics, Pin-Oscillator Frequency



A. One output active at a time.

图 3-10.



B. One output active at a time.

图 3-11.

3.1.13 POR/Brownout Reset (BOR)⁽³⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC(start)}	See 图 3-12	dV _{CC} /dt ≤ 3 V/s			0.7 × V _(B_IT-)		V
V _(B_IT-)	See 图 3-12 through 图 3-14	dV _{CC} /dt ≤ 3 V/s			1.35		V
V _{hys(B_IT-)}	See 图 3-12	dV _{CC} /dt ≤ 3 V/s			140		mV
t _{d(BOR)}	See 图 3-12				2000		μs
t _(reset)	Pulse length needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally		2.2 V	2			μs

(3) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level V_(B_IT-) + V_{hys(B_IT-)} is ≤ 1.8 V.

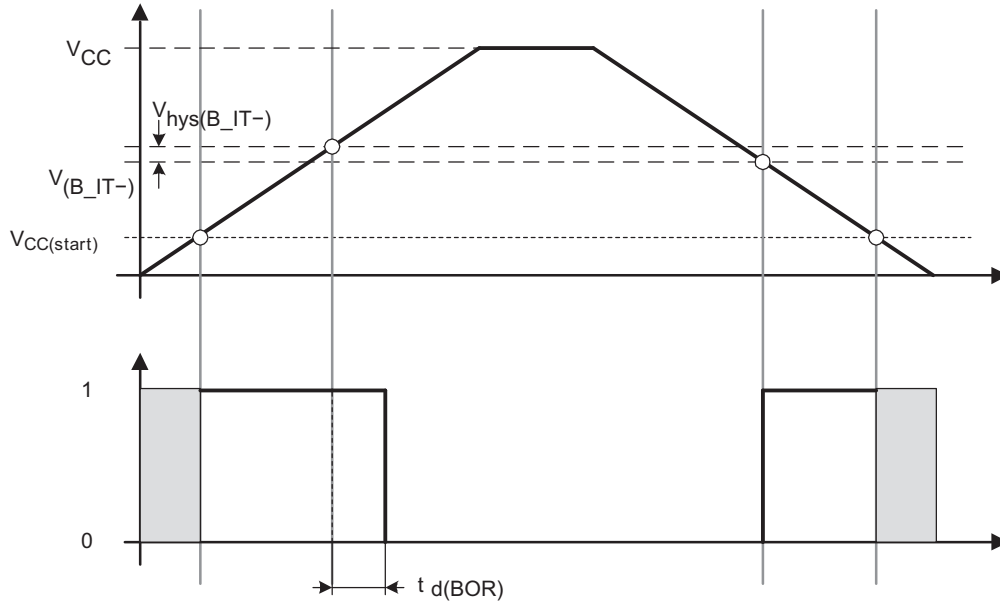


图 3-12. POR/Brownout Reset (BOR) vs Supply Voltage

3.1.14 Typical Characteristics, POR/Brownout Reset (BOR)

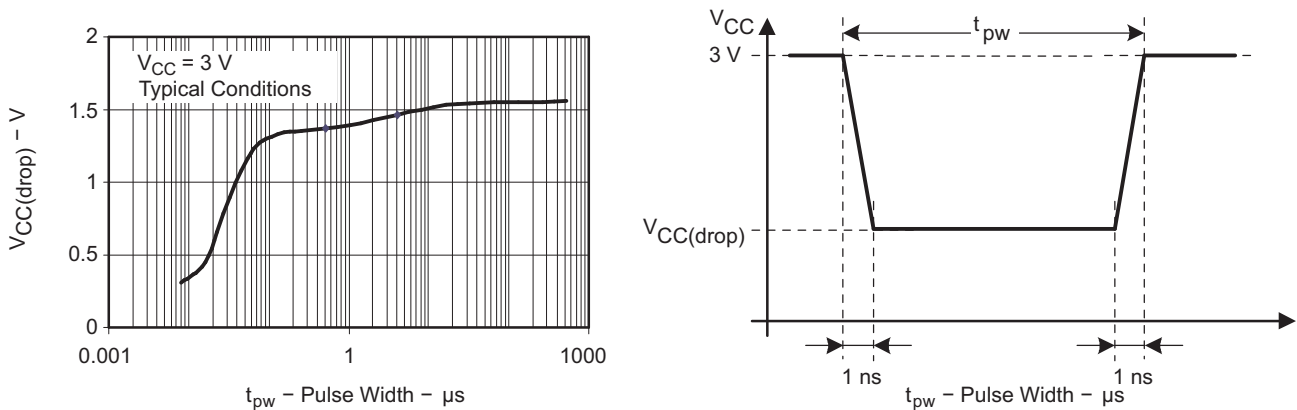


图 3-13. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

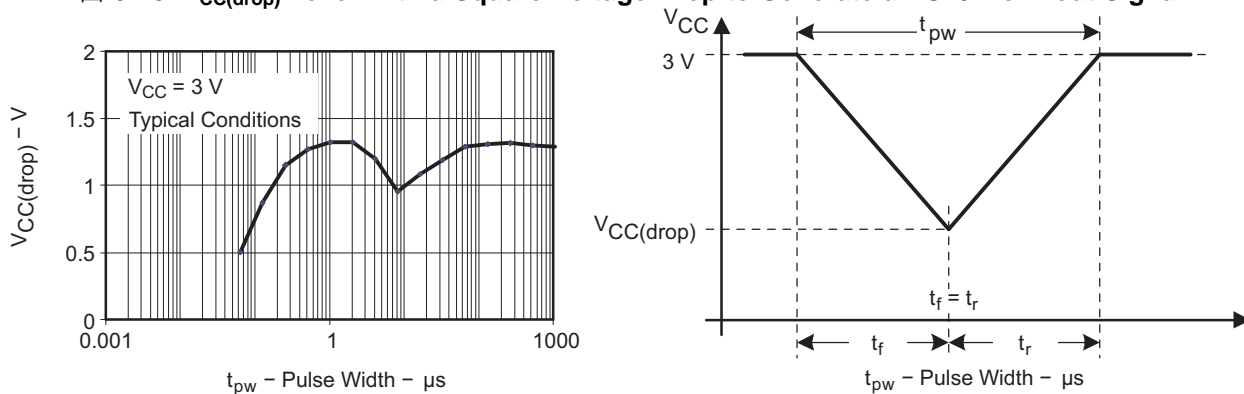


图 3-14. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

3.1.15 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3		3.6	
f _{DCO(0,0)}	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	3 V	0.06		0.14	MHz
f _{DCO(0,3)}	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	3 V	0.07		0.17	MHz
f _{DCO(1,3)}	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	3 V		0.15		MHz
f _{DCO(2,3)}	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	3 V		0.21		MHz
f _{DCO(3,3)}	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	3 V		0.30		MHz
f _{DCO(4,3)}	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	3 V		0.41		MHz
f _{DCO(5,3)}	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	3 V		0.58		MHz
f _{DCO(6,3)}	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	3 V	0.54		1.06	MHz
f _{DCO(7,3)}	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	3 V	0.80		1.50	MHz
f _{DCO(8,3)}	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	3 V		1.6		MHz
f _{DCO(9,3)}	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	3 V		2.3		MHz
f _{DCO(10,3)}	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	3 V		3.4		MHz
f _{DCO(11,3)}	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	3 V		4.25		MHz
f _{DCO(12,3)}	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	3 V	4.30		7.30	MHz
f _{DCO(13,3)}	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	3 V	6.00	7.8	9.60	MHz
f _{DCO(14,3)}	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	3 V	8.60		13.9	MHz
f _{DCO(15,3)}	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
f _{DCO(15,7)}	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S _{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)} / f_{DCO(RSEL,DCO)}$	3 V		1.35		ratio
S _{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)} / f_{DCO(RSEL,DCO)}$	3 V		1.08		ratio
Duty cycle		Measured at SMCLK output	3 V		50		%

3.1.16 Calibrated DCO Frequencies, Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature ⁽¹⁾	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	3	%
1-MHz tolerance over V _{CC}	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	30°C	1.8 V to 3.6 V	-3	±2	3	%
1-MHz tolerance overall	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	1.8 V to 3.6 V	-6	±3	6	%
8-MHz tolerance over temperature ⁽¹⁾	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	3	%
8-MHz tolerance over V _{CC}	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	30°C	2.2 V to 3.6 V	-3	±2	3	%
8-MHz tolerance overall	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	2.2 V to 3.6 V	-6	±3	6	%
12-MHz tolerance over temperature ⁽¹⁾	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	3	%
12-MHz tolerance over V _{CC}	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	30°C	2.7 V to 3.6 V	-3	±2	3	%
12-MHz tolerance overall	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	2.7 V to 3.6 V	-6	±3	6	%
16-MHz tolerance over temperature ⁽¹⁾	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	3	%
16-MHz tolerance over V _{CC}	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	30°C	3.3 V to 3.6 V	-3	±2	3	%
16-MHz tolerance overall	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	3.3 V to 3.6 V	-6	±3	6	%

(1) This is the frequency change from the measured frequency at 30°C over temperature.

3.1.17 Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{DCO,LPM3/4}	DCO clock wake-up time from LPM3/4 ⁽¹⁾	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz	3 V	1.5		μs
t _{CPU,LPM3/4}	CPU wake-up time from LPM3/4 ⁽²⁾			1/f _{MCLK} + t _{Clock,LPM3/4}		

- (1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
- (2) Parameter applicable only if DCOCLK is used for MCLK.

3.1.18 Typical Characteristics, DCO Clock Wake-Up Time From LPM3/4

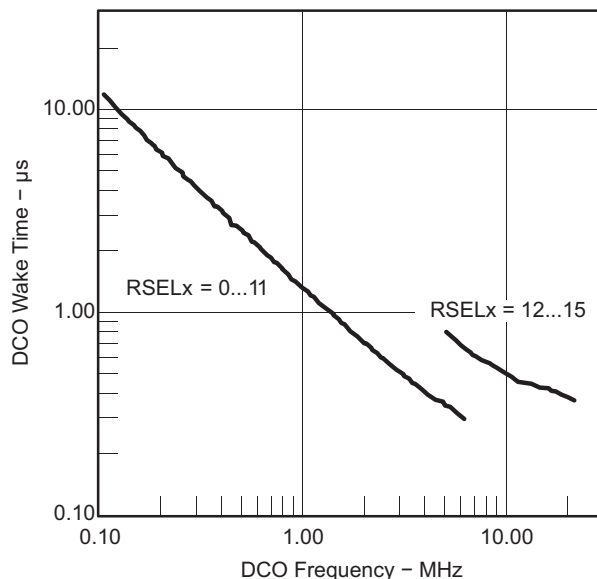


图 3-15. DCO Wake-Up Time From LPM3 vs DCO Frequency

3.1.19 Crystal Oscillator, XT1, Low-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER ⁽¹⁾		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{LFXT1,LF}	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
f _{LFXT1,LF,logic}	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
O _{A,LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 Hz, C _{L,eff} = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 Hz, C _{L,eff} = 12 pF			200		
C _{L,eff}	Integrated effective load capacitance, LF mode ⁽²⁾	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
Duty cycle	LF mode	XTS = 0, Measured at P2.0/ACLK, f _{LFXT1,LF} = 32768 Hz	2.2 V	30	50	70	%
f _{Fault,LF}	Oscillator fault frequency, LF mode ⁽³⁾	XTS = 0, XCAPx = 0, LFXT1Sx = 3 ⁽⁴⁾	2.2 V	10		10000	Hz

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (4) Measured with logic-level input frequency but also applies to operation with crystals.

3.1.20 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T _A	V _{CC}	MIN	TYP	MAX	UNIT
f _{VLO}	VLO frequency	-40°C to 85°C	3 V	4	12	20	kHz
df _{VLO} /dT	VLO frequency temperature drift	-40°C to 85°C	3 V		0.5		%/°C
df _{VLO} /dV _{CC}	VLO frequency supply voltage drift	25°C	1.8 V to 3.6 V		4		%/V

3.1.21 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{TA} Timer_A input clock frequency	SMCLK, duty cycle = 50% ± 10%			f _{SYSTEM}		MHz
t _{TA,cap} Timer_A capture timing	TA0, TA1	3 V	20			ns

3.1.22 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI} USCI input clock frequency	SMCLK, duty cycle = 50% ± 10%			f _{SYSTEM}		MHz
f _{max,BITCLK} Maximum BITCLK clock frequency (equals baudrate in MBaud) ⁽¹⁾		3 V	2			MHz
t _r UART receive deglitch time ⁽²⁾		3 V	50	100	600	ns

(1) The DCO wake-up time must be considered in LPM3/4 for baud rates above 1 MHz.

(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their width should exceed the maximum specification of the deglitch time.

3.1.23 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 3-16 and 图 3-17)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI} USCI input clock frequency	SMCLK, duty cycle = 50% ± 10%				f _{SYSTEM}	MHz
t _{SU,MI} SOMI input data setup time		3 V	75			ns
t _{HD,MI} SOMI input data hold time		3 V	0			ns
t _{VALID,MO} SIMO output data valid time	UCLK edge to SIMO valid, C _L = 20 pF	3 V			20	ns

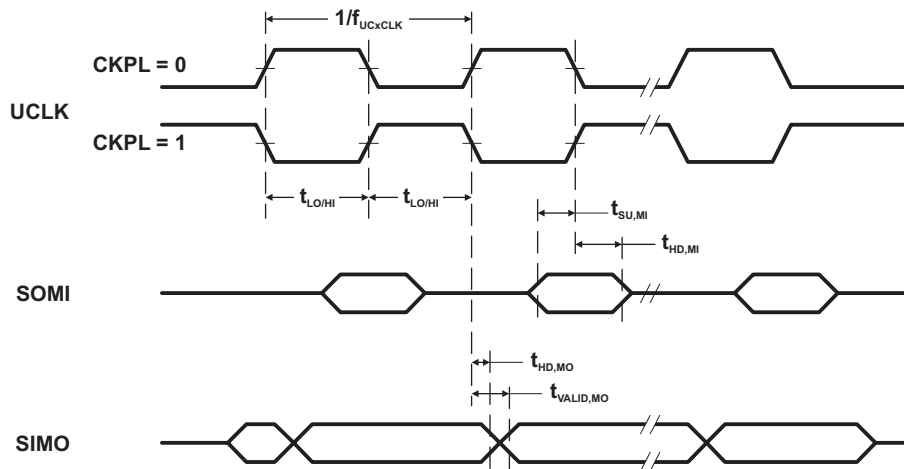


图 3-16. SPI Master Mode, CKPH = 0

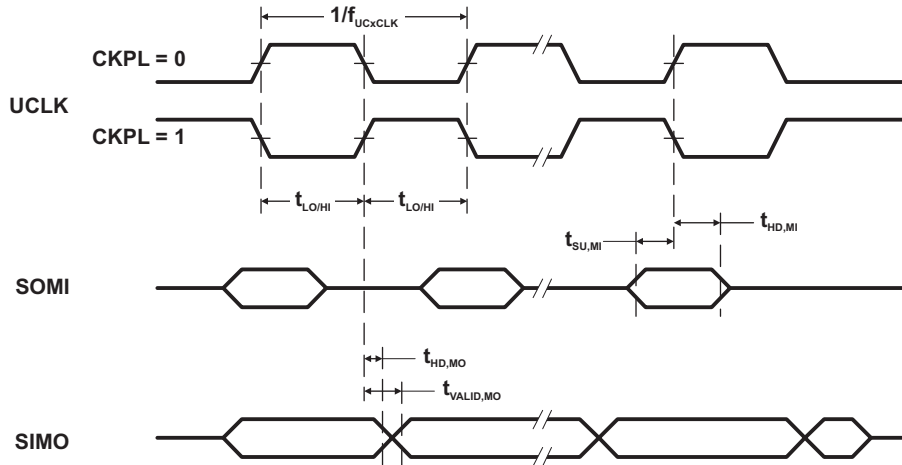


图 3-17. SPI Master Mode, CKPH = 1

3.1.24 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 3-18 and 图 3-19)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{STE,LEAD}	STE lead time, STE low to clock		3 V		50		ns
t _{STE,LAG}	STE lag time, Last clock to STE high		3 V	10			ns
t _{STE,ACC}	STE access time, STE low to SOMI data out		3 V		50		ns
t _{STE,DIS}	STE disable time, STE high to SOMI high impedance		3 V		50		ns
t _{SU,SI}	SIMO input data setup time		3 V	15			ns
t _{HD,SI}	SIMO input data hold time		3 V	10			ns
t _{VALID,SO}	SOMI output data valid time	UCLK edge to SOMI valid, C _L = 20 pF	3 V		50	75	ns

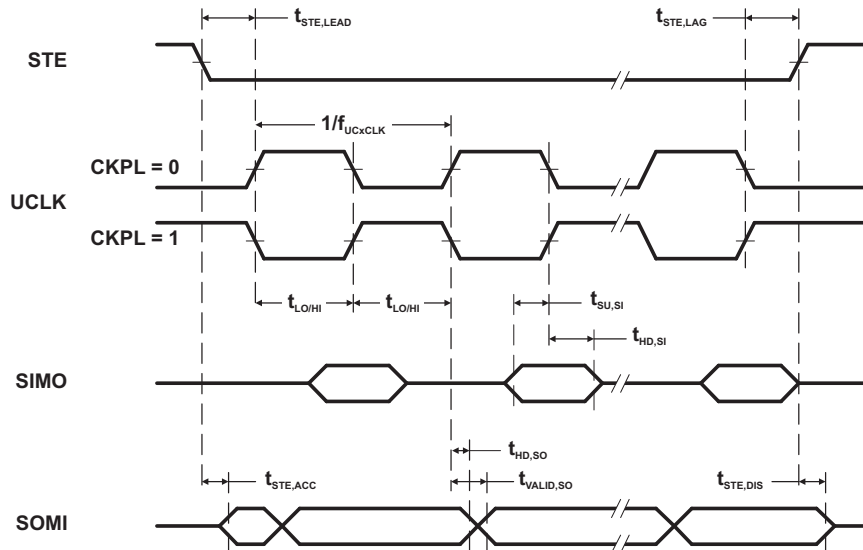


图 3-18. SPI Slave Mode, CKPH = 0

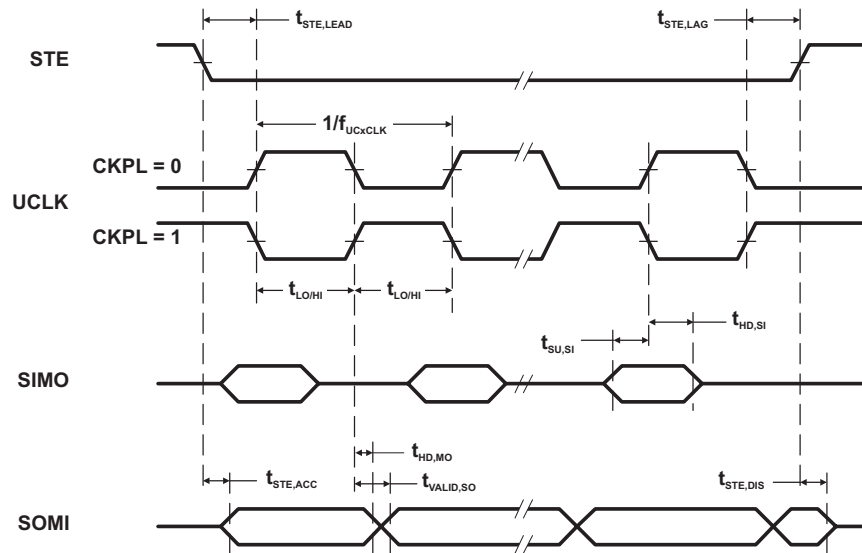


图 3-19. SPI Slave Mode, CKPH = 1

3.1.25 USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 3-20)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI}	USCI input clock frequency				f _{SYSTEM}	MHz
f _{SCL}	SCL clock frequency	3 V	0		400	kHz
t _{HD,STA}	Hold time (repeated) START	3 V	4.0			μs
	f _{SCL} ≤ 100 kHz					
	f _{SCL} > 100 kHz		0.6			
t _{SU,STA}	Setup time for a repeated START	3 V	4.7			μs
	f _{SCL} ≤ 100 kHz					
	f _{SCL} > 100 kHz		0.6			
t _{HD,DAT}	Data hold time	3 V	0			ns
t _{SU,DAT}	Data setup time	3 V	250			ns
t _{SU,STO}	Setup time for STOP	3 V	4.0			μs
t _{SP}	Pulse width of spikes suppressed by input filter	3 V	50	100	600	ns

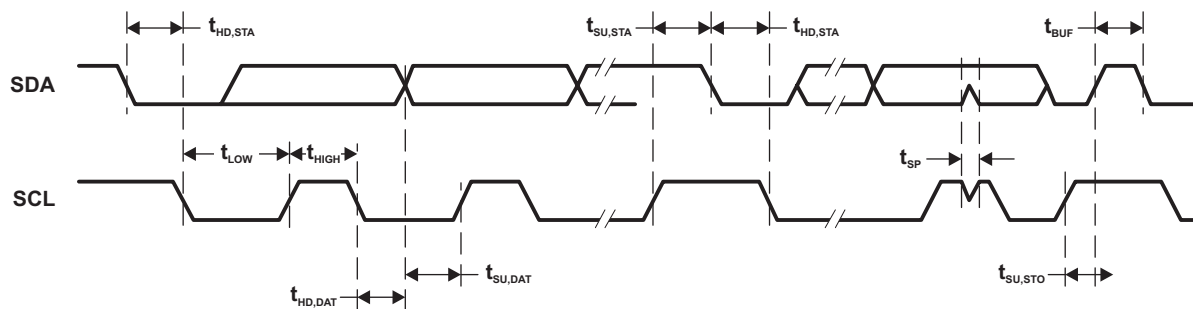


图 3-20. I2C Mode Timing

3.1.26 Comparator_A+

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _(DD) ⁽¹⁾	CAON = 1, CARSEL = 0, CAREF = 0	3 V		45		μA
I _(Refladder/ RefDiode)	CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at CA0 and CA1	3 V		45		μA
V _(IC) Common-mode input voltage	CAON = 1	3 V	0		V _{CC} -1	V
V _(Ref025) (Voltage at 0.25 V _{CC} node) / V _{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at CA0 and CA1	3 V		0.24		
V _(Ref050) (Voltage at 0.5 V _{CC} node) / V _{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at CA0 and CA1	3 V		0.48		
V _(RefVT) See 图 3-21 and 图 3-22	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at CA0 and CA1, T _A = 85°C	3 V		490		mV
V _(offset) Offset voltage ⁽²⁾		3 V		±10		mV
V _(hys) Input hysteresis	CAON = 1	3 V		0.7		mV
t _(response) Response time (low-high and high-low)	T _A = 25°C, Overdrive 10 mV, Without filter: CAF = 0	3 V		120		ns
	T _A = 25°C, Overdrive 10 mV, With filter: CAF = 1			1.5		μs

(1) The leakage current for the Comparator_A+ terminals is identical to I_{(kg(Px,y))} specification.

(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.

3.1.27 Typical Characteristics – Comparator_A+

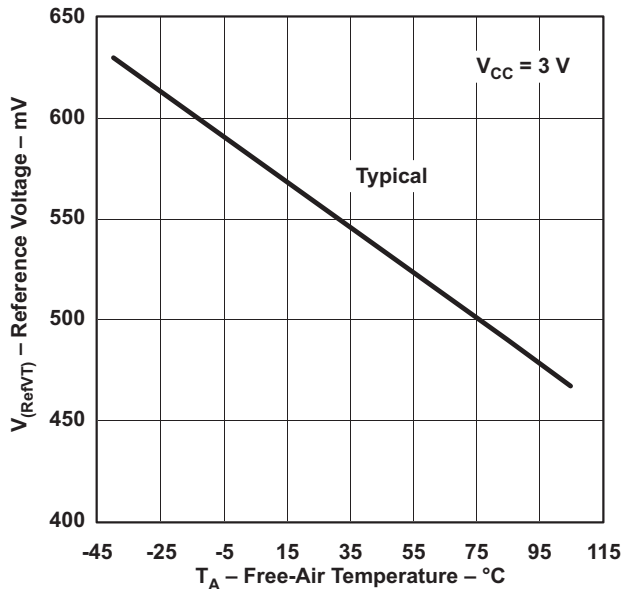


图 3-21. V_(RefVT) vs Temperature, V_{CC} = 3 V

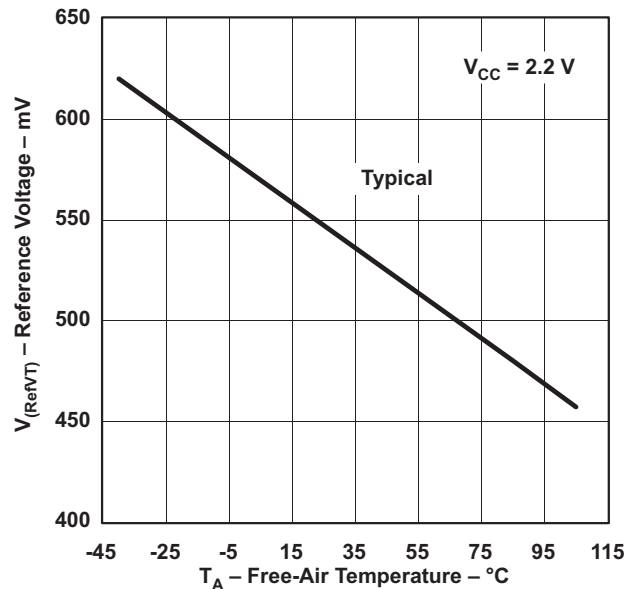


图 3-22. V_(RefVT) vs Temperature, V_{CC} = 2.2 V

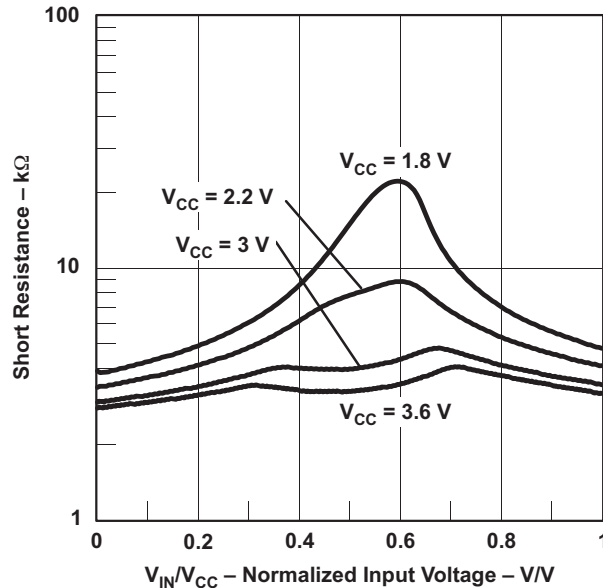


图 3-23. Short Resistance vs V_{IN}/V_{CC}

3.1.28 10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽³⁾

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC}	Analog supply voltage	V _{SS} = 0 V		2.2		3.6	V
V _{Ax}	Analog input voltage ⁽¹⁾	All Ax terminals, Analog inputs selected in ADC10AE register	3 V	0		V _{CC}	V
I _{ADC10}	ADC10 supply current ⁽²⁾	f _{ADC10CLK} = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	25°C	3 V	0.6		mA
I _{REF+}	Reference supply current, reference buffer disabled ⁽³⁾	f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	25°C	3 V	0.25		mA
		f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0			0.25		
I _{REFB,0}	Reference buffer supply current with ADC10SR = 0 ⁽³⁾	f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	25°C	3 V	1.1		mA
I _{REFB,1}	Reference buffer supply current with ADC10SR = 1 ⁽³⁾	f _{ADC10CLK} = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1	25°C	3 V	0.5		mA
C _I	Input capacitance	Only one terminal Ax can be selected at one time	25°C	3 V		27	pF
R _I	Input MUX ON resistance	0 V ≤ V _{Ax} ≤ V _{CC}	25°C	3 V	1000		Ω

- (3) The leakage current is defined in the leakage current table with Px.y/Ax parameter.
- (1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
- (2) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
- (3) The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

3.1.29 10-Bit ADC, Built-In Voltage Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
V _{CC,REF+}	Positive built-in reference analog supply voltage range	I _{VREF+} ≤ 1 mA, REF2_5V = 0		2.2			V	
		I _{VREF+} ≤ 1 mA, REF2_5V = 1		2.9				
V _{REF+}	Positive built-in reference voltage	I _{VREF+} ≤ I _{VREF+,max} , REF2_5V = 0	3 V	1.41	1.5	1.59	V	
		I _{VREF+} ≤ I _{VREF+,max} , REF2_5V = 1		2.35	2.5	2.65		
I _{LD,VREF+}	Maximum VREF+ load current		3 V			±1	mA	
	VREF+ load regulation	I _{VREF+} = 500 μA ± 100 μA, Analog input voltage V _{AX} ≠ 0.75 V, REF2_5V = 0	3 V				±2	LSB
		I _{VREF+} = 500 μA ± 100 μA, Analog input voltage V _{AX} ≠ 1.25 V, REF2_5V = 1					±2	
	VREF+ load regulation response time	I _{VREF+} = 100 μA → 900 μA, V _{AX} ≠ 0.5 × VREF+, Error of conversion result ≤ 1 LSB, ADC10SR = 0	3 V			400	ns	
C _{VREF+}	Maximum capacitance at pin VREF+	I _{VREF+} ≤ ±1 mA, REFON = 1, REFOUT = 1	3 V			100	pF	
TC _{REF+}	Temperature coefficient	I _{VREF+} = const with 0 mA ≤ I _{VREF+} ≤ 1 mA	3 V			±100	ppm/°C	
t _{REFON}	Settling time of internal reference voltage to 99.9% VREF	I _{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 → 1	3.6 V			30	μs	
t _{REFBURST}	Settling time of reference buffer to 99.9% VREF	I _{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1, ADC10SR = 0	3 V			2	μs	

3.1.30 10-Bit ADC, External Reference⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{REF+}	Positive external reference input voltage range ⁽¹⁾	V _{REF+} > V _{REF-} , SREF1 = 1, SREF0 = 0		1.4		V _{CC}	V
		V _{REF-} ≤ V _{REF+} ≤ V _{CC} - 0.15 V, SREF1 = 1, SREF0 = 1 ⁽²⁾		1.4		3	
V _{REF-}	Negative external reference input voltage range ⁽³⁾	V _{REF+} > V _{REF-}		0		1.2	V
ΔV _{REF}	Differential external reference input voltage range, ΔV _{REF} = V _{REF+} - V _{REF-}	V _{REF+} > V _{REF-} ⁽⁴⁾		1.4		V _{CC}	V
I _{VREF+}	Static input current into VREF+	0 V ≤ V _{REF+} ≤ V _{CC} , SREF1 = 1, SREF0 = 0	3 V			±1	μA
		0 V ≤ V _{REF+} ≤ V _{CC} - 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1 ⁽²⁾	3 V			0	
I _{VREF-}	Static input current into VREF-	0 V ≤ V _{REF-} ≤ V _{CC}	3 V			±1	μA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C₁, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.

(1) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.

(2) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REFBURST = 1.

(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.

(4) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

3.1.31 10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{ADC10CLK}	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	3 V	0.45		6.3	MHz
		ADC10SR = 0 ADC10SR = 1		0.45		1.5	
f _{ADC10OSC}	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, f _{ADC10CLK} = f _{ADC10OSC}	3 V	3.7		6.3	MHz
t _{CONVERT}	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, f _{ADC10CLK} = f _{ADC10OSC} f _{ADC10CLK} from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0	3 V	2.06		3.51	μs
				13 × ADC10DIV × 1/f _{ADC10CLK}			
t _{ADC10ON}	Turn-on settling time of the ADC	(1)				100	ns

(1) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.

3.1.32 10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
E _I	Integral linearity error		3 V			±1	LSB
E _D	Differential linearity error		3 V			±1	LSB
E _O	Offset error	Source impedance R _S < 100 Ω	3 V			±1	LSB
E _G	Gain error		3 V		±1.1	±2	LSB
E _T	Total unadjusted error		3 V		±2	±5	LSB

3.1.33 10-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{SENSOR}	Temperature sensor supply current ⁽¹⁾	REFON = 0, INCHx = 0Ah, T _A = 25°C	3 V		60		μA
TC _{SENSOR}		ADC10ON = 1, INCHx = 0Ah ⁽²⁾	3 V		3.55		mV/°C
t _{Sensor(sample)}	Sample time required if channel 10 is selected ⁽³⁾	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	3 V	30			μs
I _{VMID}	Current into divider at channel 11	ADC10ON = 1, INCHx = 0Bh	3 V			⁽⁴⁾	μA
V _{MID}	V _{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, V _{MID} ≠ 0.5 × V _{CC}	3 V		1.5		V
t _{VMID(sample)}	Sample time required if channel 11 is selected ⁽⁵⁾	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	3 V	1220			ns

(1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).

(2) The following formula can be used to calculate the temperature sensor output voltage:

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} (273 + T [^{\circ}\text{C}]) + V_{\text{Offset,sensor}} [\text{mV}] \text{ or } \\ V_{\text{Sensor,typ}} = TC_{\text{Sensor}} T [^{\circ}\text{C}] + V_{\text{Sensor}}(T_A = 0^{\circ}\text{C}) [\text{mV}]$$

(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.

(4) No additional current is needed. The V_{MID} is used during sampling.

(5) The on-time t_{VMID(on)} is included in the sampling time t_{VMID(sample)}; no additional on time is needed.

3.1.34 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC(PGM/ERASE)}	Program and erase supply voltage			2.2		3.6	V
f _{FTG}	Flash timing generator frequency			257		476	kHz
I _{PGM}	Supply current from V _{CC} during program		2.2 V/3.6 V		1	5	mA
I _{ERASE}	Supply current from V _{CC} during erase		2.2 V/3.6 V		1	7	mA
t _{CPT}	Cumulative program time ⁽¹⁾		2.2 V/3.6 V			10	ms
t _{CMErase}	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/erase endurance			10 ⁴	10 ⁵		cycles
t _{Retention}	Data retention duration	T _J = 25°C		100			years
t _{Word}	Word or byte program time	(2)			30		t _{FTG}
t _{Block, 0}	Block program time for first byte or word	(2)			25		t _{FTG}
t _{Block, 1-63}	Block program time for each additional byte or word	(2)			18		t _{FTG}
t _{Block, End}	Block program end-sequence wait time	(2)			6		t _{FTG}
t _{Mass Erase}	Mass erase time	(2)			10593		t _{FTG}
t _{Seg Erase}	Segment erase time	(2)			4819		t _{FTG}

- (1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
- (2) These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

3.1.35 RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _(RAMh)	RAM retention supply voltage ⁽¹⁾	CPU halted	1.6		V

- (1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

3.1.36 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{SBW}	Spy-Bi-Wire input frequency		2.2 V	0		20	MHz
t _{SBW,Low}	Spy-Bi-Wire low clock pulse length		2.2 V	0.025		15	μs
t _{SBW,En}	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge ⁽¹⁾)		2.2 V			1	μs
t _{SBW,Ret}	Spy-Bi-Wire return to normal operation time		2.2 V	15		100	μs
f _{TCK}	TCK input frequency ⁽²⁾		2.2 V	0		5	MHz
R _{Internal}	Internal pulldown resistance on TEST		2.2 V	25	60	90	kΩ

- (1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum t_{SBW,En} time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
- (2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

3.1.37 JTAG Fuse⁽³⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _{CC(FB)}	Supply voltage during fuse-blow condition	T _A = 25°C	2.5		V
V _{FB}	Voltage level on TEST for fuse blow		6	7	V
I _{FB}	Supply current into TEST during fuse blow			100	mA

- (3) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t _{FB}	Time to blow fuse			1	ms

3.2 MSP430 Core Operation

注

For support and specific questions related to the MSP430 in the TPS65835 device, please refer to TI's E2E PMU forum and post relevant questions to the forum at the following link:

[TI E2E PMU Forum.](#)

Please format your posting as follows:

- **Title:** TPS65835 "specific topic"
- **Body:** Question, with supporting code and oscilloscope screen captures if applicable.

3.2.1 Description

The MSP430 integrated into the TPS65835 is from the MSP430x2xx family of ultralow-power microcontrollers. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1_μs. The list of the peripherals and modules included in this MSP430 are as follows:

- Up to 16 MHz CPU
- 16 kB Flash Memory
- 512 B RAM
- Basic Clock Module
 - Internal Frequencies up to 16 MHz with one Calibrated Frequency
 - Internal Very-Low-Power Low-Frequency (LF) Oscillator
 - 32 kHz Crystal Support
 - External Digital Clock Source
- 10-Bit ADC
 - 200-ksps Analog-to-Digital (A/D) Converter with Internal Reference, Sample-and-Hold, and Autoscan
- Comparator A+ (Comp_A+)
 - For Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion
- Timer0_A3 and Timer1_A3
 - Up to Two 16-Bit Timer_A with Three Capture/Compare Registers
- Watchdog WDT+
- USCI A0, Universal Serial Communication Interface
 - Enhanced UART Supporting Auto baudrate Detection (LIN)
 - IrDA Encoder and Decoder
 - Synchronous SPI
 - I²C
- USCI B0, Universal Serial Communication Interface
 - Synchronous SPI
 - I²C
- JTAG / Spy-By-Wire

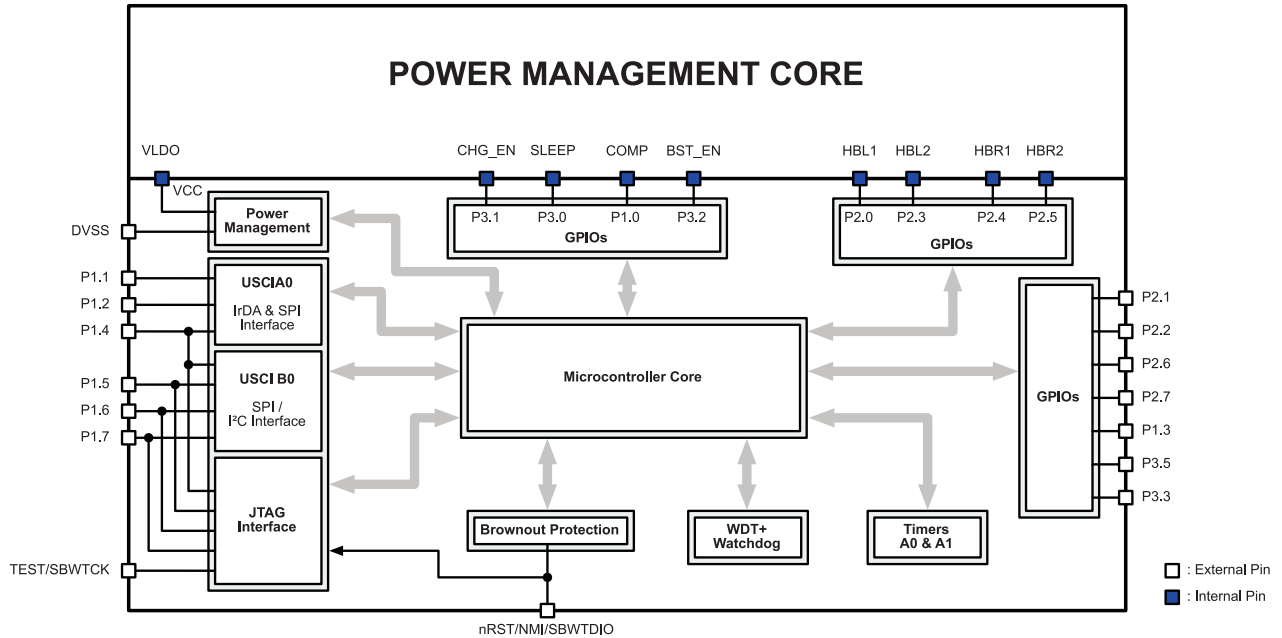


图 3-24. MSP430 Functional Block Diagram

3.2.2 Accessible MSP430 Pins

There are a number of internal pins connected between the MSP430 core and the power management core as well as external pins on the MSP430. Internal pins are not available externally but can be controlled by the MSP430 core in various ways. A table describing all available MSP430 pin functions (表 3-1) along with a block diagram detailing the MSP430 core and the pin connectivity (see 图 3-24) has been made available.

表 3-1. Internally Connected Pins: MSP430 to Power Management Core

Power Management Core Pin	MSP430 Core Pin	Functionality
VLDO	AVCC / DVCC	Voltage supplied by LDO on power management core, connected to MSP430 power management module Enabled by SWITCH pin input
COMP	P1.0 / A0 / CA0	Scaled down voltage of the BAT pin. Connected to Comparator_A+ channel CA0 or ADC channel A0 of the MSP430 To use "COMP" and Comp_A+ module function of the MSP430, the pin must be configured properly DO NOT CONFIGURE THIS PIN AS A GPIO AND PULL THIS PIN UP OR DOWN, THIS WILL INCREASE THE OPERATING CURRENT OF THE DEVICE
BST_EN	P3.2	Enable pin for the boost on the power management core, ACTIVE HIGH
CHG_EN	P3.1	Enable pin for the charger on the power management core, ACTIVE HIGH
SLEEP	P3.0	Can put entire device into SLEEP state dependent upon system events, e.g., extended loss of IR or RF synchronization ⁽¹⁾
HBL1	P2.0	Control pin 1 for left frame of active shutter glasses
HBL2	P2.3	Control pin 2 for left frame of active shutter glasses
HBR1	P2.4	Control pin 1 for right frame of active shutter glasses
HBR2	P2.5	Control pin 2 for right frame of active shutter glasses

(1) Note that the SLEEP signal can not be used to wake the system if it is already in the SLEEP state since the LDO used to power the MSP430 would be disabled in this state.

表 3-2. Externally Available MSP430 Pins

Pin Name	I/O	Functionality
P1.1/ TA0.0/ UCA0RXD/ UCA0SOMI/ A1/ CA1	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI0A input, compare: Out0 output USCI_A0 receive data input in UART mode USCI_A0 slave data out/master in SPI mode ADC10 analog input A1 Comparator_A+, CA1 input
P1.2/ TA0.1/ UCA0TXD/ UCA0SIMO/ A2/ CA2	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI1A input, compare: Out1 output USCI_A0 transmit data output in UART mode USCI_A0 slave data in/master out in SPI mode ADC10 analog input A2 Comparator_A+, CA2 input
P1.3/ ADC10CLK/ A3 VREF-/VEREF-/ CA3/ CAOUT	I/O	General-purpose digital I/O pin ADC10, conversion clock output ADC10 analog input A3 ADC10 negative reference voltage Comparator_A+, CA3 input Comparator_A+, output
P1.4/ SMCLK/ UCB0STE UCA0CLK/ A4 VREF+/VEREF+/ CA4 TCK	I/O	General-purpose digital I/O pin SMCLK signal output USCI_B0 slave transmit enable USCI_A0 clock input/output ADC10 analog input A4 ADC10 positive reference voltage Comparator_A+, CA4 input JTAG test clock, input terminal for device programming and test
P1.5/ TA0.0/ UCB0CLK/ UCA0STE/ A5/ CA5/ TMS	I/O	General-purpose digital I/O pin Timer0_A, compare: Out0 output USCI_B0 clock input/output USCI_A0 slave transmit enable ADC10 analog input A5 Comparator_A+, CA5 input JTAG test mode select, input terminal for device programming and test
P1.6/ TA0.1/ A6/ CA6/ UCB0SOMI/ UCB0SCL/ TDI/TCLK	I/O	General-purpose digital I/O pin Timer0_A, compare: Out1 output ADC10 analog input A6 Comparator_A+, CA6 input USCI_B0 slave out/master in SPI mode USCI_B0 SCL I2C clock in I2C mode JTAG test data input or test clock input during programming and test
P1.7/ A7/ CA7/ CAOUT/ UCB0SIMO/ UCB0SDA/ TDO/TDI	I/O	General-purpose digital I/O pin ADC10 analog input A7 Comparator_A+, CA7 input Comparator_A+, output USCI_B0 slave in/master out in SPI mode USCI_B0 SDA I2C data in I2C mode JTAG test data output terminal or test data input during programming and test ⁽¹⁾
P2.1/ TA1.1	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI1A input, compare: Out1 output
P2.2/ TA1.1	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI1B input, compare: Out1 output
P2.6/ XIN/ TA0.1	I/O	General-purpose digital I/O pin XIN, Input terminal of crystal oscillator TA0.1, Timer0_A, compare: Out1 output
P2.7/ XOUT	I/O	General-purpose digital I/O pin Output terminal of crystal oscillator ⁽²⁾
P3.3/ TA1.2	I/O	General-purpose digital I/O pin Timer1_A, compare: Out2 output
P3.5/ TA0.1	I/O	General-purpose digital I/O pin Timer0_A, compare: Out0 output

(1) TDO or TDI is selected via JTAG instruction.

(2) If P2.7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

表 3-2. Externally Available MSP430 Pins (continued)

Pin Name	I/O	Functionality
nRST/ NMI/ SBWTDIO	I	Reset Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTCK	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DVSS	N/A	MSP430 ground reference

3.2.3 MSP430 Port Functions and Programming Options

This section details the programming options that are available for each of the pins that are accessible on the MSP430.

表 3-3. Internal MSP430 Pin Functions and Programming Options

PIN NAME (P_x) ⁽¹⁾	x	FUNCTION	MSP430 CONTROL BITS / SIGNALS ⁽²⁾				
			P_DIR.x	P_SEL.x	P_SEL2.x	ADC10AE.x INCH.x=1	CAPD.y
P1.0/ A0/ CA0	0	P1.x (I/O)	I: 0; O: 1	0	0	0	0
		A0	X	X	X	1 (y = 0)	0
		CA0	X	X	X	0	1 (y = 0)
P2.0/ TA1.0	0	P2.x (I/O), HBL1 internal signal	I: 0; O: 1	0	0	—	—
		Timer1_A3.TA0	1	1	0	—	—
P2.3/ TA1.0	3	P2.x (I/O), HBL2 internal signal	I: 0; O: 1	0	0	—	—
		Timer1_A3.TA0	1	1	0	—	—
P2.4/ TA1.2	4	P2.x (I/O), HBR1 internal signal	I: 0; O: 1	0	0	—	—
		Timer1_A3.TA2	1	1	0	—	—
P2.5/ TA1.2	5	P2.x (I/O), HBR2 internal signal	I: 0; O: 1	0	0	—	—
		Timer1_A3.TA2	1	1	0	—	—
P3.0/ TA0.2	0	P3.x (I/O), SLEEP signal	I: 0; O: 1	0	0	—	—
		Timer0_A3.TA2	1	1	0	—	—
P3.1/ TA1.2	1	P3.x (I/O), CHG_EN signal, ACTIVE HIGH	I: 0; O: 1	0	0	—	—
		Timer1_A3.TA2	1	1	0	—	—
P3.2/ TA1.2	2	P3.x (I/O), BST_EN signal, ACTIVE HIGH	I: 0; O: 1	0	0	—	—
		Timer1_A3.TA2	1	1	0	—	—

(1) Example: To program port P2.0, the appropriate control bits and MSP430 signals would need to be referenced as "P2DIR.0", "P2SEL.0", and "P2SEL2.0".

(2) X = don't care, — = not applicable

表 3-4. External MSP430 Port 1 Functions and Programming Options

PIN NAME (P1.x) ⁽¹⁾	x	FUNCTION	MSP430 CONTROL BITS / SIGNALS ⁽²⁾				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1	CAPD.y
P1.1/ TA0.0/ UCA0RXD/ UCA0SOMI/ A1/ CA1/ Pin Osc	1	P1.x (I/O)	I: 0; O: 1	0	0	0	0
		TA0.0	1	1	0	0	0
		TA0.CCI0A	0	1	0	0	0
		UCA0RXD	from USCI	1	1	0	0
		UCA0SOMI	from USCI	1	1	0	0
		A1	X	X	X	1 (y = 1)	0
		CA1	X	X	X	0	1 (y = 1)
		Capacitive sensing	X	0	1	0	0
P1.2/ TA0.1/ UCA0TXD/ UCA0SIMO/ A2/ CA2/ Pin Osc	2	P1.x (I/O)	I: 0; O: 1	0	0	0	0
		TA0.1	1	1	0	0	0
		TA0.CCI1A	0	1	0	0	0
		UCA0TXD	from USCI	1	1	0	0
		UCA0SIMO	from USCI	1	1	0	0
		A2	X	X	X	1 (y = 2)	0
		CA2	X	X	X	0	1 (y = 2)
		Capacitive sensing	X	0	1	0	0
P1.3/ ADC10CLK/ A3/ VREF-/ VEREF-/ CA3 Pin Osc	3	P1.x (I/O)	I: 0; O: 1	0	0	0	0
		ADC10CLK	1	1	0	0	0
		A3	X	X	X	1 (y = 3)	0
		VREF-	X	X	X	1	0
		VEREF-	X	X	X	1	0
		CA3	X	X	X	0	1 (y = 3)
		Capacitive sensing	X	0	1	0	0
		P1.4/ SMCLK/ UCB0STE/ UCA0CLK/ VREF+/ VEREF+/ A4/ CA4/ TCK/ Pin Osc	4	P1.x (I/O)	I: 0; O: 1	0	0
SMCLK	1			1	0	0	0
UCB0STE	from USCI			1	1	1 (y = 4)	0
UCA0CLK	from USCI			1	1	1 (y = 4)	0
VREF+	X			X	X	1	0
VEREF+	X			X	X	1	0
A4	X			X	X	1 (y = 4)	0
CA4	X			X	X	0	1 (y = 4)
TCK (JTAG Mode = 1)	X			X	X	0	0
Capacitive sensing	X			0	1	0	0
P1.5/ TA0.0/ UCB0CLK/ UCA0STE/ A5/ CA5/ TMS/ Pin Osc	5	P1.x (I/O)	I: 0; O: 1	0	0	0	0
		TA0.0	1	1	0	0	0
		UCB0CLK	from USCI	1	1	0	0
		UCA0STE	from USCI	1	1	0	0
		A5	X	X	X	1 (y = 5)	0
		CA5	X	X	X	0	1 (y = 5)
		TMS (JTAG Mode = 1)	X	X	X	0	0
		Capacitive sensing	X	0	1	0	0

(1) Example: To program port P1.1, the appropriate control bits and MSP430 signals would need to be referenced as "P1DIR.1", "P1SEL.1", and "P1SEL2.1".

(2) X = don't care

表 3-4. External MSP430 Port 1 Functions and Programming Options (continued)

PIN NAME (P1.x) ⁽¹⁾	x	FUNCTION	MSP430 CONTROL BITS / SIGNALS ⁽²⁾				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1	CAPD.y
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0
UCB0SOMI/		UCB0SOMI	from USCI	1	1	0	0
UCB0SCL/		UCB0SCL	from USCI	1	1	0	0
A6/		A6	X	X	X	1 (y = 6)	0
CA6/		CA6	X	X	X	0	1 (y = 6)
TDI/TCLK/		TDI/TCLK (JTAG Mode = 1)	X	X	X	0	0
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0	0	0
UCB0SIMO/		UCB0SIMO	from USCI	1	1	0	0
UCB0SDA/		UCB0SDA	from USCI	1	1	0	0
A7/		A7	X	X	X	1 (y = 7)	0
CA7/		CA7	X	X	X	0	1 (y = 7)
CAOUT/		CAOUT	1	1	0	0	0
TDO/TDI/		TDO/TDI (JTAG Mode = 1)	X	X	X	0	0
Pin Osc		Capacitive sensing	X	0	1	0	0

表 3-5. External MSP430 Port 2 Functions and Programming Options

PIN NAME (P2.x) ⁽¹⁾	x	FUNCTION	MSP430 CONTROL BITS / SIGNALS ⁽²⁾		
			P2DIR.x	P2SEL.x	P2SEL2.x
P2.1/	1	P2.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.CCI1A	0	1	0
		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.2/	2	P2.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.CCI1B	0	1	0
		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.6/	6	P2.x (I/O)	I: 0; O: 1	0	0
XIN/		XIN, LFXT1 Oscillator Input	0	1	0
TA0.1/		Timer0_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.7/	7	P2.x (I/O)	I: 0; O: 1	0	0
XOUT/		XOUT, LFXT1 Oscillator Output	1	1	0
Pin Osc		Capacitive sensing	X	0	1

(1) Example: To program port P2.1, the appropriate control bits and MSP430 signals would need to be referenced as "P2DIR.1", "P2SEL.1", and "P2SEL2.1".

(2) X = don't care

表 3-6. External MSP430 Port 3 Functions and Programming Options

PIN NAME (P3.x) ⁽¹⁾	x	FUNCTION	MSP430 CONTROL BITS / SIGNALS ⁽²⁾		
			P3DIR.x	P3SEL.x	P3SEL2.x
P3.3/ TA1.1/ Pin Osc	3	P3.x (I/O)	I: 0; O: 1	0	0
Timer1_A3.TA2		1	1	0	
Capacitive sensing		X	0	1	
P3.5/ TA1.1/ Pin Osc	5	P3.x (I/O)	I: 0; O: 1	0	0
Timer0_A3.TA2		1	1	0	
Capacitive sensing		X	0	1	

(1) Example: To program port P3.3, the appropriate control bits and MSP430 signals would need to be referenced as "P3DIR.3", "P3SEL.3", and "P3SEL2.3".

(2) X = don't care

3.2.4 Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
 - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator is disabled
 - Crystal oscillator is stopped

3.2.5 MSP430x2xx User's Guide

To view the user's guide for the MSP430 integrated into this device, see [MSP430x2xx Family User's Guide](#). The list of peripherals found in this MSP430 is listed in the section: [节 3.2.1](#).

4 APPLICATION INFORMATION

4.1 Applications Schematic

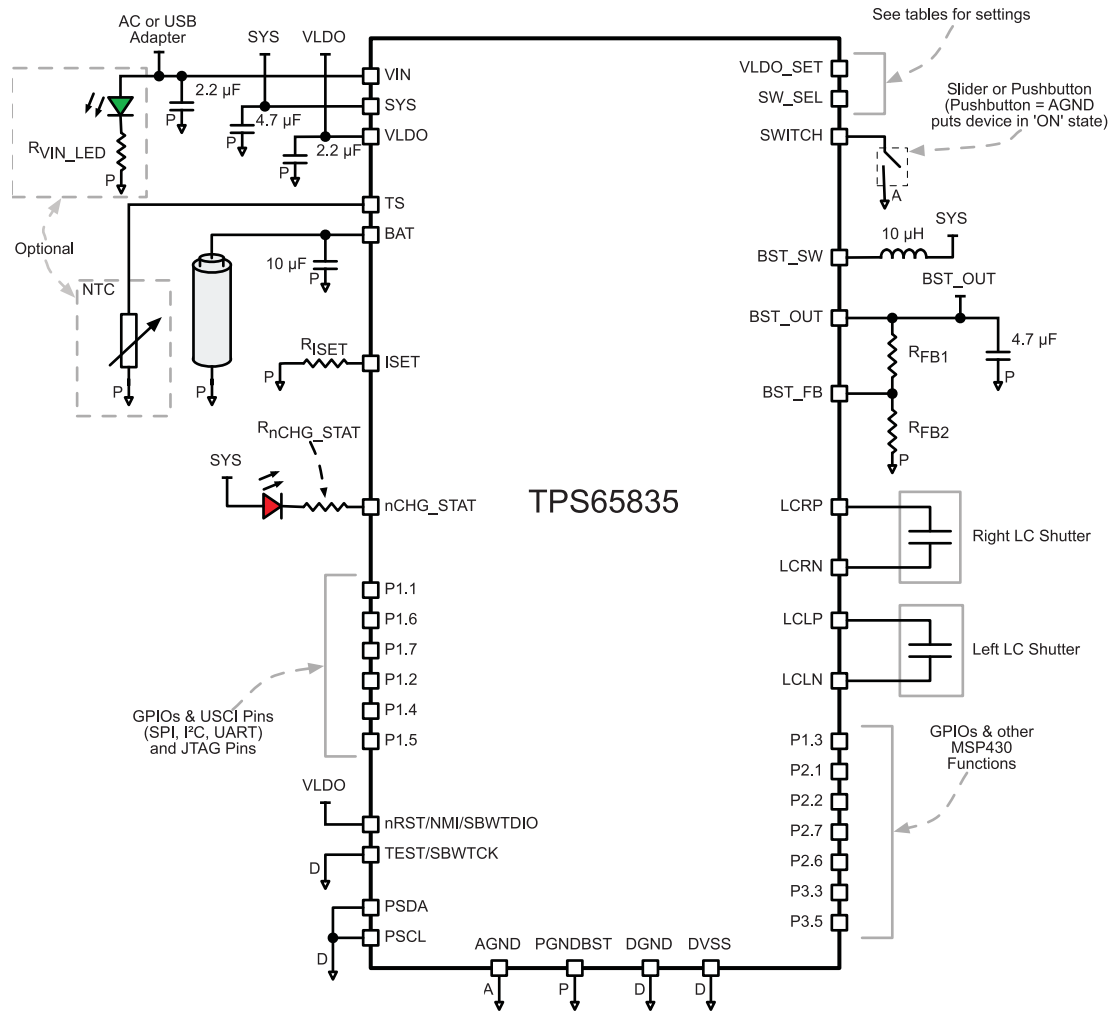


图 4-1. TPS65835 Applications Schematic

4.2 Boost Converter Application Information

4.2.1 Setting Boost Output Voltage

To set the boost converter output voltage of this device, two external resistors that form a feedback network are required. The values recommended below (in 表 4-1) are given for a desired quiescent current of 5 μA when the boost is enabled and switching. See 图 4-2 for the detail of the applications schematic that shows the boost feedback network and the resistor names used in the table below.

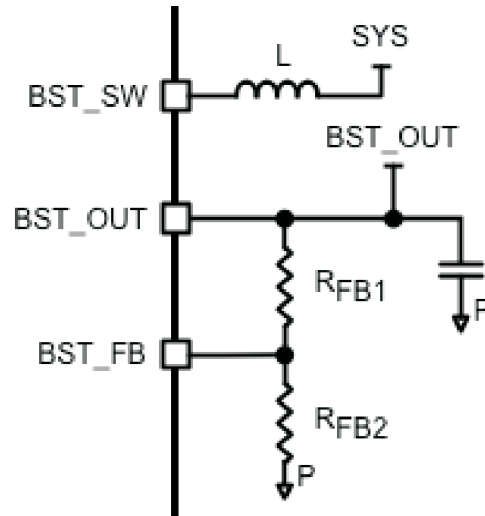


图 4-2. Boost Feedback Network Schematic

表 4-1. Recommended R_{FB1} and R_{FB2} Values (for $I_{Q(FB)} = 5 \mu A$)

Targeted V_{BST_OUT}	$R_{FB1}^{(1)}$	$R_{FB2}^{(1)}$
8 V	1.3 M Ω	240 k Ω
10 V	1.8 M Ω	240 k Ω
12 V	2.2 M Ω	240 k Ω
14 V	2.4 M Ω	240 k Ω
16 V	3.0 M Ω	240 k Ω

(1) Resistance values given in closest standard value (5% tolerance, E24 grouping).

These resistance values can also be calculated using the following information. To start, it is helpful to target a quiescent current through the boost feedback network while the device is operating ($I_{Q(FB)}$). When the boost output voltage and this targeted quiescent current is known, the total feedback network resistance can be found.

The value for R_{FB2} can be found by using the boost feedback pin voltage ($V_{FB} = 1.2$ V, see "Electrical Characteristics" in 节 2) and $I_{Q(FB)}$ in the following equation:

$$R_{FB1} + R_{FB2} = V_{BST_OUT} / I_{Q(FB)}$$

$$R_{FB2} = (1.2 \text{ V}) / I_{Q(FB)}$$

To find R_{FB1} , simply subtract the R_{FB2} from $R_{FB(TOT)}$:

$$R_{FB1} = R_{FB(TOT)} - R_{FB2}$$

4.2.2 Boost Inductor Selection

The selection of the boost inductor and output capacitor is very important to the performance of the boost converter. The boost has been designed for optimized operation when a 10 μH inductor is used. Smaller inductors, down to 4.7 μH , may be used but there will be a slight loss in overall operating efficiency. A few inductors that have been tested and found to give good performance can be found in the list below:

Recommended 10 μH inductors

- TDK VLS201612ET-100M (10 μH , $I_{MAX} = 0.53$ A, $R_{DC} = 0.85 \Omega$)
- Taiyo Yuden CBC2016B100M (10 μH , $I_{MAX} = 0.41$ A, $R_{DC} = 0.82 \Omega$)

4.2.3 Boost Capacitor Selection

The recommended minimum value for the capacitor on the boost output, BST_OUT pin, is 4.7 μ F. Values that are larger can be used with the measurable impact being a slight reduction in the boost converter output voltage ripple while values smaller than this will result in an increased boost output voltage ripple. Note that the voltage rating of the capacitor should be sized for the maximum expected voltage at the BST_OUT pin.

4.3 Bypassing Default Push-Button SWITCH Functionality

If the SWITCH pin functionality is not required to power on and off the device because of different system requirements (SWITCH timing requirements of system will be controlled by the internal MSP430), then the feature can be bypassed. The following diagram shows the connections required for this configuration.

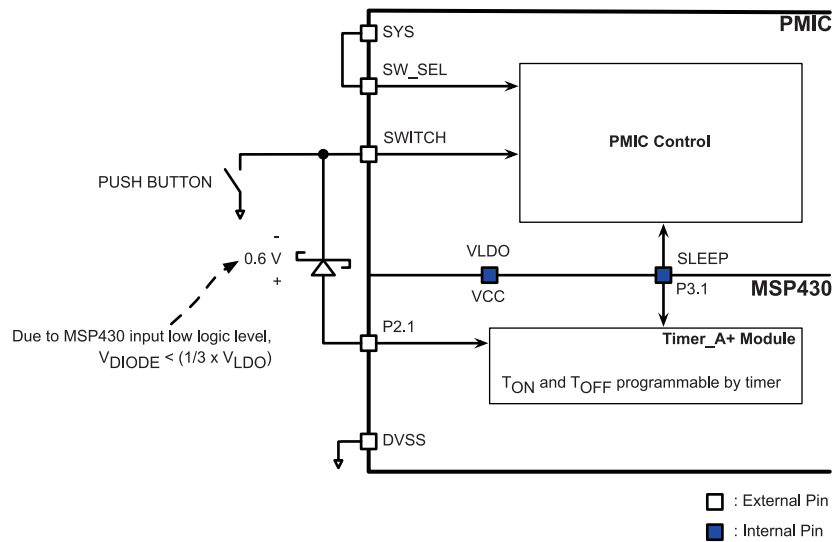


图 4-3. Bypassing Default TPS65835 Push Button SWITCH Timing

In a system where a different push-button SWITCH off timing is required, the SLEEP pin is used to control the power off of the device. After system power up, the MCU must force the SLEEP pin to a high state ($V_{SLEEP} > V_{IH(PMIC)}$). Once the SWITCH push-button is pressed to shut the system down, a timer in the MCU should be active and counting the desired t_{OFF} time of the device. Once this t_{OFF} time is detected, the MCU can assert the SLEEP signal to a logic low level ($V_{SLEEP} < V_{IL(PMIC)}$). It is on the falling edge of the SLEEP signal where the system will be powered off (see 图 4-4)

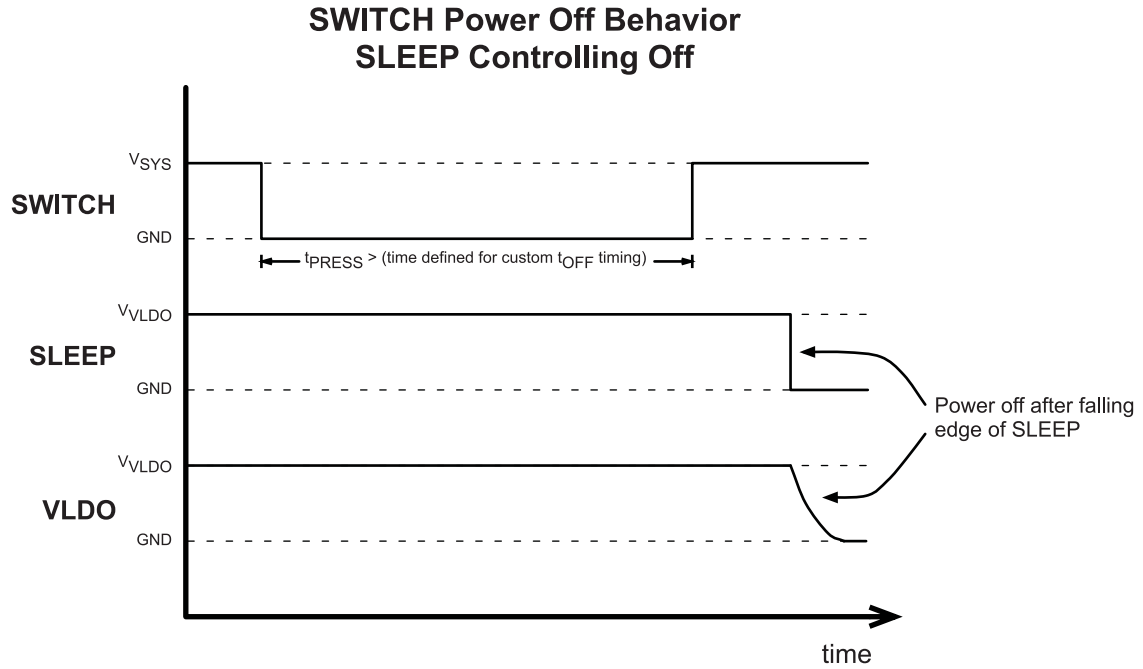


图 4-4. SWITCH Press and SLEEP Signal to Control System Power Off

4.4 MSP430 Programming

In order to program the integrated MSP430 in the TPS65835 device, ensure that the programming environment supports the TPS65835 device.

4.4.1 Code To Setup Power Functions

This section will detail a basic code to control the MSP430 in the TPS65835 and how to configure the power functions and control the power die. Please reference [表 3-3](#) for the details on configuring the MSP430 pins. Note that `"/` is a comment and this code was written using Code Composer Studio in C.

```
// SETUP H-BRIDGE PINS
P2DIR |= (BIT5 + BIT4 + BIT3 + BIT0); // Set PxDIR to 1 for outputs
P2REN |= (BIT5 + BIT4 + BIT3 + BIT0); // Enable pullup/pulldown resistors on outputs

// SETUP SLEEP, CHG_EN, AND BST_EN
P3DIR |= (BIT2 + BIT1 + BIT0); // Set PxDIR to 1 for outputs
P3REN |= (BIT2 + BIT1 + BIT0); // Enable pullup/pulldown resistors on outputs
```

The previous code setup the power pins for outputs, now they must be controlled with MSP430 code. Refer to the following code to perform initial setup and to control the power functions (SLEEP, CHG_EN, and BST_EN):

```
P3OUT &= ~BIT0; // Set SLEEP mode signal low; SLEEP Function is disabled
// P3OUT |= BIT0; // Set SLEEP mode signal high (sleep control via MSP430)

// P3OUT &= ~BIT1; // Set CHG_EN signal low (disable charger)
P3OUT |= BIT1; // Set CHG_EN signal high (enable charger)

// P3OUT &= ~BIT2; // Set BST_EN low (disable boost)
P3OUT |= BIT2; // Set BST_EN high (enable boost)
```

The H-Bridge pins can be controlled in a similar manner (see [节 2.10.1](#)). The following code is only meant to cover each H-Bridge mode of operation and the appropriate code needed to put it in that state:

```
// BOTH SIDES IN OPEN STATE
P2OUT &= ~(BIT3 + BIT0); // HBL2 = 0, HBL1 = 0
P2OUT &= ~(BIT5 + BIT4); // HBR2 = 0, HBR1 = 0

// BOTH SIDES IN GROUNDED STATE
P2OUT |= BIT3 + BIT0; // HBL2 = 1, HBL1 = 1
P2OUT |= BIT5 + BIT4; // HBR2 = 1, HBR1 = 1



// LEFT SIDE IN CHARGE+ STATE
P2OUT &= ~BIT3; P2OUT |= BIT0; // HBL2 = 0, HBL1 = 1

// LEFT SIDE IN CHARGE- STATE
P2OUT |= BIT3; P2OUT &= ~BIT0; // HBL2 = 1, HBL1 = 0

// RIGHT SIDE IN CHARGE+ STATE
P2OUT &= ~BIT5; P2OUT |= BIT4; // HBR2 = 0, HBR1 = 1

// RIGHT SIDE IN CHARGE- STATE
P2OUT |= BIT5; P2OUT &= ~BIT4; // HBR2 = 1, HBR1 = 0
```

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65835RKPR	ACTIVE	VQFN	RKP	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65835	
TPS65835RKPT	ACTIVE	VQFN	RKP	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65835	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

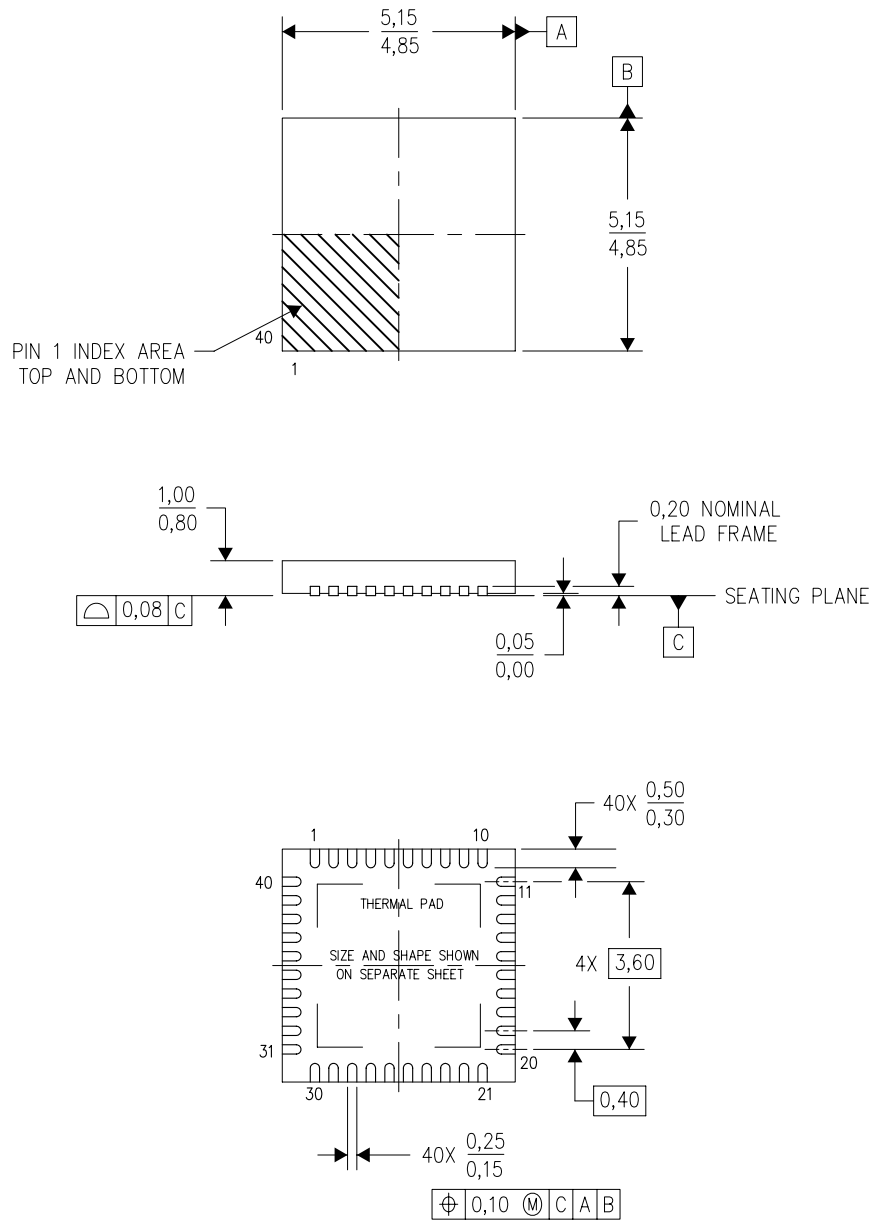
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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RKP (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4211175/B 01/12

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RKP (S-PVQFN-N40)

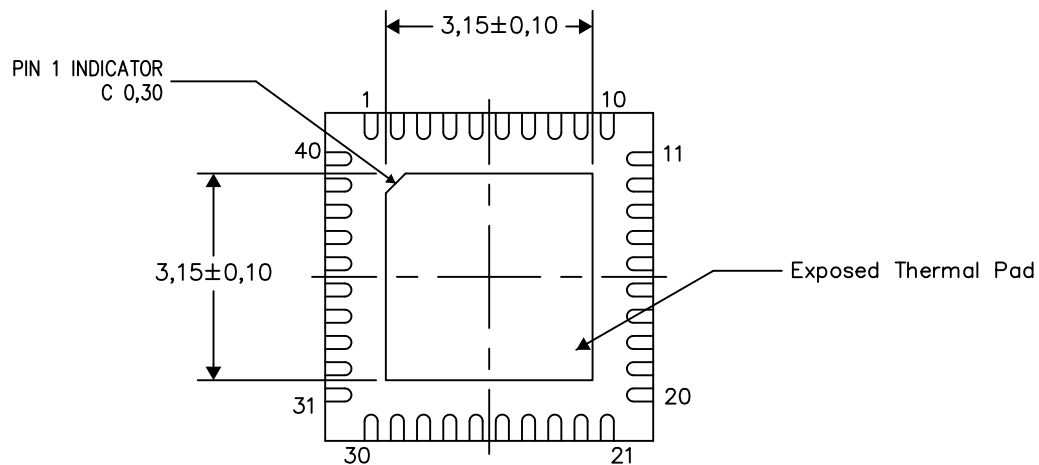
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

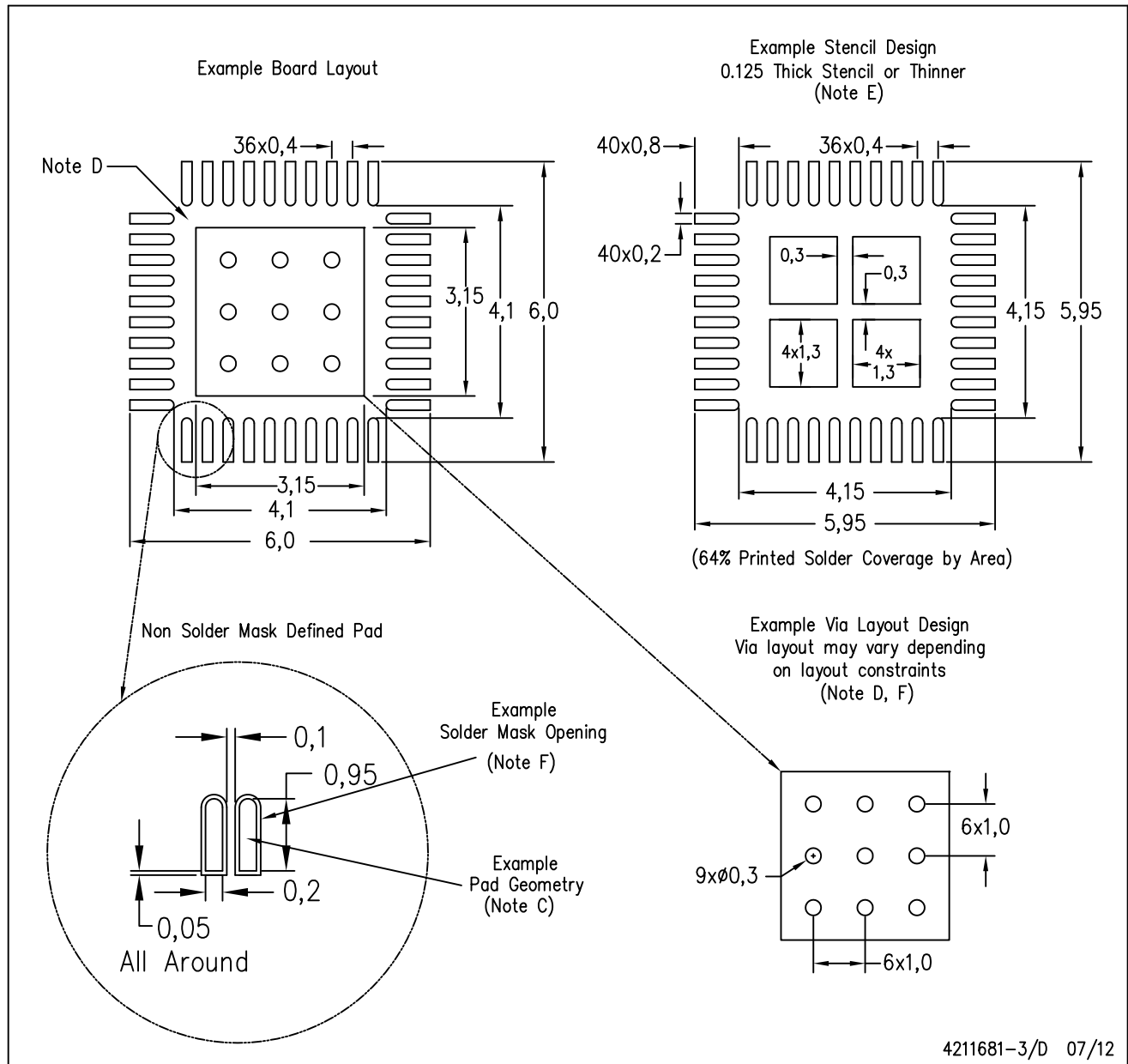
Exposed Thermal Pad Dimensions

4211176-3/H 06/12

NOTE: All linear dimensions are in millimeters

RKP (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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