SM74104 具有自适应延迟的高压半桥栅极驱动器

1 特性

- 可再生能源等级
- 可驱动高侧和低侧 N 沟道金属氧化物半导体场效应晶体管 (MOSFET)
- 具有可编程附加延迟的自适应上升沿和下降沿
- 单输入控制
- 自举电源电压高达 118VDC
- 短暂关断传播延迟（典型值为 25ns）
- 可以 15ns 的上升和下降时间驱动 1000pF 负载
- 电源轨欠压锁定

2 典型应用

- 电流反馈推挽式电源转换器
- 高电压降压稳压器
- 有源钳位正激电源转换器
- 半桥和全桥转换器

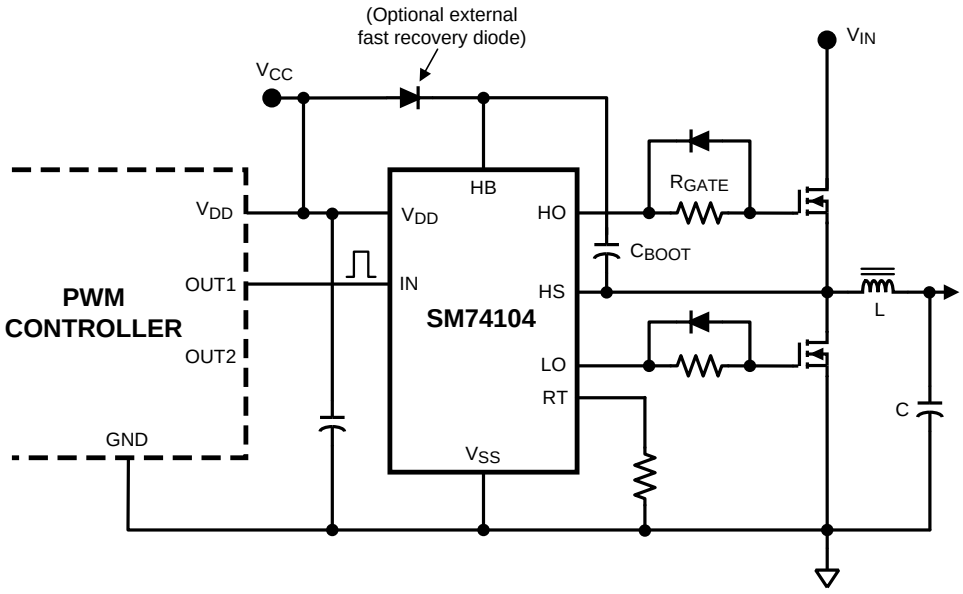
3 说明

SM74104 高压栅极驱动器设计用于驱动采用同步降压配置的高侧和低侧 N 沟道 MOSFET。 该悬空高侧驱动器能够在高达 100V 的电源电压下工作。 高侧和低侧栅极驱动器由单个输入控制。 该器件采用自适应方式来控制每一个状态变化，从而避免发生击穿。 除了自适应转换时序之外，还可以添加与外部设置电阻成比例的附加延时。 该器件集成了一个高压二极管，用于对高侧栅极驱动自举电容进行充电。 稳健可靠的电平转换器同时拥有高运行速度和低功耗特性，并且可提供从控制逻辑到高侧栅极驱动器的干净电平转换。 该器件在低侧和高侧电源轨上提供了欠压锁定功能。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SM74104	WSON (10)	4.0mm x 4.0mm
	SOIC (8)	4.9mm x 3.9mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



SM74104 驱动采用同步降压配置进行连接的 MOSFET

目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D **Page**

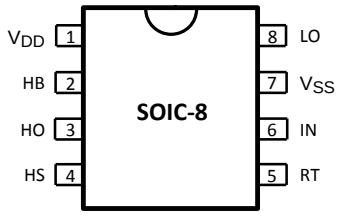
- 已添加 *ESD 额定值表，热性能信息表，特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1

Changes from Revision B (April 2013) to Revision C **Page**

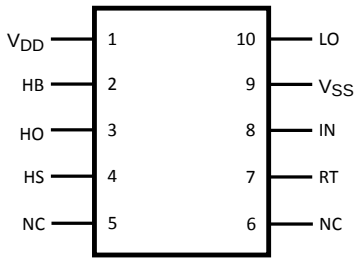
- 已更改 国家数据表的布局至 TI 格式 1

5 Pin Configuration and Functions

8-Pin SOIC
Package D
Top View



10-Pin WSON
Package DPR
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	D	DPR		
VDD	1	1	I	Positive supply voltage input.
HB	2	2	I	Positive connection for high-side bootstrap capacitor.
HO	3	3	O	High-side output to drive the top MOSFET.
HS	4	4	I	Switch node pin.
RT	5	7	I	Delay timer pin. The additional delay of the timer prevents lower and upper MOSFETs from conducting simultaneously, thereby preventing shoot-through. Timer delay is set with a resistor to ground.
IN	6	8	I	PWM control input for LO and HO outputs.
VSS	7	9	-	Ground pin.
LO	8	10	O	Low-side output to drive the bottom MOSFET.
N/C	-	5, 6	-	No connect.
Exposed Pad	-	Exposed Pad	-	The exposed die attach pad (DAP) on the 10-pin WSON package functions as a thermal connection and can be soldered to a copper plane under the device. The DAP nas no direct electrical connection to any of the pins. It can be left floating, but it is recommended to connect this to V_{SS}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
V_{DD} to V_{SS}	–0.3	18	V
V_{HB} to V_{HS}	–0.3	18	V
IN to V_{SS}	–0.3	V_{DD} + 0.3	V
LO Output	–0.3	V_{DD} + 0.3	V
HO Output	V_{HS} – 0.3	V_{HB} + 0.3	V
V_{HS} to V_{SS}	–1	100	V
V_{HB} to V_{SS}		118	V
RT to V_{SS}	–0.3	5	V
T_{stg} Storage Temperature Range	–55	150	°C
Maximum Junction Temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except 2, 3, and 4	±2000	V
			Pins 2, 3, and 4	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{DD}	9	14	V
HS	–1	100	V
HB	V_{HS} + 8	V_{HS} + 14	V
HS Slew Rate		50	V/ns
Junction Temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		SM74104		UNIT
		D	DPR	
		8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.5	37.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.1	38.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	55.6	14.9	
ψ_{JT}	Junction-to-top characterization parameter	9.7	0.4	
ψ_{JB}	Junction-to-board characterization parameter	54.9	15.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	4.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating junction temperature range, V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0 V, RT = 100 kΩ, no load on LO or HO, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	LI = HI = 0V		0.4	0.6	mA
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		1.9	3	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	0.2	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.3	3	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	V_{HS} = V_{HB} = 100V		0.05	10	µA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.08		mA
INPUT PINS						
V_{IL}	Low Level Input Voltage Threshold		0.8	1.8		V
V_{IH}	High Level Input Voltage Threshold			1.8	2.2	V
R_I	Input Pulldown Resistance		100	200	500	kΩ
TIME DELAY CONTROLS						
V_{RT}	Nominal Voltage at RT		2.7	3	3.3	V
I_{RT}	RT Pin Current Limit	RT = 0V	0.75	1.5	2.25	mA
T_{D1}	Delay Timer, RT = 10 kΩ		58	90	130	ns
T_{D2}	Delay Timer, RT = 100 kΩ		140	200	270	ns
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold		6.0	6.9	7.4	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		5.7	6.6	7.1	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.60	0.9	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.85	1.1	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		0.8	1.5	Ω
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA		0.25	0.4	V
V_{OHL}	High-Level Output Voltage	I_{LO} = –100 mA V_{OHL} = V_{DD} – V_{LO}		0.35	0.55	V
I_{OHL}	Peak Pullup Current	V_{LO} = 0V		1.6		A
I_{OLL}	Peak Pulldown Current	V_{LO} = 12V		1.8		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA		0.25	0.4	V
V_{OHH}	High-Level Output Voltage	I_{HO} = –100 mA, V_{OHH} = V_{HB} – V_{HO}		0.35	0.55	V
I_{OHH}	Peak Pullup Current	V_{HO} = 0V		1.6		A
I_{OLH}	Peak Pulldown Current	V_{HO} = 12V		1.8		A

6.6 Switching Characteristics

Over operating junction temperature range, $V_{DD} = V_{HB} = 12$ V, $V_{SS} = V_{HS} = 0$ V, no load on LO or HO, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LPHL}	Lower Turn-Off Propagation Delay (IN Rising to LO Falling)			25	56	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (IN Falling to HO Falling)			25	56	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		15		ns
t_R, t_F	Either Output Rise/Fall Time (3V to 9V)	C_L = 0.1 µF		0.6		µs
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 20 mA, I_R = 200 mA		50		ns

6.7 Typical Performance Characteristics

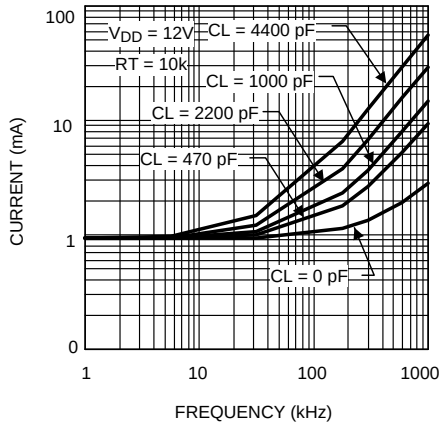


Figure 1. I_{DD} vs Frequency

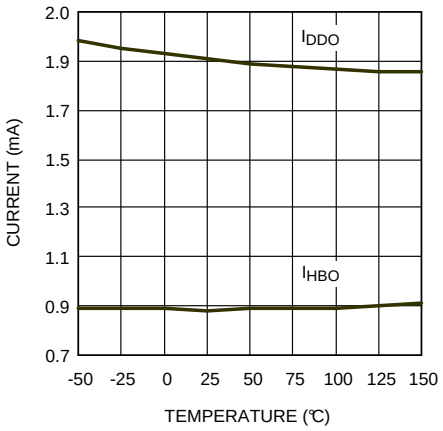


Figure 2. Operating Current vs Temperature

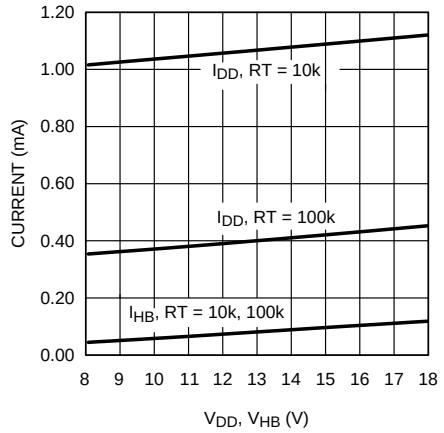


Figure 3. Quiescent Current vs Supply Voltage

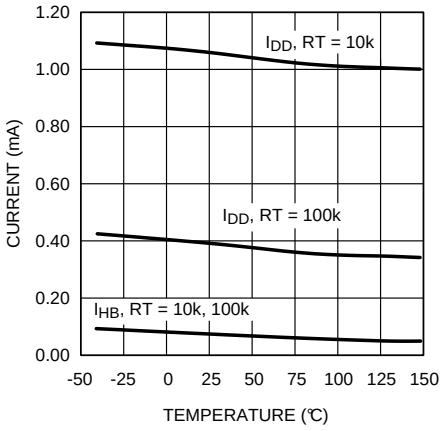


Figure 4. Quiescent Current vs Temperature

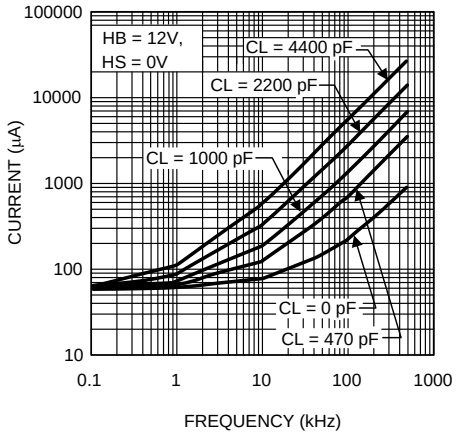


Figure 5. I_{HB} vs Frequency

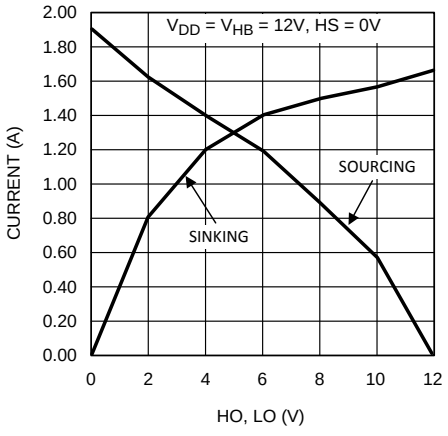


Figure 6. HO & LO Peak Output Current vs Output Voltage

Typical Performance Characteristics (continued)

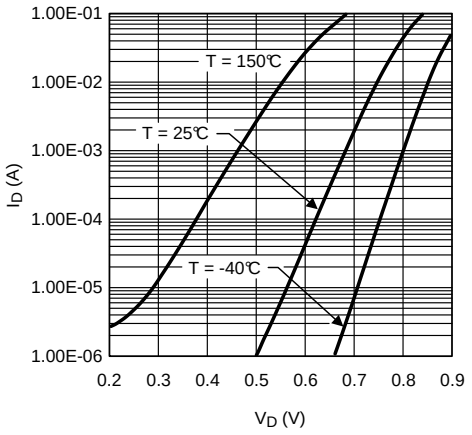


Figure 7. Diode Forward Voltage

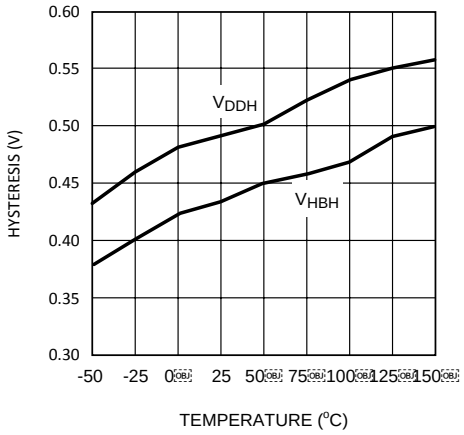


Figure 8. Undervoltage Threshold Hysteresis vs Temperature

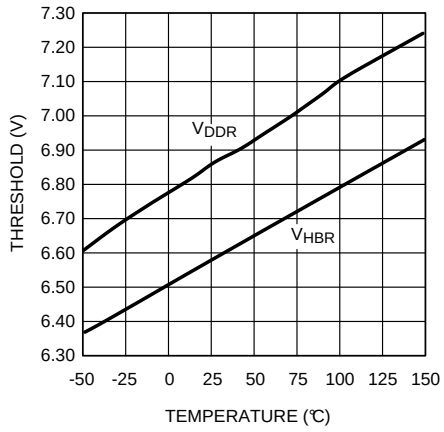


Figure 9. Undervoltage Rising Threshold vs Temperature

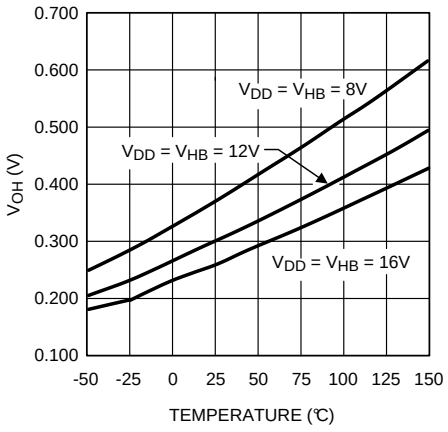


Figure 10. LO & HO Gate Drive—High Level Output Voltage vs Temperature

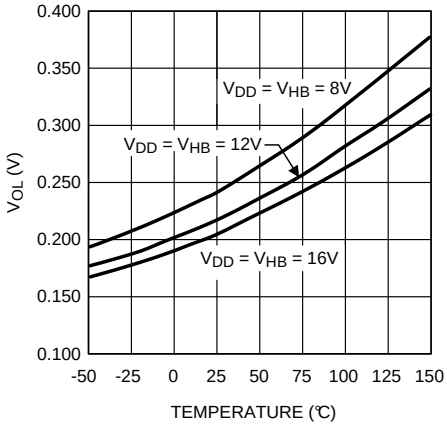


Figure 11. LO & HO Gate Drive—Low Level Output Voltage vs Temperature

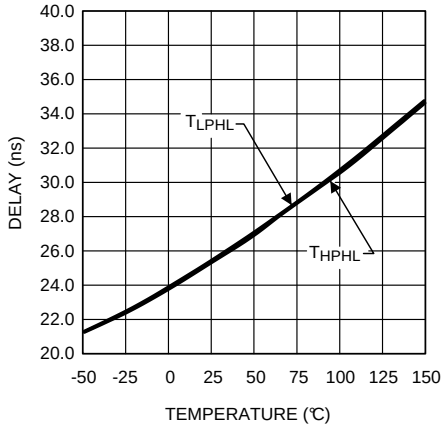


Figure 12. Turn Off Propagation Delay vs Temperature

Typical Performance Characteristics (continued)

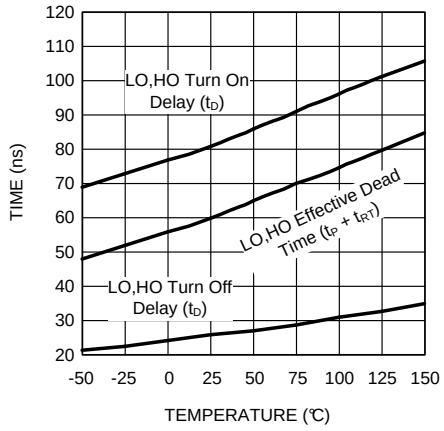


Figure 13. Timing vs Temperature RT = 10K

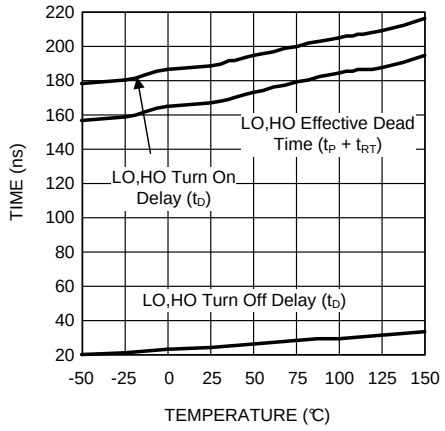


Figure 14. Timing vs Temperature RT = 100K

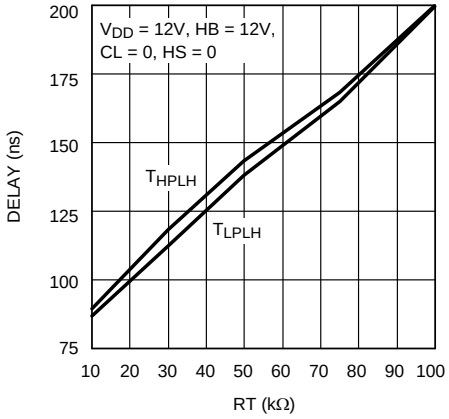


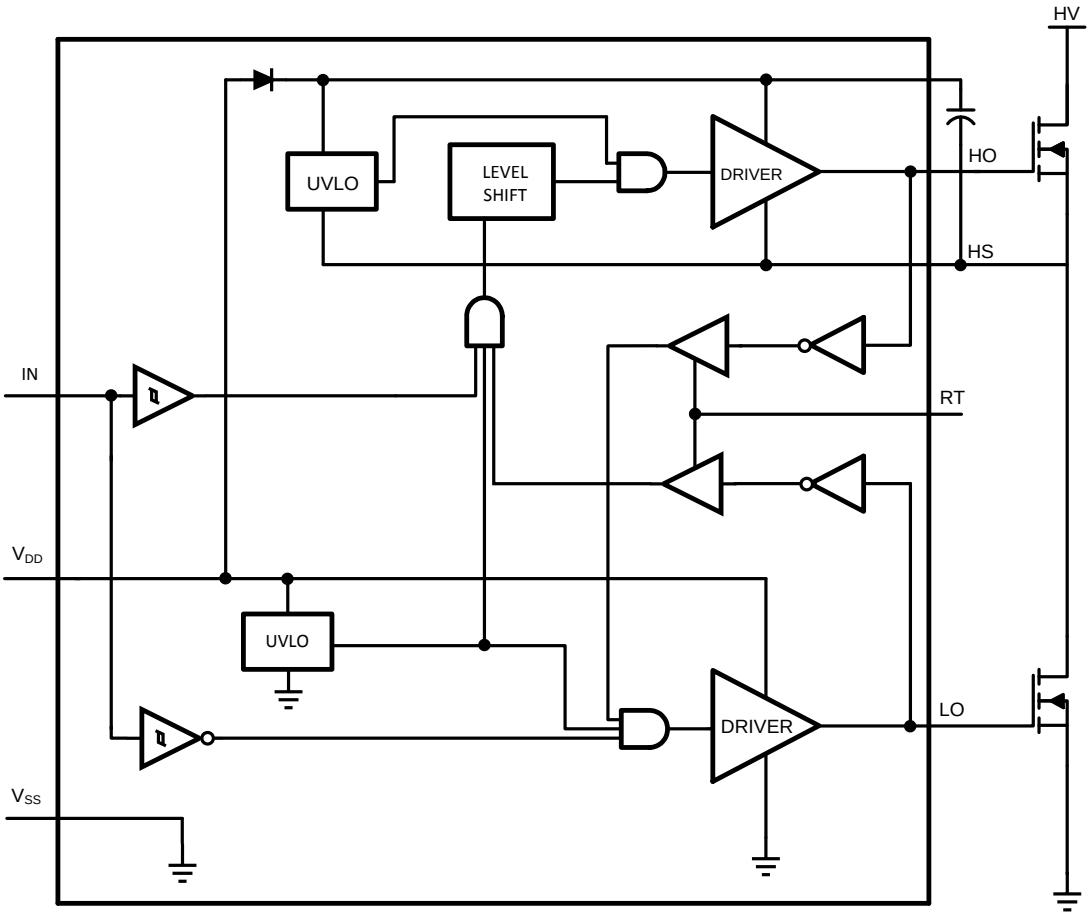
Figure 15. Turn On Delay vs RT Resistor Value

7 Detailed Description

7.1 Overview

SM74104 is a high voltage, high speed, dual output driver designed to drive top and bottom MOSFETs connected in synchronous buck or half-bridge configuration. SM74104 also features adaptive delay to prevent shoot-through current through top and bottom MOSFETs during switching transitions. The outputs that drive the top and bottom MOSFETs are controlled by one externally provided PWM signal.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Input Control

Referring to the timing diagram in Figure 16, the rising edge of the PWM input (IN) turns off the bottom MOSFET (LO) after a short propagation delay (t_P). An adaptive circuit in the SM74104 monitors the bottom gate voltage (LO) and triggers a programmable delay generator when the LO pin falls below an internally set threshold (≈ Vdd/2). The gate drive of the upper MOSFET (HO) is disabled until the deadtime expires. The upper gate is enabled after the TIMER delay (t_P+T_{RT}), and the upper MOSFET turns-on. The additional delay of the timer prevents lower and upper MOSFETs from conducting simultaneously, thereby preventing shoot-through.

Feature Description (continued)

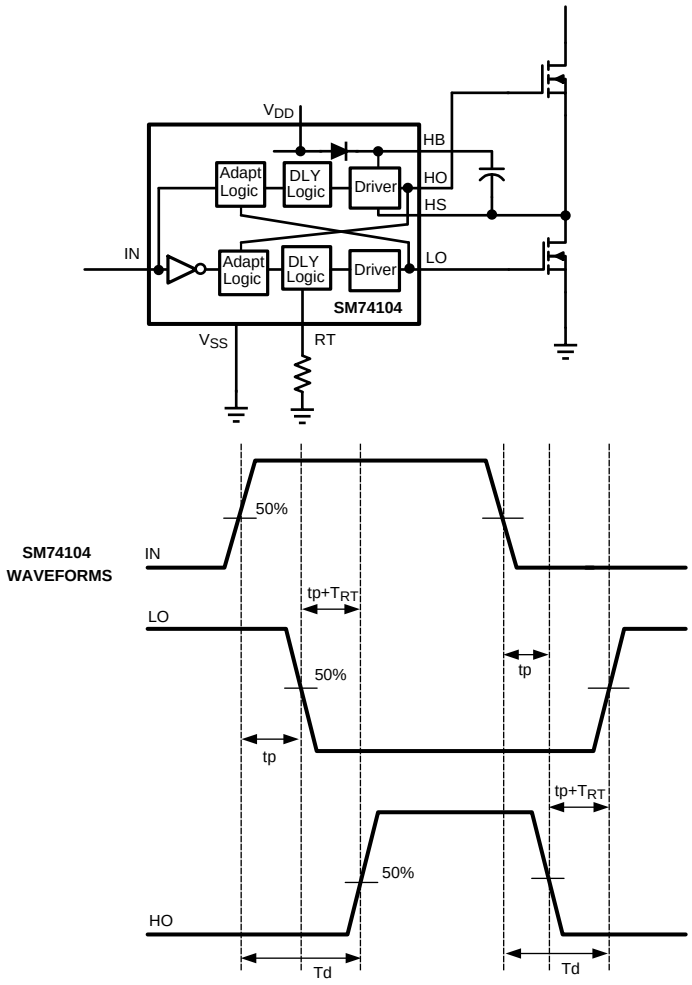


Figure 16. Application Timing Waveforms

A falling transition on the PWM signal (IN) initiates the turn-off of the upper MOSFET and turn-on of the lower MOSFET. A short propagation delay (t_P) is encountered before the upper gate voltage begins to fall. Again, the adaptive shoot-through circuitry and the programmable deadtime TIMER delays the lower gate turn-on time. The upper MOSFET gate voltage is monitored and the deadtime delay generator is triggered when the upper MOSFET gate voltage with respect to ground drops below an internally set threshold (≈ Vdd/2). The lower gate drive is momentarily disabled by the timer and turns on the lower MOSFET after the deadtime delay expires (t_P+T_{RT}).

7.3.2 Setting the Delay Timer with RT

The RT pin is biased at 3V and current limited to 1mA. It is designed to accommodate a resistor between 5K and 100K, resulting in an effective dead-time proportional to RT and ranging from 90ns to 200ns. RT values below 5K will saturate the timer and are not recommended.

7.4 Device Functional Modes

7.4.1 Startup and UVLO

Both top and bottom drivers include under-voltage lockout (UVLO) protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage ($V_{HB} – V_{HS}$) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn-on the external MOSFETs, and the built-in hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to V_{DD} pin of SM74104, the top and bottom gates are held low until V_{DD} exceeds UVLO threshold, typically about 6.9V. Any UVLO condition on the bootstrap capacitor will disable only the high side output (HO).

7.5 Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2 \quad (1)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

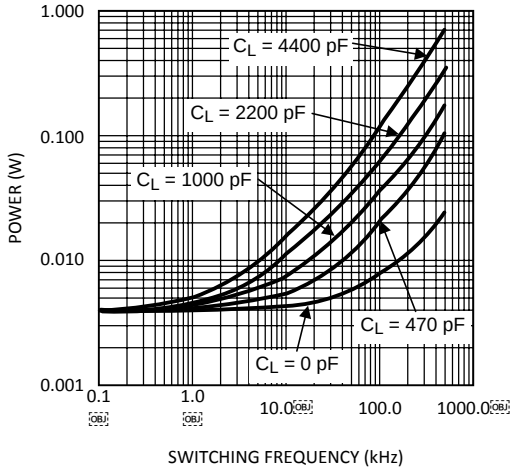


Figure 17. Gate Driver Power Dissipation (LO + HO)
V_{CC} = 12V, Neglecting Diode Losses

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

Power Dissipation Considerations (continued)

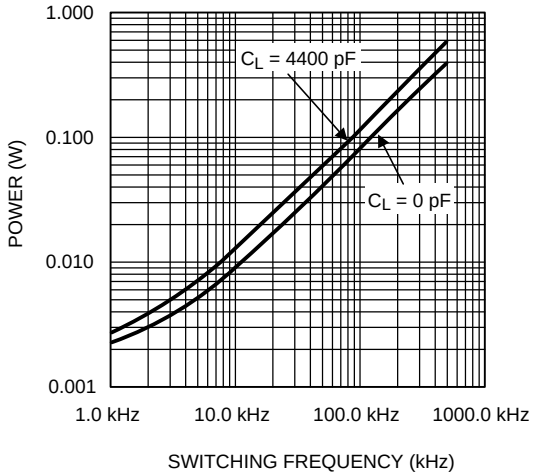


Figure 18. Diode Power Dissipation V_{IN} = 80V

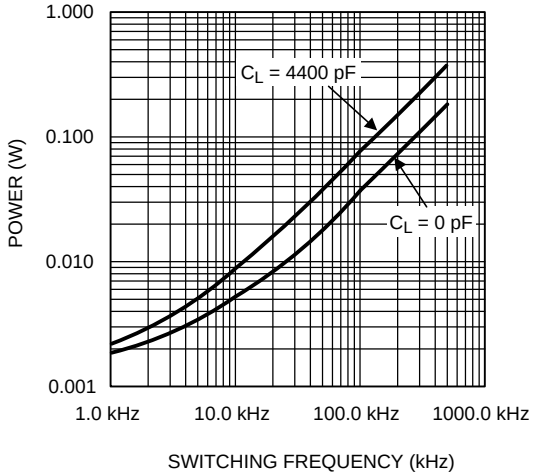


Figure 19. Diode Power Dissipation V_{IN} = 40V

The total IC power dissipation can be estimated from the above plots by summing the gate drive losses with the bootstrap diode losses for the intended application. Because the diode losses can be significant, an external diode placed in parallel with the internal bootstrap diode (refer to Figure 20) can be helpful in removing power from the IC. For this to be effective, the external diode must be placed close to the IC to minimize series inductance and have a significantly lower forward voltage drop than the internal diode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SM74104 can drive both a high-side and a low-side MOSFET using only one PWM input control signal. The internal level shifter provides a means for the control input to drive the high-side MOSFET. The SM74104 prevents shoot-through issues through adaptive transition timing and an additional time delay can be added by use of an external resistor at the RT pin.

8.2 Typical Application

The SM74104 is used to drive MOSFETs connected in a synchronous buck configuration as shown in Figure 20. A single control signal from an external PWM controller provides the control input to drive both the high-side and low-side MOSFET. The HO and LO outputs of the SM74104 can provide very fast switching of the MOSFETs, thereby reducing switching losses and improving the overall efficiency of the system.

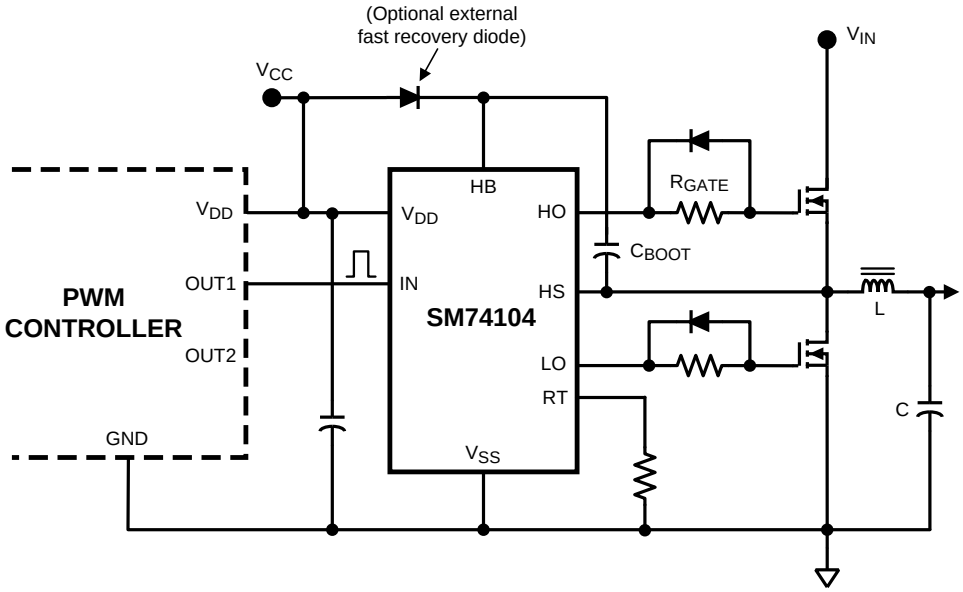


Figure 20. Typical Application

8.2.1 Design Requirements

The RT resistor should be sized such that the appropriate time delay is added between the switching transitions of the top and bottom MOSFETs. The exact RT value will depend on the selected MOSFETs, their switching speeds, and the desired delay time needed to prevent shoot-through. An optional external fast recovery diode should be placed between the VDD and HB pins to minimize the stress on the internal bootstrap diode and decrease the average power dissipation in the IC. An R_{GATE} resistor and a parallel diode may also be placed in the path of the MOSFET gates. The R_{GATE} resistor will decrease the ON switching speed of the MOSFET and can help damp possible oscillations on the line. The parallel diode will provide a current path around R_{GATE} during the OFF switching of the MOSFET, which can ensure fast shut off of the MOSFET to further prevent shoot-through.

Typical Application (continued)

8.2.2 Detailed Design Procedure

See Power Supply Recommendations, Layout, and Power Dissipation Considerations for key design considerations regarding the input supply, grounding, component placement, and power calculations specific to the SM74104.

8.2.3 Application Curve

An adaptive circuit in the SM74104 monitors the gate voltages of the top and bottom MOSFETs and triggers a programmable delay generator to prevent both MOSFETs from conducting simultaneously. The timer delay, T_{RT}, can be programmed with a resistor placed between RT and VSS. The value of T_{RT} will vary with the RT resistor value as shown in Figure 21.

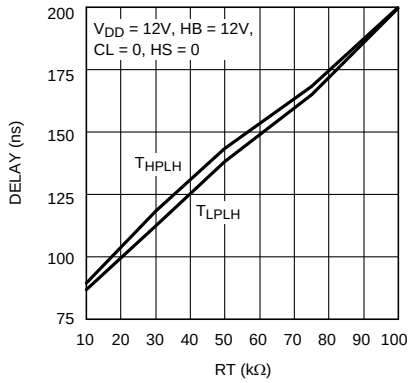


Figure 21. Turn On Delay vs RT Resistor Value

9 Power Supply Recommendations

A low ESR/ESL capacitor must be connected as close as possible to the IC between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from V_{DD} during turn-on of the external MOSFET. Also, to prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}). In both cases, the traces should be as short as possible to reduce the series resistance.

10 Layout

10.1 Layout Guidelines

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized.

1. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
2. Grounding considerations:
   - The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   - The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
3. The resistor on the RT pin must be placed very close to the IC and separated from high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

10.2 Layout Example

Figure 22 shows an example layout for the SM74104 in the 8-pin SOIC package option.

Layout Example (接下页)

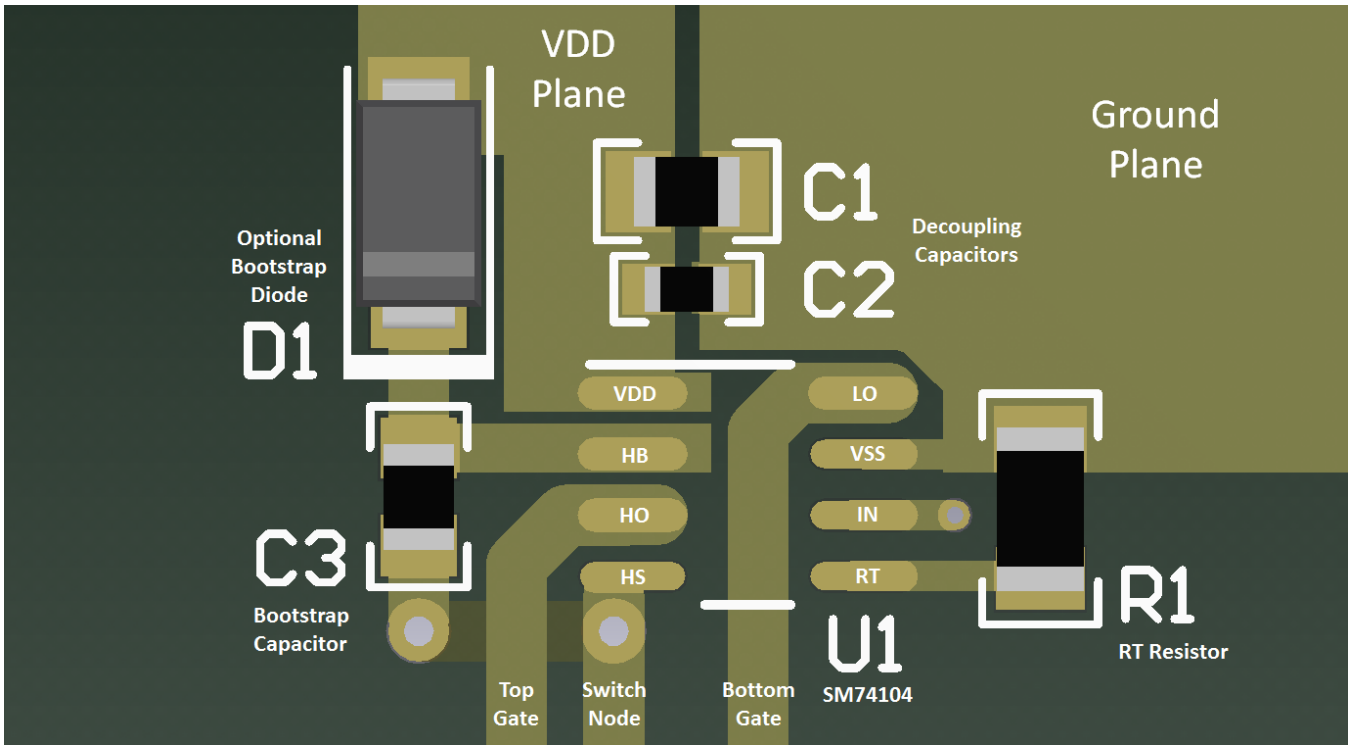


Figure 22. SM74104 Layout Example

11 器件和文档支持

11.1 商标

All trademarks are the property of their respective owners.

11.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SM74104MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	74104 MA	Samples
SM74104MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	74104 MA	Samples
SM74104SD/NOPB	ACTIVE	WSON	DPR	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	S74104	Samples
SM74104SDX/NOPB	ACTIVE	WSON	DPR	10	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	S74104	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

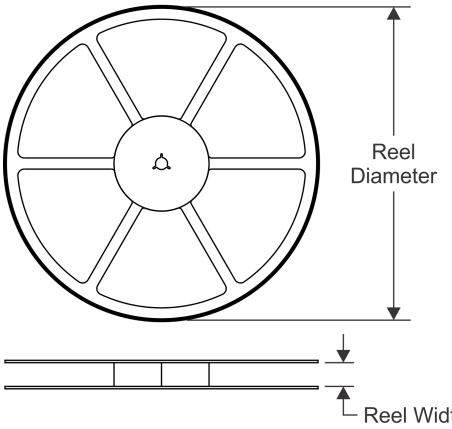
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

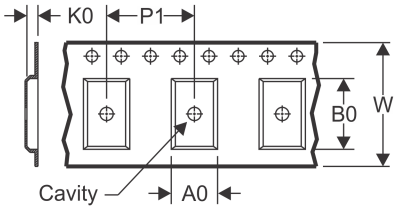
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

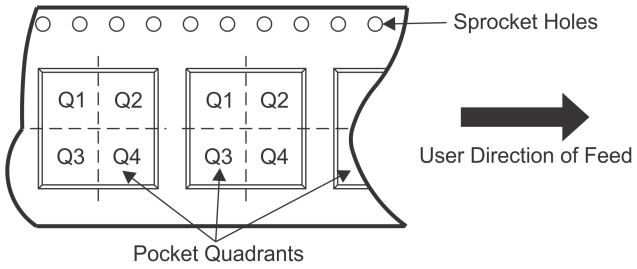


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

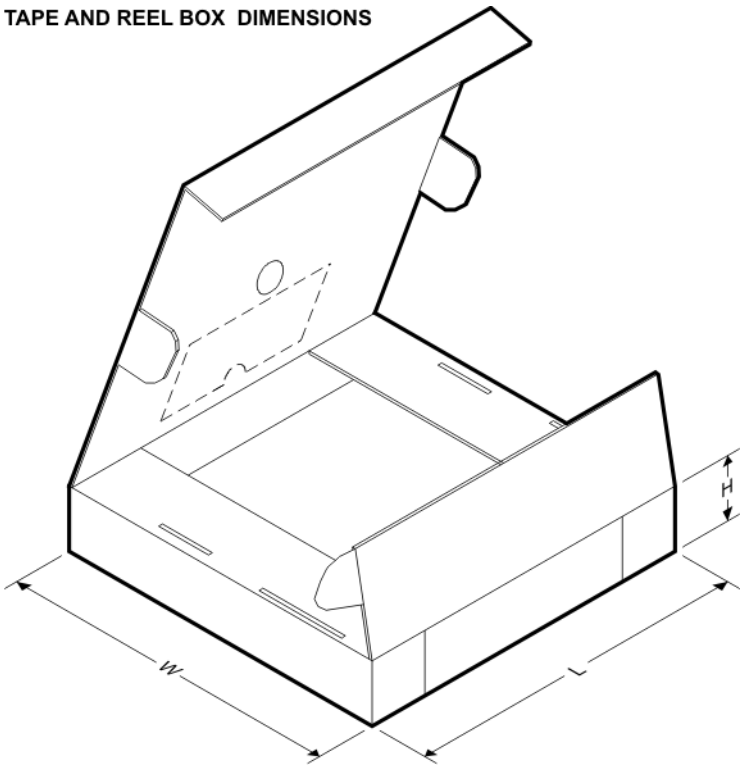
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM74104MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
SM74104SD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
SM74104SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

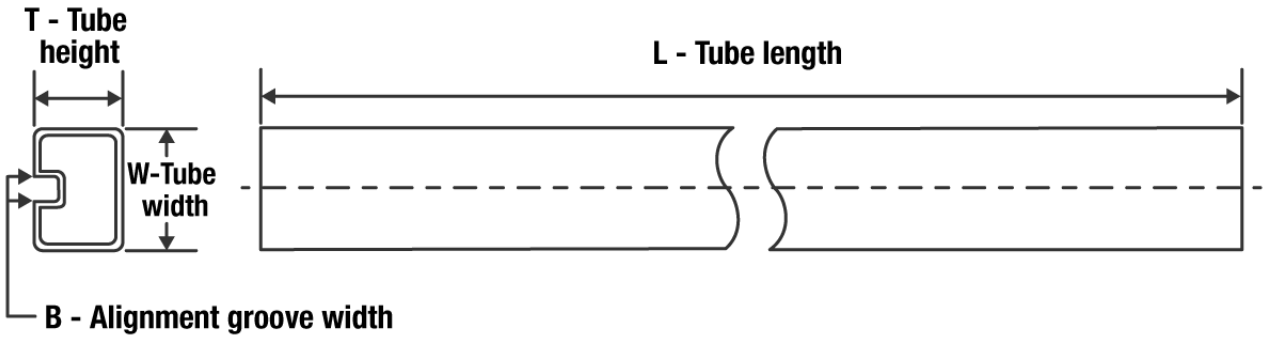
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM74104MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
SM74104SD/NOPB	WSON	DPR	10	1000	208.0	191.0	35.0
SM74104SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

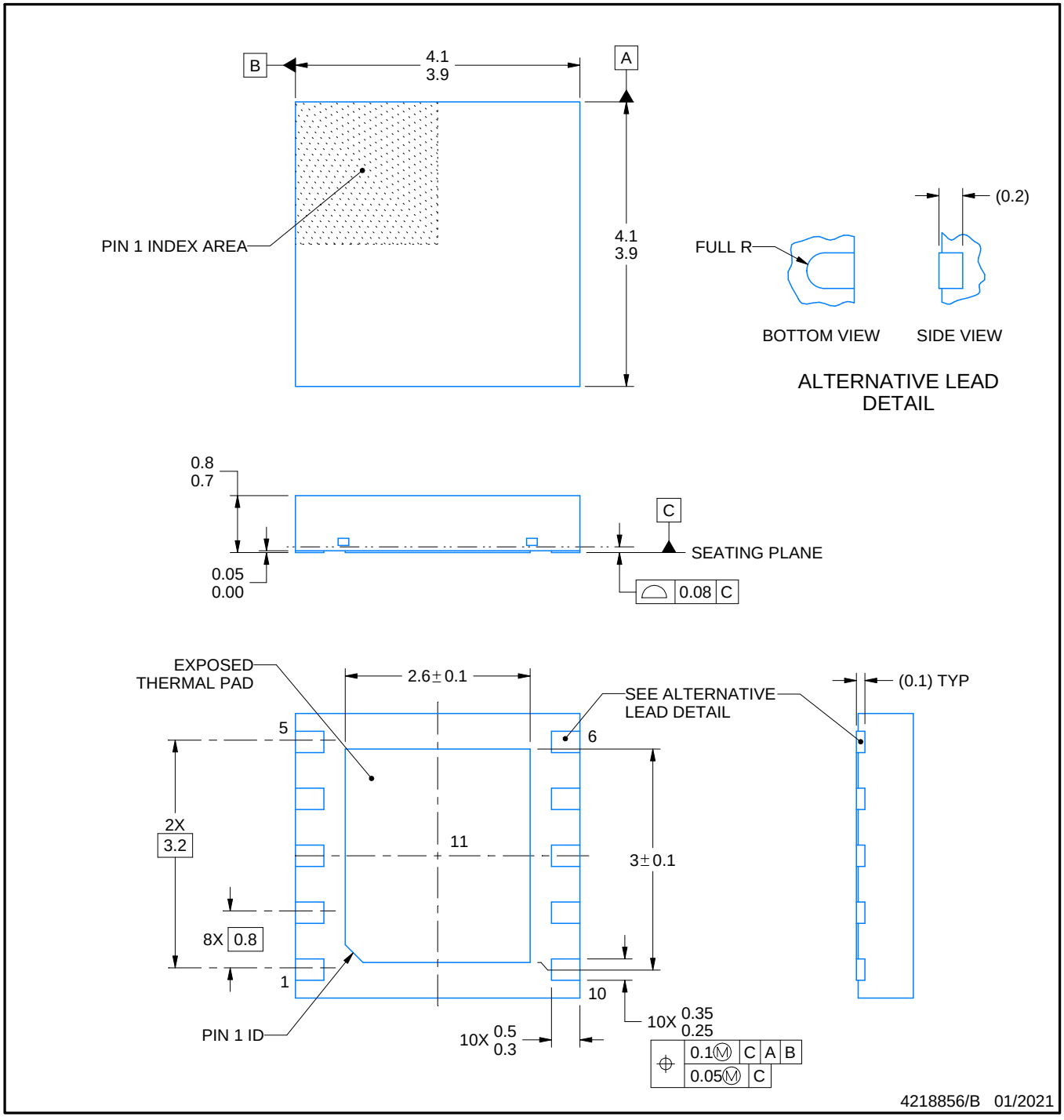
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SM74104MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DPR0010A

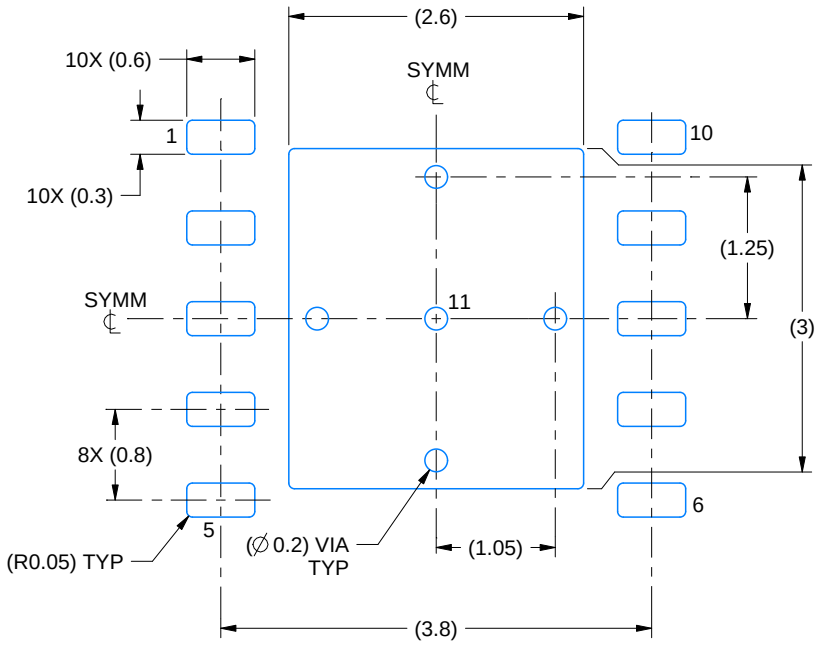
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

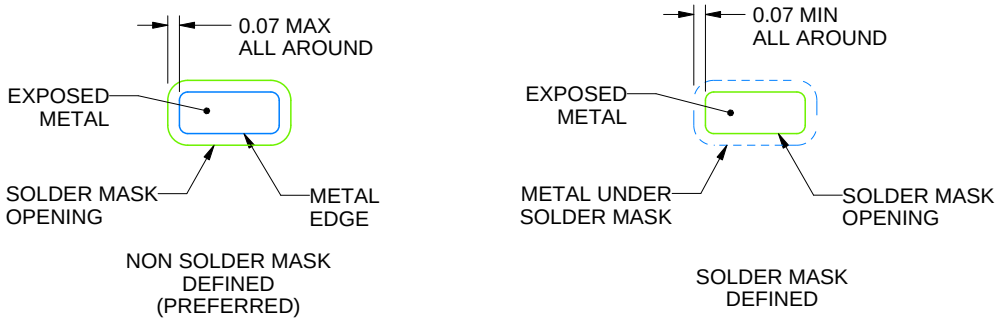


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

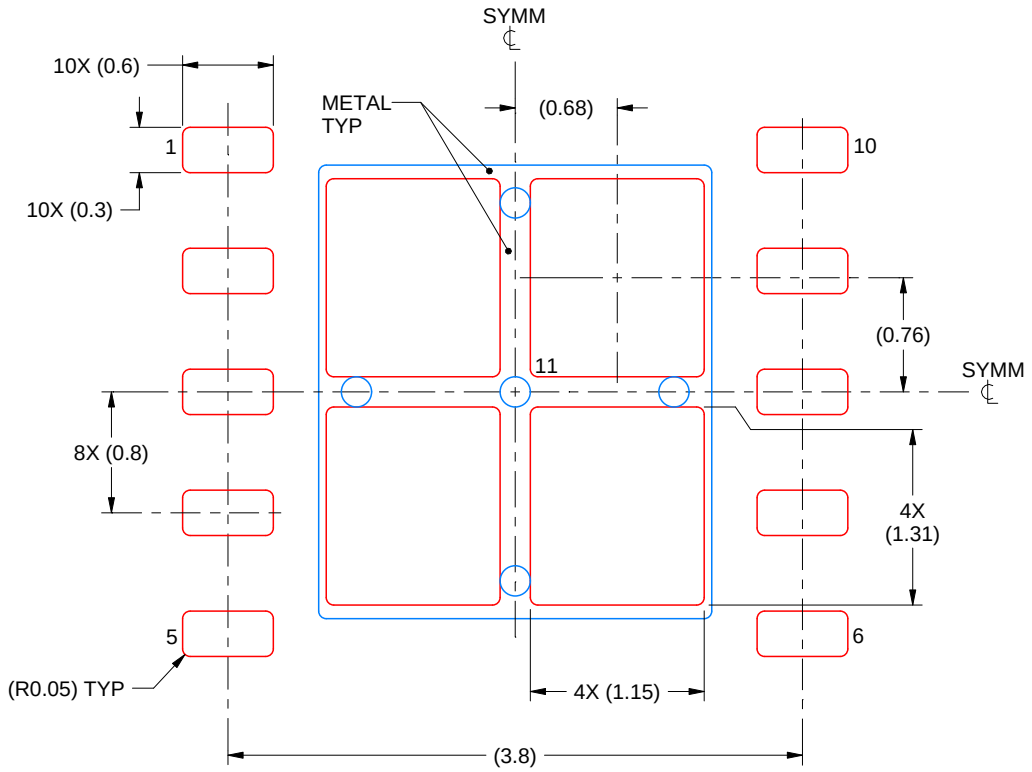


SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



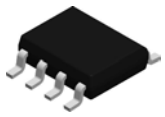
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218856/B 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

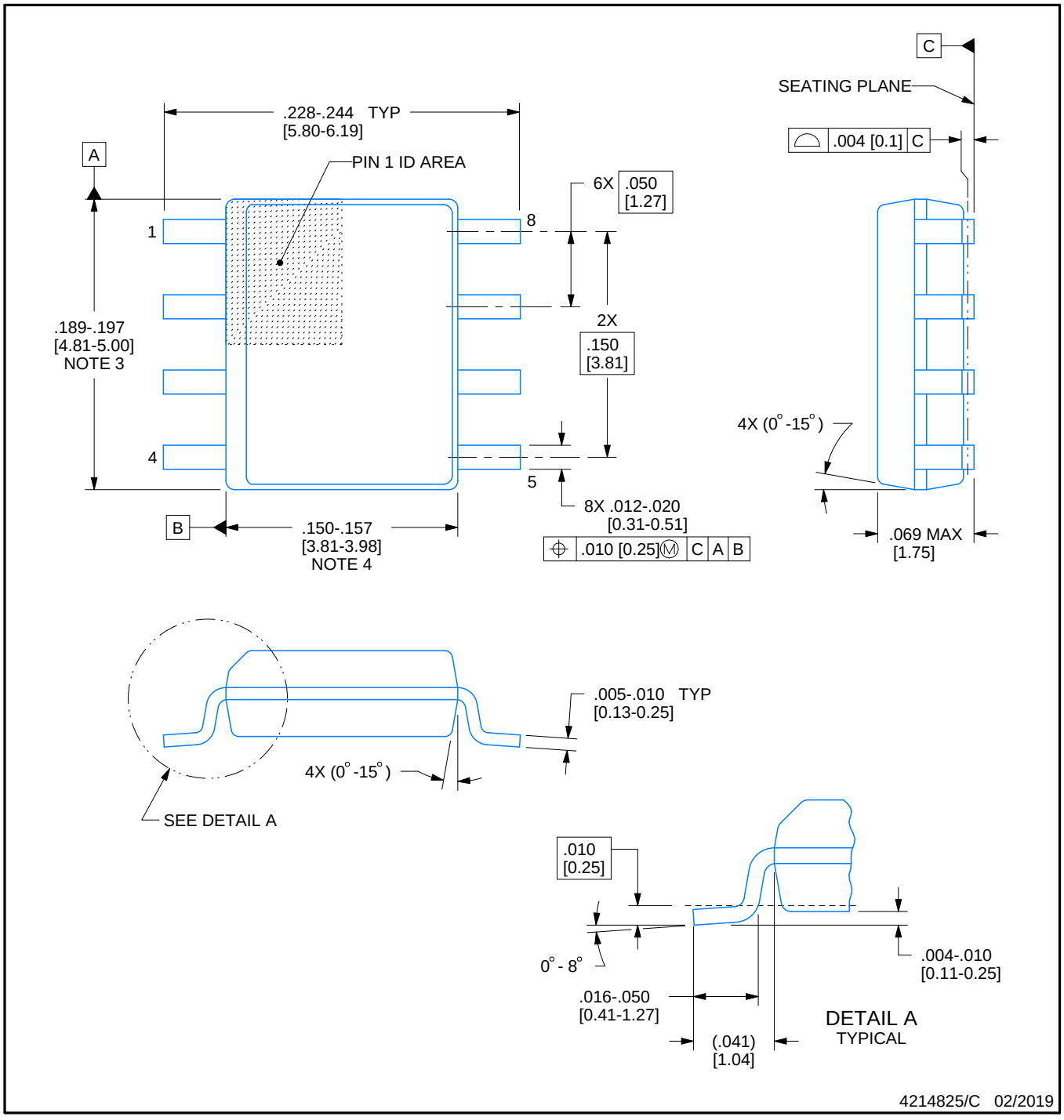


PACKAGE OUTLINE

D0008A

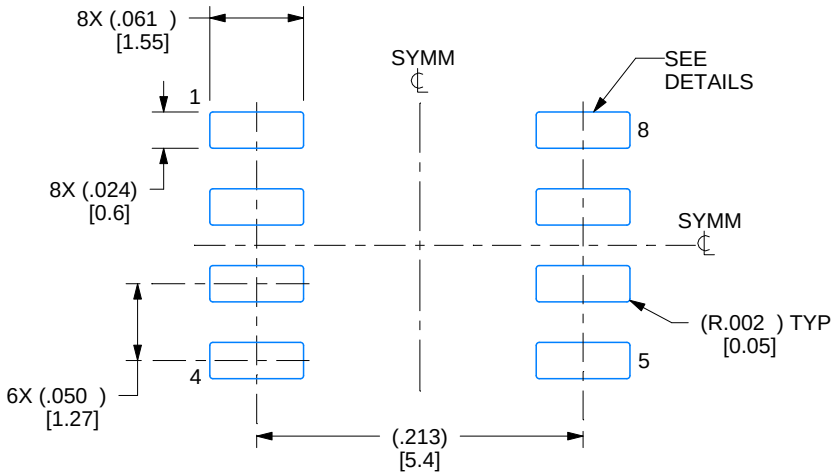
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

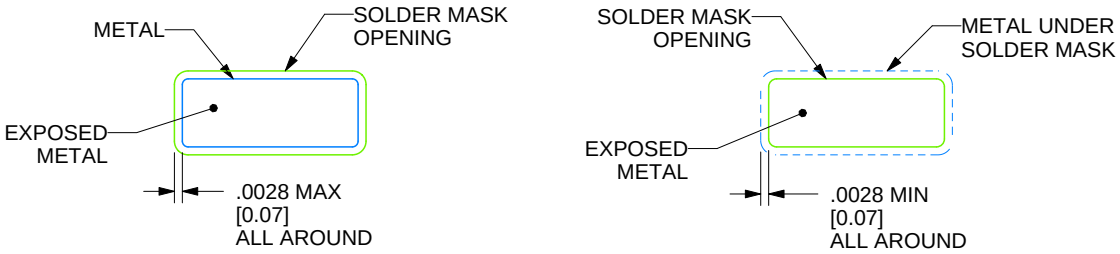


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

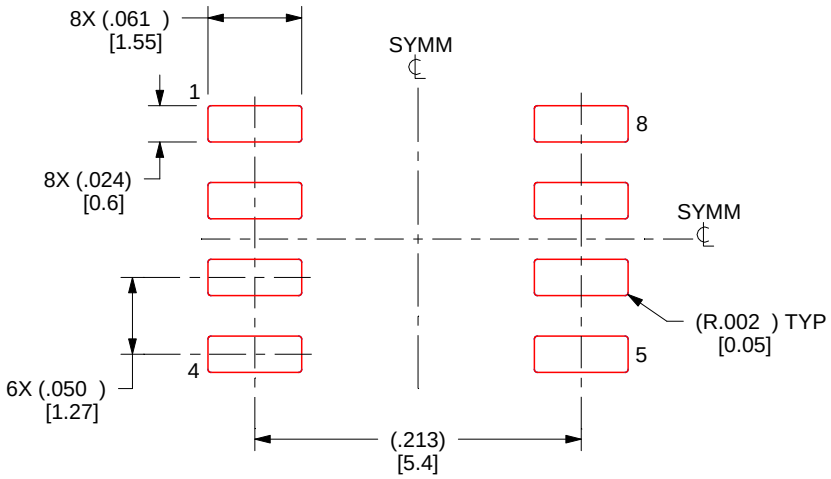
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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