TLV2186 精密、轨至轨输入和输出、24V、零漂移运算放大器

1 特性

- 高精度：
  - 温漂：0.1μV/°C
  - 低失调电压：10μV
- 低静态电流：90μA
- 出色的动态性能：
  - 增益带宽：750kHz
  - 压摆率：0.35V/μs
- 强大设计：
  - RFI/EMI 滤波输入
- 轨至轨输入/输出
- 电源电压范围：4.5V 至 24V

2 应用

- 精密高侧电流检测
- 桥式放大器
- 应变仪
- 温度测量
- 电阻式温度检测器
- 称重计
- 测热仪表
- 电源

3 说明

TLV2186 是一款低功耗、24V、轨至轨输入和输出的零漂移运算放大器。TLV2186 具有 仅 10μV 的典型失调电压和 0.1μV/°C 的典型失调电压温漂。该器件非常适合精密仪表、信号测量和有源滤波 应用。

TLV2186 具有低静态电流消耗 (90μA)，非常适合功率敏感型 应用，如电池供电和便携式系统。

此外，高共模架构以及低失调电压可实现正电源轨的高侧电流分流监控。该器件还在运输、装卸和组装期间提供强大的 ESD 保护。

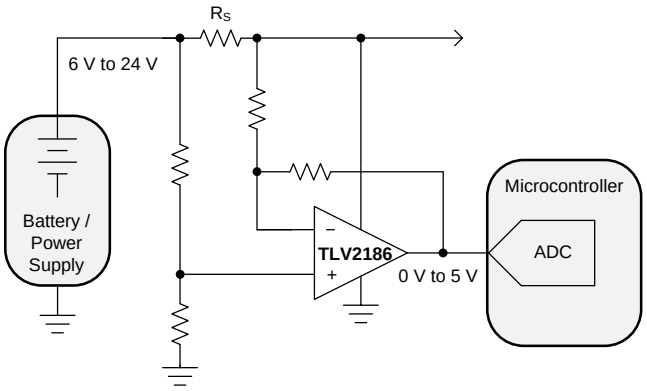
此器件的额定工作温度范围为 –40°C 至 +125°C。

器件信息(1)

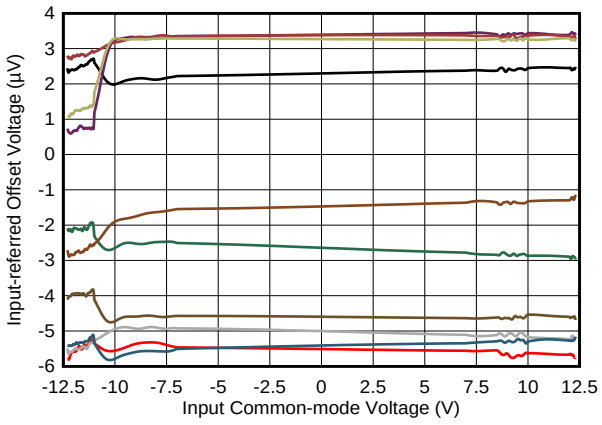
器件型号	封装	封装尺寸（标称值）
TLV2186	SOIC (8)	4.90mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

高侧电流分流监控器应用



V_{OS} 与输入共模电压



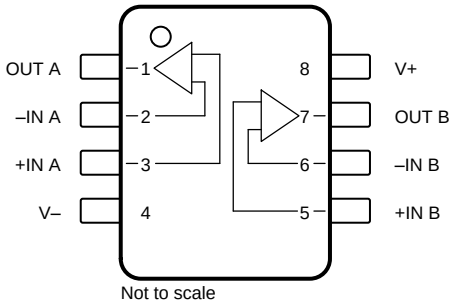
目录

4 修订历史记录

日期	修订版本	说明
2019 年 7 月	*	初始发行版

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V–	4	—	Negative supply
V+	8	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)			26	V
	Input voltage	Common-mode	(V–) –0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Output short-circuit(2)		Continuous		
T_J	Operating junction temperature		-40	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply Voltage	Single supply	4.5		24	V
		Dual supply	±2.25		±12	
T_A	Specified temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV2186 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	72.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±2.25V to ±12V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±10	±250	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.1	±1.0	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±0.05	±1	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				0.1	0.6	nA
		T_A = –40℃ to +85℃				0.6	
		T_A = –40℃ to +125℃				5	
I_{OS}	Input offset current				0.1	1.2	nA
		T_A = –40℃ to +85℃				1.2	
		T_A = –40℃ to +125℃				2	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			110		nV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			38		$nV/\sqrt{Hz}$
i_N	Input current noise	f = 1 kHz			100		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 < V_{CM} < (V+) + 0.1 V, T_A = –40℃ to +125℃	V_S = ±2.25 V	108	126		dB
			V_S = ±12 V	110	134		
		(V–) – 0.1 < V_{CM} < (V+) + 0.1 V, T_A = –40℃ to +125℃	V_S = ±2.25 V	106	114		
			V_S = ±12 V	106	120		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				750		kHz
SR	Slew rate	1-V step, G = 1			0.35		V/µs
t_S	Settling time	To 0.1%, 1-V step , G = 1			7.5		µs
	Overload recovery time	V_{IN} × gain > V_S			10		µs
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 5		MΩ || pF
Z_{ICM}	Common-mode				50 || 2.5		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±12 V	(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ	120	140		dB
			(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_L = 10 kΩ, T_A = –40°C to 125°C	120	134		
			(V–) + 0.65 V < V_O < (V+) – 0.65 V, R_L = 2 kΩ	120	140		
			(V–) + 0.65 V < V_O < (V+) – 0.65 V, R_L = 2 kΩ, T_A = –40°C to 125°C	120	134		
OUTPUT							
V_O	Voltage output swing from both rails	No load			5	20	mV
		R_L = 10 kΩ			60	100	
		R_L = 2 kΩ			340	500	
		R_L = 10 kΩ, T_A = –40℃ to +125℃			90	115	
I_{SC}	Short-circuit current				±20		mA
C_{LOAD}	Capacitive load drive			See typical curves			
R_O	Open-loop output impedance			See typical curves			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = ±2.25 to ±12 V			90	130	µA
			T_A = –40°C to 125°C			150	

6.6 Typical Characteristics

表 1. Typical Characteristic Graphs

DESCRIPTION	FIGURE
Offset Voltage Distribution	图 1
Offset Voltage Drift (-40°C to +125C°C)	图 2
Input Bias Current Distribution	图 3
Input Offset Current Distribution	图 4
Offset Voltage vs Common-Mode Voltage	图 5
Offset Voltage vs Supply Voltage	图 6
Open-Loop Gain and Phase vs Frequency	图 7
Closed-Loop Gain vs Frequency	图 8
Input Bias Current and Offset Current vs Temperature	图 9
Output Voltage Swing vs Output Current (Sourcing)	图 10
Output Voltage Swing vs Output Current (Sinking)	图 11
CMRR and PSRR vs Frequency	图 12
CMRR vs Temperature	图 13
PSRR vs Temperature	图 14
0.1-Hz to 10-Hz Voltage Noise	图 15
Input Voltage Noise Spectral Density vs Frequency	图 16
THD+N vs Frequency	图 17
THD+N vs Output Amplitude	图 18
Quiescent Current vs Supply Voltage	图 19
Quiescent Current vs Temperature	图 20
Open-Loop Gain vs Temperature (10 kΩ)	图 21
Open-Loop Gain vs Temperature (2 kΩ)	图 22
Open-Loop Output Impedance vs Frequency	图 23
Small-Signal Overshoot vs Capacitive Load (Gain = –1, 10-mV step)	图 24
Small-Signal Overshoot vs Capacitive Load (Gain = 1, 10-mV step)	图 25
No Phase Reversal	图 26
Positive Overload Recovery	图 27
Negative Overload Recovery	图 28
Small-Signal Step Response (Gain = 1, 10-mV step)	图 29
Small-Signal Step Response (Gain = –1, 10-mV step)	图 30
Large-Signal Step Response (Gain = 1, 10-V step)	图 31
Large-Signal Step Response (Gain = –1, 10-V step)	图 32
Phase Margin vs Capacitive Load	图 33
Settling Time (1-V Step, 0.1% Settling)	图 34
Short Circuit Current vs Temperature	图 35
Maximum Output Voltage vs Frequency	图 36
EMIRR vs Frequency	图 37
Channel Separation	图 38

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

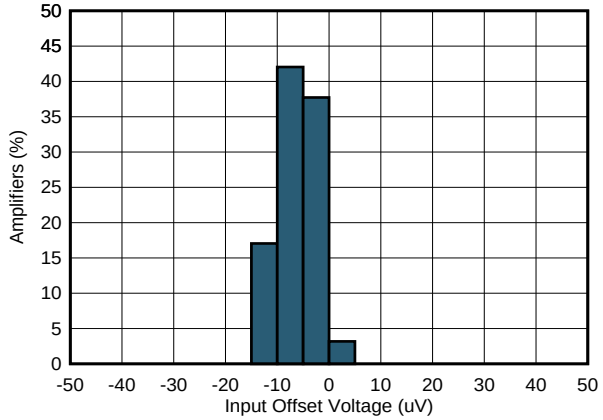


图 1. Offset Voltage Distribution

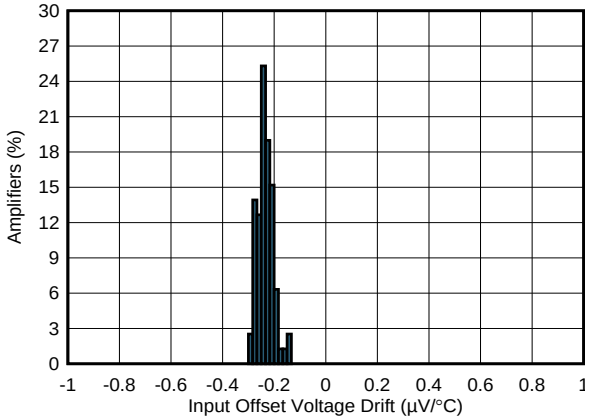


图 2. Offset Voltage Drift (-40°C to 125C°C)

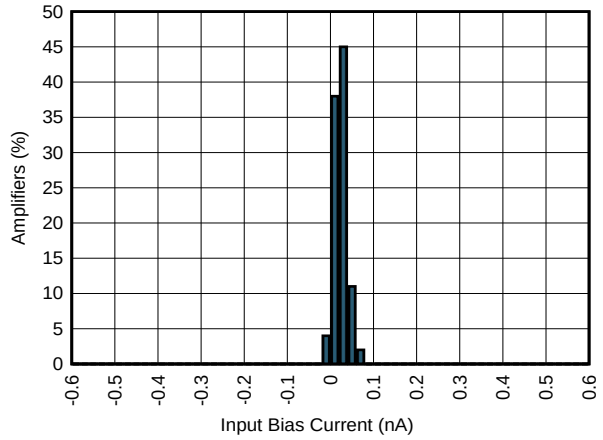


图 3. Input Bias Current Distribution

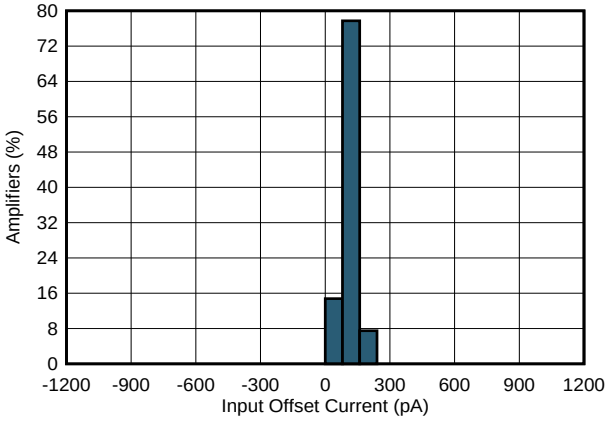


图 4. Input Offset Current Distribution

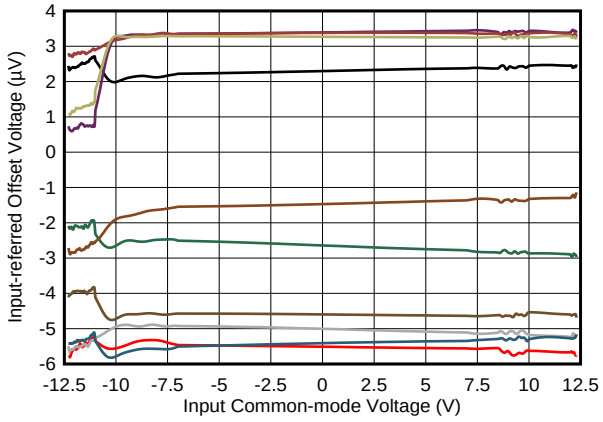


图 5. Offset Voltage vs Common-Mode Voltage

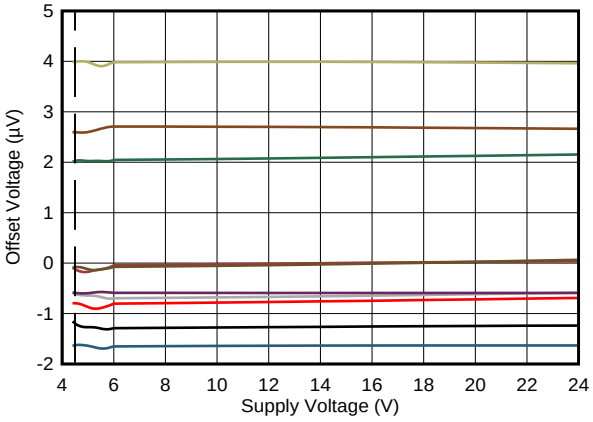


图 6. Offset Voltage vs Supply Voltage

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

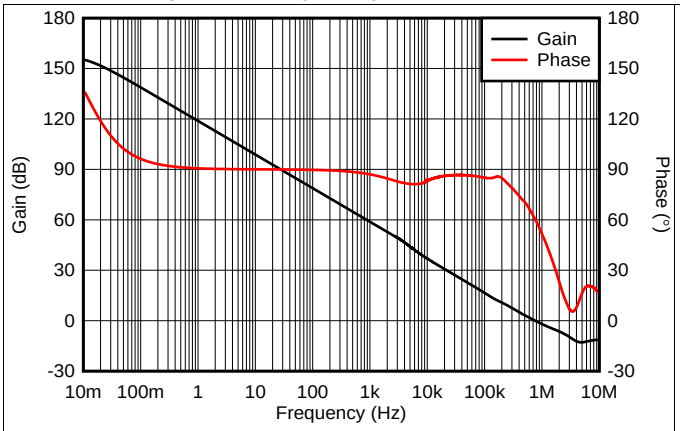


图 7. Open-Loop Gain and Phase vs Frequency

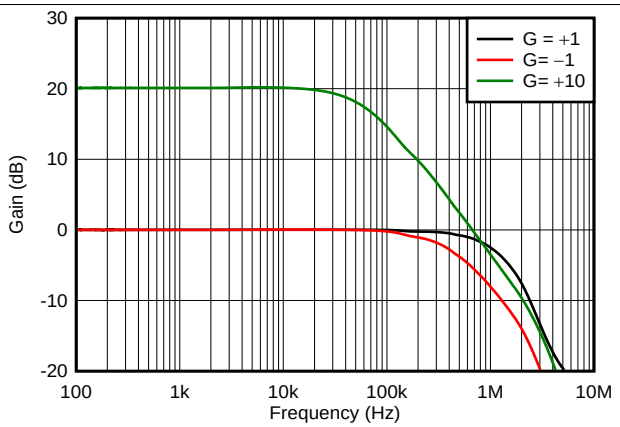


图 8. Closed-Loop Gain vs Frequency

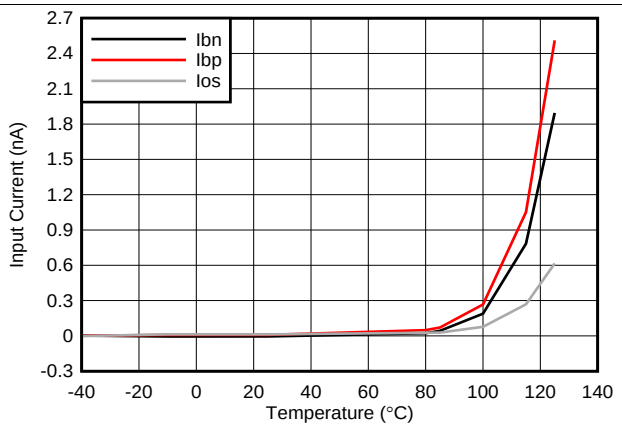


图 9. Input Bias Current and Offset Current vs Temperature

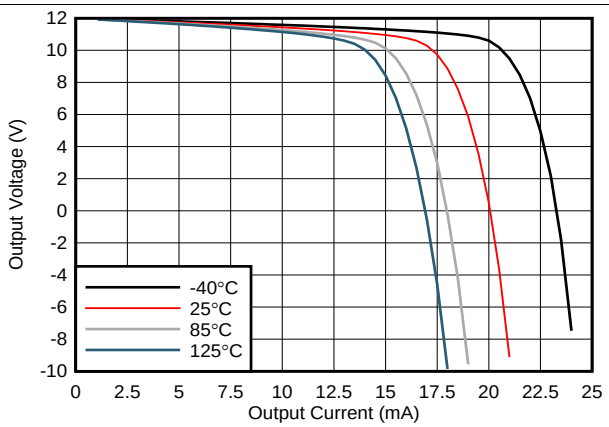


图 10. Output Voltage Swing vs Output Current (Sourcing)

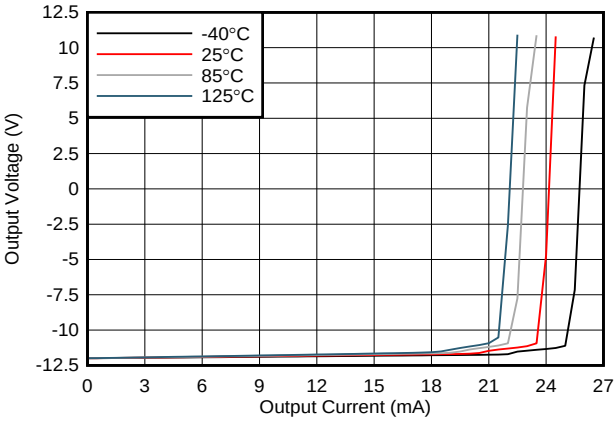


图 11. Output Voltage Swing vs Output Current (Sinking)

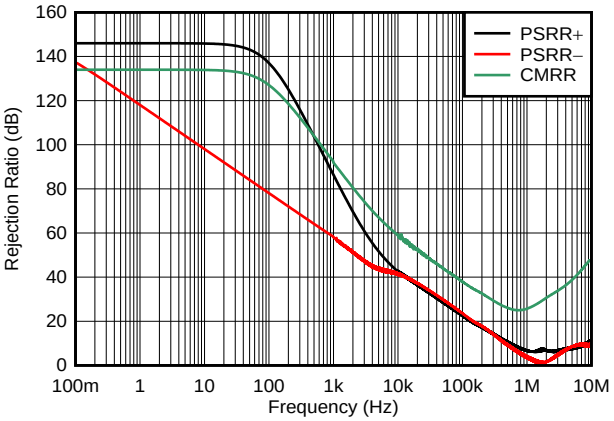


图 12. CMRR and PSRR vs Frequency

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

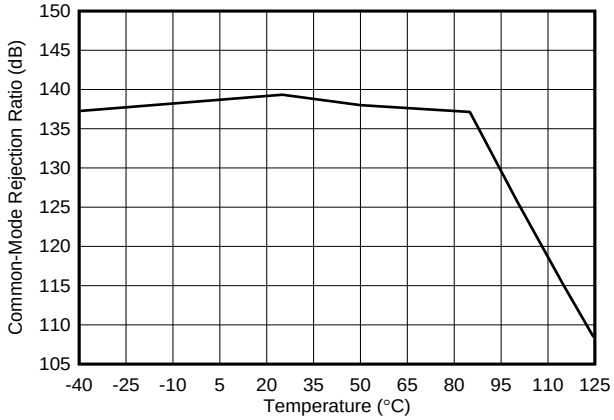


图 13. CMRR vs Temperature

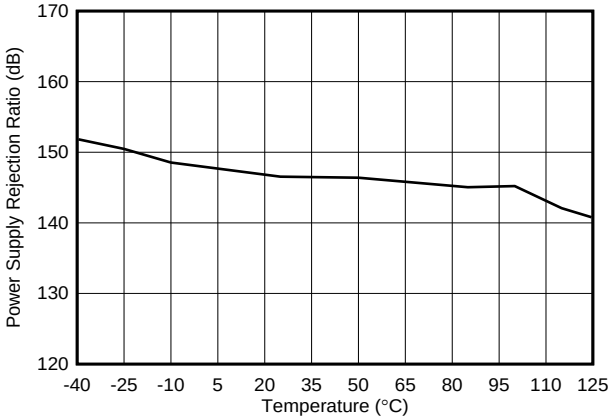


图 14. PSRR vs Temperature

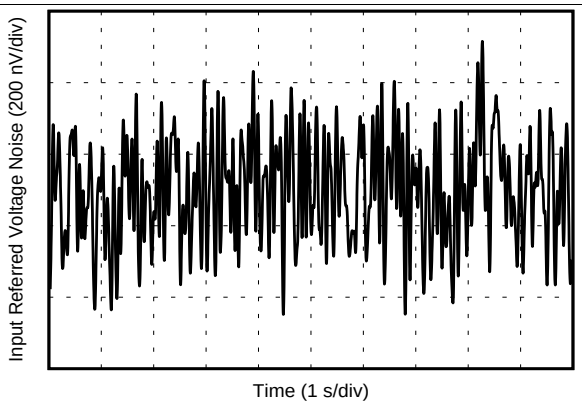


图 15. 0.1-Hz to 10-Hz Voltage Noise

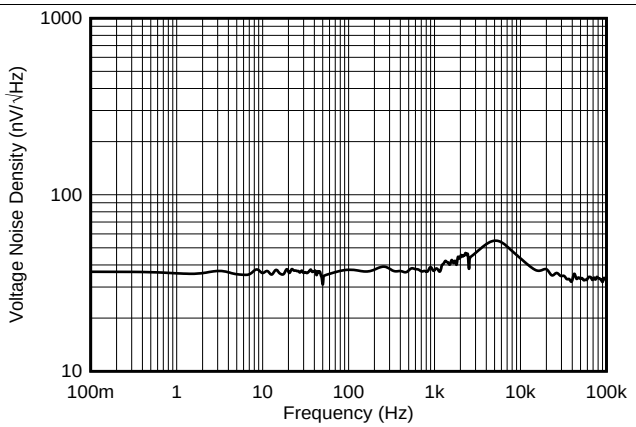


图 16. Input Voltage Noise Spectral Density vs Frequency

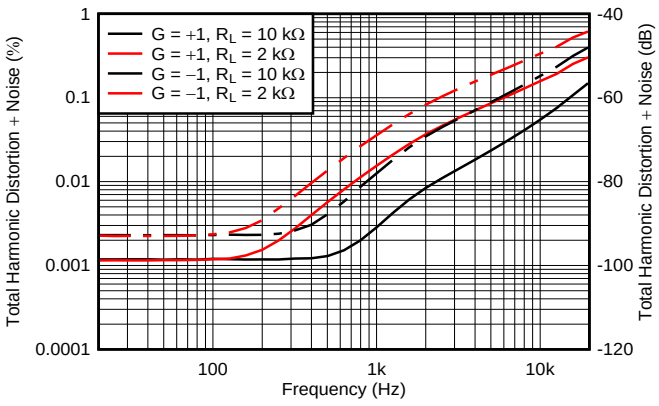


图 17. THD+N vs Frequency

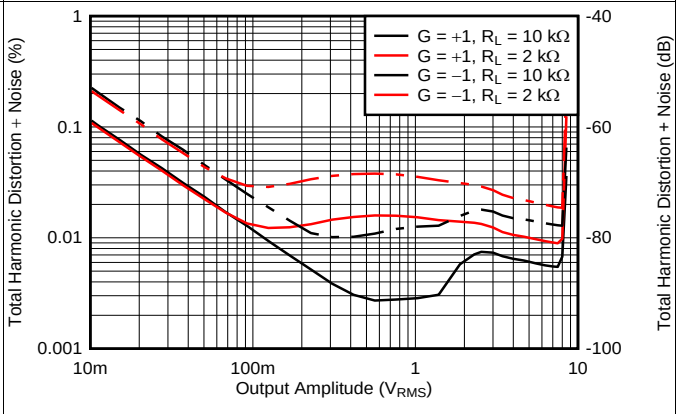


图 18. THD+N vs Output Amplitude

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

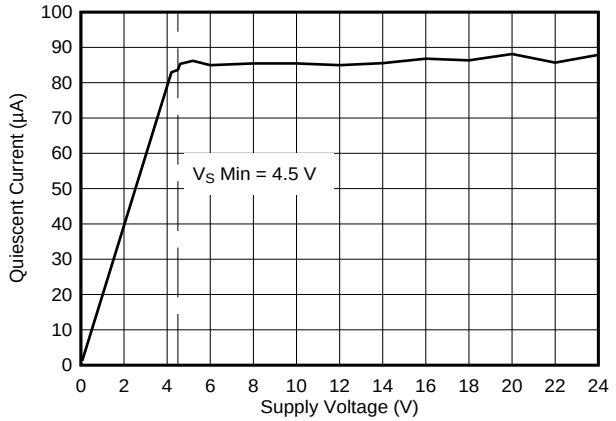


图 19. Quiescent Current vs Supply Voltage

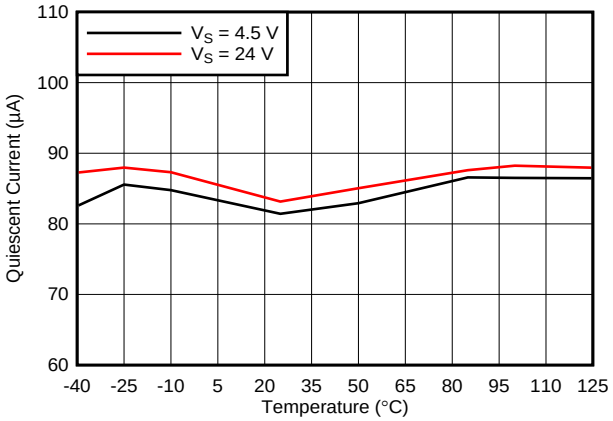


图 20. Quiescent Current vs Temperature

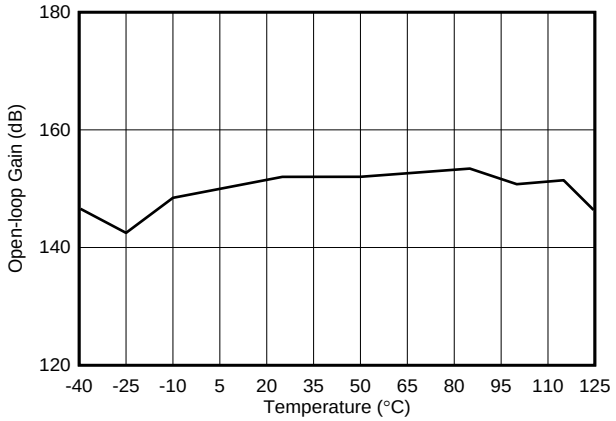
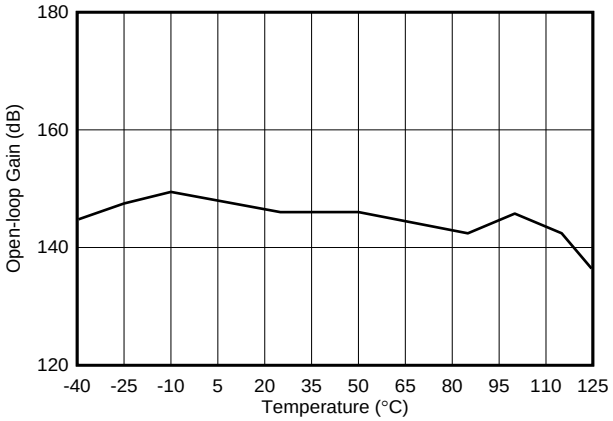


图 21. Open-Loop Gain vs Temperature



R_L = 2 kΩ

图 22. Open-Loop Gain vs Temperature

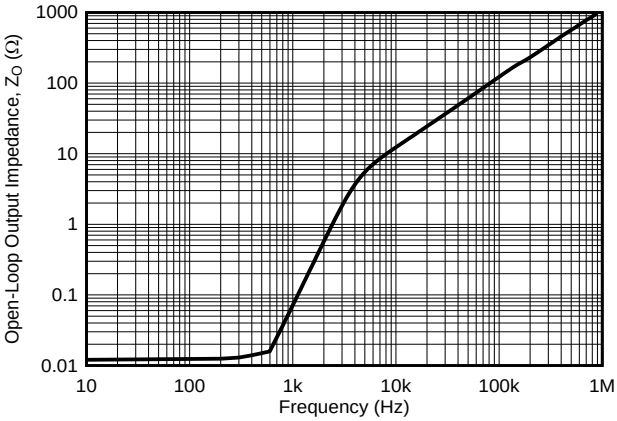
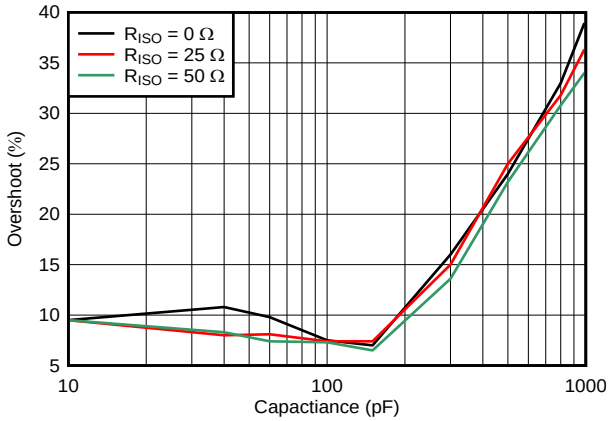


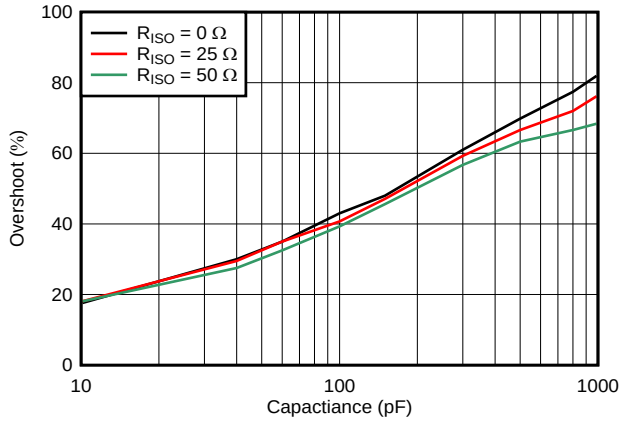
图 23. Open-Loop Output Impedance vs Frequency



Gain = –1, 10-mV step

图 24. Small-Signal Overshoot vs Capacitive Load

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)



Gain = 1, 10-mV step

图 25. Small-Signal Overshoot vs Capacitive Load

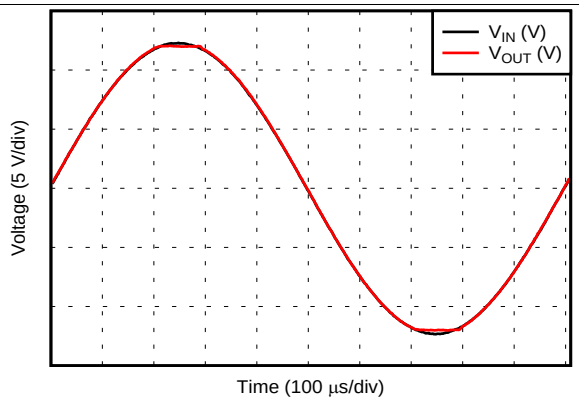


图 26. No Phase Reversal

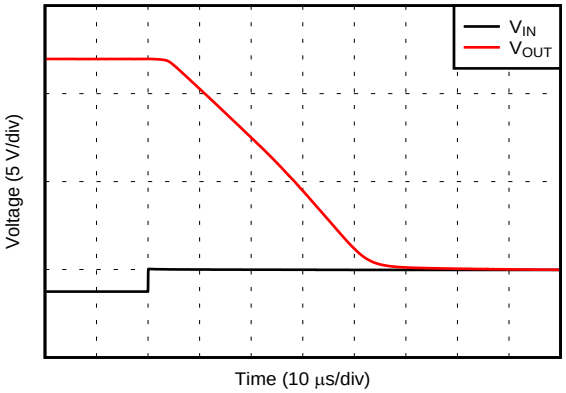


图 27. Positive Overload Recovery

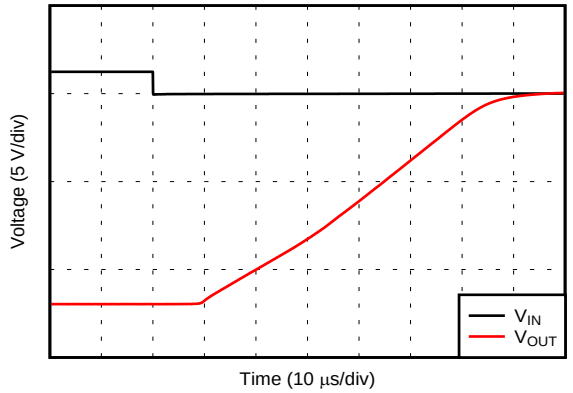
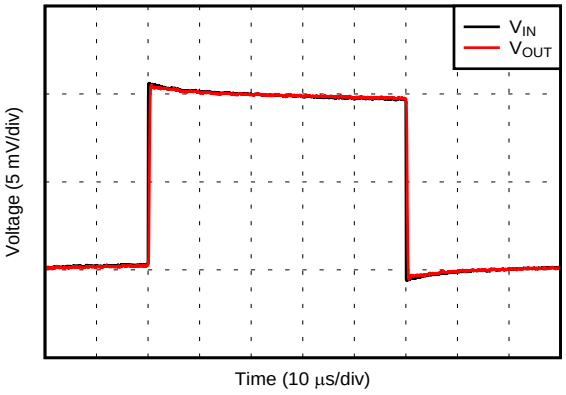
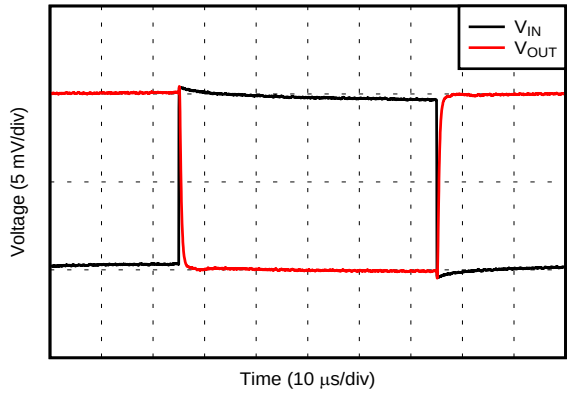


图 28. Negative Overload Recovery



Gain = 1, 10-mV step

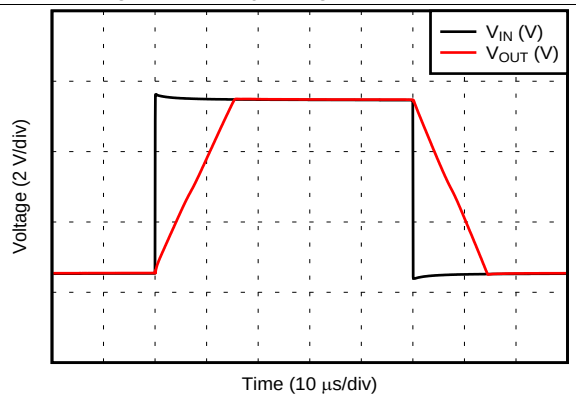
图 29. Small-Signal Step Response



Gain = –1, 10-mV step

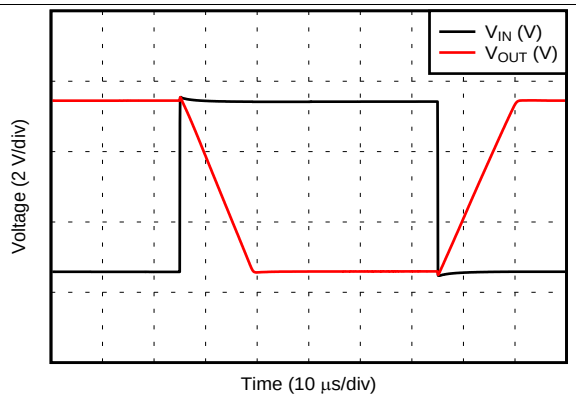
图 30. Small-Signal Step Response

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)



Gain = 1, 10-V step

图 31. Large-Signal Step Response



Gain = –1, 10-V step

图 32. Large-Signal Step Response

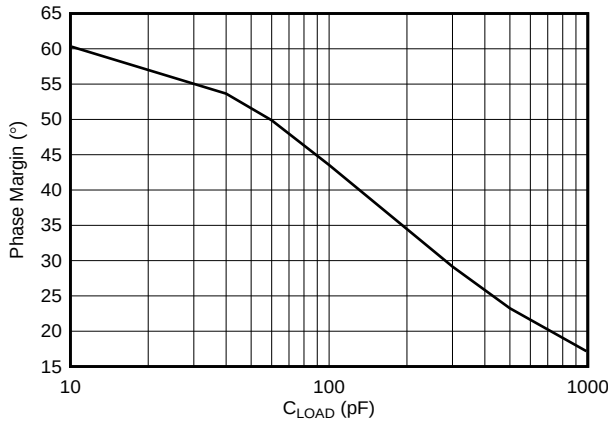
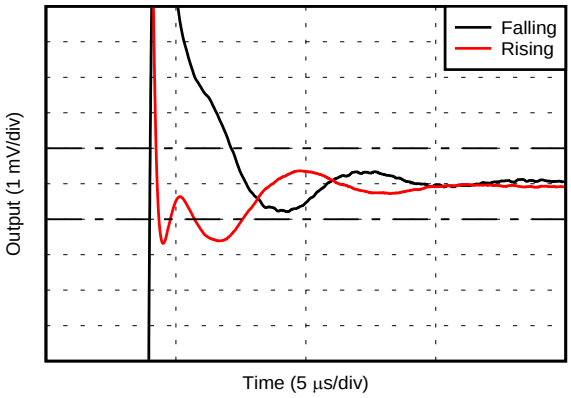


图 33. Phase Margin vs Capacitive Load



1-V step, 0.1% settling

图 34. Settling Time

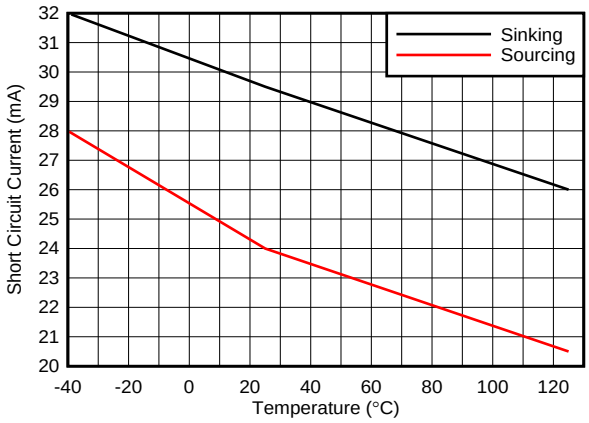


图 35. Short Circuit Current vs Temperature

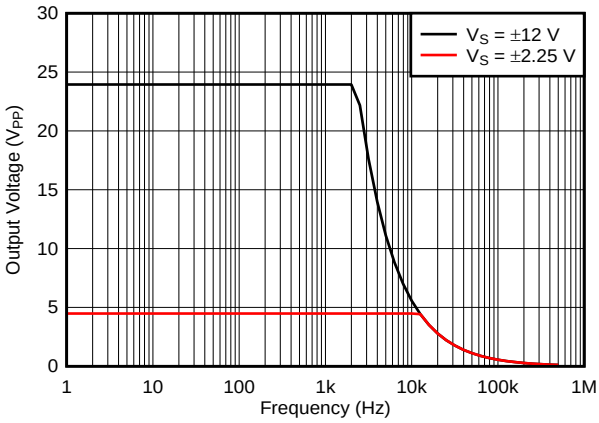


图 36. Maximum Output Voltage vs Frequency

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

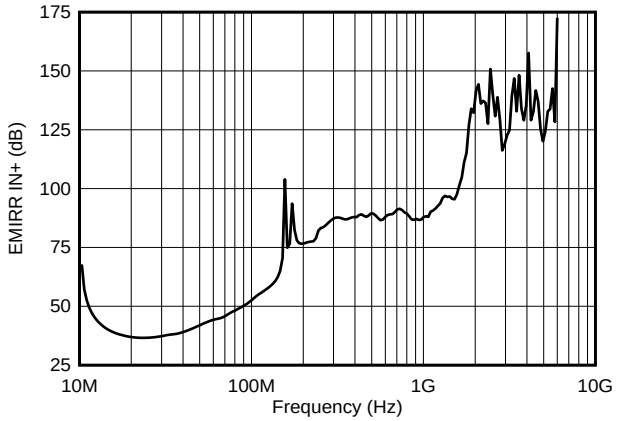


图 37. EMIRR vs Frequency

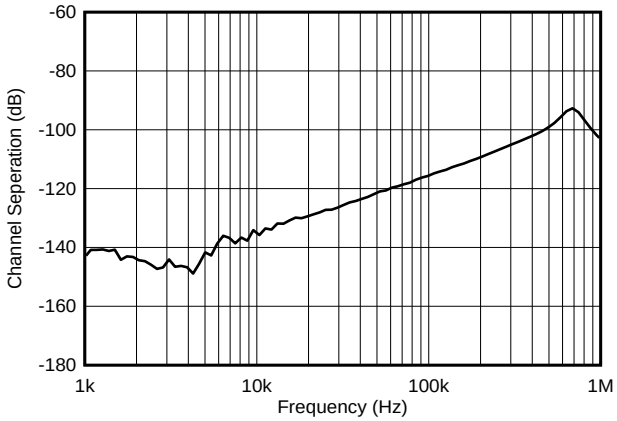


图 38. Channel Separation

7 Detailed Description

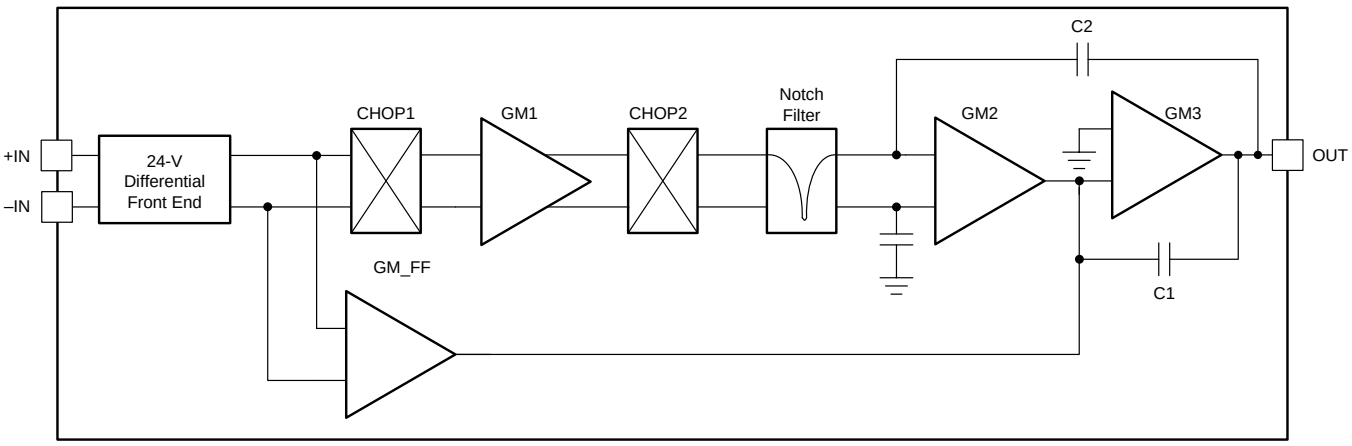
7.1 Overview

The TLV2186 operational amplifier combines precision offset and drift with excellent overall performance, making the device a great choice for a wide variety of precision applications. The precision offset drift of only 0.1 µV/°C provides stability over the entire operating temperature range of –40°C to +125°C. In addition, this device offers excellent linear performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate. See the *Layout Guidelines* section for details and a layout example.

The TLV2186 is part of a family of zero-drift, MUX-friendly, rail-to-rail output operational amplifiers. This device operates from 4.5 V to 24 V, is unity-gain stable, and is designed for a wide range of general-purpose and precision applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise, zero flicker noise, and outstanding distortion performance when operating below the chopper frequency.

7.2 Functional Block Diagram

The *Functional Block Diagram* shows a representation of the proprietary TLV2186 architecture.



7.3 Feature Description

The TLV2186 operational amplifier has several integrated features to help maintain a high level of precision through a variety of applications. These include a rail-to-rail inputs, phase-reversal protection, input bias current clock feedthrough, EMI rejection, electrical overstress protection and MUX-friendly Inputs.

7.3.1 Rail-to-Rail Inputs

Unlike many chopper amplifiers, the TLV2186 has rail-to-rail inputs that allow the input common-mode voltage to not only reach, but exceed the supply voltages by 200 mV. This configuration simplifies power-supply requirements by not requiring headroom over the input signal range.

The TLV2186 is specified for operation from 4.5 V to 24 V (±2.25 V to ±12 V) with rail-to-rail inputs. Many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

7.3.2 Phase-Reversal Protection

The TLV2186 has internal phase-reversal protection. Some op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV2186 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in 图 39.

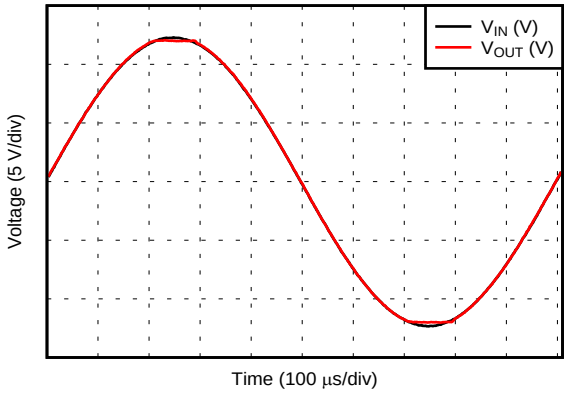


图 39. No Phase Reversal

7.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers such as the TLV2186 use a switching architecture on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the pulses from amplifying, however the pulses may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter, such as an RC network.

Feature Description (接下页)

7.3.4 EMI Rejection

The TLV2186 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV2186 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 40 shows the results of this testing on the TLV2186. 表 2 lists the EMIRR +IN values for the TLV2186 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 2 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

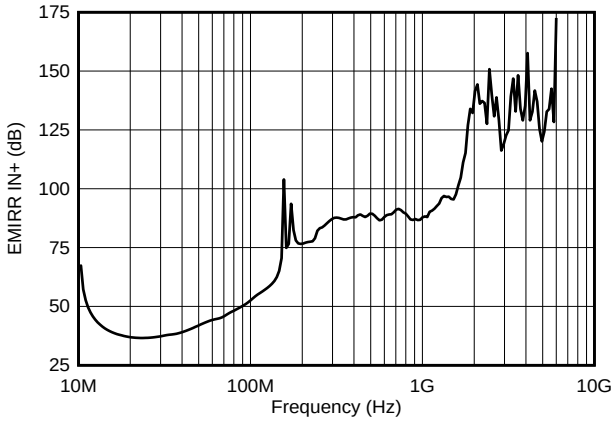


图 40. EMIRR Testing

表 2. TLV2186 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	48.4 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	69.1 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	88.9 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.5 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	95.5 dB

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR +IN, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance
- EMIRR is more simple to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any pin of the operational amplifier may result in adverse effects, as the amplifier would not have sufficient loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output may result in unexpected dc offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

The EMIRR +IN of the TLV2186 is plotted versus frequency as shown in 图 40. The TLV2186 unity-gain bandwidth is 750 kHz. EMIRR performance below this frequency denotes interfering signals that fall within the op amp bandwidth.

7.3.4.1 EMIRR +IN Test Configuration

图 41 shows the circuit configuration for testing the EMIRR +IN. An RF source is connected to the op amp noninverting input terminal using a transmission line. The op amp is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The multimeter samples and measures the resulting DC offset voltage. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy.

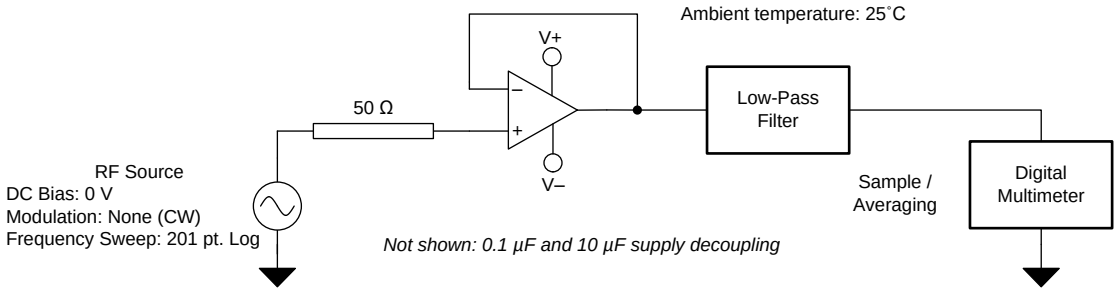


图 41. EMIRR +IN Test Configuration

7.3.5 Electrical Overstress

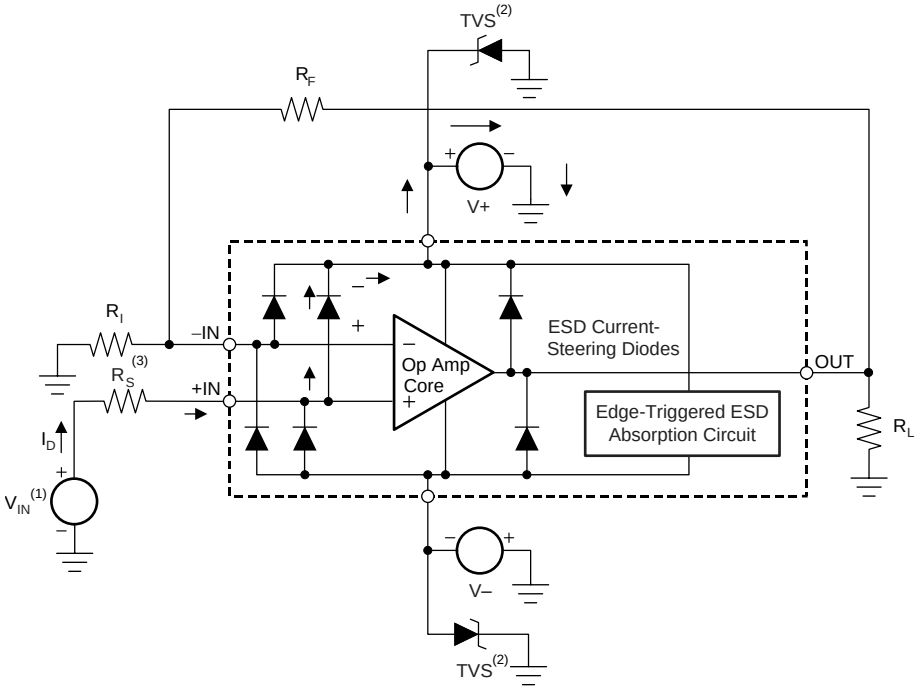
Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. See 图 42 for an illustration of the ESD circuits contained in the TLV2186 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger or threshold voltage that is greater than the normal operating voltage of the TLV2186, but less than the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit, as shown in 图 42, the ESD protection components are intended to remain inactive, and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.



(1) V_{IN} = (V+) + 500 mV

(2) TVS: 26 V > $V_{TVSBR\ (min)}$ > V+ ; where $V_{TVSBR\ (min)}$ is the minimum specified value for the transient voltage suppressor breakdown voltage.

(3) Suggested value is approximately 5 kΩ in example overvoltage condition.

图 42. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

图 42 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies V+ or V– are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current-steering diodes. This state is not a normal bias condition; the amplifier most likely does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, external zener diodes must be added to the supply pins, as shown in 图 42. The zener voltage must be selected such that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

7.3.6 MUX-Friendly Inputs

The TLV2186 features a proprietary input stage design that allows an input differential voltage to be applied while maintaining high input impedance. Typically, high-voltage CMOS or bipolar-junction input amplifiers feature antiparallel diodes that protect input transistors from large V_{GS} voltages that may exceed the semiconductor process maximum and permanently damage the device. Large V_{GS} voltages can be forced when applying a large input step, switching between channels, or attempting to use the amplifier as a comparator.

The TLV2186 solves these problems with a switched-input technique that prevents large input bias currents when large differential voltages are applied. This solves many issues seen in switched or multiplexed applications, where large disruptions to RC filtering networks are caused by fast switching between large potentials. The TLV2186 offers outstanding settling performance as a result of these design innovations and built-in slew rate boost and wide bandwidth. The TLV2186 can also be used as a comparator. Differential and common-mode *Absolute Maximum Ratings* still apply relative to the power supplies.

7.4 Device Functional Modes

The TLV2186 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the TLV2186 is 24 V (±12 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV2186 operational amplifier combines precision offset and drift with excellent overall performance, making the device ideal for many precision applications. The precision offset drift of only 0.1 µV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The following application examples highlight only a few of the circuits where the TLV2186 can be used.

8.1.1 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

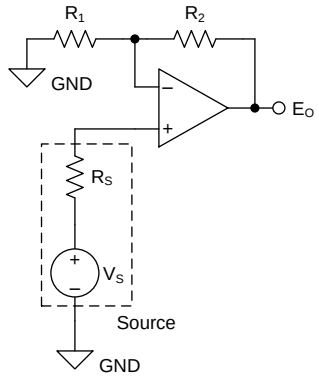
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

图 43 illustrates both noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the TLV2186 means that the current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

Application Information (接下页)

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$(1)\quad E_O = \left(1 + \frac{R_2}{R_1}\right) \cdot \sqrt{(e_S)^2 + (e_N)^2 + \left(e_{R_1 \| R_2}\right)^2 + (i_N \cdot R_S)^2 + \left(i_N \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

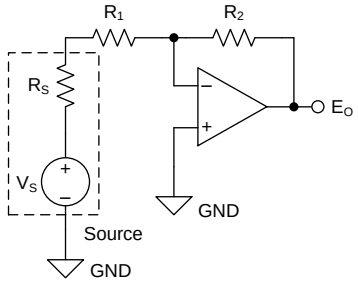
$$(2)\quad e_S = \sqrt{4 \cdot k_B \cdot T(K) \cdot R_S} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_S$$

$$(3)\quad e_{R_1 \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_1 \| R_2$$

$$(4)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(5)\quad T(K) = 237.15 + T(°C) \quad [\,K\,] \quad \text{Temperature in kelvins}$$

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$(6)\quad E_O = \left(1 + \frac{R_2}{R_S + R_1}\right) \cdot \sqrt{(e_N)^2 + \left(e_{R_1 + R_S \| R_2}\right)^2 + \left(i_N \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

$$(7)\quad e_{R_1 + R_S \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } (R_1 + R_S) \| R_2$$

$$(8)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(9)\quad T(K) = 237.15 + T(°C) \quad [\,K\,] \quad \text{Temperature in kelvins}$$

(1) e_n is the voltage noise spectral density of the amplifier. For the TLV2186 series of operational amplifiers, e_n = 38 nV/$\sqrt{Hz}$ at 1 kHz.

(2) For additional resources on noise calculations visit *TI Precision Labs*.

图 43. Noise Calculation in Gain Configurations

8.2 Typical Applications

8.2.1 High-Side Current Sensing

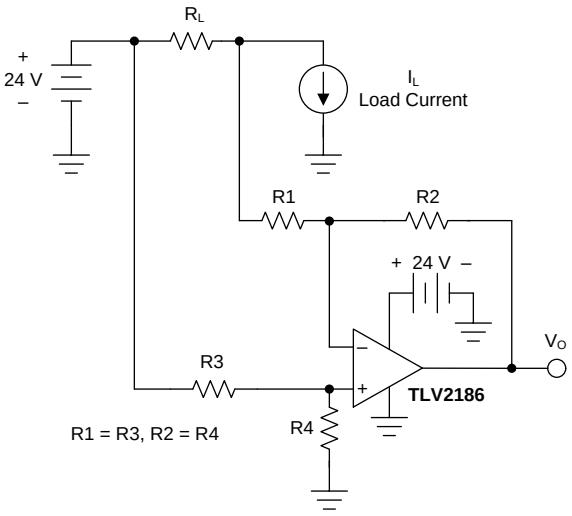


图 44. High-Side Current Monitor

8.2.1.1 Design Requirements

A common systems requirement is to monitor the current being delivered to a load. Monitoring makes sure that normal current levels are being maintained, and also provides an alert if an overcurrent condition occurs.

Fortunately, a relatively simple current monitor solution can be achieved using a precision rail-to-rail input/output op amp such as the TLV2186. This device has an input common-mode voltage (V_{CM}) range that extends 200 mV beyond each power supply rail allowing for operation at the supply rail.

The TLV2186 is configured as a difference amplifier with a predetermined gain. The difference amplifier inputs are connected across a sense resistor through which the load current flows. The sense resistor may be connected to the high side or low side of the circuit through which the load current flows. Commonly, high-side current sensing is applied and an applicable TLV2186 configuration is in 图 44. Low-side current sensing may be applied as well if the sense resistor can be placed between the load and ground.

Use the following parameters for this design example:

- Single supply: 24 V
- Linear output voltage range: 0.3 V to 3.3 V
- I_{load}: 1 A to 11 A

The design details and equations below can be used to reconfigure this design for different output voltage ranges and current loads.

8.2.1.2 Detailed Design Procedure

Designing a high-side current monitor circuit is straightforward providing the amplifier electrical characteristics are carefully consideration so that linear operation is maintained. Other additional considerations, such as the input voltage range of the analog to digital converter (ADC) that follows the current monitor stage, must be kept in mind while configuring the system.

Consider the design of a TLV2186 high-side current monitor with an output voltage range set to be compatible with the input of ADC with an input range of 3.3 V, such as one integrated in a microcontroller. The full-scale input range of such a converter is 0 V to 3.3 V. The TLV2186 can be operated from a single 24-V supply, referenced to ground. Although the TLV2186 is specified as a rail-to-rail input/output (RRIO) amplifier, the linear output operating range (like all amplifiers) does not quite extend all the way to the supply rails. This linear operating range must be taken into consideration.

Typical Applications (接下页)

The TLV2186 is powered by 24 V; therefore, the device is easily capable of providing the 3.3-V positive level, or even more if the ADC has a wider input range. However, because the TLV2186 output does not swing completely to 0 V, the specified lower swing limit must be observed in the design.

The best measure of an op amp linear output voltage range comes from the open-loop voltage gain (A_{OL}) specification listed in the *Electrical Characteristics* table. The A_{OL} test conditions specify a linear swing range 300 mV from each supply rail (R_L = 10 kΩ). Therefore, the linear swing limit on the low end (V_{oMIN}) is 300 mV, and 3.3 V is the V_{oMAX} limit, thus yielding an 11:1 V_{oMAX} to V_{oMIN} ratio. This ratio proves important in determining the difference amplifier operating parameters.

An optimum load current, I_{LOAD} of 10 A is used as an example. In most applications, however, the ability to monitor current levels well below 10 A is useful. This situation is where the 11:1 V_{oMAX} to V_{oMIN} ratio is crucial. If 11 A is set as the maximum current, this current must correspond to a 3.3-V output. Using the 11:1 ratio, the minimum current of 1 A corresponds to 300 mV.

Selection of the current sense resistor R_S comes down to how much voltage drop can be tolerated at maximum current and the permissible power loss, or dissipation. A good compromise for a 10-A sense application is an R_S of 10 mΩ. That value results in a power dissipation of 1 W, and a 0.1-V drop at 10 amps.

Next, determine the gain of the TLV2186 difference amplifier circuit. The maximum current of 11 A flowing through a 10-mΩ sense resistor results in 110 mV across the resistor. That voltage appears as a differential voltage, V_R, that is applied across the TLV2186 difference amplifier circuit inputs:

$$V_S = I_L * R_S$$
$$V_S = 11\,A * 10\,m\Omega = 110\,mV \quad (1)$$

The TLV2186 required voltage gain is determined from:

$$G_A = \frac{V_{OMAX}}{V_S}$$
$$G_A = \frac{3.3\,V}{0.11\,V} = 30\frac{V}{V} \quad (2)$$

Now, checking the V_{oMIN} using I_L = 1 A:

$$V_{OMIN} = G_A * I_{SMIN} * R_S$$
$$V_{OMIN} = 30\frac{V}{V} * 1\,A * 10\,m\Omega = 300\,mV \quad (3)$$

The complete TLV2186 high-side current monitor is shown in 图 45. The circuit is capable of monitoring a current range of < 1 A to 11 A, with a V_{CM} very close to the 24-V supply voltage.

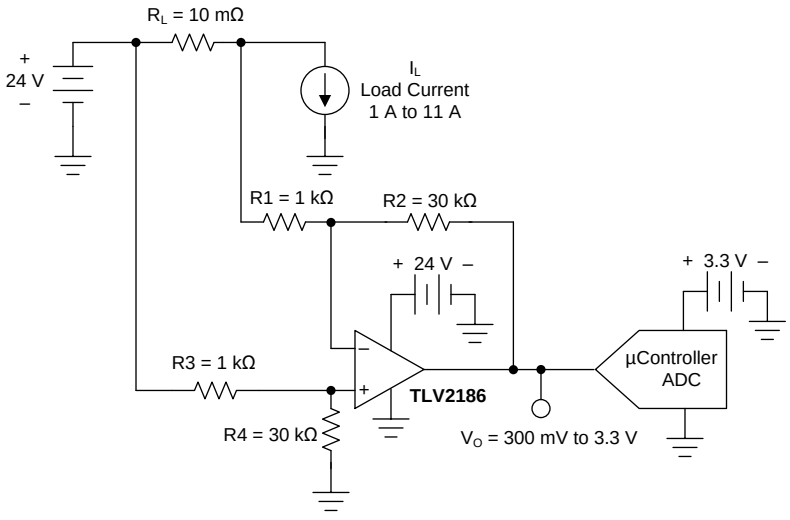


图 45. TLV2186 Configured as a High-Side Current Monitor

Typical Applications (接下页)

In this example, the TLV2186 output voltage is intentionally limited to 3.3 V. However, because of the 24-V supply, the output voltage could be much higher to allow for a higher-voltage data converter with a higher dynamic range.

The circuit in 图 45 was checked using the TINA Spice circuit simulation tool to verify the correct operation of the TLV2186 high-side current monitor. The simulation results are seen in 图 46. The performance is exactly as expected. Upon careful inspection of the plots, one possible surprise is that V_O continues towards zero as the sense current drops below 1 A, where V_O is 300 mV and less.

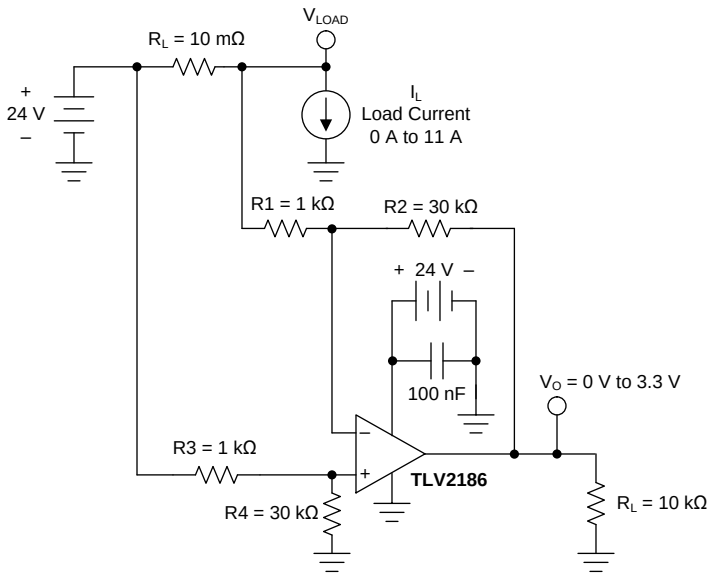


图 46. TLV2186 High-Side Current-Monitor Simulation Schematic

The TLV2186 output, as well as other CMOS output amplifiers, often swing closer to 0 V than the linear output parameters suggest. The *Electrical Characteristics* table lists under the OUTPUT subsection V_O, which is an *output slam* to the rail measure. It is not an indication of the linear output range, but instead how close the output can move towards the supply rail. In that region, the amplifier output approaches saturation, and the amplifier ceases to operate linearly. Thus, in the current-monitor application, the current-measurement capability may continue well below the 300 mV output level. However, keep in mind that the linearity errors are becoming large.

Lastly, some notes about maximizing the high-side current monitor performance:

- All resistor values are critical for accurate gain results. The resistor pairs of [R1 and R3] and [R2 and R4] must be matched as closely as possible to minimize common-mode mismatch error. Use a 0.1% tolerance, or better. Often, selecting two adjacent resistors on a reel provides close matching compared to random selection.
- Keep the closed-loop gain, G_A, to which the TLV2186 difference amplifier is set, to a reasonable value. Doing so reduces gain error and can be used to maximize bandwidth. A G_A of 30 V/V is used in the example.
- Although current monitoring is often used for monitoring dc supply currents, ac current can also be monitored. The –3-dB bandwidth, or upper cutoff frequency, of the circuit of is:

$$f_H = \frac{GBW}{\text{Noise Gain}} \quad (4)$$

where

- GBW is the amplifier unity gain bandwidth; 750 kHz for the TLV2186.
- Noise gain is equal to the gain as seen looking into the op amp noninverting input, as shown in 公式 5.

$$G_{NG} = 1 + \frac{R2}{R1} \quad (5)$$

Typical Applications (接下页)

For the TLV2186 circuit in 图 45:

$$G_{NG} = 1 + \frac{30\ k\Omega}{1\ k\Omega} = 31\frac{V}{V}$$

$$f_H = \frac{750\ kHz}{31} = 24.2\ kHz$$

Make sure that the amplifier slew rate is sufficient to support the expected output voltage swing range and waveform. Also, if a single power supply such as 24 V is used, the ac power source applied to the sense input must have a positive dc component to keep the V_{CM} above 0 V. The input voltage cannot drop below 0 V if normal operation is to be maintained.

The TLV2186 output can attain a 0 V output level if a small negative voltage is used to power the V– pin instead of ground. The LM7705 is a switched capacitor voltage inverter with a regulated, low-noise, –0.23-V fixed voltage output. Powering the TLV2186 V– pin at this level approximately matches the 300-mV linear output voltage swing lower limit, thus extending the output swing to 0 V, or very near 0 V. Doing so greatly improves the resolution at low sense current levels.

The LM7705 requires only about 78 μA of quiescent current, but be aware that the specified supply range is 3 V to 5.25 V. The 3.3-V or 5-V supply used by the ADC could be tapped as a power source.

For more information about amplifier-based, high-side current monitors, see the *TI Analog Engineer's Circuit Cookbook: Amplifiers*.

8.2.1.3 Application Curve

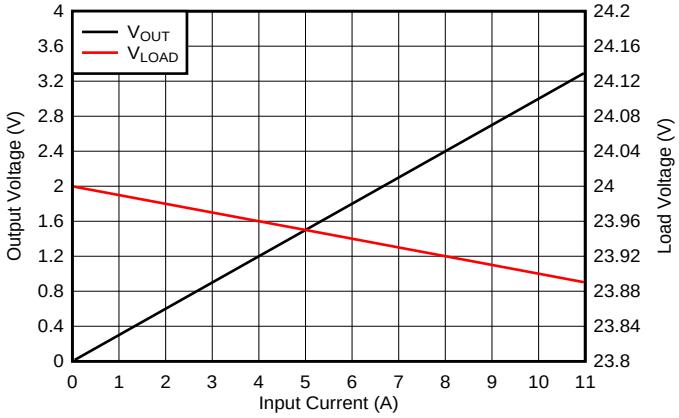


图 47. High-Side Results

Typical Applications (接下页)

8.2.2 Bridge Amplifier

图 48 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI file: *Bridge Amplifier Circuit*.

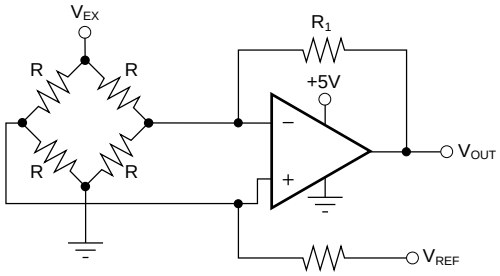


图 48. Bridge Amplifier

8.2.3 Low-Side Current Monitor

图 49 shows the TLV2186 configured in a low-side current-sensing application. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the TLV2186, with a gain of 201. In this example, the load current is set from 0 A to 500 mA, and corresponds to an output voltage range from 0 V to 10 V. The output range can be adjusted by changing the shunt resistor or gain of the configuration. Click the following link to download the TINA-TI file: *Current-Sensing Circuit*.

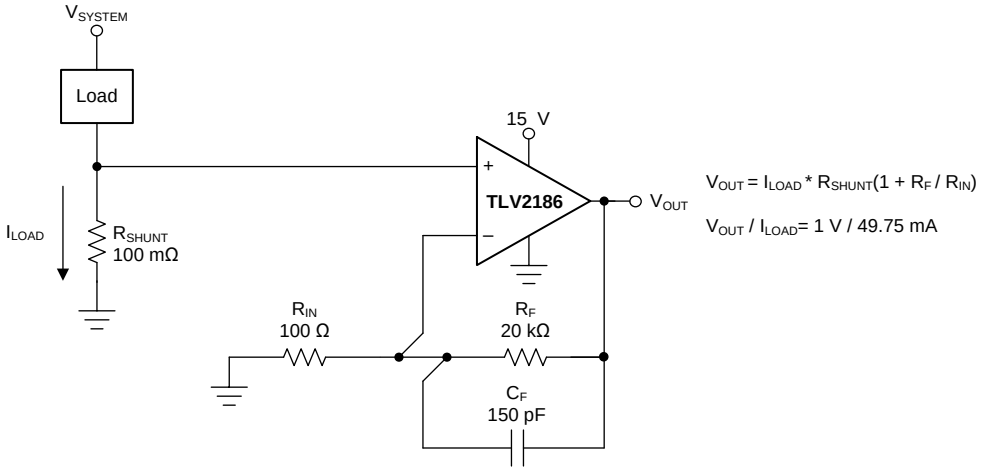
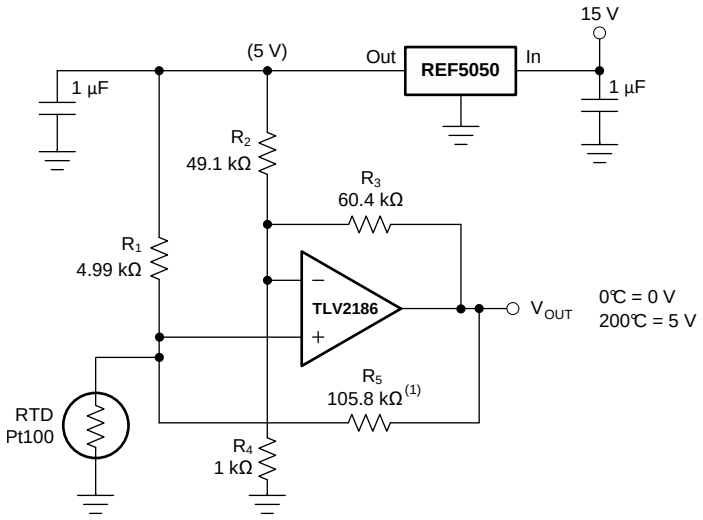


图 49. Low-Side Current Monitor

Typical Applications (接下页)

8.2.4 RTD Amplifier With Linearization

See the *Analog Linearization of Resistance Temperature Detectors* technical brief for an in-depth analysis of 图 50. Click the following link to download the TINA-TI file: *RTD Amplifier with Linearization*.



(1) R_5 provides positive-varying excitation to linearize output.

图 50. RTD Amplifier With Linearization

9 Power Supply Recommendations

The TLV2186 is specified for operation from 4.5 V to 24 V (±2.25 V to ±12 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- For the lowest offset voltage, avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Also:
  - Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
  - Thermally isolate components from power supplies or other heat sources.
  - Shield operational amplifier and input circuitry from air currents, such as cooling fans.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see*The PCB is a component of op amp design*.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in 图 51, keep the feedback resistor (R3) and gain resistor (R4) close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

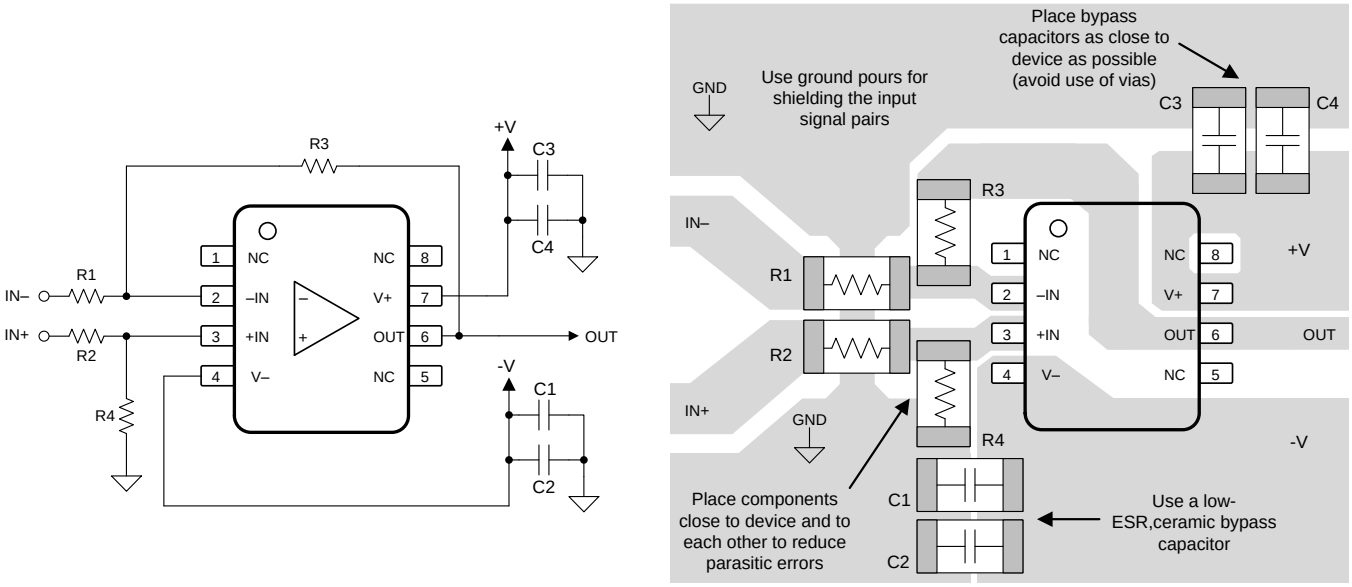


图 51. Operational Amplifier Board Layout for Difference Amplifier Configuration

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA-TI™ 是一款基于 SPICE 引擎的电路仿真程序，简单易用并且功能强大。TINA-TI™ 是 TINA™软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI™ 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI™ 提供全面的后处理能力，便于用户以多种方式获得结果，用户可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的功能，从而构建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI™ 软件。请下载 TINA-TI™ 文件夹中的免费 TINA-TI™ 软件。

11.1.1.2 TI 高精度设计

欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。TI 高精度设计是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《零漂移放大器：特性和优势》*
- 德州仪器 (TI)，*《运算放大器设计组件 PCB》*
- 德州仪器 (TI)，*《适合所有人的运算放大器》*
- 德州仪器 (TI)，*《运算放大器增益稳定性，第 3 部分：交流增益误差分析》*
- 德州仪器 (TI)，*《运算放大器增益稳定性，第 2 部分：直流增益误差分析》*
- 德州仪器 (TI)，*《在全差分有源滤波器中使用无限增益、MFB 滤波器拓扑》*
- 德州仪器 (TI)，*《运算放大器性能分析》*
- 德州仪器 (TI)，*《运算放大器的单电源运行》*
- 德州仪器 (TI)，*《放大器调优》*
- 德州仪器 (TI)，*《无铅组件涂层的储存寿命评估》*
- 德州仪器 (TI)，*《反馈曲线图定义运算放大器交流性能》*
- 德州仪器 (TI)，*《运算放大器的 EMI 抑制比》*
- 德州仪器 (TI)，*《电阻式温度检测器的模拟线性化》*
- 德州仪器 (TI)，*《TI 精密设计 TIPD102 高侧电压-电流 (V-I) 转换器》*

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration

社区资源 **(**接下页**)**

among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

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TINA, DesignSoft are trademarks of DesignSoft, Inc.
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11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2186IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T2186	Samples
TLV2186IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PVDY	Samples
TLV2186IDSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PVDY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

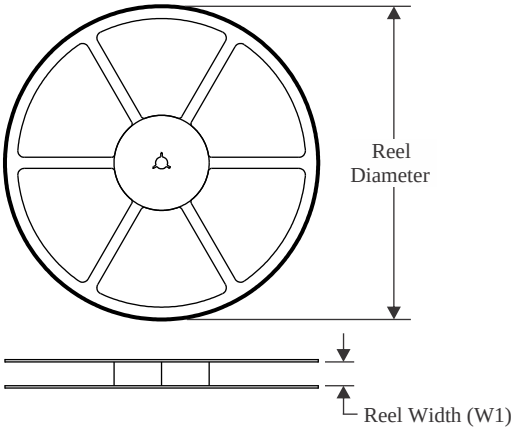
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

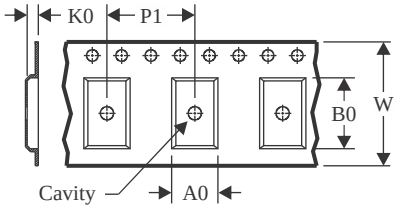
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

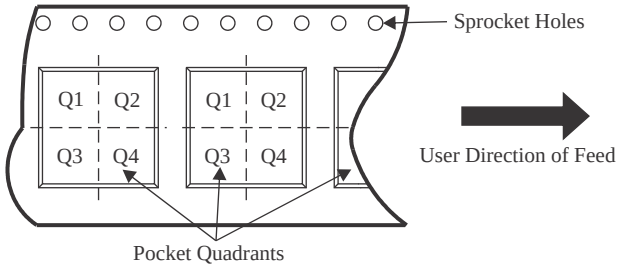


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

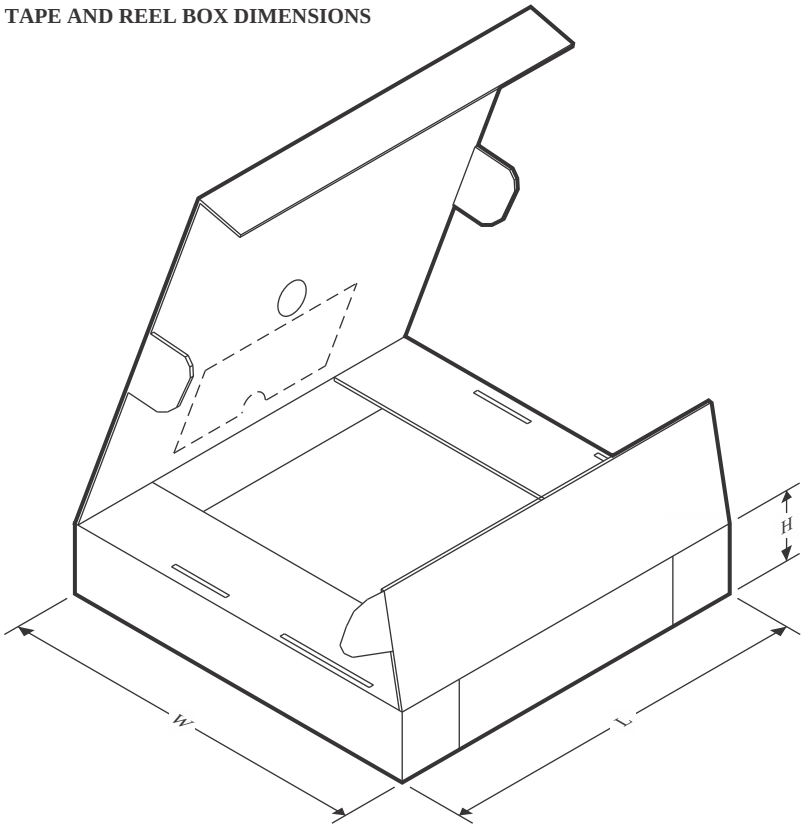
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2186IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2186IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV2186IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2186IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV2186IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV2186IDSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

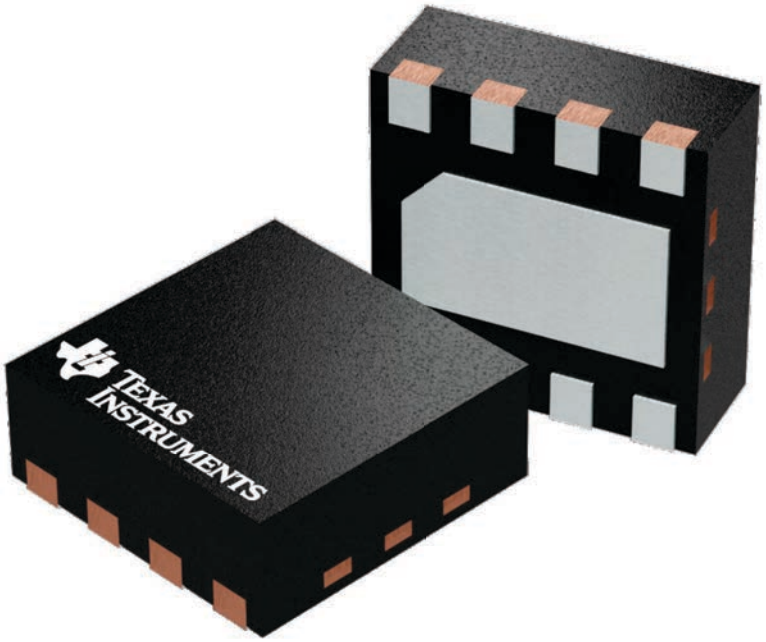
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



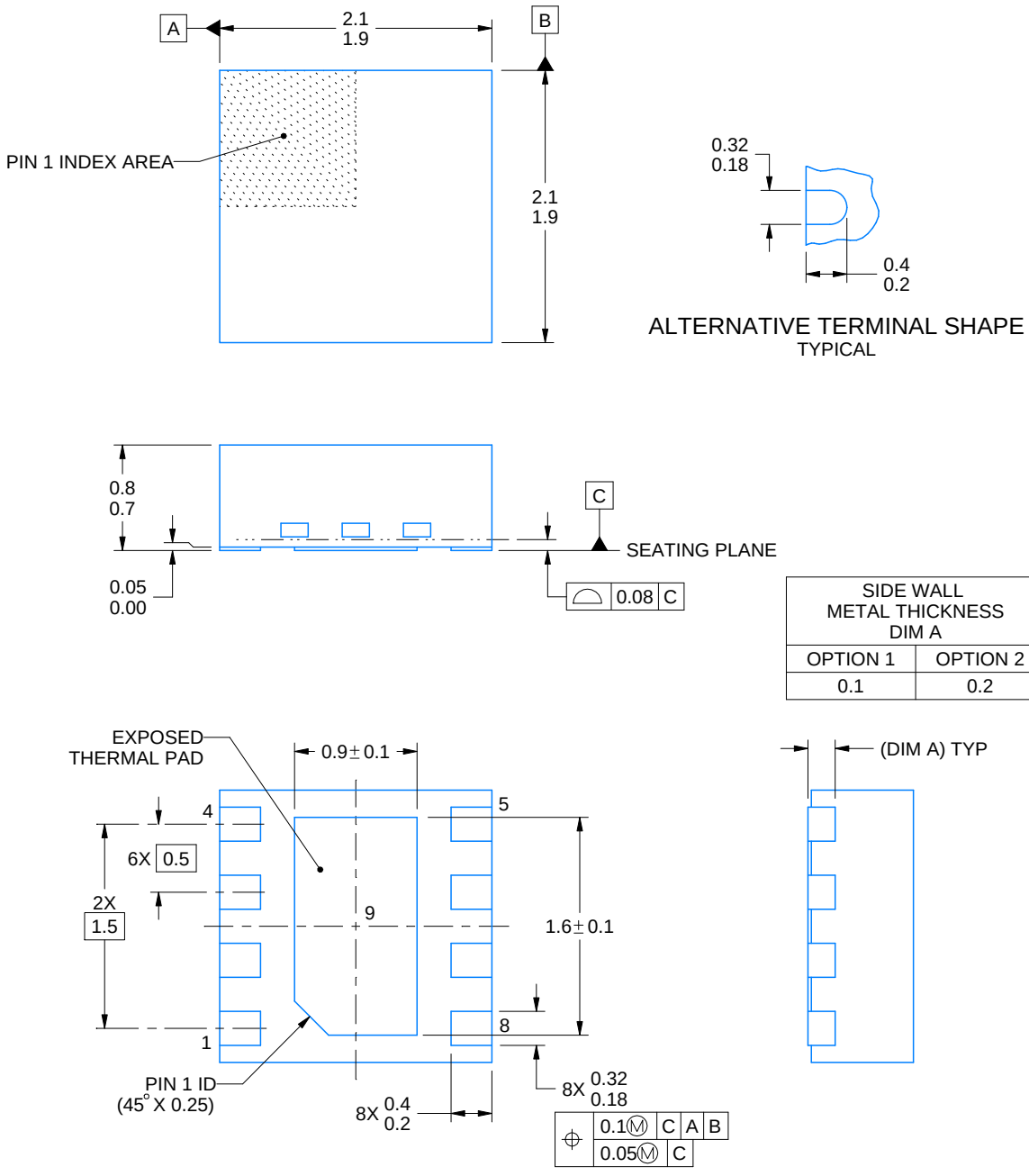
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

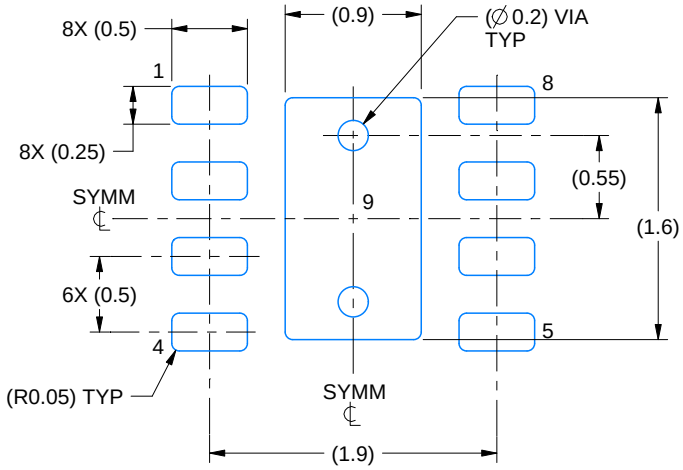
PLASTIC SMALL OUTLINE - NO LEAD



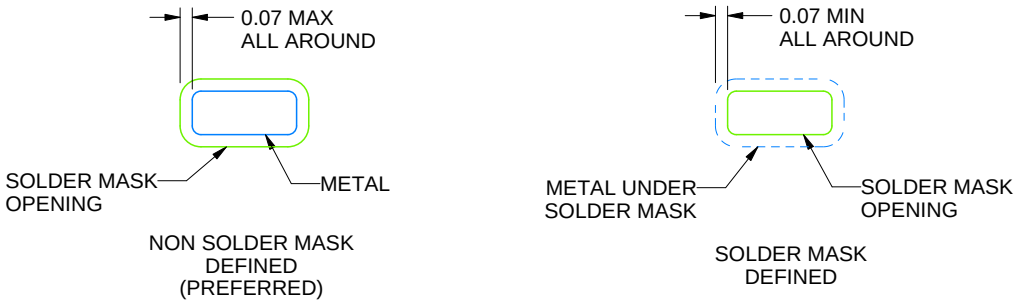
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

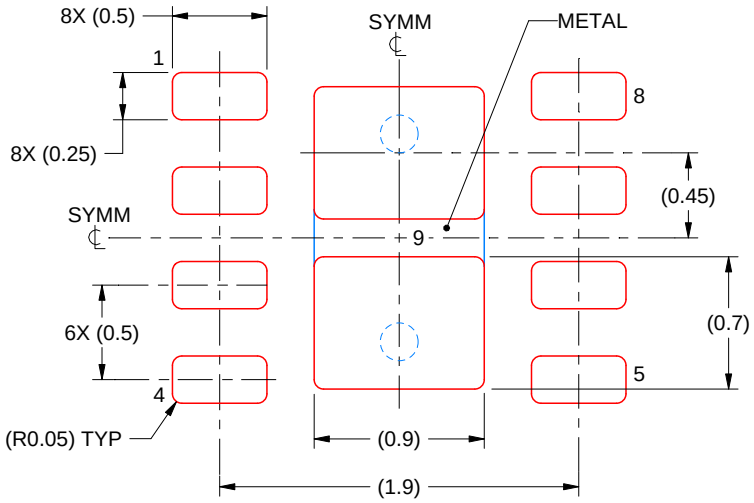


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



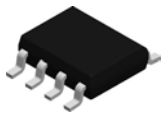
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

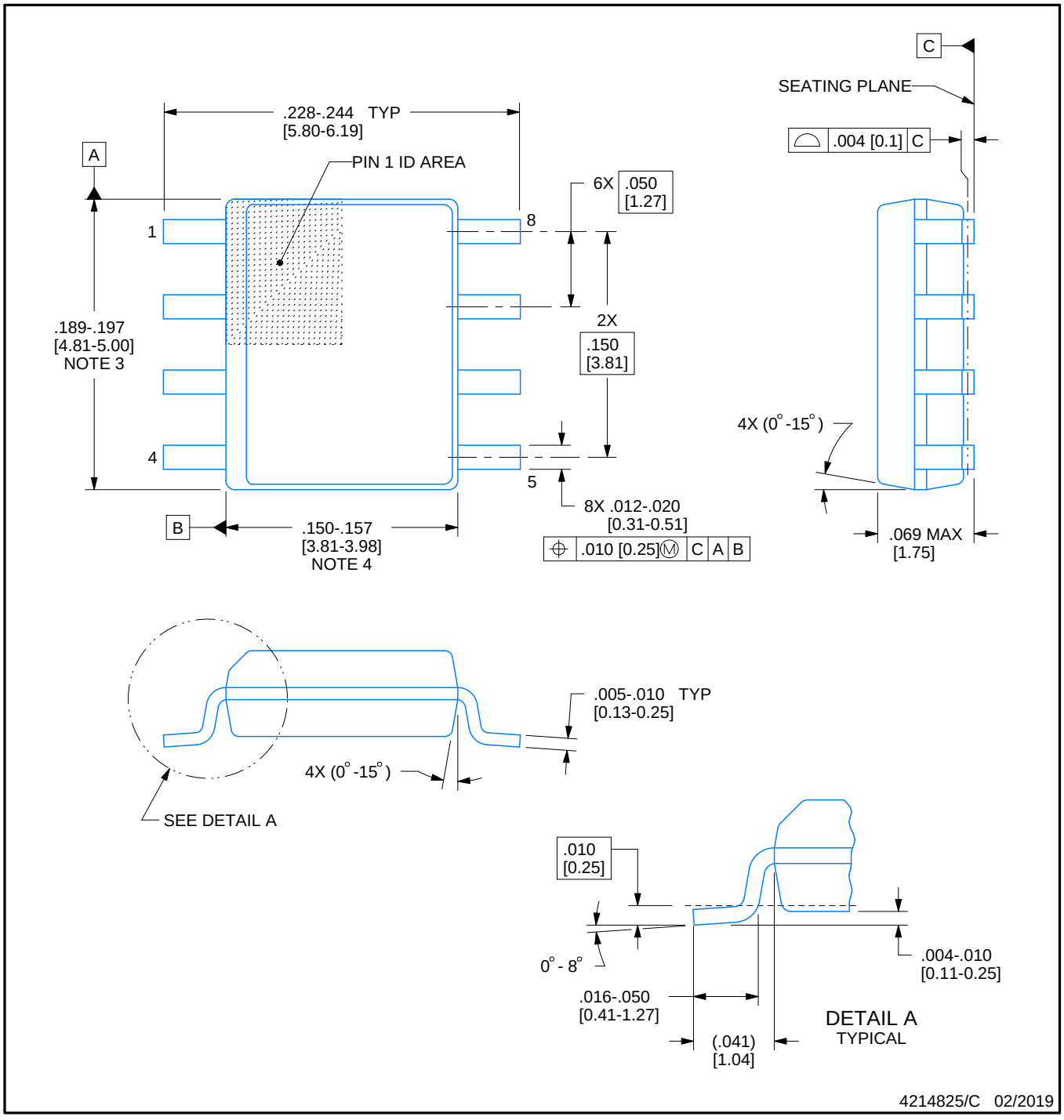


PACKAGE OUTLINE

D0008A

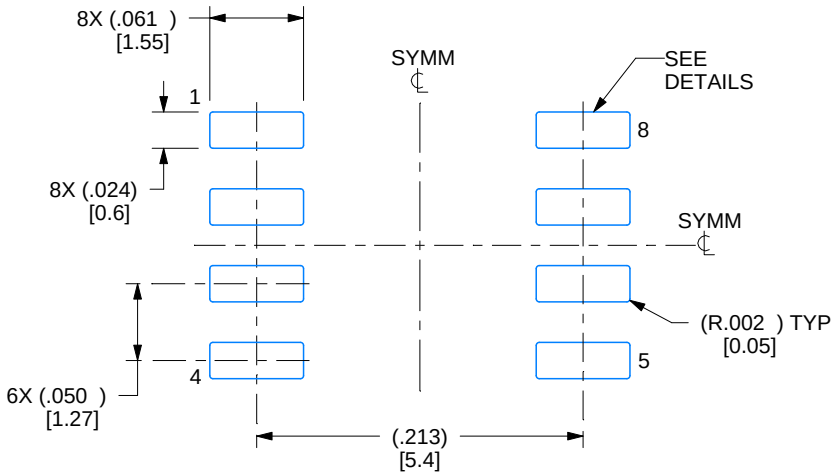
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

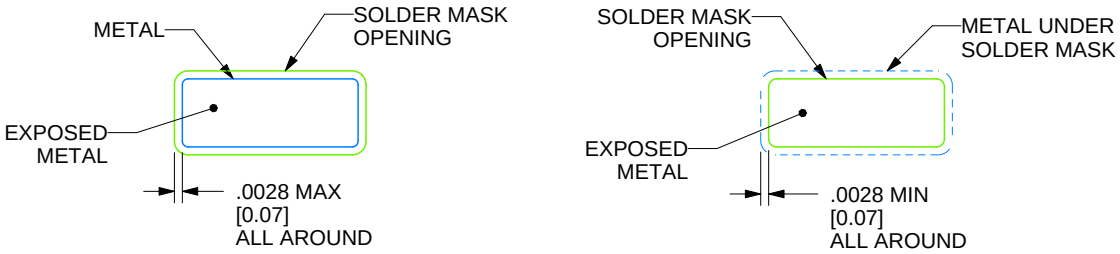


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

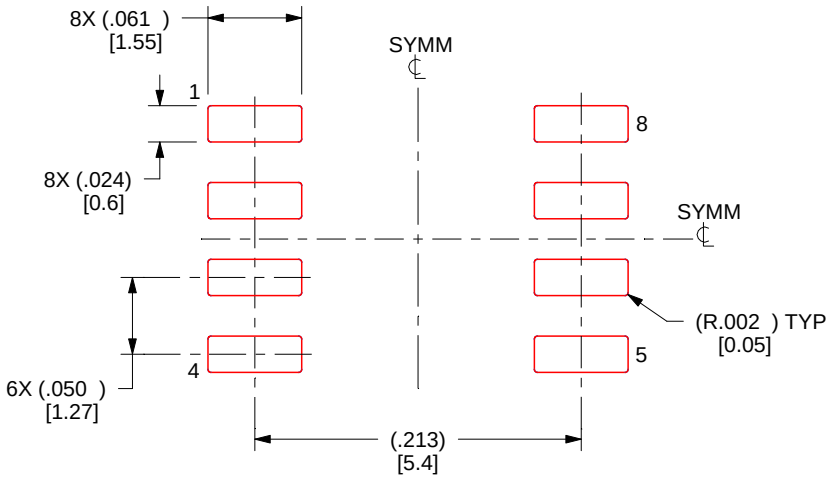
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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