具有集成开关的 4.5V 至 18V 输入、1.5A 降压转换器

1 特性

- 1.5A 持续输出电流
- 4.5V 至 18V 电源电压范围
- 2V 至 18V 转换电压范围
- DCAP2™ 模式控制支持快速瞬态响应
- 低输出纹波且支持所有 MLCC 输出电容器
- 用于轻负载控制的跳跃模式
- 针对较低占空比应用进行了优化的高效率集成式 FET
- 高效率，关断时电源电流少于 10μA
- 软启动时间可调节
- 支持预偏置软启动
- 700kHz 开关频率
- 逐周期过流限制
- 漏极开路电源正常指示
- 内部自举开关
- 小型 3mm × 3mm 16 引脚 QFN (RGT) 封装

2 应用

- 服务器负载点
- 用于计算电源系统的分布式非隔离型直流/直流转换器

3 说明

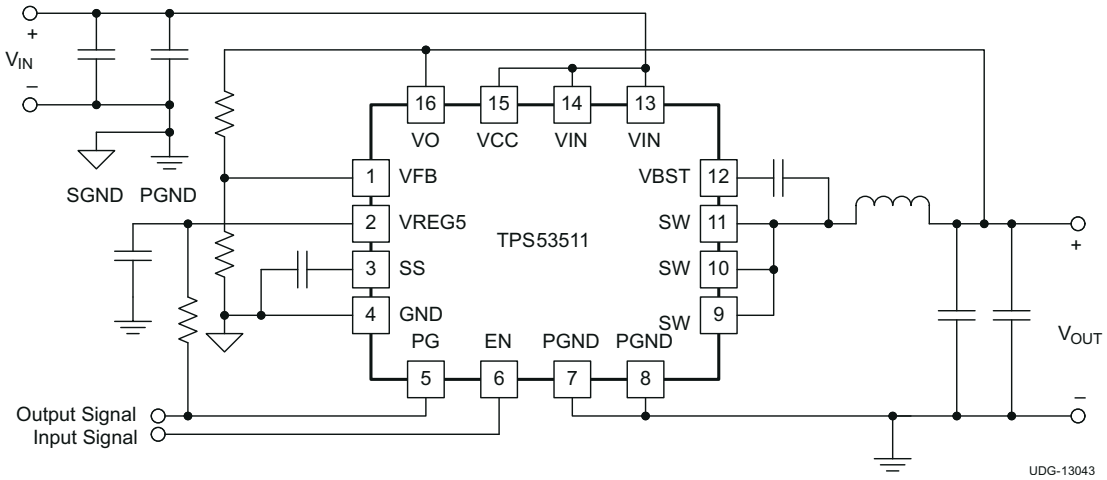
TPS53511 是一款自适应导通时间 D-CAP2™ 模式同步降压转换器。该器件适用于计算电源系统中的负载点 (POL)，并提供了一种具有成本效益、低元件数量的低待机电流解决方案。TPS53511 的主控制环路采用 D-CAP2™ 模式控制，无需外部元件便可实现快速瞬态响应。自适应导通时间控制支持在高负载条件下 PWM 模式与轻负载条件下减频运行之间的无缝操作，从而实现高效率。

TPS53511 的专有电路还可使其适应低等效串联电阻 (ESR) 输出电容器（如 POSCAP 或 SP-CAP）和超低 ESR 陶瓷电容器。该器件采用 4.5V 至 18V 的电源输入电压以及 2V 至 18V 的输入电源电压工作，提供可调缓启动时间和电源正常功能，还支持预偏置软启动功能。TPS53511 采用 16 引脚 QFN 封装，设计运行温度范围为 -40°C 到 85°C。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS53511	VQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (May 2013) to Revision B (August 2021)	Page
• 添加了以下部分：*ESD 额定值、引脚配置和功能、概述、功能方框图、特性说明、器件功能模式、应用和实现、应用信息、典型应用、设计要求、详细设计过程、应用曲线、电源相关建议、布局、布局指南、布局示例、器件和文档支持、机械封装和可订购信息*	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Changed V_{ENH} min value to 1.5 V	6

Changes from Revision * (March 2013) to Revision A (May 2013)	Page
• Changed minimum value for Current limit specification in Electrical characteristics table	6
• Changed 图 6-3	8
• Changed 图 6-5	8
• Changed 图 6-6	8
• Changed 图 6-7	8
• Changed 图 6-11	8
• Changed 图 6-12	8
• Changed 图 8-1	13

5 Pin Configuration and Functions

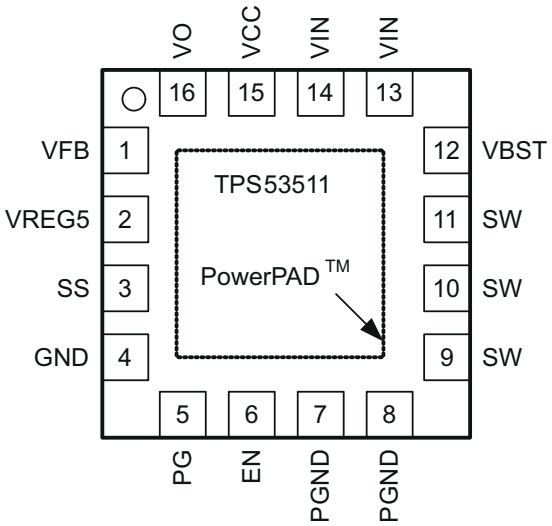


图 5-1. 16-Pin RGT Package (Top View)

表 5-1. Pin Functions

PIN		I/O/P	DESCRIPTION
NAME	NO.		
EN	6	I	Enable control input
GND	4	—	Signal ground pin
PG	5	O	Open-drain power-good output
PGND	7	P	Ground returns for low-side MOSFET. Also serves as inputs of current comparators. Connect PGND and GND strongly together near the device.
	8		
SS	3	I/O	Soft-start control. An external capacitor should be connected to GND.
SW	9	I/O	Switch node connection between high-side N-channel FET and low-side N-channel FET. Also serves as inputs to current comparator.
	10		
	11		
VBST	12	I	Supply input for high-side N-channel FET gate driver (boost terminal). Connect a capacitor from this pin to respective SW terminals. An internal PN diode is connected between the VREG5 and VBST pins.
VCC	15	I	Supply input for 5-V internal linear regulator for the control circuitry.
VFB	1	I	Converter feedback input. Connect with feedback resistor divider.
VIN	13	I	Power input and connected to high side N-channel FET drain
	14		
VO	16	I	Connect to the output of the converter. This terminal is used for on-time adjustment.
VREG5	2	O	5.5-V power supply output. A capacitor (typical 1-µF) should be connected to GND.
PowerPAD		—	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
Input voltage range	VIN, VCC, EN		–0.3	20	V
	VBST		–0.3	26	
	VBST (with respect to SW)		–0.3	6.5	
	SS, VO, VFB		–0.3	6.5	
	SW	DC	–2	20	
		Transient < 10 ns	–3	20	
Voltage differential	GND to PowerPAD		–0.2	0.2	V
Output voltage range	PG, VREG5		–0.3	6.5	V
	PGND		–0.3	0.3	
Output current	I_{OUT}			1.5	A
Storage junction temperature			–55	150	°C
Operating junction temperature			–40	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
Input voltage range	VIN		2.0		18.0	V
	VCC		4.5		18.0	
	EN		–0.1		18.0	
	VBST		–0.1		24.0	
	VBST(with respect to SW)		–0.1		5.7	
	VO, VFB, SS		–0.1		5.5	
	SW	DC	–1.8		18.0	
		Transient, < 10 ns	–3		18	
Output voltage range	PG, VREG5		–0.1		5.7	V
	PGND		–0.1		0.1	
Junction temperature range, T_J			–40		125	°C
Operating free-air temperature, T_A			–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS53511 QFN (RGT) 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	45.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	57.3	
θ_{JB}	Junction-to-board thermal resistance(4)	18.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	18.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	3.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

over recommended free-air temperature range, V_{VIN} = 12 V, PGND = GND (unless otherwise noted). (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VCC}	Operating, non-switching supply current	T_A = 25°C, V_{EN} = 5 V, V_{VFB} = 0.8 V		850	1300	µA
$I_{VCC(sdn)}$	Shutdown supply current	T_A = 25°C, V_{EN} = 0 V		1.8	10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage		1.5			V
V_{ENL}	EN low-level input voltage				0.4	V
V_{VFB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{VFB}	Voltage light load mode	T_A = 25°C, V_{OUT} = 1.05 V, I_{OUT} = 10 mA		771		mV
	Threshold voltage, continuous mode	T_A = 25°C, V_{OUT} = 1.05 V	757	765	773	mV
		T_A = 0°C to 85°C, V_{OUT} = 1.05 V(1)	753		777	
		T_A = –40°C to 85°C, V_{OUT} = 1.05 V(1)	751		779	
I_{VFB}	Input current	V_{FB} = 0.8 V, T_A = 25°C	-0.1	0	0.1	µA
R_{Dischg}	V_O discharge resistance	V_{EN} = 0 V, V_{OUT} = 0.5 V, T_A = 25°C		50	100	Ω
V_{VREG5} OUTPUT						
V_{VREG5}	Output voltage	T_A = 25°C, 6 V < V_{VCC} < 18 V, 0 < I_{VREG5} < 5 mA	5.3	5.5	5.7	V
V_{LN5}	Line regulation	6 V < V_{VCC} < 18 V, I_{VREG5} = 5 mA			20	mV
V_{LD5}	Load regulation	0 < I_{VREG5} < 5 mA			100	mV
I_{VREG5}	Output current	Vcc = 6 V, V_{VREG5} = 4 V, T_A = 25°C		70		mA
MOSFET						
$R_{DS(on)H}$	High-side switch resistance	T_A = 25°C, (V_{BST} – V_{SW}) = 5.5 V		120		mΩ
$R_{DS(on)L}$	Low-side switch resistance	T_A = 25°C		70		mΩ
CURRENT LIMIT						
I_{OCL}	Current limit	L_{OUT} = 1.5 µH(1)	1.65	2.00	2.75	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(1)		150		°C
		Hysteresis(1)		25		
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{VIN} = 12 V, V_{OUT} = 1.05 V		145		ns
$t_{OFF(min)}$	Minimum off time	T_A = 25°C, V_{VFB} = 0.7 V		260	310	ns
SOFT-START FUNCTION						
I_{SSC}	Soft-start charge current	V_{SS} = 0 V	1.4	2.0	2.6	µA
I_{SSD}	Soft-start discharge current	V_{SS} = 0.5 V	0.1	0.2		mA
POWER GOOD						
$V_{THPG(UV)}$	Power-good undervoltage threshold	V_{VFB} rising (good)	85%	90%	95%	
		V_{VFB} falling (fault)		85%		
$V_{THPG(OV)}$	Power-good overvoltage threshold	V_{VFB} rising (fault)	110%	115%	120%	
		V_{VFB} falling (good)		110%		
I_{PG}	Sink current	V_{PG} = 0.5 V	2.5	5.0		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	110%	115%	120%	
t_{OVPDEL}	Output OVP propagation delay			5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis		10%		

over recommended free-air temperature range, V_{VIN} = 12 V, PGND = GND (unless otherwise noted). (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{UVPDEL}	Output UVP delay			0.25		ms
t_{UVPEN}	Output UVP enable delay	Relative to soft-start time		t_{SS} × 1.7		
UNDERVOLTAGE LOCKOUT						
UVLO	Wakeup V_{REG5} voltage threshold		3.55	3.80	4.05	V
	Hysteresis V_{REG5} voltage threshold		0.23	0.35	0.47	

(1) Specified by design. Not production tested.
(2) See PS pin description for levels.

6.6 Typical Characteristics

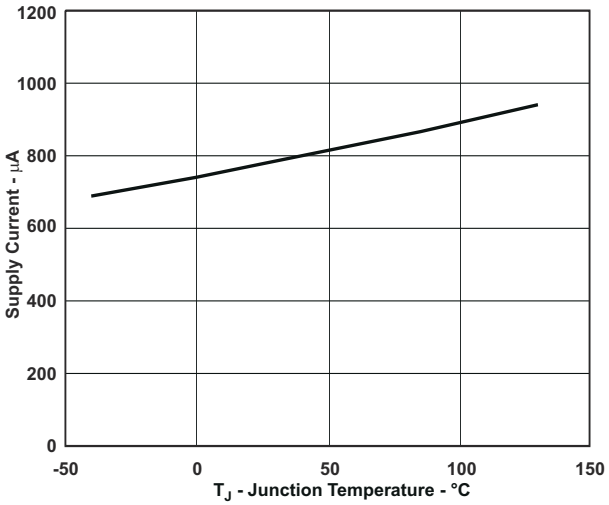


图 6-1. V_{CC} Supply Current vs. Junction Temperature

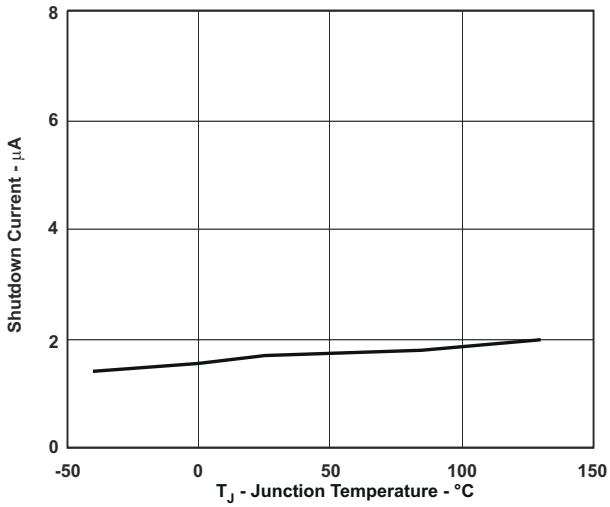


图 6-2. V_{CC} Shutdown Current vs. Junction Temperature

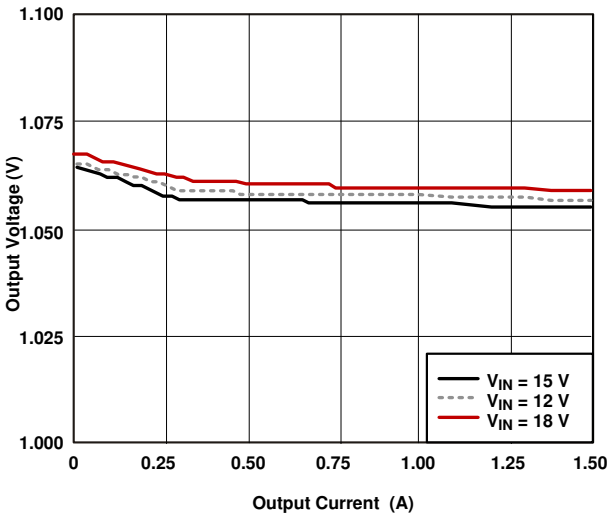


图 6-3. 1.05-V Output Voltage vs. Output Current

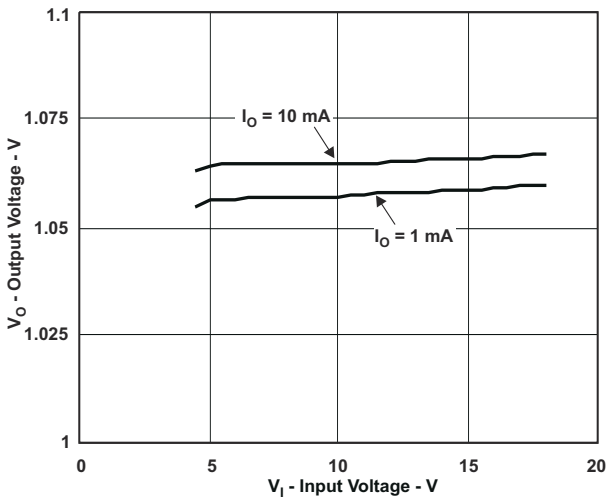


图 6-4. 1.05-V Output Voltage vs. Input Voltage

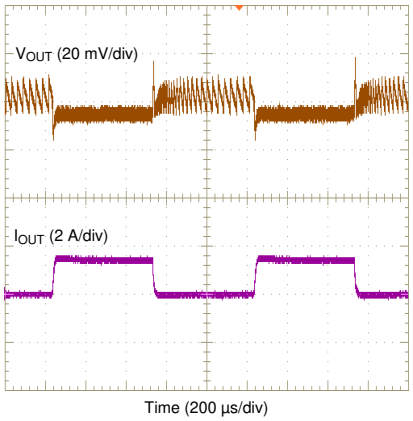


图 6-5. Load Transient Response, 1.05 V, 0 A to 1.5 A

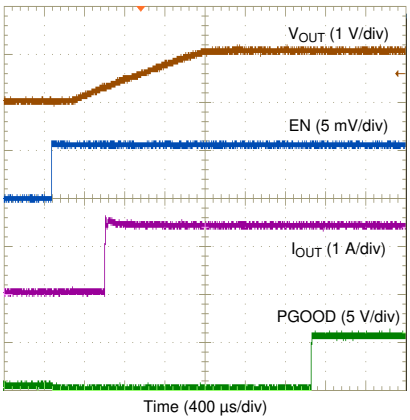


图 6-6. Start-Up

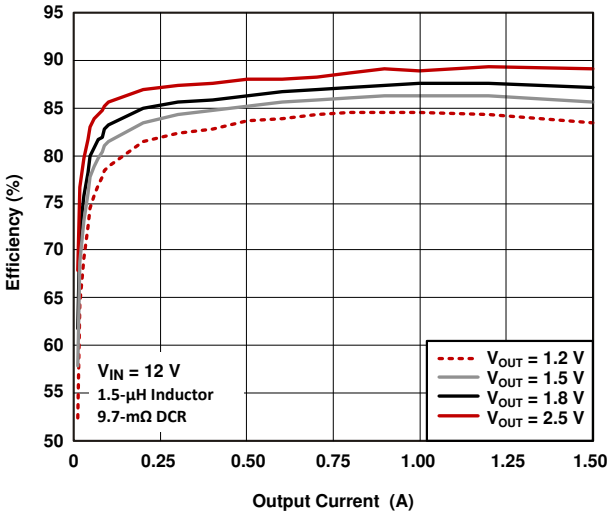


图 6-7. Efficiency vs. Output Current

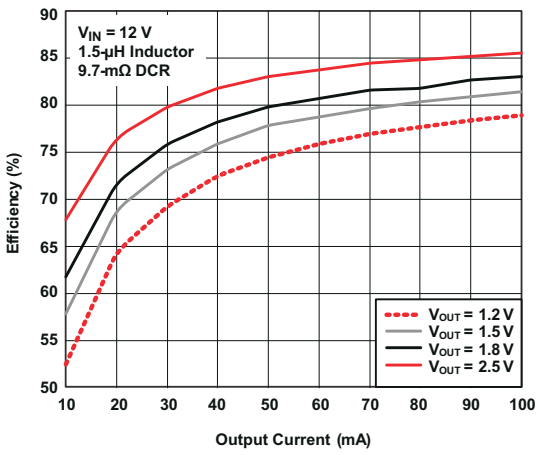


图 6-8. Light Load Efficiency vs. Output Current

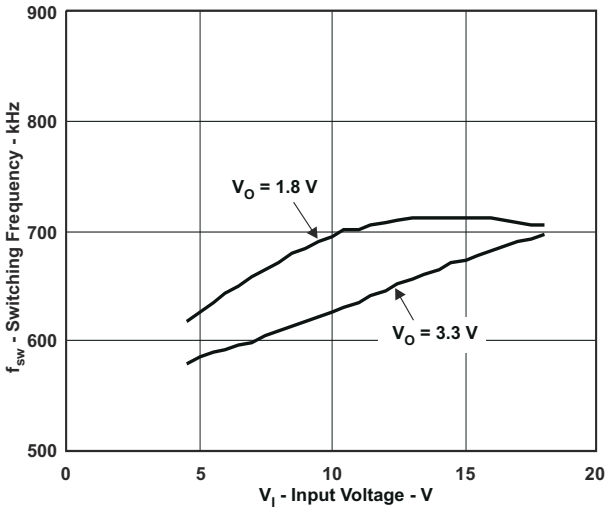


图 6-9. Switching Frequency vs Input Voltage

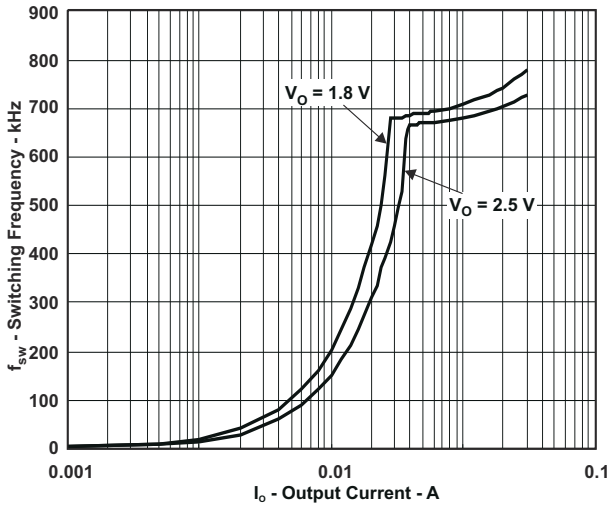


图 6-10. Switching Frequency vs Output Current

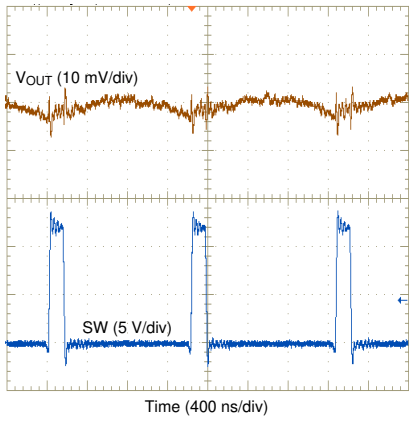


图 6-11. Output Voltage Ripple

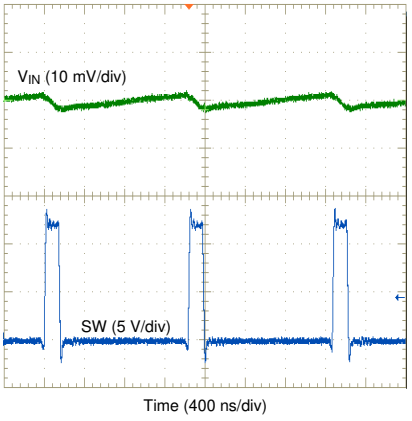


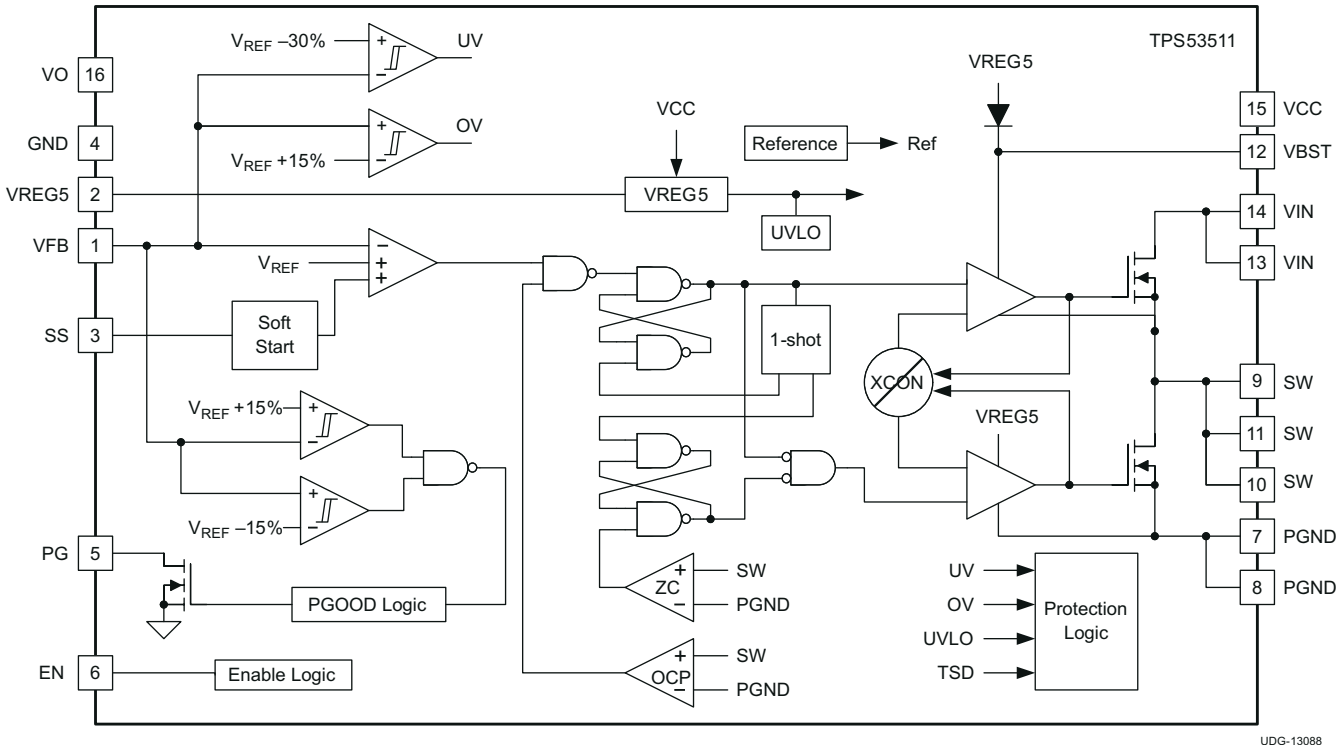
图 6-12. Input Voltage Ripple

7 Detailed Description

7.1 Overview

The TPS53511 is a 1.5-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the TPS53511 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot timer is set by the converter input voltage, V_{VIN}, and the output voltage, V_{VO}, to maintain a pseudo-fixed frequency over the output voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR-induced output ripple from D-CAP2™ mode control.

7.3.2 PWM Frequency and Adaptive On-Time Control

TPS53511 uses an adaptive on-time control scheme and does not have a dedicated on-board oscillator. The device runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on time is inversely proportional to the input voltage and proportional to the output voltage. The actual frequency can vary from 700 kHz depending on the off time, which is ended when the fed back portion of the output voltage falls to the VFB threshold voltage.

7.3.3 Soft Start and Pre-Biased Soft-Start Function

The soft-start time function is adjustable. When the EN pin becomes high, 2-µA current begins charging the capacitor, which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow-start time is shown in 方程式 1. The VFB voltage is 0.765 V and SS pin source current is 2 µA.

$$t_{SS(ms)} = \frac{C_{SS} \times V_{REF}}{I_{SS(\mu A)}} = \frac{C_{SS} \times 0.765}{2} \quad (1)$$

where

- C_{SS} is the value of the capacitor connected between the SS pin and GND.
- C_{SS} is expressed in nF.

This unique circuit prevents current from being pulled from the output during start-up if the output is pre-biased. When the soft start commands a voltage higher than the pre-bias level (internal soft-start voltage becomes greater than feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low-side FET gate driver pulses with a narrow on time. It then increments the on time on a cycle-by-cycle basis until it coincides with the time dictated by (1 – D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and makes sure the output voltage (the VO pin) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

7.3.4 Power Good

The power-good function is activated after soft start has finished. The power-good function becomes active after 1.7 times soft-start time. When the feedback voltage is within ±10% of the target value, internal comparators detect power good state and the power-good signal becomes high. The power-good output, PG, is an open-drain output. When the feedback voltage goes ±15% outside of the target value, the power-good signal becomes low after a 10-µs internal delay. During an undervoltage condition, when the feedback voltage returns to be within ±10% of the target value, the power-good signal goes HIGH again.

7.3.5 Output Discharge Control

The TPS53511 discharges the output when EN is low, or the controller is turned off by the protection function (OVP, UVP, UVLO, and thermal shutdown). The output is discharged by an internal 50-Ω MOSFET, which is connected from VO to PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

7.3.6 Current Protection

Output current is limited by cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller keeps the OFF state when the inductor current is larger than the over current trip level. To provide accuracy and a cost-effective solution, the device supports temperature compensated internal MOSFET $R_{DS(on)}$ sensing.

The inductor current is monitored by the voltage between the PGND pin and the SW pin. In an overcurrent condition, the current to the load exceeds the current to the output capacitor; thus, the output voltage tends to fall off. Eventually the output voltage becomes less than the undervoltage protection threshold and the device shuts down.

7.3.7 Overvoltage/Undervoltage Protection

The TPS53511 detects overvoltage and undervoltage conditions by monitoring the feedback voltage (the VFB pin). This function is enabled after approximately 1.7 times the soft-start time. When the feedback voltage becomes higher than 115% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET turns on. Normal operation can be restored only by cycling the VCC or EN pin voltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 µs, the

device latches off both internal high-side and low-side MOSFET. Similar to the overvoltage protection, the device is latched off, and normal operation can be restored only by cycling the VCC or EN pin voltage.

7.3.8 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the voltage of the V_{VREG5} pin. When the V_{VREG5} voltage is lower than UVLO threshold voltage, the TPS53511 is shut off. This protection is non-latching.

7.3.9 Thermal Shutdown

Thermal protection is self-activating. If the junction temperature exceeds the threshold value (typically 150°C), the TPS53511 shuts off. This protection is non-latching.

7.4 Device Functional Modes

7.4.1 Light Load Mode Control

The TPS53511 is designed with Auto-Skip mode to increase light-load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as is was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in 方程式 2.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The following example illustrates the design process and component selection for a single output synchronous buck converter using TPS53511. The schematic of a design example is shown in 图 8-1. The specification of the converter is listed in 表 8-1.

8.2 Typical Application

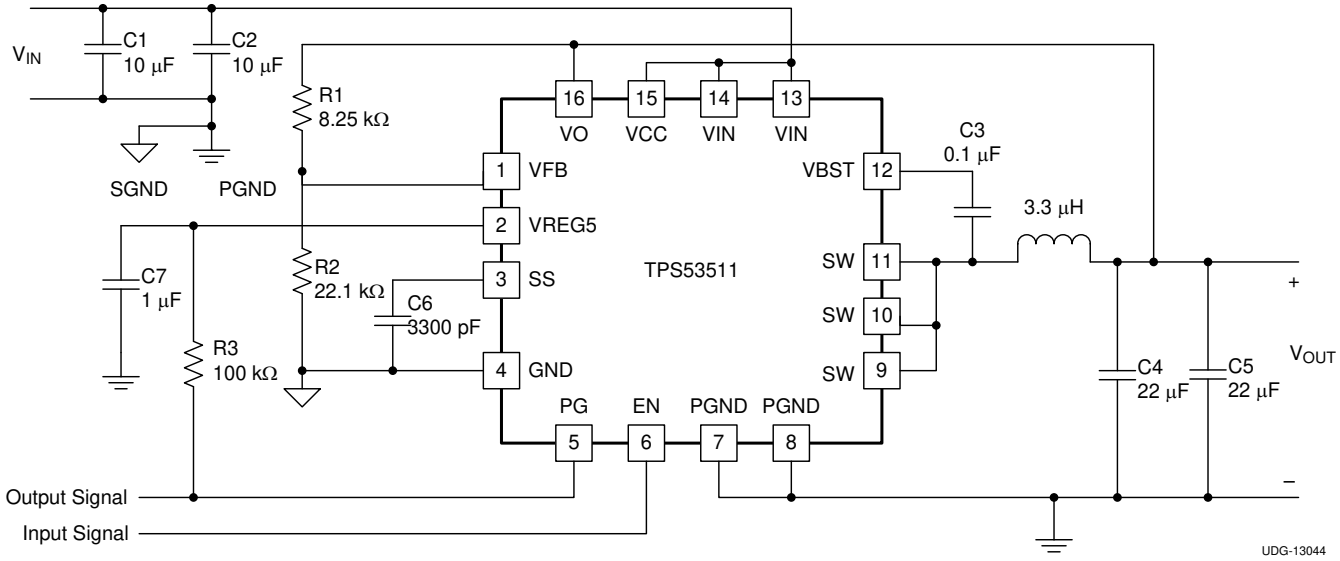


图 8-1. Typical 12-V Input Application Circuit

8.2.1 Design Requirements

表 8-1. Specification of the Single Output Synchronous Buck Converter

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5	12	18	V
V_{OUT}	Output voltage			1.05		V
V_{RIPPLE}	Output ripple	I_{OUT} = 1.5 A		3% of V_{OUT}		V
I_{OUT}	Output current			1.5		A
f_{SW}	Switching frequency			700		kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Inductor Selection

The value of the output filtering inductor determines the magnitude of the current ripple, which also affects the output voltage ripple for a certain output capacitance value. Increasing the inductance value reduces the ripple current, and thus, results in reduced conduction loss and output ripple voltage. Alternatively, low inductance value is needed due to the demand of low profile and fast transient response. Therefore, it is important to obtain a compromise between the low ripple current and low inductance value.

In practical application, the peak-to-peak current ripple is usually designed to be between 1/4 to1/2 of the rated load current. Since the magnitude of the current ripple is determined by inductance value, switching frequency, input voltage and output voltage, the required inductance value for a certain required ripple ΔI is shown in 方程式 3. Also, the chosen inductor should be rated for the peak current calculated from 方程式 4.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times I_{RIPPLE} \times f_{SW}} \tag{3}$$

$$I_{L(peak)} = I_{OUT} + \left(\frac{I_{RIPPLE}}{2} \right) \tag{4}$$

where

- V_{IN} is the input voltage.
- V_{OUT} is the output voltage.
- I_{RIPPLE} is the required current ripple.
- f_{SW} is the switching frequency.

For this design example, the inductance value is selected to provide approximately 30% peak-to-peak ripple current at maximum load. For this design, a nearest standard value was chosen: 3.3 µH. For 3.3 µH, the calculated peak current is 1.71 A.

8.2.2.2 Output Capacitor Selection

The capacitor value and ESR determines the amount of output voltage ripple. It is recommended to use a ceramic output capacitor. Using 方程式 5 to 方程式 6, an initial estimate for the capacitor value and ESR can be calculated. As the load transients are significant, consider using the load step instead of ripple current to calculate the maximum ESR.

$$C > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{RIPPLE}}{I_{RIPPLE}} - ESR} \tag{5}$$

$$ESR < \frac{V_{OUT(ripple)}}{I_{RIPPLE}} \tag{6}$$

For this design, the minimum required capacitance is 8.45 µF and maximum ESR is 33 mΩ. Therefore, two TDK C3216JB0J226M 22-µF output capacitors are used. The maximum ESR is 12 mΩ for each capacitor.

8.2.2.3 Input Capacitor Selection

The device requires an input decoupling capacitor and a bulk capacitor. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. The capacitor voltage rating must to be greater than the maximum input voltage. In case of separate V_{VCC} and V_{VIN}, a ceramic capacitor over 10 µF is recommended for the input voltage. Placing a ceramic capacitor with a value higher than 0.1 µF for the VCC is recommended also.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF capacitor must be connected between the VBST and SW pin for proper operation. A ceramic capacitor is recommended.

8.2.2.5 VREG5 Capacitor Selection

A 1-µF capacitor must be connected between the VREG5 and SW pin for proper operation. A ceramic capacitor is recommended.

8.2.2.6 Output Voltage Setting Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Begin by using 方程式 7 and 方程式 8 to calculate V_{OUT}.

To improve efficiency at light-load condition, use resistors with a relatively larger value. However, too high resistance value make the circuit more susceptible to noise, and voltage errors from the VFB input current is more noticeable.

For output voltages from 0.76 V to 2.5 V:

$$V_{OUT} = 0.765 \times \left(1 + \left(\frac{R1}{R2}\right)\right) \tag{7}$$

For output voltages over 2.5 V:

$$V_{OUT} = \left(0.763 + 0.0017 \times V_{OUT}\right) \times \left(1 + \frac{R1}{R2}\right) \tag{8}$$

The required output voltage for this design is 1.05 V. So 方程式 7 is used to calculate the value of R1. R2 is 22.1 kΩ, therefore, R1 is 8.25 kΩ.

8.2.3 Application Curves

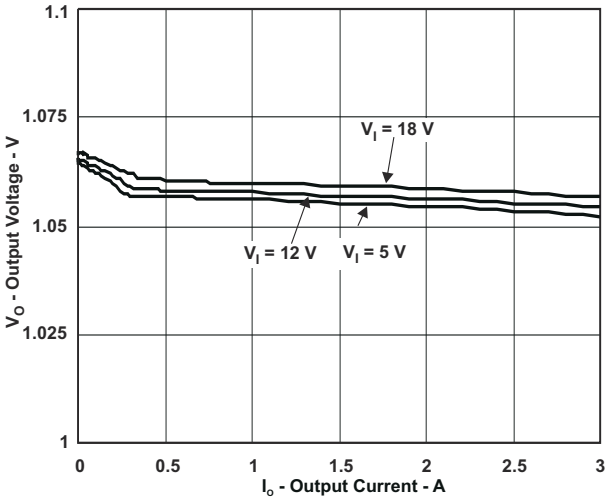


图 8-2. 1.05-V Output Voltage vs. Output Current

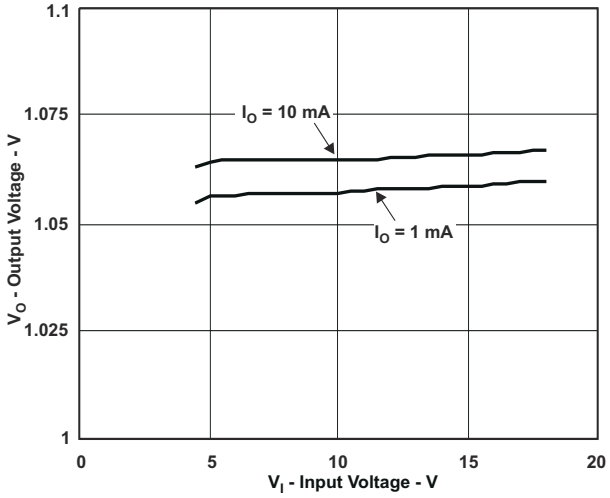


图 8-3. 1.05-V Output Voltage vs. Input Voltage

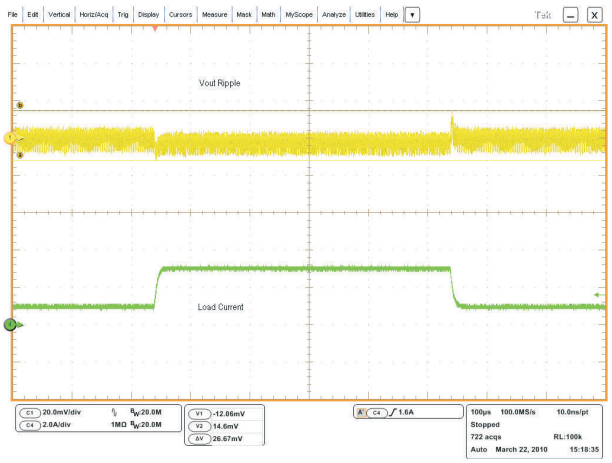


图 8-4. 1.05-V, 0-A to 3-A Load Transient Response

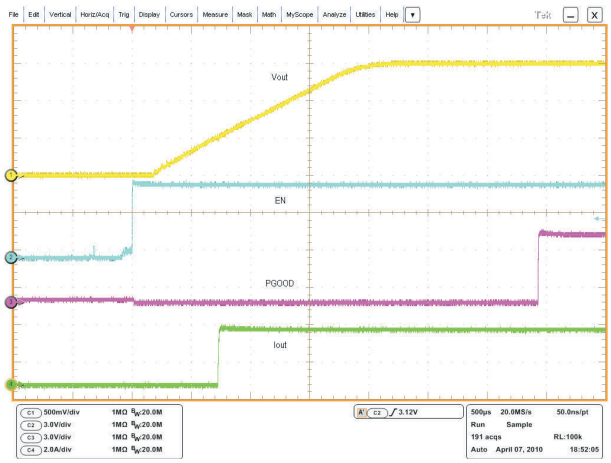


图 8-5. Start-Up

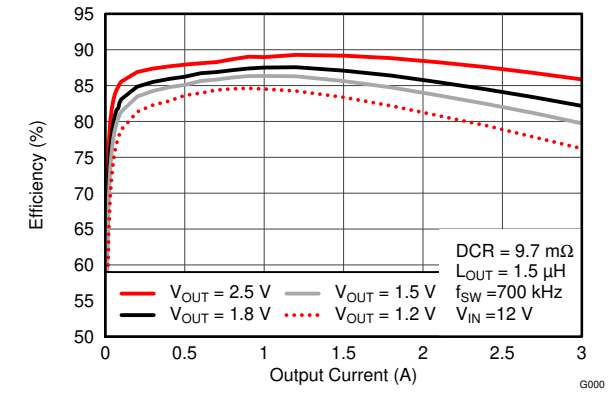


图 8-6. Efficiency vs. Output Current

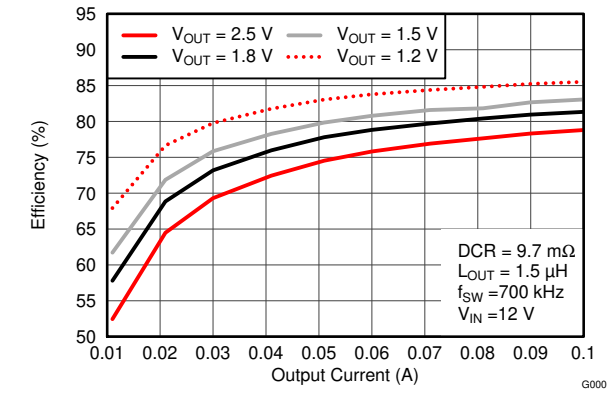


图 8-7. Light-Load Efficiency vs. Output Current

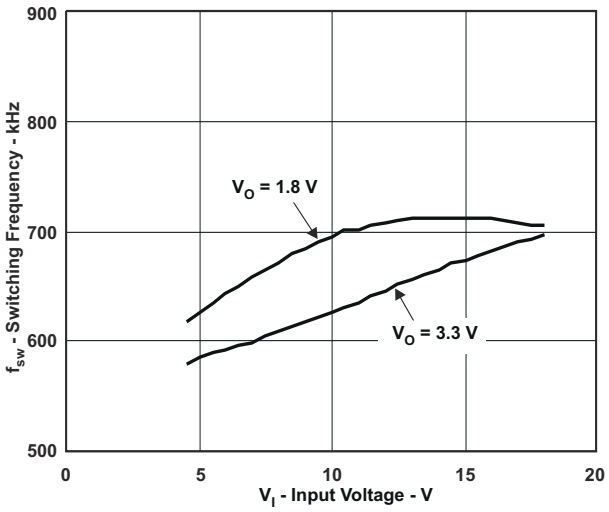


图 8-8. Switching Frequency vs. Input Voltage

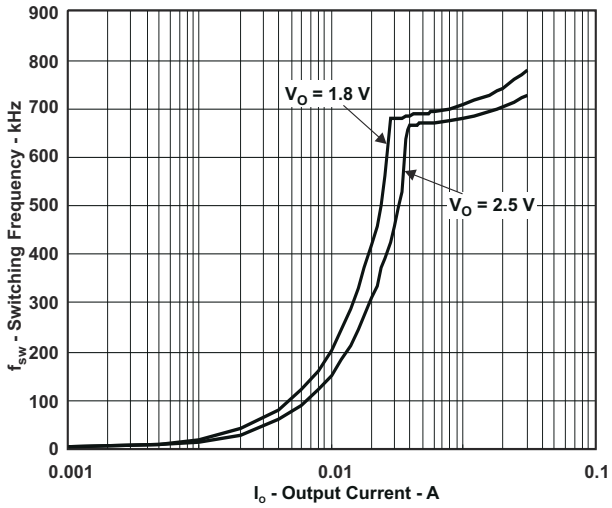


图 8-9. Switching Frequency vs. Output Current

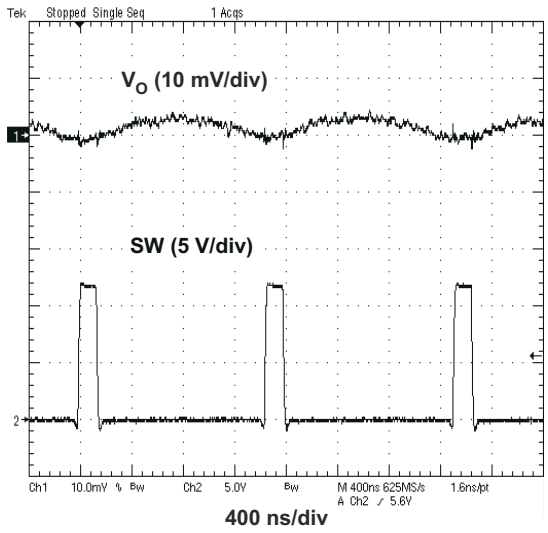


图 8-10. Output Voltage Ripple

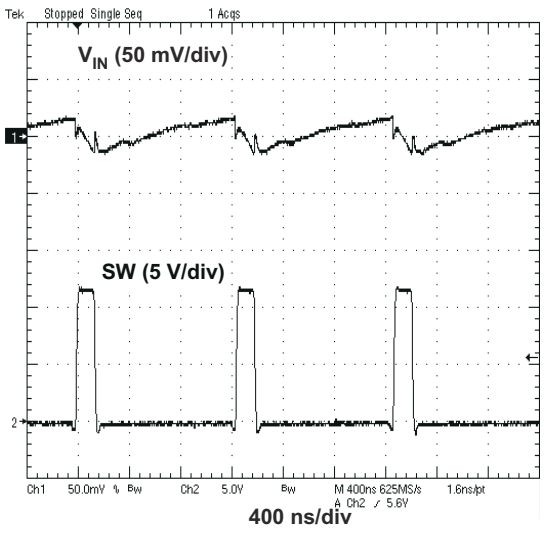


图 8-11. Input Voltage Ripple

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4.5 V and 18 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS53311 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μF is a typical choice.

10 Layout

10.1 Layout Considerations

- Keep the input switching current loop as small as possible.
- Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection between the signal and power grounds.
- Do not allow switching current to flow under the device.
- Keep the pattern lines for VIN and PGND broad.
- Exposed pad of the device must be connected to PGND with solder.
- VREG5 capacitor should be connected to a broad pattern of the PGND.
- Output capacitor should be connected to a broad pattern of the PGND.
- Voltage feedback loop should be as short as possible, and preferably with ground shield.
- Lower resistor of the voltage divider, which is connected to the VFB pin should be tied to SGND.
- Providing sufficient via is preferable for VIN, SW and PGND connection.
- PCB pattern for VIN, SW, and PGND should be as broad as possible.
- If VIN and VCC are shorted, VIN and VCC patterns need to be connected with broad pattern lines.
- VIN capacitor should be placed as close as possible to the device.

10.1.1 Thermal Information

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be connected to an external heat sink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heat sink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heat sink structure designed into the PCB. This design optimizes the heat transfer from the device.

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to the *PowerPAD™ Thermally Enhanced Package Technical Brief* and the *PowerPAD™ Made Easy Application Brief*.

10.2 Layout Example

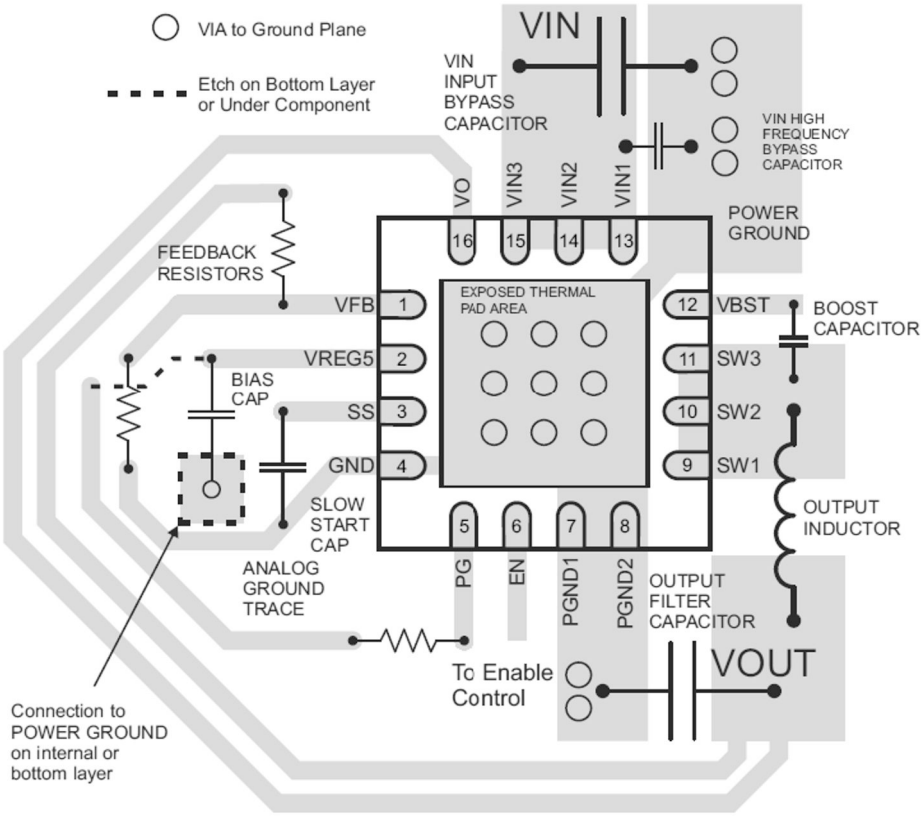


图 10-1. Layout Example

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Device Support

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

DCAP2™ is a trademark of TI.
PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com/legal/termsofsale.html) 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53511RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	53511	Samples
TPS53511RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	53511	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

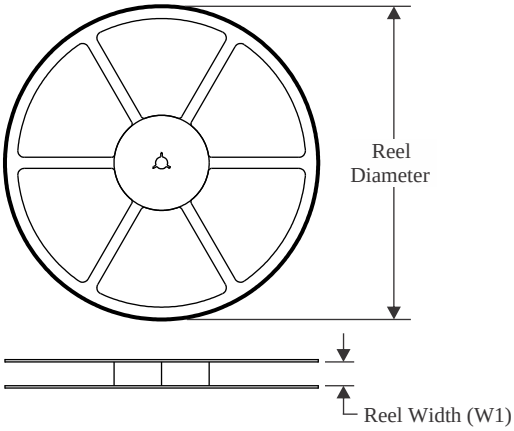
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

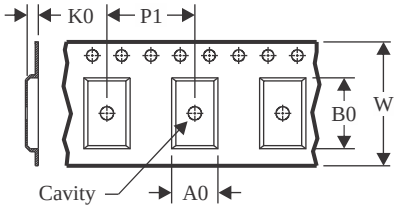
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

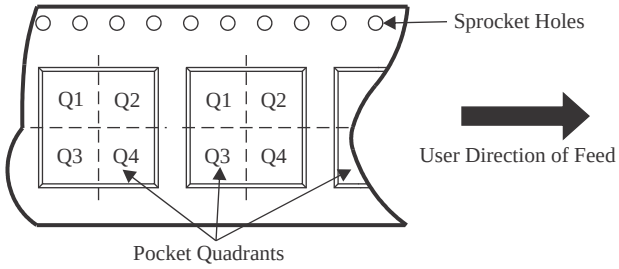


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

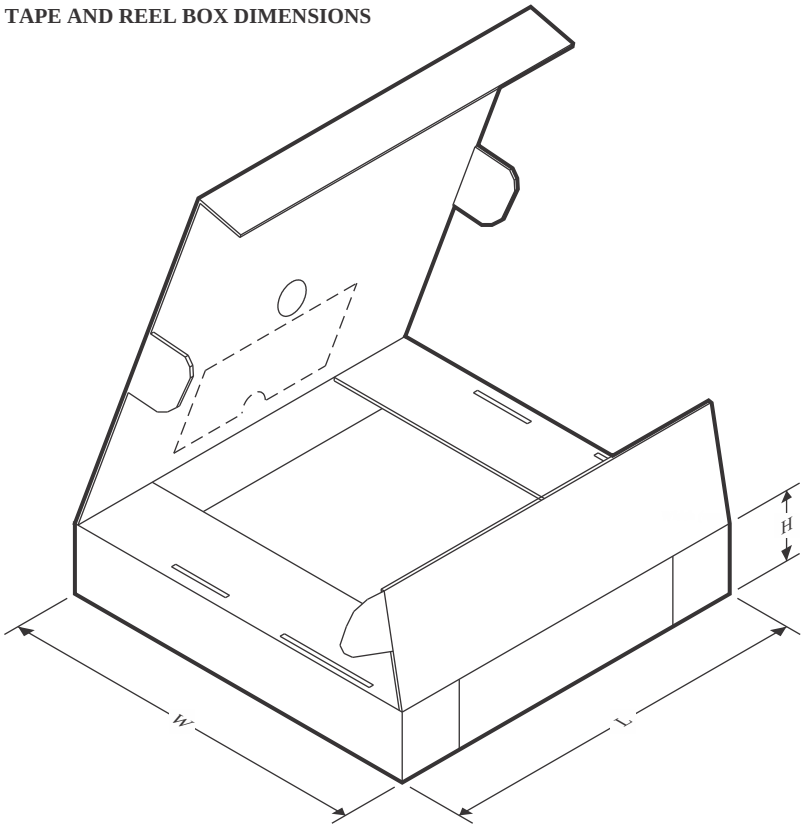
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53511RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53511RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

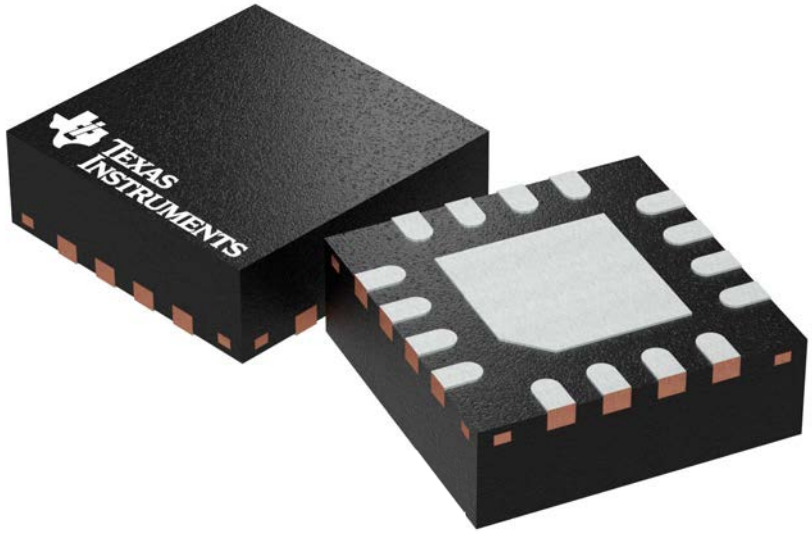


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53511RGTR	VQFN	RGT	16	3000	335.0	335.0	25.0
TPS53511RGTT	VQFN	RGT	16	250	182.0	182.0	20.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



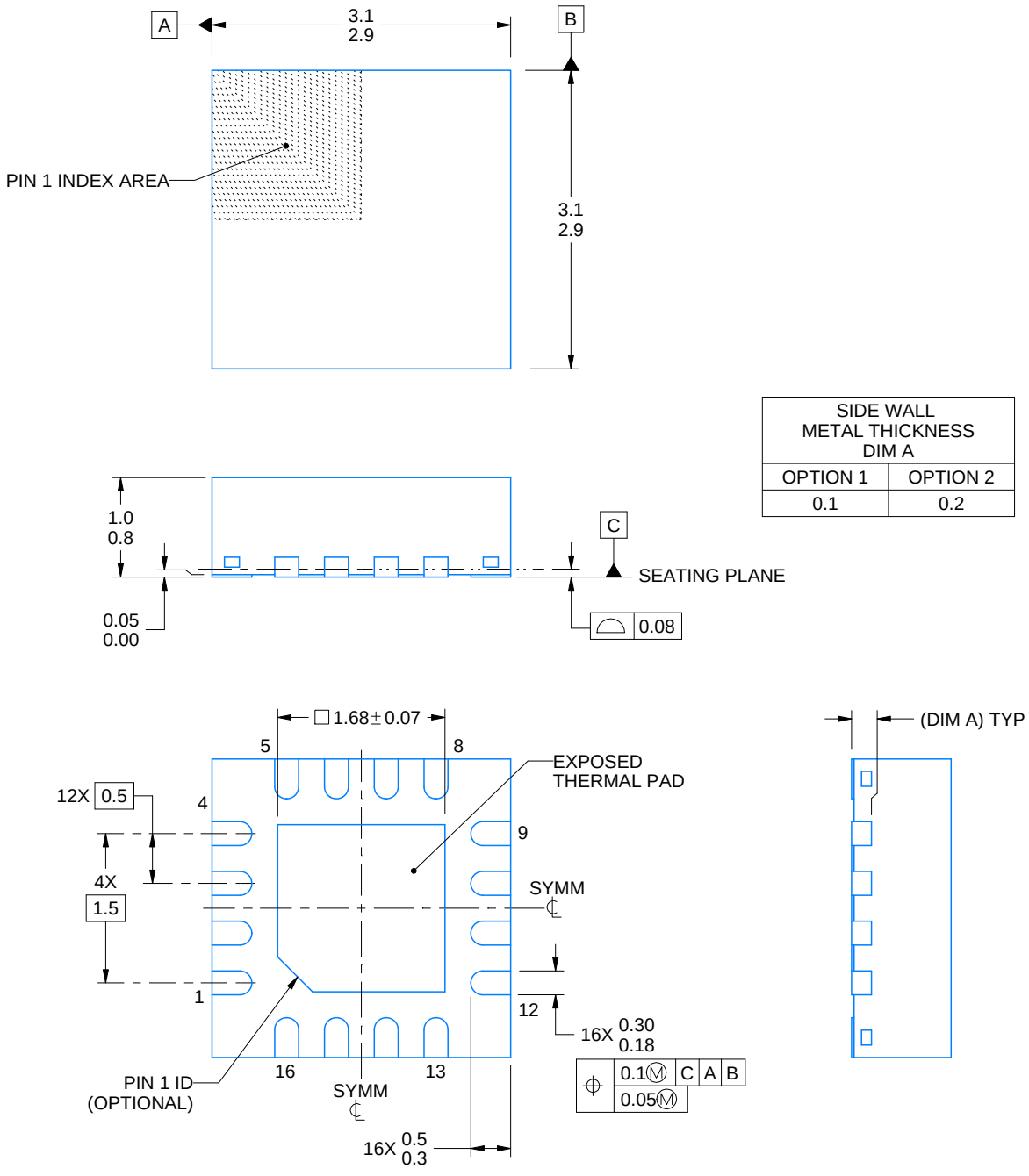
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

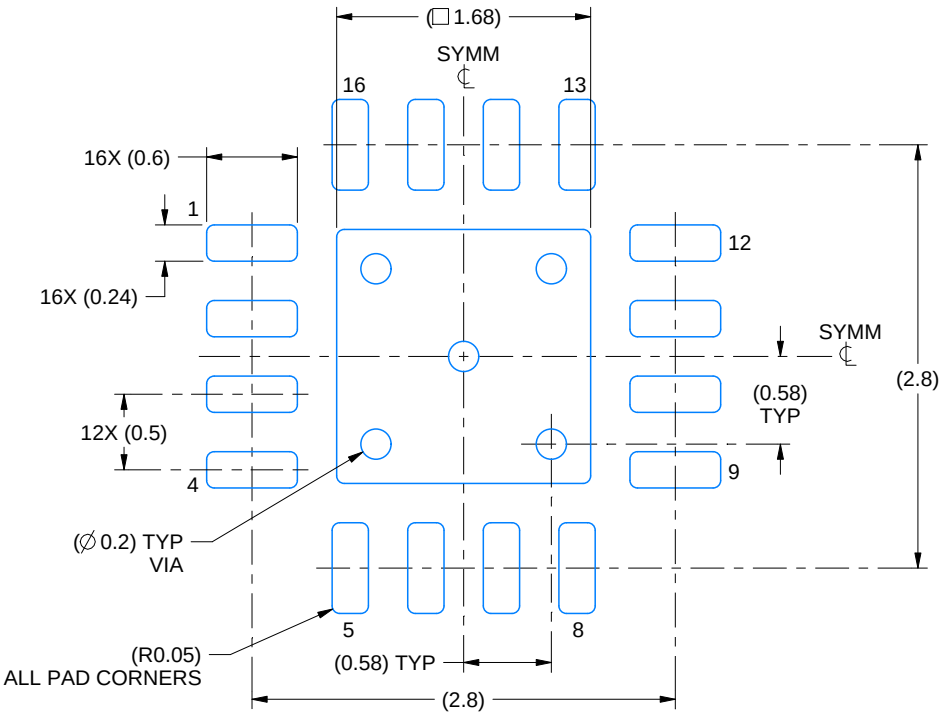
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

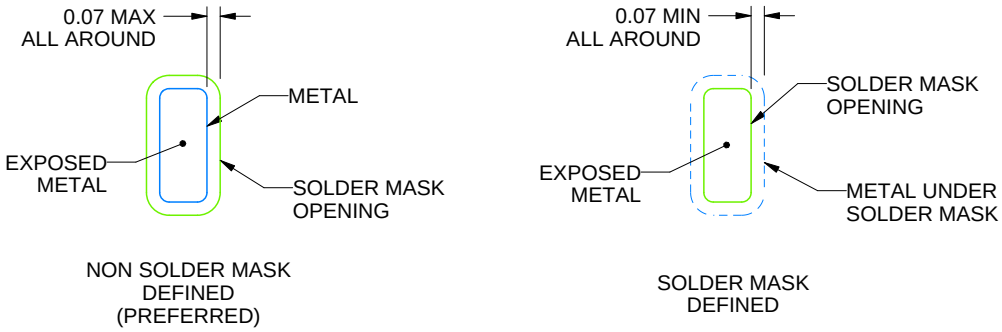


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

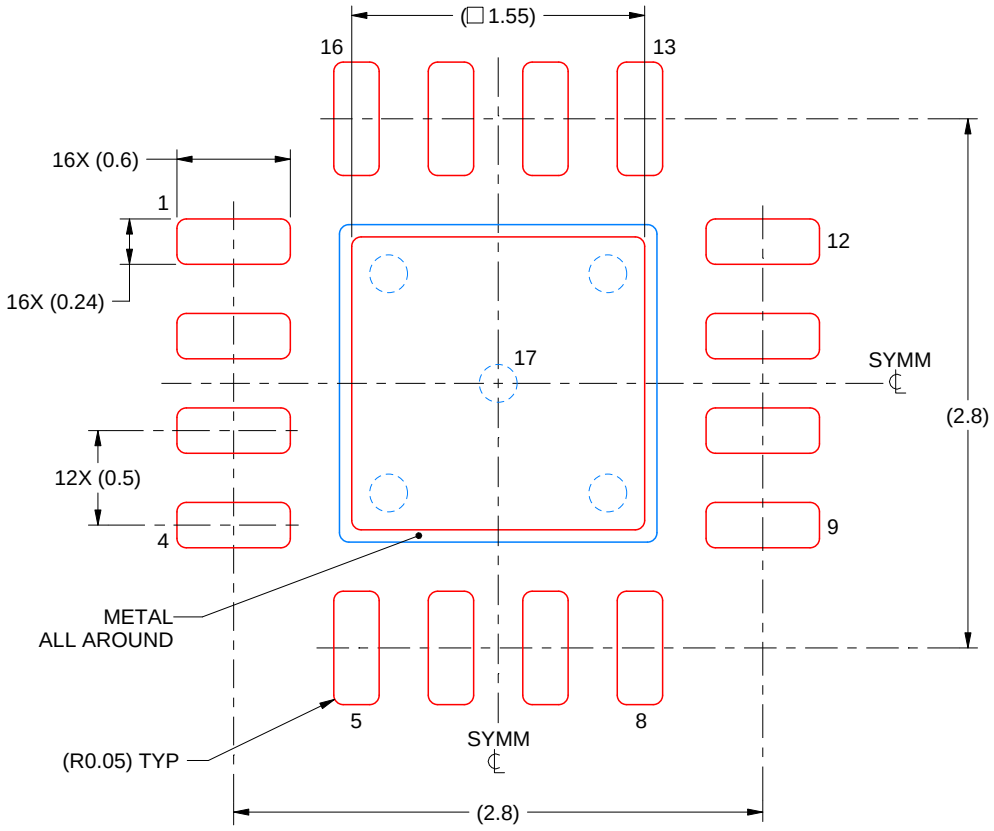


SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265