

具有集成开关的 TPS53316 高效 5A 降压稳压器

1 特性

- 最大效率96%
- 持续5A输出电流能力
- 支持所有片式多层陶瓷(MLCC)输出电容器
- SmoothPWM™自动跳跃 Eco-Mode™, 用于提高轻负载效率
- 电压模式控制
- 单电源轨出入
- 可选频率
- 可选过电流保护(OCP)阈值
- 可选软启动时间
- 2.9V 至 6V 输入电压范围
- 可调节输出电压范围从0.6V到最高 $0.8 \times V_{IN}$
- 禁用期间软停止输出放电
- 过流、过压和过热保护
- 漏极开路电源良好指示
- 内部自举电路开关
- 支持预偏置启动功能
- 小型 3mm × 3mm、16 引脚、QFN 封装
- 低 $R_{DS(on)}$ (对于 3.3V 输入为 22mΩ, 对于 5V 输入为 18mΩ)

2 应用

- 用于 5V 降压 电压轨的 低电压应用
- 用于 3.3V 降压 电压轨的 低电压应用

3 说明

TPS53316 器件在 200mm² 的 PCB 面积内总共使用 16 个组件来提供全集成的 3.3V 或 5V 输入同步降压转换器。由于低 $R_{DS(on)}$ 和 TI 专有 SmoothPWM 跳跃运行模式, 它可以实现 96% 的峰值效率, 并且在负载低至 100mA 时实现 90% 以上的效率。它只需要 2 个 22μF 陶瓷输出电容器即可实现电源密集型 5A 解决方案。

TPS53316 提供 750kHz、1.1MHz 和 2MHz 开关频率选项, 预偏置启动, 可选内部软启动, 输出软放电, 内部 VBST 开关, 电源正常, EN/输入 UVLO, 过流, 过压, 欠压和过热保护以及所有陶瓷输出电容器支持。它支持 2.9V 至 6V 范围

内的输入电压, 无需额外的偏置电压。输出电压可调, 范围为 0.6V 至

$0.8 \times V_{IN}$ 。

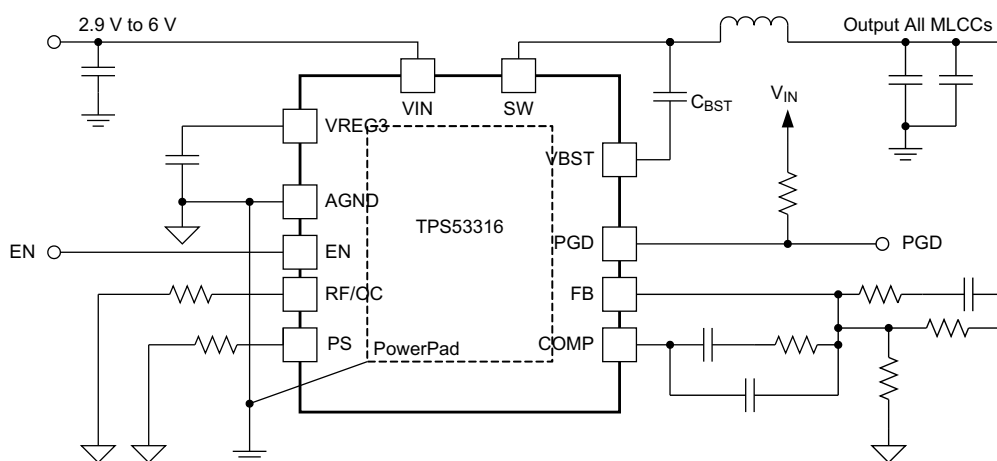
TPS53316 采用 3mm × 3mm、16 引脚、QFN 封装 (绿色环保, 符合 RoHS 标准并且无铅), 额定工作温度范围为 -40°C 至 85°C。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS53316	四方扁平无引线 (QFN) (16)	3.00mm × 3.00mm

(1) 要了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

典型应用电路



UDG-11233

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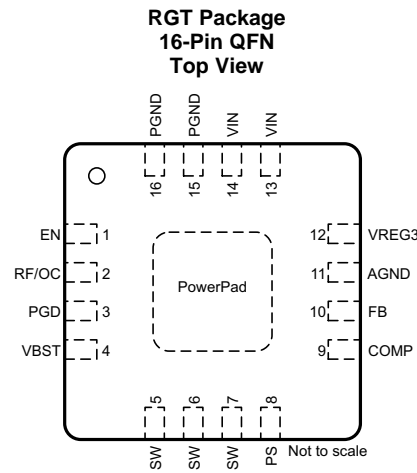
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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (December 2011) to Revision A	Page
• 已添加 ESD 额定值表，特性 说明部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分	1
• 已删除 订购信息表；请参见数据表末尾的 POA	1
• Deleted Lead temperature, 1.6 mm (1/16 inch) from case for 10 seconds: 300°C maximum	4
• Changed R8 value in the Typical 3.3-V Input Application Circuit Diagram From: 5.76 kΩ To: 57.6 kW	18

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	EN	I	Enable pin. Internally pulled-up to the VIN pin through a 2-M Ω resistor. The EN voltage must be less than ($V_{IN} + 0.5$ V).
2	RF/OC	I	Switching frequency and OC level configuration pin: Connecting to ground: 1.1 MHz, 6.5-A OCP Pulled high or floating (internal pulled high): 1.1 MHz, 4.5-A OCP Connect with 24.3 k Ω to GND: 750 kHz, 4.5-A OCP Connect with 57.6 k Ω to GND: 750 kHz, 6.5-A OCP Connect with 105 k Ω to GND: 2 MHz, 4.5-A OCP Connect with 174 k Ω to GND: 2 MHz, 6.5-A OCP
3	PGD	O	Power good output flag. Open-drain output. Pull up to an external rail through a resistor.
4	VBST	P	Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal.
5	SW	B	Output inductor connection to integrated power devices
6	SW	B	Output inductor connection to integrated power devices
7	SW	B	Output inductor connection to integrated power devices
8	PS	I	Mode configuration pin (with 10- μ A current): Connecting to ground: Forced CCM with 4x softstart time Pulled high or floating (internal pulled high): Forced CCM master Connect with 24.3 k Ω to GND: HEF mode with 4x softstart time Connect with 57.6 k Ω to GND: HEFF mode Connect with 105 k Ω to GND: DE mode Connect with 174 k Ω to GND: DE mode with 4x softstart time
9	COMP	O	Error amplifier compensation terminal. Type III compensation method is generally recommended for stability.
10	FB	I	Voltage feedback pin. Use for OVP, UVP, and PGD determination.
11	AGND	G	Device analog ground terminal
12	VREG3	O	3.3-V LDO output, serves as supply voltage for internal analog circuitry. The EN pin controls the turnon function of the LDO.
13	VIN	P	Gate driver supply and power conversion input voltage. The input range is from 2.9 V to 6 V.
14	VIN	P	Gate driver supply and power conversion input voltage. The input range is from 2.9 V to 6 V.
15	PGND	P	Device power ground terminal
16	PGND	P	Device power ground terminal
—	PowerPad	—	Thermal pad of the device. Use 4 or 5 vias to connect to GND plane for heat dissipation.

(1) B = Bidirectional, G = Ground, I = Input, O = Output, P = Supply

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
Input voltage	VIN	-0.3	7	V	
	VBST	-0.3	17		
	VBST (with respect to LL)	-0.3	7		
	EN	-0.3	7		
	FB, PS, RF/OC	-0.3	3.7		
Output voltage	SW	DC	-1	7	V
		Pulse < 20 ns, E = 5 μJ	≥-5	<10	
	PGD	-0.3	7		
	COMP, VREG3	-0.3	3.7		
	PGND	-0.3	0.3		
Junction temperature, T _J		-40	150	°C	
Operating open-air temperature, T _A		-40	85	°C	
Storage temperature, T _{stg}		-55	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Input voltage	VIN (main supply)	2.9	6	V
	VBST	-0.1	13.5	
	VBST (with respect to SW)	-0.1	6	
	EN,	-0.1	6	
	FB, PS, RF/OC	-0.1	3.5	
Output voltage	SW	-1	6.5	V
	PGD	-0.1	6	
	COMP, VREG3	-0.1	3.5	
	PGND	-0.1	0.1	
T _J Junction temperature	-40	125	°C	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS53316	UNIT
		RGT (QFN)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	45.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	54.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	18.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	18.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{IN} = 3.3 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: VOLTAGE, CURRENTS, AND UVLO						
V _{VIN}	VIN supply voltage	Nominal input voltage range	2.9		6	V
I _{VIN(sdn)}	VIN shutdown current	EN = LO			15	μA
I _{VIN}	VIN supply current	EN = HI, V _{FB} = 0.63 V, No load		2	3.5	mA
V _{UVLO}	VIN UVLO threshold	Ramp up, EN = HI		2.8		V
V _{UVLO(hys)}	VIN UVLO hysteresis	VIN UVLO hysteresis		120		mV
V _{REG3}	LDO output	V _{VIN} = 5 V, 0 ≤ I _{DD} ≤ 5 mA	3.135	3.3	3.465	V
VOLTAGE FEEDBACK LOOP: VREF AND ERROR AMPLIFIER						
V _{VREF}	VREF	Internal precision reference voltage		0.6		V
TOL _{VREF}	VREF tolerance	0°C ≤ T _A ≤ 85°C	-1%		1%	
		-40°C ≤ T _A ≤ 85°C	-1.25%		1.25%	
UGBW ⁽¹⁾	Unity gain bandwidth		14			MHz
A _{OL} ⁽¹⁾	Open-loop gain		80			dB
I _{FBINT}	FB input leakage current	Sourced from FB pin			30	nA
I _{EA(max)} ⁽¹⁾	Output sinking and sourcing current	C _{COMP} = 20 pF		5		mA
SR ⁽¹⁾	Slew rate			5		V/μs
OCP: OVERCURRENT AND ZERO CROSSING						
I _{OCP3A} ⁽²⁾	Overcurrent limit on high-side FET	4.5-A setting, when I _{OUT} exceeds this threshold for 4 consecutive cycles, V _{VIN} = 3.3 V, V _{OUT} = 1.5 V with 1-μH inductor, f _{SW} = 1.1 MHz, T _A = 25°C	4.05	4.5	4.95	A
I _{OCP3A} ⁽²⁾	One-time overcurrent latch off on the low-side FET	4.5-A setting, immediate shuts down when sensed current reach this value V _{VIN} = 3.3 V, V _{OUT} = 0.6 V with 1-μH inductor, f _{SW} = 1.1 MHz, T _A = 25°C	4.49	5.1	5.61	A
I _{OCP5A} ⁽²⁾	Overcurrent limit on high-side FET	6.5-A setting, when I _{OUT} exceeds this threshold for 4 consecutive cycles, V _{VIN} = 3.3 V, V _{OUT} = 1.5 V with 1-μH inductor, f _{SW} = 1.1 MHz, T _A = 25°C	6.1	6.8	7.5	A
I _{OCP5A} ⁽²⁾	One time overcurrent latch off on the low-side FET	6.5-A setting, immediate shut down when sensed current reaches this value V _{VIN} = 3.3 V, V _{OUT} = 0.6 V with 1-μH inductor, f _{SW} = 1.1 MHz, T _A = 25°C	6.75	7.5	8.3	A
t _{hiccup}	Hiccup time interval	f _{SW} = 1.1 MHz		14.5		ms
V _{ZXOFF} ⁽¹⁾	Zero crossing comparator internal offset	PGND – SW, SKIP mode	-4.5	-3	-1.5	mV

(1) Ensured by design. Not production tested.

(2) See [Figure 5](#) and [Figure 6](#) on OCP level for other operating conditions.

Electrical Characteristics (continued)

 over operating free-air temperature range, $V_{IN} = 3.3\text{ V}$, $PGND = GND$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION: OVP, UVP, PGD, AND INTERNAL THERMAL SHUTDOWN						
V_{OVP}	Overvoltage protection threshold voltage	Measured at the FB w/r/t VREF	114%	117%	120%	
V_{UVP}	Undervoltage protection Threshold voltage	Measured at the FB w/r/t VREF	80%	83%	86%	
V_{PGDL}	PGD low threshold	Measured at the FB w/r/t VREF	80%	83%	86%	
V_{PGDU}	PGD upper threshold	Measured at the FB w/r/t VREF	114%	117%	120%	
$V_{INMINPG}$	Minimum input voltage for valid PGD at start-up	Measured at V_{IN} with 1-mA sink current on PGD pin at start-up		1		V
$THSD^{(1)}$	Thermal shutdown		130	140	150	°C
$THSD_{HYS}^{(1)}$	Thermal shutdown hysteresis	Controller start again after temperature has dropped		40		°C
LOGIC PINS: I/O VOLTAGE AND CURRENT						
V_{PGPD}	PGD pull-down voltage	Pulldown voltage with 4-mA sink current		0.1	0.3	V
I_{PGLK}	PGD leakage current	Hi-Z leakage current, Apply 3.3 V in off state	-2	0	2	μA
R_{ENPU}	Enable pullup resistor			2.25		MΩ
V_{ENH}	EN logic high	$V_{VIN} = 3.3\text{ V}$	0.82	0.97	1.1	V
		$V_{VIN} = 5\text{ V}$	0.95	1.1	1.25	V
V_{ENHYS}	EN hysteresis	$V_{VIN} = 3.3\text{ V}$		0.16	0.24	V
		$V_{VIN} = 5\text{ V}$		0.2	0.275	V
PS_{THS}	PS mode threshold voltage	Level 1 to level 2 ⁽³⁾		0.12		V
		Level 2 to level 3		0.4		
		Level 3 to level 4		0.8		
		Level 4 to level 5		1.4		
		Level 5 to level 6		2.2		
I_{PS}	PS source	10-μA pull-up current when enabled	8	10	12	μA
RF/OC_{THS}	RF/OC pin threshold voltage	Level 1 to level 2 ⁽⁴⁾		0.12		V
		Level 2 to level 3		0.4		
		Level 3 to level 4		0.8		
		Level 4 to level 5		1.4		
		Level 5 to level 6		2.2		
$I_{RF/OC}$	RF/OC source current	10-μA pullup current when enabled	8	10	12	μA
BOOT STRAP: VOLTAGE AND LEAKAGE CURRENT						
I_{VBSTLK}	VBST leakage current	$V_{VIN} = 3.3\text{ V}$, $V_{VBST} = 6.6\text{ V}$, $T_A = 25^\circ\text{C}$			1	μA
TIMERS: SS, FREQUENCY, RAMP, ON-TIME AND I/O TIMING						
t_{SS_1}	Delay after EN Asserting	EN = 'HI'		0.2		ms
t_{SS_2}	Soft-start ramp_up time	$0\text{ V} \leq V_{SS} \leq 0.6\text{ V}$		0.4		ms
		$0\text{ V} \leq V_{SS} \leq 0.6\text{ V}$, 4 x SS time (option2)		1.6		
$t_{PGDENDLY}$	PGD start-up delay time	$V_{SS} = 0.6\text{ V}$ to PGD (SSOK) going high		0.3		ms
		$V_{SS} = 0.6\text{ V}$ to PGD (SSOK), option 2		1.2		
t_{OVPDLY}	OVP delay time	Time from FB out of +20% of VREF to OVP fault	1	1.7	2.5	μs
t_{UVPDLY}	UVP delay time	Time from FB out of -20% of VREF to UVP fault		10		μs
f_{SW}	Switching frequency	All modes, $f_{SET} = 0.75\text{ MHz}$	0.653	0.725	0.798	MHz
		All modes, $f_{SET} = 1.1\text{ MHz}$	0.99	1.1	1.21	
		FCCM and DE mode, $f_{SET} = 2\text{ MHz}$	1.71	1.9	2.09	
		HEF mode, $f_{SET} = 2\text{ MHz}$	1.566	1.8	2.034	

(3) See PS pin description for levels.

(4) See RF/OC pin description for levels.

Electrical Characteristics (continued)

 over operating free-air temperature range, $V_{IN} = 3.3\text{ V}$, $PGND = GND$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Ramp amplitude ⁽¹⁾	$2.9\text{ V} \leq V_{VIN} \leq 6\text{ V}$		$V_{VIN}/4$		V
$t_{MIN(off)}$	Minimum OFF time, FCCM and DE	All frequencies		90	130	ns
	Minimum OFF time, HEF	$f_{SW} = 1.1\text{ MHz}$		160	240	ns
D_{MAX}	Maximum duty cycle, FCCM and DE	$f_{SW} = 1.1\text{ MHz}$	84%	89%		
D_{MAX}	Maximum duty cycle, HEF	All frequencies	75%	81%		
R_{SFTSTP}	Soft-discharge transistor resistance	$EN = LO$, $V_{VIN} = 3.3\text{ V}$, $V_{OUT} = 0.5\text{ V}$		60		Ω

6.6 Typical Characteristics

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

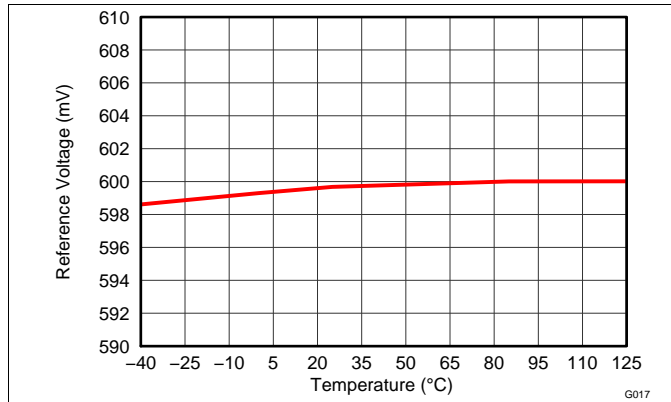


Figure 1. Reference Voltage vs Temperature

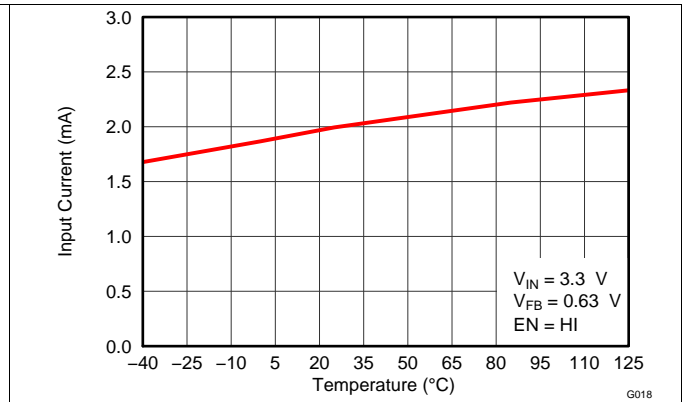


Figure 2. Input Current vs Temperature

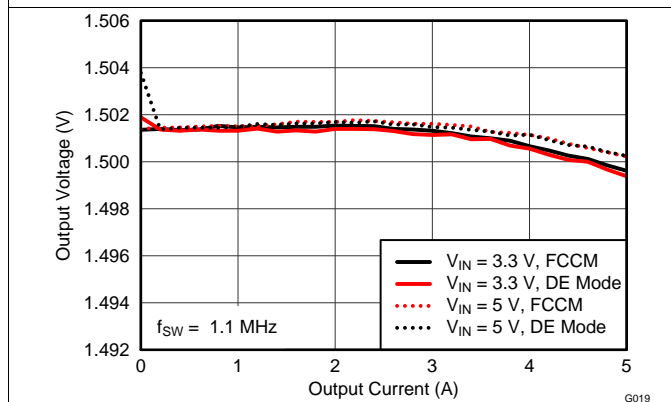


Figure 3. Output Voltage vs Output Current

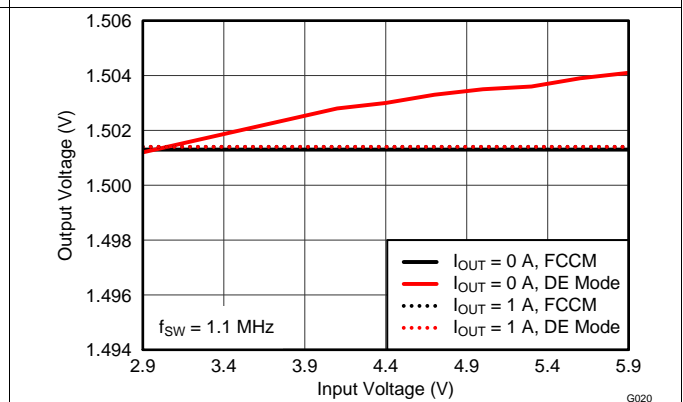


Figure 4. Output Voltage vs Input Voltage

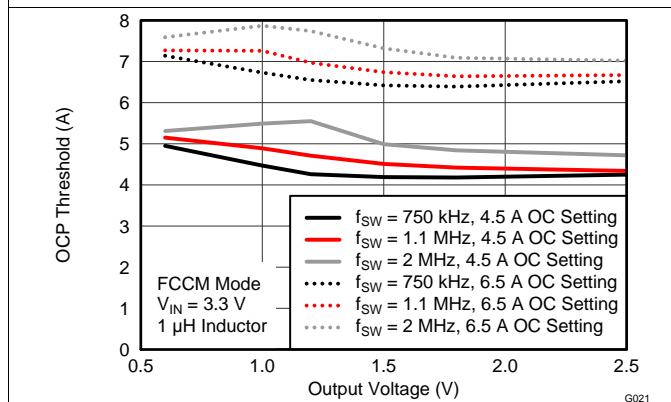


Figure 5. OCP Threshold vs Output Voltage

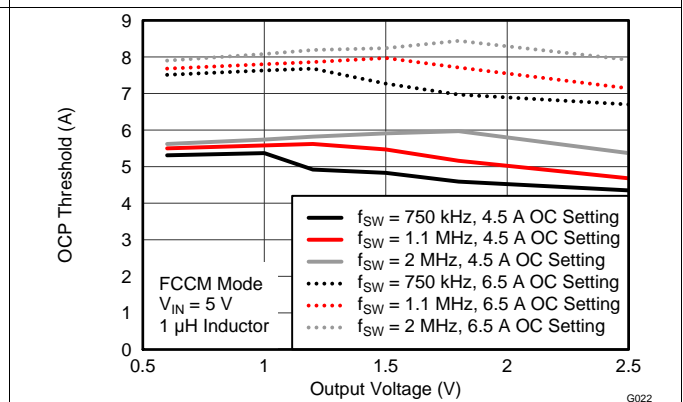
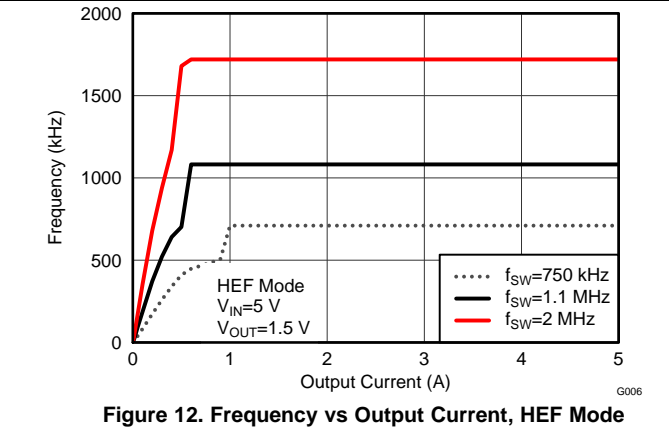
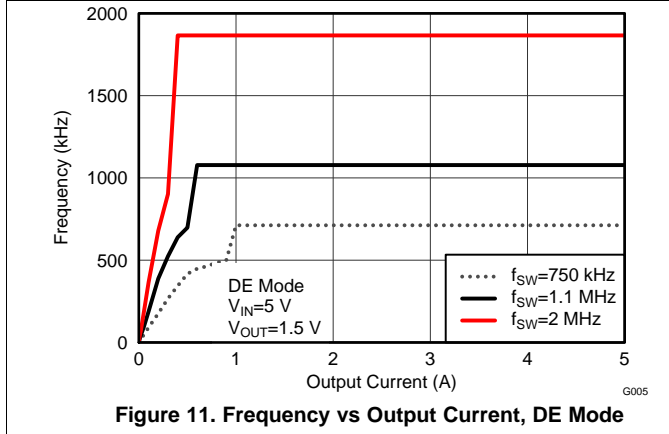
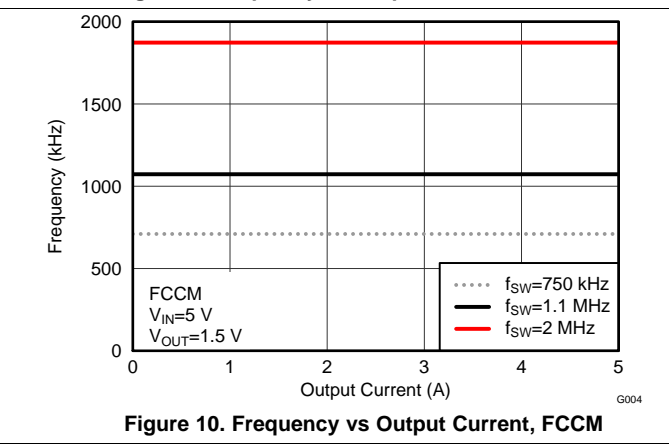
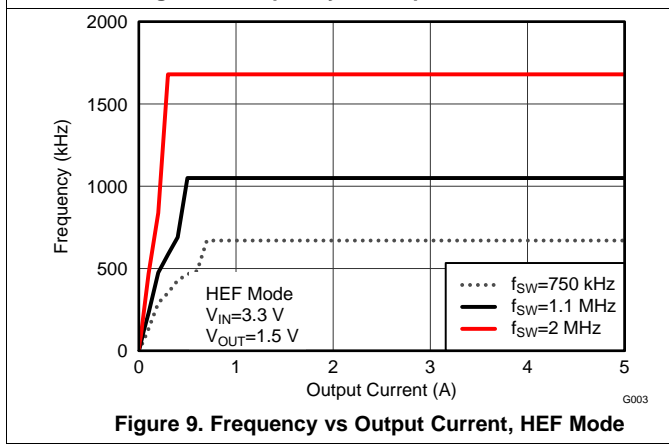
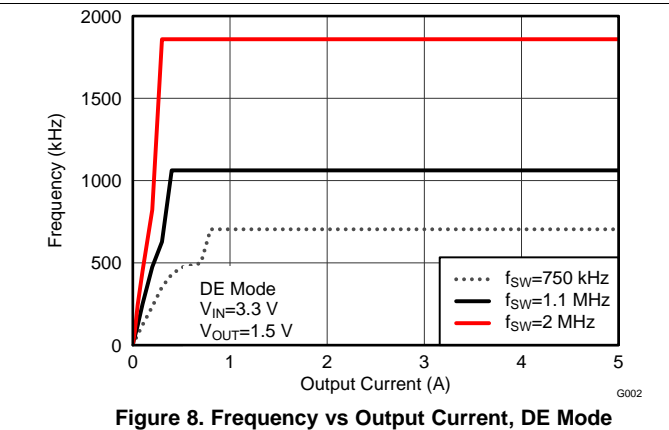
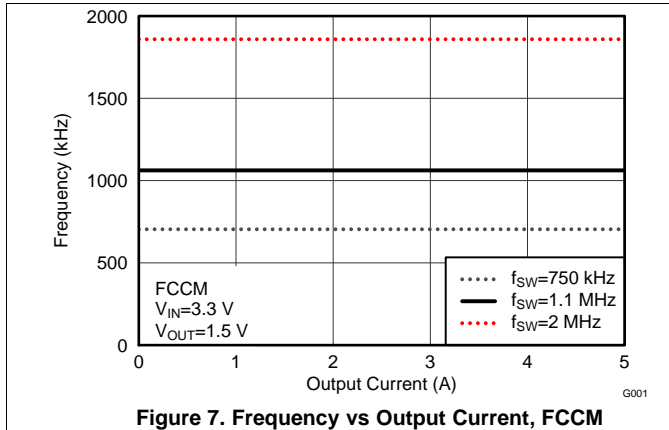


Figure 6. OCP Threshold vs Output Voltage

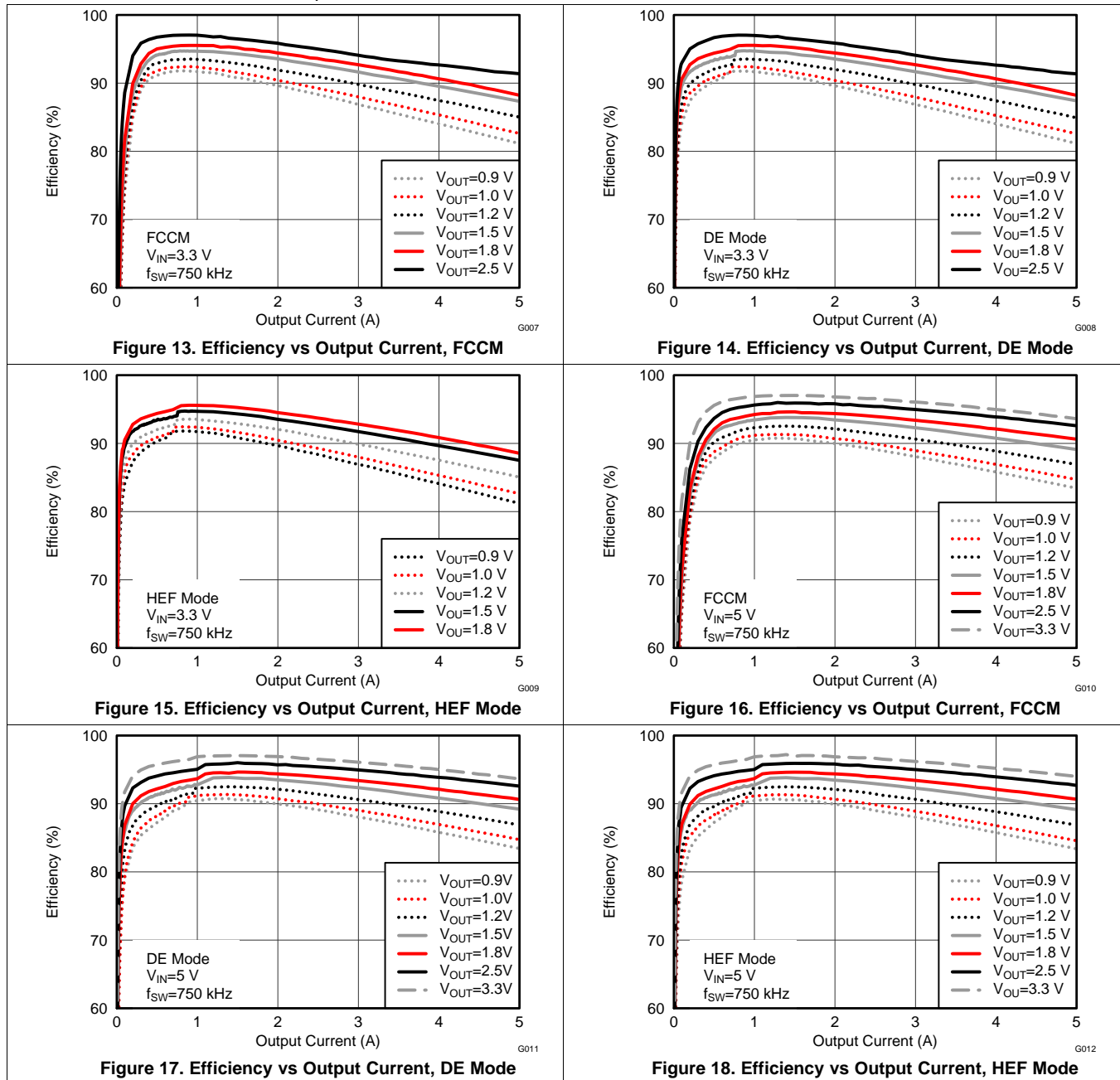
Typical Characteristics (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω



Typical Characteristics (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω



Typical Characteristics (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

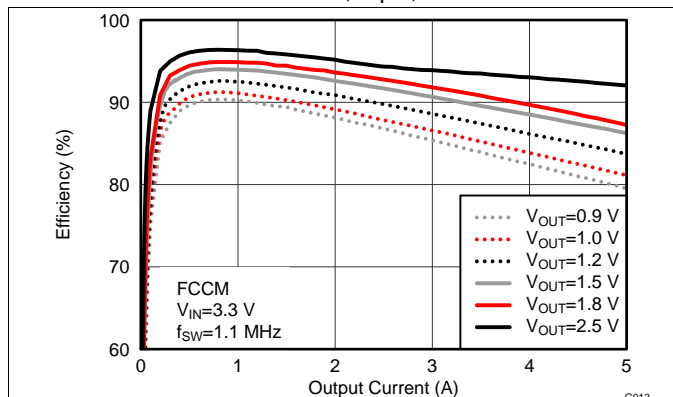


Figure 19. Efficiency vs Output Current, FCCM

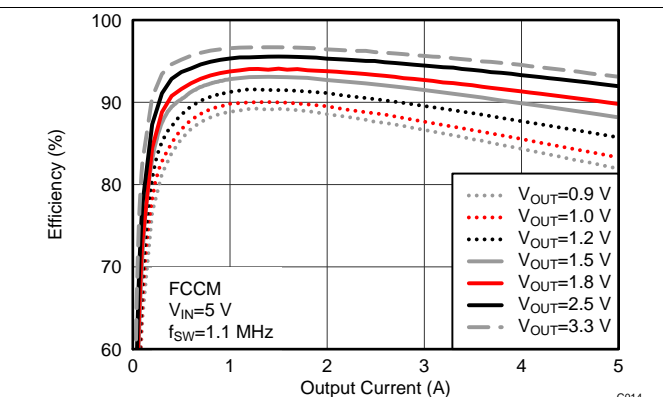


Figure 20. Efficiency vs Output Current, FCCM

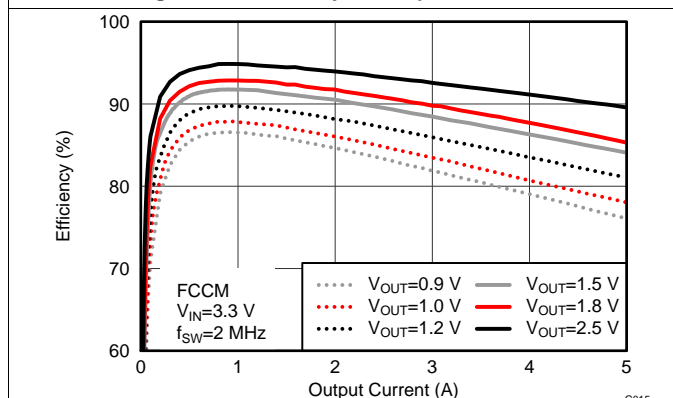


Figure 21. Efficiency vs Output Current, FCCM

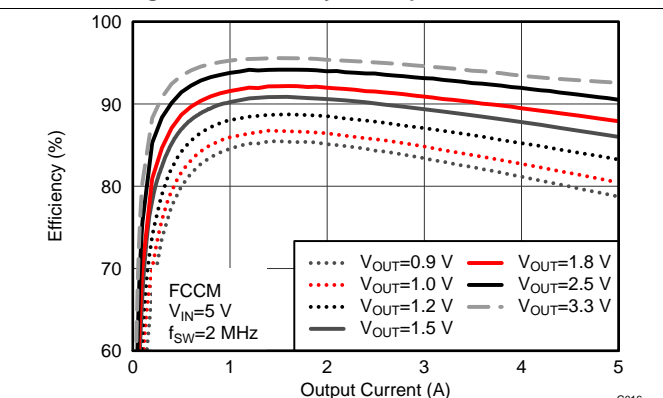


Figure 22. Efficiency vs Output Current, FCCM

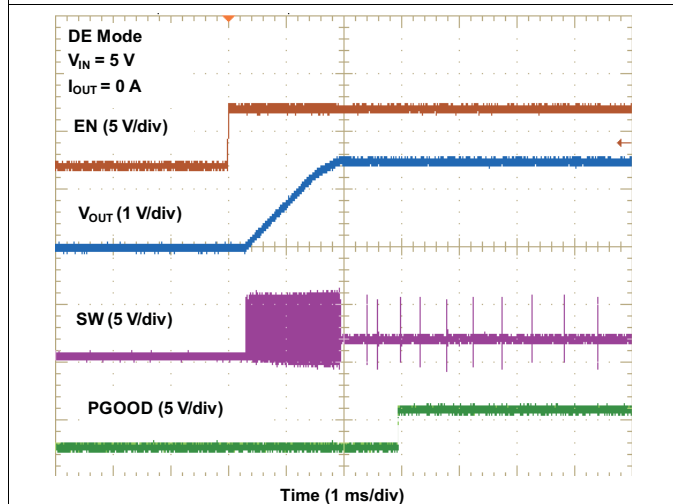


Figure 23. Normal Start-up

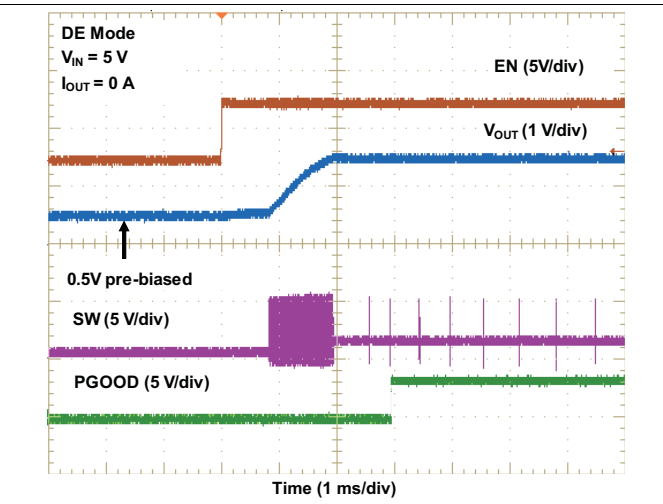


Figure 24. Prebiased Start-up

Typical Characteristics (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

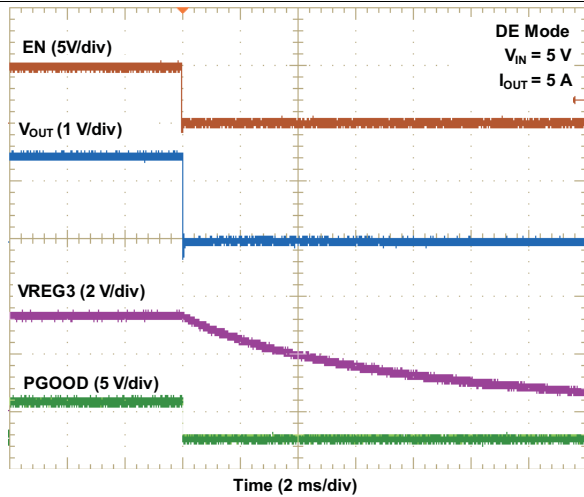


Figure 25. Turnoff Enable

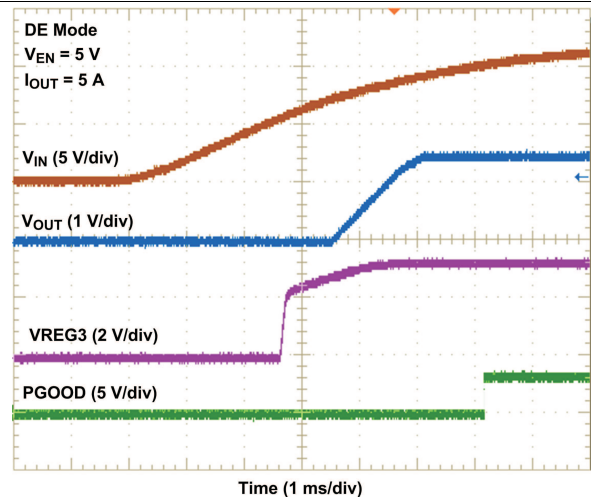


Figure 26. UVLO Start-Up Waveform

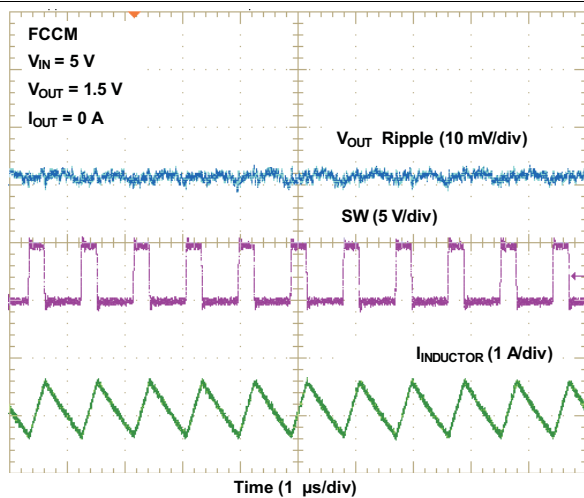


Figure 27. Output Voltage Ripple – FCCM

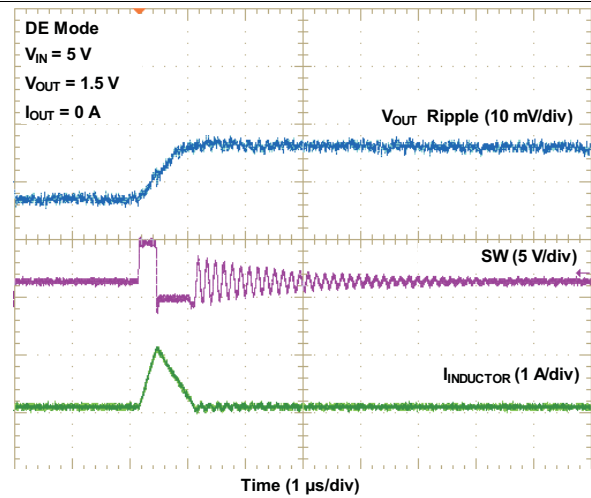


Figure 28. Output Voltage Ripple – DE Mode

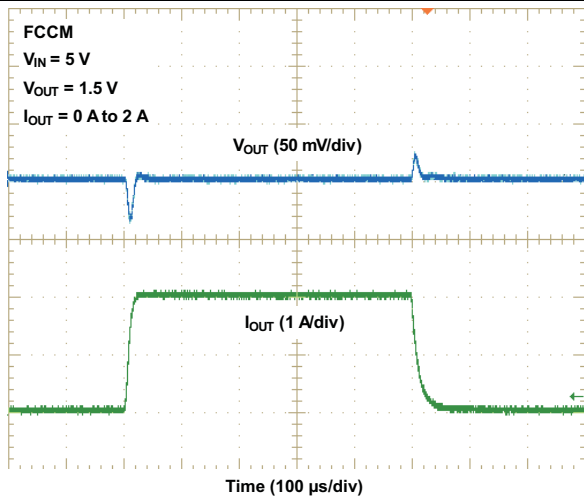


Figure 29. Load Transient – FCCM

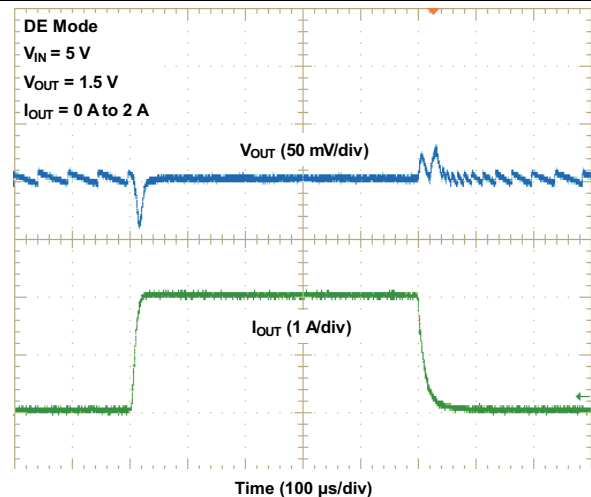


Figure 30. Load Transient – DE Mode

Typical Characteristics (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

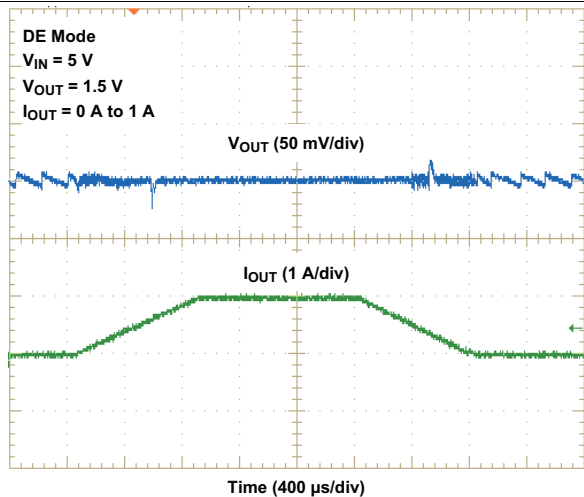


Figure 31. DE Mode DCM and CCM Transition

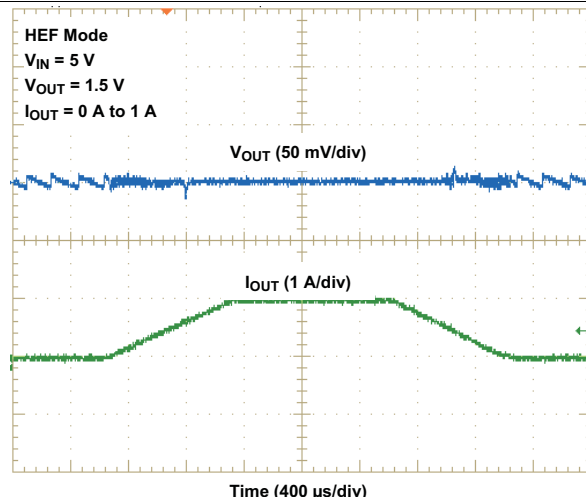


Figure 32. HEF Mode DCM and CCM Transition

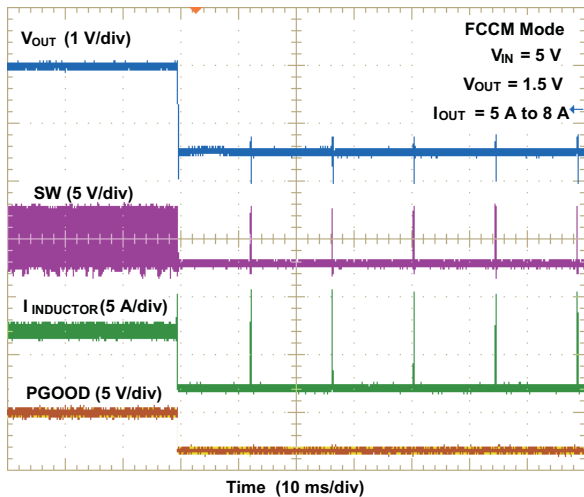


Figure 33. Overcurrent Protection

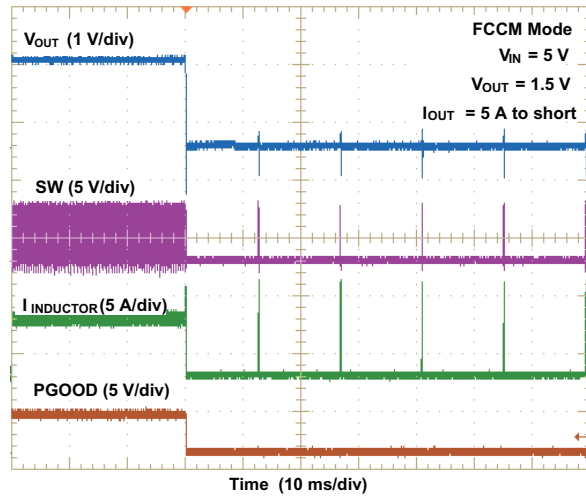


Figure 34. Short-Circuit Protection

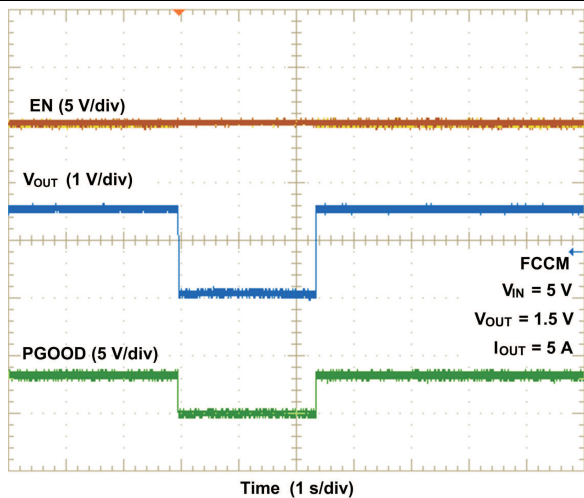


Figure 35. Overtemperature Protection

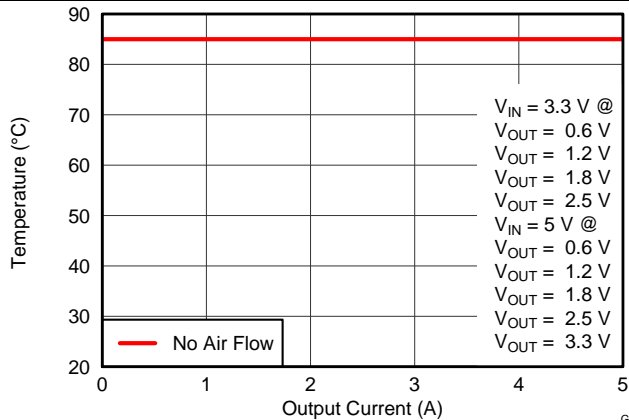


Figure 36. Safe Operating Area

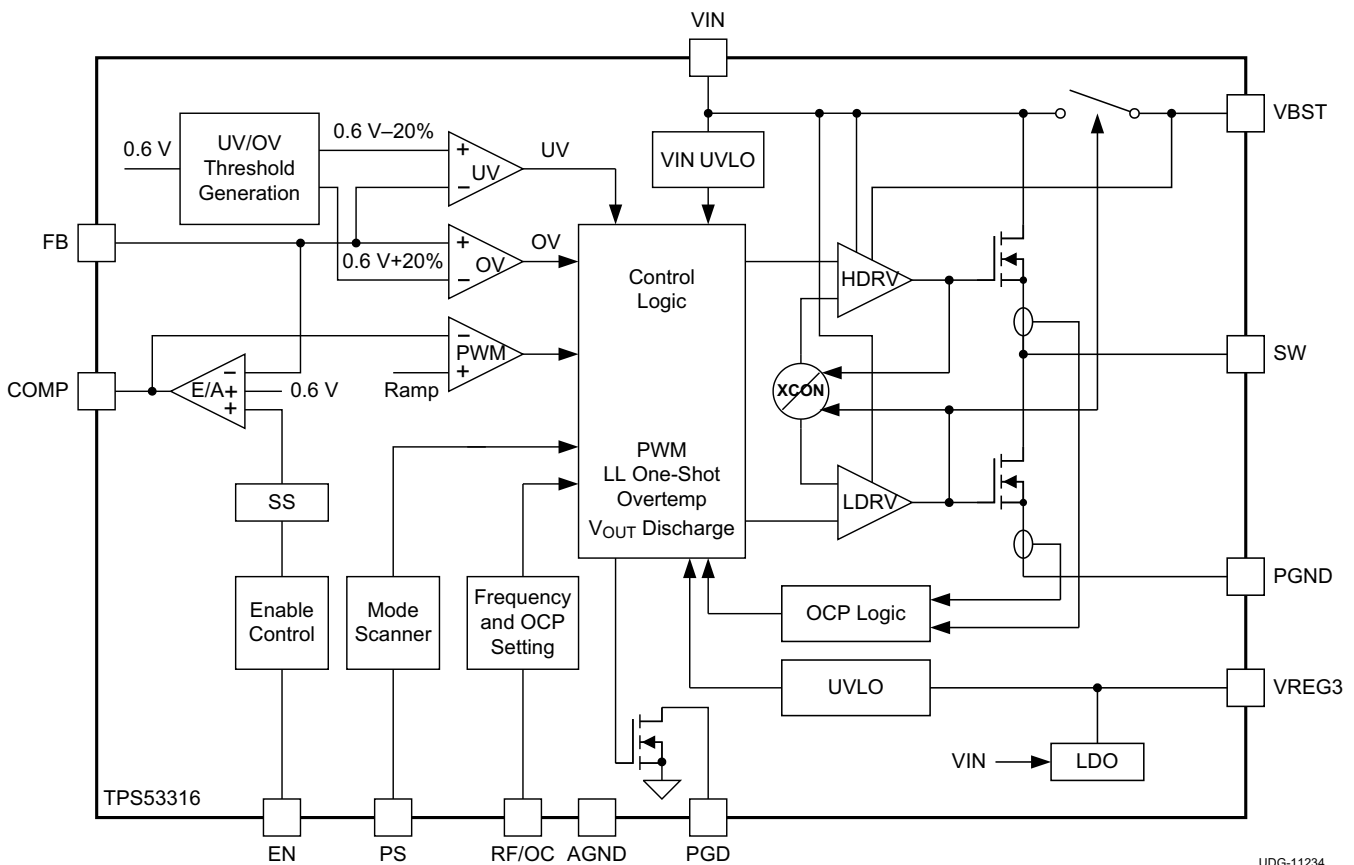
7 Detailed Description

7.1 Overview

The TPS53316 is a high-efficiency switching regulator with two integrated N-channel MOSFETs and is capable of delivering up to 5 A of load current. The TPS53316 provides output voltage from 0.6 V up to $0.8 \times V_{IN}$ from 2.9-V to 6-V wide input voltage range.

This device employs 3 operation modes to fit into various application requirements. The skip mode operation provides reduced power loss and increases the efficiency at light load. The unique, patented PWM modulator enables smooth light load to heavy load transition while maintaining fast load transient.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Overcurrent and Frequency Setting

The overcurrent and frequency setting are determined by RF/OC pin connection as shown in [Table 1](#). At start-up, the RF/OC pin sources 10- μ A current and then sense the voltage on this pin to determine the switching frequency and OCP threshold.

Table 1. Overcurrent and Frequency Setting

RF/OC PIN CONNECTION	FREQUENCY (kHz)	OVERCURRENT THRESHOLD (A)
GND	1100	6.5
24.3 k Ω to GND	750	4.5
57.6 k Ω to GND	750	6.5
105 k Ω to GND	2000	4.5
174 k Ω to GND	2000	6.5
Floating or pulled to VREG3	1100	4.5

7.3.2 Soft-Start Operation

The soft-start operation reduces the inrush current during the start-up time. A slow rising reference is generated by the soft-start circuitry and send to the input of the error amplifier. When the soft-start ramp voltage is less than 600 mV, the error amplifier uses this ramp voltage as the reference. When the ramp voltage reaches 600 mV, the error amplifier switch to a fixed 600-mV reference. The typical soft-start time is 400 μ s for 1 \times soft-start time setting and 1.6 ms for 4 times the soft-start time setting.

7.3.3 Power Good

The TPS53316 monitors the voltage on the FB pin. If the FB voltage is within 117% and 83% of the reference voltage, the power good signal remains high. If FB voltage is out of this window, power good pin is pulled low by the internal open-drain output.

During start-up operation, the input voltage must be higher than 1 V to have valid power good logic, and the power good signal has 300 μ s (1.2 ms with 4 times setting) delay after FB falling into the power good window. There is also 10- μ s delay during shutdown after FB falling out of the power good window.

7.3.4 UVLO Function

The TPS53316 provides UVLO protection for input voltage. If the input voltage is higher than UVLO threshold voltage, the device starts up. When the voltage becomes lower than the threshold voltage minus the hysteresis, the device shuts off. The typical UVLO rising threshold is 2.8 V and the hysteresis is 130 mV.

A similar UVLO function is provided to the VREG3 pin. The typical UVLO rising threshold is 2.8 V and the hysteresis is 75 mV for VREG3.

7.3.5 Overcurrent Protection

The TPS53316 continuously monitors the current flowing through high-side and low-side MOSFETs. If the current through the high-side FET exceeds 6.8 A (or 4.5 A with 4.5-A setting), the high-side FET turns off and the low-side FET turns on. An OC counter starts to increment to count the occurrence of the overcurrent events. The converter shuts down immediately when the OC counter reaches 4. The OC counter resets if the detected current is less 6.8 A after an OC event.

Another set of overcurrent circuitry monitors the current through low-side FET. If the current through the low-side FET exceeds 7.5 A (or 5.1 A with 4.5-A setting), the overcurrent protection is engaged and turns off both high-side and low-side FETs immediately. The device is fully protected against overcurrent during both on-time and off-time.

After an OCP event, the device attempts to restart after a hiccup delay (14.5 ms typical). If the OC condition clears before restart, the device starts up normally. Otherwise the hiccup process repeats.

7.3.6 Overvoltage Protection

The TPS53316 monitors the voltage divided feedback voltage to detect the overvoltage and undervoltage conditions. When the feedback voltage is greater than 117% of the reference, the high-side MOSFET turns off and the low-side MOSFET turns on. Then the output voltage drops and reaches the undervoltage threshold. At that point the low-side MOSFET turns off and the device enters high-impedance state.

7.3.7 Undervoltage Protection

When the feedback voltage is lower than 83% of the reference voltage, the undervoltage protection counter starts. If the feedback voltage remains lower than the undervoltage threshold voltage after 10 μ s, the device turns off both high-side and low-side MOSFETs and enters high-impedance state. After a hiccup delay (14.5 ms typical), the device attempts to restart. If the UV condition clears before restart, the device starts up normally. Otherwise the hiccup process repeats.

7.3.8 Overtemperature Protection

The TPS53316 continuously monitors the die temperature. If the die temperature exceeds the threshold value (140°C typical), the device shuts off. When the device is cooled to 40°C below the overtemperature threshold, it restarts and returns to normal operation.

7.3.9 Output Discharge

When the EN pin is low, the TPS53316 discharges the output capacitors through an internal MOSFET switch between SW and GND while the high-side and low-side MOSFETs remain OFF. The typical discharge switch-ON resistance is 60 Ω . This function is disabled when the input voltage is less than 1 V.

7.4 Device Functional Modes

7.4.1 Operation Mode

The TPS53316 has 3 operation modes determined by PS connection as listed in [Table 2](#). Each mode has two soft-start and power good delay options (1 time and 4 times). At start-up, the PS pin sources 10 μ A of current and then sense the voltage on this pin to determine the operation mode and soft-start time.

Table 2. Operation Mode Selection

PS PIN CONNECTION	OPERATION MODE	AUTO-SKIP AT LIGHT LOAD	SOFT-START TIME
GND	FCCM	No	4 times
24.3 k Ω to GND	HEF Mode	Yes	4 times
57.6 k Ω to GND	HEF Mode	Yes	1 times
105 k Ω to GND	DE Mode	Yes	1 time
174 k Ω to GND	DE Mode	Yes	4 times
Floating or pulled to VREG3	FCCM	No	1 time

In forced continuous conduction mode (FCCM), the high-side FET is ON during the on-time and low-side FET is ON during the off-time. The switching is synchronized to the internal clock thus the switching frequency is fixed.

In diode emulation mode (DE), the high-side FET is ON during the on-time and low-side FET is ON during the off-time until the inductor current reaches zero. An internal zero-crossing comparator detects the zero crossing of inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic control and turns off the low-side FET.

When the load is increased, the inductor current is always positive and the zero-crossing comparator does not send a zero-crossing signal. The converter enters into continuous conduction mode (CCM) when no zero-crossing is detected for two consecutive PWM pulses. The switching is synchronized to the internal clock and the switching frequency is fixed.

In high-efficiency mode (HEF), the converter does not synchronize to internal clock during CCM. Instead, the PWM modulator determines the switching frequency. The operation in discontinuous conduction mode (DCM) is the same as DE mode.

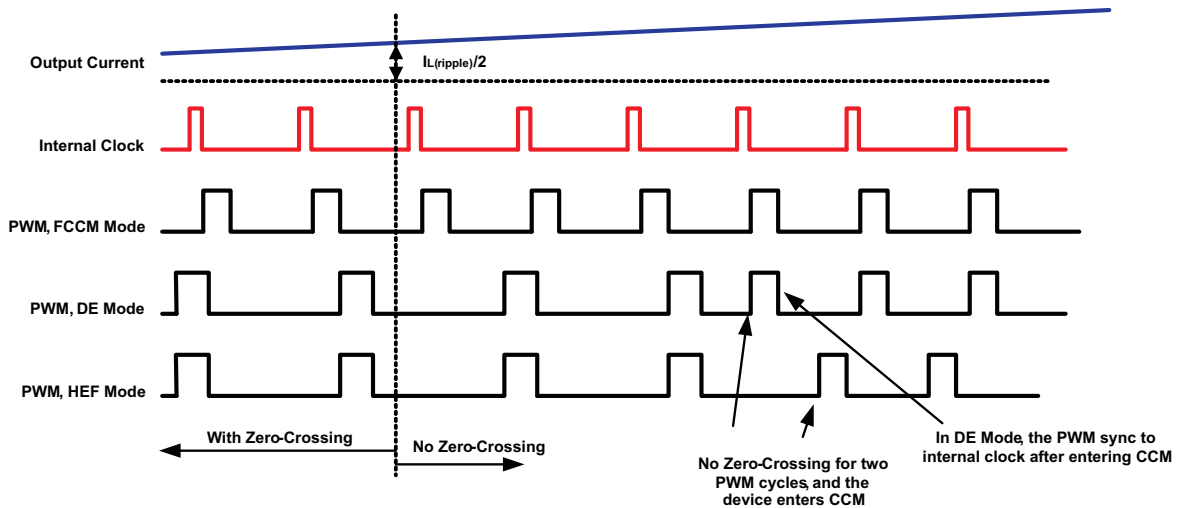
In both DE and HEF modes, the device operates under CCM with fixed SW frequency if the load current is higher than half of the inductor ripple current. When the load current is decreased and seven consecutive zero-crossing events are detected, the device enters DCM and light load control is enabled. The on-pulse in DCM is designed to be 25% higher than CCM to provide hysteresis to avoid chattering between CCM and DCM.

The PS pins also set the soft-start time and power good start-up delay of the device. The nominal sort-start time is 400 μ s from the time $V_{OUT} = 0$ V to when $V_{OUT} = 100\%$, and the nominal power good delay is 300 μ s from the time $V_{OUT} = 100\%$ to when power good is asserted. When the PS pin is connected to GND directly or with a resistor with a value of 24.3 k Ω or 174 k Ω , the soft-start time and power good delay is 4 times the nominal (1.6 ms for soft-start time and 1.2 ms for power good delay).

7.4.2 Light Load Operation

In skip modes (DE and HEF) when the load current is less than half of inductor ripple current, the inductor current reaches zero by the end of off-time. The light load control scheme then turns off the low-side MOSFET when inductor current reaches zero. Because there is no negative inductor current, the energy delivered to the load per switching cycle is increased compared to the normal PWM mode operation. The controller then reduces the switching frequency to maintain the output voltage regulation. The switching loss is reduced and thus efficiency is improved.

In both DE and HEF mode, when the load current decreases, the switching frequency also decreases continuously in discontinuous conduction mode (DCM). When the load current is 0 A, the minimum switching frequency is reached. It is also required that the difference between $V_{V_{BST}}$ and $V_{S_{W}}$ to be higher than 2.4 V to ensure the supply for high-side gate driver.



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Figure 37. TPS53316 Operation Modes in Light and Heavy Load Conditions

7.4.3 Forced Continuous Conduction Mode

When the PS pin is grounded or greater than 2.2 V, the TPS53316 is operating in continuous conduction mode in both light and heavy load condition. In this mode, the switching frequency remains constant over the entire load range which is suitable for applications requiring tight control of switching frequency at a cost of lower efficiency at light load.

8 Application and Implementation

NOTE

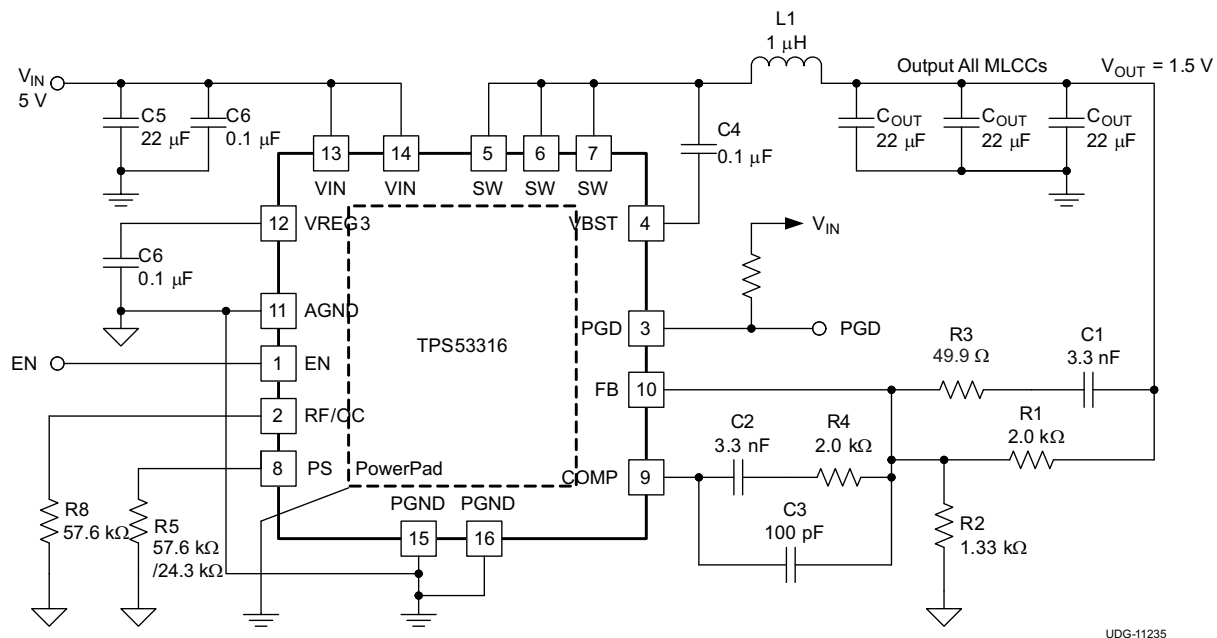
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS53316 device is a high-efficiency synchronous-buck converter. The device suits low output voltage point-of-load applications with 5-A or lower output current in computing and similar digital consumer applications.

8.2 Typical Application

This design example describes a voltage-mode, 5-A synchronous buck converter with integrated MOSFETs. The device provides a fixed 1.5-V output at up to 5 A from a 5-V input bus.



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Figure 38. Typical 3.3-V Input Application Circuit Diagram

8.2.1 Design Requirements

Table 3 lists the parameters for this design example.

Table 3. TPS53316 Design Example Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Voltage range	V_{IN}	2.9	3.3 or 5	6	V
Maximum input current	$V_{IN} = 5\text{ V}$, $I_{OUT} = 5\text{ A}$		1.76		A
No load input current	No load input current $V_{IN} = 5\text{ V}$, $I_{OUT} = 0\text{ A}$ under DE/HEF mode		3		mA

Typical Application (continued)

Table 3. TPS53316 Design Example Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS					
Output voltage			1.5		V
Output voltage regulation	Setpoint accuracy ($V_{IN} = 2.9\text{ V} - 6\text{ V}$, $I_{OUT} = 0\text{ A} - 5\text{ A}$)	-1%		1%	
	Line regulation ($V_{IN} = 2.9\text{ V} - 6\text{ V}$, $I_{OUT} = 5\text{ A}$)		0.1%		
	Load regulation ($V_{IN} = 5\text{ V}$, $I_{OUT} = 0\text{ A} - 5\text{ A}$)		0.1%		
Output voltage ripple	$V_{IN} = 5\text{ V}$, $I_{OUT} = 5\text{ A}$		10		mVPP
Output load current		0		5	A
Overcurrent limit	$V_{IN} = 3.3\text{ V}$, $f_{SW} = 750\text{ kHz}$		6.5 or 4.5		A
SYSTEM CHARACTERISTICS					
Switching frequency			0.75		MHz
Peak efficiency	$V_{IN} = 5\text{ V}$, $I_{OUT} = 1.8\text{ A}$, $f_{SW} = 750\text{ kHz}$		92.7%		
Full-load efficiency	$V_{IN} = 5\text{ V}$, $I_{OUT} = 5\text{ A}$, $f_{SW} = 750\text{ kHz}$		89%		
Operating temperature			25		°C

8.2.2 Detailed Design Procedure

Select the external components using the following steps.

8.2.2.1 Determine the Value of R1 and R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in [Figure 38](#). R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended value for R1 is between 1 kΩ and 10 kΩ. Determine R2 using [Equation 1](#).

$$R2 = \frac{0.6}{V_{OUT} - 0.6} \times R1 \quad (1)$$

8.2.2.2 Choose the Inductor

The inductance value must be determined to give the ripple current of approximately 20% to 40% of maximum output current. The inductor ripple current is determined by [Equation 2](#).

$$I_{L(\text{ripple})} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

The inductor also must have a low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

8.2.2.3 Choose the Output Capacitor(s)

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has three components. $V_{RIPPLE(C)}$ represents the ripple due to the output capacitance and is shown in [Equation 4](#).

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \quad (3)$$

$$V_{RIPPLE(C)} = \frac{I_{L(\text{ripple})}}{8 \times C_{OUT} \times f_{SW}} \quad (4)$$

$$V_{RIPPLE(ESR)} = I_{L(\text{ripple})} \times ESR \quad (5)$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L} \quad (6)$$

When ceramic output capacitor is chosen, the ESL component is usually negligible. In the case when multiple output capacitors are used, the total ESR and ESL must be the equivalent of the all output capacitors in parallel.

When operating in DCM, the output ripple is dominated by the component determined by capacitance. It also varies with load current and can be expressed as shown in [Equation 7](#).

$$V_{\text{RIPPLE(DCM)}} = \frac{(\alpha \times I_{\text{L(ripple)}} - I_{\text{OUT}})^2}{2 \times f_{\text{SW}} \times C_{\text{OUT}} \times I_{\text{L(ripple)}}$$

where

- α is the DCM on-time coefficient (typical value is 1.25) and can be expressed as
$$\alpha = \frac{t_{\text{ON(DCM)}}}{t_{\text{ON(CCM)}} \quad (7)$$

[Figure 39](#) illustrates the DCM output voltage ripple.

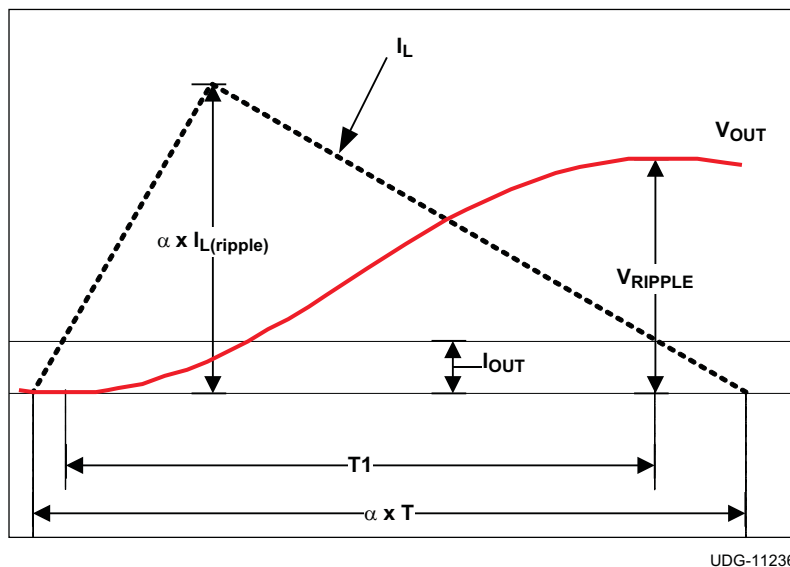


Figure 39. Discontinuous Mode Output Voltage Ripple

8.2.2.4 Choose the Input Capacitors

The selection of input capacitor must be determined by the ripple current requirement. The ripple current generated by the converter must be absorbed by the input capacitors as well as the input source. The RMS ripple current from the converter can be expressed as shown in [Equation 8](#).

$$I_{\text{IN(ripple)}} = I_{\text{OUT}} \times \sqrt{D \times (1 - D)}$$

where

- D is the duty cycle and can be expressed as
$$D = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \quad (8)$$

To minimize the ripple current drawn from the input source, sufficient input decoupling capacitors must be placed close to the device. The ceramic capacitor is recommended due to the low ESR and low ESL. The input voltage ripple can be calculated in [Equation 9](#) when the total input capacitance is determined.

$$V_{\text{IN(ripple)}} = \frac{I_{\text{OUT}} \times D}{f_{\text{SW}} \times C_{\text{IN}}} \quad (9)$$

8.2.2.5 Compensation Design

The TPS53316 employs voltage mode control. To effectively compensation the power stage and ensures fast transient response, Type III compensation is typically used.

The control to output transfer function can be described in Equation 10.

$$G_{CO} = 4 \times \frac{1 + s \times C_{OUT} \times ESR}{1 + s \times \left(\frac{L}{DCR + R_{LOAD}} + C_{OUT} \times (ESR + DCR) \right) + s^2 \times L \times C_{OUT}} \quad (10)$$

The output LC filter introduces a double pole which can be calculated in Equation 11.

$$f_{DP} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}} \quad (11)$$

The ESR zero of can be calculated in Equation 12.

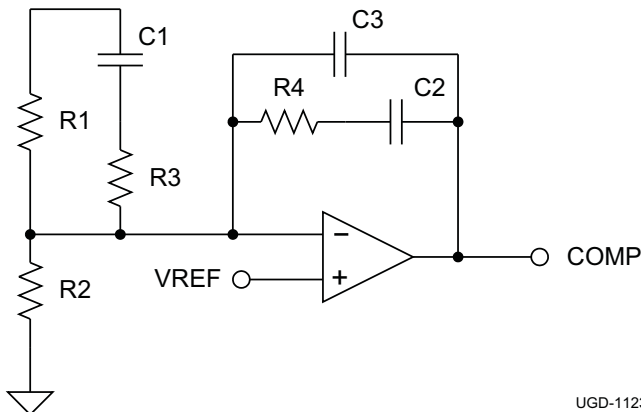
$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \quad (12)$$

Figure 40 shows the configuration of Type III compensation and typical pole and zero locations. Equation 13 through Equation 15 describe the compensator transfer function and poles and zeros of the Type III network.

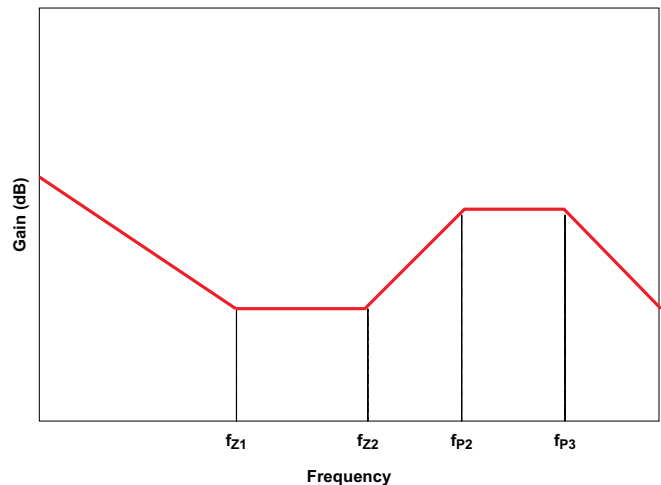
$$G_{EA} = \frac{(1 + s \times C1 \times (R1 + R3))(1 + s \times R4 \times C2)}{(s \times R1 \times (C2 + C3)) \times (1 + s \times C1 \times R3) \times \left(1 + s \times R4 \times \frac{C2 \times C3}{C2 + C3} \right)} \quad (13)$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R4 \times C2} \quad (14)$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C1} \cong \frac{1}{2 \times \pi \times R1 \times C1} \quad (15)$$



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Figure 40. Type III Compensation Network Schematic

Figure 41. Type III Compensation Network Waveform

$$f_{P1} = 0 \quad (16)$$

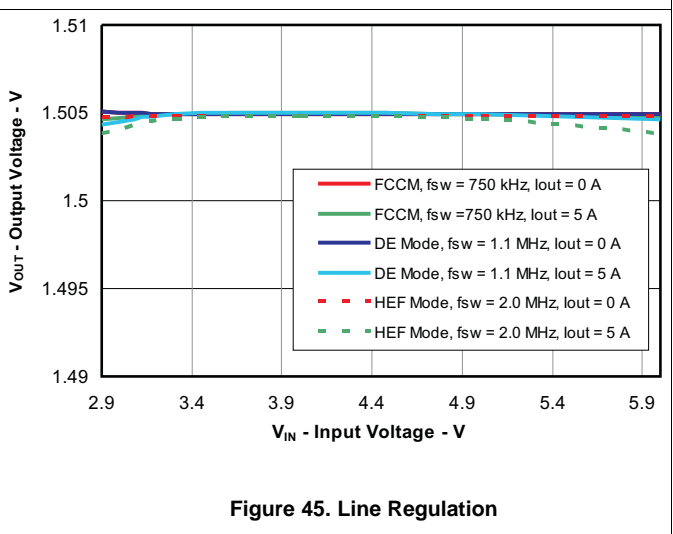
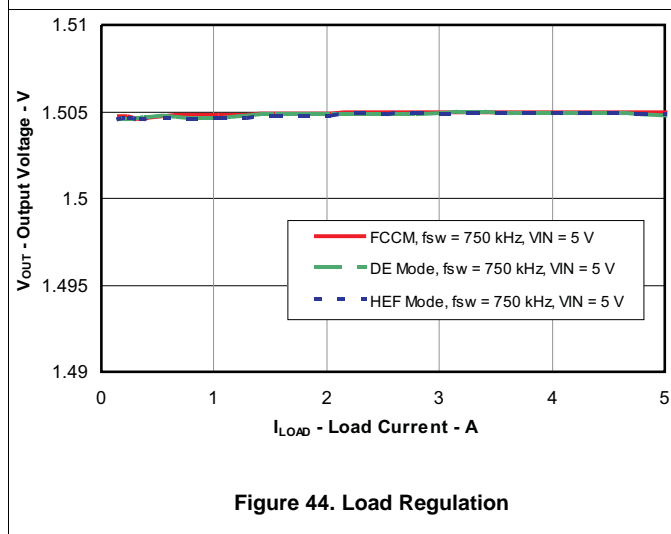
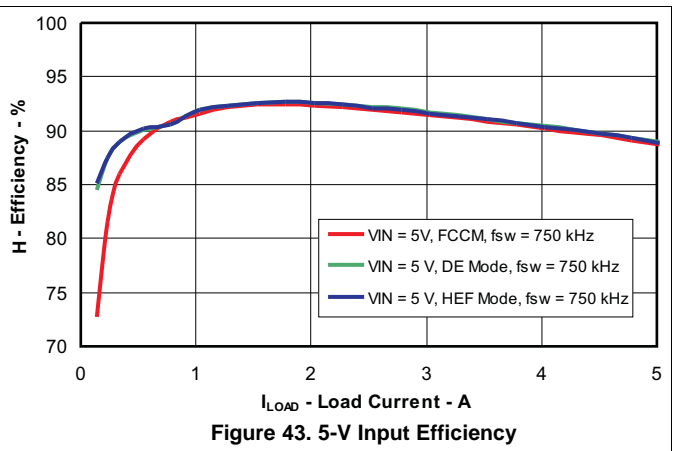
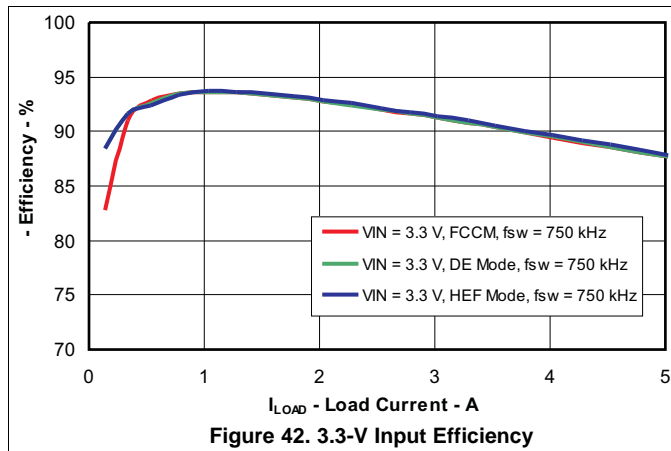
$$f_{P2} = \frac{1}{2 \times \pi \times R3 \times C1} \quad (17)$$

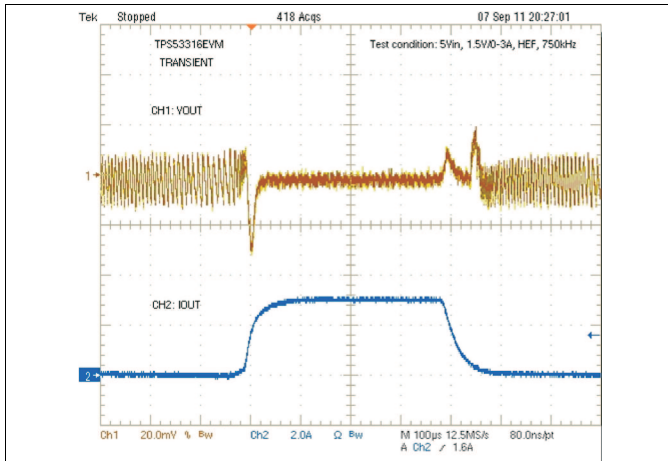
$$f_{P3} = \frac{1}{2 \times \pi \times R4 \times \left(\frac{C2 \times C3}{C2 + C3} \right)} \cong \frac{1}{2 \times \pi \times R4 \times C3} \quad (18)$$

The two zeros can be placed near the double-pole frequency to cancel the response from the double pole. One pole can be used to cancel ESR zero, and the other non-zero pole can be placed at half switching frequency to attenuate the high frequency noise and switching ripple. Suitable values can be selected to achieve a compromise between high phase margin and fast response. A phase margin higher than 45° is required for stable operation.

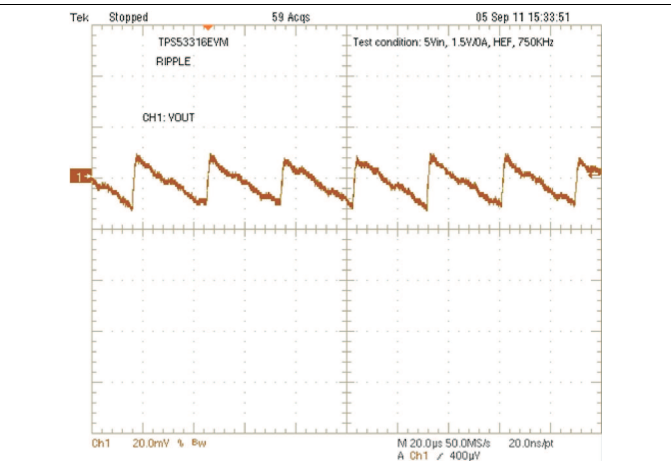
For DCM operation, a C3 capacitor value between 56 pF and 150 pF is recommended for output capacitance between 20 μF to 200 μF.

8.2.3 Application Curves

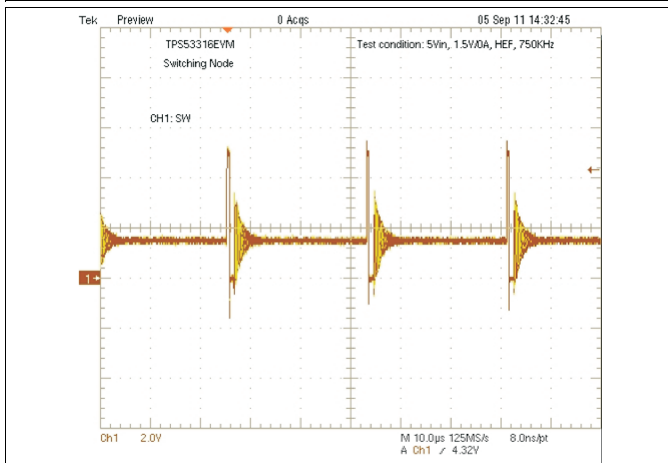




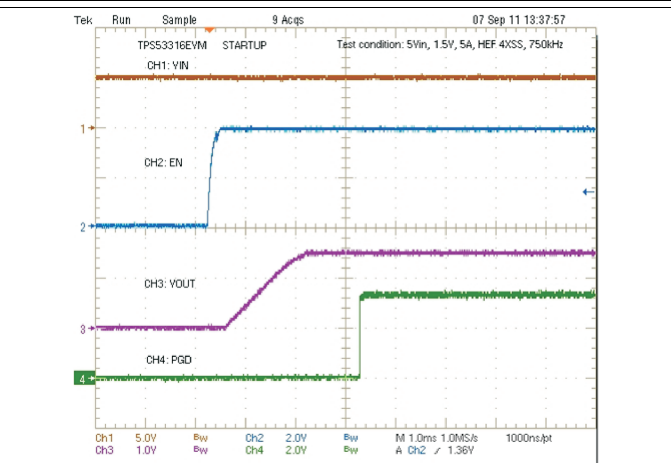
5-V VIN, 1.5-V VOUT, HEF Mode, and $f_{SW} = 750$ kHz
Figure 46. Load 0-3 A Transient Under HEF Mode



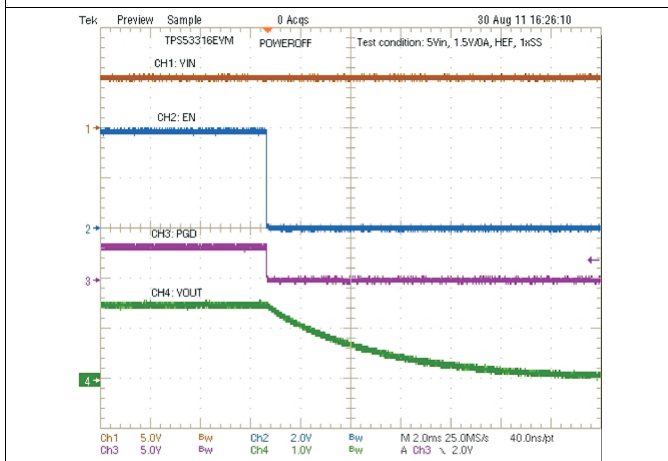
5-V VIN, 1.5-V VOUT, 0-A, HEF Mode, and $f_{SW} = 750$ kHz
Figure 47. Output Ripple



5-V VIN, 1.5-V VOUT, 0-A, HEF Mode, and $f_{SW} = 750$ kHz
Figure 48. Switching Node

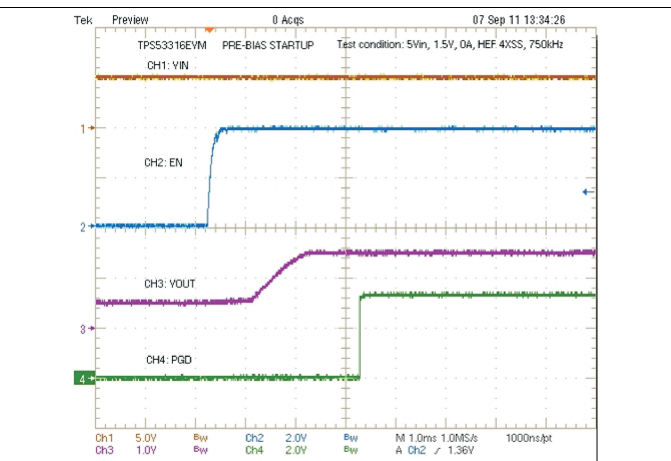


5-V VIN, 1.5-V VOUT, 5-A IOUT, and 4 times soft start
Figure 49. Turnon Waveform



5-V VIN, 1.5-V VOUT, and 0-A IOUT

Figure 50. Turnoff Waveform



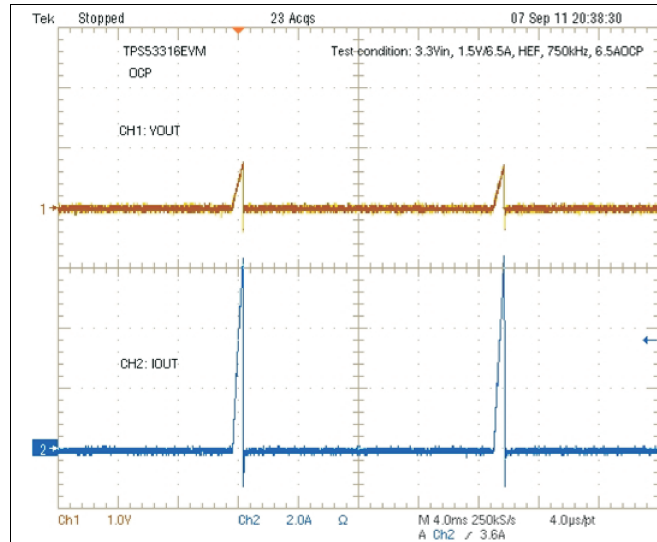
5-V VIN, 1.5-V VOUT, 0-A IOUT, 4 times soft start, and 0.5-V prebias

Figure 51. Prebias Turnon Waveform

TPS53316

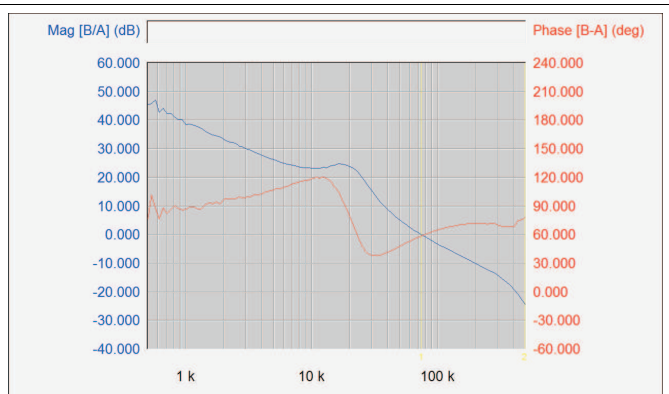
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3.3-V VIN, 1.5-V VOUT, 6.5-A IOUT, 4 times soft start, 750 kHz, and 6.5-A OCP

Figure 52. Overcurrent Protection Waveform



5-V VIN, 1.5-V VOUT, 5-A IOUT, HEF mode, and $f_{SW} = 750$ kHz

Figure 53. Loop Gain

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.9 V and 6 V. The input voltage source V_{IN} must be a 0-V to 6-V variable DC source capable of supplying 5 ADC. Proper bypassing of input supplies is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in [Layout](#).

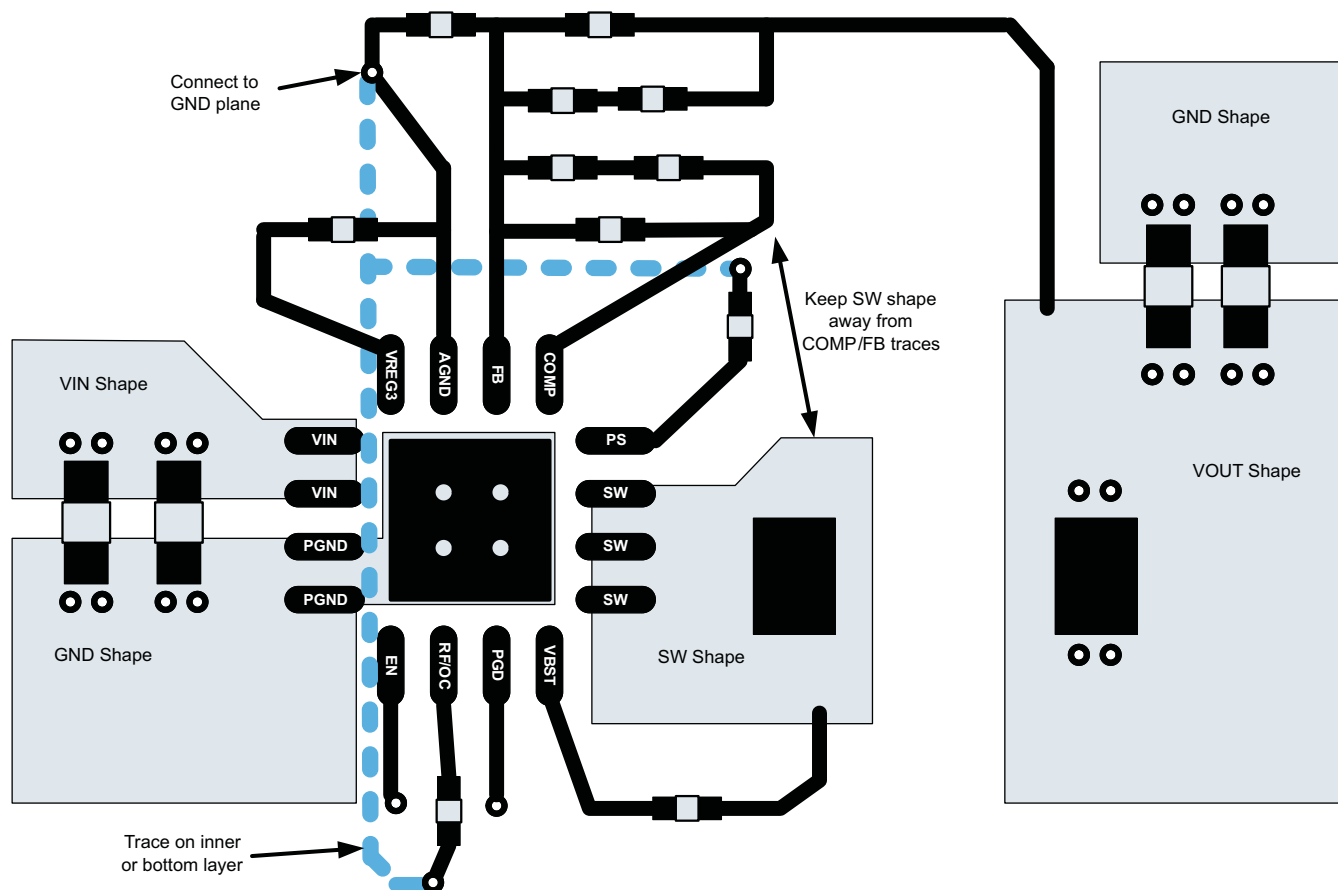
10 Layout

10.1 Layout Guidelines

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout:

- Separate the power ground and analog ground. Connect analog ground to GND plane with single via or a 0- Ω resistor at a quiet place.
- Use 4 vias to connect the thermal pad to power ground.
- Place V_{IN} and V_{REG3} decoupling capacitors as close to the device as possible.
- Use wide traces for V_{IN} , V_{OUT} , PGND and SW. These nodes carry high-current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep analog signals (FB, COMP) away from noisy signals (SW, VBST).
- See [5-A Step-Down Regulator with Integrated Switcher](#) (SLUU671) for a layout example.

10.2 Layout Example



UDG-11270

Figure 54. Layout Recommendation

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

《具有集成开关的 5A 降压稳压器》(SLUU671)

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的通知我 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

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11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53316RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3316	Samples
TPS53316RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3316	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53316RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53316RGTT	VQFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53316RGTR	VQFN	RGT	16	3000	338.0	355.0	50.0
TPS53316RGTT	VQFN	RGT	16	250	205.0	200.0	33.0

RGT 16

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

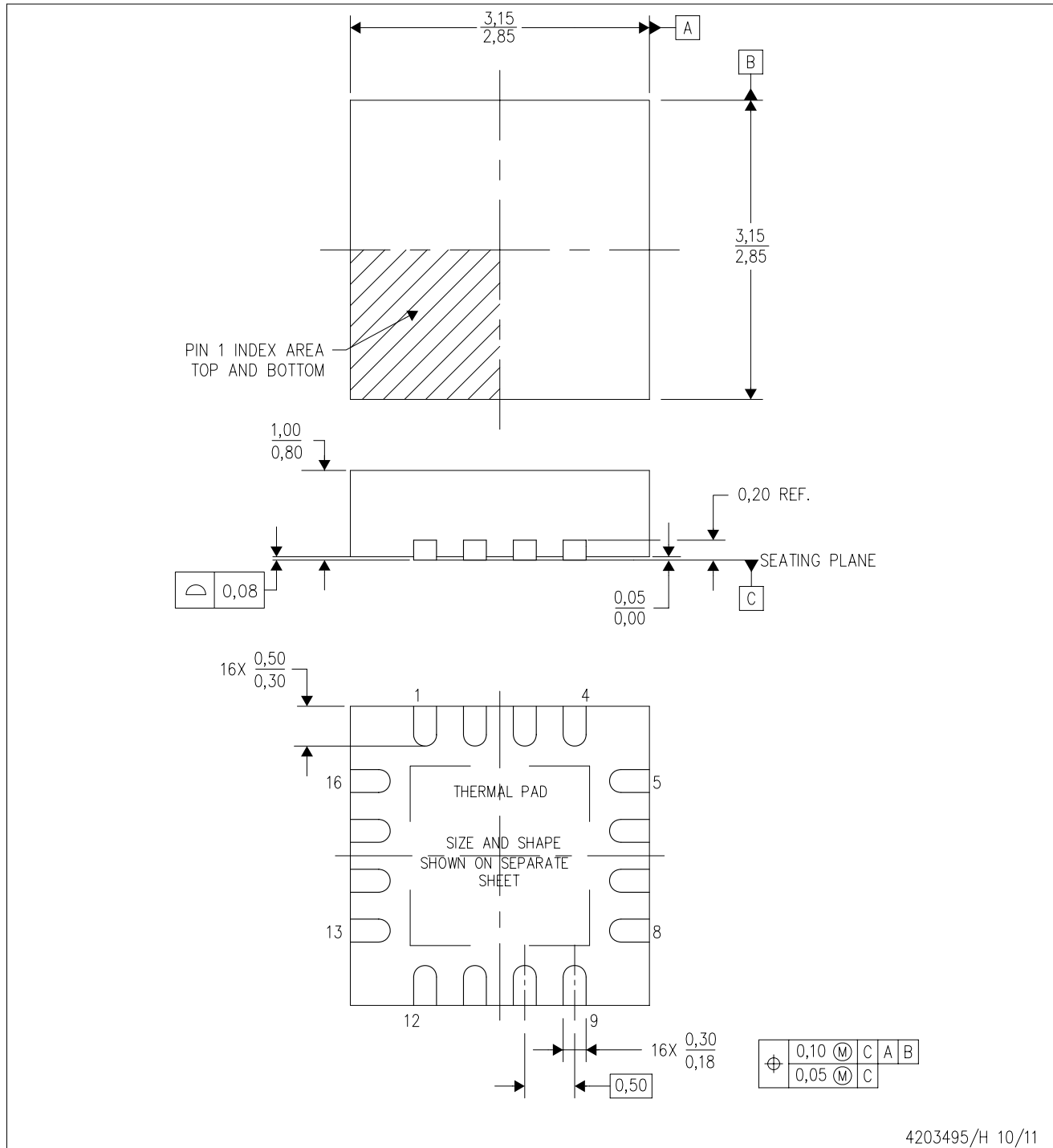


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

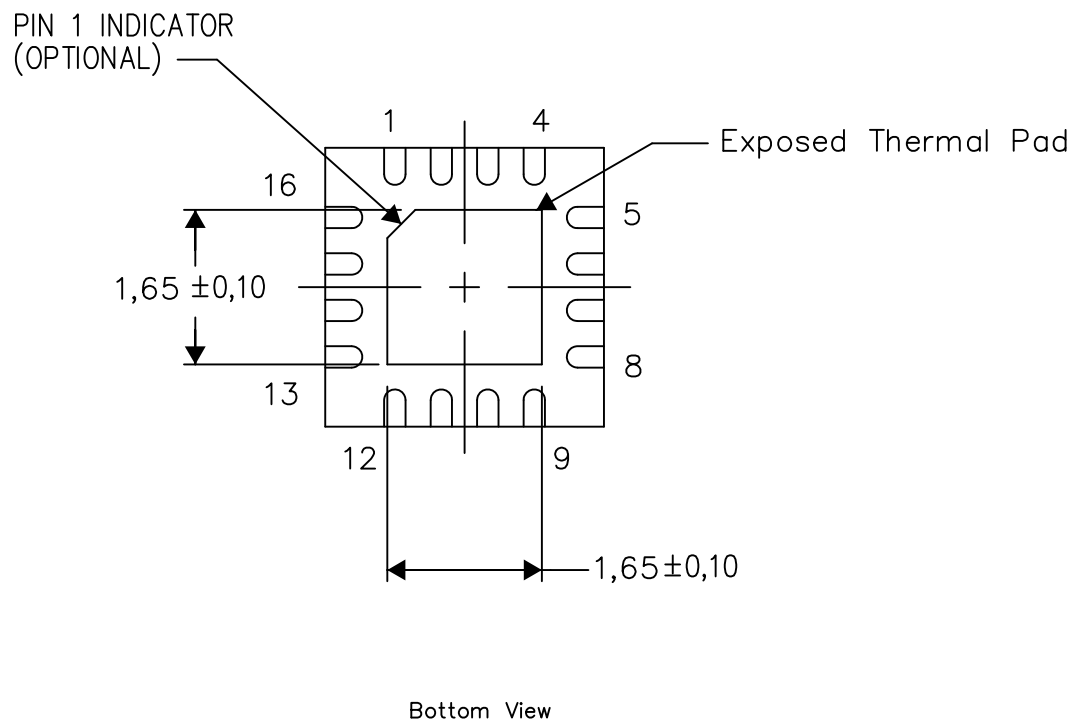
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206349-7/Z 08/15

NOTE: All linear dimensions are in millimeters



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



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NOTES:

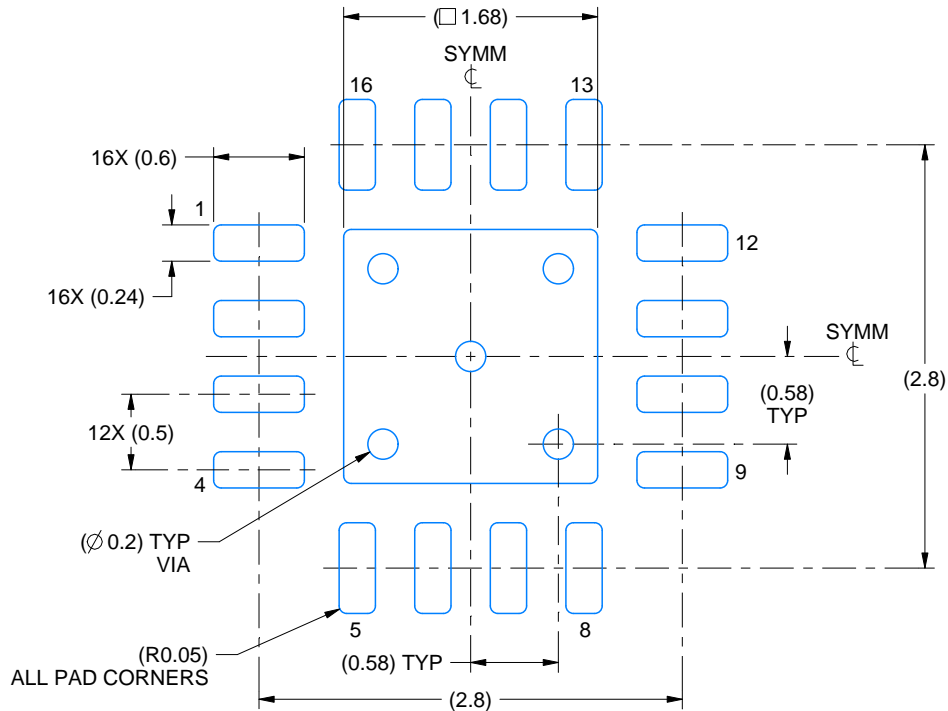
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

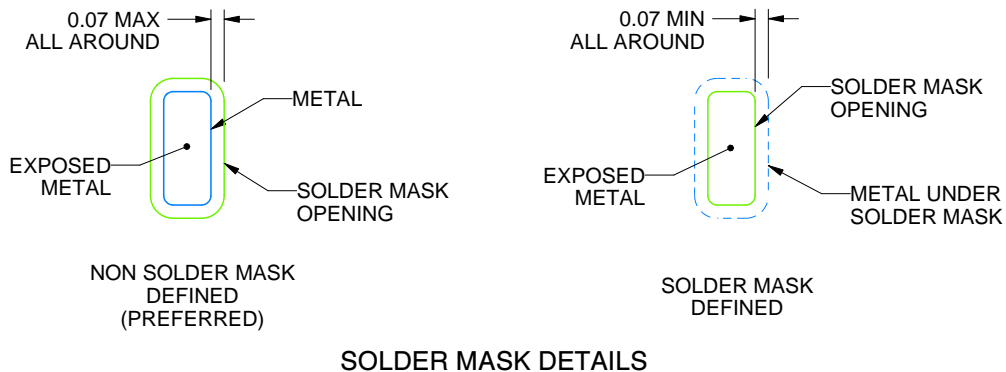
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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