

## TLV6256x 采用 5 引脚 SOT-23 封装的 1.5A 高效降压转换器

### 1 特性

- 输入电压范围：2.7V 至 5.5V
- 1.5MHz 典型开关频率
- 输出电流高达 1.5A（最大值）
- 自适应接通时间电流控制
- 针对轻载效率的省电模式
- 50 $\mu$ A 运行静态电流
- 效率高达 95%
- 过流保护
- 95% 最大占空比
- 出色的交流和瞬态负载响应
- 电源正常输出，TLV62566
- 250 $\mu$ s 的内部软启动（典型值）
- 可调节输出电压
- 热关断保护
- 采用 5 引脚小外形尺寸晶体管 (SOT)-23 封装

### 2 应用

- 便携式设备
- DSL 调制解调器
- 硬盘驱动器
- 机顶盒
- 平板电脑

### 3 说明

TLV62565/6 器件是针对小型解决方案尺寸和高效率进行优化的同步降压转换器。此器件集成了能够传送高达 1.5A 输出电流的开关。

此器件借助谷值电流模式控制系统配置，根据自适应接通时间进行工作。中等或重负载时的典型工作频率为 1.5MHz。此器件被优化以便即使在使用小型外部组件时也能实现极低的输出电压纹波，并且特有一个出色的负载瞬态响应。

轻负载期间，TLV62565/6 在最低静态电流（典型值 50 $\mu$ A）时自动进入省电模式以在整个负载电流范围内保持高效率。关断时，流耗减少至小于 1 $\mu$ A。

TLV62565/6 通过一个外部电阻分压器来提供一个可调输出电压。输出电压启动斜坡由一个内部软启动控制，通常为 250 $\mu$ s。通过配置使能 (TLV62565) 和电源正常 (TLV62566) 引脚也有可能实现电源排序。其它诸如过流保护和过热保护的特性是内置的。

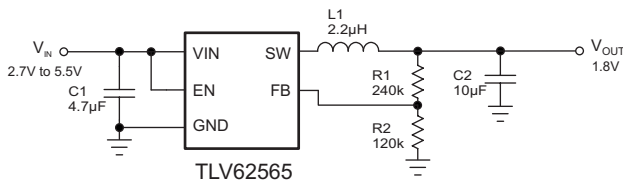
TLV62565/6 器件采用 5 引脚 SOT-23 封装。

#### 器件信息(1)

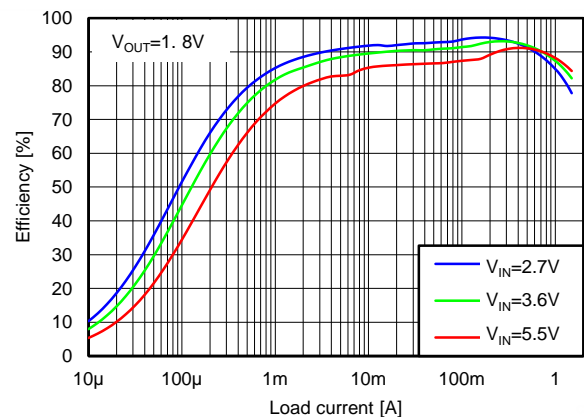
器件型号	封装	封装尺寸（标称值）
TLV62565 和 TLV62566	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

### 4 简化电路原理图



效率与负载电流间的关系



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## 5 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

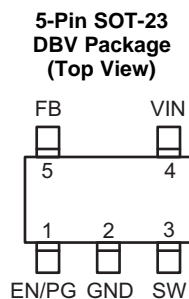
Changes from Revision A (November 2014) to Revision B	Page
• Added Storage temperature to Absolute Maximum Ratings .....	4
• Changed Handling Ratings to ESD Ratings .....	4
• Deleted Storage temperature from ESD Ratings .....	4
• 已更改 Thermal Information to Thermal Considerations and moved to Layout section .....	18

Changes from Original (October 2013) to Revision A	Page
• 已更改 添加了处理额定值表，特性描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。 .....	1
• Added "T <sub>A</sub> = -40°C to 85°C" to the V <sub>FB</sub> , Feedback regulation voltage Test Conditions .....	5
• Added V <sub>FB</sub> , Feedback regulation voltage Test Conditions and values for "PWM operation, T <sub>A</sub> = 85°C" .....	5

## 6 Device Comparison Table

PART NUMBER	FUNCTION
TLV62566	EN
TLV62566	PG

## 7 Pin Configuration and Functions



### Pin Functions

NAME	PIN		I/O/PWR	DESCRIPTION
	NUMBER			
	TLV62565	TLV62566		
EN	1	—	I	Device enable logic input. Logic HIGH enables the device, logic low disables the device and turns it into shutdown.
FB	5	5	I	Feedback pin for the internal control loop. Connect this pin to the external feedback divider.
GND	2	2	PWR	Ground pin.
PG	—	1	O	Power Good open drain output. This pin is high impedance if the output voltage is within regulation. It is pulled low if the output is below its nominal value. It is also in logic low when $V_{IN}$ below UVLO or thermal shutdown triggers.
SW	3	3	PWR	Switch pin connected to the internal MOSFET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	4	4	PWR	Power supply voltage input.

## 8 Specifications

### 8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	V <sub>IN</sub> , EN,PG	-0.3	7	V
	SW	-0.3	V <sub>IN</sub> +0.3	V
	FB	-0.3	3.6	V
Sink current, I <sub>PG</sub>	PG		660	μA
Continuous total power dissipation		See <a href="#">Thermal Information</a>		
Operating junction temperature, T <sub>J</sub>		-40	150	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

### 8.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions<sup>(1)</sup>

		MIN	TYP	MAX	UNIT
V <sub>IN</sub>	Input voltage, V <sub>IN</sub>	2.7		5.5	V
T <sub>A</sub>	Operating ambient temperature	-40		85	°C

- (1) Refer to the [Application and Implementation](#) section for further information.

### 8.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV62565, TLV62566	UNIT
		DBV (5 Pins)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	208.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	73.7	
R <sub>θJB</sub>	Junction-to-board thermal resistance	36.1	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.3	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	35.3	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 8.5 Electrical Characteristics

Over recommended free-air temperature range,  $V_{IN} = 3.6\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$V_{IN}$	Input voltage		2.7		5.5	V
$I_Q$	Quiescent current into VIN pin	$I_{OUT} = 0\text{ mA}$ , Not switching		50		$\mu\text{A}$
$V_{UVLO}$	Under voltage lock out	$V_{IN}$ falling		2.2	2.3	V
	Under voltage lock out hysteresis			200		mV
$T_{JSD}$	Thermal shutdown	Junction temperature rising		150		$^\circ\text{C}$
	Thermal shutdown hysteresis	Junction temperature falling below $T_{JSD}$		20		
<b>LOGIC INTERFACE, TLV62565</b>						
$V_{IH}$	High-level input voltage	$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	1.2			V
$V_{IL}$	Low-level input voltage	$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$			0.4	V
$I_{SD}$	Shutdown current into VIN pin	EN = LOW		0.1	1	$\mu\text{A}$
$I_{EN,LKG}$	EN leakage current			0.01	0.16	$\mu\text{A}$
<b>POWER GOOD, TLV62566</b>						
$V_{PG}$	Power Good low threshold	$V_{FB}$ falling referenced to $V_{FB}$ nominal		90%		
	Power Good high threshold	$V_{FB}$ rising referenced to $V_{FB}$ nominal		95%		
$V_L$	Low level voltage	$I_{sink} = 500\text{ }\mu\text{A}$			0.4	V
$I_{PG,LKG}$	PG Leakage current	$V_{PG} = 5.0\text{ V}$		0.01	0.17	$\mu\text{A}$
<b>OUTPUT</b>						
$V_{OUT}$	Output voltage		0.6		$D_{MAX} \cdot V_{IN}$	V
$V_{FB}$	Feedback regulation voltage	PWM operation, $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	0.588	0.6	0.612	V
		PWM operation, $T_A = 85^\circ\text{C}$	0.594	0.6	0.606	V
		PFM comparator threshold		0.9%		
$I_{FB}$	Feedback input bias current	$V_{FB} = 0.6\text{ V}$		10	100	nA
$R_{DS(on)}$	High-side FET on resistance	$I_{SW} = 500\text{ mA}$ , $V_{IN} = 3.6\text{ V}$		173		m $\Omega$
	Low-side FET on resistance	$I_{SW} = 500\text{ mA}$ , $V_{IN} = 3.6\text{ V}$		105		
$I_{LIM,LS}$	Low-side FET valley current limit		1.5			A
$I_{LIM,HS}$	High-side FET peak current limit		1.8			A
$f_{SW}$	Switching frequency			1.5		MHz
$D_{MAX}$	Maximum duty cycle			95%		
$t_{OFF,MIN}$	Minimum off time			40		ns

## 8.6 Typical Characteristics

**表 1. Table of Graphs**

		FIGURE
Efficiency	vs Load current ( $V_{OUT} = 1.8\text{ V}$ , $V_{IN} = 2.7\text{ V}, 3.6\text{ V}, 5.5\text{ V}$ )	<a href="#">图 1</a>
	vs Load current ( $V_{OUT} = 1.2\text{ V}$ , $V_{IN} = 2.7\text{ V}, 3.6\text{ V}, 5.5\text{ V}$ )	<a href="#">图 2</a>
	vs Load current ( $V_{OUT} = 3.3\text{ V}$ , $V_{IN} = 4.2\text{ V}, 5.5\text{ V}$ )	<a href="#">图 3</a>
Output voltage	vs Input voltage (Line regulation, $V_{OUT} = 1.8\text{ V}$ , Load = 0.5 A, 1 A, 1.5 A)	<a href="#">图 4</a>
	vs Load current (Load regulation, $V_{OUT} = 1.8\text{ V}$ , $V_{IN} = 2.7\text{ V}, 3.6\text{ V}, 5.5\text{ V}$ )	<a href="#">图 5</a>
Quiescent current	vs Input voltage	<a href="#">图 6</a>
$R_{DS(on)}$	vs Input voltage, High-Side FET	<a href="#">图 7</a>
	vs Input voltage, Low-Side FET	<a href="#">图 8</a>
Switching frequency	vs Load current, $V_{OUT} = 1.8\text{ V}$	<a href="#">图 9</a>

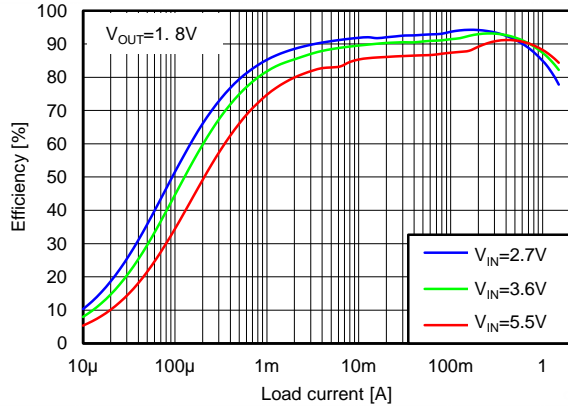


图 1. Efficiency vs Load Current

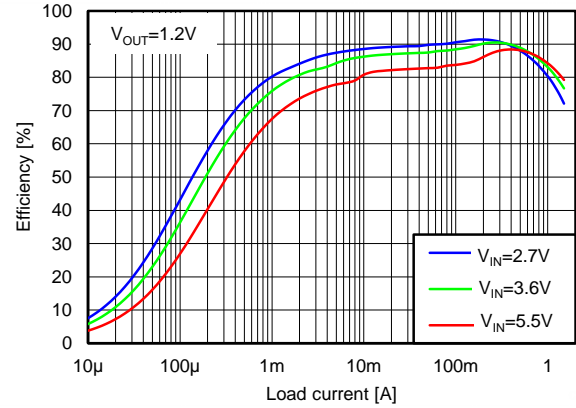


图 2. Efficiency vs Load Current

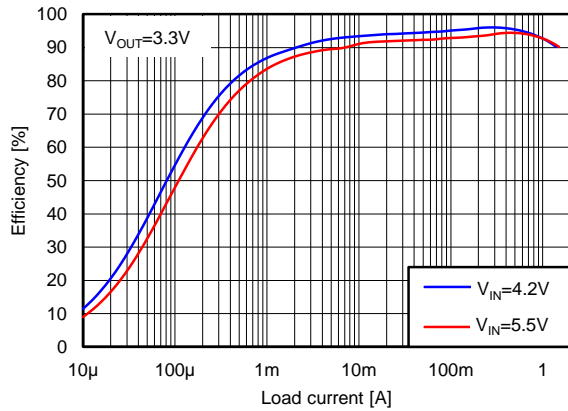


图 3. Efficiency vs Load Current

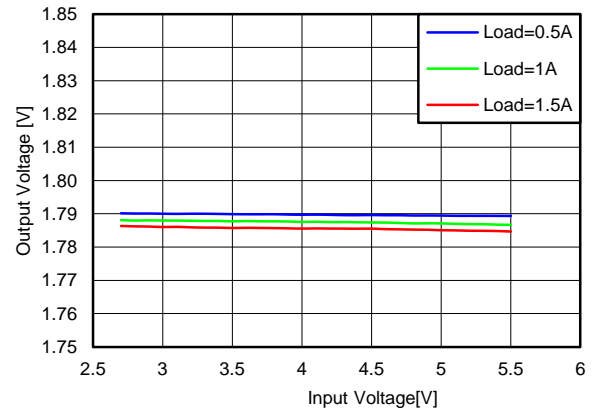


图 4. Output Voltage vs Input Voltage

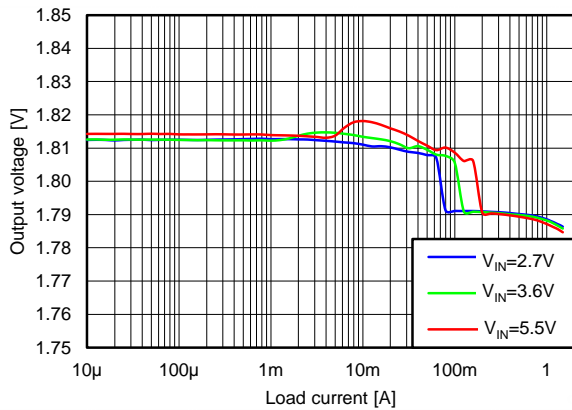


图 5. Output Voltage vs Load Current

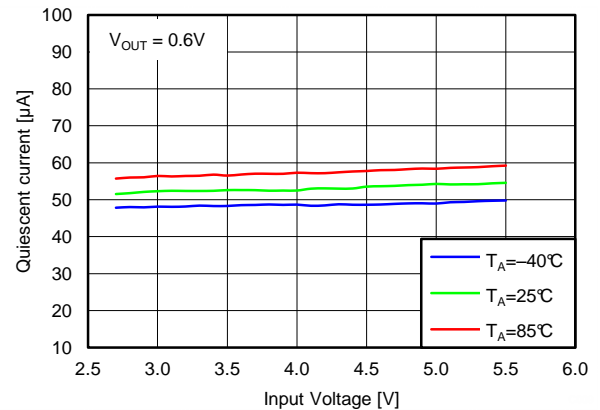


图 6. Quiescent Current vs Input Voltage

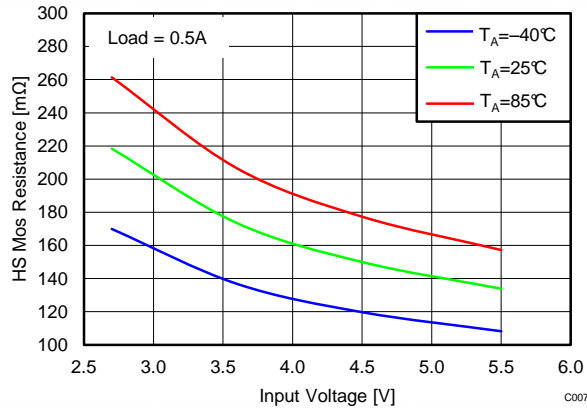


图 7. High-Side FET  $R_{DS(on)}$  vs Input Voltage

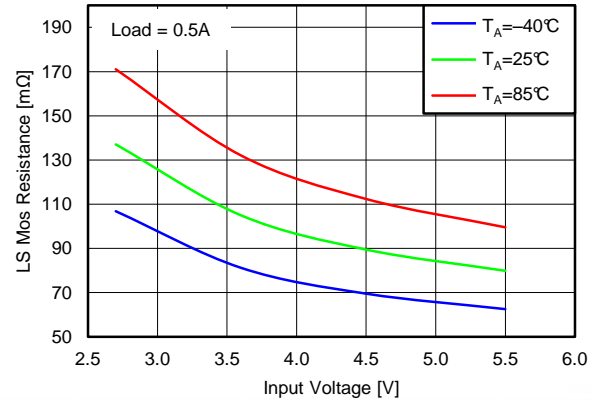


图 8. Low-Side FET  $R_{DS(on)}$  vs Input Voltage

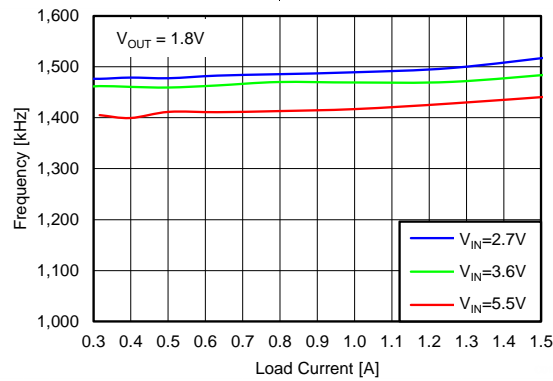


图 9. Switching Frequency vs Load Current

## 9 Parameter Measurement Information

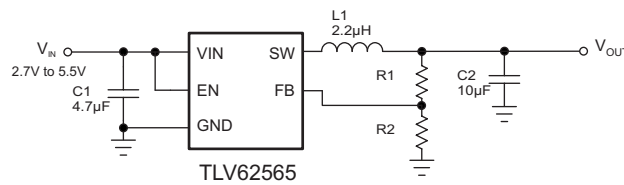


表 2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	4.7 $\mu$ F, Ceramic Capacitor, 6.3 V, X5R, size 0603, GRM188R60J475ME84	Murata
C2	10 $\mu$ F, Ceramic Capacitor, 6.3 V, X5R, size 0603, GRM188R60J106ME84	Murata
L1	2.2 $\mu$ H, Power Inductor, 2.5 A, size 4mmx4mm, LQH44PN2R2MP0	Murata
R1,R2	Chip resistor,1%,size 0603	Std.



## 10 Detailed Description

### 10.1 Overview

The TLV62565/6 device family includes two high-efficiency synchronous step-down converters. Each device operates with an adaptive on-time control scheme, which is able to dynamically adjust the on-time duration based on the input voltage and output voltage so that it can achieve relative constant frequency operation. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the  $V_{IN}/V_{OUT}$  ratio, a simple circuit sets the required on time for the high-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current. At the beginning of each switching cycle, the high-side switch is turned on and the inductor current ramps up to a peak current that is defined by on time and inductance. In the second phase, once the on time expires, the high-side switch is turned off while the low-side switch is being turned on. The current through the inductor then decays until triggering the valley current limit determined by the output of the error amplifier. Once this occurs, the on timer is set to turn the high-side switch back on again and the cycle is repeated.

The TLV62565/6 device family offers excellent load transient response with a unique fast response constant on-time valley current mode. The switching frequency changes during load transition so that the output voltage comes back in regulation faster than a traditional fixed PWM control scheme. 图 10 shows the operation principles of the load transient response of the TLV62565/6. Internal loop compensation is integrated which simplifies the design process while minimizing the number of external components. At light load currents the device automatically operates in Power Save Mode with pulse frequency modulation (PFM).

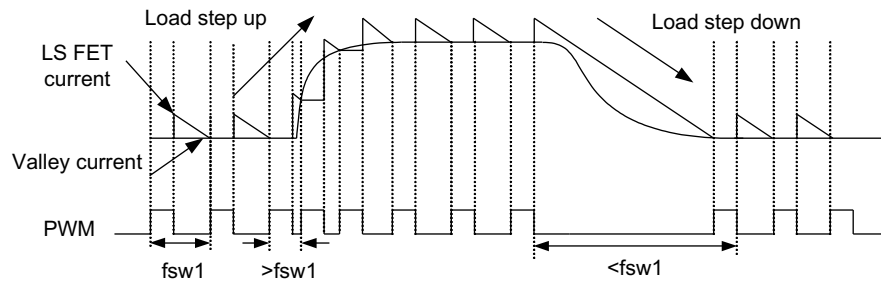


图 10. Operation in Load Transient

## 10.2 Functional Block Diagrams

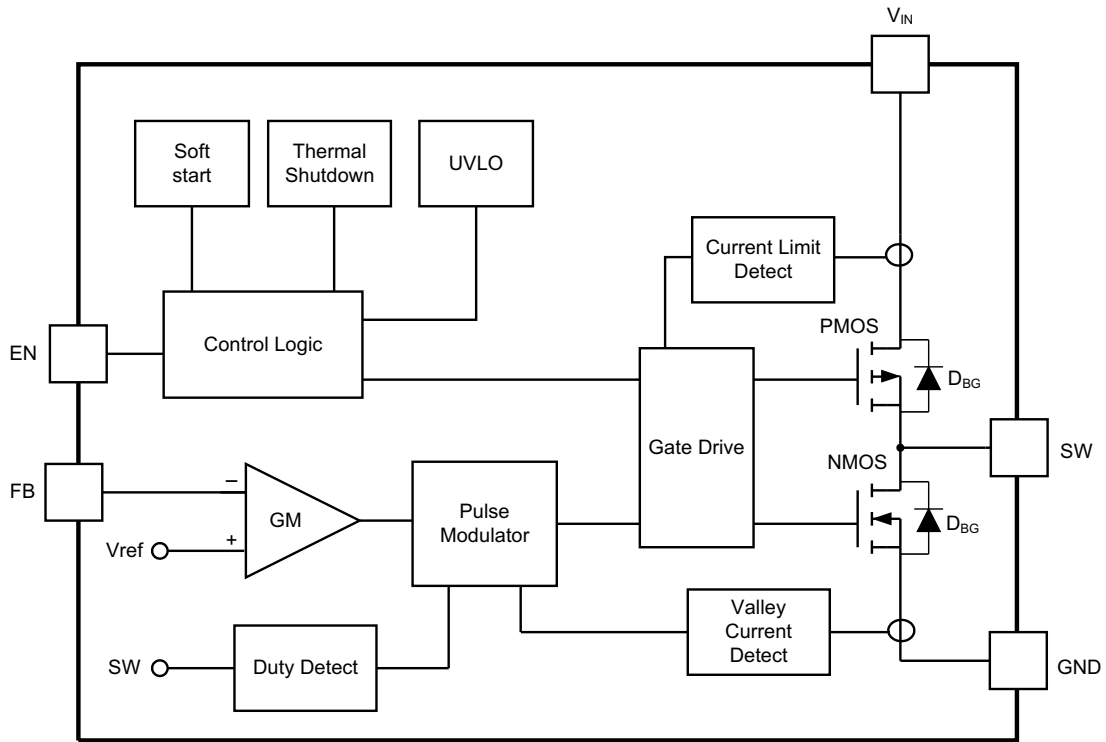


图 11. TLV62565 Functional Block Diagram

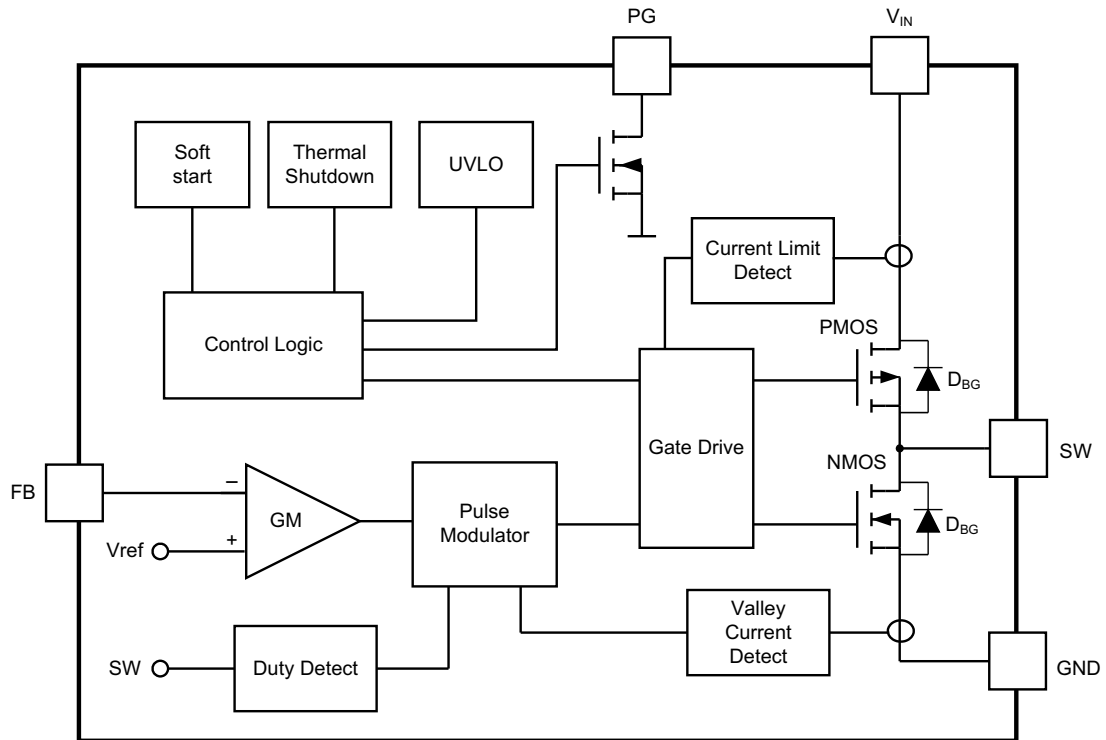


图 12. TLV62566 Functional Block Diagram

## 10.3 Feature Description

### 10.3.1 Power Save Mode

The device integrates a Power Save Mode with PFM to improve efficiency at light load. In Power Save Mode, the device only switches when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and stops switching when the output voltage is higher than the set threshold voltage. PFM is exited and PWM mode entered in case the output current can no longer be supported in Power Save Mode. The threshold of the PFM comparator is typically 0.9% higher than the normal reference voltage. 图 13 shows the details of PFM/PWM mode transition.

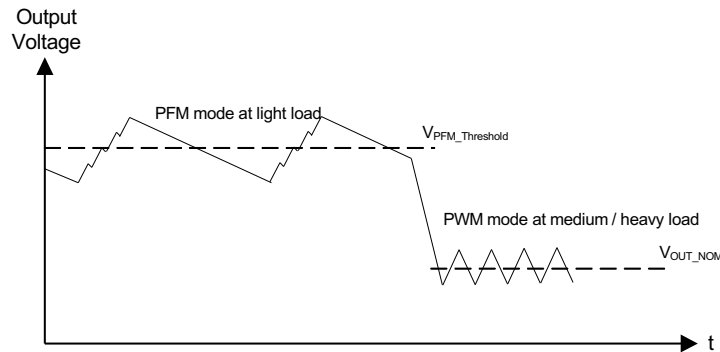


图 13. Output Voltage in PFM/PWM Mode

### 10.3.2 Enabling/Disabling the Device

The device is enabled by setting the EN input to a logic HIGH. Accordingly, a logic LOW disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

### 10.3.3 Soft Start

After enabling the device, internal soft-start circuitry monotonically ramps up the output voltage which reaches nominal output voltage during a soft-start time of 250  $\mu$ s (typical). This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

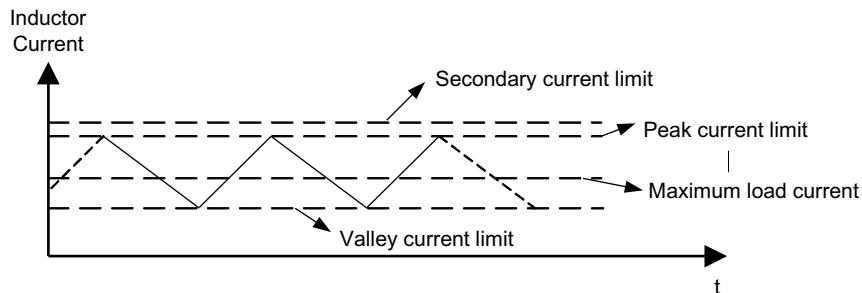
If the output voltage is not reached within the soft-start time, such as in the case of a heavy load, the converter enters regular operation. The TLV62565/6 are able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

### 10.3.4 Switch Current Limit

The switch current limit prevents the device from high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition.

The TLV62565/6 adopt valley current control by sensing the current of the low-side MOSFET. Once the low-side valley switch current limit is tripped, the low-side MOSFET is turned off and limits the inductor's valley current. The high-side current is also limited which is determined by the on time of the high-side MOSFET and inductor value calculated by 公式 1. For example, with 3.6  $V_{IN}$  to 1.8  $V_{OUT}$  and 2.2- $\mu$ H specification, the peak current limit is approximately 1.97 A with a typical valley current limit of 1.7 A.

Additionally, there is a secondary high-side current limit (typical 2 A) to prevent the current from going too high, which is shown in 图 14. Due to the internal propagation delay, the real current limit value might be higher than the static current limit in the electrical characteristics table.

**Feature Description (接下页)**

**图 14. Switch Current Limit**

$$I_{PEAK,LIMIT} = I_{VALLEY,LIMIT} + \Delta I_L$$

$$\Delta I_L = \frac{V_{OUT}}{L} \times \frac{(1-D)}{f_{SW}}$$

where:

- $I_{PEAK,LIMIT}$  is the high-side peak current limit
- $I_{VALLEY,LIMIT}$  is the low-side valley current limit

(1)

**10.3.5 Power Good**

The TLV62566 integrates a Power Good output going low when the output voltage is below its nominal value. The Power Good output stays high impedance once the output is above 95% of the regulated voltage and is low once the output voltage falls below typically 90% of the regulated voltage. The PG pin is an open drain output and is specified to sink typically up to 0.5 mA. The Power Good output requires a pull-up resistor connected to any voltage lower than 5.5 V. When the device is off due to UVLO or thermal shutdown, the PG pin is pulled to logic low.

**10.4 Device Functional Modes**
**10.4.1 Under Voltage Lockout**

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than  $V_{UVLO}$  with  $V_{HYS\_UVLO}$  hysteresis.

**10.4.2 Thermal Shutdown**

The device enters thermal shutdown once the junction temperature exceeds typically  $T_{JSD}$ . Once the device temperature falls below the threshold with hysteresis, the device returns to normal operation automatically. Power Good is pulled low when thermal protection is triggered.

## 11 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 11.1 Application Information

The TLV6256x devices are synchronous step-down converters optimized for small solution size and high efficiency. The devices integrate switches capable of delivering an output current up to 1.5 A.

### 11.2 Typical Application

TLV62565 2.7-V to 5.5-V input, 1.2-V output converter.

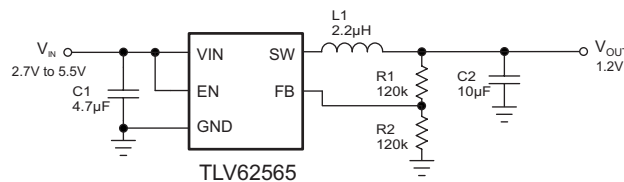


图 15. TLV62565 1.2-V Output Application

#### 11.2.1 Design Requirements

##### 11.2.1.1 Output Filter Design

The inductor and output capacitor together provide a low-pass frequency filter. To simplify this process, 表 3 outlines possible inductor and capacitor value combinations.

表 3. Matrix of Output Capacitor and Inductor Combinations

L [ $\mu$ H] <sup>(1)</sup>	C <sub>OUT</sub> [ $\mu$ F] <sup>(2) (3)</sup>				
	4.7	10	22	47	100
1					
2.2		+ <sup>(4)</sup>	+ <sup>(4)</sup>	+ <sup>(4)</sup>	
4.7					

- (1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
- (2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.
- (3) For low output voltage applications ( $\leq 1.2$  V), more output capacitance is recommended (usually  $\geq 22$   $\mu$ F) for smaller ripple.
- (4) Typical application configuration. '+' indicates recommended filter combinations.

### 11.2.1.2 Inductor Selection

The main parameters for inductor selection is inductor value and then saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 公式 2 is given:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where:

- $I_{OUT,MAX}$  is the maximum output current
- $\Delta I_L$  is the inductor current ripple
- $f_{SW}$  is the switching frequency
- $L$  is the inductor value

(2)

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than  $I_{L,MAX}$ . In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. The recommended inductors are listed in 表 4.

**表 4. List of Recommended Inductors**

INDUCTANCE [μH]	CURRENT RATING [mA]	DIMENSIONS L x W x H [mm <sup>3</sup> ]	DC RESISTANCE [mΩ typ]	TYPE	MANUFACTURER
2.2	2500	4 x 3.7 x 1.65	49	LQH44PN2R2MP0	Murata
2.2	3000	4 x 4 x 1.8	50	NRS4018T2R2MDGJ	Taiyo Yuden

### 11.2.1.3 Input and Output Capacitor Selection

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. The closer the input capacitor is placed to the  $V_{IN}$  and GND pins, the lower the switch ring. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 4.7-μF input capacitance is sufficient; a larger value reduces input voltage ripple.

The architecture of the TLV62565/6 allow use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. The TLV62565/6 are designed to operate with an output capacitance of 10 μF to 47 μF, as outlined in 表 3.

## 11.2.2 Detailed Design Procedure

### 11.2.2.1 Setting the Output Voltage

An external resistor divider is used to set output voltage. By selecting R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is  $V_{FB}$ . [公式 3](#), [公式 4](#), and [公式 5](#) can be used to calculate R1 and R2.

When sizing R2, in order to achieve low quiescent current and acceptable noise sensitivity, use a minimum of 5  $\mu$ A for the feedback current  $I_{FB}$ . Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

$$R2 = \frac{V_{FB}}{I_{FB}} = \frac{0.6V}{5\mu A} = 120k\Omega \quad (4)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1\right) \quad (5)$$

### 11.2.2.2 Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current,  $I_L$
- Output ripple voltage,  $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination. Applications with the recommended L-C combinations in [表 3](#) are designed for good loop stability as well as fast load transient response.

As a next step in the evaluation of the regulation loop, the load transient response is illustrated. The TLV62565/6 use a constant on time with valley current mode control, so the on time of the high-side MOSFET is relatively consistent from cycle to cycle when a load transient occurs. Whereas the off time adjusts dynamically in accordance with the instantaneous load change and brings  $V_{OUT}$  back to the regulated value.

During recovery time,  $V_{OUT}$  can be monitored for settling time, overshoot, or ringing which helps judge the stability of the converter. Without any ringing, the loop usually has more than 45° of phase margin.

11.2.3 Application Performance Curves

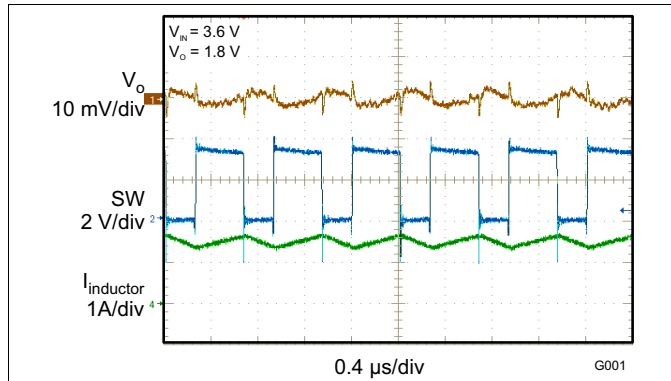


图 16. Typical Application (PWM Mode)

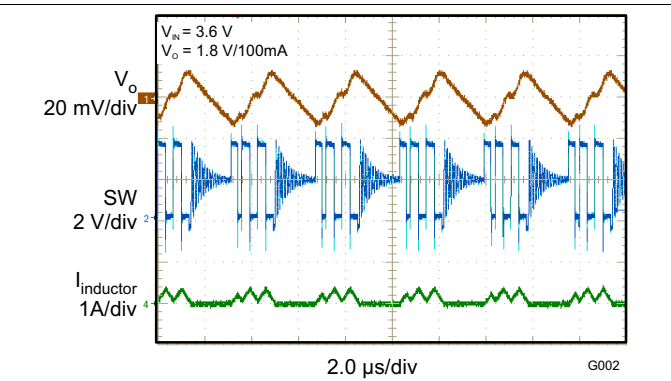


图 17. Typical Application (PFM Mode)

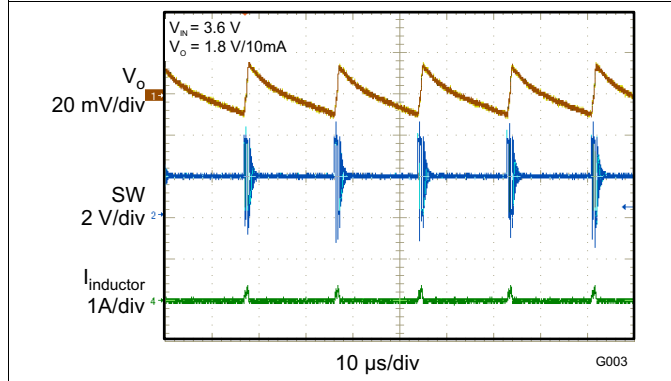


图 18. Typical Application (PFM Mode)

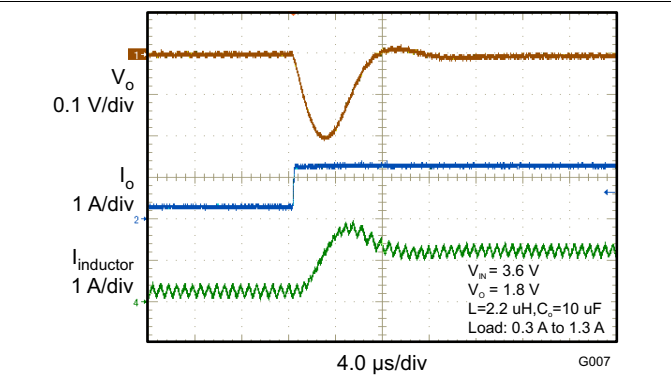


图 19. Load Transient

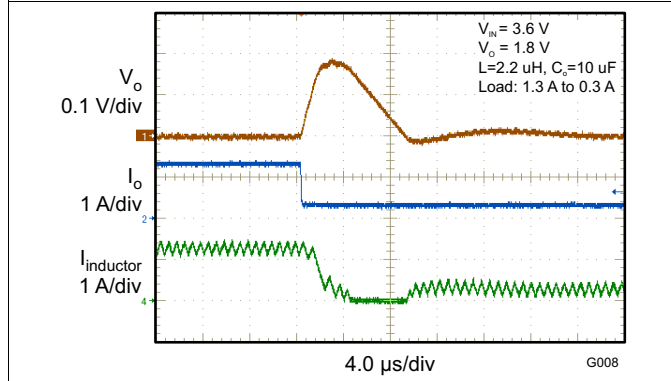


图 20. Load Transient

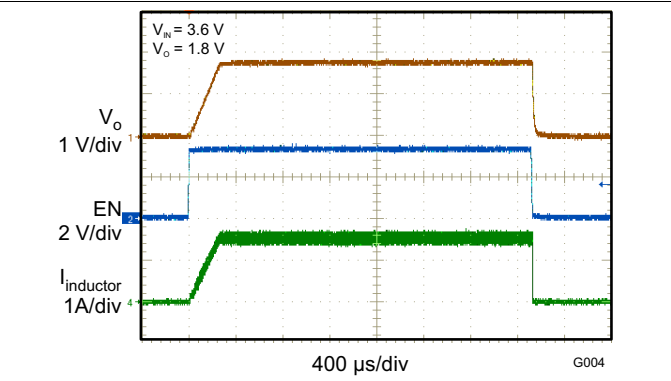
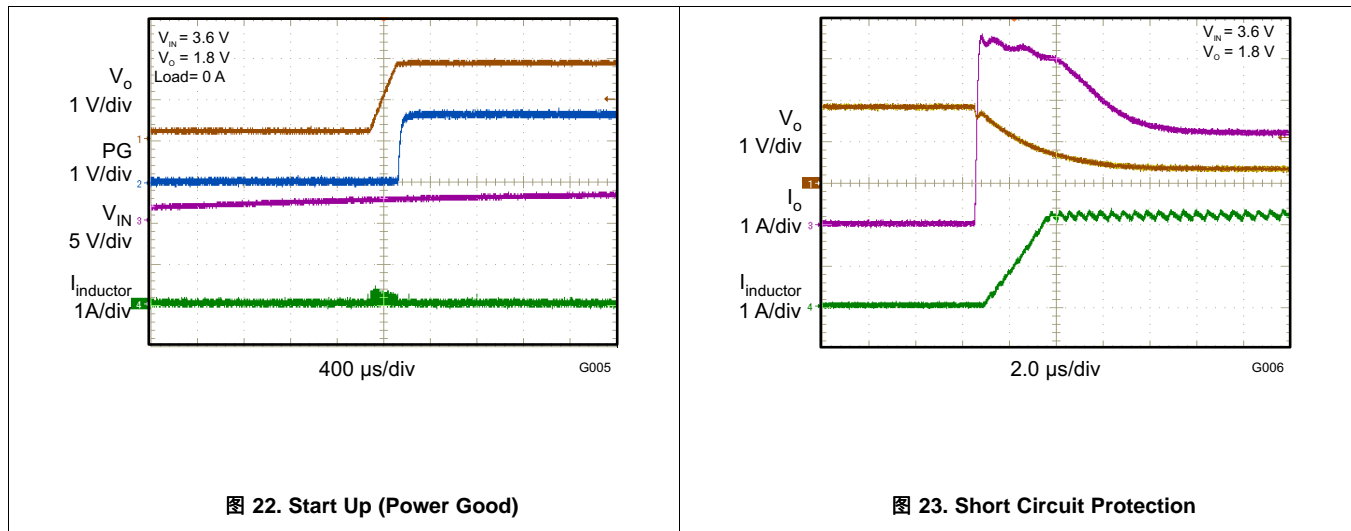


图 21. Start Up





## 12 Power Supply Recommendations

The power supply to the TLV62565 and TLV62566 needs to have a current rating according to the supply voltage, output voltage and output current of the TLV62565 and TLV62566.

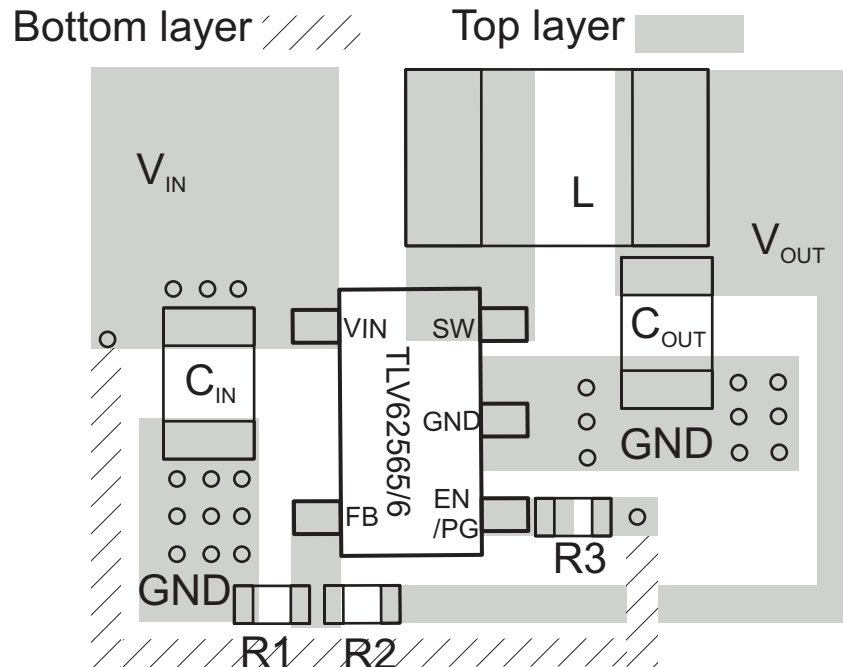
## 13 Layout

### 13.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TLV62565 devices.

- The input/output capacitors and the inductor should be placed as close as possible to the IC.
- This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance.
- A common power GND should be used.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB is a signal trace .
- Special care should be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small.
- GND layers might be used for shielding.
- Keep these traces away from SW nodes .

### 13.2 Layout Example



Note: PG connected to VIN via R3, EN direct connect to VIN

图 24. TLV62565 Layout

### 13.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes [SZZA017](#) and [SPRA953](#).

## 14 器件和文档支持

### 14.1 器件支持

#### 14.1.1 第三方产品免责声明

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### 14.2 文档支持

#### 14.2.1 相关文档

应用报告《半导体和 IC 封装热指标》（文件编号：[SPRA953](#)）

应用报告《采用 JEDEC PCB 设计的线性 and 逻辑封装散热特性》（文件编号：[SZZA017](#)）

### 14.3 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 5. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TLV62565	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
TLV62566	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 14.4 商标

All trademarks are the property of their respective owners.

### 14.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 14.6 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

## 15 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62565DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	SIK	<a href="#">Samples</a>
TLV62565DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	SIK	<a href="#">Samples</a>
TLV62566DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	SIL	<a href="#">Samples</a>
TLV62566DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	SIL	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62565DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62565DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62565DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV62565DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62565DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62566DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62566DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62566DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62566DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62565DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62565DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62565DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV62565DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV62565DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV62566DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62566DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62566DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV62566DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0





# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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