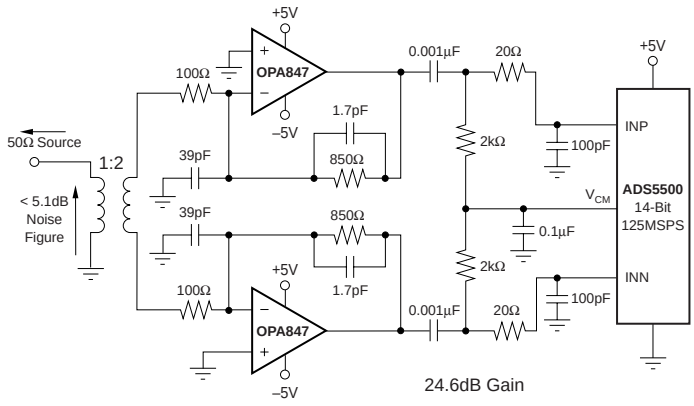
Wideband, Ultra-Low Noise, Voltage-Feedback OPERATIONAL AMPLIFIER with Shutdown

FEATURES

- HIGH GAIN BANDWIDTH: 3.9GHz
- LOW INPUT VOLTAGE NOISE: 0.85nV/$\sqrt{Hz}$
- VERY LOW DISTORTION: –105dBc (5MHz)
- HIGH SLEW RATE: 950V/µs
- HIGH DC ACCURACY: V_{IO} < ±100µV
- LOW SUPPLY CURRENT: 18.1mA
- LOW SHUTDOWN POWER: 2mW
- STABLE FOR GAINS ≥ 12

APPLICATIONS

- HIGH DYNAMIC RANGE ADC PREAMPS
- LOW NOISE, WIDEBAND, TRANSIMPEDANCE AMPLIFIERS
- WIDEBAND, HIGH GAIN AMPLIFIERS
- LOW NOISE DIFFERENTIAL RECEIVERS
- ULTRASOUND CHANNEL AMPLIFIERS
- IMPROVED UPGRADE FOR THE OPA687, CLC425, AND LMH6624



Ultra-High Dynamic Range Differential ADC Driver

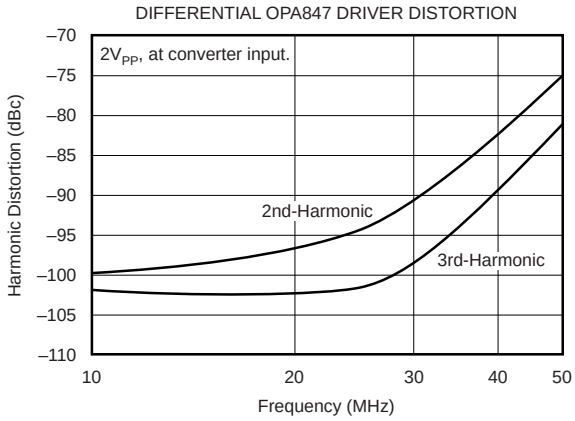
DESCRIPTION

The OPA847 combines very high gain bandwidth and large signal performance with an ultra-low input noise voltage (0.85nV/$\sqrt{Hz}$) while using only 18mA supply current. Where power saving is critical, the OPA847 also includes an optional power shutdown pin that, when pulled low, disables the amplifier and decreases the supply current to < 1% of the powered-up value. This optional feature may be left disconnected to ensure normal amplifier operation when no power-down is required.

The combination of very low input voltage and current noise, along with a 3.9GHz gain bandwidth product, make the OPA847 an ideal amplifier for wideband transimpedance applications. As a voltage gain stage, the OPA847 is optimized for a flat frequency response at a gain of +20V/V and is stable down to gains as low as +12V/V. New external compensation techniques allow the OPA847 to be used at any inverting gain with excellent frequency response control. Using this technique in a differential Analog-to-Digital Converter (ADC) interface application, shown below, can deliver one of the highest dynamic-range interfaces available.

OPA847 RELATED PRODUCTS

SINGLES	INPUT NOISE VOLTAGE (nV/$\sqrt{Hz}$)	GAIN BANDWIDTH PRODUCT (MHz)
OPA842	2.6	200
OPA843	2.0	800
OPA846	1.2	1750



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	$\pm 6.5 V_{DC}$
Internal Power Dissipation	See Thermal Analysis Section
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: D, DBV	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating (Human Body Model)	1500V
(Charge Device Model)	1500V
(Machine Model)	100V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

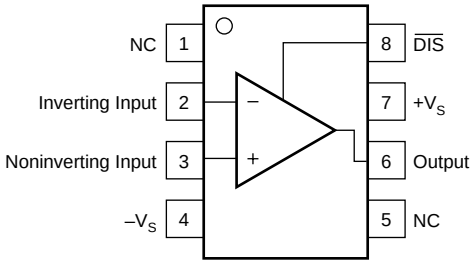
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA847	SO-8	D	–40°C to +85°C	OPA847	OPA847ID	Rails, 100
"	"	"	"	"	OPA847IDR	Tape and Reel, 2500
OPA847	SOT23-6	DBV	–40°C to +85°C	OATI	OPA847IDBVT	Tape and Reel, 250
"	"	"	"	"	OPA847IDBVR	Tape and Reel, 3000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI web site at www.ti.com.

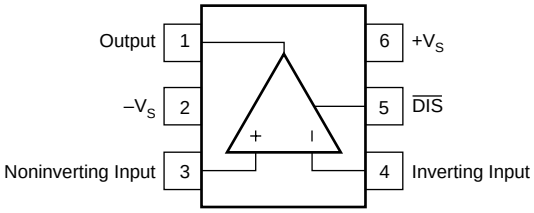
PIN CONFIGURATIONS

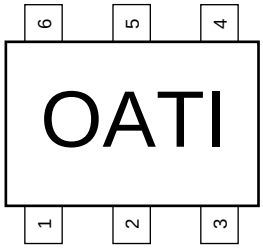
Top View **SO**



NC = No Connection

Top View **SOT**





Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

$R_L = 100\Omega$, $R_F = 750\Omega$, $R_G = 39.2\Omega$, and G = +20 (see Figure 1 for AC performance only), unless otherwise noted.

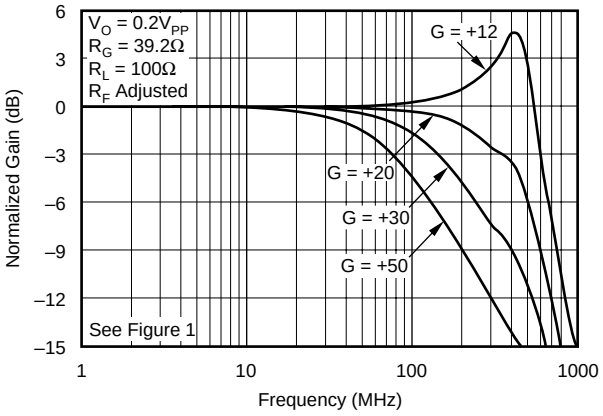
PARAMETER	CONDITIONS	OPA847ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 1)								
Closed-Loop Bandwidth	G = +12, R_G = 39.2Ω, V_O = 200mV_{PP}	600				MHz	typ	C
	G = +20, R_G = 39.2Ω, V_O = 200mV_{PP}	350	230	210	195	MHz	min	B
	G = +50, R_G = 39.2Ω, V_O = 200mV_{PP}	78	63	60	57	MHz	min	B
Gain Bandwidth Product (GBP)	G ≥ +50	3900	3100	3000	2800	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +20, R_L = 100Ω	60	40	35	30	MHz	min	B
Peaking at a Gain of +12		4.5	7	10	12	dB	max	B
Harmonic Distortion	G = +20, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	–74	–70	–69	–68	dBc	max	B
	R_L = 500Ω	–105	–90	–89	–88	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–103	–96	–91	–88	dBc	max	B
	R_L = 500Ω	–110	–105	–100	–90	dBc	max	B
2-Tone, 3rd-Order Intercept	G = +20, f = 20MHz	39	37	36	35	dBm	min	B
Input Voltage Noise Density	f > 1MHz	0.85	0.92	0.98	1.0	nV/$\sqrt{Hz}$	max	B
Input Current Noise Density	f > 1MHz	2.5	3.5	3.6	3.7	pA/$\sqrt{Hz}$	max	B
Pulse Response								
Rise-and-Fall Time	0.2V Step	1.2	1.75	2.0	2.2	ns	max	B
Slew Rate	2V Step	950	700	625	535	V/µs	min	B
Settling Time to 0.01%	2V Step	20				ns	typ	C
0.1%	2V Step	10	12	14	18	ns	max	B
1%	2V Step	6	8	10	12	ns	max	B
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V	98	**90**	89	88	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.1	**±0.5**	±0.58	±0.60	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V	±0.25	±0.25	±1.5	±1.5	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	–19	**–39**	–41	–42	µA	max	A
Input Bias Current Drift (magnitude)	V_{CM} = 0V	–15	–15	–40	–70	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.1	**±0.6**	±0.7	±0.85	µA	max	A
Input Offset Current Drift	V_{CM} = 0V	±0.1	±0.1	±2	±3.5	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)(5)		±3.3	**±3.1**	±3.0	±2.9	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±0.5V, Input-Referred	110	**95**	93	90	dB	min	A
Input Impedance								
Differential	V_{CM} = 0V	2.7 || 2.0				kΩ || pF	typ	C
Common-Mode	V_{CM} = 0V	2.3 || 1.7				MΩ || pF	typ	C
OUTPUT								
Output Voltage Swing	≥ 400Ω Load	±3.5	**±3.3**	±3.1	±3.0	V	min	A
	100Ω Load	±3.4	**±3.2**	±3.0	±2.9	V	min	A
Current Output, Sourcing	V_O = 0V	100	**60**	56	52	mA	min	A
Current Output, Sinking	V_O = 0V	–75	**–60**	–56	–52	mA	min	A
Closed-Loop Output Impedance	G = +20, f = < 100kHz	0.003				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage		±6	**±6**	±6	±6	V	max	A
Maximum Quiescent Current	V_S = ±5V	18.1	**18.4**	18.7	18.9	mA	max	A
Minimum Quiescent Current	V_S = ±5V	18.1	**17.8**	17.5	17.1	mA	min	A
Power-Supply Rejection Ratio								
+PSRR, –PSRR	|V_S| = 4.5V to 5.5V, Input-Referred	100	**95**	93	90	dB	min	A
POWER-DOWN (disabled low)	(Pin 8 on SO-8; Pin 5 on SOT23-6)							
Power-Down Quiescent Current (+V_S)		–200	**–270**	–320	–370	µA	max	A
On Voltage (enabled high or floated)		3.5	**3.75**	3.85	3.95	V	min	A
Off Voltage (disabled asserted low)		1.8	**1.7**	1.6	1.5	V	max	A
Power-Down Pin Input Bias Current	($V_{\overline{DIS}}$ = 0)	150	**190**	200	210	µA	max	A
Power-Down Time		200				ns	typ	C
Power-Up Time		60				ns	typ	C
Off Isolation	5MHz, Input to Output	70				dB	typ	C
THERMAL								
Specification ID, IDBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DBV SOT23		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C specifications. (2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +23°C at high temperature limit for over temperature specifications. (3) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out of node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

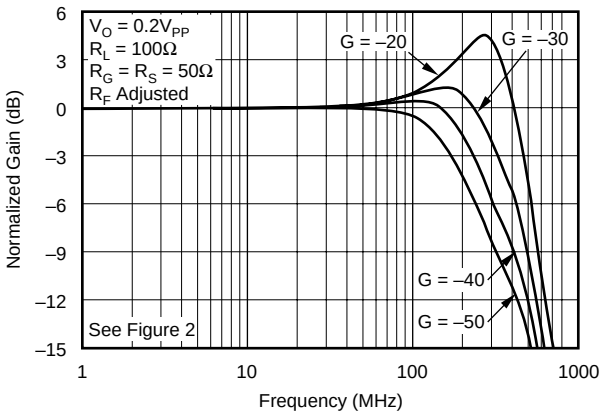
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

T_A = 25°C, G = +20V/V, R_G = 39.2Ω, and R_L = 100Ω, unless otherwise noted.

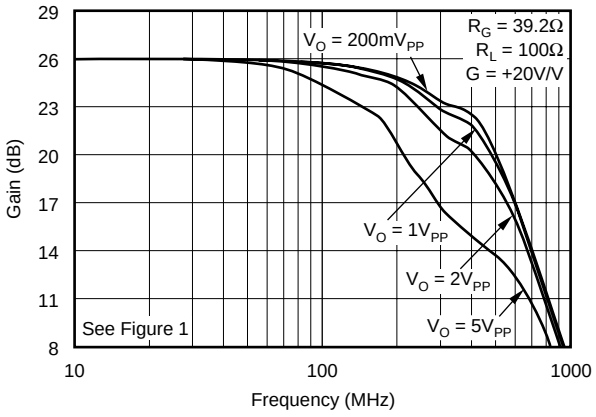
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



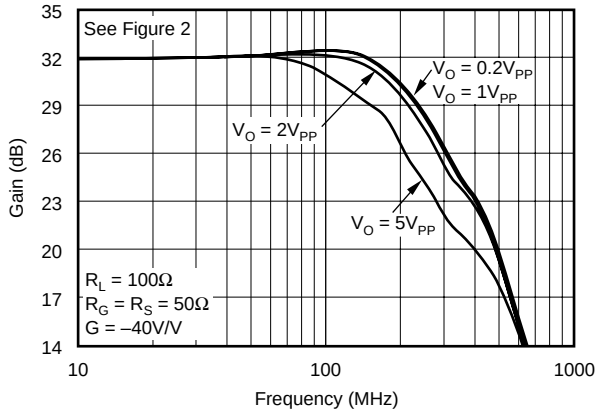
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



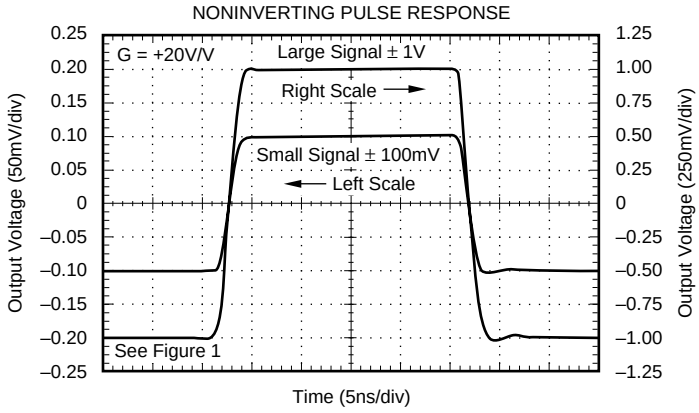
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



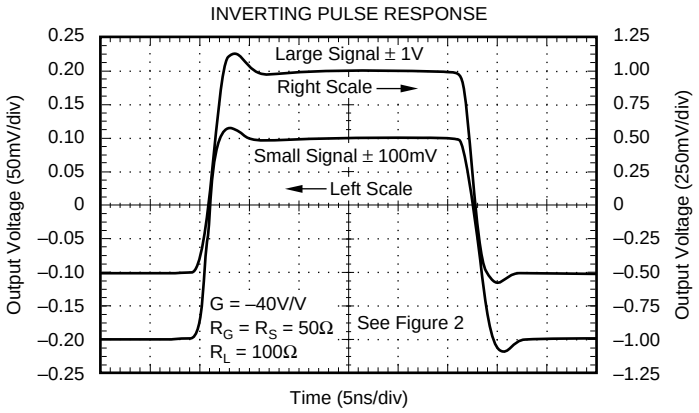
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



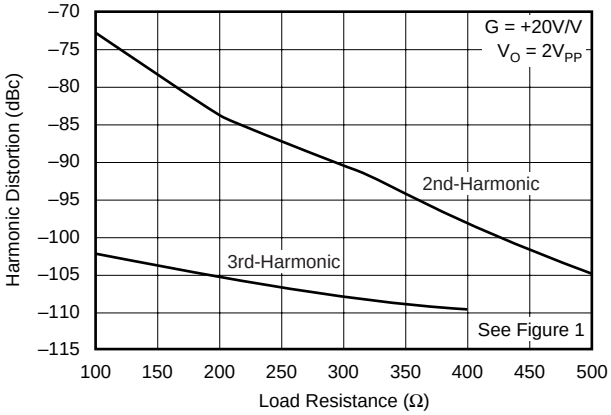
INVERTING PULSE RESPONSE



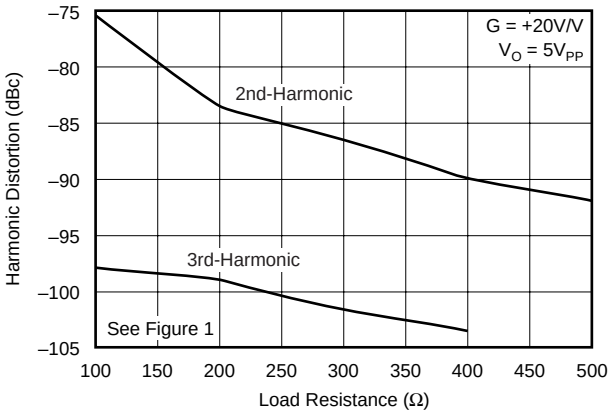
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

$T_A = 25°C$, G = +20V/V, $R_G = 39.2\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

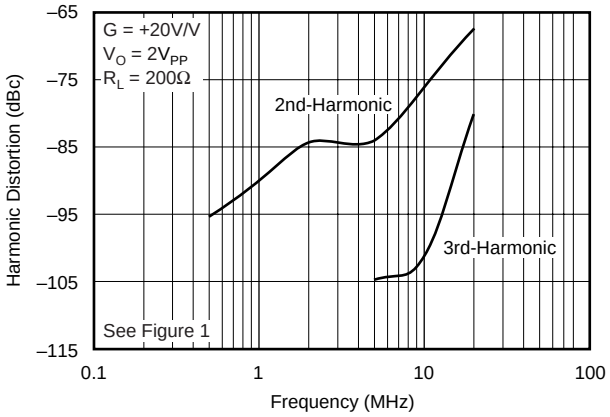
5MHz HARMONIC DISTORTION vs LOAD RESISTANCE



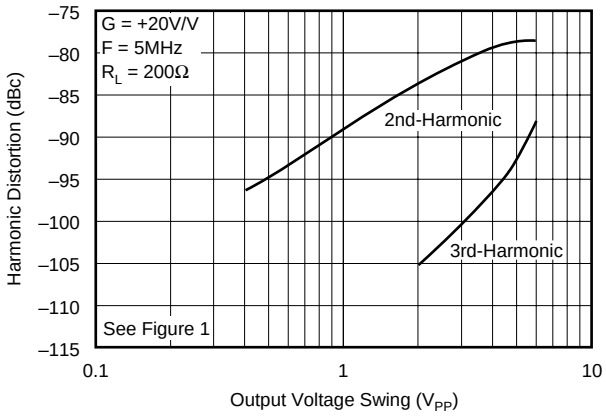
1MHz HARMONIC DISTORTION vs LOAD RESISTANCE



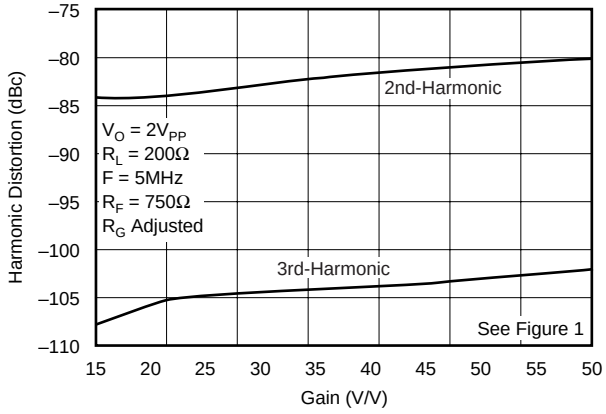
HARMONIC DISTORTION vs FREQUENCY



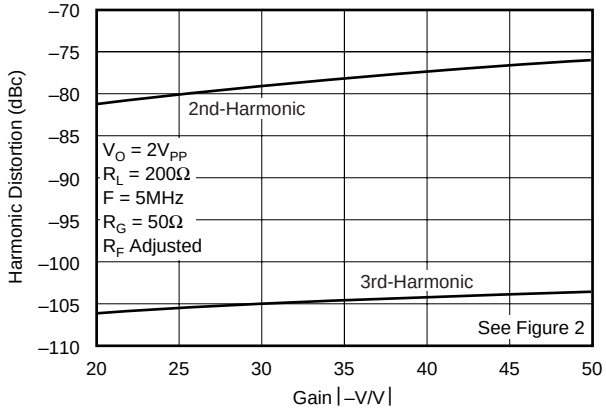
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



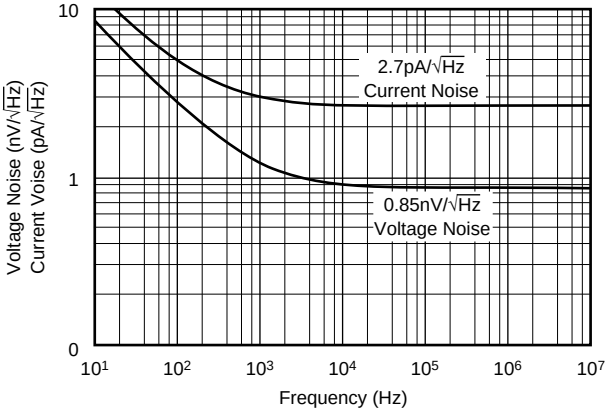
HARMONIC DISTORTION vs INVERTING GAIN



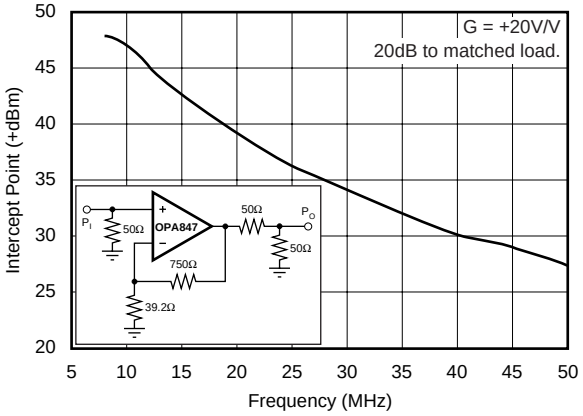
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

$T_A = 25°C$, G = +20V/V, $R_G = 39.2\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

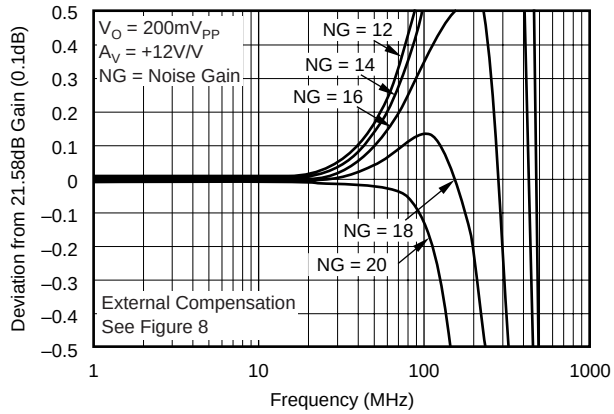
INPUT VOLTAGE AND CURRENT NOISE



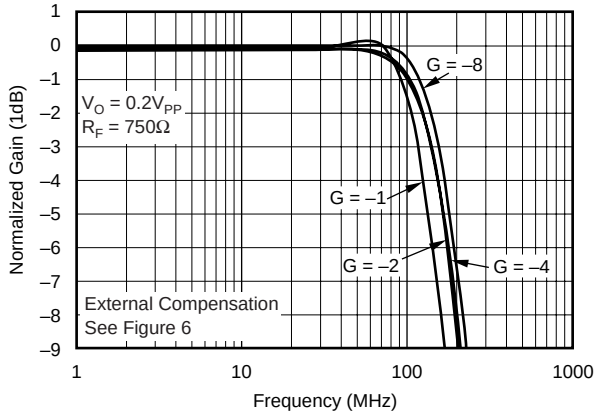
2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT



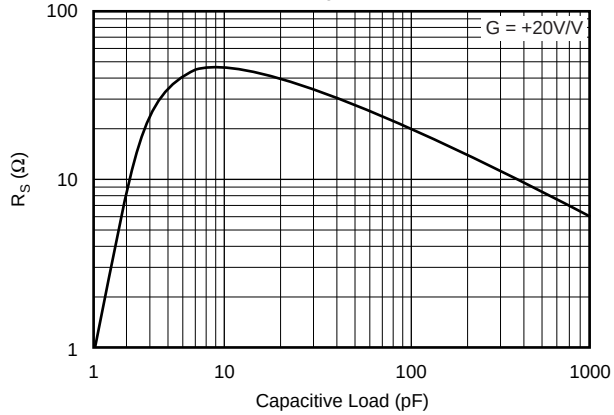
NONINVERTING GAIN FLATNESS TUNE



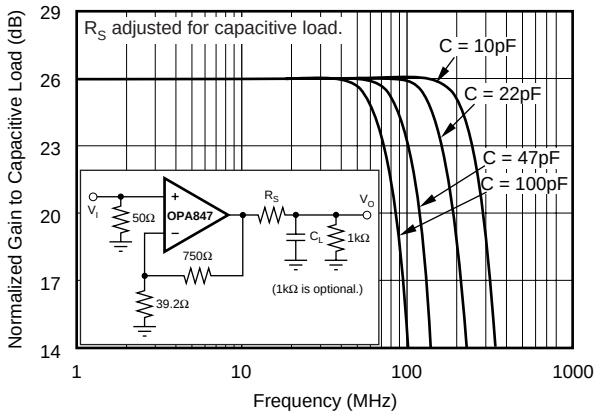
LOW GAIN INVERTING BANDWIDTH



RECOMMENDED R_S vs CAPACITIVE LOAD



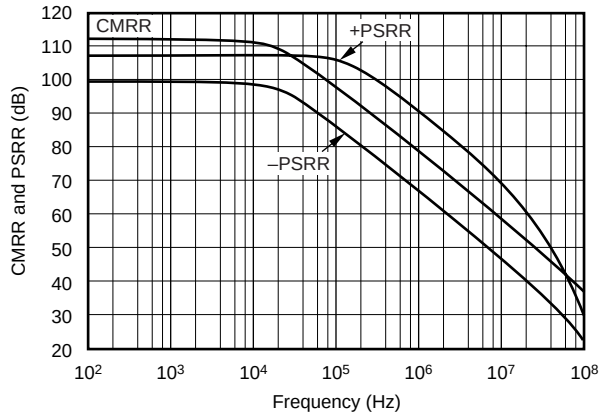
FREQUENCY RESPONSE vs CAPACITIVE LOAD



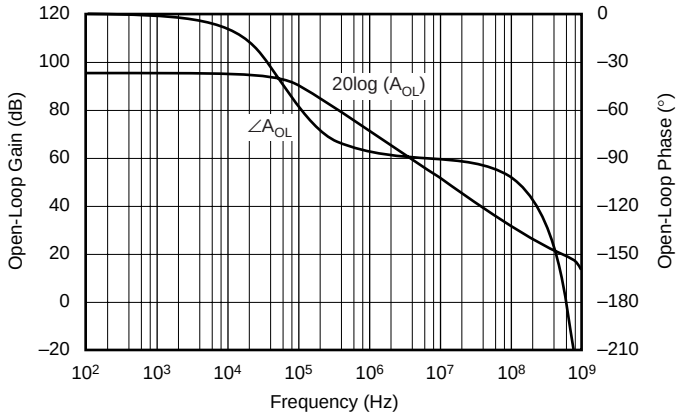
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

$T_A = 25°C$, G = +20V/V, $R_G = 39.2\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

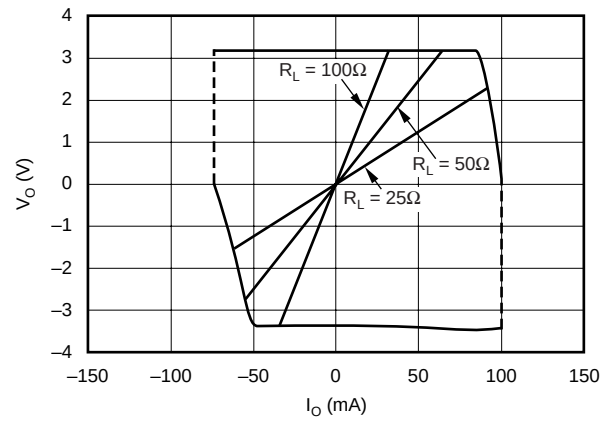
COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs FREQUENCY



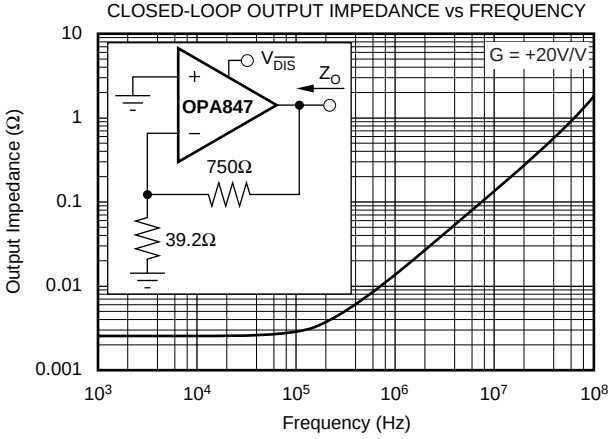
OPEN-LOOP GAIN AND PHASE



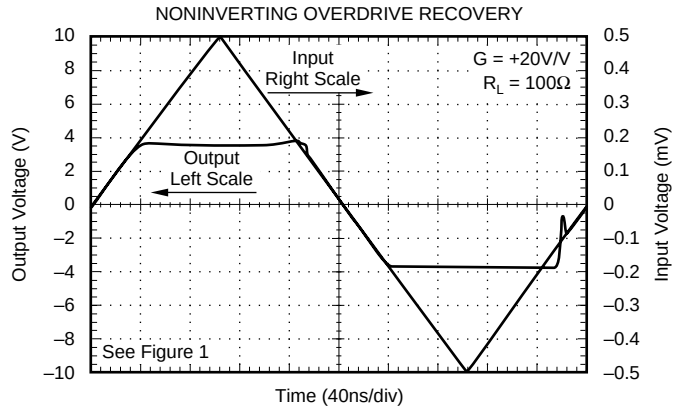
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



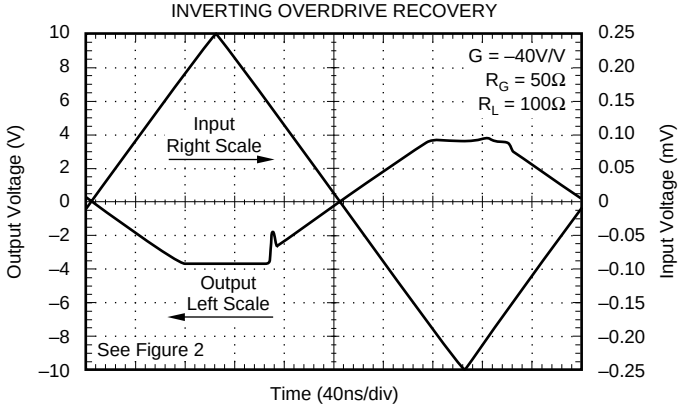
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



NONINVERTING OVERDRIVE RECOVERY



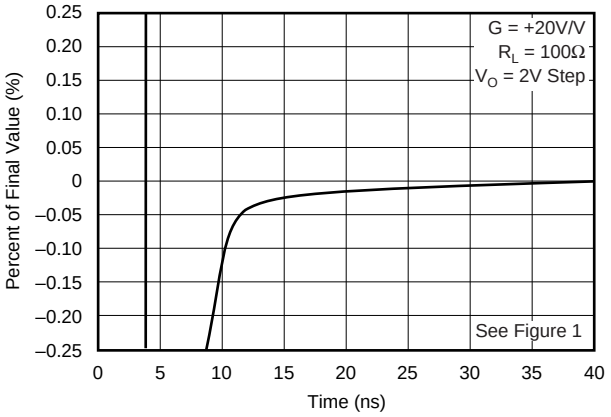
INVERTING OVERDRIVE RECOVERY



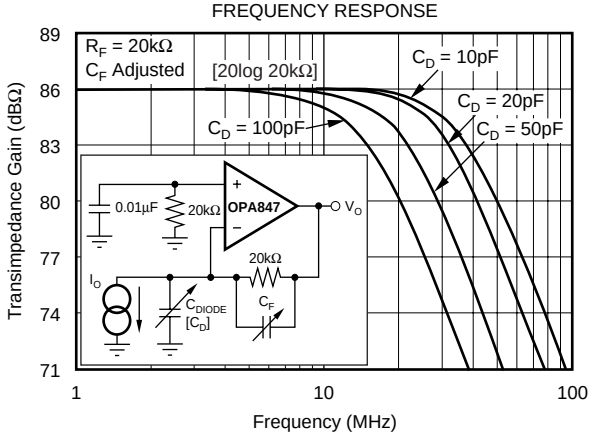
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

$T_A = 25°C$, G = +20V/V, $R_G = 39.2\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

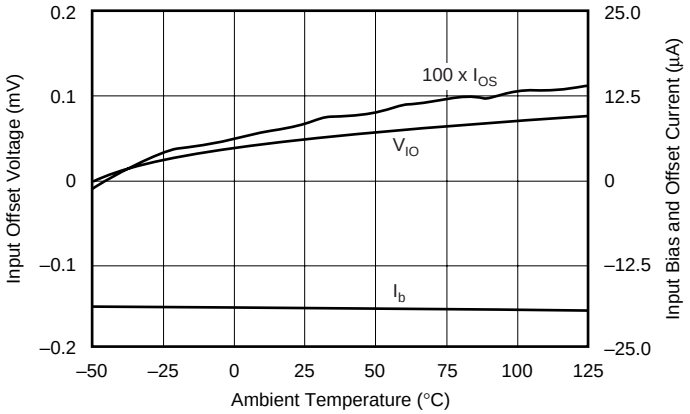
SETTLING TIME



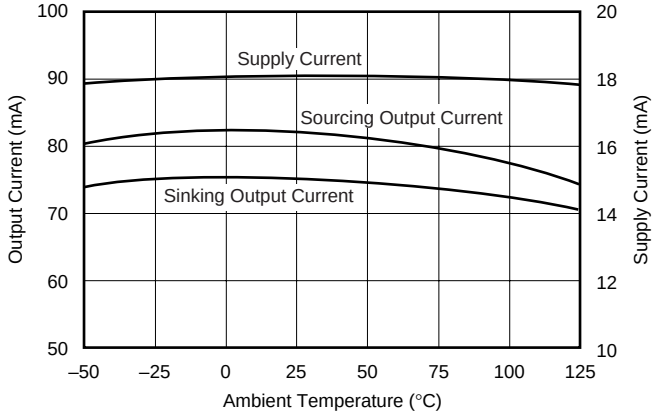
PHOTODIODE TRANSIMPEDANCE FREQUENCY RESPONSE



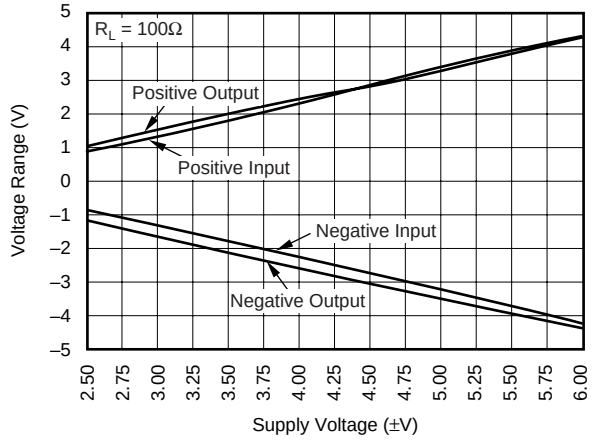
TYPICAL DC DRIFT OVER TEMPERATURE



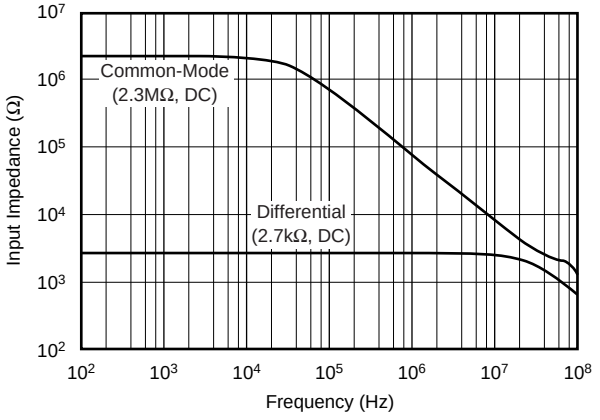
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



COMMON-MODE INPUT RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE



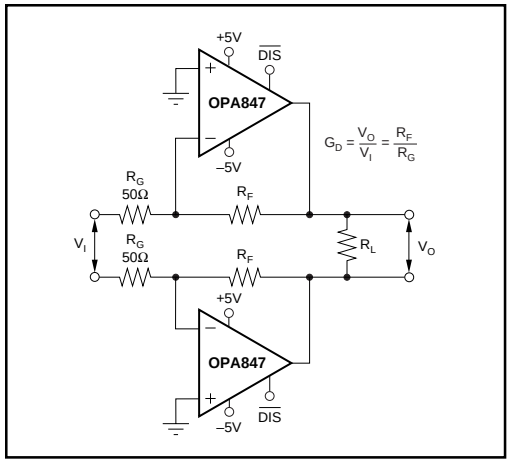
COMMON-MODE AND DIFFERENTIAL INPUT IMPEDANCE



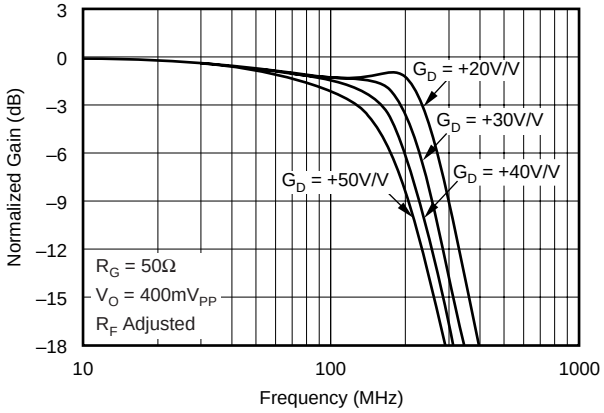
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

$T_A = 25°C$, $G_D = 40V/V$, $R_G = 50\Omega$, and $R_L = 400\Omega$, unless otherwise noted.

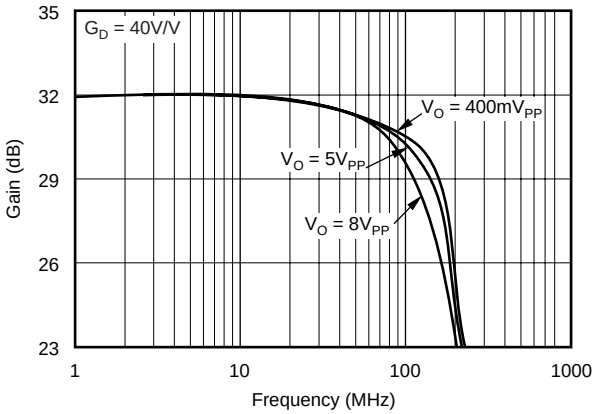
DIFFERENTIAL PERFORMANCE TEST CIRCUIT



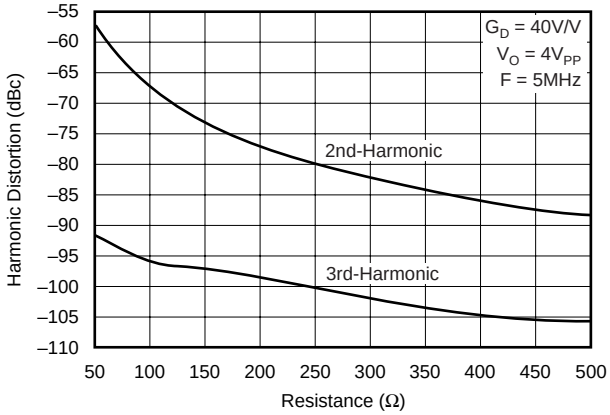
DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE



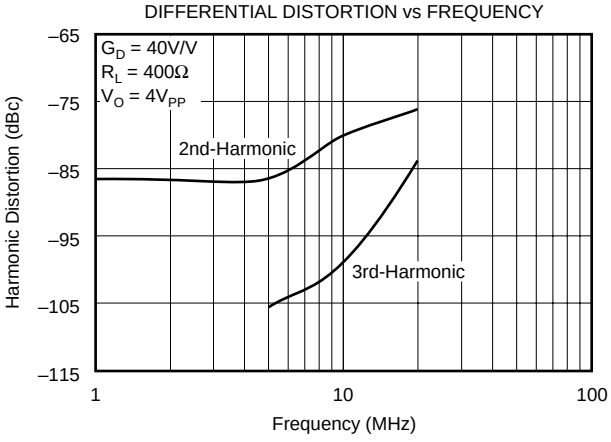
DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE



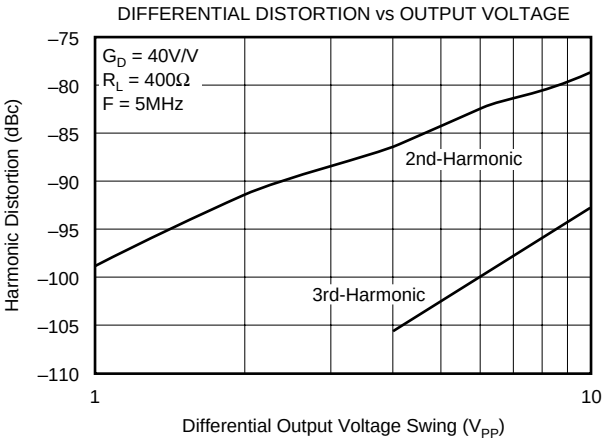
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



APPLICATIONS INFORMATION

WIDEBAND, NONINVERTING OPERATION

The OPA847 provides a unique combination of a very low input voltage noise along with a very low distortion output stage to give one of the highest dynamic range op amps available. Its very high gain bandwidth product (GBP) can be used to either deliver high signal bandwidths at high gains, or to deliver very low distortion signals at moderate frequencies and lower gains. To achieve the full performance of the OPA847, careful attention to PC board layout and component selection is required, as discussed in the following sections of this data sheet.

Figure 1 shows the noninverting gain of a +20V/V circuit used as the basis for most of the Typical Characteristics. Most of the curves are characterized using signal sources with a 50Ω driving impedance and with measurement equipment presenting a 50Ω load impedance. In Figure 1, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in Figure 1) while output power specifications are at the matched 50Ω load. The total 100Ω load at the output combined with the 790Ω total feedback network load presents the OPA847 with an effective output load of 89Ω for the circuit of Figure 1.

Voltage-feedback op amps, unlike current-feedback designs, can use a wide range of resistor values to set their gain. The circuit of Figure 1, and the specifications at other gains, use an R_G set to 39.2Ω and R_F adjusted to get the desired gain. Using this guideline ensures that the noise added at the output due to the Johnson noise of the resistors does not significantly increase the total over that due to the 0.85nV/√Hz input voltage noise for the op amp itself. This R_G is suggested as a good starting point for design. Other values are certainly acceptable, if required by the design.

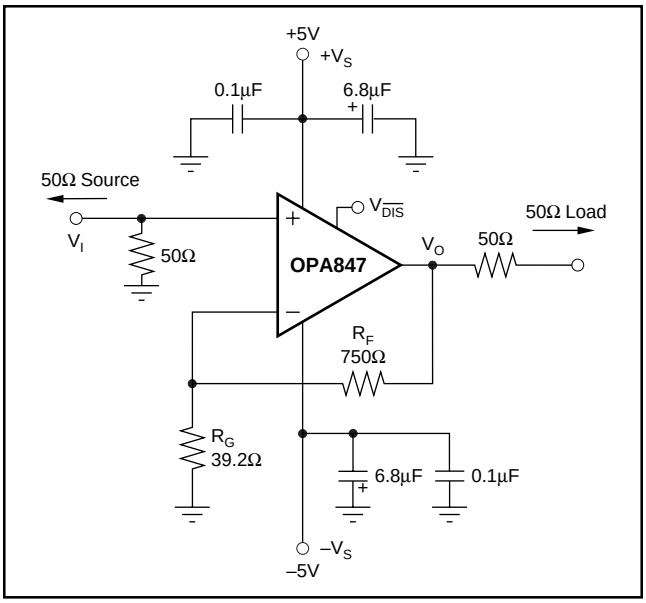


FIGURE 1. Noninverting G = +20 Specification and Test Circuit.

WIDEBAND, INVERTING GAIN OPERATION

There can be significant benefits to operating the OPA847 as an inverting amplifier. This is particularly true when a matched input impedance is required. Figure 2 shows the inverting gain of a –40V/V circuit used as a starting point for the Typical Characteristics showing inverting mode performance.

Driving this circuit from a 50Ω source, and constraining the gain resistor (R_G) to equal 50Ω, gives both a signal bandwidth and a noise advantage. R_G, in this case, acts as both the input termination resistor and the gain setting resistor for the circuit. Although the signal gain for the circuit of Figure 2 is double that for Figure 1, their noise gains are nearly equal when the 50Ω source resistor is included. This has the interesting effect of approximately doubling the equivalent GBP for the amplifier. This can be seen by observing that the gain of –40 bandwidth of 240MHz shown in the Typical Characteristics implies a gain bandwidth product of 9.6GHz, giving a far higher bandwidth at a gain of –40 than at a gain of +40. While the signal gain from R_G to the output is –40, the noise gain for bandwidth setting purposes is $1 + R_F/(2 \bullet R_G)$. In the case of a –40V/V gain, using an $R_G = R_S = 50\Omega$ gives a noise gain = 1 + 2kΩ/100Ω = 21. This inverting gain of –40V/V therefore has a frequency response that more closely matches the gain of a +20 frequency response.

If the signal source is actually the low impedance output of another amplifier, R_G should be increased to be greater than the minimum value allowed at the output for that amplifier and R_F adjusted to get the desired gain. It is critical for stable operation of the OPA847 that this driving amplifier show a very low output impedance through frequencies exceeding the expected closed-loop bandwidth for the OPA847.

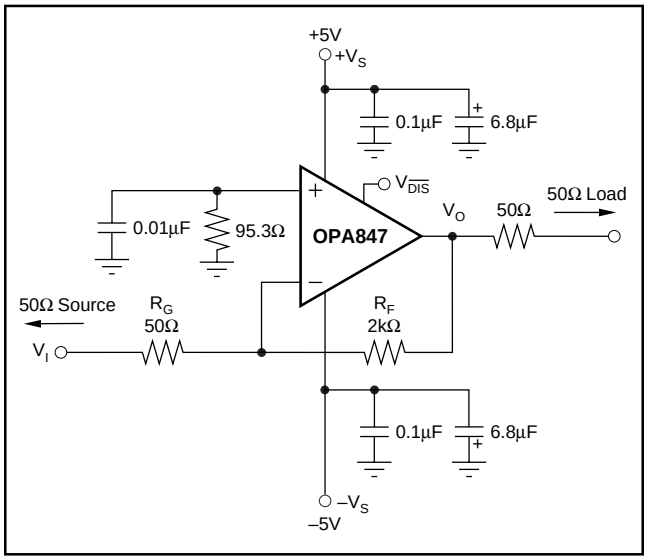


FIGURE 2. Noninverting G = –40 Specification and Test Circuit.

WIDEBAND, HIGH SENSITIVITY, TRANSIMPEDANCE DESIGN

The high GBP and low input voltage and current noise for the OPA847 make it an ideal wideband transimpedance amplifier for low to moderate transimpedance gains. Very high transimpedance gains (> 100kΩ) will benefit from the low input noise current of a JFET input op amp such as the OPA657. Unity-gain stability in the op amp is not required for application as a transimpedance amplifier. Figure 3 shows one possible transimpedance design example that would be particularly suitable for the 155Mbit data rate of an OC-3 receiver. Designs that require high bandwidth from a large area detector with relatively low transimpedance gain will benefit from the low input voltage noise for the OPA847. The amplifier's input voltage noise is peaked up over frequency by the diode source capacitance, and can (in many cases) become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage ($-V_B$) applied, the desired transimpedance gain (R_F), and the GBP for the OPA847 (3900MHz). With these three variables set (including the parasitic input capacitance for the OPA847 added to C_D), the feedback capacitor value (C_F) can be set to control the frequency response.

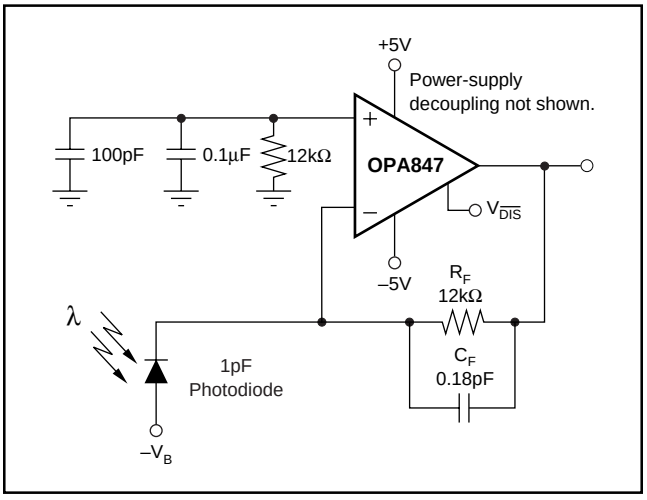


FIGURE 3. Wideband, High Sensitivity, OC-3 Transimpedance Amplifier.

To achieve a maximally flat 2nd-order Butterworth frequency response, set the feedback pole as shown in Equation 1.

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \qquad (1)$$

Adding the common-mode and differential mode input capacitance (1.2 + 2.5)pF to the 1pF diode source capacitance of Figure 3, and targeting a 12kΩ transimpedance gain using the 3900MHz GBP for the OPA847 requires a feedback pole set to 74MHz to get a nominal Butterworth frequency response design. This requires a total feedback capacitance of 0.18pF. That total is shown in Figure 3, but recall that typical surface-mount resistors have a parasitic capacitance of 0.2pF, leaving no external capacitor required for this design.

Equation 2 gives the approximate –3dB bandwidth that results if C_F is set using Equation 1.

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} (Hz) \qquad (2)$$

The example of Figure 3 gives approximately 104MHz flat bandwidth using the 0.18pF feedback compensation capacitor. This bandwidth easily supports an OC-3 receiver with exceptional sensitivity.

If the total output noise is bandlimited to a frequency less than the feedback pole frequency, a very simple expression for the equivalent input noise current is shown as Equation 3.

(3)

$$i_{EQ} = \sqrt{i_N^2 + \left(\frac{4kT}{R_F}\right)^2 + \frac{(E_N 2\pi C_D F)^2}{3}}$$

where:

i_{EQ} = Equivalent input noise current if the output noise is bandlimited to $f < 1/2\pi R_F C_F$

i_N = Input current noise for the op amp inverting input

e_N = Input voltage noise for the op amp

C_D = Total Inverting Node Capacitance

f = Bandlimiting frequency in Hz (usually a post filter prior to further signal processing)

Evaluating this expression up to the feedback pole frequency at 74MHz for the circuit of Figure 3 gives an equivalent input noise current of 3.0pA/$\sqrt{Hz}$. This is slightly higher than the 2.5pA/$\sqrt{Hz}$ input current noise for the op amp. This total equivalent input current noise is slightly increased by the last term in the equivalent input noise expression. It is essential in this case to use a low-voltage noise op amp. For example, if a slightly higher input noise voltage, but otherwise identical, op amp were used instead of the OPA847 in this application (say 2.0nV/$\sqrt{Hz}$), the total input referred current noise would increase to 3.7pA/$\sqrt{Hz}$. Low input voltage noise is required for the best sensitivity in these wideband transimpedance applications. This is often unspecified for dedicated transimpedance amplifiers with a total output noise for a specified source capacitance given instead. It is the relatively high input voltage noise for those components that cause higher than expected output noise if the source capacitance is higher than specified.

The output DC error for the circuit of Figure 3 is minimized by including a 12kΩ to ground on the noninverting input. This reduces the contribution of input bias current errors (for total output offset voltage) to the offset current times the feedback resistor. To minimize the output noise contribution of this resistor, 0.01µF and 100pF capacitors are included in parallel. Worst-case output DC error for the circuit of Figure 3 at 25°C is:

V_{OS} = ±0.5mV (input offset voltage) ± 0.6µA (input offset current) • 12kΩ = ±7.2mV

Worst-case output offset DC drift (over the 0°C to 70°C span) is:

dV_{OS}/dT = ±1.5µV/°C (input offset drift) ± 2nA/°C (input offset current drift) • 12kΩ = ±21.5µV/°C.

Even with bias current cancellation, the output DC errors are dominated in this example by the offset current term. Improved output DC precision and drift are possible, particularly at higher transimpedance gains, using the JFET input OPA657. The JFET input removes the input bias current from the error equation (eliminating the need for the resistor to ground on the noninverting input), leaving only the input offset voltage and drift as an output DC error term.

Included in the Typical Characteristics are transimpedance frequency response curves for a fixed 20kΩ gain over various detector diode capacitance settings. These curves are repeated in Figure 4, along with the test circuit. As the photodiode capacitance changes, the feedback capacitor must change to maintain a stable and flat frequency response. Using Equation 1, C_F is adjusted to give the Butterworth frequency responses shown in Figure 4.

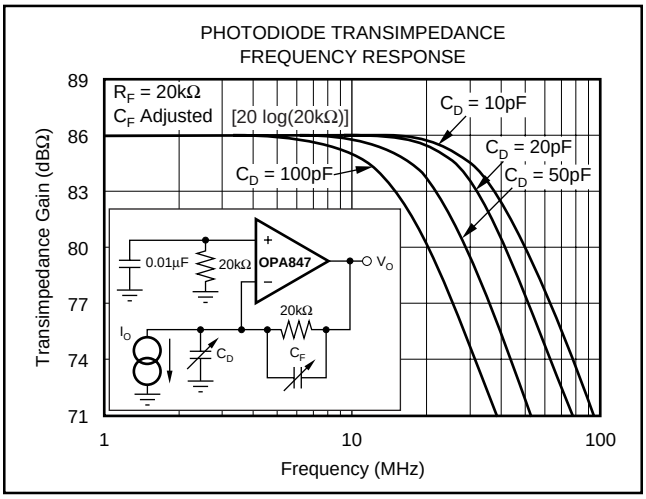


FIGURE 4. Transimpedance Bandwidth vs C_D.

LOW-GAIN COMPENSATION FOR IMPROVED SFDR

Where a low gain is desired, and inverting operation is acceptable, a new external compensation technique can be used to retain the full slew rate and noise benefits of the OPA847, while giving increased loop gain and the associated distortion improvements offered by a non-unity-gain stable op amp. This technique shapes the loop gain for good stability, while giving an easily controlled 2nd-order low-pass frequency response. This technique is used for the circuit on the front page of this data sheet in a differential configuration to achieve extremely low distortion through high frequencies (< –90dBc through 30MHz). The amplifier portion of this circuit is set up for a differential gain of 8.5V/V from a differential input signal to the output. Using the input transformer shown improves the noise figure and translates from a single-ended to a differential signal. If the source is differential already, it can be fed directly into the gain setting resistors. To set the compensation capacitors (C_S and C_F), consider the half circuit of Figure 5, where the 50Ω source is reflected through the 1:2 transformer, then cut in half, and grounded to give a total impedance to the AC ground for the circuit on the front page equal to 200Ω.

Considering only the noise gain (which is the same as the noninverting signal gain) for the circuit of Figure 5, the low-frequency noise gain (N_{G1}) is set by the resistor ratio, while the high-frequency noise gain (N_{G2}) is set by the capacitor ratio. The capacitor values set both the transition frequencies and the high-frequency noise gain. If the high-frequency noise gain, determined by $N_{G2} = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp, and the noise gain pole (set by $1/R_FC_F$) is placed correctly, a very well controlled 2nd-order low-pass frequency response results.

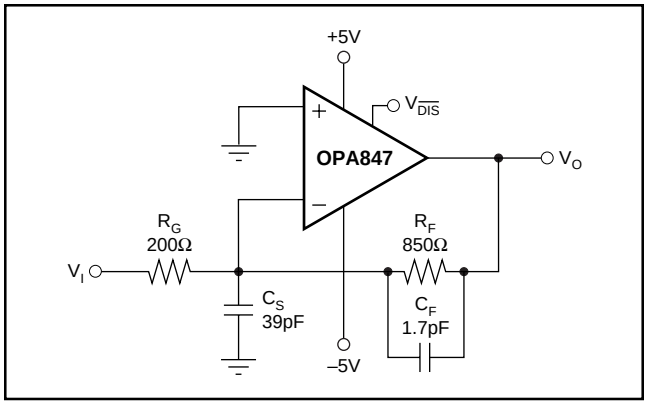


FIGURE 5. Broadband, Low-Inverting Gain External Compensation.

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. The first parameter is the target high-frequency noise gain (NG_2), which should be greater than the minimum stable gain for the OPA847. Here, a target of $NG_2 = 24$ is used. The second parameter is the desired low-frequency signal gain, which also sets the low-frequency noise gain (NG_1). To simplify this discussion, we will target a maximally flat, 2nd-order, low-pass Butterworth frequency response (Q = 0.707). The signal gain shown in Figure 5 sets the low-frequency noise gain to $NG_1 = 1 + R_F/R_G$ (= 5.25 in this example). Then, using only these two gains and the GBP for the OPA847 (3900MHz), the key frequency in the compensation is set by Equation 4.

$$Z_O = \frac{GBP}{NG_1^2}\left[\left(1-\frac{NG_1}{NG_2}\right)-\sqrt{1-2\frac{NG_1}{NG_2}}\right] \qquad (4)$$

Physically, this Z_O (4.4MHz for the values shown above) is set by $1/(2\pi R_F(C_F + C_S))$ and is the frequency at which the rising portion of the noise gain would intersect the unity gain if projected back to a 0dB gain. The actual zero in the noise gain occurs at $NG_1 \bullet Z_O$ and the pole in the noise gain occurs at $NG_2 \bullet Z_O$. That pole is physically set by $1/(R_FC_F)$. Since GBP is expressed in Hz, multiply Z_O by 2π and use to get C_F by solving Equation 5.

$$C_F = \frac{1}{2\pi R_F Z_O NG_2} (= 1.76pF) \qquad (5)$$

Finally, since C_S and C_F set the high-frequency noise gain, determine C_S using Equation 6 (solving for C_S by using $NG_2 = 24$):

$$C_S = (NG_2 - 1)C_F \quad (6)$$

which gives C_S = 40.6pF.

Both of these calculated values have been reduced slightly in Figure 5 to account for parasitics. The resulting closed-loop bandwidth is approximately equal to Equation 7.

$$f_{-3dB} \cong \sqrt{Z_O \bullet GBP} \quad (7)$$

For the values shown in Figure 5, f_{-3dB} is approximately 131MHz. This is less than that predicted by simply dividing the GBP product by NG_1. The compensation network controls the bandwidth to a lower value, while providing the full slew rate at the output and an exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \bullet Z_O$.

Using this low-gain inverting compensation, along with the differential structure for the circuit shown on the front page of this data sheet, gives a significant reduction in harmonic distortion. The measured distortion at $2V_{PP}$ output does not rise above –95dB until frequencies > 20MHz are applied.

The Typical Characteristics show the exceptional bandwidth control possible using this technique at low inverting gains. Figure 6 repeats the measured results with the test circuit shown.

The compensation capacitors, C_S and C_F, are set by targeting a high-frequency noise gain of 21 and using equations 4 through 6. This approach allows relatively low inverting gain applications to use the full slew rate and low input noise of the OPA847.

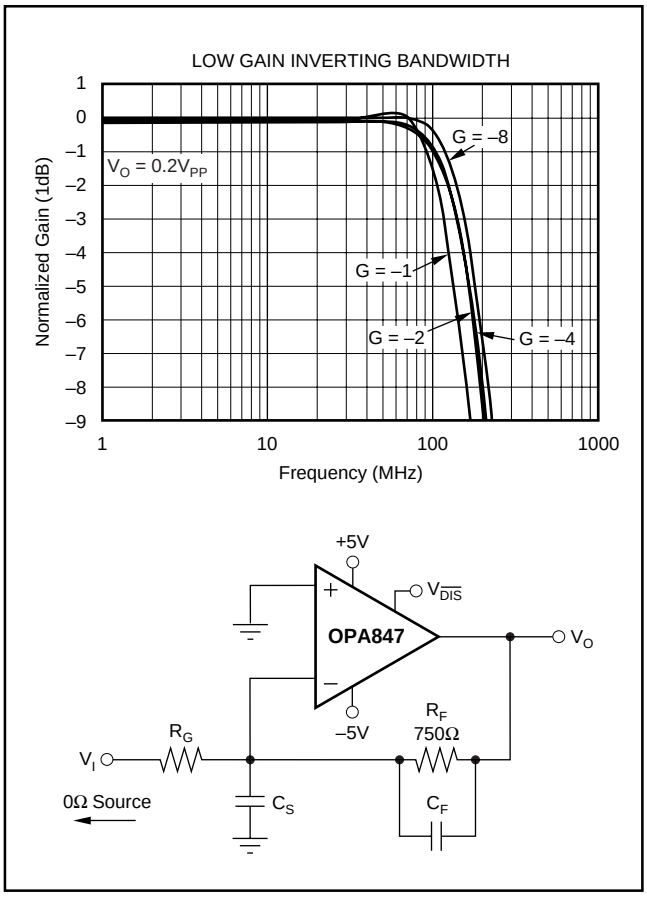


FIGURE 6. Low-Gain Inverting Performance.

LOW-NOISE FIGURE, HIGH DYNAMIC RANGE AMPLIFIER

The low input noise voltage of the OPA847 and its very high 2-tone, 3rd-order intermodulation intercept can be used to good advantage as a fixed-gain amplifier. While input noise figures in the 10dB range (for a matched 50Ω input) are easily achieved with just the OPA847, Figure 7 illustrates a technique to reduce the noise figure even further, while providing a broadband, high-gain HF amplifier stage using two stages of the OPA847.

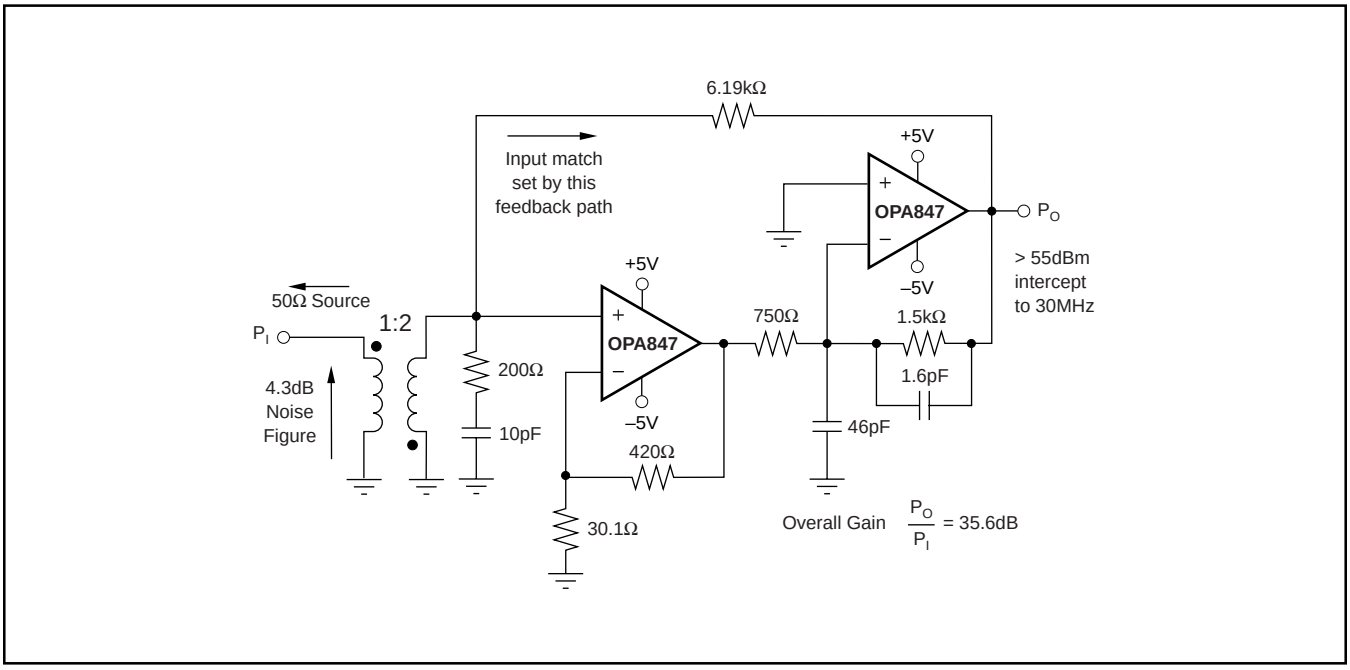


FIGURE 7. Very High Dynamic Range HF Amplifier.

This circuit uses two stages of forward gain with an overall feedback loop to set the input impedance match. The input transformer provides both a noiseless voltage gain and a signal inversion to retain an overall noninverting signal path from P_I to P_O. The second amplifier stage is inverting to provide the correct feedback polarity through the 6.19kΩ resistor. To achieve a 50Ω input match at the primary of the 1:2 transformer, the secondary must see a 200Ω load impedance. At higher frequencies, the match is provided by the 200Ω resistor in series with 10pF. The low-noise figure (4.3dB) for this circuit is achieved by using the transformer, the low-voltage noise OPA847, and the input match set by the feedback at lower frequencies intended for this HF design. The 1st-stage amplifier provides a gain of +15V/V. The very high SFDR is provided by operating the output stage at a low signal gain of –2 and using the inverting compensation technique to shape the noise gain to hold it stable. This 2nd-stage compensation is set to intentionally bandlimit the overall response to approximately 100MHz. For output loads > 400Ω, this circuit can give a 2-tone SFDR that exceeds 90dB through 30MHz. In narrowband applications, the 3rd-order intercept exceeds 55dBm. Besides offering a very high dynamic range, this circuit improves on standard HF amplifiers by offering a precisely controlled gain and a very flexible output interface capability.

NONINVERTING GAIN FLATNESS COMPENSATION

Decreasing the operating gain from the nominal design point of +20 decreases the phase margin. This increases Q for the closed-loop poles, peaks up the frequency response, and extends the bandwidth. A peaked frequency response shows overshoot and ringing in the pulse response, as well as higher integrated output noise. When operating the OPA847 at a noninverting gain < +12V/V, increased peaking and possible sustained oscillations may result. However, operation at low gains may be desirable to take advantage of the higher slew rate and exceptional DC precision of the OPA847. Numerous external compensation techniques are suggested for operating a high-gain op amp at low gains. Most of these give zero/pole pairs in the closed-loop response that cause long term settling tails in the pulse response and/or phase nonlinearity in the frequency response.

Figure 8 shows a resistor-based compensation technique that allows the flatness at low noninverting signal gains to be controlled separately from the signal gain. This approach retains the full slew rate to the output but gives up some of the low-noise benefit of the OPA847. Including the effect of the total source impedance (25Ω in Figure 8), tuning resistor R_1 can be set using Equation 8.

$$R_1 = \frac{R_F + R_S A_V}{NG - A_V} \quad (8)$$

where:

A_V = desired signal gain (+12V/V in Figure 8)

NG = target noise gain (adjusted in Figure 9)

R_S = total source impedance

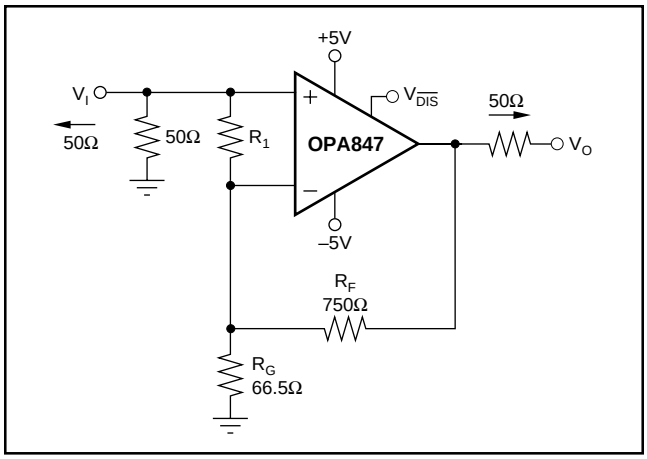


FIGURE 8. Low Noninverting Gain Flatness Trim.

The effect of this noninverting gain flatness tune is shown in Figure 9. At an NG of 12, R_1 is removed and only R_F and R_G are present in Figure 8. The peaking is typically 4.5dB, as shown in the small-signal frequency response curves versus gain curves at this setting. As R_1 is decreased, the operating noise gain (NG) increases, reducing the peaking and bandwidth until the nominal design point of +20 noise gain gives a non-peaked response.

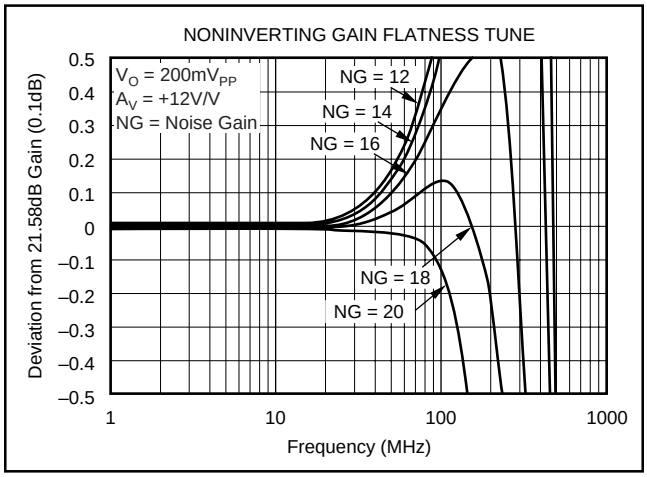


FIGURE 9. Frequency Response Flatness with External Tuning Resistor.

DIFFERENTIAL OPERATION

Operating two OPA847 amplifiers in a differential inverting configuration can further suppress even-order harmonic terms. The Typical Characteristics show measured performance for this condition. These measurements were done at the relatively high gain of 40V/V. Even lower distortion is possible operating at lower gains using the external inverting compensation techniques, as discussed previously. For the distortion data presented in Figure 10, the output swing is increased to 4V_{PP} into 400Ω to allow direct comparison to the single-channel data at 2V_{PP} into 200Ω. Comparing the 2nd- and 3rd-harmonics at 20MHz in Figure 10 to the gain of +20, 2V_{PP}, 200Ω data, shows the 2nd-harmonic is reduced to –76dBc (from –67dBc) and the 3rd-harmonic is reduced from –80dBc to –85dBc. Using the two

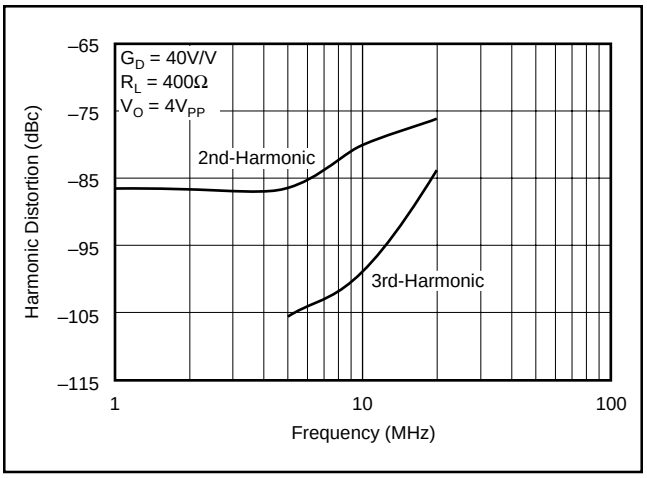


FIGURE 10. Differential Distortion vs Frequency.

amplifiers in this configuration has significantly reduced the 2nd-harmonic, even after doubling the output voltage swing (to 4V_{PP}) and the gain (to 40V/V).

SINGLE-SUPPLY OPERATION

The OPA847 can be operated from a single power supply if system constraints require it. Operation from a single +5V to +12V supply is possible with minimal change in AC performance. The Typical Characteristics show the input and output voltage ranges for a bipolar supply range from ±2.5V to ±6.0V. The Common-Mode Input Range and Output Swing vs Supply Voltage curve shows that the required headroom on both the input and output pins remains at approximately 1.5V over this entire range. On a single +5V supply, for instance, this means the noninverting input should remain centered at +2.5V ± 1V, as should the output pin. Figure 11 shows an example application biasing the noninverting input at mid-supply and running an AC-coupled input to the inverting gain path. Since the gain resistor is blocked off for DC, the bias point on the noninverting input appears at the output, centering up the output as well as on the power supply. The OPA847 can support this mode of operation down to a single supply of +5V and up to a single supply of +12V. If shutdown is desired for single-supply operation, it is important to realize that the shutdown pin is referenced from the positive supply pin. Open collector (drain) interfaces are suggested for single-supply operation above +5V.

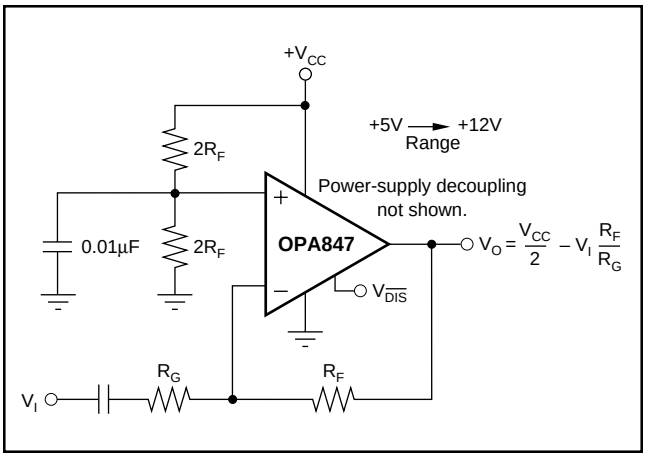


FIGURE 11. Single-Supply Inverting Amplifier.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA847 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table I.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA847ID	SO-8	DEM-OPA-SO-1B	SBOU026
OPA847IDBV	SOT23-6	DEM-OPA-SOT-1B	SBOU027

TABLE I. Demonstration Fixtures by Package.

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA847 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA847 in its intended application. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role in circuit performance. A SPICE model for the OPA847 is available through the TI web site (www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO MINIMIZE NOISE

The OPA847 provides a very low input noise voltage while requiring a low 18.1mA of quiescent current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. See Figure 12 for the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise power. This computation adds all the contributing noise powers at the output by superposition, then takes the square

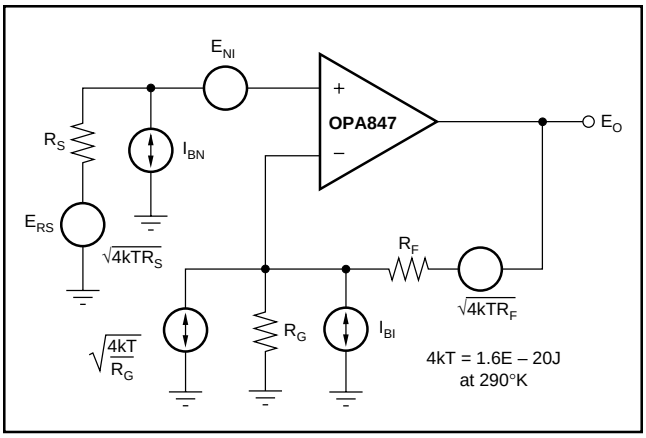


FIGURE 12. Op Amp Noise Analysis Model.

root to get back to a spot noise voltage. Equation 9 shows the general form for this output noise voltage using the terms illustrated in Figure 11.

(9)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_F}\,NG$$

Dividing this expression by the noise gain ($NG = 1 + R_F/R_G$) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 10.

(10)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Putting high resistor values into Equation 10 can quickly dominate the total equivalent input-referred noise. A 45Ω source impedance on the noninverting input adds a Johnson voltage noise term equal to the amplifier's voltage noise by itself. As a simplifying constraint, set $R_G = R_S$ in Equation 10 and assume an $R_S/2$ source impedance at the noninverting input, where R_S is the signal source impedance and another matching R_S to ground is at the noninverting input. This results in Equation 11, where NG > 12 is assumed to further simplify the expression.

$$E_N = \sqrt{E_{NI}^2 + \frac{5}{4}\left(I_B R_S\right)^2 + 4kT\left(\frac{3R_S}{2}\right)} \qquad (11)$$

Evaluating this expression for $R_S = 50\Omega$ gives a total equivalent input noise of $1.4nV/\sqrt{Hz}$. Note that at these higher gains, the simplified input referred spot noise expression of Equation 11 does not include the gain. This is a good approximation for NG > 12, as is typically required by stability considerations.

FREQUENCY RESPONSE CONTROL

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the Electrical Characteristics. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) predicts the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low gains (increased feedback factors), most high-speed amplifiers exhibit a more complex response with lower phase margin. The OPA847 is compensated to give a maximally flat 2nd-order Butterworth closed-loop response at a noninverting gain of +20 (see Figure 1). This results in a typical gain of +20 bandwidth of 350MHz, far exceeding that predicted by dividing the 3900MHz GBP by 20. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +50, the OPA847 very nearly matches the 78MHz bandwidth predicted using the simple formula and the typical GBP of 3900MHz.

Inverting operation offers some interesting opportunities to increase the available GBP. When the source impedance is matched by the gain resistor (see Figure 2), the signal gain is $(1 + R_F/R_G)$, while the noise gain for bandwidth purposes is $(1 + R_F/2R_G)$. This cuts the noise gain almost in half, increasing the minimum operating gain for inverting operation under these condition to –22 and the equivalent gain bandwidth product to > 7.8GHz.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC, including additional external capacitance that may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA847 can be very susceptible to decreased stability and may give closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem are suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics help the designer pick a recommended R_S versus capacitive load. The resulting frequency response curves show a flat response for several selected capacitive loads and recommended R_S combinations. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA847. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully and add the recommended series resistor as close as possible to the OPA847 output pin (see the Board Layout section).

The criterion for setting the R_S resistor is a maximum bandwidth, flat frequency response at the load. For the OPA847 operating in a gain of +20, the frequency response at the output pin is very flat to begin with, allowing relatively small values of R_S to be used for low capacitive loads. As the signal gain is increased, the unloaded phase margin also increases. Driving capacitive loads at higher gains requires lower R_S values than those shown for a gain of +20.

DISTORTION PERFORMANCE

The OPA847 is capable of delivering an exceptionally low distortion signal at high frequencies over a wide range of gains. The distortion plots in the Typical Characteristics show the typical distortion under a wide variety of conditions. Most of these plots are limited to a 110dB dynamic range. The OPA847's distortion driving a 200Ω load does not rise above –90dBc until either the signal level exceeds $2.0V_{PP}$ and/or the fundamental frequency exceeds 5MHz. Distortion in the audio band is < –130dBc.

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration this is the sum of $R_F + R_G$, while in the inverting configuration this is only R_F (see Figure 2). Increasing the output voltage swing increases harmonic distortion directly. A 6dB increase in output swing generally increases the 2nd-harmonic 12dB and the 3rd-harmonic 18dB. Increasing the signal gain also increases the 2nd-harmonic distortion. Finally, the distortion increases as the fundamental frequency increases due to the rolloff in the loop gain with frequency. Conversely, the distortion improves going to lower frequencies down to the dominant open-loop pole at approximately 80kHz.

The OPA847 has an extremely low 3rd-order harmonic distortion. This also gives a high 2-tone 3rd-order intermodulation intercept, as shown in the Typical Characteristics. This intercept curve is defined at the 50Ω load when driven through a 50Ω matching resistor to allow direct comparisons to R_F devices. This matching network attenuates the voltage swing from the output pin to the load by 6dB. If the OPA847 drives directly into the input of a high-impedance device, such as an ADC, this 6dB attenuation is not taken. Under these conditions, the intercept as reported in the Typical Characteristics increases by a minimum of 6dBm. The intercept is used to predict the intermodulation spurious power levels for two closely spaced frequencies. If the two test frequencies, f_1 and f_2, are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $\Delta_f = |f_2 - f_1|/2$, the two 3rd-order, close-in spurious tones appear at $f_O \pm 3 \bullet \Delta_f$. The difference between the two equal test-tone power levels and these intermodulation spurious power levels is given by $\Delta dBc = 2(IM3 - P_O)$, where IM3 is the intercept taken from the Typical Characteristics and P_O is the power level in dBm at the 50Ω load for one of the two closely spaced test frequencies. For instance, at 30MHz, the OPA847 at a gain of +20 has an intercept of 34dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be $2V_{PP}$, this requires each tone to be 4dBm. The 3rd-order intermodulation spurious tones will then be 2(34 – 4) = 60dBc below the test-tone power level (–56dBm). If this same $2V_{PP}$ 2-tone envelope is delivered directly into the input of an ADC without the matching loss or the loading of the 50Ω network, the intercept would increase to at least 40dBm. With the same signal and gain conditions, but now driving directly into a light load, the spurious tones will then be at least 2(40 – 4) = 72dBc below the 4dBm test-tone power levels centered on 30MHz. Tests have shown that they are in fact much lower due to the lighter loading presented by most ADCs.

DC ACCURACY AND OFFSET CONTROL

The OPA847 can provide excellent DC signal accuracy due to its high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of its low ±0.5mV input offset voltage, careful attention to the input bias current cancellation is also required. The low-noise input stage for the OPA847 has a relatively high input bias current (19μA typical into the pins), but with a very close match between the two input currents—typically ±100nA input offset current. Figures 13 and 14 show typical distributions of input offset voltage and current for the OPA847.

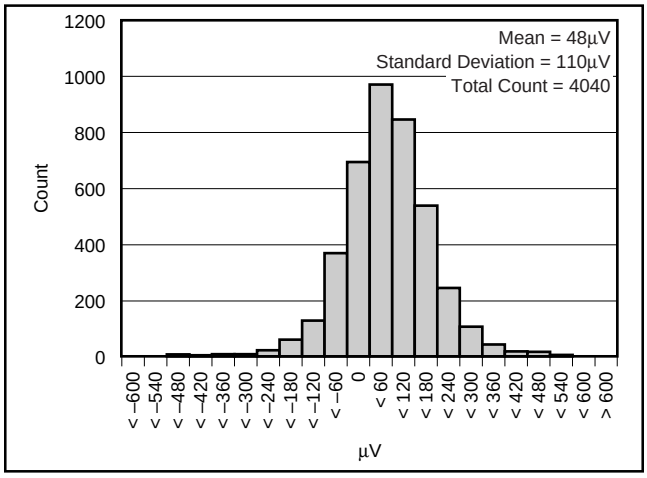


FIGURE 13. Input Offset Voltage Distribution in μV.

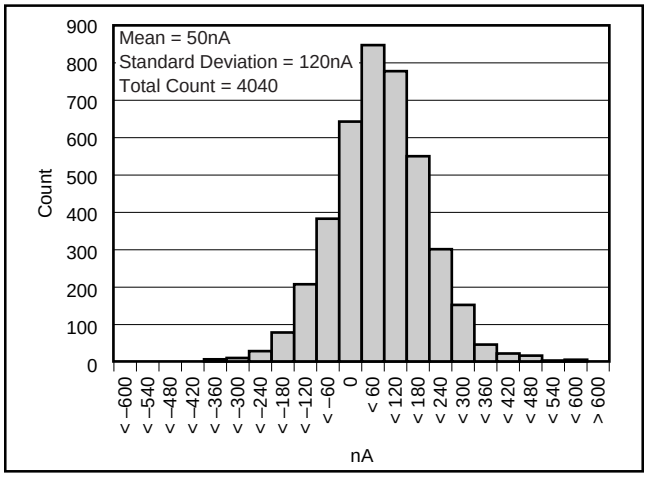


FIGURE 14. Input Offset Current Distribution in nA.

The total output offset voltage can be considerably reduced by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 1 is to insert a 12.1Ω series resistor into the noninverting input from the 50Ω terminating resistor. When the 50Ω source resistor is DC-coupled, this increases the source impedance for the noninverting input bias current to 37.1Ω. Since this is now equal to the impedance looking out of the inverting input (R_F || R_G) for Figure 1, the circuit cancels the gains for the bias currents to the output, leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using the 750Ω feedback resistor, this output error is now less than ±0.85µA • 750Ω = ±640µV over the full temperature range for the circuit of Figure 1, with a 12.1Ω resistor added as described. The output DC offset is then dominated by the input offset voltage multiplied by the signal gain. For the circuit of Figure 1, this is a worst-case output DC offset of ±0.6mV • 20 = ±12mV over the full temperature range.

A fine-scale output offset null, or DC operating point adjustment, is sometimes required. Numerous techniques are available for introducing a DC offset control into an op amp circuit. Most of these techniques eventually reduce to setting up a DC current through the feedback resistor. One key consideration to selecting a technique is to ensure that it has a minimal impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input can be considered. For a DC-coupled inverting input signal, this DC offset signal sets up a DC current back into the source that must be considered. An offset adjustment placed on the inverting op amp input can also change the noise gain and frequency response flatness. Figure 15 shows one example of an offset adjustment for a DC-coupled signal path that has minimum impact on the signal frequency response.

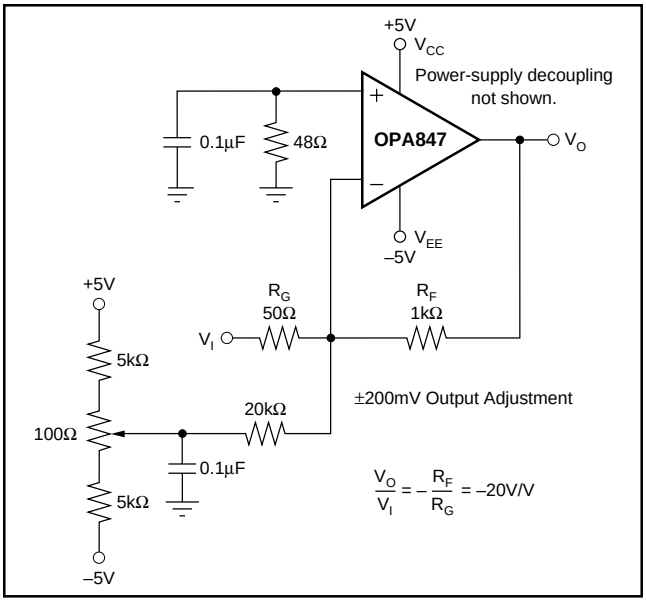


FIGURE 15. DC-Coupled, Inverting Gain of –20 with Output Offset Adjustment.

In this case, the input is brought into an inverting gain resistor with the DC adjustment as an additional current summed into the inverting node. The resistor values setting this offset adjustment are much larger than the signal path resistors. This ensures that this adjustment has minimal impact on the loop gain and, hence, the frequency response.

POWER SHUTDOWN OPERATION

The OPA847 provides an optional power shutdown feature that can be used to reduce system power. If the $V_{\overline{DIS}}$ control pin is left unconnected, the OPA847 operates normally. This shutdown is intended only as a power saving feature. Forward path isolation is very good for small signals. Large signal isolation is not ensured. Using this feature to multiplex two or more outputs together is not recommended. Large signals applied to the shutdown output stages can turn on parasitic devices, degrading signal linearity for the desired channel.

Turn-on time is very quick from the shutdown condition, typically < 60ns. Turn-off time is strongly dependent on the external circuit configuration, but is typically 200ns for the circuit of Figure 1. Using the OPA847 with higher external resistor values, such has high-gain transimpedance circuits, slows the shutdown time since the time constants for the internal nodes to discharge are longer.

To shutdown, the control pin must be asserted low. This logic control is referenced to the positive supply, as shown in the simplified circuit of Figure 16.

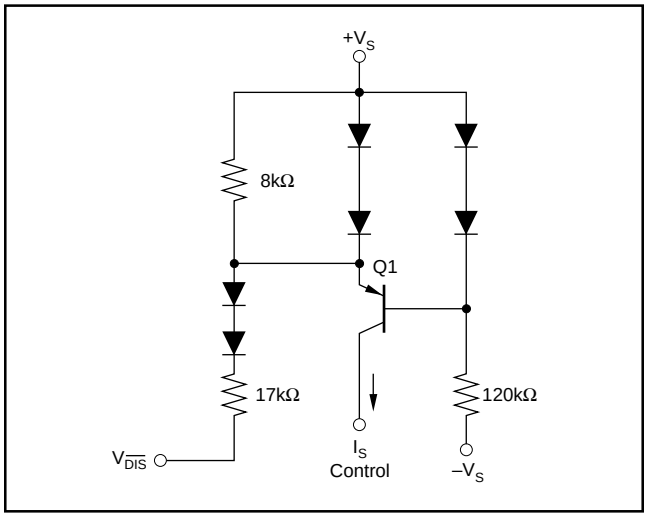


FIGURE 16. Simplified Shutdown Control Circuit.

In normal operation, base current to Q1 is provided through the 120kΩ resistor, while the emitter current through the 8kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled low, additional current is pulled through the 8kΩ resistor, eventually turning on these two diodes (≈ 180µA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the shutdown mode is only that required to operate the circuit of Figure 16.

The shutdown feature for the OPA847 is a positive-supply referenced, current-controlled interface. Open-collector (or drain) interfaces are most effective, as long as the controlling logic can sustain the resulting voltage (in open mode) that appears at the $V_{\overline{DIS}}$ pin. The $V_{\overline{DIS}}$ pin voltage is one diode below the positive supply voltage applied to the OPA847 if the logic voltage is open. For voltage output logic interfaces, the on/off voltage levels described in the Electrical Characteristics apply only for a +5V supply. An open-drain interface is recommended for a shutdown operation using a higher positive supply and/or logic families with inadequate high-level voltage swings.

THERMAL ANALYSIS

The OPA847 does not require heatsinking or airflow in most applications. Maximum desired junction temperature sets the maximum allowed internal power dissipation, as described here. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to half either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \bullet R_L)$, where R_L includes feedback network loading. This is the absolute highest power that can be dissipated for a given R_L. All actual applications dissipate less power in the output stage.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA847IDBV (SOT23-6 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load. Maximum internal power is:

$P_D = 10V \bullet 18.9mA + 5^2/(4(100\Omega \parallel 789\Omega)) = 259mW$

Maximum $T_J = +85°C + (0.26W \bullet 150°C/W) = 124°C$

All actual applications will operate at a lower junction temperature than the 124°C computed above. Compute your actual output stage power to get an accurate estimate of maximum junction temperature, or use the results shown here as an absolute maximum.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier like the OPA847 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, create a window around the signal I/O pins in all of the ground and power planes around these pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These can be placed somewhat further from the device and can be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components preserves the high-frequency performance of the OPA847. Use resistors that have low reactance at high frequencies. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound-type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 2.0kΩ, this parasitic capacitance can add a pole and/or zero below 400MHz that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations. It has been suggested here that a good starting point for design would be to set R_G to 39.2Ω. Doing this automatically keeps the resistor noise terms low, and minimizes the effect of their parasitic capacitance. Transimpedance applications can use much higher resistor values. The compensation techniques described in this data sheet allow excellent frequency response control, even with very high feedback resistor values.

d) Connections to other wideband devices on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load. Low parasitic

capacitive loads (< 4pF) may not need an R_S, since the OPA847 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases from +20V/V (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard and, in fact, a higher impedance environment improves distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA847 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source-end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of Recommended R_S vs Capacitive Load. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA847 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA847 onto the board.

INPUT AND ESD PROTECTION

The OPA847 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 17.

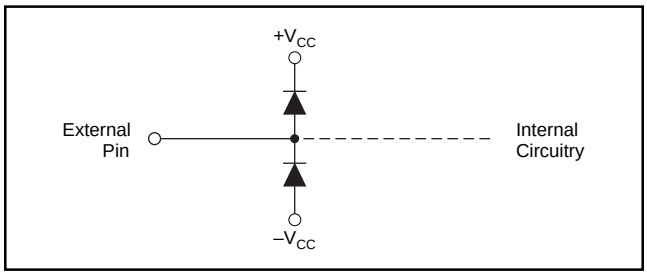


FIGURE 17. Internal ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA847), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
12/08	E	2	Absolute Maximum Ratings	Changed minimum Storage Temperature Range from –40°C to –65°C.
4/06	D	15	Design-In Tools	Board part number changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA847ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 847	Samples
OPA847IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OATI	Samples
OPA847IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OATI	Samples
OPA847IDBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OATI	Samples
OPA847IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 847	Samples
OPA847IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 847	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

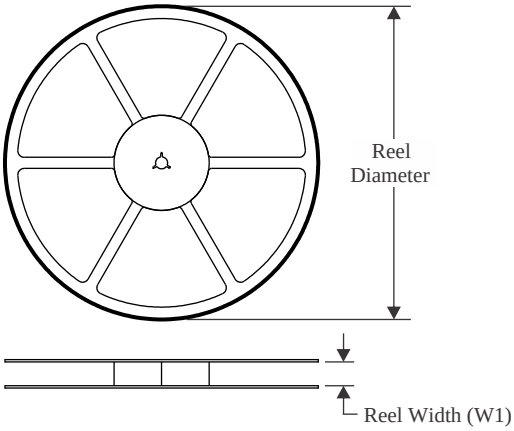
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

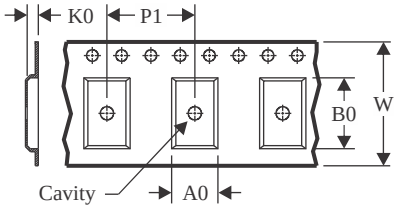
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

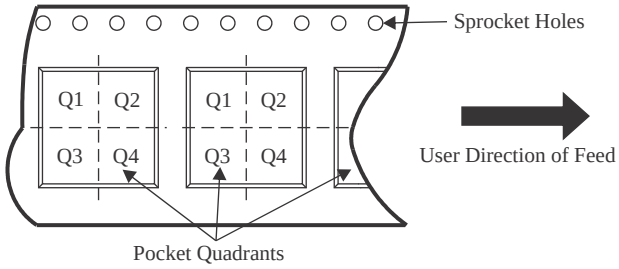


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

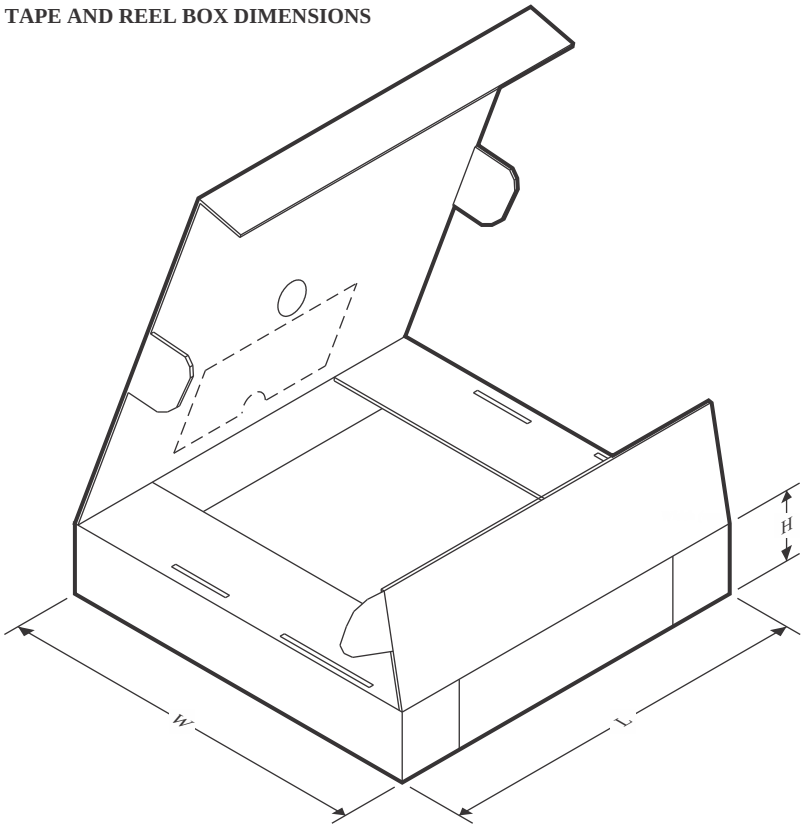
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA847IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA847IDBVT	SOT-23	DBV	6	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA847IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

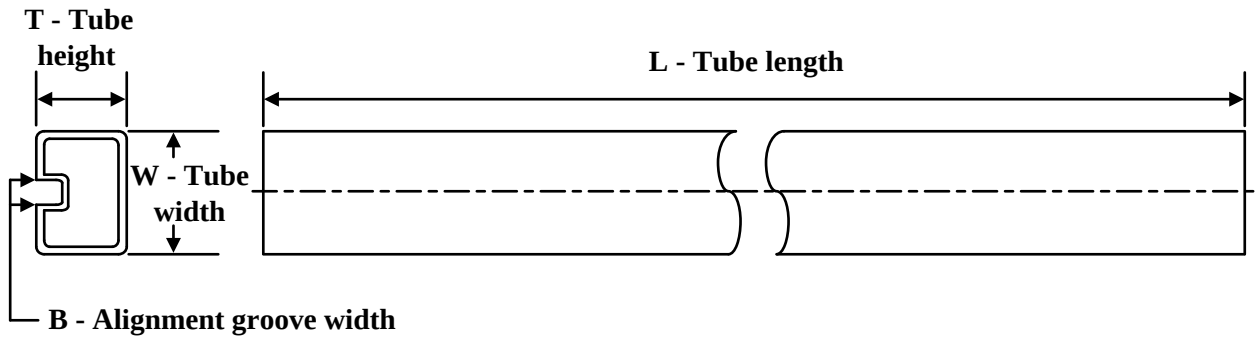
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

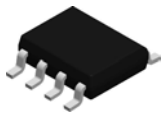
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA847IDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
OPA847IDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
OPA847IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA847ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA847IDG4	D	SOIC	8	75	506.6	8	3940	4.32

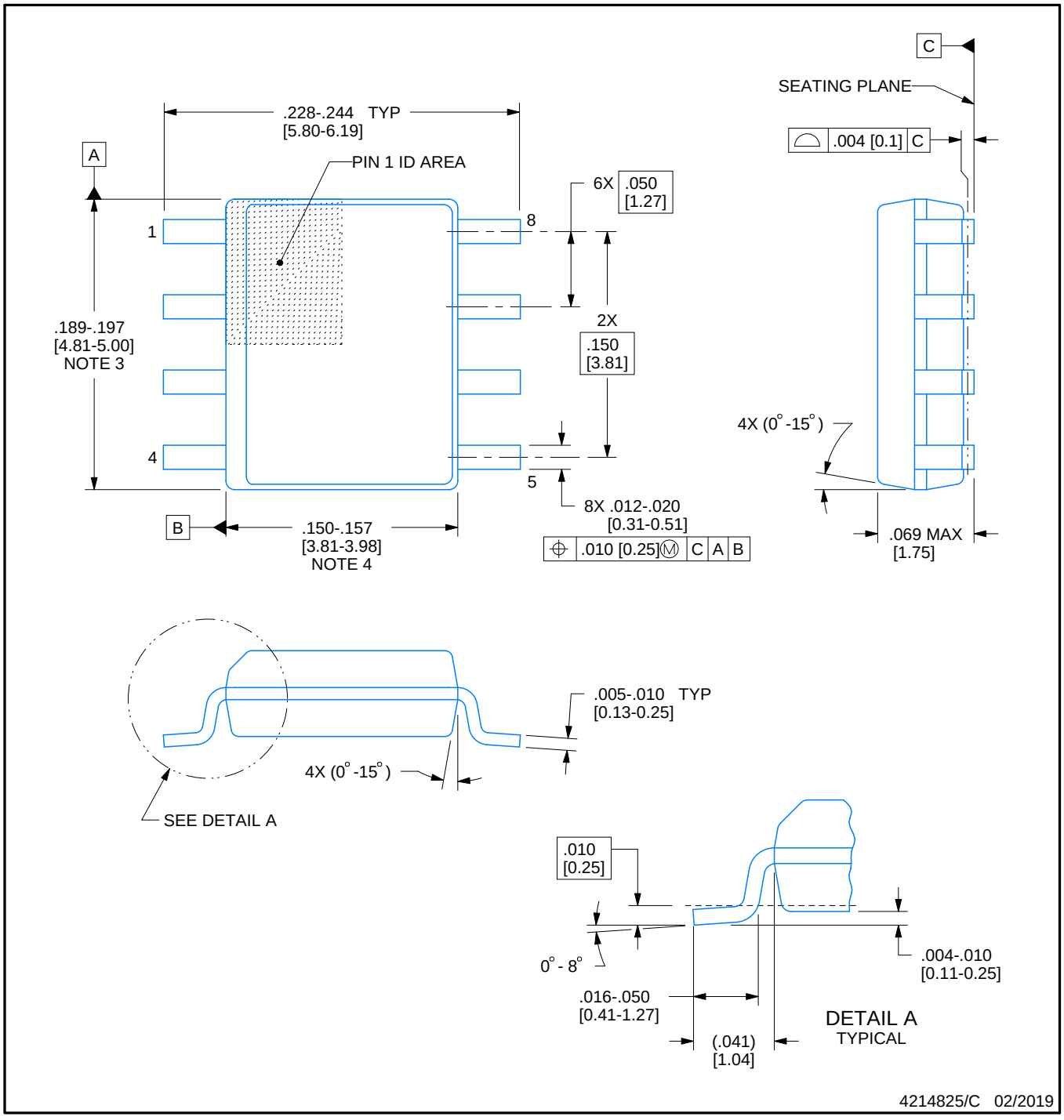


PACKAGE OUTLINE

D0008A

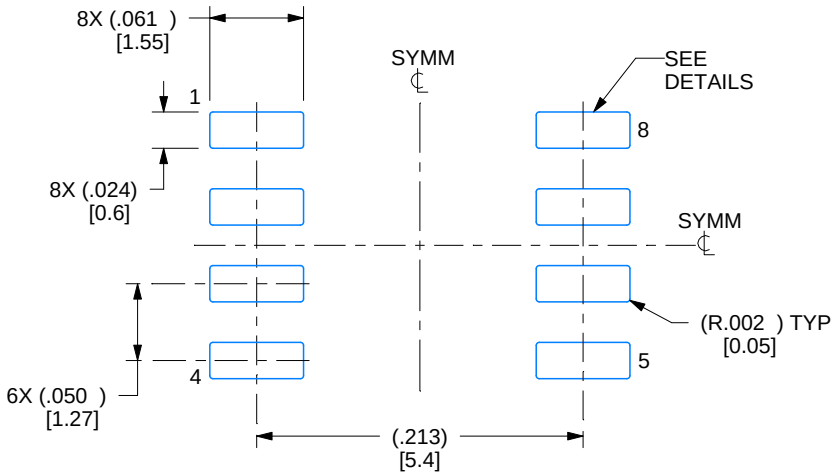
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

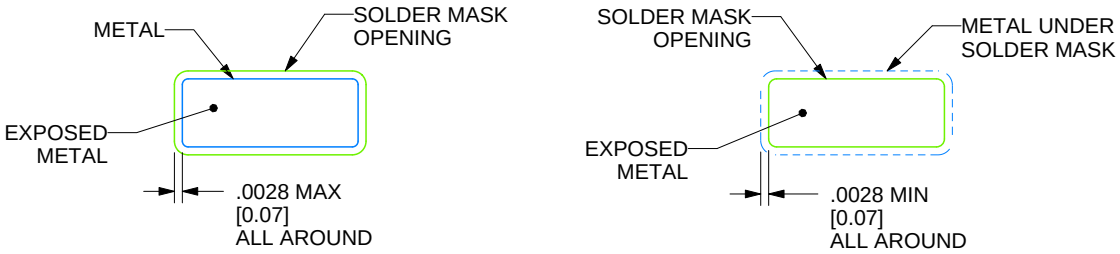


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

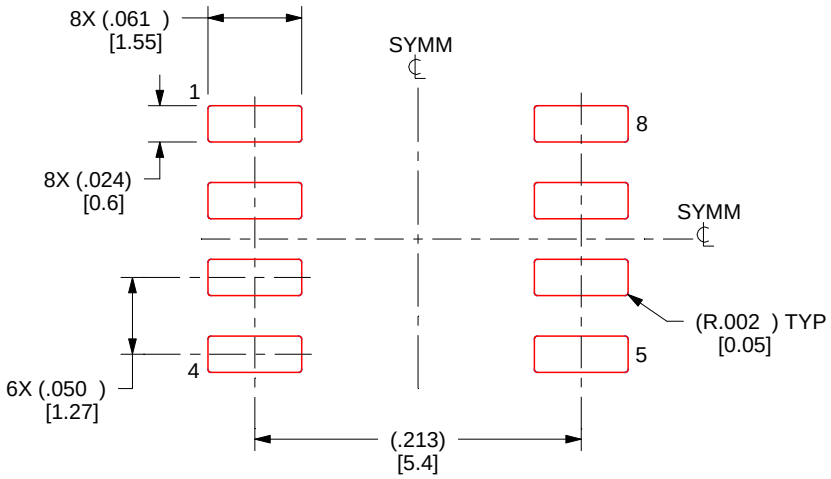
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

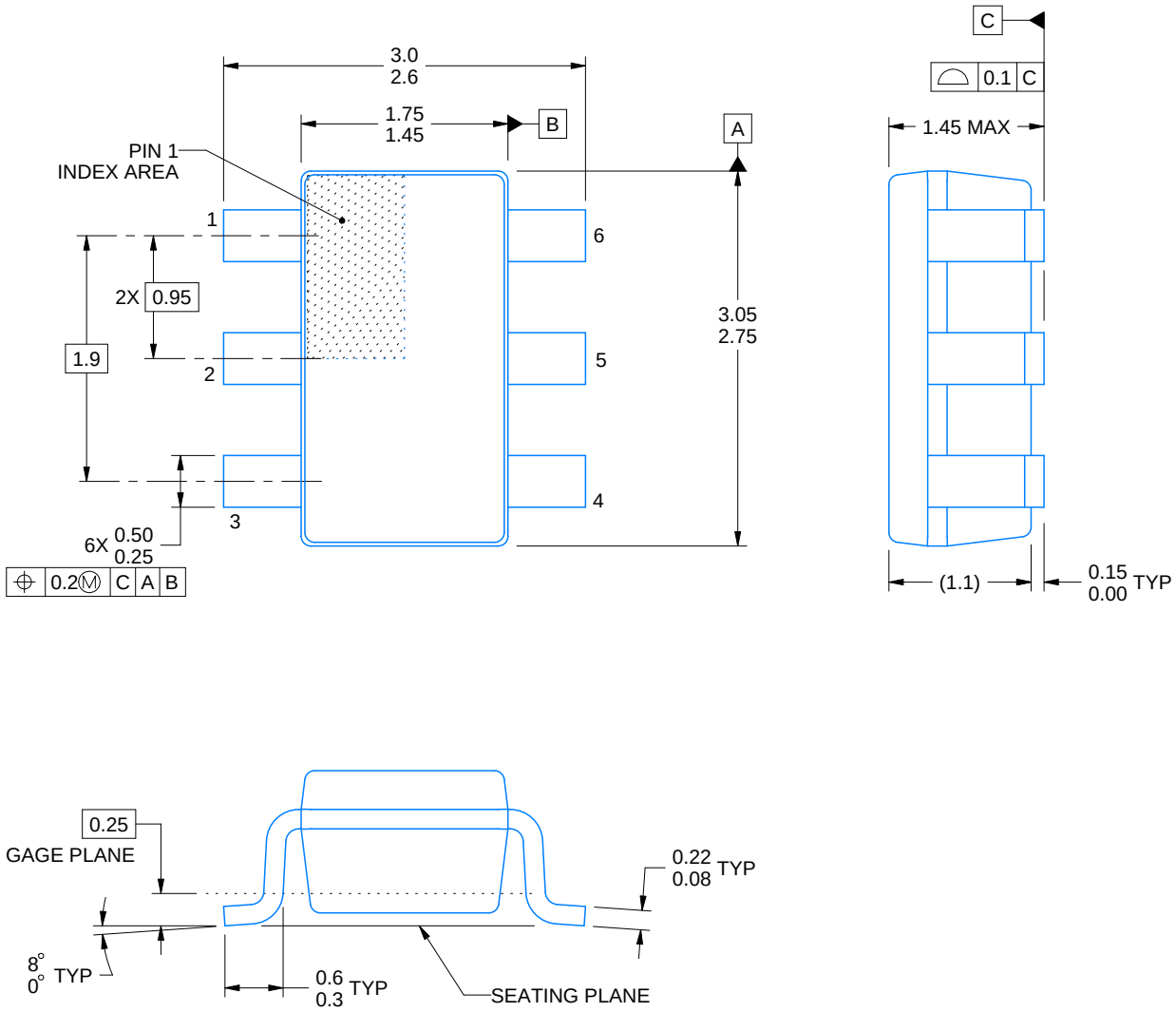
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

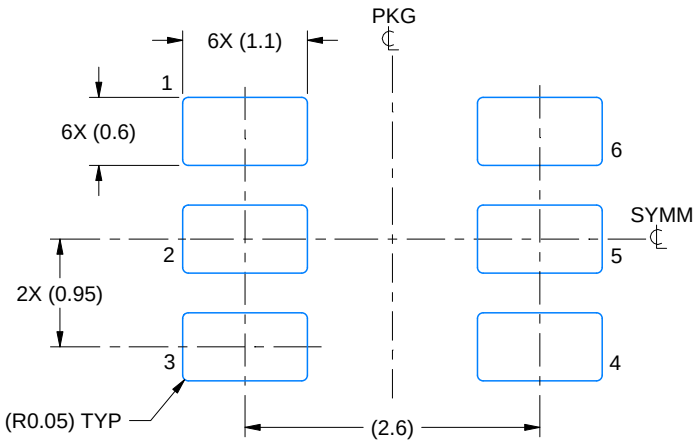
SMALL OUTLINE TRANSISTOR



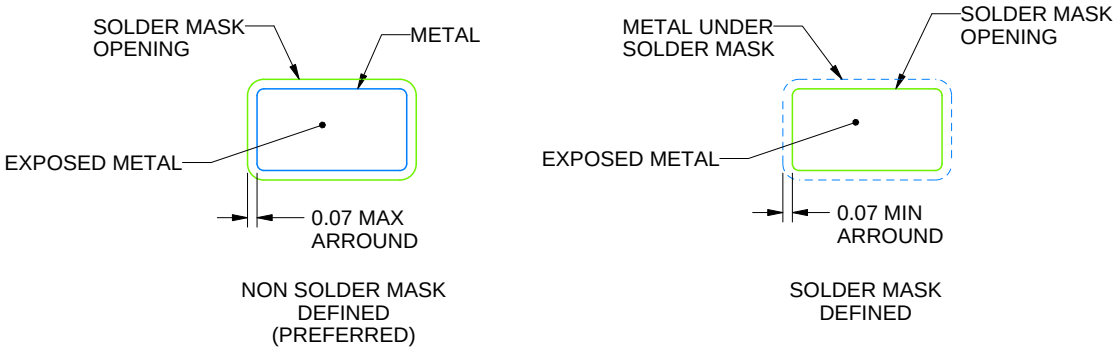
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

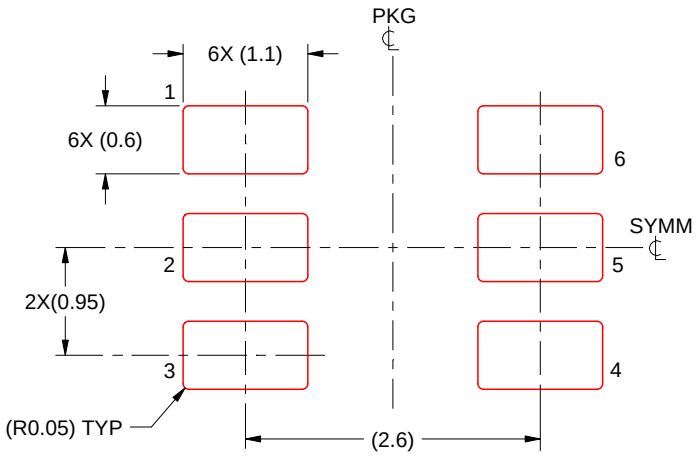


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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