LMR70503 SIMPLE SWITCHER® Buck-Boost Converter For Negative Output Voltage in µSMD

Check for Samples: LMR70503

FEATURES

- **Tiny 8-Bump Thin DSBGA Package: 0.84 mm × 1.615 mm × 0.6 mm**
- **2.8 V to 5.5 V Input Voltage Range**
- **Adjustable Output Voltage: -0.9 V to -5.5 V**
- **320 mA Switch Current Limit**
- **500 kHz Minimum Switching Frequency**
- **Ground Referred Enable Input**
- **Under Voltage Lock Out (UVLO)**
- **No External Compensation**
- **Internal Soft Start**
- **1 µA Shutdown Supply Current**
- **Small Output Voltage Ripple**
- **WEBENCH® Enabled**

APPLICATIONS

- **General Purpose Negative Voltage Supply**
- **Negative Rail / Bias Supply For Op-amp And Data Converters**
- **LCD Biasing**

PERFORMANCE BENEFITS

- **Easy To Use**
- **Tiny Overall Solution Size Reduces System Cost**

DESCRIPTION

The LMR70503 is a buck-boost converter with adjustable negative output voltage in a tiny 8-bump thin DSBGA package. Its unique control method is designed to provide fast transient response, low output noise, high efficiency, and tight regulation in the smallest possible PCB area. The LMR70503 has built in soft start, peak current limit, minimum switching frequency, and Under Voltage Lock Out (UVLO), with no external compensation required. For ease of use, the Enable pin is referred to the IC ground, instead of the lowest potential of the IC: the negative output voltage.

System Performance

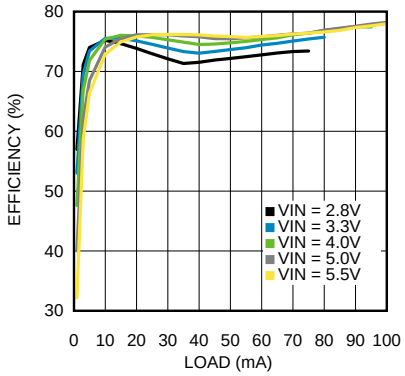


Figure 1. Efficiency, V_{OUT}= -5.0 V

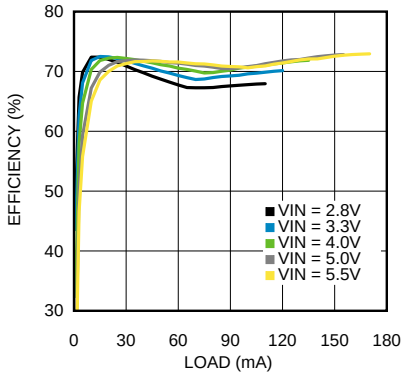
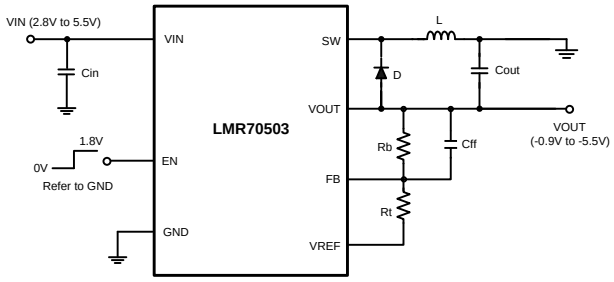


Figure 2. Efficiency, V_{OUT}= -2.5 V

Typical Application Circuit



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Connection Diagram

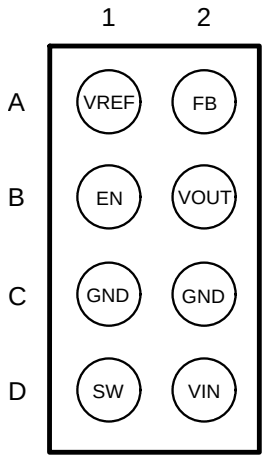


Figure 3. LMR70503 Bump Locations - Top View

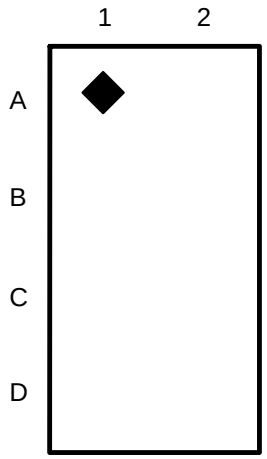


Figure 4. LMR70503 Package Marking - Top View (Diamond Denotes Bump A1)

PIN DESCRIPTIONS

Pin Number	Name	Description
A1	VREF	Reference voltage output; connect to the bottom feedback resistor.
B1	EN	Active high enable input for the device. Enable voltage level is referred to GND. Device must be enabled only with the presence of valid VIN (2.8 V to 5.5 V). The peak of the Enable input voltage must always lower than VIN voltage.
C1, C2	GND	Analog ground for internal bias circuitry.
D1	SW	Switch node pin, connected to the internal high side MOSFET. The cathode of the external Schottky diode must be connected as close as possible to this pin, in order to reduce inductance in the discontinuous current path.
A2	FB	FB is connected to VOUT and VREF through two feedback resistors. It is compared to GND to regulate the output voltage.
B2	VOUT	Output voltage. The anode of the external Schottky diode and output filter capacitor(s) should be connected to this pin.
D2	VIN	Power supply input pin, connected to the internal high side MOSFET and powers the internal circuity.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

VIN to GND	-0.5 V to 6.0 V
VOUT to GND	-6.5 V to 0.5 V
SW to GND	-6.5 V to VIN +0.2 V
EN to GND	-0.5 V to VIN
FB to GND	-0.5V to 5.5V
ESD Rating(3)	±2 kV
Junction Temperature	150 °C
Storage Temperature Range	-65 °C to 150 °C
For Soldering Specs see: SNOA549	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) ESD using the human body model which is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD22–A114.

OPERATING RATINGS

Input Voltage Range (V_{IN})	2.8 V to 5.5 V
Output Voltage Range (V_{OUT})	-0.9 V to -5.5 V
Junction Temperature Range (T_J)	-40°C to 125°C

ELECTRICAL CHARACTERISTICS

Specifications with standard typeface are for T_J = 25°C only; limits in bold face type apply over the operating junction temperature (T_J) range of -40 °C to +125 °C. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = 3.3 V, V_{OUT} = -5.0 V, V_{EN} = 1.8 V, unless otherwise indicated in the conditions column.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{REF}	Reference Voltage	R_{REF}=100 kΩ to GND	**1.166**	1.19	**1.214**	V
I_{SD}	Shutdown Current	EN = 0 V V_{IN} = 5.5 V		0.01	**1**	µA
I_Q	Quiescent Current	EN = 1.8 V, V_{IN} = 5.5 V, No Switching		245	**300**	µA
$UVLO_{RISE}$	V_{IN} Under Voltage Lock Out Threshold - Rising			2.55	**2.7**	V
$UVLO_{HYS}$	V_{IN} Under Voltage Lock Out Hysteresis Band		**0.1**	0.13		V
$V_{EN-RISE}$	EN Input Voltage Rising Threshold	V_{IN} = 5.5 V		1.05	**1.2**	V
V_{EN-HYS}	EN Input Voltage Threshold Hysteresis	V_{IN} = 5.5 V	**0.1**	0.15		V
I_{EN}	Enable Current			30		nA
I_{FB}	FB pin current			10		nA
F_{SW-MIN}	Minimum Switching frequency		**400**	500		kHz
T_{ON-MIN}	Minimum High Side Switch On Time	Load = 0 A		70		ns
R_{DSON}	Switch On State Resistance	V_{IN} = 2.8V		1.1	**2**	Ω

(1) Min and Max limits are 100% production tested at an ambient temperature (T_A) of 25 °C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical specifications represent the most likely parametric norm at 25°C operation.

ELECTRICAL CHARACTERISTICS (continued)

Specifications with standard typeface are for T_J = 25°C only; limits in bold face type apply over the operating junction temperature (T_J) range of -40 °C to +125 °C. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = 3.3 V, V_{OUT} = -5.0 V, V_{EN} = 1.8 V, unless otherwise indicated in the conditions column.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
$I_{PEAK-CL}$	Switch Peak Current limit (3)		**270**	320	**370**	mA
$TSD_{TH-HIGH}$	Thermal Shutdown Threshold - Rising	Junction Temperature		165		°C
TSD_{HYS}	Thermal Shutdown Hysteresis Band	Junction Temperature		10		°C

(3) The switch peak current limit is internally trimmed. The actual peak current limit observed on the applications are dependant on the input voltage V_{IN}, inductance value L and junction temperature T_J.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, the following conditions apply: V_{IN} = 3.3 V, V_{OUT} = -5.0 V, V_{EN} = 1.8 V, C_{IN} = 10 µF 6.3 V X5R ceramic capacitor; C_{OUT} = 2 × 22 µF 6.3 V X5R ceramic capacitor; L = 6.8 µH (VLS2012ET-6R8M); $T_{AMBIENT}$ = 25 °C.

Efficiency, V_{OUT} = -5.0 V

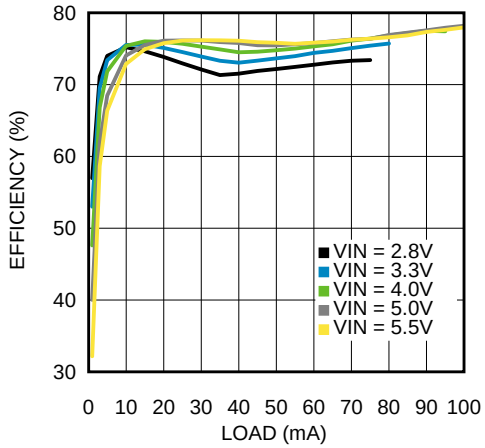


Figure 5.

Output Regulation, V_{OUT} = -5.0 V

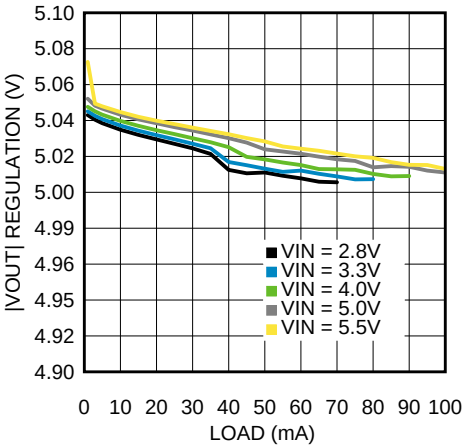


Figure 6.

Efficiency, V_{OUT} = -3.3 V

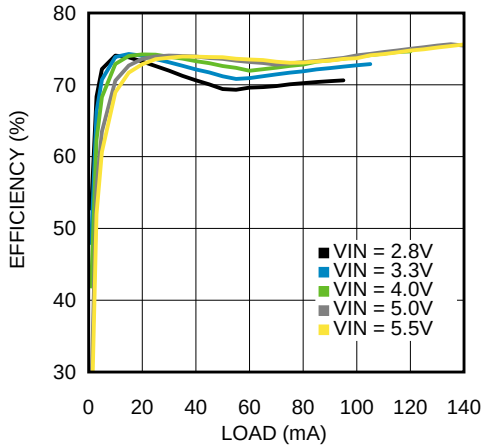


Figure 7.

Output Regulation, V_{OUT} = -3.3 V

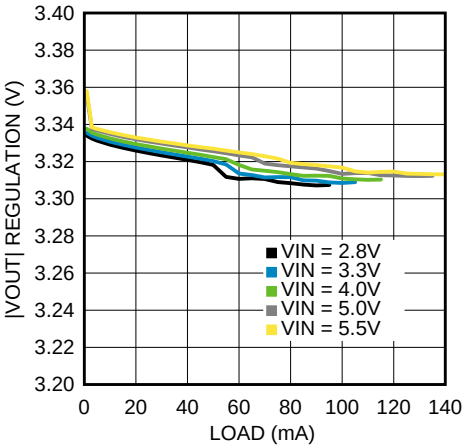


Figure 8.

Efficiency, V_{OUT} = -2.5 V

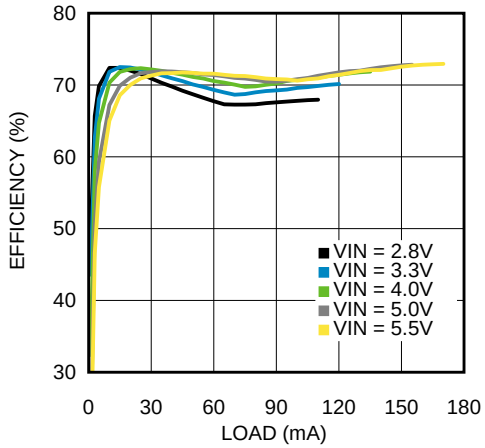


Figure 9.

Output Regulation, V_{OUT} = -2.5 V

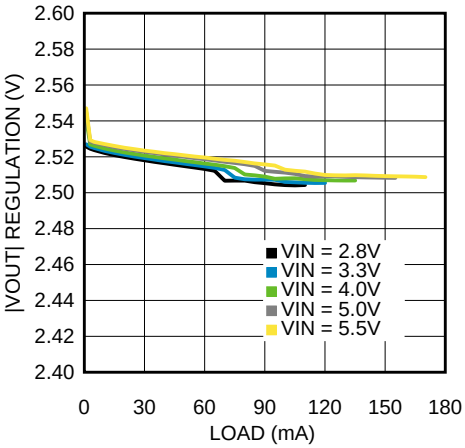


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 3.3 V, V_{OUT} = -5.0 V, V_{EN} = 1.8 V, C_{IN} = 10 µF 6.3 V X5R ceramic capacitor; C_{OUT} = 2 × 22 µF 6.3 V X5R ceramic capacitor; L = 6.8 µH (VLS2012ET-6R8M); $T_{AMBIENT}$ = 25 °C.

Efficiency, V_{OUT} = -1.5 V

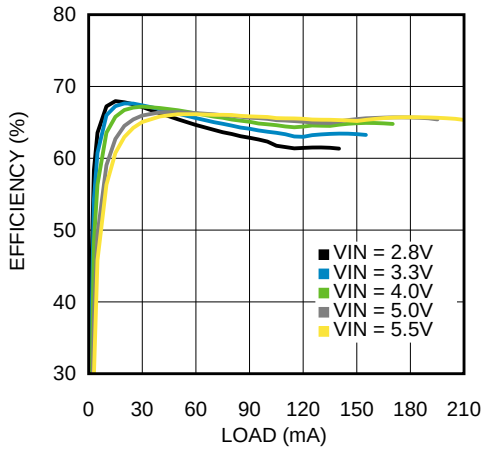


Figure 11.

Output Regulation, V_{OUT} = -1.5 V

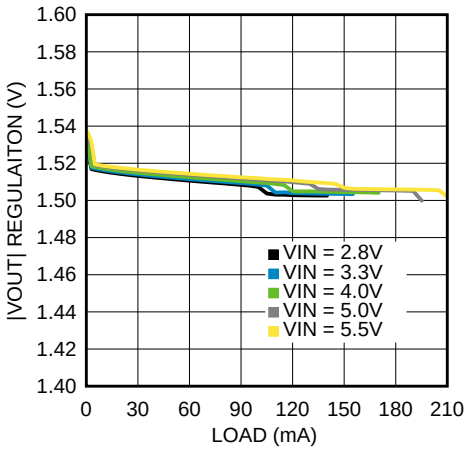


Figure 12.

Efficiency, V_{OUT} = -0.9 V

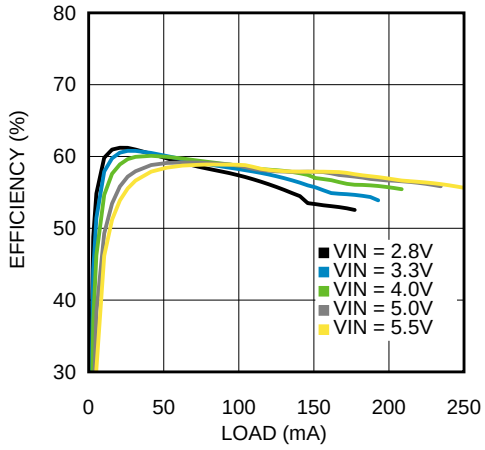


Figure 13.

Output Regulation, V_{OUT} = -0.9 V

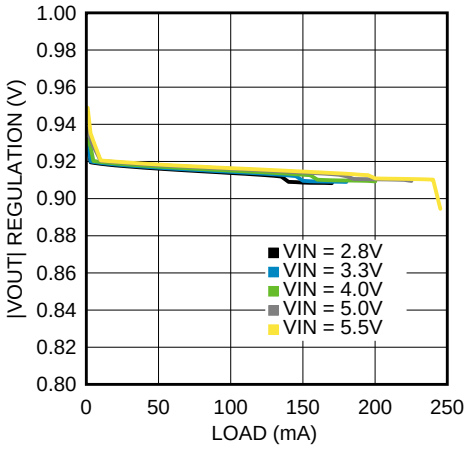


Figure 14.

Maximum Load Current

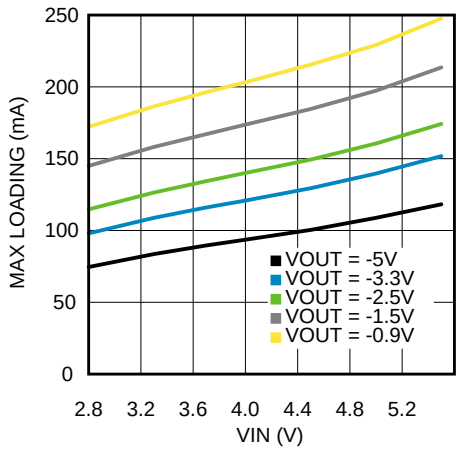


Figure 15.

Minimum Switching Frequency

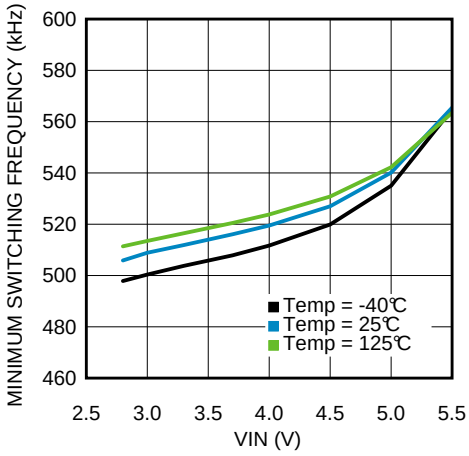


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 3.3 V, V_{OUT} = -5.0 V, V_{EN} = 1.8 V, C_{IN} = 10 µF 6.3 V X5R ceramic capacitor; C_{OUT} = 2 × 22 µF 6.3 V X5R ceramic capacitor; L = 6.8 µH (VLS2012ET-6R8M); $T_{AMBIENT}$ = 25 °C.

No Load Supply Current

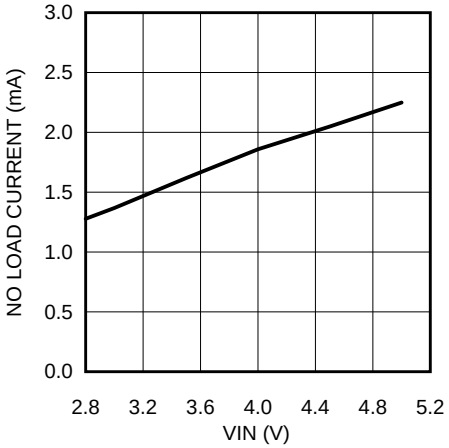


Figure 17.

Rds-on

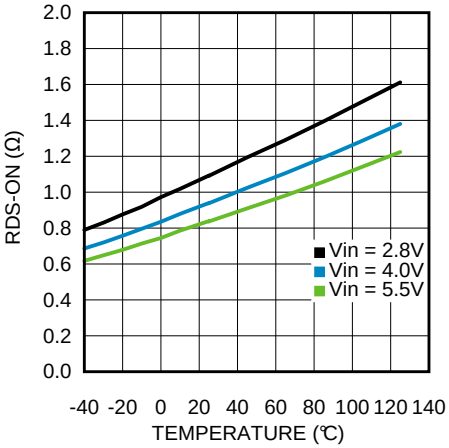


Figure 18.

Enable Thresholds

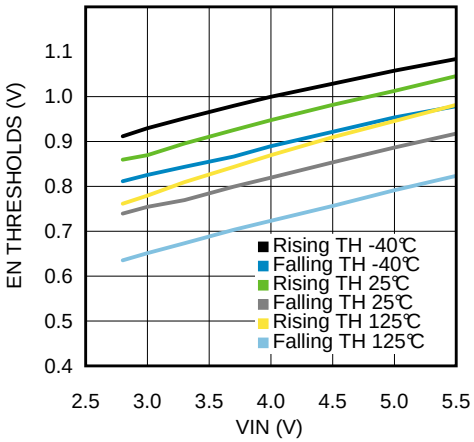


Figure 19.

Soft Start Time (No Load)

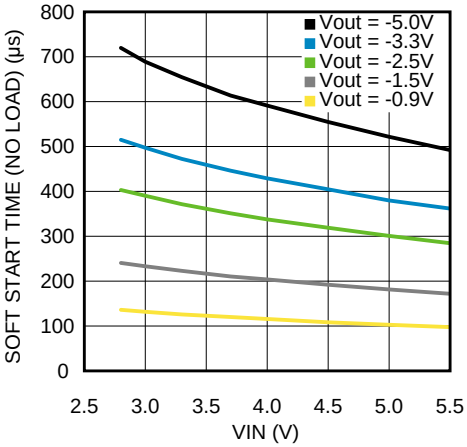


Figure 20.

Soft Start Delay Time (From EN Rising Edge)

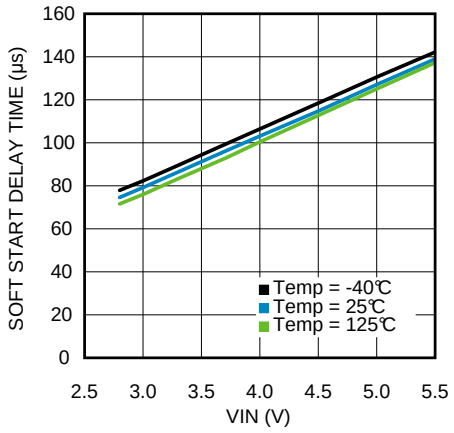


Figure 21.

Soft Off Time, V_{OUT} = -5.5 V (No Load, From EN Falling Edge)

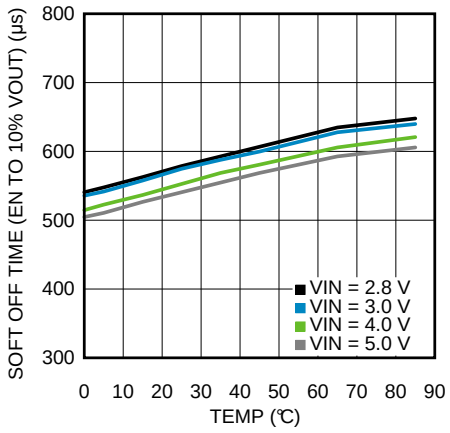


Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 3.3 V, V_{OUT} = -5.0 V, V_{EN} = 1.8 V, C_{IN} = 10 µF 6.3 V X5R ceramic capacitor; C_{OUT} = 2 × 22 µF 6.3 V X5R ceramic capacitor; L = 6.8 µH (VLS2012ET-6R8M); $T_{AMBIENT}$ = 25 °C.

Soft Start And Soft Off Waveform
V_{IN} = 5.0 V, V_{OUT} = -5.0 V, No Load

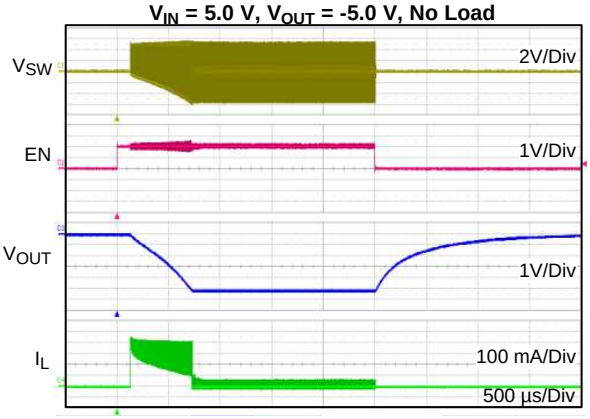


Figure 23.

Soft Start And Soft Off Waveform
V_{IN} = 5.0 V, V_{OUT} = -5.0 V, Load = 50 Ω

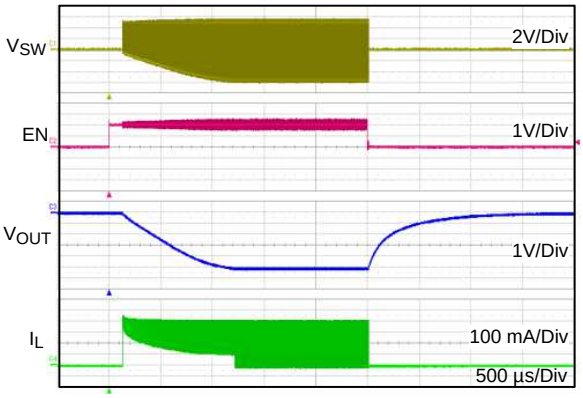


Figure 24.

Typical Switching Waveform
V_{IN} = 5.0 V, V_{OUT} = -5.0 V, No Load

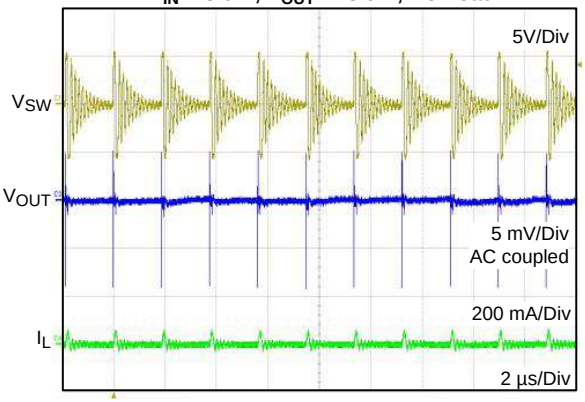


Figure 25.

Typical Switching Waveform
V_{IN} = 5.0 V, V_{OUT} = -5.0 V, I_{OUT} = 70 mA

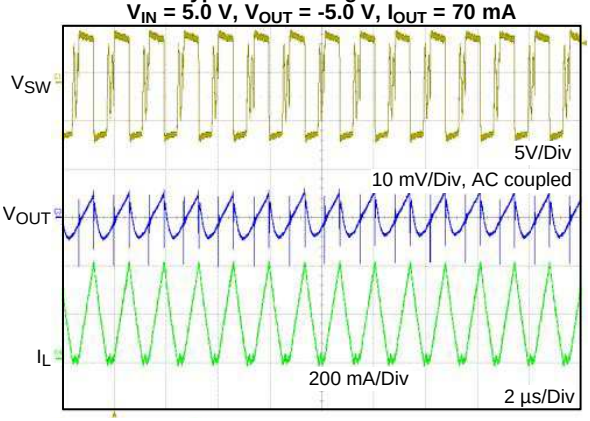


Figure 26.

Load Transient, V_{IN} = 4.0 V, V_{OUT} = -5.5 V
Load steps between 2 mA and 50 mA

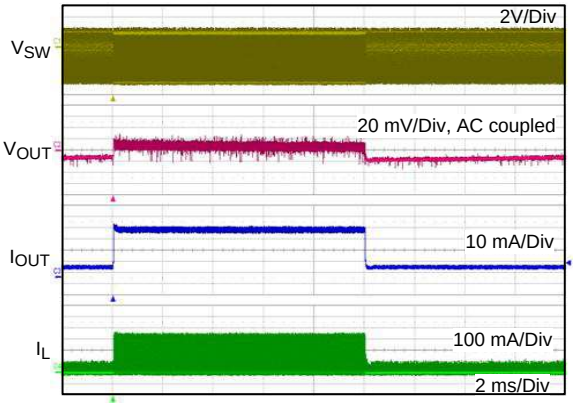


Figure 27.

Short Circuit Waveform
V_{IN} = 5.0 V, V_{OUT} = -5.5 V

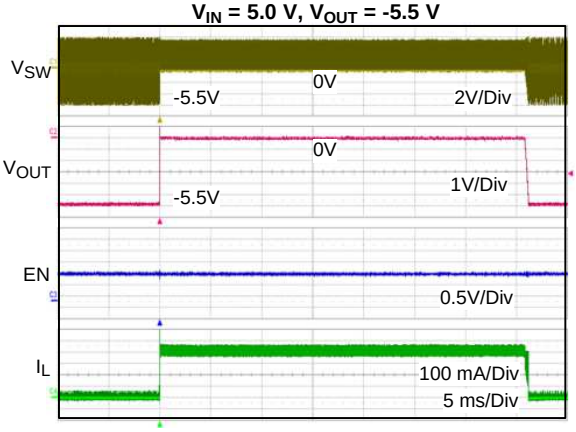
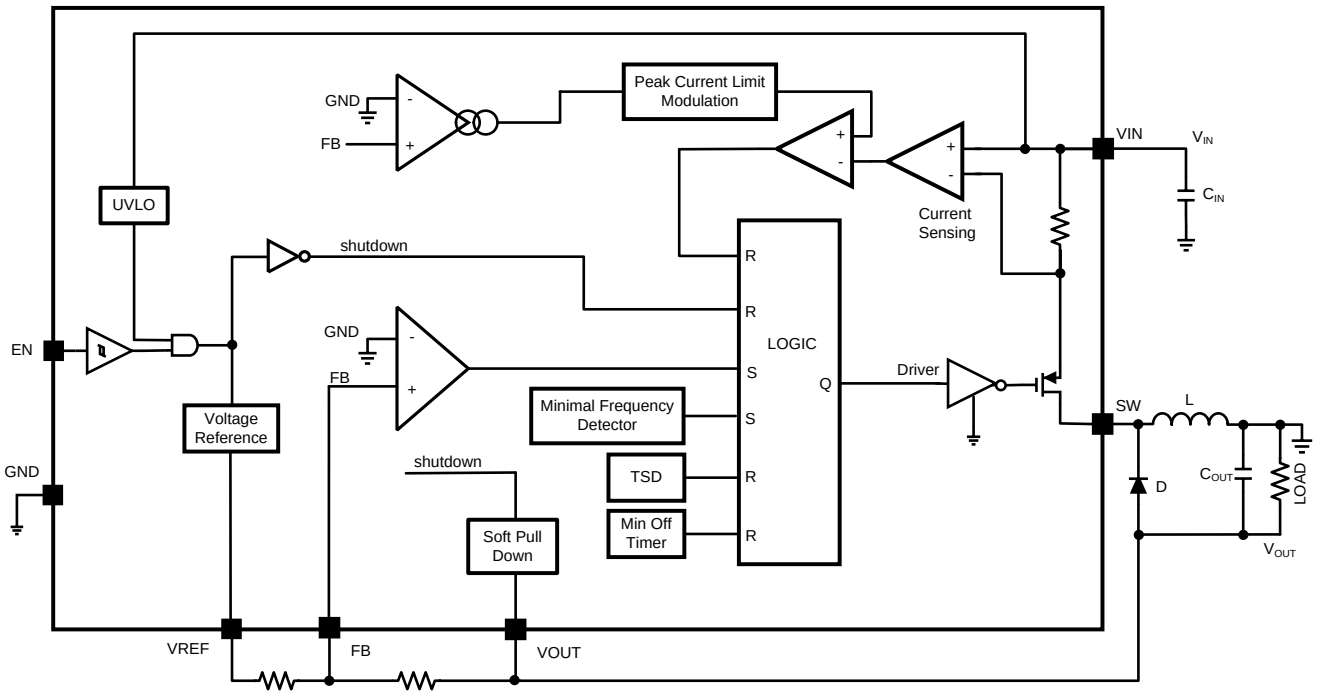


Figure 28.

BLOCK DIAGRAM



OPERATING DESCRIPTION

The LMR70503 integrates an inverting buck-boost controller and a high-side MOSFET in one tiny 8-bump thin DSBGA package. A simplified buck-boost converter schematic is shown in Figure 29.

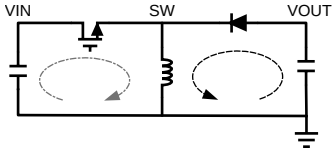


Figure 29. Buck Boost Converter

The LMR70503 controller incorporates a unique peak current mode control method with a minimum switching frequency limit. The integrated switch is turned off when its current crosses the peak current limit, while it is turned on when the magnitude of V_{OUT} droops below a threshold. When the switch is off, the inductor current goes through the diode and charges the output capacitor(s). With fixed peak current limit, the switching frequency decreases with decreased load current. At light load, the switching frequency will decrease to the audible frequency range, which is not acceptable in many applications. The LMR70503 is designed to operate with peak current mode control and limit the switching frequency to 500 kHz (typical) minimum, to avoid audible frequency interference. At light load, when the switching frequency drops to the minimum, the inductor current limit is reduce instead of frequency to maintain regulation. The LMR70503 also incorporates an internal dummy load to compensate for the extra charges in the minimum ON-time (T_{ON-MIN}) condition. More details on the LMR70503 operation are described in the later sessions. Typical switching waveforms in discontinuous conduction mode (DCM) and continuous conduction mode (CCM), including the inductor current, the switch node voltage and the output voltage ripple (absolute value), are shown in Figure 30.

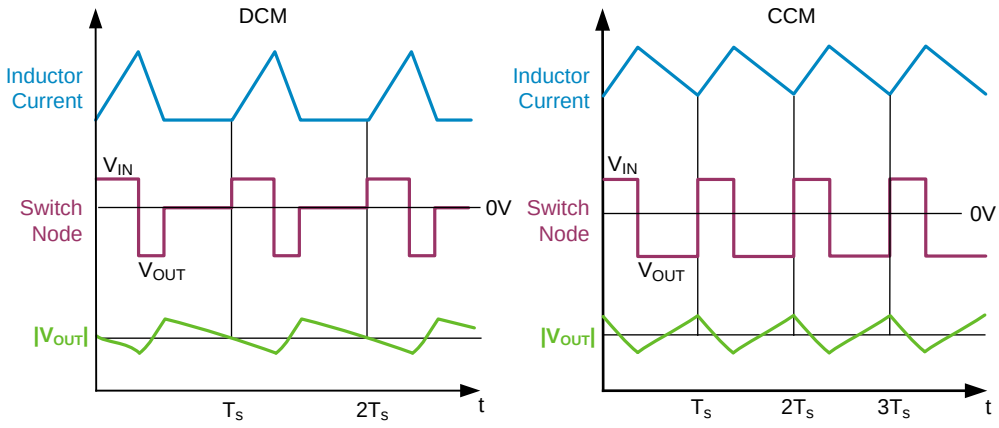


Figure 30. Typical Waveforms In Buck Boost Converter

Figure 31 illustrates the switching frequency, the peak current limit, the output voltage and the dummy load with different load current. More details on each operation mode will be described later.

1. No load to very light load: high side switch is turned on for T_{ON-MIN}; switching frequency is limited at the minimum switching frequency; and the dummy load is turned on.
2. Light load: switching frequency is limited at the minimum switching frequency, peak current limit increases with increased load current; and the dummy load is off.
3. Heavy load: peak current equals the maximum peak current limit; switching frequency increases with increased load current; and the dummy load is off.

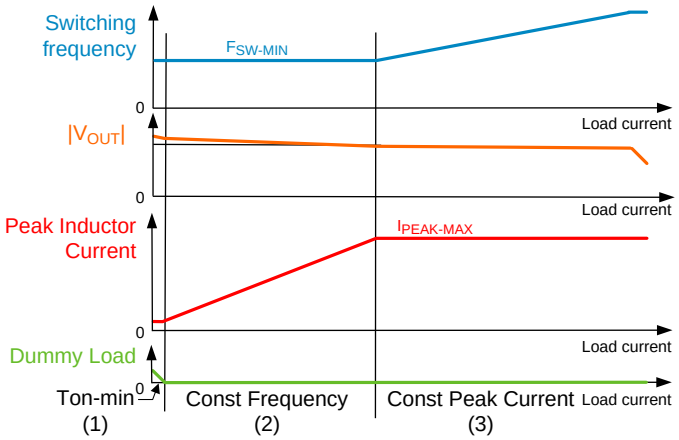


Figure 31. The LMR70503 Operation Modes vs. Load Current

Minimum Switching Frequency Operation

In a typical peak current mode controlled DC-DC converter, the peak current limit is constant and the switching frequency decreases when load current reduces. To maintain low noise operation and avoid audio frequency interference, the minimum switching frequency of the LMR70503 is limited at 500 kHz typically. At heavy load, the peak current limit remains constant and the switching frequency varies with the load to regulate the output voltage. With reduced loading, the absolute output voltage is going to be charged higher than regulation if the switching frequency cannot decrease accordingly. Therefore, to regulate the output voltage with minimum frequency at light load, the peak current limit is reduced, in proportional to the output voltage offset.

In this mode, as shown in Figure 31, the switching frequency is fixed to the minimum switching frequency, the peak inductor current increases with load current, and the output voltage magnitude has a small offset above regulation.

Minimum ON-Time and Dummy Load

When load current is near zero, the peak inductor current can not reduce further due to T_{ON-MIN} of the high side switch. Under such conditions, an internal dummy load is turned on by sensing excessive output voltage offset, which removes the extra charge from the output capacitor(s). In this condition, the switching frequency is fixed to the minimum value. The peak inductor current value is at its minimum value, as shown in Figure 31. The dummy load current is zero when the LMR70503 operates with on time higher than T_{ON-MIN}.

The minimum peak inductor current is determined by

$$I_{PEAK-MIN} = T_{ON-MIN} \times V_{IN} / L \quad (1)$$

where

- V_{IN} is the supply voltage
- L is the inductance value

The peak inductor current is higher with higher V_{IN}. The inductor current falling slew rate is determined by

$$SR_{FALLING} = (|V_{OUT}| + V_F) / L \quad (2)$$

where

- $|V_{OUT}|$ is the absolute value of the output voltage
- V_F is the forward voltage drop of the power diode

At lower $|V_{OUT}|$, it takes longer time to discharge the inductor current to zero. Therefore, there is more energy to charge the output capacitor(s). The output voltage will have more offset at higher V_{IN} and lower V_{OUT}. The dummy load current is a function of the FB voltage: the more the offset at the FB node, the higher the dummy load current, as shown in Figure 32.

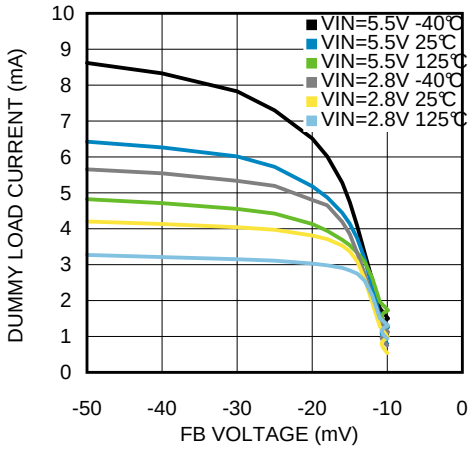


Figure 32. Dummy Load Current vs. FB Voltage

Constant Peak Current Operation

If the load current increases in the minimum switching frequency mode, the peak current limit will reach the maximum peak current limit ($I_{PEAK-MAX}$). After this point, the LMR70503 behaves as a constant peak current converter with frequency modulation. The transition load level between the constant frequency mode and the constant peak current mode varies with V_{IN}, V_{OUT} and L.

The $I_{PEAK-MAX}$ is trimmed to 320 mA in the LMR70503. Due to propagation delays in the comparator and gate drive, the measured peak inductor current will be higher than the trimmed value. The additional offset on the maximum peak current is proportional to the inductor current rising slope: V_{IN} / L, approximately. For a typical inductor, the inductance will reduce at hot temperature. Therefore, $I_{PEAK-MAX}$ is the highest with 5.5 V input voltage at hot temperature.

In the constant peak current operation mode, the switching frequency will increase with the increased load current, until the high side switch off time equals the minimum off-time ($T_{OFF-MIN}$) limit. If the load keeps increasing when the switch operates with $T_{OFF-MIN}$, V_{OUT} will drop out of regulation due to loading limits of buck-boost type of converters. The maximum loading capability is higher with higher V_{IN}, larger L, lower V_{OUT}, and less losses in the converter. Figure 33 shows the measured maximum load current measured with the typical BOM shown in Table 1. To increase the maximum loading capability with given V_{IN} and V_{OUT}, one can choose a higher inductance value and a diode with lower forward voltage drop V_F.

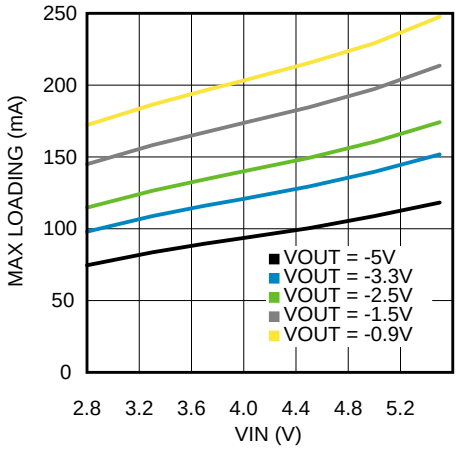


Figure 33. LMR70503 Loading Capability vs. V_{IN}, L = 6.8 µH

The built-in $T_{OFF-MIN}$ time is a function of both V_{IN} and V_{OUT}, as shown in Figure 34.

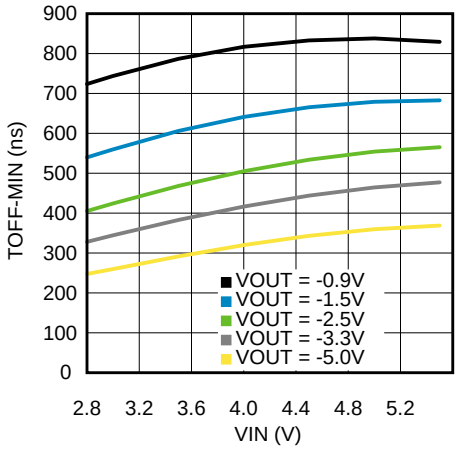


Figure 34. Minimum Off Time vs. V_{IN} at room temperature

Enable And UVLO

The LMR70503 features an enable (EN) pin and associated comparator to allow the user to easily sequence the LMR70503 from an external voltage rail, or to manually set the input UVLO threshold. Enable threshold levels are referred to the LMR70503 ground, instead of the lowest potential: the negative output voltage. Enable turning on (rising) and turning off (falling) thresholds are shown in Figure 35.

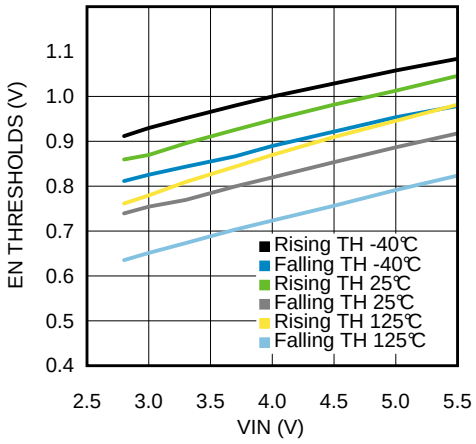


Figure 35. Enable Rising And Falling Thresholds vs. V_{IN}

It is important to ensure that a valid input voltage (2.8 V ≤ V_{IN}≤ 5.5 V) is present on the VIN pin before the EN input is asserted. Also, as stated in the Absolute Maximum Ratings section of this data sheet, the voltage on the EN pin must always be less than V_{IN}. This applies to both static and dynamic operation, and during start up and shut down sequences. If these precautions are not followed, an internal test mode may be activated; possibly damaging the regulator. The EN input must not be left floating. A resistor divider can be added from VIN to EN if an external enable signal is not available.

An input under voltage lock-out (UVLO) circuit prevents the regulator from turning on when the input voltage is not great enough to properly bias the internal circuitry. The typical UVLO rising threshold is 2.55 V and typical hysteresis band is 0.13 V.

Soft Start And Soft Off

The LMR70503 begins to operate when EN goes high with the presence of valid V_{IN}, or V_{IN} swings below UVLO level and back up with the presence of valid EN voltage. The soft start action is inherent with the maximum peak current limit and minimum off time. During start up, the inductor current rises to the maximum peak current limit, then the high-side switch is turned off for $T_{OFF-MIN}$ and the output capacitor(s) is charged during this time. Then the high-side turns on to repeat the cycle. After the output voltage is charged to the regulation level, the LMR70503 will operate in steady state. The soft start time will be longer with more output capacitance, and / or lower supply voltage V_{IN}, and / or more loading during start up. Figure 36 shows soft start vs V_{IN} with L= 6.8 µH and no load. Soft-start is reset any time the part is shut down or a thermal shutdown event occurs.

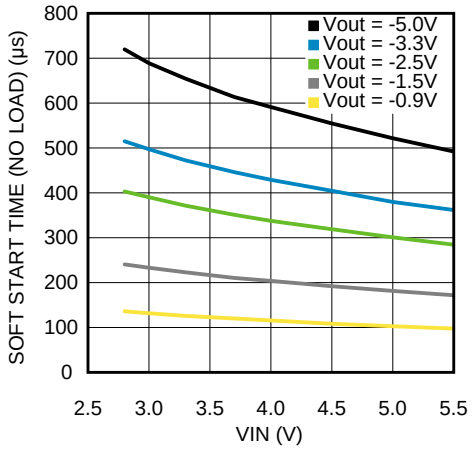


Figure 36. Soft Start Time (No Load) vs. V_{IN}

The LMR70503 will shutdown when EN pin voltage goes below the falling threshold, or V_{IN} goes below UVLO falling threshold. When shutdown, the LMR70503 incorporates an output voltage discharge feature to bring the output voltage to zero volts, regardless of the load current. When the EN input is taken below its lower threshold, an internal MOSFET turns on and discharges the output capacitors. Typical soft off times (from EN falling edge to 10% of Vout) over V_{IN} and temperature are shown in Figure 37. Figure 38 shows the typical off time from 90% to 10% of Vout.

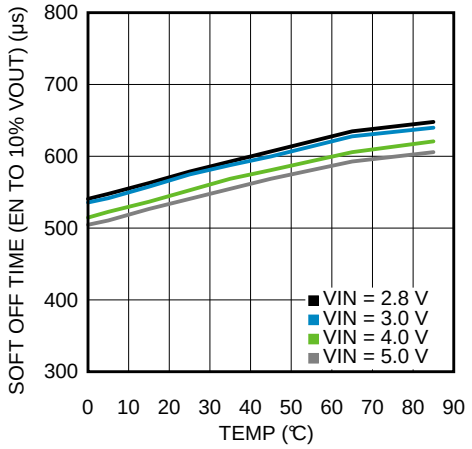


Figure 37. Soft Off Time (EN Falling Edge To 10% Vout) vs. Temperature, V_{OUT} = -5.5 V, No Load

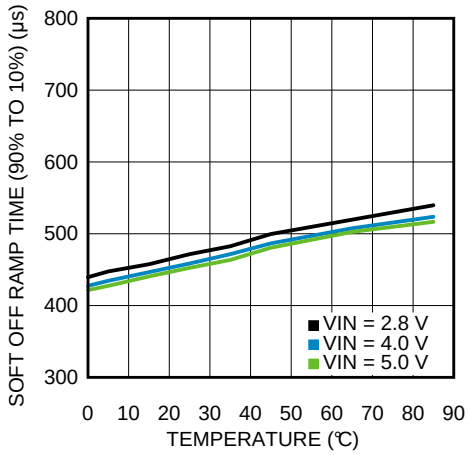


Figure 38. Soft Off Time (90% To 10% Vout) vs. Temperature, V_{OUT} = -5.5 V, No Load

Short Circuit Protection

Peak current mode control has inherent short circuit protection. The protection level is the maximum inductor current limit level. It varies with V_{IN} and temperature due to propagation delays. The minimum off-time limits the current going through the inductor during a short circuit condition.

Over-Temperature Protection

Internal thermal shutdown (TSD) circuitry protects the LMR70503 should the maximum junction temperature be exceeded. This protection is activated at 165 °C (typical), with the result that the regulator will shutdown until the junction temperature drops below 155 °C (typical). Of course the LMR70503 must not be operated continuously above 125 °C.

Design Guide

Output Voltage Setting

The output voltage of the LMR70503 is programmable by the voltage divider resistors. The reference voltage is typically 1.19 V. To avoid overloading the V_{REF} circuity, the resistor R_T tied between V_{REF} and FB is recommended to be between 20 kΩ and 100 kΩ. With a selected R_T, R_B tied between V_{OUT} and FB can be found by

$$R_B = R_T * |V_{OUT}| / V_{REF} \quad (3)$$

A feed-forward capacitor C_{FF} can be used between V_{OUT} and FB nodes to improve transient performance. 10 pF C0G, NP0 type of capacitor is recommended in LMR70503 applications.

Input Capacitor And Output Capacitor Selection

The input capacitor selection is based on both input voltage ripple and RMS current. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the regulator current during switch on-time. Low ESR ceramic capacitors are preferred. A minimum value of 10µF at 6.3 V, is required at the input of the LMR70503. Larger values of input capacitance are desirable to reduce voltage ripple and noise on the input supply.

The output capacitor is responsible for filtering the output voltage and suppling load current during transients and during the power diode off-time. Best performance is achieved with ceramic capacitors. For most applications, a minimum value of 22 µF, 6.3 V capacitor is required at the output of the LMR70503. The percentage of ripple coupled to the FB node can be found by

$$\text{RIPPLE PERCENTAGE} = V_{REF} / (|V_{OUT}| + V_{REF})$$

where

- $|V_{OUT}|$ is the magnitude of the output voltage
- V_{REF} is the reference voltage (4)

With lower magnitude V_{OUT}, a higher percentage of output voltage ripple is coupled to the FB node. Output voltage ripple is also coupled to the FB node via the feed-forward capacitor C_{FF}. Excessive ripple at the FB node may trigger peak current limit modulation causing unstable operation. Higher output capacitance is needed at lower magnitude output voltage. For V_{OUT} = -0.9 V, a minimum of 44 µF, 6.3 V capacitor is required. Avoid using too much capacitance at C_{FF}.

A capacitor between V_{IN} and V_{OUT} also can be used to provide high frequency bypass. This capacitor is equivalent to the output capacitors in the small signal model. It also reduces the output voltage ripple if sufficiency capacitance is used. The voltage rating for this capacitor should be higher than $V_{IN} + |V_{OUT}|$.

All ceramic capacitors have large voltage coefficients, in addition to normal tolerances and temperature coefficients. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum capacitance up to the desired value. This may also help with RMS current constraints by sharing the current among several capacitors. With the LMR70503, ceramic capacitors rated at 6.3 V, or higher, are suitable for all input and output voltage combinations. Many times it is desirable to use an electrolytic capacitor on the input, in parallel with the ceramics. The moderate ESR of this capacitor can help to damp any ringing on the input supply caused by long power leads. This method can also help to reduce voltage spikes that may exceed the maximum input voltage rating of the LMR70503.

Power Inductor Selection

The power inductor selection is critical to the operation of the LMR70503. It affects the efficiency, the operation mode transition point, the maximum loading capability and the size / cost of the solution. A 4.7 µH or 6.8 µH inductor is recommended for most LMR70503 applications. The maximum loading capability is reduced with smaller inductance value. The no load V_{OUT} offset is higher at low V_{OUT} with smaller inductance value, due to higher peak current with the same T_{ON-MIN}. Higher inductance value usually comes with higher DCR with the same size and cost. Higher DCR will reduce the efficiency especially at heavy load.

The inductor must be rated above the maximum peak current limit to prevent saturation. Good design practice requires that the inductor rating be adequate for the maximum $I_{PEAK-MAX}$ over V_{IN} and temperature, plus some safety margin. If the inductor is not rated for the maximum expected current, saturation at high current may cause damage to the LMR70503 and/or the power diode. The DCR of the inductor should be as small as possible with given size / cost constrains to achieve optimal efficiency.

Power Diode Selection

A Schottky type power diode is required for all LMR70503 applications. The parameters of interests include the reverse voltage rating, the DC current rating, the repetitive peak current rating, the forward voltage drop, the reverse leakage current and the parasitic capacitance. In a buck-boost, this diode sees a reverse voltage of :

$$V_{R-DIODE} = |V_{OUT}| + V_{IN} \quad (5)$$

The reverse breakdown voltage rating of the diode should be selected for this value, plus safety margin. A good rule of thumb is to select a diode with a reverse voltage rating of 1.3 times this maximum. Select a diode with a DC current rating at least equal to the maximum load current that will be seen in the application and the repetitive peak current rating higher than $I_{PEAK-MAX}$ over V_{IN} and temperature. The forward voltage drop of the power diode is a big part of the power loss in a buck-boost converter. It is preferred to be as low as possible. The reverse leakage current and the parasitic capacitance are also part of the power losses in the converter, but usually less pronounced than the forward voltage drop loss. Pay attention to the temperature coefficients of all the parameters. Some of them may vary greatly over temperature and may adversely affect the efficiency over temperature.

PC Board Layout Guidelines

Board layout is critical for the proper operation of switching power converters. Switch mode converters are very fast switching devices. In such cases, the rapid increase of current combined with the parasitic trace inductance generates unwanted L·di/dt noise spikes. The magnitude of this noise tends to increase as the output current increases. This noise may turn into electromagnetic interference (EMI) and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise. The most important layout rule is to keep the AC current loops as small as possible.

Figure 29 shows the current flow in a buck-boost converter. The two dotted arrows indicate the current paths when the high side switch is on and when the power diode is on, respectively. The components and traces that contain discontinuous currents are critical in PCB layout design, since discontinuous currents contain high di/dt and high frequency noise. The components that carry critical discontinuous currents include the input capacitor(s), the high side switch, the power diode and the output capacitor(s). These components need to be placed as close as possible to each other and the traces between them must be made as short and wide as possible: place the input capacitor(s) as close as possible to the VIN pin of the LMR70503; place the cathode of the diode as close as possible to the SW pin; the anode of the diode should be as close as possible to the output capacitor(s); the GND end of the output capacitor(s) should be as close as possible to that of the input capacitor(s). Doing so will yield a small loop area, reducing the loop inductance and EMI.

The feedback resistors R_B and R_T should be placed as close as possible to the FB pin. Since FB is a high impedance node, noise is likely be coupled to the FB node if the trace is long. The traces from V_{OUT} to the resistor divider and from the divider to the FB pin should be far away from the discontinuous current path. It is recommended to use 4-layer board with ground plane as an internal layer, route the discontinuous current path on the top layer and the feedback path on the other side of the ground plane. Then the feedback path will be shielded from switching noise.

To avoid functional problems due to layout, review the PCB layout example in Figure 39. It is also recommended to use 1oz copper boards or heavier to help reducing the parasitic inductances of board traces.

PCB Layout Example

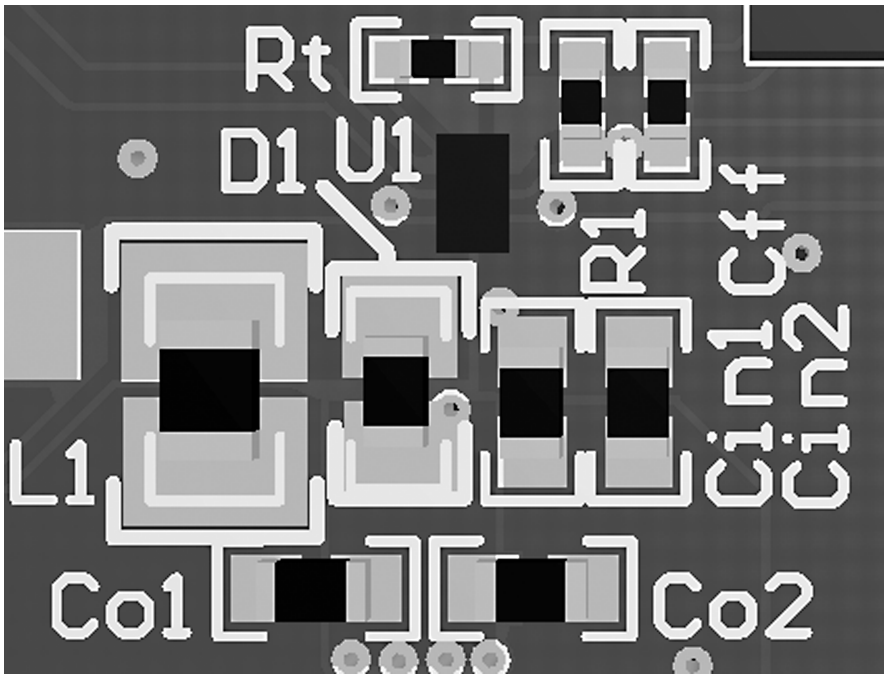
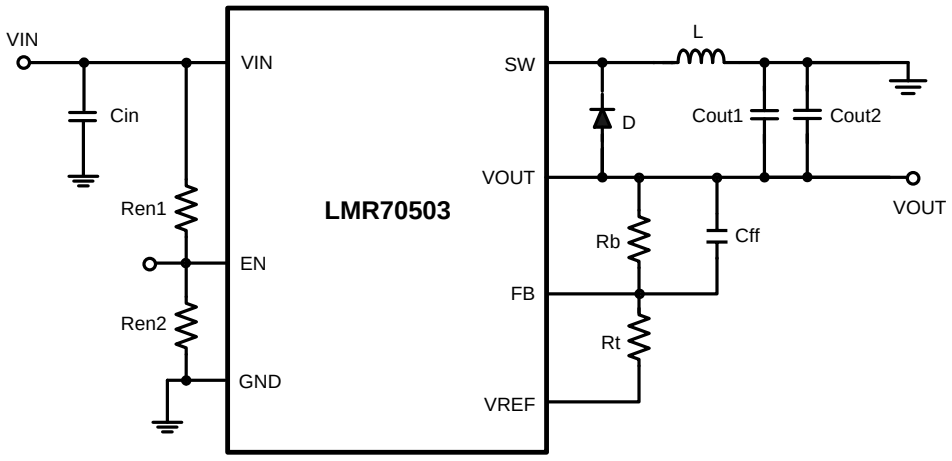


Figure 39. PCB Layout Example (top layer and top overlay)

LMR70503 Typical Application Circuit



LMR70503 Application Circuit Bill of Materials

V_{IN} = 2.8 V to 5.5 V, V_{OUT} has options of -0.9 V, -1.5 V, -2.5 V, -3.3 V and -5.0 V. Optimized for minimum solution size.

Table 1. Bill of Materials

Designator	Description	Case Size	Manufacturer	Manufacturer P/N
U1	Inverting Buck-Boost	8-bump thin DSBGA	Texas Instruments	LMR70503TM NOPB
C_{IN}	Ceramic 10 µF 10 V X5R 0603	0603	TDK	C1608X5R1A106M
C_{OUT1}, C_{OUT2}	Ceramic 22 µF 6.3 V X5R 0603	0603	TDK	C1608X5R0J226M
C_{ff}	CAP CER 10PF 50V 5% NP0 0402	0402	Murata	GRM1555C1H100JZ01D
D	Schottky 30 V 500 mA	SOD882	NXP Semi	PMEG3005EL
L	6.8 µH, 0.76 A 362 mΩ	2.0*2.0*1.2mm	TDK	VLS2012ET-6R8M
R_T	RES, 100k ohm, 1%, 0.063W, 0402	0402	Vishay Dale	CRCW0402100KFKED
R_B (1)	422 kΩ For Vout = -5.0V	0402	Vishay Dale	CRCW0402422KFKED
	274 kΩ For Vout = -3.3V	0402	Vishay Dale	CRCW0402274KFKED
	210 kΩ For Vout = -2.5V	0402	Vishay Dale	CRCW0402210KFKED
	127 kΩ For Vout = -1.5V	0402	Vishay Dale	CRCW0402127KFKED
	75 kΩ For Vout = -0.9V	0402	Vishay Dale	CRCW040275K0FKED
R_{EN1}, R_{EN2}	RES, 20k ohm, 5%, 0.063W, 0402	0402	Vishay Dale	CRCW040220K0JNED

(1) R_B is represented by R1 in Figure 39.

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR70503TM/NOPB	ACTIVE	DSBGA	YFX	8	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S3	Samples
LMR70503TMX/NOPB	ACTIVE	DSBGA	YFX	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

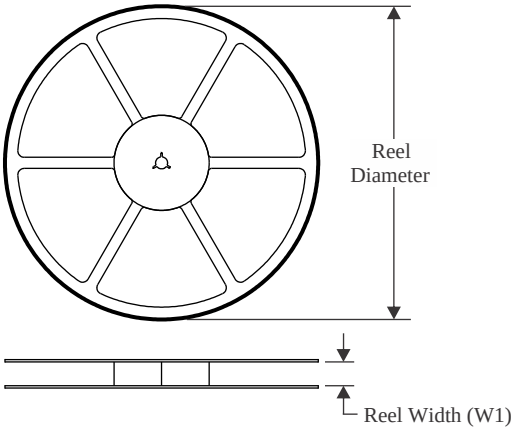
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

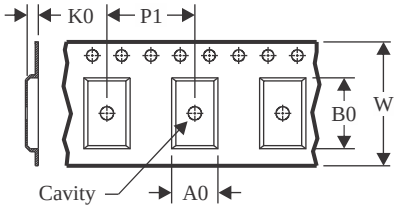
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

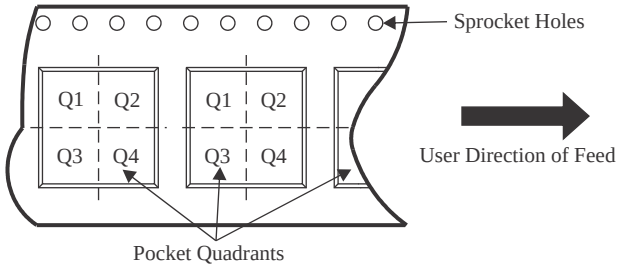


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

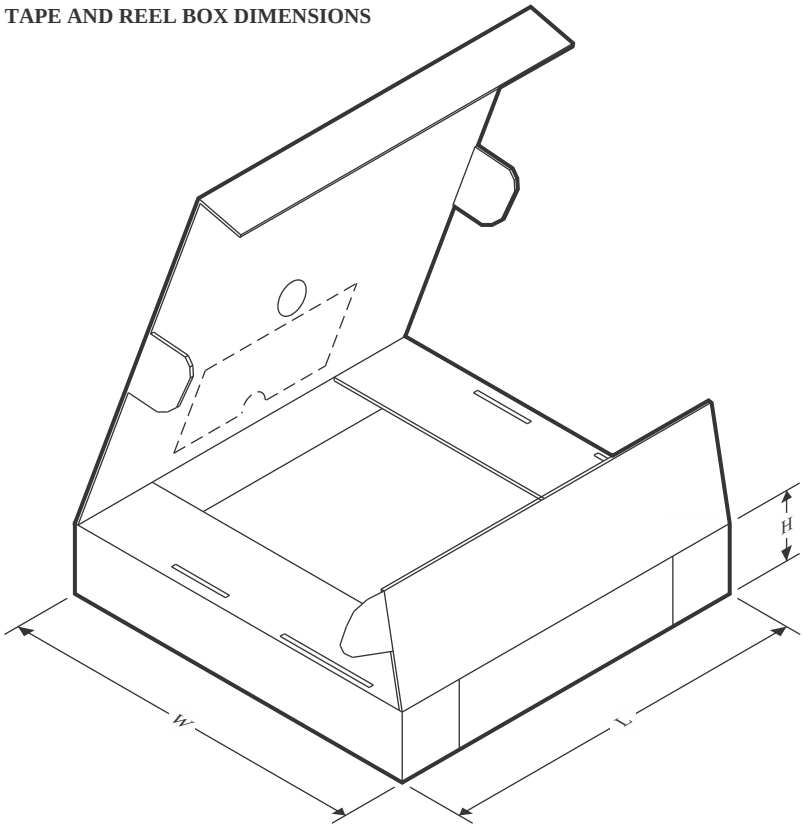
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR70503TM/NOPB	DSBGA	YFX	8	250	178.0	8.4	0.91	1.69	0.7	4.0	8.0	Q1
LMR70503TMX/NOPB	DSBGA	YFX	8	3000	178.0	8.4	0.91	1.69	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

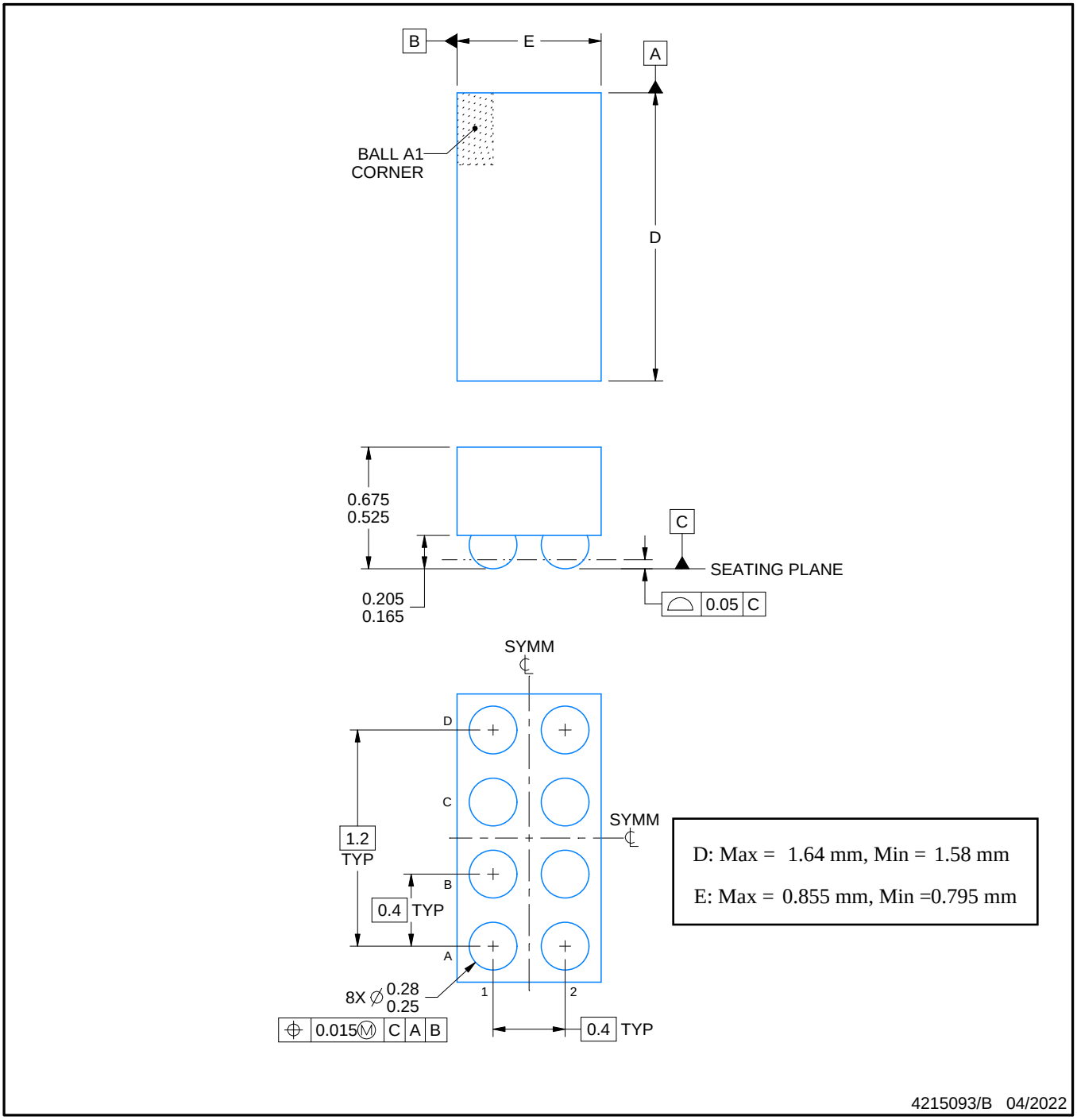
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR70503TM/NOPB	DSBGA	YFX	8	250	208.0	191.0	35.0
LMR70503TMX/NOPB	DSBGA	YFX	8	3000	208.0	191.0	35.0

PACKAGE OUTLINE

YFX0008

DSBGA - 0.675 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

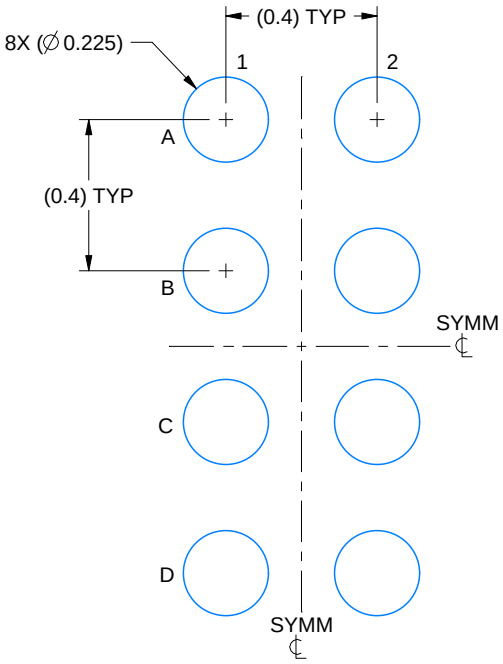
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

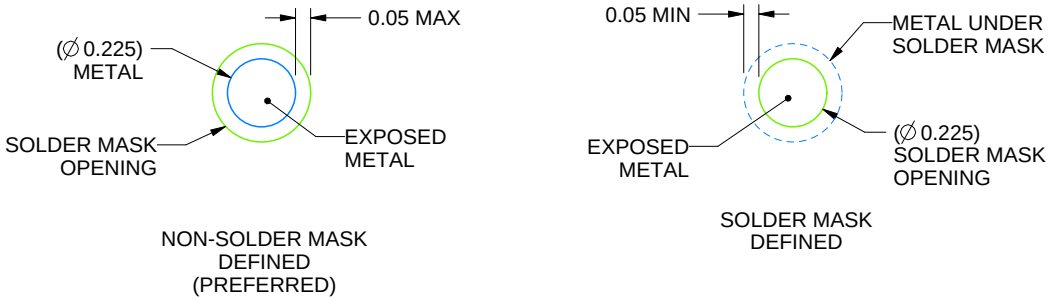
YFX0008

DSBGA - 0.675 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

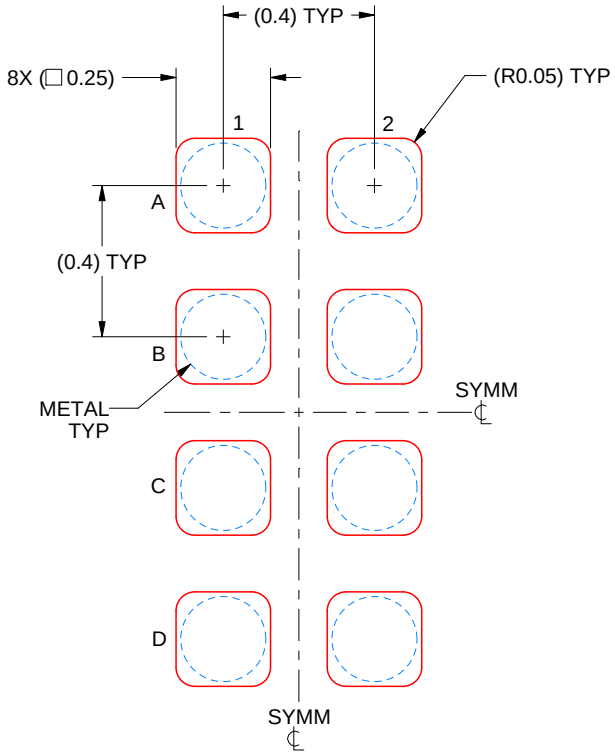


SOLDER MASK DETAILS
NOT TO SCALE

4215093/B 04/2022

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4215093/B 04/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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