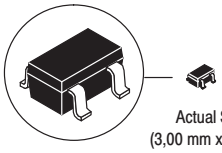


1.5K-BIT SERIAL EPROM WITH SDQ INTERFACE

Check for Samples: bq2024

FEATURES

- **1536 Bits of One-Time Programmable (OTP) EPROM For Storage Of User-Programmable Configuration Data**
- **Factory-Programmed Unique 64-Bit Identification Number**
- **Bus-Interface Architecture Allowing Multiple bq2024's Attached to a Single Host**
- **Single-Wire Interface to Reduce Circuit Board Routing**
- **Synchronous Communication Reduces Host Interrupt Overhead**
- **No Standby Power Required**
- **Address Space Backward Compatible With bq2022A**
- **8-byte RAM Buffer for Faster Write**
- **Page Address Redirection**
- **15KV IEC 61000-4-2 Air Charge on SDQ**
- **Available in a 3-Pin SOT23 Package and TO-92 Package**

APPLICATIONS

- **Security Encoding**
- **Inventory Tracking**
- **Product-Revision Maintenance**
- **Battery-Pack Identification**

DESCRIPTION

The bq2024 is a 1.5K-bit serial EPROM containing a factory-programmed, unique 48-bit identification number, 8-bit CRC generation, and the 8-bit family code (09h). A 64-bit status register controls write protection and page redirection.

The bq2024 SDQ™ interface requires only a single connection and a ground return. The DATA pin is also the sole power source for the bq2024. The bus architecture allows multiple SDQ devices to be connected to a single host.

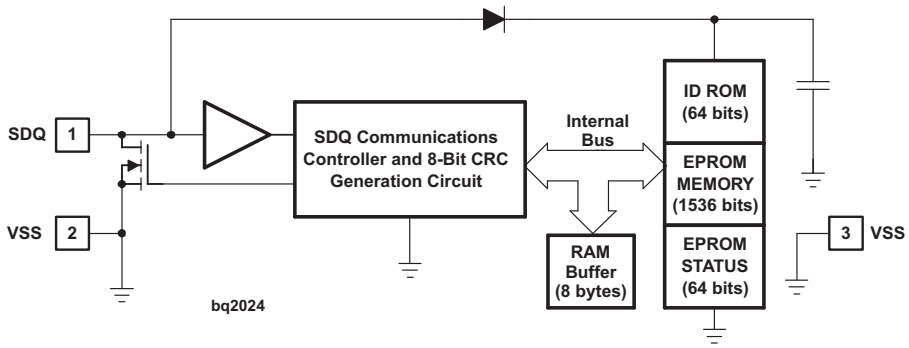
The small surface-mount package options saves printed-circuit-board space, while the low cost makes it ideal for applications such as battery pack configuration parameters, record maintenance, asset tracking, product-revision status, and access-code security.

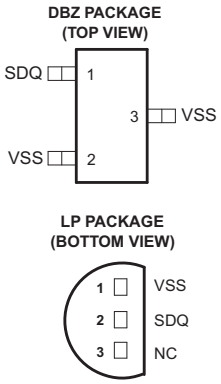
ORDERING INFORMATION(1)

T_A (2)	PACKAGED DEVICES(3)		
	PART NUMBER	PACKAGE	STATUS
–20°C to 70°C	bq2024DBZR	SOT23-3	Production
	bq2024LPR	TO-92	Preview

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Device specified to communicate at –40°C to 85°C.
(3) The device is available only in tape and reel with a base quantity of 3000 units for the bq2024DBZR and 2000 units for the bq2024LPR.

BLOCK DIAGRAM





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SDQ is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNIT
V_{PU}	DC voltage applied to data		–0.3 V to 7 V
I_{OL}	Low-level output current		40 mA
	ESD IEC 61000-4-2 Air discharge	Data to V_{SS}, V_{SS} to data	15 kV
T_A	Operating free-air temperature range		–20°C to 70°C
$T_{A(Comm)}$	Communication free-air temperature range	Communication is specified by design	–40°C to 85°C
T_{stg}	Storage temperature range		–55°C to 125°C
	Lead temperature (soldering, 10 s)		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = –20°C to 70°C; $V_{PU(min)}$ = 2.65 V_{DC} to 5.5 V_{DC}, all voltages relative to VSS

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{DATA}	Supply current	V_{PU} = 5.5 V			20	µA
V_{OL}	Low-level output voltage	Logic 0, V_{PU} = 5.5 V, I_{OL} = 4 mA, SDQ pin			0.4	V
		Logic 0, V_{PU} = 2.65 V, I_{OL} = 2 mA			0.4	
V_{OH}	High-level output voltage	Logic 1		V_{PU}	5.5	
I_{OL}	Low-level output current (sink)	V_{OL} = 0.4 V, SDQ pin			4	mA
V_{IL}	Low-level input voltage	Logic 0			0.8	V
V_{IH}	High-level input voltage	Logic 1	2.2			V
V_{PP}	Programming voltage		11.5		12	V

AC SWITCHING CHARACTERISTCS

T_A = –20°C to 70°C; $V_{PU(min)}$ = 2.65 V_{DC} to 5.5 V_{DC}, all voltages relative to VSS

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_c	Bit cycle time (1)		60		120	µs
t_{WSTRB}	Write start cycle (1)		1		15	µs
t_{WDSU}	Write data setup (1)		t_{WSTRB}		15	µs
t_{WDH}	Write data hold (1) (2)		60		t_c	µs
t_{rec}	Recovery time (1)		1			µs
		For memory command only	5			
t_{RSTRB}	Read start cycle (1)		1		13	µs
t_{ODD}	Output data delay (1)		t_{RSTRB}		13	µs
t_{ODHO}	Output data hold (1)		17		60	µs
t_{RST}	Reset time (1)		480			µs
t_{PPD}	Presence pulse delay (1)		15		60	µs
t_{PP}	Presence pulse (1)		60		240	µs
t_{EPROG}	EPROM programming time		2500			µs
t_{PSU}	Program setup time		5			µs

(1) 5-kΩ series resistor between SDQ pin and V_{PU}. (See Figure 1)
(2) t_{WDH} must be less than t_c to account for recovery.

AC SWITCHING CHARACTERISTCS (continued)

T_A = –20°C to 70°C; $V_{PU(min)}$ = 2.65 V_{DC} to 5.5 V_{DC}, all voltages relative to VSS

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PREC}	Program recovery time		5			µs
t_{PRE}	Program rising-edge time				5	µs
t_{PFE}	Program falling-edge time				5	µs
t_{RSTREC}			480			µs

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
bq2024DBZR			
SDQ	1	I	Data
VSS	2, 3	-	Ground
bq2024LPR, bq2024LPFR			
VSS	1	-	GND
SDQ	2	I	Data
NC	3	-	No connection

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The block diagram on page 1 shows the relationships among the major control and memory sections of the bq2024. The bq2024 has three main data components: a 1536-bit factory-programmed ROM, including 8-bit family code, 48-bit identification number and 8-bit CRC value, EPROM, and EPROM STATUS bytes. Power for read and write operations is derived from the DATA pin. An internal capacitor stores energy while the signal line is high and releases energy during the low times of the DATA pin, until the pin returns high to replenish the charge on the capacitor. A special manufacturer's PROGRAM PROFILE BYTE can be read to determine the programming profile required to program the part.

1536-BIT EPROM

Table 1 is a memory map of the 1536-bit EPROM section of the bq2024, configured as six pages of 32 bytes each. The 8-byte RAM buffers are additional registers used when programming the memory. Data are first written to the RAM buffer and then verified by reading an 8-bit CRC from the bq2024 that confirms proper receipt of the data. If the buffer contents are correct, a programming command is issued and an 8-byte segment of data is written into the selected address in memory. This process ensures data integrity when programming the memory. The details for reading and programming the 1536-bit EPROM portion of the bq2024 are in the *Memory Function Commands* section of this data sheet.

Table 1. 1536-BIT EPROM Data Memory Map

ADDRESS(HEX)	PAGE
00A0-00BF	Page 5
0080-009F	Page 4
0060-007F	Page 3
0040-005F	Page 2
0020-003F	Page 1
0000-001F	Page 0

EPROM STATUS MEMORY

In addition to the programmable 1536 bits of memory, there are 64 bits of status information contained in the EPROM STATUS memory. The STATUS memory is accessible with separate commands. The STATUS bits are EPROM and are read or programmed to indicate various conditions to the software interrogating the bq2024. The first byte of the STATUS memory contains the write protect page bits, that inhibit programming of the corresponding page in the 1536-bit main memory area if the appropriate write-protection bit is programmed. Once a bit has been programmed in the write protect page byte, the entire 32-byte page that corresponds to that bit can no longer be altered but may still be read. The write protect bits may be cleared by using the WRITE STATUS command.

The next six bytes of the EPROM STATUS memory contain the page address redirection bytes. Bits in the EPROM status bytes can indicate to the host what page is substituted for the page by the appropriate redirection byte. The hardware of the bq2024 makes no decisions based on the contents of the page address redirection bytes. This feature allows the user's software to make a data patch to the EPROM by indicating that a particular page or pages should be replaced with those indicated in the page address redirection bytes. The ones complement of the new page address is written into the page address redirection byte that corresponds to the original (replaced) page. If a page address redirection byte has an FFh value, the data in the main memory that corresponds to that page are valid. If a page address redirection byte has some other hex value, the data in the page corresponding to that redirection byte are invalid, and the valid data can now be found at the ones complement of the page address indicated by the hexadecimal value stored in the associated page address redirection byte. A value of FDh in the redirection byte for page 1, for example, indicates that the updated data are now in page 2. The details for reading and programming the EPROM status memory portion of the bq2024 are given in the *Memory Function Commands* section.

Table 2. EPROM Status Bytes

ADDRESS (HEX)	PAGE
00h	Write protection bits BIT0 - write protect page 0 BIT1 - write protect page 1 BIT2 - write protect page 2 BIT3 - write protect page 3 BIT4 -write protect page 4 BIT5 -write protect page 5 BIT6 to 7 -bitmap of used pages
01h	Redirection byte for page 0
02h	Redirection byte for page 1
03h	Redirection byte for page 2
04h	Redirection byte for page 3
05h	Redirection byte for page 4
06h	Redirection byte for page 5
07h	Factory programmed 00h

Error Checking

To validate the data transmitted from the bq2024, the host generates a CRC value from the data as they are received. This generated value is compared to the CRC value transmitted by the bq2024. If the two CRC values match, the transmission is error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. Details are found in the *CRC Generation Section* of this data sheet.

Customizing the bq2024

The 64-bit ID identifies each bq2024. The 48-bit serial number is unique and programmed by Texas Instruments. The default 8-bit family code is 09h; however, a different value can be reserved on an individual customer basis. Contact your Texas Instruments sales representative for more information.

Bus Termination

Because the drive output of the bq2024 is an open-drain, N-channel MOSFET, the host must provide a source current or a 5-kΩ external pullup, as shown in the typical application circuit in Figure 1.

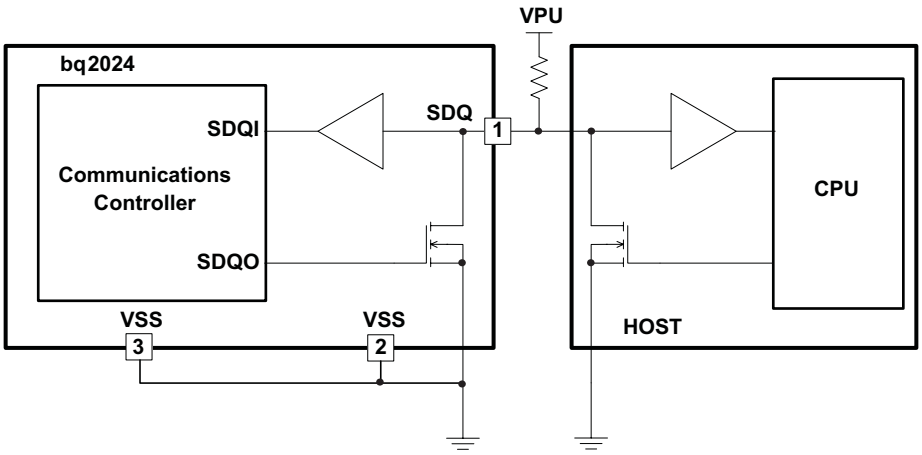


Figure 1. Typical Applications Circuit

Serial Communication

A host reads, programs, or checks the status of the bq2024 through the hierarchical command structure of the SDQ interface. Figure 2 shows that the host must first issue a ROM command before the EPROM memory or status can be read or modified. The ROM command either selects a specific device when multiple devices are on the SDQ bus, or skips the selection process in single SDQ device applications.

Initialization	ROM Command Sequence	Memory/Status Command Sequence

Figure 2. General Command Sequence

Initialization

Initialization consists of two pulses, the RESET and the PRESENCE pulses. The host generates the RESET pulse, while the bq2024 responds with the PRESENCE pulse. The host resets the bq2024 by driving the DATA bus low for at least 480 µs. For more details, see the *RESET* section under *SDQ Signaling*.

ROM COMMANDS

READ ROM

The READ ROM command sequence is the fastest sequence that allows the host to read the 8-bit family code and 48-bit identification number. It is used if only one SDQ slave device is attached to the bus. The READ ROM sequence starts with the host generating the RESET pulse of at least 480 µs. The bq2024 responds with a PRESENCE pulse. Next, the host continues by issuing the READ ROM command, 33h, and then reads the ROM and CRC byte using the READ signaling (see the READ and WRITE signals section) during the data frame.

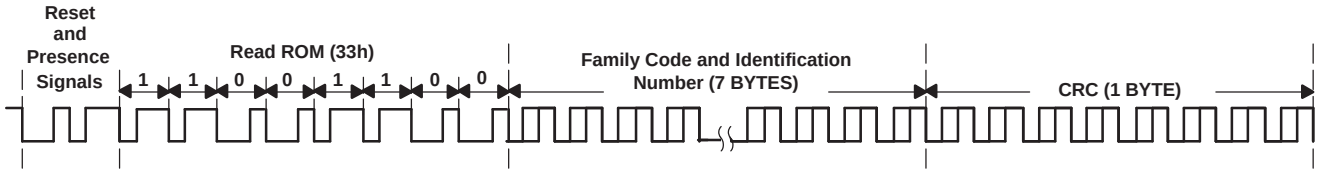


Figure 3. READ ROM Sequence

MATCH ROM

The MATCH ROM command, 55h, is used by the host to select a specific SDQ device when the family code and identification number is known. The host issues the MATCH ROM command followed by the family code, ROM number, and the CRC byte. Only the device that matches the 64-bit ROM sequence is selected and available to perform subsequent Memory/Status Function commands.

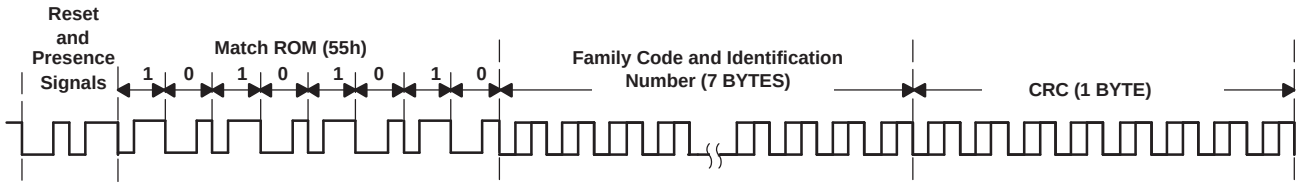


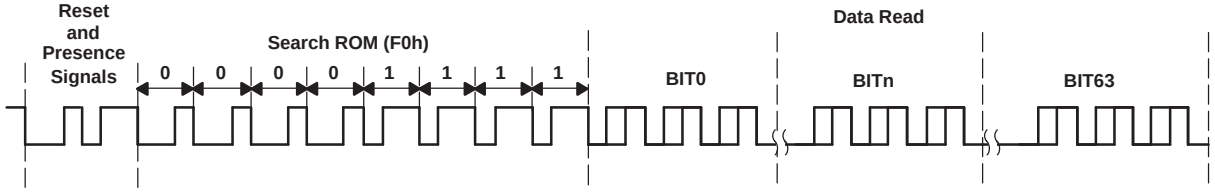
Figure 4. MATCH ROM Sequence

SEARCH ROM

The SEARCH ROM command, F0h, is used to obtain the 8-bit family code and the 48-bit identification number and 8-bit CRC of any SDQ device when it is unknown. All devices on the bus are read under the SEARCH ROM command with the use of a collision-detect and device-decode method. Figure 5 shows the SEARCH ROM sequence started by the host, generating the RESET pulse of at least 480 µs. The bq2024 responds with a PRESENCE pulse. The host then issues the command in the command frame by writing an F0h. During the DATA READ of the SEARCH ROM sequence, each bit is transmitted three times. The bq2024 transmits the bit followed by the complement of the bit. The host in turn retransmits the bit just read. Collision detection is performed by comparing the bit and bit complement time-slots. If they are both zero, this indicates that a collision has occurred, indicating multiple devices on the bus. The device decode is achieved in the third transmission of the bit from the host back to the bq2024. If the bit transmitted by the host does not match the bit transmitted by the bq2024, then the device with mismatch stops transmitting. Devices that did match, continue transmitting. This process is continued until all bits of a single device are read. The SEARCH ROM command is reissued and the process is repeated to read additional devices.

NOTE

If the number of devices on the bus is unknown, the SEARCH ROM command should be used.



A. ***B = bit(*** *n*): *n*th bit transmitted by bq2024

B. ***C =*** $\overline{\textbf{\textit{bit(n)}}}$: complement of *n*th bit transmitted by bq2024

C. ***H = bit(*** *n*): *n*th bit transmitted by host

Figure 5. SEARCH ROM Sequence

SKIP ROM

This SKIP ROM command, CCh, allows the host to access the memory/status functions without issuing the 64-bit ROM code sequence. The SKIP ROM command is directly followed by a memory/status functions command. Because this command can cause bus collisions when multiple SDQ devices are on the same bus, this command should be issued in single device applications.

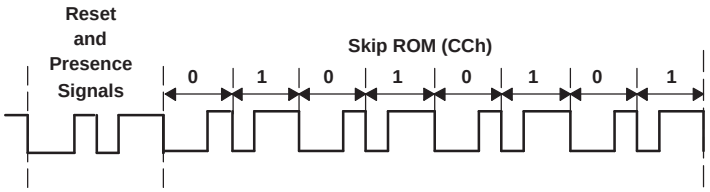


Figure 6. SKIP ROM Sequence

MEMORY/STATUS FUNCTION COMMANDS

Six memory/status function commands allow read and modification of the 1536-bit EPROM data memory or the 64-bit EPROM status memory. There are two types of READ MEMORY command, plus the WRITE MEMORY, READ STATUS, and WRITE STATUS commands. Additionally, the part responds to a PROGRAM PROFILE byte command. The bq2024 responds to memory/status function commands only after a part is selected by a ROM command.

READ DATA MEMORY COMMANDS

Two READ MEMORY commands are available on the bq2024. Both commands are used to read data from the 1536-bit EPROM data field. They are the READ MEMORY/Page CRC and the READ MEMORY/Field CRC commands. The READ MEMORY/Page CRC generates CRC at the end any 32-byte page boundary whereas the READ MEMORY/Field CRC generates CRC when the end of the 1536-bit data memory is reached.

READ MEMORY/Page CRC

To read memory and generate the CRC at the 32-byte page boundaries of the bq2024, the ROM command is followed by the READ MEMORY/Generate CRC command, C3h, followed by the address low byte and then the address high byte.

An 8-bit CRC of the command byte and address bytes is computed by the bq2024 and read back by the host to confirm that the correct command word and starting address were received. If the CRC read by the host is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the host is correct, the host issues read time slots and receives data from the bq2024 starting at the initial address and continuing until the end of a 32-byte page is reached. At that point, the host sends eight additional read time slots and receive an 8-bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page. Once the 8-bit CRC has been received, data is again read from the 1536-bit EPROM data field starting at the next page. This sequence continues until the final page and its accompanying CRC are read by the host. Thus each page of data can be considered to be 33 bytes long, the 32 bytes of user-programmed EPROM data and an 8-bit CRC that gets generated automatically at the end of each page.

Initialization and ROM Command Sequence	READ MEMORY/Generate CRC Command	Address Low Byte		Address High Byte		Read and Verify CRC	EPROM Memory and CRC Byte Generated at 32-Byte Page Boundaries
	C3h	A0	A7	A8	A15		

NOTE: Individual bytes of address and data are transmitted LSB first.

Figure 7. READ MEMORY/Page CRC

READ MEMORY/Field CRC

To read memory without CRC generation on 32-byte page boundaries, the ROM command is followed by the READ MEMORY command, F0h, followed by the address low byte and then the address high byte.

NOTE

As shown in Figure 8, individual bytes of address and data are transmitted LSB first.

An 8-bit CRC of the command byte and address bytes is computed by the bq2024 and read back by the host to confirm that the correct command word and starting address were received. If the CRC read by the host is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the host is correct, the host issues read time slots and receives data from the bq2024 starting at the initial address and continuing until the end of the 1536-bit data field is reached or until a reset pulse is issued. If reading occurs through the end of memory space, the host may issue eight additional read time slots and the bq2024 responds with an 8-bit CRC of all data bytes read from the initial starting byte through the last byte of memory. After the CRC is received by the host, any subsequent read time slots appear as logical 1s until a reset pulse is issued. Any reads ended by a reset pulse prior to reaching the end of memory does not have the 8-bit CRC available.

Initialization and ROM Command Sequence	READ MEMORY Command F0h	Address Low Byte A0 A7	Address High Byte A8 A15	Read and Verify CRC	Read EPROM Memory Until End of EPROM Memory	Read and Verify CRC

Figure 8. READ MEMORY/Field CRC

WRITE MEMORY

The WRITE MEMORY command is used to program the 1536-bit EPROM memory field. The 1536-bit memory field is programmed in 8-byte segments. Data is first written into an 8-byte RAM buffer one byte at a time. The contents of the RAM buffer is then ANDed with the contents of the EPROM memory field when the programming command is issued.

Figure 9 illustrates the sequence of events for programming the EPROM memory field. After issuing a ROM command, the host issues the WRITE MEMORY command, 0Fh, followed by the low byte and then the high byte of the starting address. The bq2024 calculates and transmits an 8-bit CRC based on the WRITE command and address.

If at any time during the WRITE MEMORY process, the CRC read by the host is incorrect, a reset pulse must be issued, and the entire sequence must be repeated.

After the bq2024 transmits the CRC, the host then transmits 8 bytes of data to the bq2024. Another 8-bit CRC is calculated and transmitted based on the 8 bytes of data. If this CRC agrees with the CRC calculated by the host, the host transmits the program command 5Ah and then applies the programming voltage for at least 2500 µs or t_{EPROG}. The contents of the RAM buffer is then logically ANDed with the contents of the 8-byte EPROM offset by the starting address.

The starting address can be any integer multiple of eight between 0000 and 00BF (hex) such as 0000, 0008, and 0010 (hex).

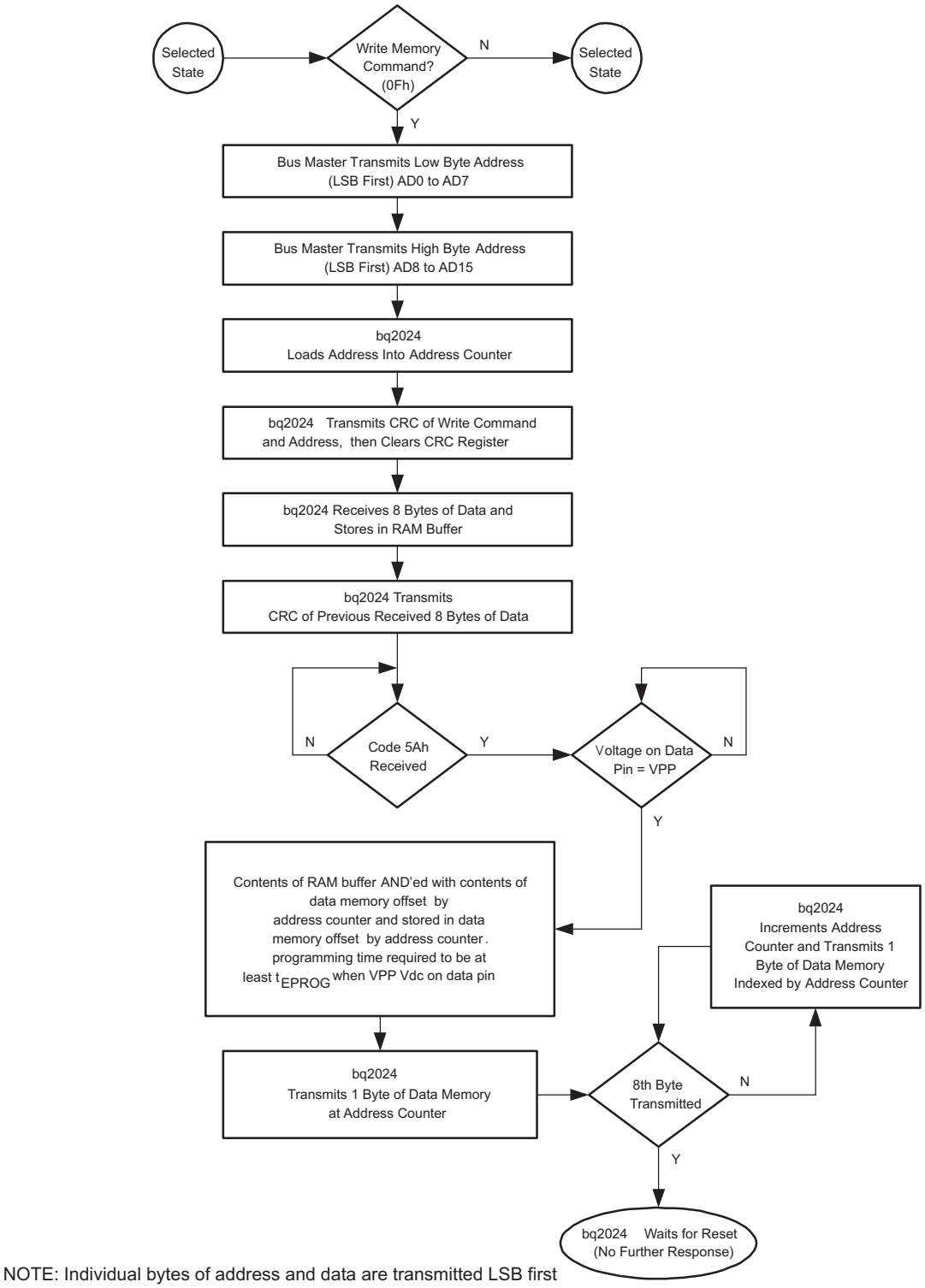
The WRITE DATA MEMORY command sequence can be terminated at any point by issuing a reset pulse except during the program pulse period t_{PROG}.

NOTE

The bq2024 responds with the data from the selected EPROM address sent least significant-bit first. This response should be checked to verify the programmed byte. If the programmed byte is incorrect, then the host must reset the part and begin the write sequence again.

For both of these cases, the decision to continue programming is made entirely by the host, because the bq2024 is not able to determine if the 8-bit CRC calculated by the host agrees with the 8-bit CRC calculated by the bq2024.

Prior to programming, bits in the 1536-bit EPROM data field appear as logical 1s.



NOTE: Individual bytes of address and data are transmitted LSB first

Figure 9. WRITE MEMORY Command Flow

READ STATUS

The READ STATUS command is used to read data from the EPROM status data field. After issuing a ROM command, the host issues the READ STATUS command, AAh, followed by the address low byte and then the address high byte.

NOTE

An 8-bit CRC of the command byte and address bytes is computed by the bq2024 and read back by the host to confirm that the correct command word and starting address were received.

If the CRC read by the host is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the host is correct, the host issues read time slots and receives data from the bq2024 starting at the supplied address and continuing until the end of the EPROM Status data field is reached. At that point, the host receives an 8-bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte through the final factory-programmed byte that contains the 00h value.

This feature is provided because the EPROM status information may change over time making it impossible to program the data once and include an accompanying CRC that is always valid. Therefore, the READ status command supplies an 8-bit CRC that is based on (and always is consistent with) the current data stored in the EPROM status data field.

After the 8-bit CRC is read, the host receives logical 1s from the bq2024 until a reset pulse is issued. The READ STATUS command sequence can be ended at any point by issuing a reset pulse.

Initialization and ROM Command Sequence	READ MEMORY Command AAh	Address Low Byte A0 A7	Address High Byte A8 A15	Read and Verify CRC	Read STATUS Memory Until End of STATUS Memory	Read and Verify CRC

Figure 10. READ STATUS Command

WRITE STATUS

The Write Status command is used to program the EPROM Status data field after the bq2024 has been selected by a ROM command

The flow chart in Figure 11 illustrates that the host issues the Write Status command, 55h, followed by the address low byte and then the address high byte the followed by the byte of data to be programmed.

NOTE

Individual bytes of address and data are transmitted LSB first. An 8-bit CRC of the command byte, address bytes, and data byte is computed by the bq2024 and read back by the host to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the host is incorrect, a reset pulse must be issued and the entire sequence must be repeated. If the CRC received by the host is correct, the program command (5Ah) is issued. After the program command is issued, then the programming voltage, V_{PP} is applied to the DATA pin for period t_{PROG}. Prior to programming, the first seven bytes of the EPROM STATUS data field appear as logical 1s. For each bit in the data byte provided by the host that is set to a logical 0, the corresponding bit in the selected byte of the EPROM STATUS data field is programmed to a logical 0 after the programming pulse has been applied at the byte location. The eighth byte of the EPROM STATUS byte data field is factory-programmed to contain 00h.

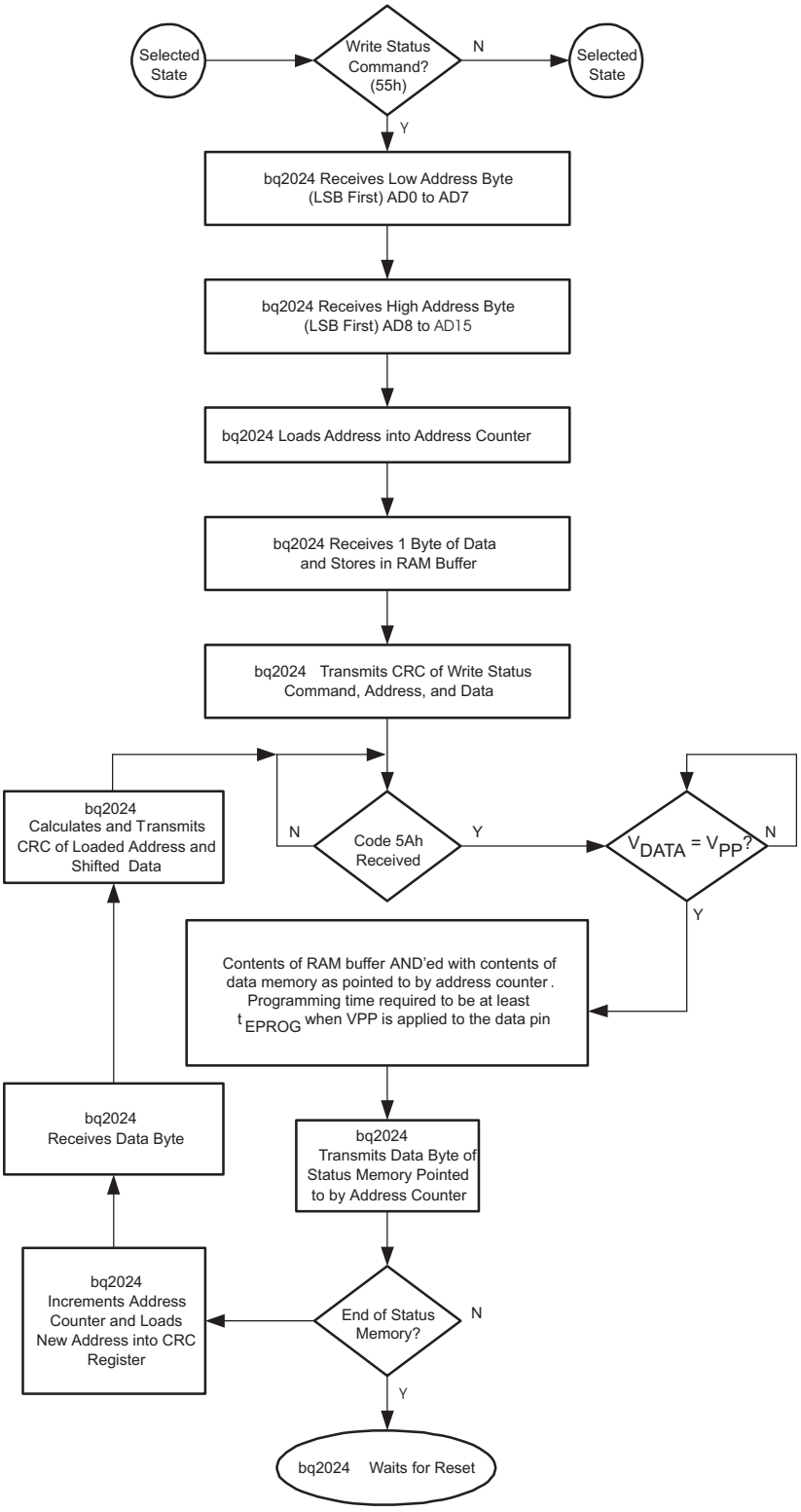


Figure 11. WRITE STATUS Command Flow

After the programming pulse is applied and the data line returns to V_{PU}, the host issues eight read time slots to verify that the appropriate bits have been programmed. The bq2024 responds with the data from the selected EPROM STATUS address sent least significant bit first. This response should be checked to verify the programmed byte. If the programmed byte is incorrect, then the host must reset the device and begin the write sequence again. If the bq2024 EPROM data byte programming was successful, the bq2024 automatically increments its address counter to select the next byte in the STATUS MEMORY data field. The least significant byte of the new two-byte address is also loaded into the 8-bit CRC generator as a starting value. The host issues the next byte of data using eight write time slots.

As the bq2024 receives this byte of data into the RAM buffer, it also shifts the data into the CRC generator that has been preloaded with the LSB of the current address and the result is an 8-bit CRC of the new data byte and the LSB of the new address. After supplying the data byte, the host reads this 8-bit CRC from the bq2024 with eight read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the Write Status command sequence must be restarted. If the CRC is correct, the host issues a programming pulse and the selected byte in memory is programmed.

NOTE

The initial write of the WRITE STATUS command, generates an 8-bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two-address bytes, and finally the data byte. Subsequent writes within this WRITE STATUS command due to the bq2024 automatically incrementing its address counter generates an 8-bit CRC that is the result of loading (not shifting) the LSB of the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue programming the EPROM Status registers is made entirely by the host, because the bq2024 is not able to determine if the 8-bit CRC calculated by the host agrees with the 8-bit CRC calculated by the bq2024. If an incorrect CRC is ignored and a program pulse is applied by the host, incorrect programming could occur within the bq2024. Also note that the bq2024 always increments its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the host, therefore if the EPROM data byte does not match the supplied data byte but the master continues with the WRITE STATUS command, incorrect programming could occur within the bq2024. The WRITE STATUS command sequence can be ended at any point by issuing a reset pulse.

Table 3. Command Code Summary

COMMAND (HEX)	DESCRIPTION	CATEGORY
33h	Read Serialization ROM and CRC	ROM Commands Available in Command Level I
55h	Match Serialization ROM	
F0h	Search Serialization ROM	
CCh	Skip Serialization ROM	
F0h	Read Memory/Field CRC	Memory Function Commands Available in Command Level II
AAh	Read EPROM Status	
C3h	Read Memory/Page CRC	
0Fh	Write Memory	
99h	Programming Profile	
55h	Write EPROM Status	
5Ah	Program Control	Program Command Available Only in WRITE MEMORY and WRITE STATUS Modes

PROGRAM PROFILE BYTE

The PROGRAM PROFILE byte is read to determine the WRITE MEMORY programming sequence required by a specific manufacturer. After issuing a ROM command, the host issues the PROGRAM PROFILE BYTE command, 99h. Figure 12 shows the the bq2024 responds with 55h. This informs the host that the WRITE MEMORY programming sequence is the one described in the WRITE MEMORY command section of this data sheet.

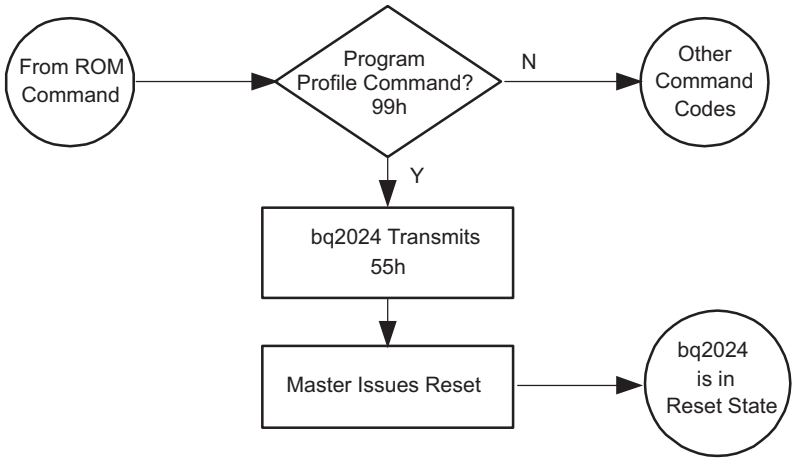


Figure 12. PROGRAM PROFILE Command Flow

SDQ SIGNALING

All SDQ signaling begins with initializing the device, followed by the host driving the bus low to write a 1 or 0, or to begin the start frame for a bit read. Figure 13 shows the initialization timing, whereas Figure 14 and Figure 15 show that the host initiates each bit by driving the DATA bus low for the start period, t_{WSTRB} / t_{RSTRB}. After the bit is initiated, either the host continues controlling the bus during a WRITE, or the bq2024 responds during a READ.

RESET AND PRESENCE PULSE

If the DATA bus is driven low for more than 120 µs, the bq2024 may be reset. Figure 13 shows that if the DATA bus is driven low for more than 480 µs, the bq2024 resets and indicates that it is ready by responding with a PRESENCE PULSE.

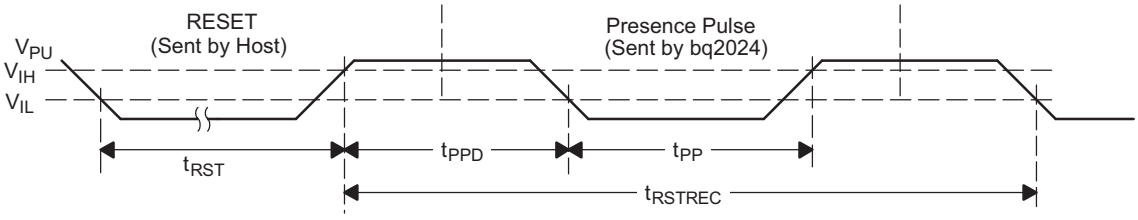


Figure 13. Reset Timing Diagram

WRITE

The WRITE bit timing diagram in Figure 14 shows that the host initiates the transmission by issuing the t_{WSTRB} portion of the bit and then either driving the DATA bus low for a WRITE 0, or releasing the DATA bus for a WRITE 1.

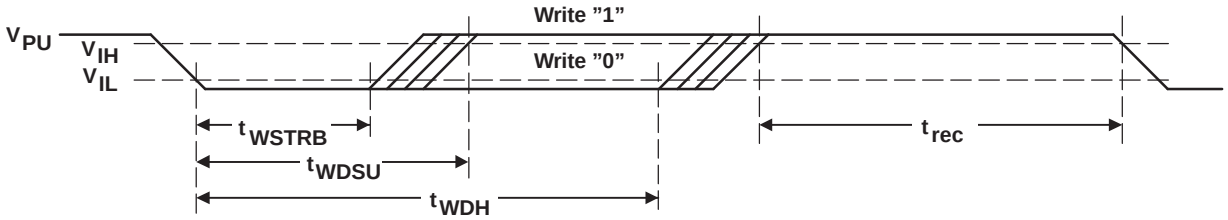


Figure 14. Write Bit Timing Diagram

READ

The READ bit timing diagram in Figure 15 shows that the host initiates the transmission of the bit by issuing the t_{RSTRB} portion of the bit. The bq2024 then responds by either driving the DATA bus low to transmit a READ 0 or releasing the DATA bus to transmit a READ 1.

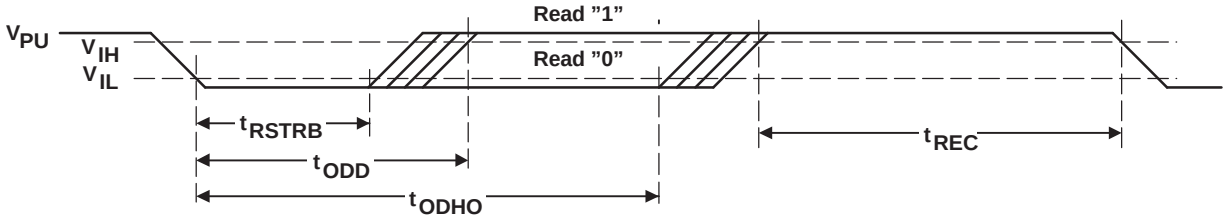


Figure 15. Read Bit Timing Diagram

PROGRAM PULSE

Figure 16. Program Pulse Timing Diagram

IDLE

If the bus is high, the bus is in the IDLE state. Bus transactions can be suspended by leaving the DATA bus in IDLE. Bus transactions can resume at any time from the IDLE state.

CRC Generation

The bq2024 has an 8-bit CRC stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the bq2024 to determine if the ROM data has been received error-free by the bus master. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$.

Under certain conditions, the bq2024 also generates an 8-bit CRC value using the same polynomial function just shown and provides this value to the bus master to validate the transfer of command, address, and data bytes from the bus master to the bq2024. The bq2024 computes an 8-bit CRC for the command, address, and data bytes received for the WRITE MEMORY and the WRITE STATUS commands and then outputs this value to the bus master to confirm proper transfer. Similarly, the bq2024 computes an 8-bit CRC for the command and address bytes received from the bus master for the READ MEMORY, READ STATUS, and READ DATA/ GENERATE 8-BIT CRC commands to confirm that these bytes have been received correctly. The CRC generator on the bq2024 is also used to provide verification of error-free data transfer as each page of data from the 1536-bit EPROM is sent to the bus master during a READ DATA/GENERATE 8-BIT CRC command, and for the eight bytes of information in the status memory field.

In each case where a CRC is used for data transfer validation, the bus master must calculate a CRC value using the polynomial function previously given and compare the calculated value to either the 8-bit CRC value stored in the 64-bit ROM portion of the bq2024 (for ROM reads) or the 8-bit CRC value computed within the bq2024. The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. No circuitry on the bq2024 prevents a command sequence from proceeding if the CRC stored in or calculated by the bq2024 does not match the value generated by the bus master. Proper use of the CRC can result in a communication channel with a high level of integrity.

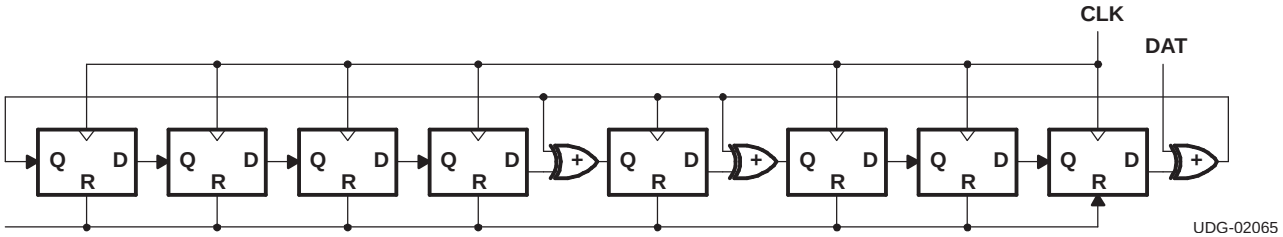


Figure 17. 8-Bit CRC Generator Circuit ($X^8 + X^5 + X^4 + 1$)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2024DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 70	CCAI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

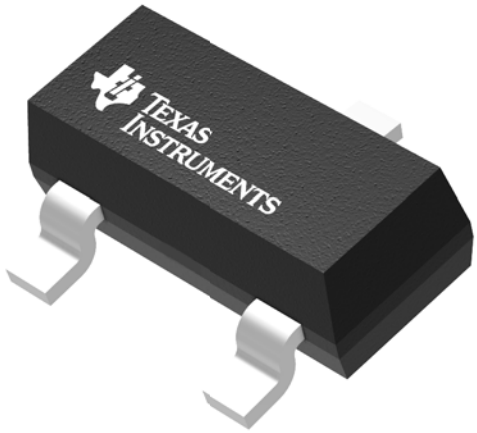
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



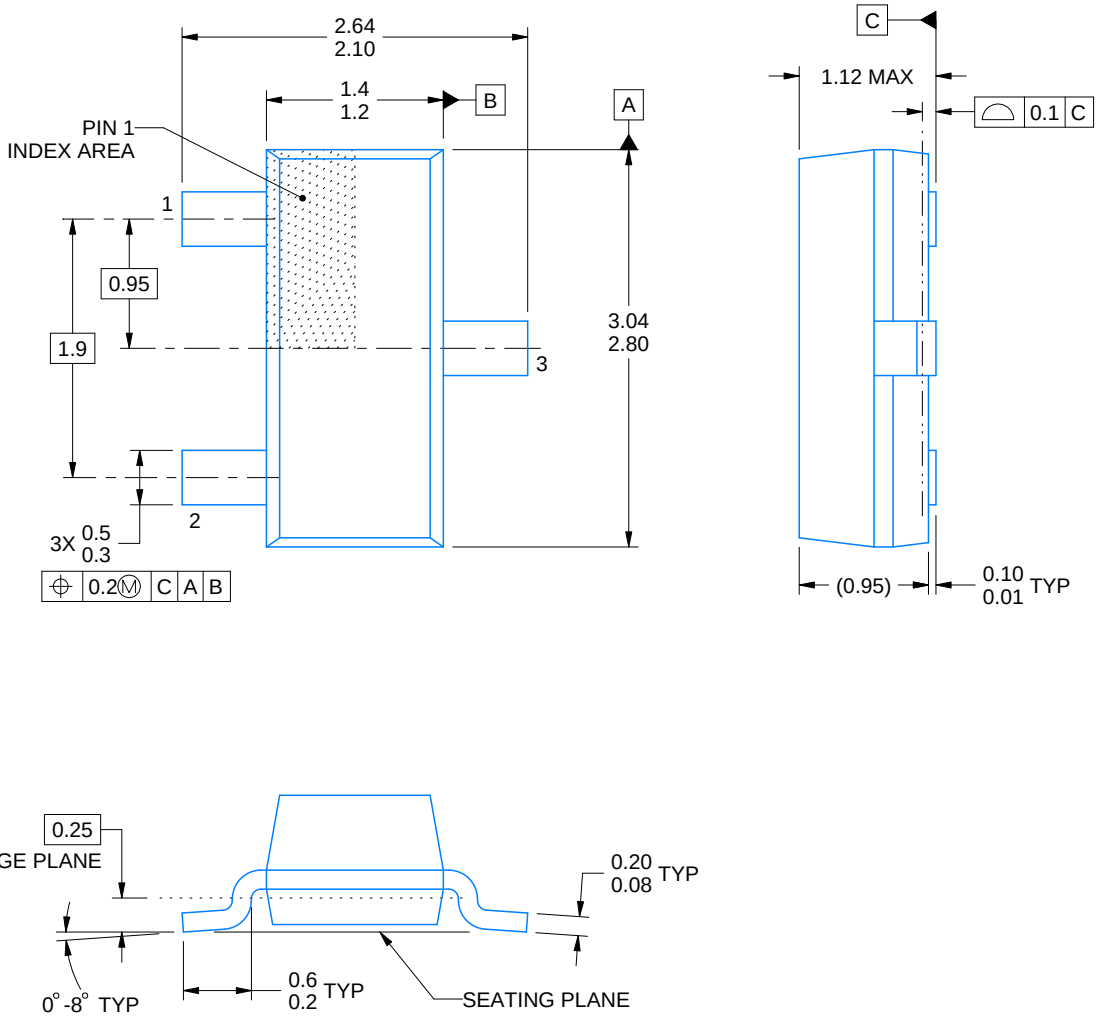
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

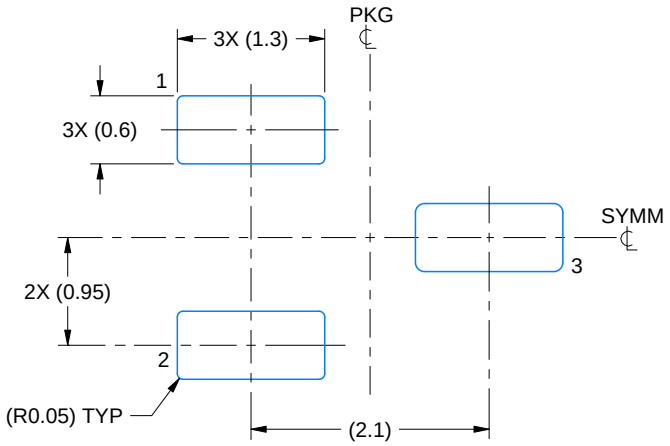
SMALL OUTLINE TRANSISTOR



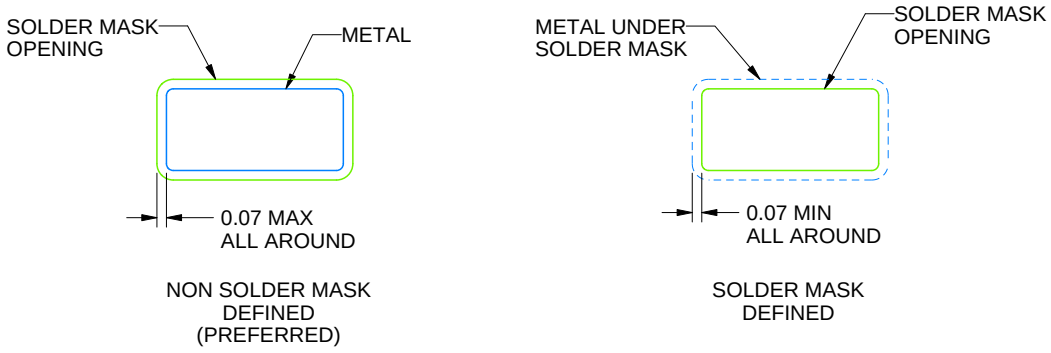
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X

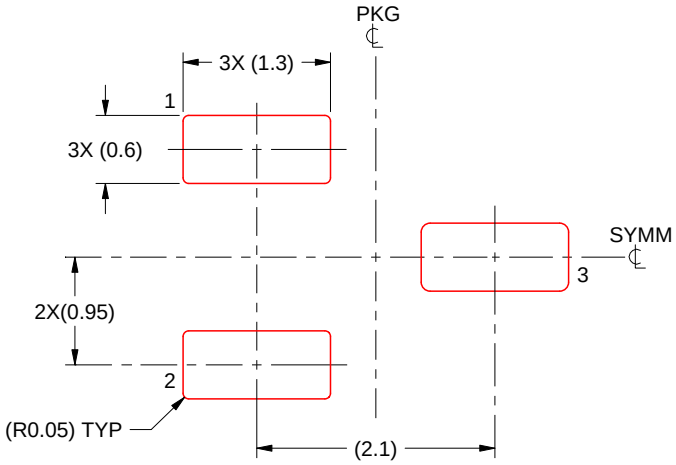


SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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