采用 SOT563 封装并具有强制 PWM 的 TLV6256xA 1A、2A 降压转换器

1 特性

- 强制 PWM 模式可减少输出电压纹波
- 效率高达 95%
- 低 $R_{DS(ON)}$ 开关：100mΩ/60mΩ
- 输入电压范围为 2.5V 至 5.5V
- 可调输出电压范围为 0.6V 至 V_{IN}
- 100% 占空比，可实现超低压降
- 1.5MHz 典型开关频率
- 电源正常输出
- 过流保护
- 内部软启动
- 热关断保护
- 采用 SOT563 封装
- 与 TLV62568、TLV62569 引脚对引脚兼容
- 借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 通用负载点 (POL) 电源
- STB 和 DVR
- IP 网络摄像头
- 无线路由器
- 固态硬盘 (SSD) – 企业级

3 说明

TLV62568A、TLV62569A 器件是经过优化而具有高效率和紧凑型解决方案尺寸的同步降压型直流/直流转换器。该器件集成了输出电流高达 2A 的开关。在整个负载范围内，该器件将以 1.5MHz 开关频率在脉宽调制 (PWM) 模式下运行。关断时，流耗减少至 2μA 以下。

内部软启动电路可限制启动期间的浪涌电流。此外，还内置了 诸如输出过流保护、热关断保护和电源正常输出等其他特性。该器件采用 SOT563 封装。

器件信息(1)

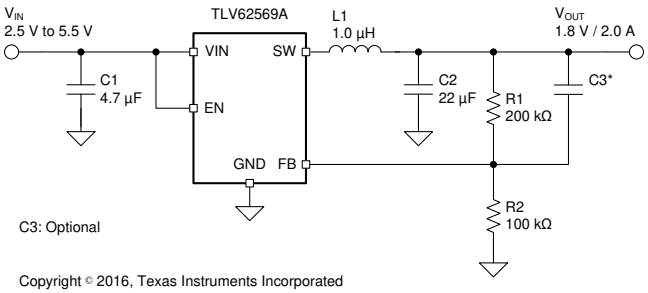
器件型号	封装	封装尺寸（标称值）
TLV62568ADRL	SOT563 (6)	1.60mm x 1.60mm
TLV62568APDRL		
TLV62569ADRL		
TLV62569APDRL		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

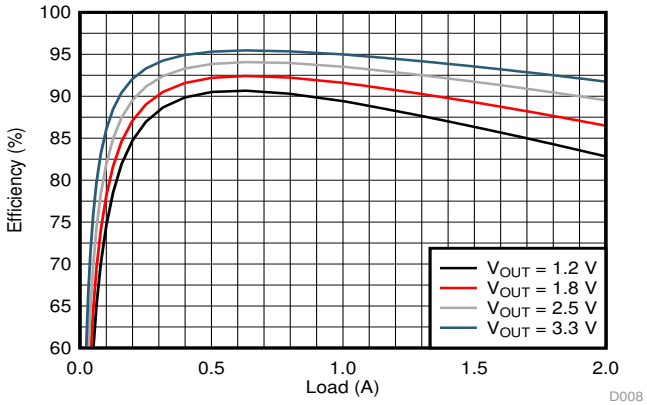
器件比较

器件型号	输出电流	功能
TLV62568ADRL	1A	-
TLV62568APDRL		电源正常
TLV62569ADRL	2A	-
TLV62569APDRL		电源正常

典型应用原理图



在 5V 输入电压下的效率



目录

4 修订历史记录

Changes from Revision A (May 2018) to Revision B **Page**

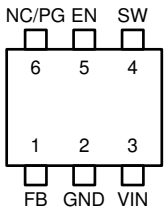
- 已更改 Power Good pin sink current capability from 1 mA to 2 mA ... 7

Changes from Original (April 2018) to Revision A **Page**

- 已更改 将状态从“预告信息”更改为“生产数据” ... 1

5 Pin Configuration and Functions

SOT563-6
DRL Package
(Top View)



Pin Functions

NAME	SOT563-6 PIN NUMBER	I/O/PWR	DESCRIPTION
FB	1	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
GND	2	PWR	Ground pin.
VIN	3	PWR	Power supply voltage input.
SW	4	PWR	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
EN	5	I	Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating.
PG	6	O	Power good open drain output pin for TLV62569APDRL. The pull-up resistor should not be connected to any voltage higher than 5.5V. If it's not used, leave the pin floating.
NC	6	-	No connection pin for TLV62569ADRL. The pin can be connected to the output or the ground for enhancing thermal performance. Or leave it floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, PG	-0.3	6	V
	SW (DC)	-0.3	V_{IN} + 0.3	
	SW (AC, less than 10ns)(3)	-3.0	9	
	FB	-0.3	3	
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		5.5	V
V_{OUT}	Output voltage	0.6		V_{IN}	V
I_{OUT}	Output current	0		2	A
T_J	Junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TLV62568Ax, TLV62569Ax		UNIT
		JEDEC (DRL)	EVM (DRL)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	142.8	124.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.1	n/a (2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.9	n/a (2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	28.7	23.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Not applicable to an EVM.

6.5 Electrical Characteristics

V_{IN} = 5.0 V, T_J = 25 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{SD}	Shutdown current into VIN pin	EN = 0 V		0.01	2	µA
V_{UVLO}	Under voltage lock out	V_{IN} falling		2.3	2.45	V
	under voltage lock out hysteresis			100		mV
T_{JSD}	Thermal shutdown	T_J rising		150		°C
		T_J falling		130		
LOGIC INTERFACE						
V_{IH}	High-level input voltage at EN pin	2.5 ≤ V_{IN} ≤ 5.5	1.2			V
V_{IL}	Low-level input voltage at EN pin	2.5 ≤ V_{IN} ≤ 5.5			0.4	V
t_{SS}	Soft startup time	From EN high to 95% of VOUT nominal		0.9		ms
V_{PG}	Power good threshold	V_{FB} rising, referenced to V_{FB} nominal		95%		
		V_{FB} falling, referenced to V_{FB} nominal		90%		
$V_{PG,OL}$	Low-level output voltage at PG pin	I_{SINK} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5 V		100		nA
$t_{PG,DLY}$	Power good delay time	V_{FB} falling		40		µs

Electrical Characteristics (continued)

V_{IN} = 5.0 V, T_J = 25 °C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{FB}	Feedback regulation voltage		0.588	0.6	0.612	V
I_{FB}	Input leakage current into FB pin	V_{FB} = 0.6 V		10		nA
$R_{DS(on)}$	High-side FET on resistance			100		mΩ
	Low-side FET on resistance			60		
I_{LIM}	High-side FET current limit	TLV62569A, TLV62569AP	3			A
		TLV62568A, TLV62568AP	2			
f_{SW}	Switching frequency			1.5		MHz

6.6 Typical Characteristics

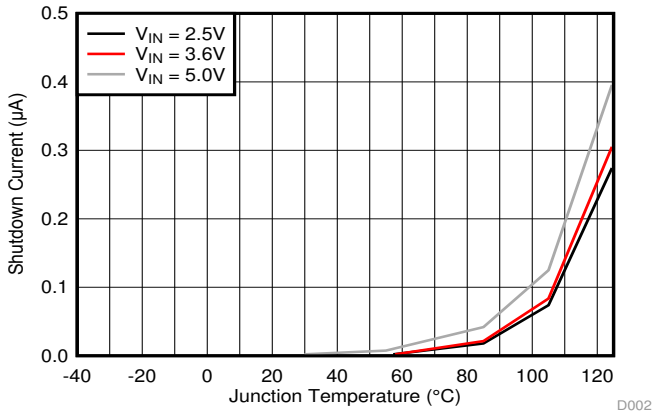


图 1. Shutdown Current vs Junction Temperature

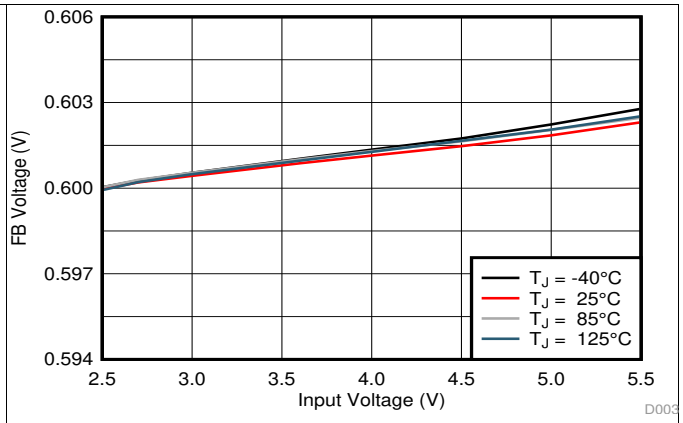


图 2. FB Voltage Accuracy

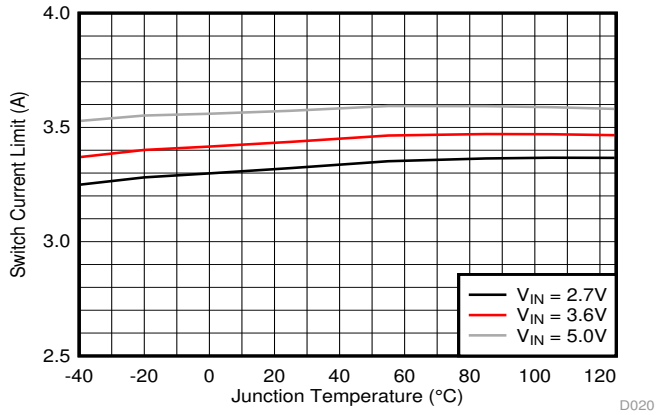


图 3. Switch Current Limit, TLV62569A

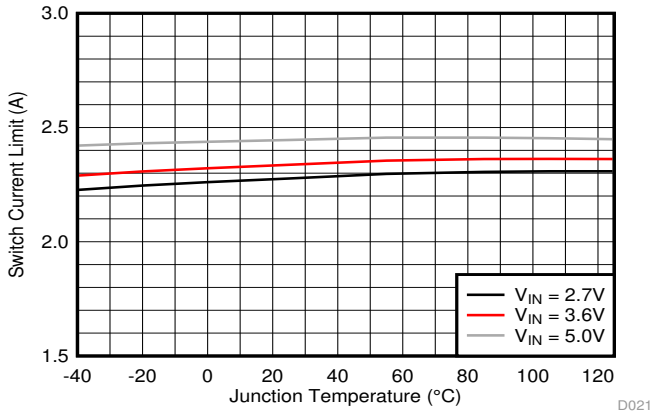


图 4. Switch Current Limit, TLV62568A

7 Detailed Description

7.1 Overview

The device is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with peak current control scheme. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) . Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

7.2 Functional Block Diagrams

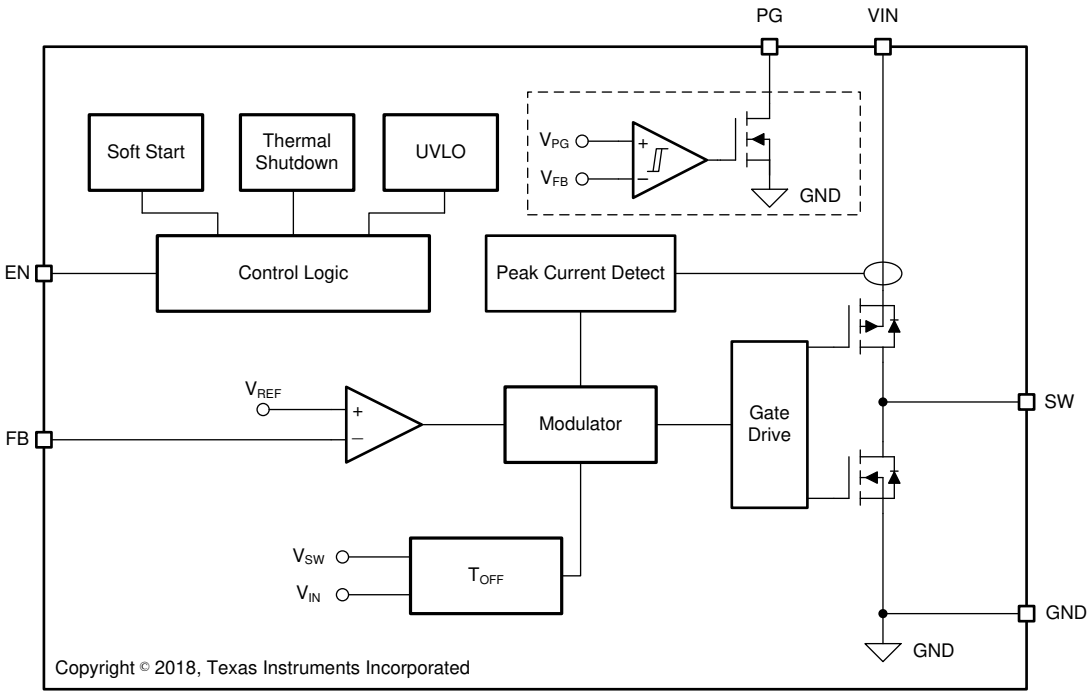


图 5. TLV62569A Functional Block Diagram

7.3 Feature Description

7.3.1 100% Duty Cycle Low Dropout Operation

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.2 Soft Startup

After enabling the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

Feature Description (接下页)

The device is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

7.3.3 Switch Current Limit

The switch current limit prevents the device from high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The device adopts the peak current control by sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to ramp down the inductor current with an adaptive off-time.

7.3.4 Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO} with V_{HYS_UVLO} hysteresis.

7.3.5 Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold, T_{JSD}. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enabling/Disabling the Device

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

7.4.2 Power Good

The TLV62568AP and TLV62569AP have a power good output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 2 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

表 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$1.4\ V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 1.4\ V$	√	

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

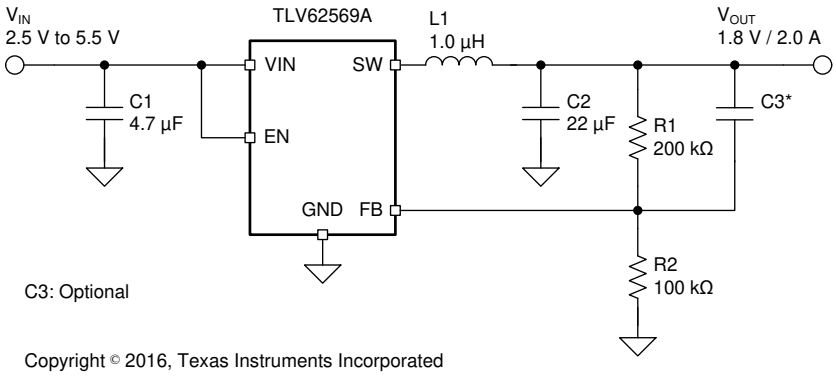


图 6. TLV62569A 1.8-V Output Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Maximum output current	2.0 A

表 3 lists the components used for the example.

表 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	4.7 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C2	22 µF, Ceramic Capacitor, 6.3 V, X7T, size 0805, GRM21BD70J226ME44	Murata
L1	1.0 µH, Power Inductor, size 4mmx4mm, XAL4020-102ME	Coilcraft
R1,R2,R3	Chip resistor,1%,size 0603	Std.
C3	Optional, 10 pF if it is needed	Std.

(1) See *Third-party Products Disclaimer*

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLV62569A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting the Output Voltage

An external resistor divider is used to set output voltage according to 公式 2.

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 200 kΩ for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

A feed forward capacitor, C3 improves the loop bandwidth to make a fast transient response (shown in 图 24). A 10-pF capacitance is recommended for R2 of 100-kΩ resistance. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289.

8.2.2.3 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 4 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

表 4. Matrix of Output Capacitor and Inductor Combinations

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)				
		4.7	10	22	47	100
0.6 ≤ V_{OUT} < 1.2	1				+	
1.2 ≤ V_{OUT}	1			++(3)	+	

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

8.2.2.4 Inductor Selection

The main parameters for inductor selection is inductor value and then saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 公式 3 is given:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where:

- $I_{OUT,MAX}$ is the maximum output current
- ΔI_L is the inductor current ripple

- f_{SW} is the switching frequency
- L is the inductor value (3)

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor.

8.2.2.5 Input and Output Capacitor Selection

The architecture of the device allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7T or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 4.7-µF input capacitance is sufficient; a larger value reduces input voltage ripple.

The device is designed to operate with an output capacitor of 22 µF to 47 µF, as outlined in 表 4.

8.2.3 Application Performance Curves

V_{IN} = 5 V, V_{OUT} = 1.8 V, T_A = 25 °C, external components shown in 表 3, unless otherwise noted.

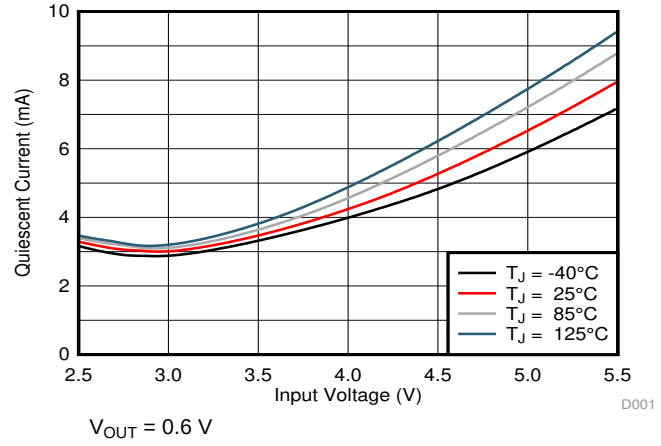


图 7. Quiescent Current

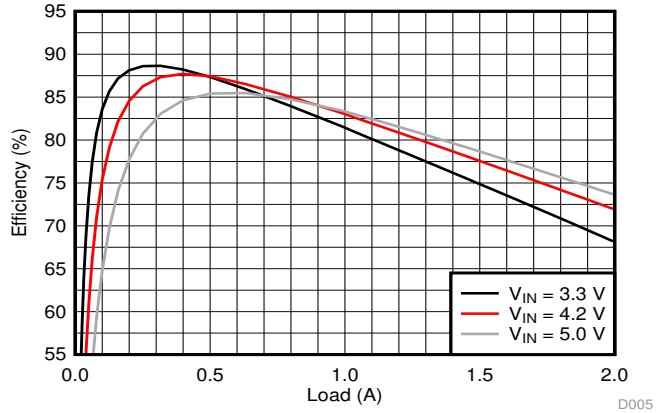


图 8. 0.6-V Output Efficiency

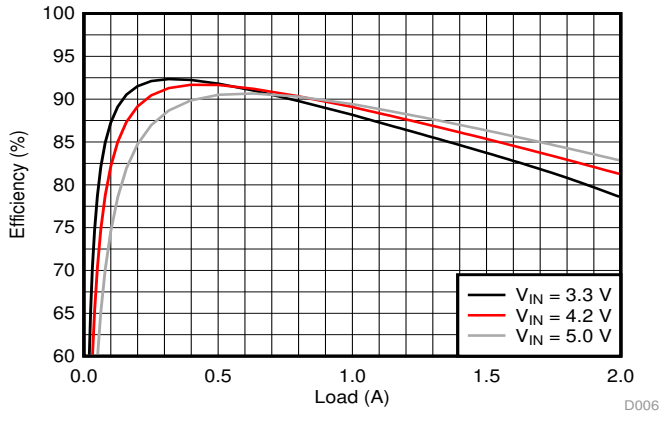


图 9. 1.2-V Output Efficiency

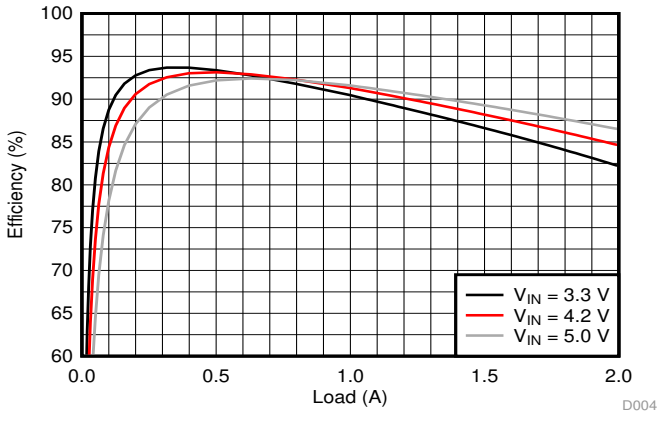


图 10. 1.8-V Output Efficiency

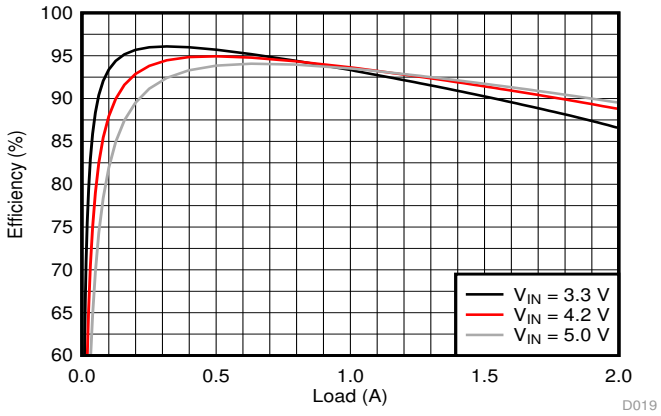


图 11. 2.5-V Output Efficiency

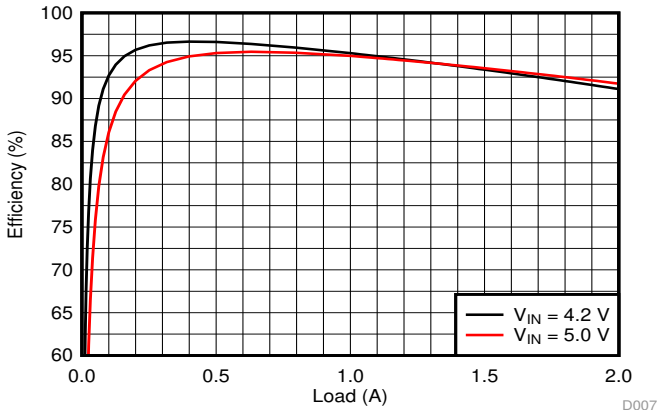


图 12. 3.3-V Output Efficiency

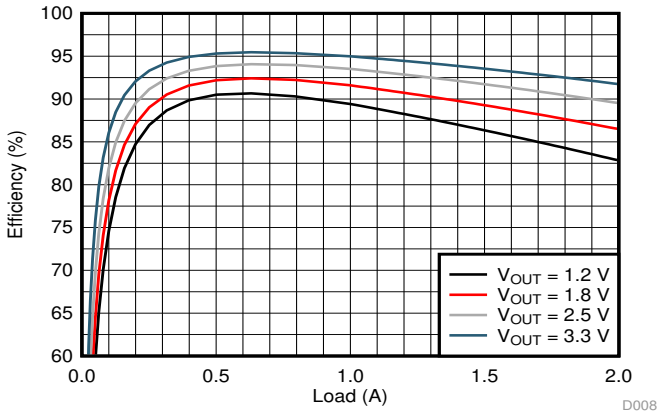


图 13. 5.0-V Input Efficiency

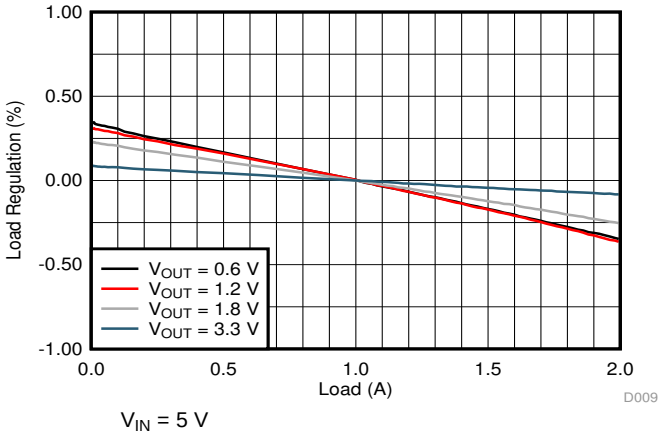


图 14. Load Regulation

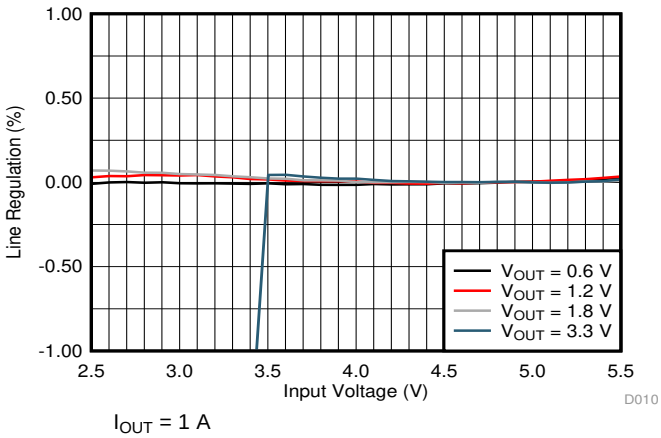


图 15. Line Regulation

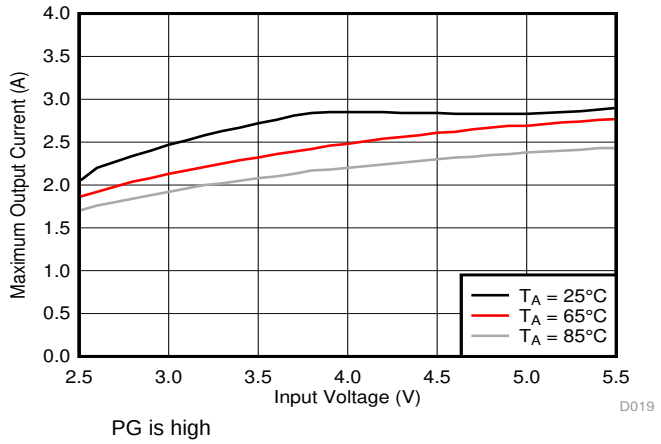
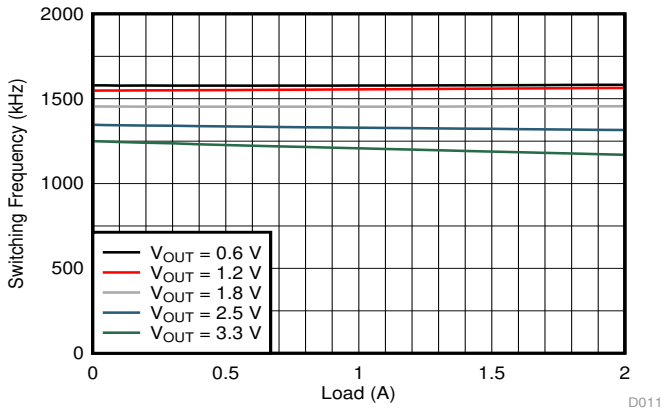
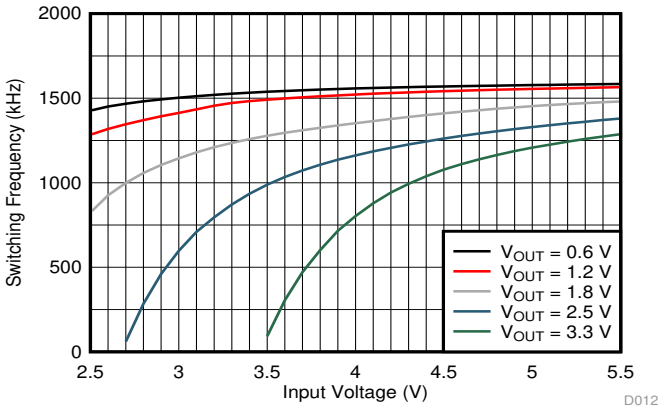


图 16. Maximum Output Current at V_{OUT} = 1.8 V



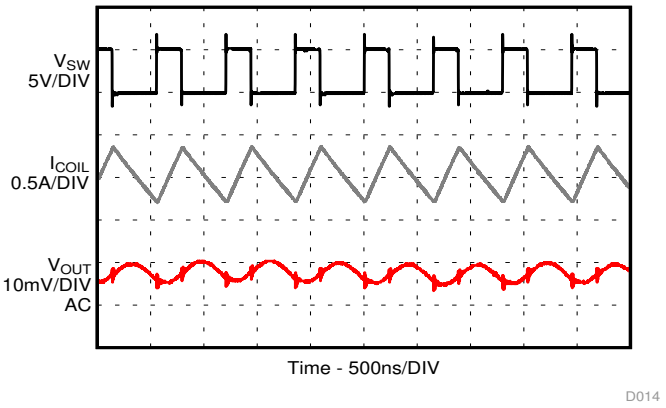
V_{IN} = 5 V

图 17. Switching Frequency vs Load



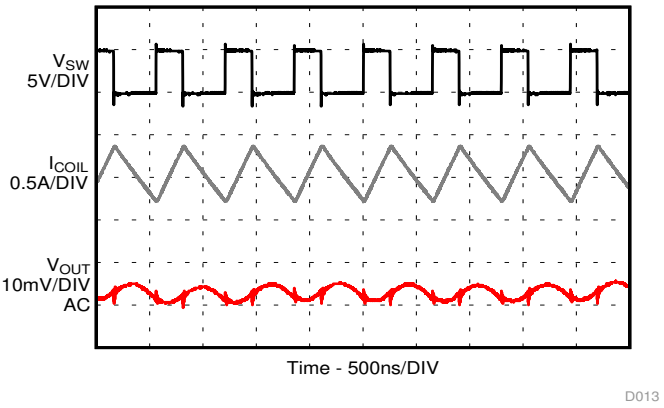
I_{OUT} = 1 A

图 18. Switching Frequency vs Input Voltage



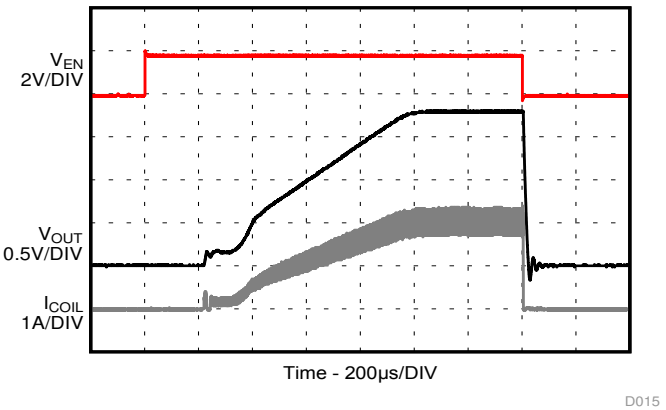
I_{OUT} = 36 mA

图 19. PWM Operation



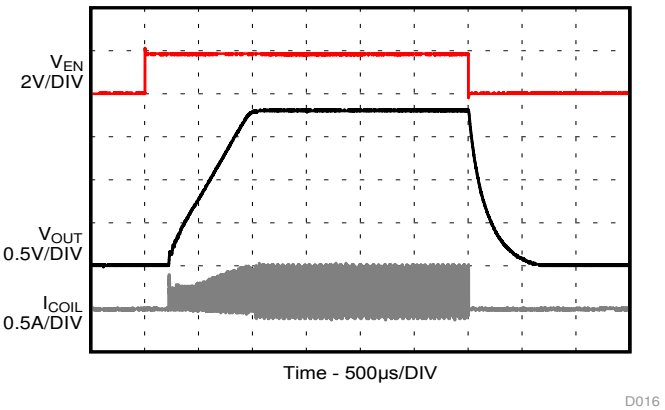
I_{OUT} = 1 A

图 20. PWM Operation



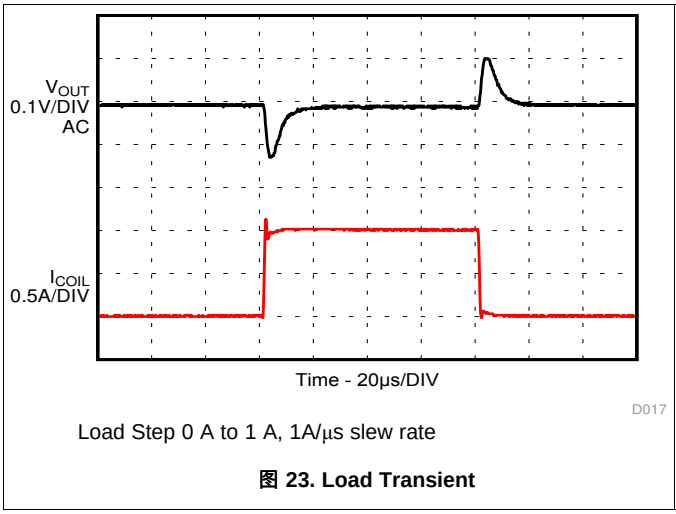
Load = 0.9 Ω

图 21. Startup and Shutdown with Load



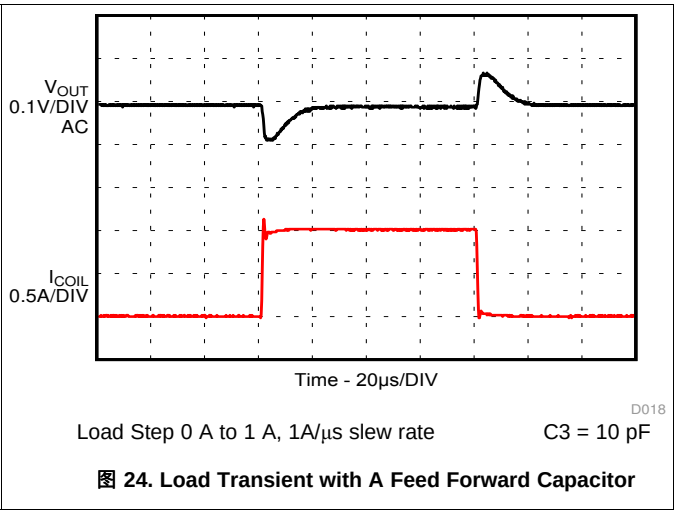
Load = 9 Ω

图 22. Startup and Shutdown with Load



Load Step 0 A to 1 A, 1A/µs slew rate

图 23. Load Transient



Load Step 0 A to 1 A, 1A/µs slew rate C3 = 10 pF

图 24. Load Transient with A Feed Forward Capacitor

9 Power Supply Recommendations

The power supply to the TLV62569A must have a current rating according to the supply voltage, output voltage and output current.

10 Layout

10.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TLV62569A device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB are signal traces. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- GND layers might be used for shielding.

10.2 Layout Example

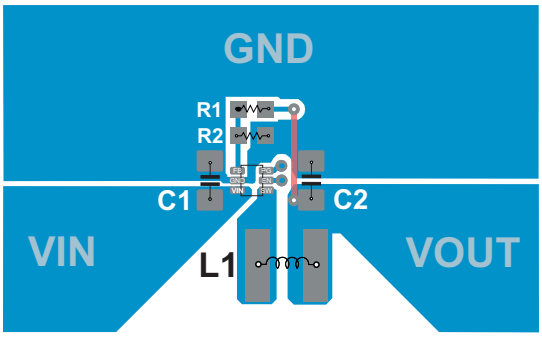


图 25. TLV62569APDRL Layout

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.1.2 开发支持

*11.1.2.1 使用 **WEBENCH®** 工具创建定制设计*

单击此处，使用 TLV62569A 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.2 文档支持

11.2.1 相关文档

- 德州仪器 (TI)，*《半导体和 IC 封装热指标》* 应用报告
- 德州仪器 (TI)，*《采用 JEDEC PCB 设计的线性和逻辑封装热工特性》* 应用报告

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 商标

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WEBENCH is a registered trademark of Texas Instruments.

11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62568ADRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BE	Samples
TLV62568ADRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BE	Samples
TLV62568APDRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BF	Samples
TLV62568APDRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BF	Samples
TLV62569ADRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BG	Samples
TLV62569ADRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BG	Samples
TLV62569APDRLR	ACTIVE	SOT-5X3	DRL	6	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BH	Samples
TLV62569APDRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1BH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

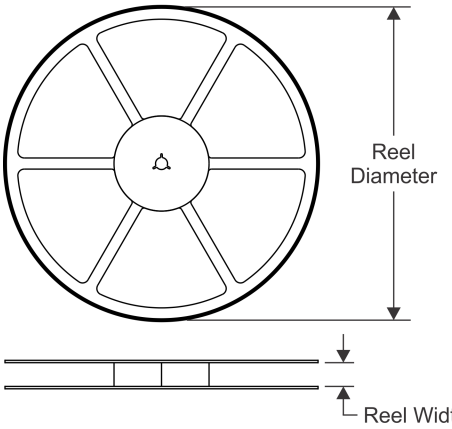
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

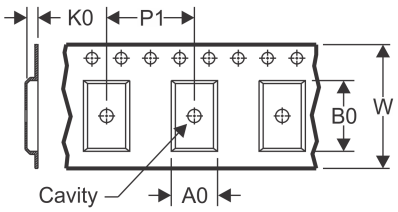
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

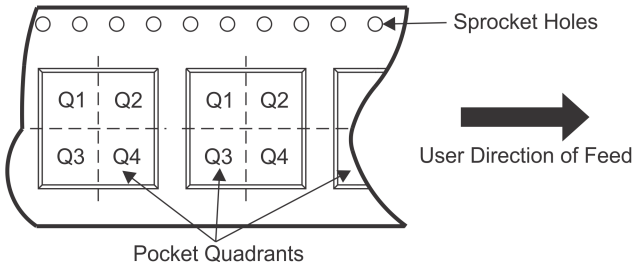


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

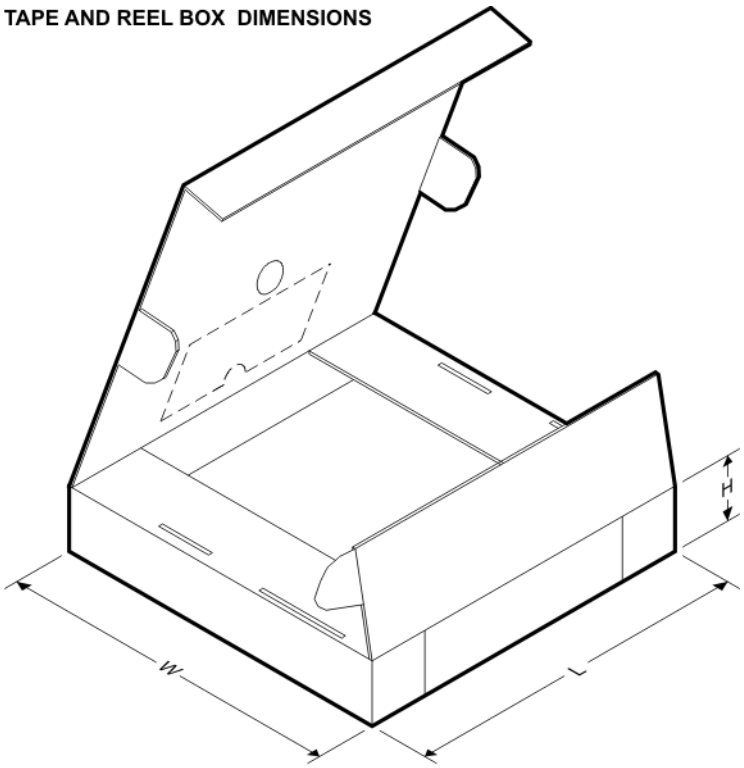
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62568ADRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62568ADRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62568APDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62568APDRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569ADRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569ADRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569APDRLR	SOT-5X3	DRL	6	3000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TLV62569APDRLT	SOT-5X3	DRL	6	250	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

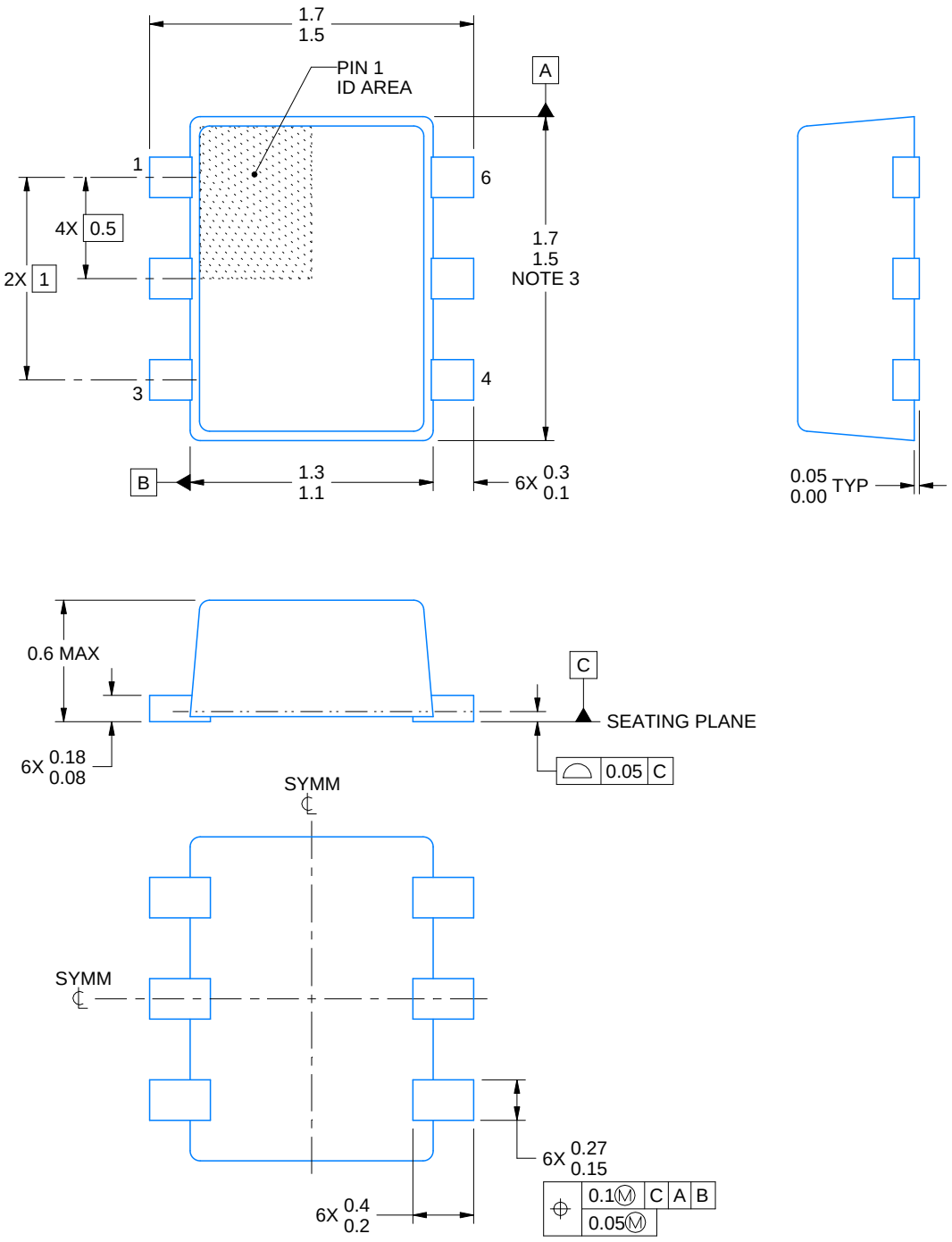
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62568ADRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62568ADRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62568APDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62568APDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62569ADRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62569ADRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0
TLV62569APDRLR	SOT-5X3	DRL	6	3000	210.0	185.0	35.0
TLV62569APDRLT	SOT-5X3	DRL	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0006A

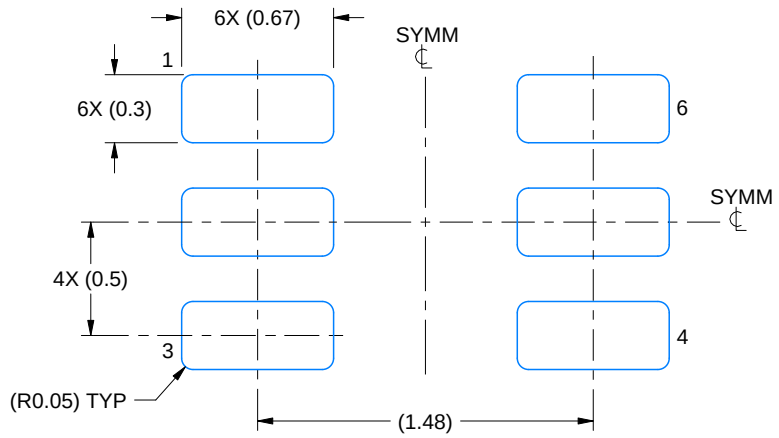
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

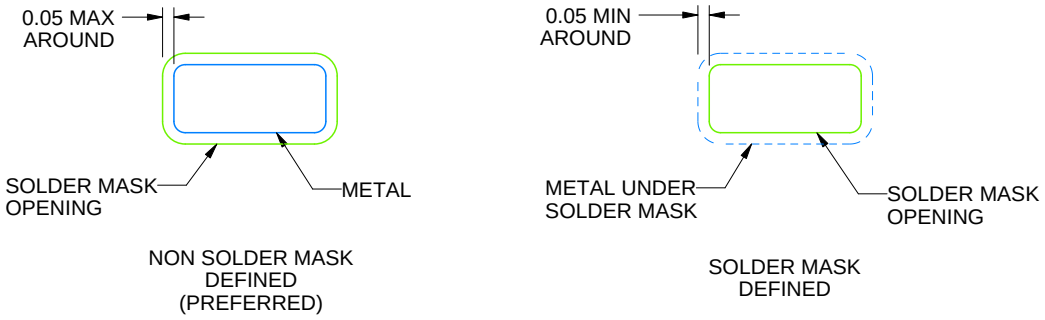


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

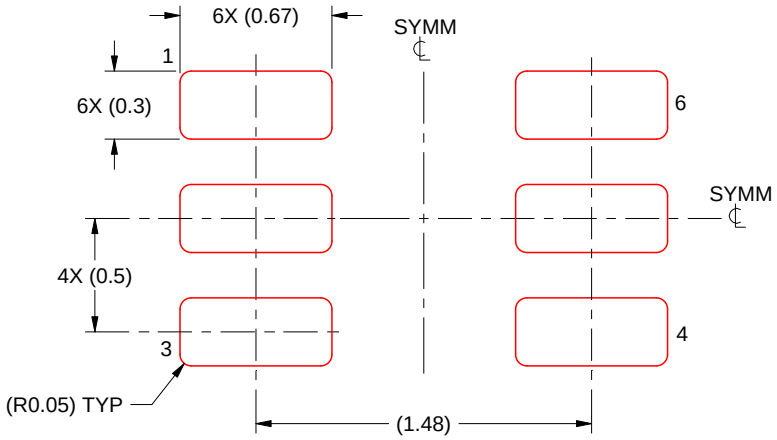
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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