

## LP8754 多相位六核降压转换器

### 1 特性

- 6 个高效降压 DC-DC 转换器内核：
  - 最大输出电流为 10A
  - 各内核捆绑到一个 6 相位转换器
  - 负载电流报告
  - 可编程过流保护 (OCP)
  - 自动脉宽调制 (PWM)/脉冲频率调制 (PFM) 和强制 PWM 操作以及自动低功耗模式设置
  - 自动增相/切相
  - 远程差分反馈电压感测
  - 输出电压斜升控制
  - $V_{OUT}$  范围为 0.6V 至 1.67V 进行动态电压调节 (DVS)
- I<sup>2</sup>C 兼容接口，支持标准 (100kHz)、快速 (400kHz) 和高速 (3.4MHz) 三种模式
- 四个可选的 I<sup>2</sup>C 地址
- 具有可编程屏蔽的中断功能
- 输出短路和输入过压保护 (OVP)
- 扩展频谱与相位控制，用于降低电磁干扰 (EMI)
- 过温保护 (OTP)
- 欠压闭锁 (UVLO)

### 2 应用

- 智能手机、电子书和平板电脑
- GSM、GPRS、EDGE、LTE、CDMA 和 WCDMA 手机
- 游戏设备

### 3 说明

LP8754 旨在满足移动电话和类似便携式应用中最新应用处理器的电源管理需求。此器件包含 6 个降压 DC-DC 转换器内核，一起捆绑在 6 相位降压转换器中。此器件由动态电压调节 (DVS) 接口或 I<sup>2</sup>C 兼容串行接口完全控制。

自动 PWM/PFM 操作搭配自动增相/切相功能，最大程度提高了宽泛输出电流范围内的效率。LP8754 支持进行远程差分电压感测，以补偿稳压器输出与负载点之间的 IR 下降，从而提高输出电压的精度。

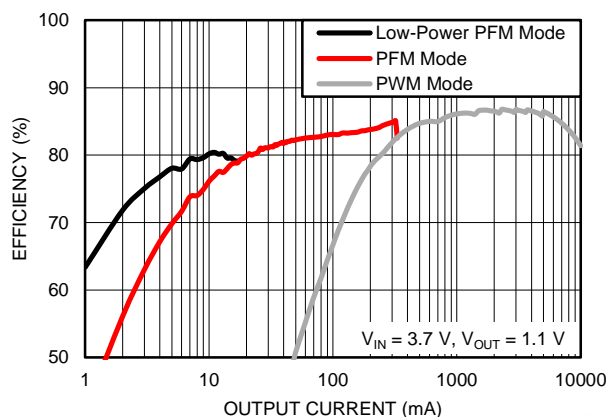
保护特性包括短路保护、电流限制、输入 OVP、UVLO、温度警告以及关断功能。此器件还提供多个错误标志，用于指示集成电路 (IC) 的状态信息。此外，I<sup>2</sup>C 回读信息包括总负载电流以及各降压内核的负载电流：LP8754 无需添加电流感测电阻就能感测到传递给负载的电流。在启动期间，器件会控制输出电压转换率，以最大程度降低过冲和浪涌电流。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (最大值)
LP8754	DSBGA (49)	3.022mm x 2.882mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

效率与负载电流间的关系



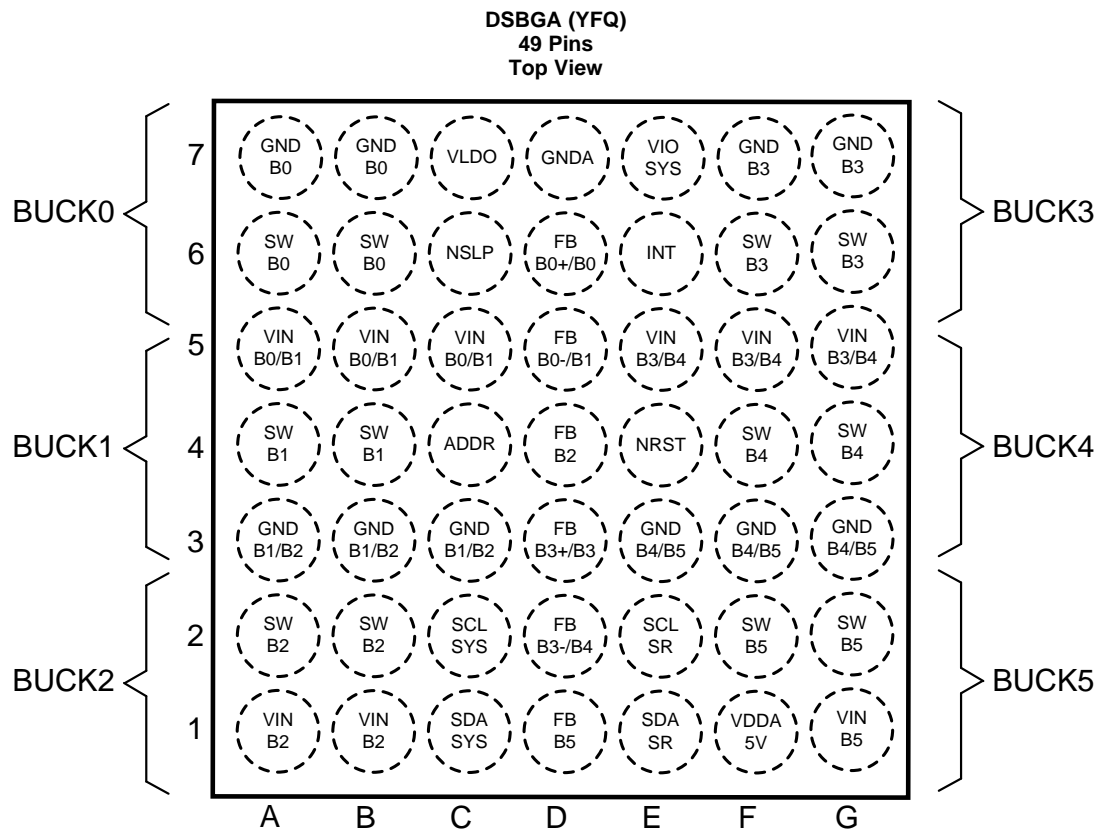
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## 4 修订历史记录

日期	修订版本	注释
2014 年 8 月	版本 A	初始 Web 版本

## 5 Pin Configuration and Functions



**Pin Functions**

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
A1, B1	VINB2	P	Input for Buck 2. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.
A2, B2	SWB2	A	Buck 2 switch node
A3, B3, C3	GNDB1/B2	G	Power Ground for Buck 1 and Buck 2
A4, B4	SWB1	A	Buck 1 switch node
A5, B5, C5	VINB0/B1	P	Input for Buck 0 and Buck 1. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.
A6, B6	SWB0	A	Buck 0 switch node
A7, B7	GNDB0	G	Power Ground for Buck 0
C1	SDASYS	D/I/O	Serial interface data input and output for system access. Connect a pullup resistor.
C2	SCLSYS	D/I	Serial interface clock input for system access. Connect a pullup resistor.
C4	ADDR	D/I	Serial bus address selection. Connect to GND (addr = 60h), VIOSYS (addr = 61h), SDASYS (addr = 62h) or SCLSYS (addr = 63h).
C6	NSLP	D/I	Full Power to Low Power state transition control signal (By default active LOW for Low-Power PFM mode)
C7	VLDO	A	Internal supply voltage capacitor pin. A ceramic low ESR 1- $\mu$ F capacitor should be connected from this pin to GNDA. The LDO voltage is generated internally, do NOT supply or load this pin externally.
D1	FBB5	A	Not used for six-phase converter. Connect to GND.
D2	FBB3-/B4	A	Not used for six-phase converter. Connect to GND.
D3	FBB3+/B3	A	Not used for six-phase converter. Connect to GND.
D4	FBB2	A	Not used for six-phase converter. Connect to GND.

**Pin Functions (continued)**

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
D5	FBB0-/B1	A	Remote sensing (negative). Connect to the respective sense pin of the processor or to the negative power supply trace of the processor as close as possible to the processor.
D6	FBB0+/B0	A	Remote sensing (positive). Connect to the respective sense pin of the processor or to the positive power supply trace of the processor as close as possible to the processor.
D7	GNDA	G	Ground
E1	SDASR	D/I/O	Serial Interface data input and output for Dynamic Voltage Scaling (DVS). Connect a pullup resistor / connect to GND if not used.
E2	SCLSR	D/I	Serial Interface clock input for DVS. Connect a pullup resistor / connect to GND if not used.
E3, F3, G3	GNDB4/B5	G	Power Ground for Buck 4 and Buck 5
E4	NRST	A	Voltage reference input for DVS interface. Setting NRST input HIGH triggers start-up sequence.
E5, F5, G5	VINB3/B4	P	Input for Buck 3 and Buck 4. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.
E6	INT	D/O	Open-drain interrupt output. Active LOW. Connect a pullup resistor to I/O supply.
E7	VIOSYS	A	This pin shall be tied to the system I/O-voltage. Bias supply voltage for the device. Enables the I/O interface: All registers are accessible via serial bus interface when this pin is pulled high. An internal power-on reset (POR) occurs when VIOSYS is toggled low/high. The I <sup>2</sup> C host should allow at least 500 $\mu$ s before sending data to the LP8754 after the rising edge of the VIOSYS line.
F1	VDDA5V	P	Input for Analog blocks
F2, G2	SWB5	A	Buck 5 switch node
F4, G4	SWB4	A	Buck 4 switch node
F6, G6	SWB3	A	Buck 3 switch node
F7, G7	GNDB3	G	Power Ground for Buck 3
G1	VINB5	P	Input for Buck 5. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.

A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
<b>INPUT VOLTAGE</b>			
Voltage on power connections (VIOSYS, VDDA5V, VINBXX)	-0.3	6	V
Voltage on logic pins (input or output pins) (SCLSYS, SDASYS, NRST, NSLP, ADDR, INT, SCLSR, SDASR)	-0.3	6	
Buck switch nodes (SWBXX)	-0.3	( $V_{VINBXX} + 0.2$ V) with 6 V max	V
VLDO, FBB0+/B0, FBB0-/B1, FBB2, FBB3+/B3, FBB3-/B4, FBB5	-0.3	2	V
All other analog pins	-0.3	6	
<b>TEMPERATURE</b>			
Junction temperature ( $T_{J-MAX}$ )		150	°C
Maximum lead temperature (soldering, 10 s) <sup>(1)</sup>		260	
Storage temperature, $T_{stg}$	-65	150	

(1) For detailed soldering specifications and information, please refer to Texas Instruments AN-1112: *DSBGA Wafer-Level Chip-Scale Package* (SNVA009).

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

	MIN	MAX	UNIT
<b>INPUT VOLTAGE</b>			
Voltage on power connections (VDDA5V, VINBXX)	2.5	5	V
Voltage on VIOSYS	1.8	smaller of 3.3 V or $V_{VINBXX}$	V
SCLSYS, SDASYS, ADDR	0	$V_{VIOSYS}$	V
SCLSR, SDASR, NSLP, INT	0	$V_{NRST}$	V
NRST	0	1.8	V
<b>TEMPERATURE</b>			
Junction temperature ( $T_J$ )	-40	125	°C
Ambient temperature ( $T_A$ )	-40	85	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground pin.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LP8754	UNIT
		YFQ	
		49 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.2	°C/W
$R_{\theta Jc top}$	Junction-to-case (top) thermal resistance	0.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	6.6	
$\psi_{JT}$	Junction-to-top characterization parameter	2.9	
$\psi_{JB}$	Junction-to-board characterization parameter	6.5	
$R_{\theta Jc bot}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 General Electrical Characteristics

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ; typical (TYP) values at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).  $V_{\text{VDDA5V}} = V_{\text{VINBXX}} = 3.7\text{ V}$ ,  $V_{\text{VIO SYS}} = V_{\text{NRST}} = 1.8\text{ V}$ ,  $V_{\text{OUT}} = 1.1\text{ V}$  (unless otherwise noted).<sup>(1)(2)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CURRENTS</b>					
$I_{\text{SHDN}}$	Shutdown supply current. Total current into power connections VDDA5V and VINBXX	$V_{\text{VIO SYS}} = 0\text{ V}$ , $V_{\text{NRST}} = 0\text{ V}$	0.1	2	$\mu\text{A}$
$I_{\text{STBY}}$	Standby mode supply current. Total current into power connections VDDA5V and VINBXX	$V_{\text{VIO SYS}} = 1.8\text{ V}$ , $V_{\text{NRST}} = 0\text{ V}$	50		
$I_{\text{Active}}$	Active mode current consumption. Total current into power connections VDDA5V and VINBXX	Low-power PFM Mode, no load, one core active		130	$\mu\text{A}$
		PFM Mode, no load, one core active		400	$\mu\text{A}$
		Forced PWM Mode, no load, one core active		14.5	mA
<b>LOGIC AND CONTROL INPUTS SCLSYS, SDASYS, ADDR</b>					
$V_{\text{IL}}$	Input low level	$V_{\text{VIO SYS}} = 1.8\text{ V to } 3.3\text{ V}$		$0.3 \times V_{\text{VIO SYS}}$	V
$V_{\text{IH}}$	Input high level	$V_{\text{VIO SYS}} = 1.8\text{ V to } 3.3\text{ V}$	$0.7 \times V_{\text{VIO SYS}}$		
$V_{\text{hys}}$	Hysteresis of Schmitt trigger inputs (SCLSYS, SDASYS)		$0.1 \times V_{\text{VIO SYS}}$		
$C_i$	Capacitance of pins	See <sup>(3)</sup>		4	pF
<b>LOGIC AND CONTROL INPUTS SCLSR, SDASR, NSLP, NRST</b>					
$V_{\text{IL}}$	Input low level	$V_{\text{NRST}} = 1.8\text{ V}$		$0.3 \times V_{\text{NRST}}$	V
$V_{\text{IH}}$	Input high level	$V_{\text{NRST}} = 1.8\text{ V}$	$0.7 \times V_{\text{NRST}}$		
$V_{\text{hys}}$	Hysteresis of Schmitt trigger inputs (SCLSR, SDASR)		$0.1 \times V_{\text{NRST}}$		
$C_i$	Capacitance of SCLSR and SDASR pins			4	pF
$R_{\text{IN}}$	Input resistance	NRST pulldown resistor to GND	1200		k $\Omega$
$V_{\text{IL\_NRST}}$	Input low level NRST			0.54	V
$V_{\text{IH\_NRST}}$	Input high level NRST		1.3		
<b>LOGIC AND CONTROL OUTPUTS</b>					
$V_{\text{OL}}$	Output low level	Voltage on INT pin, $I_{\text{SINK}} = 3\text{ mA}$ , $V_{\text{NRST}} = V_{\text{VIO SYS}} = 1.8\text{ V}$		0.4	V
		Voltage on SDASYS, SDASR, $I_{\text{SINK}} = 3\text{ mA}$ , $V_{\text{NRST}} = V_{\text{VIO SYS}} = 1.8\text{ V}$		0.36	
$R_{\text{P}}$	External pullup resistor for INT	To I/O Supply	10		k $\Omega$
<b>ALL LOGIC AND CONTROL INPUTS</b>					
$I_{\text{LEAK}}$	Input current	All logic inputs over pin voltage range. Note that NRST pin does have an 1.2-M $\Omega$ internal pulldown resistor and current through this resistor is not included into $I_{\text{LEAK}}$ rating. $T_A = 25^{\circ}\text{C}$	-1	1	$\mu\text{A}$

(1) All voltage values are with respect to network ground pin.

(2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical (Typ.) numbers are not ensured, but do represent the most likely norm.

(3) Maximum capacitance of SCLSYS or SDASYS line is 8 pF, if ADDR pin is connected to line for serial bus address selection.

## 6.6 6-Phase Buck Electrical Characteristics

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ; typical (TYP) values at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).  $V_{\text{VDDA5V}} = V_{\text{VINBXX}} = 3.7\text{ V}$ ,  $V_{\text{VIOSYS}} = V_{\text{NRST}} = 1.8\text{ V}$ ,  $V_{\text{OUT}} = 1.1\text{ V}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{\text{FB}}$	Differential feedback voltage <sup>(1)</sup> $V_{\text{FB0+}/\text{B0}} - V_{\text{FB0-}/\text{B1}}$	PWM Mode, $V_{\text{OUTSET}} = 0.6\text{ V to }1.67\text{ V}$ , $I_{\text{OUT}} \leq 10\text{ A}$ <sup>(2)</sup>	min ( $V_{\text{OUTSET}} - 2.5\%$ , $V_{\text{OUTSET}} - 25\text{ mV}$ )	$V_{\text{OUTSET}}$	max( $V_{\text{OUTSET}} + 2.5\%$ , $V_{\text{OUTSET}} + 25\text{ mV}$ )	V
		PFM Mode, $V_{\text{OUTSET}} = 0.6\text{ V to }1.67\text{ V}$ , $I_{\text{OUT}} \leq 375\text{ mA}$	min ( $V_{\text{OUTSET}} - 2.5\%$ , $V_{\text{OUTSET}} - 25\text{ mV}$ )	$V_{\text{OUTSET}}$	max( $V_{\text{OUTSET}} + 2.5\%$ , $V_{\text{OUTSET}} + 25\text{ mV}$ )	
		Low-Power PFM Mode, $V_{\text{OUTSET}} = 0.6\text{ V to }1.67\text{ V}$ , $I_{\text{OUT}} \leq 30\text{ mA}$	min ( $V_{\text{OUTSET}} - 3\%$ , $V_{\text{OUTSET}} - 30\text{ mV}$ )	$V_{\text{OUTSET}}$	max( $V_{\text{OUTSET}} + 3\%$ , $V_{\text{OUTSET}} + 30\text{ mV}$ )	
$I_{\text{LIMITP}}$	High side switch current limit	2.5-A register setting	2050	2600	3300	mA
$I_{\text{LIMITN}}$	Low side switch current limit	Reverse current	650	900	1050	
$V_{\text{OUT}}$	Output voltage	Range, programmable by register setting	0.6	1.1	1.67	V
		Step		10		mV
$f_{\text{SW}}$	Switching frequency	$2.5\text{ V} \leq V_{\text{VINBXX}} \leq 5\text{ V}$	2.7	3.0	3.4	MHz
$R_{\text{DSON\_P}}$	Pin-pin resistance for PFET	Test current = 200 mA; Split FET		120		mΩ
		Test current = 200 mA; Full FET		60		
$R_{\text{DSON\_N}}$	Pin-pin resistance for NFET	$I_{\text{OUT}} = -200\text{ mA}$		50		μA
$I_{\text{LK\_HS}}$	High-side leakage current	$V_{\text{SW}} = 0\text{ V}$ , Per Buck Core			2	μA
$I_{\text{LK\_LS}}$	Low-side leakage current	$V_{\text{SW}} = 3.7\text{ V} = V_{\text{VINBXX}}$ , per buck core			2	
$R_{\text{PD}}$	Pull-down resistor	Enabled via control register, Active only when converter disabled, Per Buck Core		250		Ω
$R_{\text{IN\_FB}}$	Differential feedback Input resistance <sup>(3)</sup>	$T_A = 25^{\circ}\text{C}$	200	300	400	kΩ

- Due to the nature of the converter operating in PFM Mode/Low-Power Mode, the feedback voltage accuracy specification is for the lower point of the ripple. Thus the converter will position the average output voltage typically slightly above the nominal PWM-Mode output voltage.
- The power switches in the LP8754 are designed to operate continuously with currents up to the switch current limit thresholds. However, when continuously operating at high current levels there will be significant heat generated within the IC and thus sustained total DC current which the device can support is typically limited by thermal constraints. Thermal issues will become extremely important when designing PCB and the thermal environment of the LP8754. PCB with high thermal efficiency is required to ensure the junction temperature is kept below  $125^{\circ}\text{C}$ . Completing thermal analyses in early stages of the product design process is highly recommended to predict thermal performance at board level. Under high current load conditions the serial bus master device must monitor the temperature of the converter using the Thermal warning feature, see [Protection Features Characteristics](#). If the 2nd thermal warning is triggered at  $120^{\circ}\text{C}$ , the application must quickly decrease the load current to keep the converter within its recommended operating temperature.
- Datasheet min/max specification limits are specified by design.



## 6.7 6-Phase Buck System Characteristics

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ; typical (TYP) values at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).  $V_{\text{VDDA5V}} = V_{\text{VINBXX}} = 3.7\text{ V}$ ,  $V_{\text{VIOSYS}} = V_{\text{NRST}} = 1.8\text{ V}$ ,  $V_{\text{OUT}} = 1.1\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$K_{\text{RAMP}}$	Ramp timer	Programmable via control register <sup>(1)</sup>				mV/ $\mu\text{s}$
		RAMP_B0[2:0] = 000		30		
		RAMP_B0[2:0] = 001		15		
		RAMP_B0[2:0] = 010		7.5		
		RAMP_B0[2:0] = 011		3.8		
		RAMP_B0[2:0] = 100		1.9		
		RAMP_B0[2:0] = 101		0.94		
		RAMP_B0[2:0] = 110		0.47		
		RAMP_B0[2:0] = 111		0.23		
$T_{\text{START}}$	Start-up time	Time from NRST-HIGH to start of switching		25		$\mu\text{s}$
$T_{\text{RAMP}}$	$V_{\text{OUT}}$ rise time	Time to ramp from 5% to 95% of $V_{\text{OUT}}$		20		$\mu\text{s}$
$I_{\text{PFM-PWM}}$	PFM-to-PWM switch-over current threshold	Average output current, programmable via control register, $V_{\text{OUT}} = 1.1\text{ V}$ . <sup>(2)</sup>				mA
		PFM_EXIT_B0[2:0] = 011		175		
		PFM_EXIT_B0[2:0] = 100		225		
		PFM_EXIT_B0[2:0] = 101		275		
		PFM_EXIT_B0[2:0] = 110		325		
$I_{\text{PWM-PFM}}$	PWM-to-PFM switchover current threshold	Average output current, Programmable via control register, $V_{\text{OUT}} = 1.1\text{ V}$ . <sup>(2)</sup>				mA
		PFM_ENTRY_B0[2:0] = 000		100		
		PFM_ENTRY_B0[2:0] = 001		125		
		PFM_ENTRY_B0[2:0] = 010		150		
		PFM_ENTRY_B0[2:0] = 011		175		
$I_{\text{ADD}}$	Phase adding level	ADD_PH_B0[2:0] = 010		500		mA
		ADD_PH_B0[2:0] = 011		600		
		ADD_PH_B0[2:0] = 100		700		
		ADD_PH_B0[2:0] = 101		800		
		ADD_PH_B0[2:0] = 110		900		
		ADD_PH_B0[2:0] = 111		1000		
$I_{\text{SHED}}$	Phase shedding level	SHED_PH_B0[2:0] = 000		300		mA
		SHED_PH_B0[2:0] = 001		400		
		SHED_PH_B0[2:0] = 010		500		
		SHED_PH_B0[2:0] = 011		600		
		SHED_PH_B0[2:0] = 100		700		
		SHED_PH_B0[2:0] = 101		800		

(1) In the real application, achievable output voltage ramp profiles are influenced by a number of factors, including the amount of output capacitance, the load current level, the load characteristic (either resistive or constant-current), and the voltage ramp amplitude. Typical values are measured with typical conditions. The falling edge ramp rate can be limited by the negative current limit  $I_{\text{LIMITN}}$ .

(2) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependant on the output voltage, input voltage, and the inductor current level. Typical values are measured with typical conditions.

## 6-Phase Buck System Characteristics (continued)

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ; typical (TYP) values at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).  $V_{\text{VDDA5V}} = V_{\text{VINBXX}} = 3.7\text{ V}$ ,  $V_{\text{VIOSYS}} = V_{\text{NRST}} = 1.8\text{ V}$ ,  $V_{\text{OUT}} = 1.1\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$\Delta V_{\text{OUT}}$	Line regulation	$2.5\text{ V} \leq V_{\text{VINBXX}} \leq 5\text{ V}$ $I_{\text{LOAD}} = 1\text{ A}$ , forced PWM		0.05		%/V	
	Load regulation in PWM mode of operation	$100\text{ mA} \leq I_{\text{LOAD}} \leq 10\text{ A}$ , Differential sensing enabled		0.2		%/A	
	Transient load step response	AUTO (no Low-Power PFM) mode, $I_{\text{OUT}} 0.5\text{ mA} \rightarrow 500\text{ mA} \rightarrow 0.5\text{ mA}$ , 100 ns load step			$\pm 30$		mV
		PWM mode, $I_{\text{OUT}} 0.6\text{ A} \rightarrow 2\text{ A} \rightarrow 0.6\text{ A}$ , 400-ns load step			$\pm 20$		mV
		PWM mode, $I_{\text{OUT}} 1\text{ A} \rightarrow 8\text{ A} \rightarrow 1\text{ A}$ , 400-ns load step			$\pm 60$		mV
Transient line response	$V_{\text{VINBXX}}$ stepping $3.3\text{ V} \leftrightarrow 3.8\text{ V}$ , $t_r = t_f = 10\text{ }\mu\text{s}$ , $I_{\text{OUT}} = 2000\text{ mA DC}$			$\pm 15$		mV	
$I_{\text{OUT}}$	Output current	DC load each phase			1670	mA	
		Six phases combined <sup>(3)</sup>			10000		
$C_{\text{OUT}}$	Output capacitance <sup>(4)</sup>	Effective capacitance during operation, $V_{\text{OUT}} = 0.6\text{ V}$ to $1.67\text{ V}$ , Min value over $T_A -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	30	50		$\mu\text{F}$	
$C_{\text{IN}}$	Input capacitance on each input voltage rail <sup>(4)(5)</sup>	Effective capacitance during operation, $2.5\text{ V} \leq V_{\text{VINBXX}} \leq 5\text{ V}$	2.5	10		$\mu\text{F}$	
L	Output inductance	Effective inductance during operation	0.25	0.47	1	$\mu\text{H}$	
$I_{\text{BALANCE}}$	Current balancing accuracy	$I_{\text{OUT}} \geq 1000\text{ mA}$		< 10%			
$V_{\text{RIPPLE\_PWM}}$	Output voltage ripple PWM mode, One phase active <sup>(6)</sup>	$C_{\text{OUT}} \text{ ESR} = 10\text{ m}\Omega$ PWM mode, $I_{\text{OUT}} = 200\text{ mA}$ Switching frequency = 3 MHz		7		mV <sub>PP</sub>	
$V_{\text{RIPPLE\_PFM}}$	Output voltage ripple PFM mode <sup>(6)</sup>	$C_{\text{OUT}} \text{ ESR} = 10\text{ m}\Omega$ PFM mode $I_{\text{OUT}} = 100\text{ }\mu\text{A}$		8		mV <sub>PP</sub>	
$V_{\text{RIPPLE\_LP}}$	Output Voltage Ripple Low-Power PFM mode <sup>(6)</sup>	$C_{\text{OUT}} \text{ ESR} = 10\text{ m}\Omega$ Low-power PFM mode $I_{\text{OUT}} = 100\text{ }\mu\text{A}$		8		mV <sub>PP</sub>	

- (3) The power switches in the LP8754 are designed to operate continuously with currents up to the switch current limit thresholds. However, when continuously operating at high current levels there will be significant heat generated within the IC and thus sustained total DC current which the device can support is typically limited by thermal constraints. Thermal issues will become extremely important when designing PCB and the thermal environment of the LP8754. PCB with high thermal efficiency is required to ensure the junction temperature is kept below  $125^{\circ}\text{C}$ . Completing thermal analyses in early stages of the product design process is highly recommended to predict thermal performance at board level. Under high current load conditions the serial bus master device must monitor the temperature of the converter using the Thermal warning feature, see [Protection Features Characteristics](#). If the 2nd thermal warning is triggered at  $120^{\circ}\text{C}$ , the application must quickly decrease the load current to keep the converter within its recommended operating temperature.
- (4) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics. The performance of the LP8754 device depends greatly on the care taken in designing the Printed Circuit Board (PCB). The use of low inductance and low serial resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the IC and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance and capacitance can easily become the performance limiting items.
- (5) In addition to these capacitors, at least one higher value capacitor (for example,  $22\text{ }\mu\text{F}$ ) should be placed close to the power pins. Note that cores B0-B1 and B3-B4 do have combined power input pins.
- (6) Ripple voltage should be measured at  $C_{\text{OUT}}$  electrode on a well-designed PCB, using suggested inductors and capacitors and with a high-quality scope probe.

### 6.8 Protection Features Characteristics

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ; typical (TYP) at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).  $V_{\text{VDDA5V}} = V_{\text{VINBXX}} = 3.7\text{ V}$ ,  $V_{\text{VIOSYS}} = V_{\text{NRST}} = 1.8\text{ V}$ ,  $V_{\text{OUT}} = 1.1\text{ V}$  (unless otherwise noted).

### Protection Features Characteristics (continued)

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ; typical (TYP) at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).  $V_{VDDA5V} = V_{VINBXX} = 3.7\text{ V}$ ,  $V_{VIOSYS} = V_{NRST} = 1.8\text{ V}$ ,  $V_{OUT} = 1.1\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VOLTAGE MONITORING</b>						
$V_{PG}$	Power good threshold voltage	Power good threshold for voltage decreasing, % of setting, $V_{OUT} = 1.1\text{ V}$	90%			
$V_{OVP}$	Input overvoltage protection trigger point <sup>(1)(2)</sup>	$V_{IN}$ rising. Voltage monitored on VDDA5V pin	5.15	5.3	5.45	V
$V_{UVLO}$	Input undervoltage lockout (UVLO) turn-on threshold <sup>(1)</sup>	$V_{IN}$ falling. Voltage monitored on VDDA5V pin	2.15	2.25	2.35	
$V_{SCP}$	Output short-circuit fault threshold	Detected by sensing the voltage on converter output with respect to GND.	400			mV
$t_{MASKSCP}$	SCP masking time	Triggered by converter start-up, specified by design	400			$\mu\text{s}$
$t_{MASKPG}$	Power Good masking time	Triggered by converter start-up, specified by design	400			$\mu\text{s}$
		Triggered by VSET transition, specified by design Slew Rate setting mV/ $\mu\text{s}$				
		30	50			$\mu\text{s}$
		15	100			
		7.5	200			
		3.8	400			
		1.9	800			
		0.94	1600			
		0.47	3200			
0.23	6400					

- (1) Undervoltage lockout (UVLO) and overvoltage protection (OVP) circuits shut down the LP8754 when the system input voltage is outside the desired operating range.
- (2) Limits for OVP trigger points apply when  $V_{VIOSYS}$  is high. False OVP alarm may occur, if the input voltage rises close to 5 V while  $V_{VIOSYS}$  is low.

### Protection Features Characteristics (continued)

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ; typical (TYP) at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted).  $V_{VDDA5V} = V_{VINBXX} = 3.7\text{ V}$ ,  $V_{VIOSYS} = V_{NRST} = 1.8\text{ V}$ ,  $V_{OUT} = 1.1\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>THERMAL SHUTDOWN AND MONITORING</b>						
T <sub>SHUT</sub>	Thermal shutdown (TSD)	Threshold, Temperature rising		150		°C
		Hysteresis		25		
T <sub>WARN</sub>	Thermal warning	Temperature rising, 1 <sup>st</sup> warning, Interrupt only		85		
		Hysteresis		10		
	Thermal warning prior to TSD	Temperature rising, 2 <sup>nd</sup> warning, Interrupt and flag set		120		
		Hysteresis		10		

### 6.9 I<sup>2</sup>C Serial Bus Timing Parameters

Serial bus address is selected by the ADDR pin. Connect the pin to GND (addr = 60h), VIOSYS (addr = 61h), SDASYS (addr = 62h), or SCLSYS (addr = 63h). Both of the serial buses share the same address; that is, if addr = 60h is selected for the System bus, the Dynamic Voltage Scaling bus will respond to the same address. Start conditions are used to secure the I<sup>2</sup>C slave address. During the I<sup>2</sup>C bus start condition, it is detected whether the ADDR is connected to SDASYS, SCLSYS, GND, or VIOSYS. The I<sup>2</sup>C host should allow at least 500 μs before sending data to the LP8754 after the rising edge of the VIOSYS line.

These specifications are ensured by design. Limits apply over the full ambient temperature range  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $V_{VDDA5V} = V_{VINBXX} = 3.7\text{ V}$ ,  $V_{VIOSYS} = V_{NRST} = 1.8\text{ V}$ ,  $V_{OUT} = 1.1\text{ V}$  (unless otherwise noted) (See [Figure 1](#)).

			MIN	NOM	MAX	UNIT
<b>DIGITAL TIMING SPECIFICATIONS (SCL, SDA)<sup>(1)(2)(3)</sup></b>						
f <sub>CLK</sub>	Serial clock frequency	Standard mode			100	kHz
		Fast mode			400	
		High-speed mode, C <sub>b</sub> = 100 pF (max)			3.4	MHz
		High-speed mode, C <sub>b</sub> = 400 pF (max) <sup>(4)</sup>			1.7	
t <sub>LOW</sub>	SCL low time	Standard mode	4.7			μs
		Fast mode	1.3			
		High-speed mode, C <sub>b</sub> = 100 pF (max)	160			ns
		High-speed mode, C <sub>b</sub> = 400 pF (max) <sup>(4)</sup>	320			
t <sub>HIGH</sub>	SCL high time	Standard mode	4			μs
		Fast mode	0.6			
		High-speed mode, C <sub>b</sub> = 100 pF (max)	60			ns
		High-speed mode, C <sub>b</sub> = 400 pF (max) <sup>(4)</sup>	120			
t <sub>SU;DAT</sub>	Data setup time	Standard mode	250			ns
		Fast mode	100			
		High-speed mode	10			
t <sub>HD;DAT</sub>	Data hold time	Standard mode	0		3.45	μs
		Fast mode	0		0.9	
		High-speed mode, C <sub>b</sub> = 100 pF (max)	0		70	ns
		High-speed mode, C <sub>b</sub> = 400 pF (max) <sup>(4)</sup>	0		150	

- (1) Unless otherwise stated, 'SDA' in this paragraph refers to both of the SDASR and SDASYS signals, and respectively 'SCL' refers to SCLSR and SCLSYS signals.
- (2) C<sub>b</sub> refers to the capacitance of one bus line. C<sub>b</sub> is expressed in pF units. The specification table provided applies to both of the interfaces; DVS and System interface.
- (3) The power-on default setting for the system bus and the DVS bus is High-speed-enabled, there is no handshaking required to initiate high speed.
- (4) For bus line loads C<sub>b</sub> between 100 pF and 400 pF the timing parameters must be linearly interpolated.

## I<sup>2</sup>C Serial Bus Timing Parameters (continued)

Serial bus address is selected by the ADDR pin. Connect the pin to GND (addr = 60h), VIOSYS (addr = 61h), SDASYS (addr = 62h), or SCLSYS (addr = 63h). Both of the serial buses share the same address; that is, if addr = 60h is selected for the System bus, the Dynamic Voltage Scaling bus will respond to the same address. Start conditions are used to secure the I<sup>2</sup>C slave address. During the I<sup>2</sup>C bus start condition, it is detected whether the ADDR is connected to SDASYS, SCLSYS, GND, or VIOSYS. The I<sup>2</sup>C host should allow at least 500 μs before sending data to the LP8754 after the rising edge of the VIOSYS line.

These specifications are ensured by design. Limits apply over the full ambient temperature range  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $V_{\text{VDDA5V}} = V_{\text{VINBXX}} = 3.7\text{ V}$ ,  $V_{\text{VIOSYS}} = V_{\text{NRST}} = 1.8\text{ V}$ ,  $V_{\text{OUT}} = 1.1\text{ V}$  (unless otherwise noted) (See Figure 1).

			MIN	NOM	MAX	UNIT
t <sub>SU;STA</sub>	Set-up time for a repeated start condition	Standard mode	4.7			μs
		Fast mode	0.6			
		High-speed mode	160			ns
t <sub>HD;STA</sub>	Hold time for a start or a repeated start condition	Standard mode	4.0			μs
		Fast mode	0.6			
		High-speed mode	160			ns
t <sub>BUF</sub>	Bus free time between a stop and start condition	Standard mode	4.7			μs
		Fast mode	1.3			
t <sub>SU;STO</sub>	Set-up time for a stop condition	Standard mode	4.0			μs
		Fast mode	0.6			
		High-speed mode	160			ns
t <sub>rDA</sub>	Rise time of SDA signal	Standard mode			1000	ns
		Fast mode	20		300	ns
		High-speed mode, C <sub>b</sub> = 100 pF (max)	10		80	ns
		High-speed mode, C <sub>b</sub> = 400 pF (max) <sup>(4)</sup>	20		160	ns
t <sub>fDA</sub>	Fall time of SDA signal	Standard mode			300	ns
		Fast Mode	6.5		300	ns
		High-speed mode, C <sub>b</sub> = 100 pF (max)	10		80	ns
		High-speed mode, C <sub>b</sub> = 400 pF (max) <sup>(4)</sup>	20		160	ns
t <sub>rCL</sub>	Rise time of SCL signal	Standard mode			1000	ns
		Fast mode	20		300	ns
		High-speed mode, C <sub>b</sub> = 100 pF (max)	10		40	ns
		High-speed mode, C <sub>b</sub> = 400 pF (max) <sup>(4)</sup>	20		80	ns
t <sub>rCL1</sub>	Rise time of SCL signal after a repeated start condition and after acknowledge bit	High-speed mode, C <sub>b</sub> = 100 pF (max)	10		80	ns
		High-speed mode, C <sub>b</sub> = 400 pF (max) <sup>(4)</sup>	20		160	ns
t <sub>fCL</sub>	Fall time of a SCL signal	Standard mode			300	ns
		Fast mode	6.5		300	ns
		High-speed mode, C <sub>b</sub> = 100 pF (max)	10		40	ns
		High-speed mode, C <sub>b</sub> = 400 pF (max) <sup>(4)</sup>	20		80	ns
C <sub>b</sub>	Capacitive load for each bus line (SCL and SDA)				400	pF
t <sub>SP</sub>	Pulse width of spike suppressed <sup>(5)</sup>	Fast mode			50	ns
		High-speed mode			10	

(5) Spike suppression filtering on SCLSYS, SCLSR, SDASYS and SDASR will suppress spikes that are less than the indicated width.

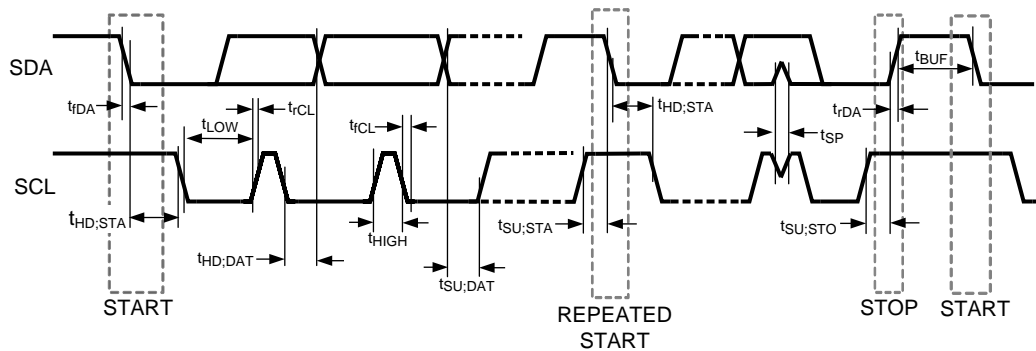


Figure 1. I<sup>2</sup>C Timing

### 6.10 Typical Characteristics

Unless otherwise specified:  $V_{VDDA5V} = V_{VINBXX} = 3.7\text{ V}$ ,  $V_{OUT} = 1.1\text{ V}$ ,  $T_A = 25^\circ\text{C}$

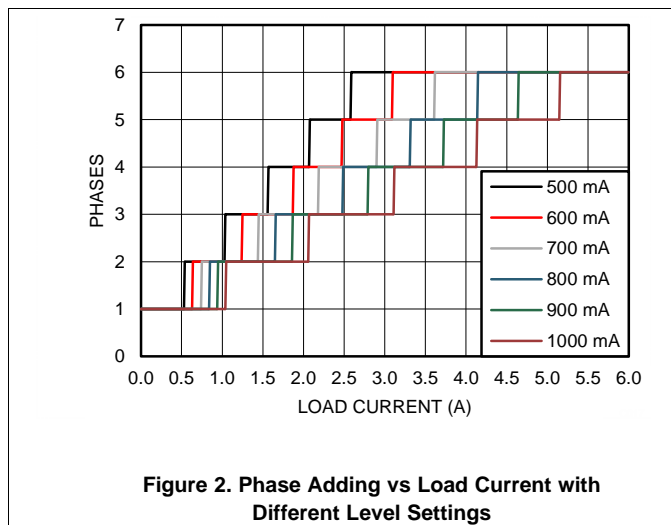


Figure 2. Phase Adding vs Load Current with Different Level Settings

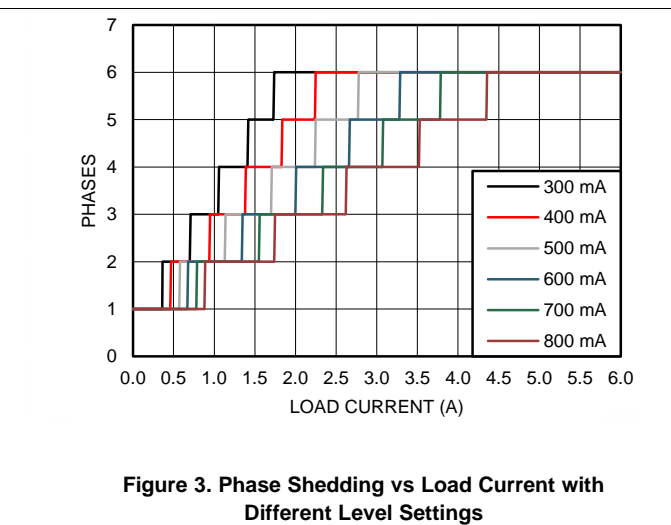


Figure 3. Phase Shedding vs Load Current with Different Level Settings

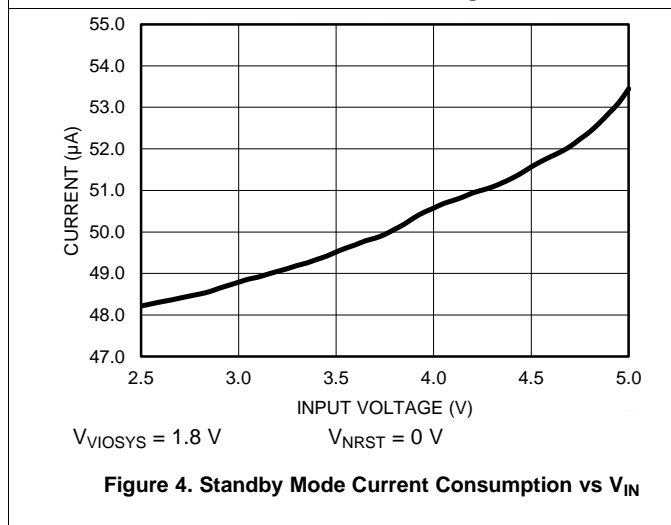


Figure 4. Standby Mode Current Consumption vs  $V_{IN}$

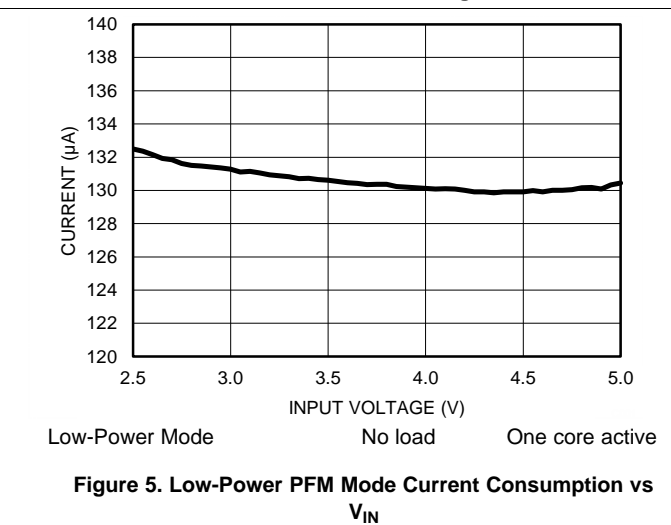
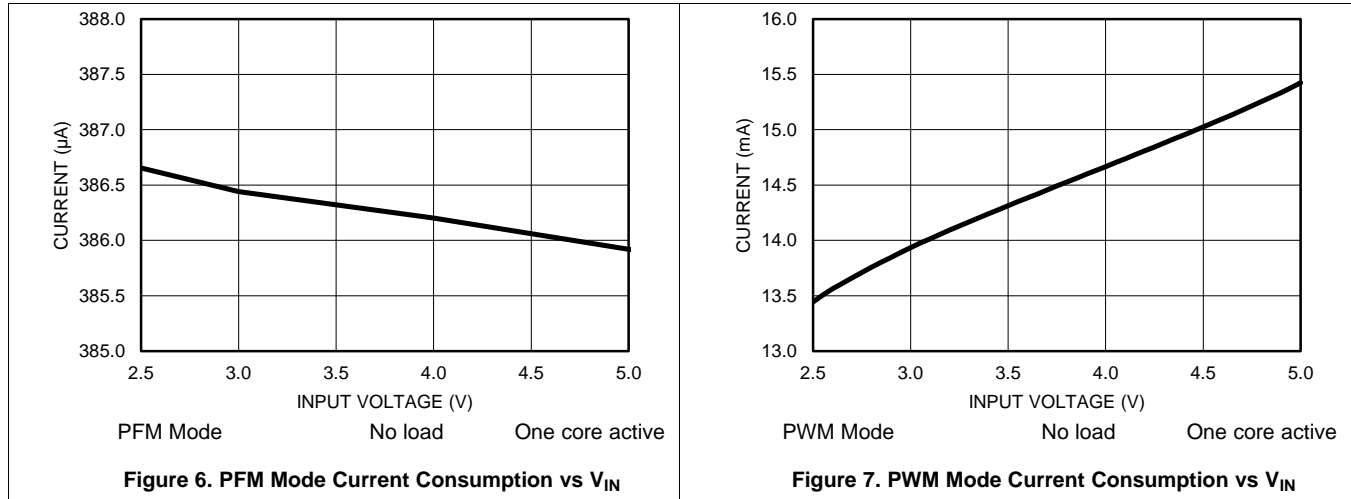


Figure 5. Low-Power PFM Mode Current Consumption vs  $V_{IN}$

**Typical Characteristics (continued)**

Unless otherwise specified:  $V_{VDDA5V} = V_{VINBXX} = 3.7\text{ V}$ ,  $V_{OUT} = 1.1\text{ V}$ ,  $T_A = 25^\circ\text{C}$



## 7 Detailed Description

### 7.1 Overview

The LP8754 is a high-efficiency, high-performance power supply IC with six step-down DC-DC converter cores. It delivers 0.6 V to 1.67 V regulated voltage rail from either a single Li-Ion or three cell NiMH/NiCd batteries to portable devices such as cell phones and PDAs.

There are three modes of operation for the 6-phase converter, depending on the output current required: PWM (Pulse Width Modulation), PFM (Pulse-Frequency Modulation), and Low-Power PFM. Converter operates in PWM mode at high load currents of approximately 250 mA or higher, depending on register setting. Lighter output current loads will cause the converter to automatically switch into PFM or Low-Power PFM mode for reduced current consumption and a longer battery life. Forced PWM is also available for highest transient performance.

Under no-load conditions the device can be set to Standby or Shutdown. Shutdown mode turns off the device, offering the lowest current consumption ( $I_{SHDN} = 0.1 \mu\text{A typ.}$ ). Additional features include soft-start, undervoltage lockout, input overvoltage protection, current overload protection, thermal warning, and thermal shutdown.

The modes and features can be programmed via control registers. All the registers can be accessed with both I<sup>2</sup>C serial interfaces: System serial interface and Dynamic voltage scaling (DVS) interface. Using DVS interface for dynamic voltage scaling prevents latencies if System serial interface is busy. Using DVS interface is optional; System serial interface can also be used for dynamic voltage scaling.

#### 7.1.1 Buck Information

The LP8754 has six integrated high-efficiency buck converter cores. The cores are designed for flexibility; most of the functions are programmable, thus allowing optimization of the SMPS operation for each application. The cores are bundled together to establish a multi-phase converter. This is shown in [Figure 24](#).

#### Operating Modes:

- OFF: Output is isolated from the input voltage rail in this mode. Output has an optional pulldown resistor which can be enabled with BUCK0\_CTRL.RDIS\_B0 bit.
- PWM: Converter operates in buck configuration. Average switching frequency is constant.
- PFM: Converter switches only when output voltage decreases below programmed threshold. Inductor current is discontinuous.
- Low-Power PFM: This mode is similar to PFM mode, but used with lower load conditions. In this mode some of the internal blocks are turned off between the PFM pulses. Load transient response is compromised due to the wake-up time.

#### Features:

- DVS support
- Automatic mode control based on the loading
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Power good flag with maskable interrupt
- Overvoltage comparator
- Phase control and spread spectrum techniques for reducing EMI
- Average output current sensing (for PFM/PWM entry/exit, phase adding/shedding, and load current reporting)
- Current balancing between the phases of the converter
- Differential voltage sensing
- Dynamic phase adding/shedding, each output being phase shifted

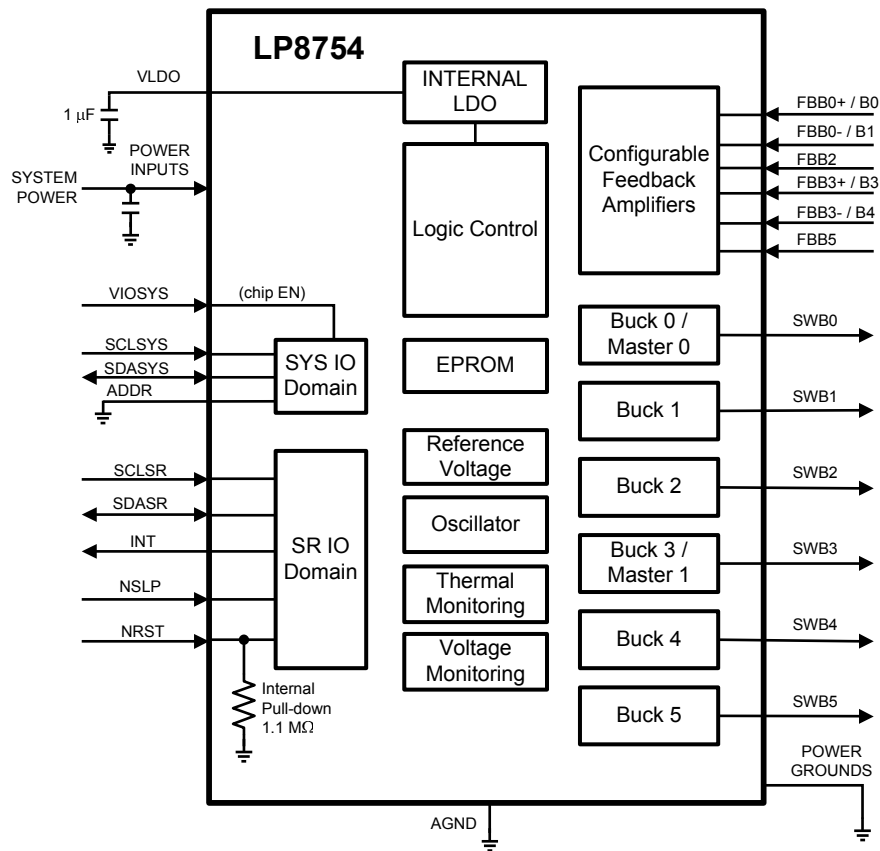


## Overview (continued)

### Programmability (The following parameters can be programmed via registers):

- Output voltage
- Forced PWM operation
- Switch current limits for high side FET
- PWM/PFM mode entry and exit (based on average output current)
- Phase adding and shedding levels
- Output voltage slew rate

## 7.2 Functional Block Diagram



## 7.3 Features Descriptions

### 7.3.1 Multi-Phase DC-DC Converters

A multi-phase synchronous buck converter offers several advantages over a single power-stage converter. For application processor power delivery, lower ripple on the input and output currents and faster transient response to load steps are the most significant advantages. Also, since the load current is evenly shared among multiple channels, the heat generated is greatly reduced for each channel due to the fact that power loss is proportional to square of current. Physical size of the output inductor shrinks significantly for the similar reason.

Features Descriptions (continued)

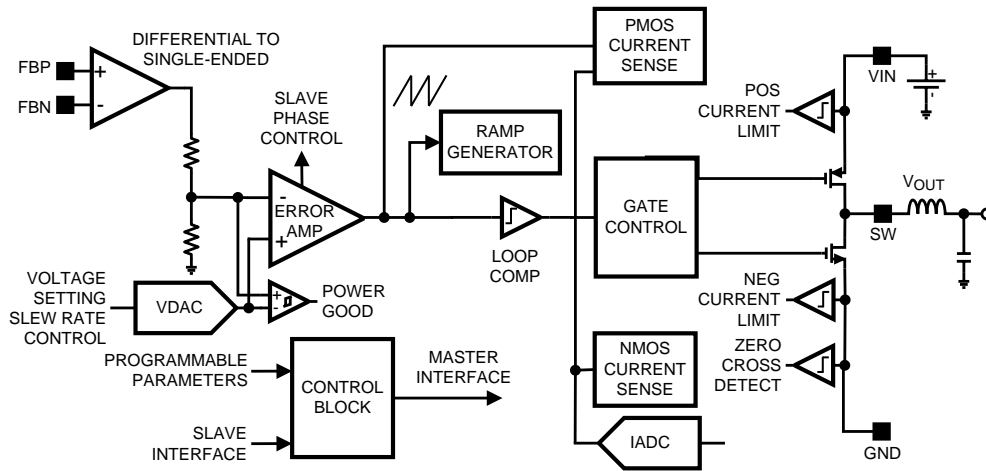


Figure 8. Detailed Block Diagram Showing One Buck Core

7.3.1.1 Multi-Phase Operation and Phase-Shedding

Under heavy load conditions, the switching phase of the bucks are interleaved. As a result, the 6-phase converter has higher effective switching frequency than the switching frequency of any one phase.

The parallel operation decreases the efficiency at low load conditions. In order to overcome this operational inefficiency, the LP8754 automatically changes the number of active phases to maximize the efficiency. This is called phase-shedding and the concept is illustrated in Figure 9.

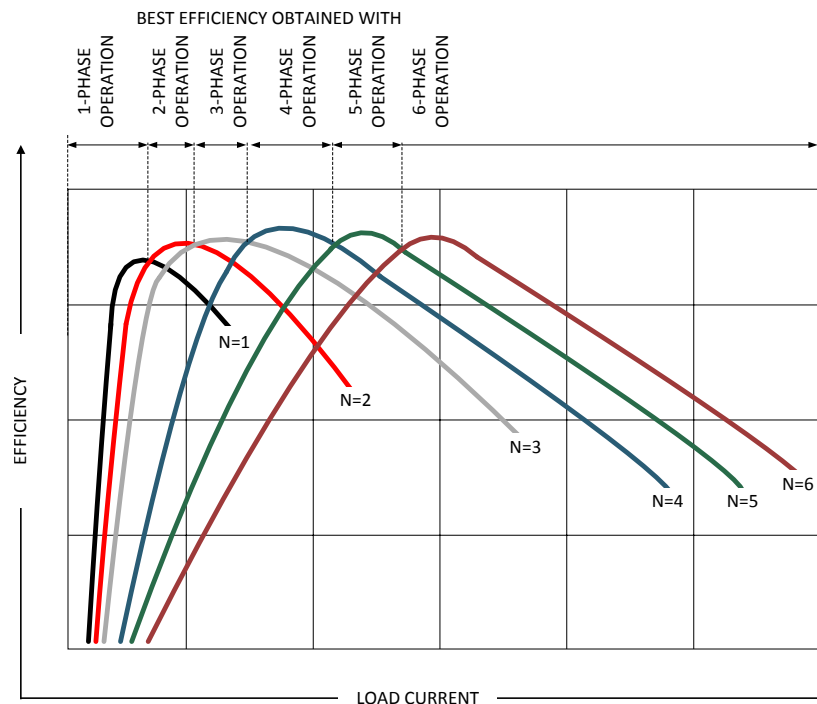


Figure 9. Multi-phase Buck Converter Efficiency vs Number of Phases; All Converters in PWM Mode <sup>(1)</sup>

(1) Graph is not to scale and is for illustrative purposes only.

## Features Descriptions (continued)

### 7.3.1.2 Transitions Between Low-Power PFM, PFM, and PWM Modes

Normal PWM-mode operation with phase-shedding can optimize efficiency at mid-to-full load, but this is usually at the expense of light-load efficiency. The LP8754 converter operates in PWM mode at a load current of 100 to 375 mA or higher; this mode transition trip-point is set by register. Lighter load current causes the device to automatically switch into PFM mode for reduced current consumption. By combining PFM and PWM modes in the same regulator and providing automatic switching, high efficiency can be achieved over a wide output load current range.

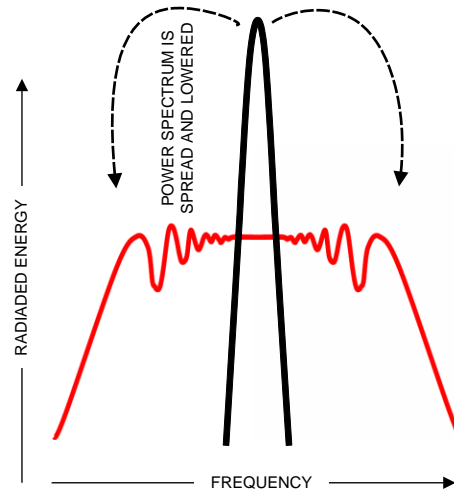
Efficiency is further enhanced when the converter enters Low-Power PFM mode. The LP8754 includes Low-Power mode function for low-current consumption. In this mode most of the internal blocks are disabled between the inductor current ramp up and ramp down phases to reduce the operating current. However, as a result, the transient performance of the converter is compromised. The Low-Power mode can be enabled by control register setting. Also, the application processor or the PMIC may provide an HW signal (NSLP) to the LP8754 input to indicate when the processor has entered a low-power state. When the signal is asserted, the LP8754 Low-Power PFM function will be enabled, and the LP8754 will run with a reduced input current. The right timing of the NSLP signal from the system is important for best load-transient performance. The NSLP signal should be asserted only when load current is stable and below 30 mA. Before the load current increases above 30 mA, the NSLP signal should be de-asserted 100  $\mu$ s (minimum) prior to a load step to prepare the converter for the higher load current.

### 7.3.1.3 Buck Converter Load Current

The buck load current can be monitored via I<sup>2</sup>C registers. Current of different buck converter cores or the total load current of the master can be selected from register 0x21 (see [SEL\\_I\\_LOAD](#)). A write to this selection register starts a current measurement sequence. The measurement sequence is a minimum of 50  $\mu$ s long. When a measurement sequence starts, the `FLAGS_1.I_LOAD_READY` bit in register 0x0E is set to '0'. After the measurement sequence is finished, the `FLAGS_1.I_LOAD_READY` bit is set to '1'. (Note that by default this bit is '0'.) The measurement result can be read from registers 0x22 (`LOAD_CURR.BUCK_LOAD_CURR[7:0]`) and 0x21 (`SEL_I_LOAD.BUCK_LOAD_CURR[10:8]`). The measurement result [10:0] LSB is 10 mA, and the maximum value of the measurement is 20 A. The LP8754 can be configured to give out an interrupt after the load current measurement sequence is finished. Load current measurement interrupt can be masked with `INT_MASKS_2.MASK_I_LOAD_READY` bit.

### 7.3.1.4 Spread Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The LP8754's register-selectable spread spectrum mode minimizes the need for output filters, ferrite beads, or chokes. In spread spectrum mode, the switching frequency varies randomly around the center frequency, reducing the EMI emissions radiated by the converter, associated passive components, and PCB traces. See [Figure 10](#).

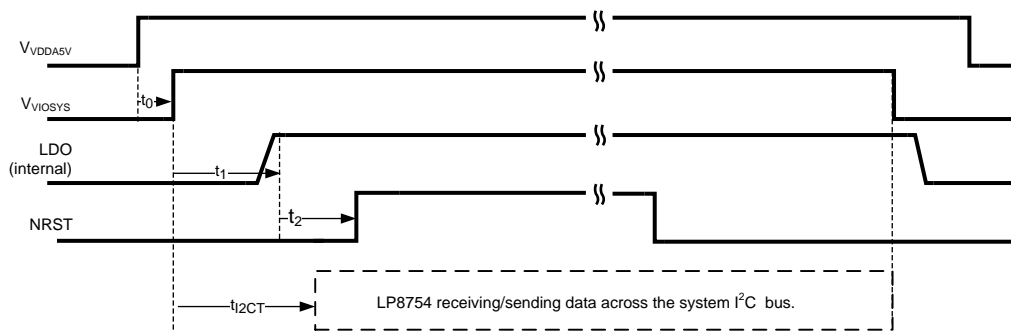
**Features Descriptions (continued)**


Where a fixed-frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the LP8754 spreads that energy over a large bandwidth.

**Figure 10. Spread Spectrum Modulation**
**7.3.2 Power-Up and Output Voltage Sequencing**

The power-up sequence for the LP8754 is as follows:

- $V_{VINBXX}$  and  $V_{VDDA5V}$  reach min recommended levels.
- $V_{VIOSYS}$  set high. Enables the system I/O interface. For power-on-reset (POR), the I<sup>2</sup>C host should allow at least 500  $\mu$ s before sending data to the LP8754 after the rising edge of the VIOSYS line.
- $V_{LDO}$  voltage is raising. The LDO voltage is generated internally. The internal POR signal is activated.
- Internal POR deasserted, OTP read.
- Device enters standby mode.
- DC-DC enable, output voltage, voltage slew rate programmed over I<sup>2</sup>C as needed by the application.
- NRST set high. The DC-DC converter can be enabled and disabled by VSET\_B0.EN\_DIS\_B0 bit or using the NRST signal.


**Figure 11. Timing Diagram for the Power-Up Sequence**

Features Descriptions (continued)

Table 1. Power-Up Sequence

PARAMETER	CONDITION <sup>(1)</sup>	MIN	TYP	MAX	UNIT
t <sub>0</sub>	V <sub>VDDA5V</sub> to V <sub>VIOSYS</sub> assertion	0			μs
t <sub>1</sub>	LDO <sub>ON</sub> Delay Time		<100	150	μs
t <sub>2</sub>	LDO <sub>ON</sub> to NRST HIGH	0			μs
t <sub>2CT</sub>	Device ready for I <sup>2</sup> C data transfer	500			μs

(1) These specification table entries are specified by design. The power input lines V<sub>VINBXX</sub>, V<sub>VDDA5V</sub> and V<sub>VIOSYS</sub> must be stable before the NRST line goes High. Also, the V<sub>LDO</sub> line must be stable 1.8 V before the NRST line goes High.

7.3.3 Device Reset Scenarios

There are three reset methods implemented on the LP8754:

- Software reset
- Hardware reset
- Power-on reset (POR)

An SW-reset occurs when the RESET.SW\_RESET bit is written first with 1, followed by 0 right after that. This event resets the control registers shown in Table 2 to the default values. The temperature, power good, and other faults are persistent over the SW reset to allow for the system to identify to cause of the failure.

An internal power-on reset (POR) occurs when the supply voltage (V<sub>VDDA5V</sub>) transitions above the POR threshold or V<sub>VIOSYS</sub> is toggled low/high. Each of the registers contain a factory-defined value upon POR, and this data remains there until any of the following occurs:

- Device sets a Flag bit, causing the Status register to be updated. The other registers remain untouched.
- A different data word is written to a writable register.

The internal registers will lose their contents if the supply voltage (V<sub>VDDA5V</sub>) goes below 1 V (typ.).

An NRST high-to-low transition initiates the hardware reset. This event resets the control registers shown in Table 2 to the default values.

Under OVP, UVLO, TSD, or V<sub>VIOSYS</sub> low (while NRST still high) conditions, a Fast Power-Down is launched.

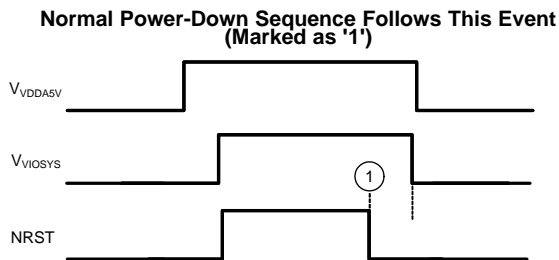


Figure 12. The External Power Control System De-asserts NRST

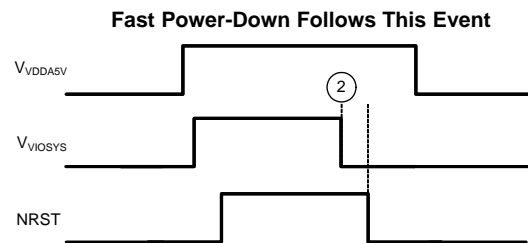


Figure 13. NRST Stays HIGH While V<sub>VIOSYS</sub> Transition from HIGH to LOW Happens (Marked as '2')

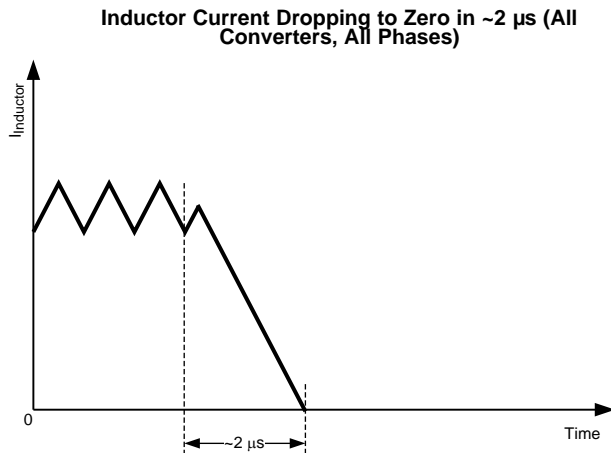


Figure 14. Fast Power-Down

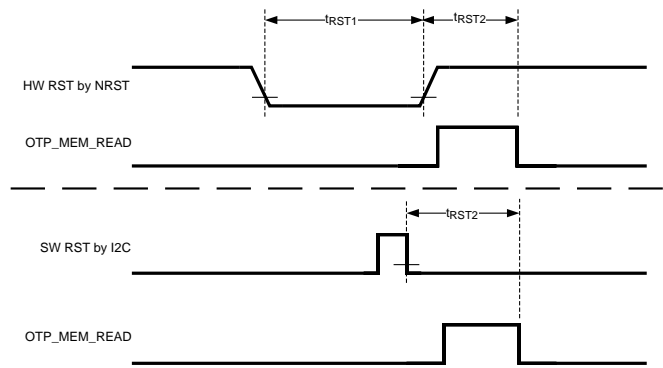


Figure 15. Reset Timings

PARAMETER		LIMIT
$t_{RST1}$	NRST active low pulse width	1 $\mu$ s min + value on DELAY_BUCK0 register.
$t_{RST2}$	NRST inactive or I <sup>2</sup> C reset event to MEMORY READ end	25 $\mu$ s max

Table 2. Hardware Reset, Power-On Reset (POR) and Software Reset: Registers After Reset

HEX ADDRESS	REGISTER	SOFTWARE RESET I <sup>2</sup> C RESET	HARDWARE RESET NRST LOW <sup>(1)</sup>	POWER-ON RESET V <sub>Viosys</sub> LOW
0x00	VSET_B0	All bits retained	All bits retained	All bits cleared
0x06	FPWM	All bits cleared	All bits cleared	All bits cleared
0x07 to 0x0C	BUCK0_CTRL to BUCK5_CTRL	All bits cleared	All bits cleared	All bits cleared
0x0D	FLAGS_0	All bits retained	All bits retained	All bits cleared
0x0E	FLAGS_1	All bits retained	All bits retained	All bits cleared
0x0F	INT_MASK0	All bits cleared	All bits cleared	All bits cleared
0x10	GENERAL	All bits cleared	All bits cleared	All bits cleared
0x11	RESET	N/A	All bits cleared	All bits cleared
0x12	DELAY_BUCK0	All bits cleared	All bits cleared	All bits cleared
0x18	CHIP_ID	Read Only		
0x19	PFM_LEV_B0	All bits cleared	All bits cleared	All bits cleared
0x1F	PHASE_LEV_B0	All bits cleared	All bits cleared	All bits cleared
0x21	SEL_I_LOAD	All bits retained	All bits retained	All bits cleared
0x22	LOAD_CURR	Read Only		
0x2E	INT_MASK_2	All bits cleared	All bits cleared	All bits cleared

(1) Reset is falling-edge sensitive and it will take effect upon complete of the power-down sequence. The registers can be updated by I2C writing when NRST is low.

### 7.3.4 Diagnosis and Protection Features

The LP8754 is capable of providing two levels of protection features: warnings for diagnosis and faults which are causing the converters to shut down. When the device detects warning or fault conditions, the LP8754 sets the flag bits indicating which fault or warning conditions have occurred; the INT pin will be pulled low. INT will be released again after a clear of flags is complete. The flag bits are persistent over reset to allow for the system to identify what was causing the interrupt and/or converter shutdown.

Also, the LP8754 has a soft-start circuit that limits in-rush current during start-up. The output voltage increase rate is 30 mV/μs (default) during soft-start.

**Table 3. Summary of Exceptions and Interrupt Signals**

EVENT	REGISTER.BIT	INTERRUPT SIGNAL PRODUCED?	INT MASK AVAILABLE?
SCP triggered	FLAGS_1.SCP	Yes	Yes
Not PowerGood	FLAGS_0.nPG_B0	Yes	Yes
TEMP status change	FLAGS_0.TEMP[1:0]	On any temperature change except for the case when TEMP[1:0] = 0b11	Yes
Thermal warning	FLAGS_1.T_WARNING	Yes	Yes
Thermal shutdown	FLAGS_1.THSD	Yes	No
OVP triggered	FLAGS_1.OVP	Yes	Yes
Load current measurement ready	FLAGS_1.I_LOAD_READY	Yes	Yes
UVLO triggered	FLAGS_1.UVLO	Yes	Yes

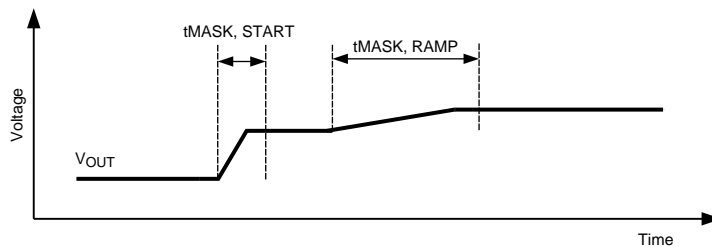
#### 7.3.4.1 Warnings for Diagnosis (No Power Down)

##### 7.3.4.1.1 Short-Circuit Protection (SCP)

A short-circuit protection feature allows the LP8754 to protect itself and external components during overload conditions. The output short-circuit fault threshold is 400 mV (typ.) .

##### 7.3.4.1.2 Power Good Monitoring

When the converter's feedback-pin voltage falls lower than 90% (typ.) of the set voltage, the FLAGS\_0.nPG\_B0 flag is set. To prevent a false alarm, the power good circuit is masked during converter start-up and voltage transitions. The duration of the power good mask is set to 400 μs for converter start-up. For voltage ramps the masking time is extended by an internal logic circuit up to 6.4 ms. (See [Protection Features Characteristics](#).)



Masking time for start-up is constant 400 μs (typ.). Masking time for voltage transitions depends on the selected ramp rates.

**Figure 16. Power Good Masking Principle**

##### 7.3.4.1.3 Thermal Warnings

Prior to the thermal shutdown, thermal warnings are set. The first warning is set at 85°C (INT pin low), and the second at 120°C (INT pin pulled low and FLAGS\_1.T\_WARNING flag set). If the chip temperature crosses any of the thresholds of 85°C, 120°C, or 150°C (see [FLAGS\\_0](#) register) the INT pin will be triggered. INT will be cleared upon read of FLAGS\_0.TEMP[1:0] bits except if FLAGS\_0.TEMP [1:0] = 0b11, which is a thermal fault event.

### 7.3.4.2 Faults (Fault State and Fast Power Down)

#### 7.3.4.2.1 Undervoltage Lockout (UVLO)

When the input voltage falls below  $V_{UVLO}$  (typ. 2.25 V) at the VDDA5V pin, the LP8754 indicates a fault by activating the FLAGS\_1.UVLO flag. The buck converter shut down without a power-down sequence (Fast Power-Down). The flag will remain active until the input voltage is raised above the UVLO threshold. If the flag is cleared while the fault persists, the flag is immediately re-asserted, and interrupt remains active.

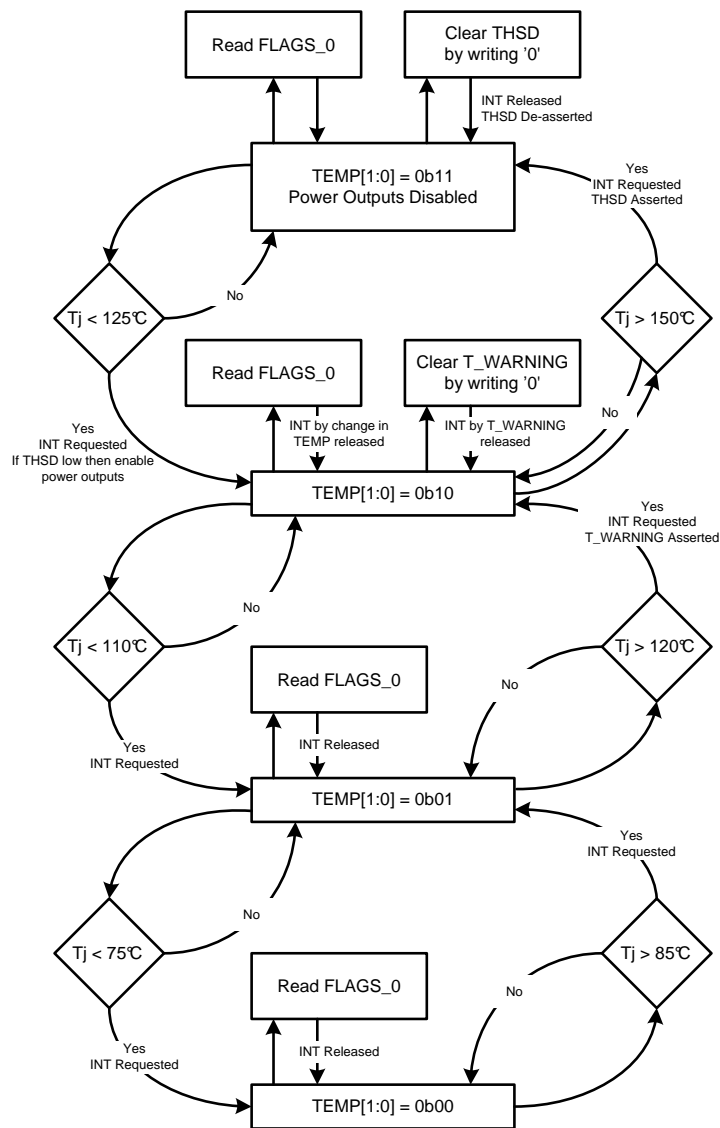
#### 7.3.4.2.2 Overvoltage Protection (OVP)

When an input voltage greater than  $V_{OVP}$  (typ. 5.3 V) is detected at the VDDA5V pin, the LP8754 indicates a fault by activating the FLAGS\_1.OVP flag. The buck converter is shut down immediately (Fast Power-Down). The flag will remain active until the input voltage is below the OVP threshold. If the flag is cleared while the fault persists, the flag is immediately re-asserted and interrupt remains active.

#### 7.3.4.2.3 Thermal Shutdown (THSD)

The LP8754 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device enters shutdown via fault-state. INT will be cleared upon write of the FLAGS\_1.THSD flag even when thermal shutdown is active. This allows automatic recovery when temperature decreases below thermal shutdown level. See [Figure 17](#) for LP8754 thermal diagnosis and protection features.





Note that INT is asserted whenever any of the thermal thresholds is crossed, if unmasked. Note also the 10°C Hysteresis on the  $T_J$  Thresholds.

Figure 17. Thermal Warnings and Thermal Shutdown Flow

## 7.4 Device Functional Modes

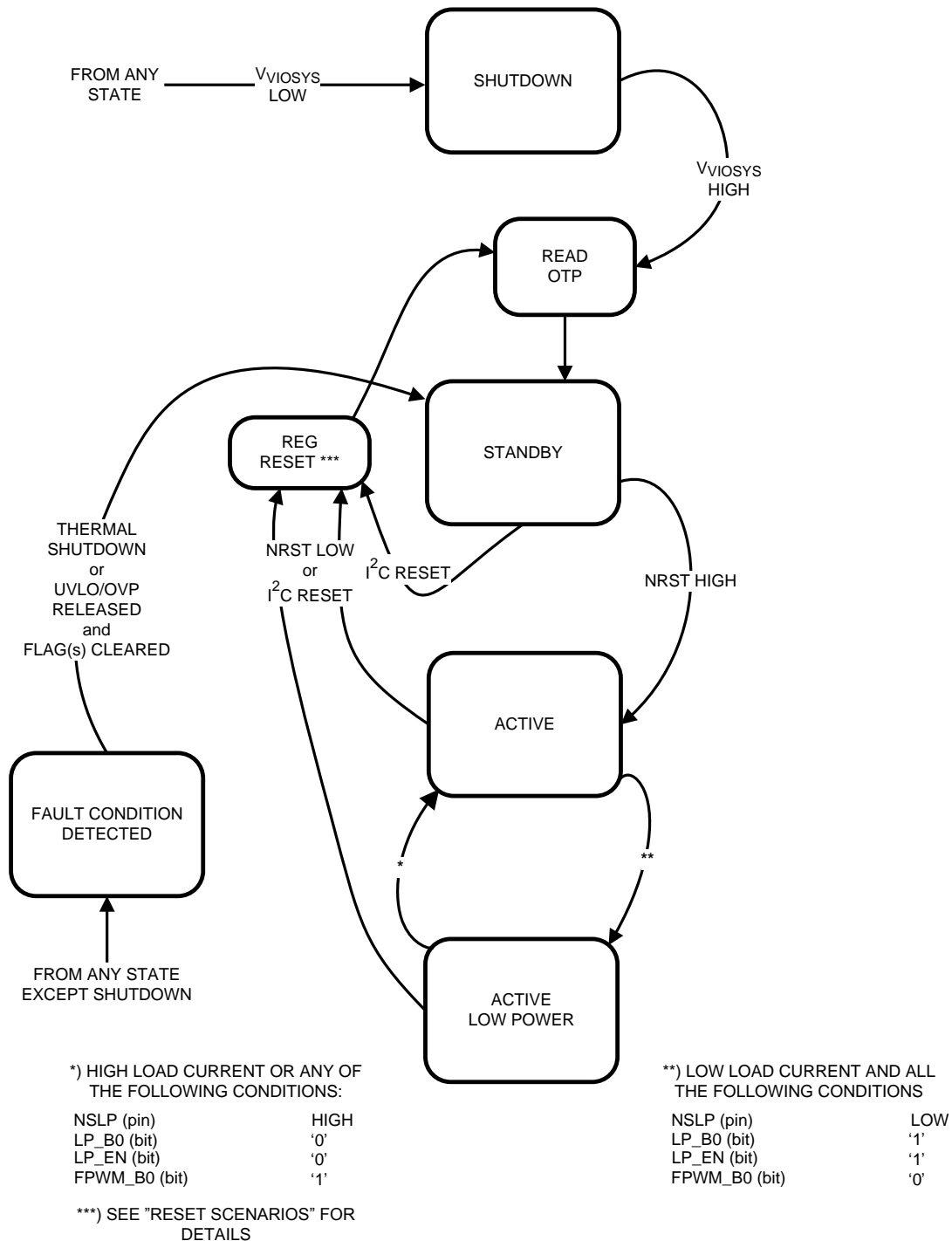
**SHUTDOWN:** All switch, reference, control and bias circuitry of the LP8754 are turned off. The main battery supply voltage is high enough to start the buck power-up sequence but  $V_{VIOSYS}$  and NRST are LOW.

**STANDBY:** Setting  $V_{VIOSYS}$  HIGH enables standby-operation. All registers can be read or written by the system master via the system serial interface. Recovery from UVLO, TSD, or OVP event also leads to standby.

**ACTIVE:** Regulated DC-DC converters are on or can be enabled with full current capability. In this mode, all features and control registers are available via the system serial bus and via DVS interface.

**LOW-POWER:** At light loads (less than approximately 30 mA), and when the load does not require highest level of transient performance, the device enters automatically Low-Power mode. In this mode the part operates at low  $I_Q$ . Conditions entering and exiting Low-Power mode are shown in Figure 18.

**Device Functional Modes (continued)**



**Figure 18. Device Operation Modes**

## 7.5 Programming

### 7.5.1 I<sup>2</sup>C-Compatible Interface

The I<sup>2</sup>C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines should each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle. Note: CLK pin is not used for serial bus data transfer. There are two buses implemented: the System I<sup>2</sup>C bus and the DVS bus. In the following paragraphs, SCL refers to both SCLSYS and SCLSR, and SDA refers to SDASYS and SDASR. The LP8754 supports standard mode (100 kHz), fast mode (400 kHz) and high-speed mode (3.4 MHz).

#### 7.5.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW.

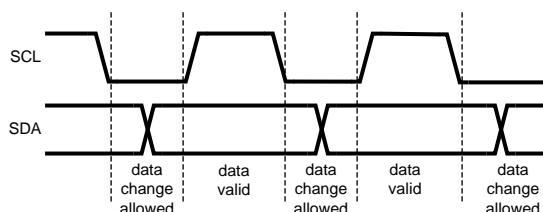


Figure 19. Data Validity Diagram

#### 7.5.1.2 Start and Stop Conditions

The LP8754 is controlled via an I<sup>2</sup>C-compatible interface. START and STOP conditions classify the beginning and end of the I<sup>2</sup>C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates the START and STOP conditions.

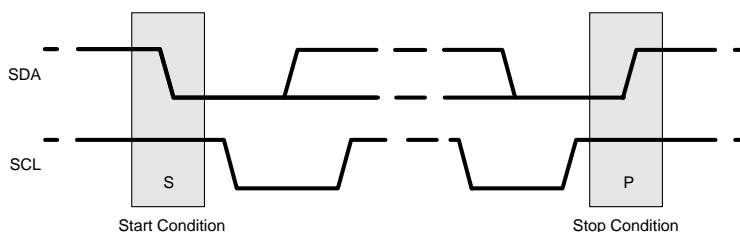


Figure 20. Start and Stop Sequences

The I<sup>2</sup>C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I<sup>2</sup>C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. Figure 1 shows the SDA and SCL signal timing for the I<sup>2</sup>C-Compatible Bus. See the [I<sup>2</sup>C Serial Bus Timing Parameters](#) for timing values.

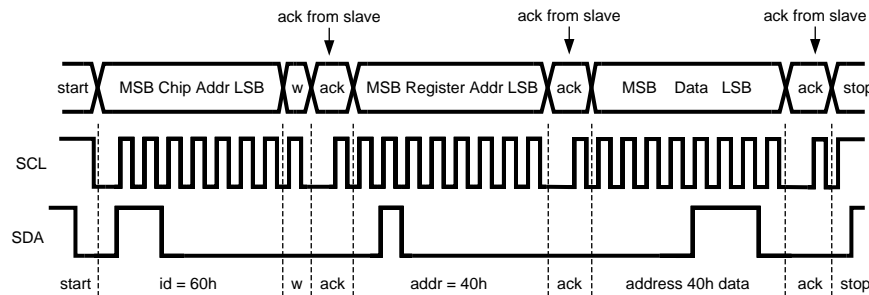
#### 7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP8754 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP8754 generates an acknowledge after each byte has been received.

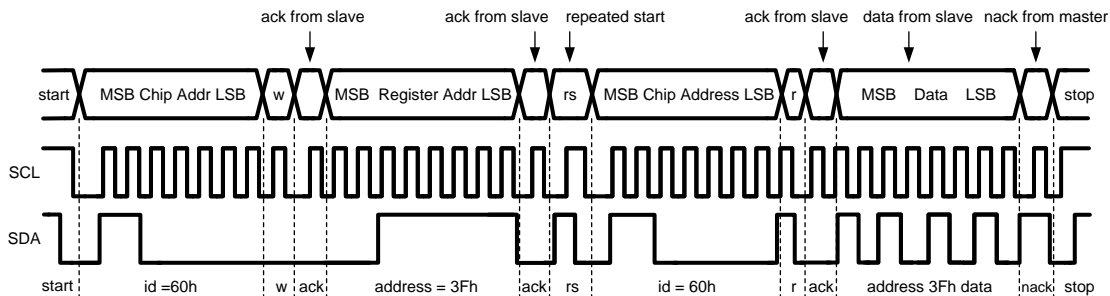
**Programming (continued)**

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.



**Figure 21. Write Cycle (w = write; SDA = '0'), id = device address = 60Hex for LP8754.**

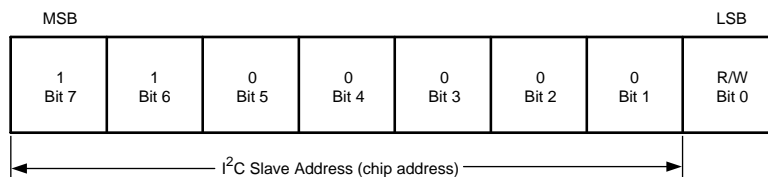


When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

**Figure 22. Read Cycle (r = read; SDA = '1'), id = device address = 60Hex for LP8754.**

**7.5.1.4 I<sup>2</sup>C-Compatible Chip Address**

The device address for the LP8754 is 0x60 (ADDR pin tied to the GND). After the START condition, the I<sup>2</sup>C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.



Here device address is 1100000Bin = 60 Hex.

**Figure 23. Device Address**

## Programming (continued)

### 7.5.1.5 Auto-Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the LP8754, the internal address index counter will be incremented by one, and the next register will be written. [Table 4](#) shows writing sequence to two consecutive registers. Note: the auto-increment feature does not work for read.

**Table 4. Auto-Increment Example**

Master Action	Start	Device Address = 60H	Write		Register Address		Data		Data		Stop
LP8754 Action				ACK		ACK		ACK		ACK	

## 7.6 Register Maps

### 7.6.1 Register Descriptions

The LP8754 is controlled by a set of registers through the system serial interface port or through the Dynamic Voltage Scaling interface. [Table 5](#) lists device registers, their addresses and their abbreviations. A more detailed description is given in the sections [VSET\\_B0](#) to [INT\\_MASK\\_2](#).

Many registers contain bits, that are reserved for future use. When writing to a register, any reserved bits should not be changed.

**Table 5. Register Descriptions**

Addr	Register	Read / Write	D7	D6	D5	D4	D3	D2	D1	D0	
0x00	VSET_B0	R/W	EN_DIS_B0	VSET_B0[6:0]							
0x06	FPWM	R/W	Reserved								FPWM_B0
0x07	BUCK0_CTRL	R/W	OC_LEV_B0[1:0]	LP_B0	RDIS_B0	Reserved	RAMP_B0[2:0]				
0x08	BUCK1_CTRL	R/W	OC_LEV_B1[1:0]	Reserved							
0x09	BUCK2_CTRL	R/W	OC_LEV_B2[1:0]	Reserved							
0x0A	BUCK3_CTRL	R/W	OC_LEV_B3[1:0]	Reserved							
0x0B	BUCK4_CTRL	R/W	OC_LEV_B4[1:0]	Reserved							
0x0C	BUCK5_CTRL	R/W	OC_LEV_B5[1:0]	Reserved							
0x0D	FLAGS_0	R/W	Reserved					nPG_B0	TEMP[1:0]		
0x0E	FLAGS_1	R/W	Reserved	I_LOAD_READY	UVLO	T_WARNIN_G	THSD	OVP	SCP		
0x0F	INT_MASK_0	R/W	Reserved					MASK_nPG_B0	MASK_OVP	MASK_SCP	
0x10	GENERAL	R/W	Reserved	EN_SS	Reserved	DIS_DIF_B0	Reserved	SLP_POL	LP_EN		
0x11	RESET	R/W	Reserved								SW_RESET
0x12	DELAY_BUCK0	R/W	DELAY_B0[7:0]								
0x18	CHIP_ID	R	DEVICE	OTP_REV[4:0]					DIE_REV[1:0]		
0x19	PFM_LEV_B0	R/W	Reserved	PFM_ENTRY_B0[2:0]			Reserved	PFM_EXIT_B0[2:0]			
0x1F	PHASE_LEV_B0	R/W	Reserved	ADD_PH_B0[2:0]			Reserved	SHED_PH_B0[2:0]			
0x21	SEL_I_LOAD	R/W	Reserved	BUCK_LOAD_CURR[10:8]			Reserved	LOAD_CURRENT_SOURCE[2:0]			
0x22	LOAD_CURR	R	BUCK_LOAD_CURR[7:0]								
0x2E	INT_MASK_2	R/W	Reserved				MASK_ILOAD_READY	MASK_UVLO	MASK_TWARINING	MASK_TEMP	

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**7.6.2 VSET\_B0**

Address: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
EN_DIS_B0		VSET_B0[6:0]					
Bits	Field	Type	Default	Description			
7	EN_DIS_B0	R/W	1	DC-DC converter Buck0 Enable/Disable. The Enable of the master Buck0 controls the operation of the slave bucks. 0 = Converter disabled 1 = Converter enabled Note: When a disable request is received the converter is disabled immediately.			
6:0	VSET_B0[6:0]	R/W	011 1100	Sets the output voltage. Defined by: $V_{OUT} = 0.5 V + 10 mV * VSET\_B0$ $V_{OUT}$ range = 0.6 V to 1.67 V NOTE: Do not use VSET_B0 values < 0001010 (10 dec) = 0.6 V. NOTE: Register settings starting from 1110110 up to 1111111 are clamped to 1.67 V.			

**7.6.3 FPWM**

Address: 0x06

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							FPWM_B0
Bits	Field	Type	Default	Description			
7:1	Reserved	R/W	001 1111				
0	FPWM_B0	R/W	1	Forced PWM mode of operation, Buck regulator 0 (Master). The setting of the master controls the operation of the slave bucks. 0 = PWM, PFM or Low-Power PFM operation mode. 1 = This will force the master converter and the slaves to operate always in the PWM mode.			

**7.6.4 BUCK0\_CTRL**

Address: 0x07

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B0[1:0]		LP_B0	RDIS_B0	Reserved	RAMP_B0[2:0]		
Bits	Field	Type	Default	Description			
7:6	OC_LEV_B0[1:0]	R/W	10	Inductor positive current limit on Buck 0. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A			
5	LP_B0	R/W	0	Allows converter to enter into Low-Power PFM mode. 1 = Entering to Low-Power PFM mode is allowed. 0 = Entering to Low-Power PFM mode is not allowed.			
4	RDIS_B0	R/W	1	Enables the output discharge resistors when the $V_{OUT}$ supply has been disabled. 1 = Enable pull-down 0 = Disable pull-down			
3	Reserved	R/W	0				

Bits	Field	Type	Default	Description
2:0	RAMP_B0[2:0]	R/W	001	This set the output voltage change ramp as follows: 000 = 30 mV/μs 001 = 15 mV/μs 010 = 7.5 mV/μs 011 = 3.8 mV/μs 100 = 1.9 mV/μs 101 = 0.94 mV/μs 110 = 0.47 mV/μs 111 = 0.23 mV/μs

### 7.6.5 BUCK1\_CTRL

Address: 0x08

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B1[1:0]		Reserved					

Bits	Field	Type	Default	Description
7:6	OC_LEV_B1[1:0]	R/W	10	Inductor positive current limit on Buck 1. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A
5:0	Reserved	R/W	01 0001	

### 7.6.6 BUCK2\_CTRL

Address: 0x09

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B2[1:0]		Reserved					

Bits	Field	Type	Default	Description
7:6	OC_LEV_B2[1:0]	R/W	10	Inductor positive current limit on Buck 2. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A
5:0	Reserved	R/W	01 0001	

### 7.6.7 BUCK3\_CTRL

Address: 0x0A

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B3[1:0]		Reserved					

Bits	Field	Type	Default	Description
7:6	OC_LEV_B3[1:0]	R/W	10	Inductor positive current limit on Buck 3. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A
5:0	Reserved	R/W	01 0001	

**LP8754**

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**7.6.8 BUCK4\_CTRL**

Address: 0x0B

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B4[1:0]		Reserved					
Bits	Field	Type	Default	Description			
7:6	OC_LEV_B4[1:0]	R/W	10	Inductor positive current limit on Buck 4. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A			
5:0	Reserved	R/W	01 0001				

**7.6.9 BUCK5\_CTRL**

Address: 0x0C

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B5[1:0]		Reserved					
Bits	Field	Type	Default	Description			
7:6	OC_LEV_B5[1:0]	R/W	10	Inductor positive current limit on Buck 5. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A			
5:0	Reserved	R/W	01 0001				

**7.6.10 FLAGS\_0**

Address: 0x0D

D7	D6	D5	D4	D3	D2	D1	D0
Reserved					nPG_B0	TEMP[1:0]	
Bits	Field	Type	Default	Description			
7:3	Reserved	R/W	X XXXX				
2	nPG_B0	R/W	0	Flag Bit <sup>(1)</sup> Power good fault flag for V <sub>OUT</sub> rail 1 = Power fault detected 0 = Power good			
1:0	TEMP[1:0]	R	00	indicates the die temperature as follows: 00: die temperature lower than 85°C 01: 85°C ≤ die temperature < 120°C 10: 120°C ≤ die temperature < 150°C 11: die temperature 150°C or higher			

(1) The flag bit can be cleared only by writing a zero to the associated register bit or power cycling the device (V<sub>VIOSYS</sub> to LOW). Reading or RESET does not clear the flag bits. After clearing, the nPG\_B0 fault flag will be raised again '1' if the fault condition persists. Any unmasked flag bit High will cause the interrupt to be asserted on the INT pin. The INT pin will be pulled Low until all the unmasked flags are clear again.

**7.6.11 FLAGS\_1**

Address: 0x0E



D7	D6	D5	D4	D3	D2	D1	D0
Reserved		I_LOAD_READ_Y	UVLO	T_WARNING	THSD	OVP	SCP

Bits	Field	Type	Default	Description
7:6	Reserved	R/W	00	
5	I_LOAD_READY	R/W	0	Flag Bit <sup>(1)</sup> 1 = Buck load current measurement data ready 0 = Buck load current measurement data not ready
4	UVLO	R/W	0	Flag Bit <sup>(1)</sup> 1= Input undervoltage lockout (UVLO): Input voltage sagged below UVLO threshold. 0 = No UVLO
3	T_WARNING	R/W	0	Flag Bit <sup>(1)</sup> 1= Thermal warning: The IC temperature exceeds 120°C, in advance of the thermal shutdown protection. 0 = No thermal warning
2	THSD	R/W	0	Flag Bit <sup>(1)</sup> 1 = Thermal shutdown event detected 0 = No thermal shutdown
1	OVP	R/W	0	Flag Bit <sup>(1)</sup> 1= Indicates overvoltage protection (OVP) circuit activation. 0 = No OVP event. The OVP circuitry monitors VDDA5V power input.
0	SCP	R/W	0	Flag Bit <sup>(1)</sup> 1= Indicates short-circuit protection (SCP) circuit activation. The bit is activated when a short-circuit condition is detected on output rail. 0 = No SCP event

- (1) The flag bit(s) can be cleared only by writing a zero to the associated register bit(s) or power cycling the device (V<sub>VIOSYS</sub> to LOW). Reading or RESET does not clear the flag bits. After clearing, the OVP, SCP fault flag(s) will be raised again '1' if the fault condition persists. The THSD flag will remain '0' after clear, even though the fault condition persists. Any unmasked flag bit High will cause the interrupt to be asserted on the INT pin. The INT pin will be pulled Low until all the unmasked flags are clear again.

### 7.6.12 INT\_MASK\_0

Address: 0x0F

D7	D6	D5	D4	D3	D2	D1	D0
Reserved					MASK_nPG_B_0	MASK_OVP	MASK_SCP

Bits	Field	Type	Default	Description
7:3	Reserved	R/W	1 1111	
2	MASK_nPG_B0	R/W	0	Interrupt mask for power good fault flag 1 = nPG_B0 does not set interrupt. 0 = nPG_B0 sets interrupt, when triggered.
1	MASK_OVP	R/W	0	Interrupt mask for Overvoltage Protection (OVP) fault flag 1 = OVP does not set interrupt. 0 = OVP sets interrupt, when triggered.
0	MASK_SCP	R/W	0	Interrupt mask for short-circuit protection SCP fault flag 1 = SCP does not set interrupt. 0 = SCP sets interrupt, when triggered.

### 7.6.13 GENERAL

Address: 0x10

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		EN_SS	Reserved	DIS_DIF_B0	Reserved	SLP_POL	LP_EN

Bits	Field	Type	Default	Description
7:6	Reserved	R/W	00	
5	EN_SS	R/W	0	Spread Spectrum 1 = Spread Spectrum enabled 0 = Spread Spectrum disabled
4	Reserved	R/W	0	
3	DIS_DIF_B0	R/W	0	Disable Differential-to-single-ended amplifier 1 = Differential amplifier disabled 0 = Differential amplifier enabled
2	Reserved	R/W	0	
1	SLP_POL	R/W	0	Sets the polarity of the NSLP pin 1 = NSLP is active high 0 = NSLP is active low
0	LP_EN	R/W	1	1 = allows Low-Power PFM mode. In order to reduce power consumption under low load conditions, the unit will automatically switch off unused internal blocks. 0 = Low-Power mode not allowed

### 7.6.14 RESET

Address: 0x11

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							SW_RESET

Bits	Field	Type	Default	Description
7:1	Reserved	R/W	000 0000	
0	SW_RESET	R/W	0	Writing this bit with '1' and '0', in this order, will reset the registers to the default values. If NRST is still kept HIGH, the converter output(s) will be regulated to the programmed register values. If a full POR reset is required V <sub>VIOSYS</sub> must be pulled low. The fault flags are persistent over SW-reset.

### 7.6.15 DELAY\_BUCK0

Address: 0x12

D7	D6	D5	D4	D3	D2	D1	D0
DELAY_B0							

Bits	Field	Type	Default	Description
7:0	DELAY_B0	R/W	0000 0000	Master delay Sets the delay time from when NRST is asserted to when the V <sub>OUT</sub> rail is enabled. Sets the delay time from when NRST is de-asserted to when the V <sub>OUT</sub> rail is disabled. DELAY = DELAY_B0 * 100 μs If DELAY_B0 = FFh, supply is never enabled. <sup>(1)</sup>

(1) If this register is set to FFh when the converter is already started, it will cause an immediate power down of the converter.

### 7.6.16 CHIP\_ID

Address: 0x18

D7	D6	D5	D4	D3	D2	D1	D0
DEVICE			OTP_REV			DIE_REV	

Bits	Field	Type	Default	Description
7	DEVICE	R	1	DEVICE Contains Device ID
6:2	OTP_REV	R	0 0001	OTP_REV Contains OTP Version ID

Bits	Field	Type	Default	Description
1:0	DIE_REV	R	00	DIE_REV Contains Revision ID

### 7.6.17 PFM\_LEV\_B0

Address: 0x19

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	PFM_ENTRY_B0[2:0]			Reserved	PFM_EXIT_B0[2:0]		

Bits	Field	Type	Default	Description
7	Reserved	R/W	0	
6:4	PFM_ENTRY_B0	R/W	011	PFM_ENTRY_B0 <sup>(1)</sup> Sets the target PFM entry level for Buck 0. The final PWM-to-PFM switchover current varies slightly and is dependant on the output voltage, input voltage and the inductor current level. 000 = 100 mA 001 = 125 mA 010 = 150 mA 011 = 175 mA 100 = 225 mA 101 = Reserved 110 = Reserved 111 = Reserved
3	Reserved	R/W	0	
2:0	PFM_EXIT_B0	R/W	110	PFM_EXIT_B0 <sup>(1)</sup> Sets the target PFM exit level for Buck 0. The final PFM-to-PWM switchover current varies slightly and is dependant on the output voltage, input voltage and the inductor current level. 000 = Reserved 001 = Reserved 010 = Reserved 011 = 175 mA 100 = 225 mA 101 = 275 mA 110 = 325 mA 111 = 375 mA

(1) For proper operation, the PFM exit current level should be at least 150 mA higher than the PFM entry current level.

### 7.6.18 PHASE\_LEV\_B0

Address: 0x1F

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	ADD_PH_B0[2:0]			Reserved	SHED_PH_B0[2:0]		

Bits	Field	Type	Default	Description
7	Reserved	R/W	0	
6:4	ADD_PH_B0	R/W	100	ADD_PH_B0 <sup>(1)</sup> Sets the level on which a phase is added. 000 = Reserved 001 = Reserved 010 = 0.5 A * No. of Active Phases 011 = 0.6 A * No. of Active Phases 100 = 0.7 A * No. of Active Phases 101 = 0.8 A * No. of Active Phases 110 = 0.9 A * No. of Active Phases 111 = 1.0 A * No. of Active Phases
3	Reserved	R/W	0	

(1) ADD\_PH\_B0 and SHED\_PH\_B0 values must be chosen so that the resulting hysteresis is a minimum of 100 mA and ADD\_PH\_B0 > SHED\_PH\_B0.

Bits	Field	Type	Default	Description
2:0	SHED_PH_B0	R/W	010	SHED_PH_B0 <sup>(1)</sup> Sets the level of phase shedding. 000 = 0.3 A * No. of Active Phases 001 = 0.4 A * No. of Active Phases 010 = 0.5 A * No. of Active Phases 011 = 0.6 A * No. of Active Phases 100 = 0.7 A * No. of Active Phases 101 = 0.8 A * No. of Active Phases 110 = Reserved 111 = Reserved

### 7.6.19 SEL\_I\_LOAD

Address: 0x21

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	BUCK_LOAD_CURR[10:8]			Reserved	LOAD_CURRENT_SOURCE[2:0]		

Bits	Field	Type	Default	Description
7	Reserved	R/W	0	
6:4	BUCK_LOAD_CURR[10:8]	R	000	BUCK_LOAD_CURR This register reports 3 MSB bits of the magnitude of the average load current of the selected Buck Converter. See <a href="#">LOAD_CURR</a> register.
3	Reserved	R/W	0	
2:0	LOAD_CURRENT_SOURCE[2:0]	R/W	000	LOAD_CURRENT_SOURCE These bits are used for choosing the Buck Converter whose load current will be measured. 000 = Converter 0 load current will be measured. 001 = Converter 1 load current will be measured. 010 = Converter 2 load current will be measured. 011 = Converter 3 load current will be measured. 100 = Converter 4 load current will be measured. 101 = Converter 5 load current will be measured. 110 = Master total load current will be measured. 111 = Reserved

### 7.6.20 LOAD\_CURR

Address: 0x22

D7	D6	D5	D4	D3	D2	D1	D0
BUCK_LOAD_CURR[7:0]							

Bits	Field	Type	Default	Description
7:0	BUCK_LOAD_CURR[7:0]	R	0000 0000	BUCK_LOAD_CURR This register reports 8 LSB bits of the magnitude of the average load current of the selected Buck Converter. The value is reported with a resolution of 10 mA per LSB and 20A max current. Three MSB bits are reported by SEL_I_LOAD.BUCK_LOAD_CURR[10:8] bits, see <a href="#">SEL_I_LOAD</a> . The current reported is an average over the last 5 milliseconds. The host system has read-only access to this register. This register is cleared to 0 on all resets. 000 0000 0000 Load current lower than 10 mA 000 0000 0001 10 mA ≤ Load current < 20 mA ... 111 1111 1110 20460 mA ≤ Load current < 20470 mA 111 1111 1111 Load current 20470 mA or higher. Note: Not production tested. Typical values for reference only.

### 7.6.21 INT\_MASK\_2

Address: 0x2E

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				MASK_ILOAD_READY	MASK_UVLO	MASK_TWARNING	MASK_TEMP
Bits	Field	Type	Default	Description			
7:4	Reserved	R/W	0000				
3	MASK_ILOAD_READY	R/W	1	Interrupt mask for load current measurement flag 1 = FLAGS_1.I_LOAD_READY does not set interrupt. 0 = FLAGS_1.I_LOAD_READY sets interrupt.			
2	MASK_UVLO	R/W	0	Interrupt mask for undervoltage lock-out flag 1 = FLAGS_1.UVLO does not set interrupt. 0 = FLAGS_1.UVLO sets interrupt, when triggered.			
1	MASK_TWARNING	R/W	1	Interrupt mask for thermal warning flag 1 = FLAGS_1.T_WARNING does not set interrupt. 0 = FLAGS_1.T_WARNING sets interrupt, when triggered.			
0	MASK_TEMP	R/W	1	Interrupt mask for die temperature flag bits 1 = FLAGS_0.TEMP[1:0] value change does not set interrupt. 0 = FLAGS_0.TEMP[1:0] value change sets interrupt.			

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LP8754 is a multi-phase step-down converter with 6 switcher cores bundled together.

### 8.2 Typical Application

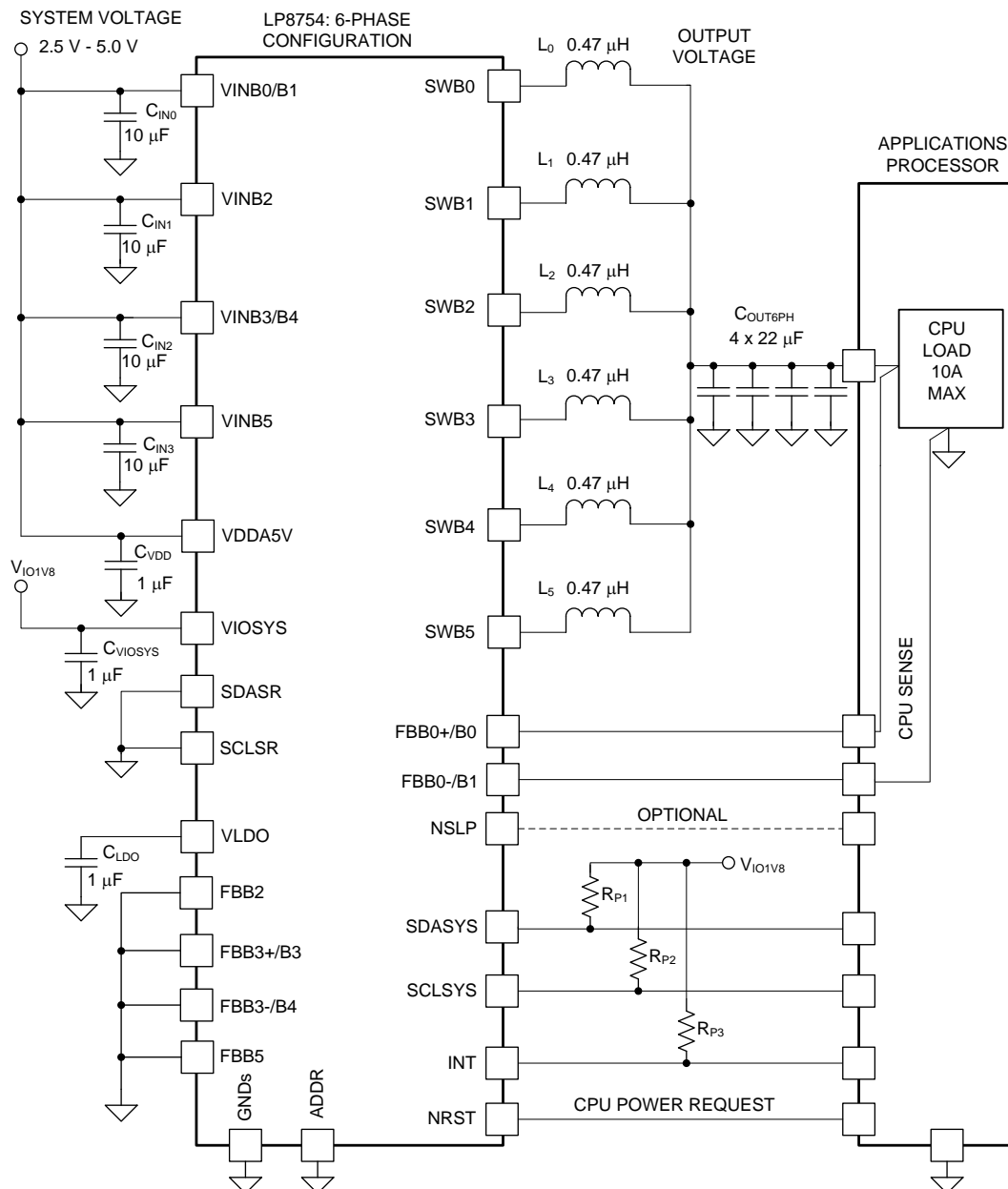


Figure 24. 6-Phase Configuration Schematic

## Typical Application (continued)

### 8.2.1 Design Requirements

Table 6 shows requirements for 6-phase configuration.

**Table 6. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 5 V
Output voltage	1.1 V
Converter operation mode	Forced PWM
Maximum load current	10 A
Inductor current limit	2.5 A

### 8.2.2 Detailed Design Procedure

The performance of the LP8754 device depends greatly on the care taken in designing the Printed Circuit Board (PCB). The use of low inductance and low serial resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the IC and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance and capacitance can easily become the performance limiting items. The separate power pins VINBXX are not connected together internally. The VINBXX power connections shall be connected together outside the package using power plane construction.

#### 8.2.2.1 Inductor Selection

The DC bias current characteristics of inductors must be considered. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. (Please request DC bias curves from the manufacturer as part of the inductor selection process.) Minimum effective value of inductance to ensure good performance is 0.25  $\mu\text{H}$  at 2.5 A (Default  $I_{\text{LIMITP}}$  typical) bias current over the inductor's operating temperature range. The inductor's DC resistance should be less than 0.05  $\Omega$  for good efficiency at high-current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Table 7 lists suggested inductors and suppliers. Shielded inductors radiate less noise and are preferable.

**Table 7. Suggested Inductors**

ITEM	MODEL	VENDOR	DIMENSIONS LxWxH (mm)	D.C.R (m $\Omega$ ) MAX
L0 to L5; Step-down converter inductor 0.47 $\mu\text{H}$	LQM21PNR47MGH	Murata	2.0 x 1.2 x 1.0	40 (typ)
	DFE252012 R47	TOKO	2.5 x 2 x 1.2	39
	DFE201612C R47N	TOKO	2.0 x 1.6 x 1.2	50

#### 8.2.2.2 Input Capacitor Selection

A ceramic input capacitor of 10  $\mu\text{F}$ , 10 V is sufficient for most applications. Place the input capacitor as close as possible to the VINBXX pin and GND pin of the device. A larger value or higher voltage rating may be used to improve input voltage filtering. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0402. Minimum effective input capacitance to ensure good performance is 2.5  $\mu\text{F}$  at maximum input voltage DC bias including tolerances and over ambient temp range, assuming that there is at least 22  $\mu\text{F}$  of additional capacitance common for all the power input pins on the system power rail.

The input filter capacitor supplies current to the PFET (high-side) switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low equivalent series resistance (ESR) provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating.

For additional noise immunity, adding a high-frequency decoupling capacitor of 100 nF to 1  $\mu\text{F}$  between VDDA5V pin and GND is recommended.

**Table 8. Suggested Input Capacitors (X5R Dielectric)**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	VOLTAGE RATING
Murata	GRM188R60J106ME84	10 $\mu$ F (20%)	0603	6.3 V
TDK	C1608X5R1A106KT	10 $\mu$ F (10%)	0603	10 V
Taiyo Yuden	LMK107BJ106MALTD	10 $\mu$ F (20%)	0603	10 V
Samsung	CL10A226MP8NUNE	22 $\mu$ F (20%)	0603	10 V

### 8.2.2.3 Output Capacitor Selection

Use ceramic capacitor, X7R or X5R types; do not use Y5V. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions. Minimum effective output capacitance to ensure good performance in 6-phase configuration is 30  $\mu$ F at the output voltage DC bias including tolerances and over ambient temp range.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its  $R_{ESR}$ . The  $R_{ESR}$  is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part.

A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreasing the PFM switching frequency. For most 6-phase applications 4 x 22- $\mu$ F 0603 capacitors for  $C_{OUT}$  is suitable. Although the converter's loop compensation can be programmed to adapt to virtually several hundreds of microfarads  $C_{OUT}$ , an effective  $C_{OUT}$  less than 120  $\mu$ F is preferred -- there is not necessarily any benefit to having a  $C_{OUT}$  higher than 120  $\mu$ F. Note that the output capacitor may be the limiting factor in the output voltage ramp, especially for very large (> 100  $\mu$ F) output capacitors. For large output capacitors, the output voltage might be slower than the programmed ramp rate at voltage transitions, because of the higher energy stored on the output capacitance. Also at start-up, the time required to charge the output capacitor to target value might be longer. At shutdown, if the output capacitor is discharged by the internal discharge resistor, more time is required to settle  $V_{OUT}$  down as a consequence of the increased time constant.

**Table 9. Suggested Output Capacitor**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	VOLTAGE RATING
Samsung	CL10A226MP8NUNE	22 $\mu$ F (20%)	0603	10 V

### 8.2.2.4 LDO Capacitor Selection

A ceramic low ESR 1- $\mu$ F capacitor should be connected between the VLDO and GNDA pins.

**Table 10. Suggested LDO Capacitor**

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	VOLTAGE RATING
Samsung	CL03A105MQ3CSNH	1 $\mu$ F (20%)	0201	6.3 V

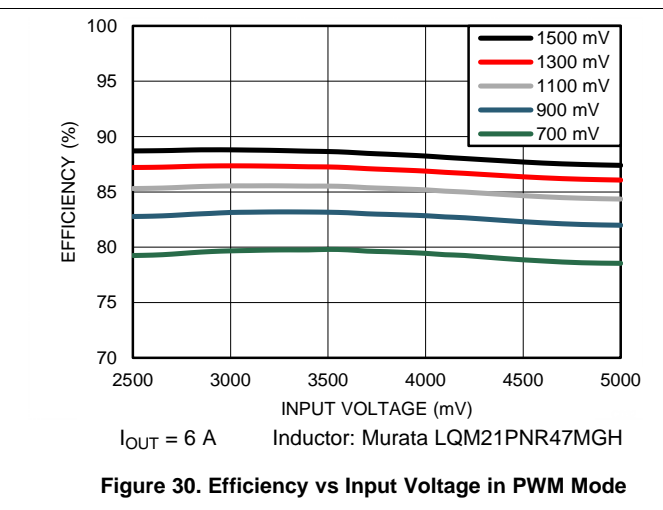
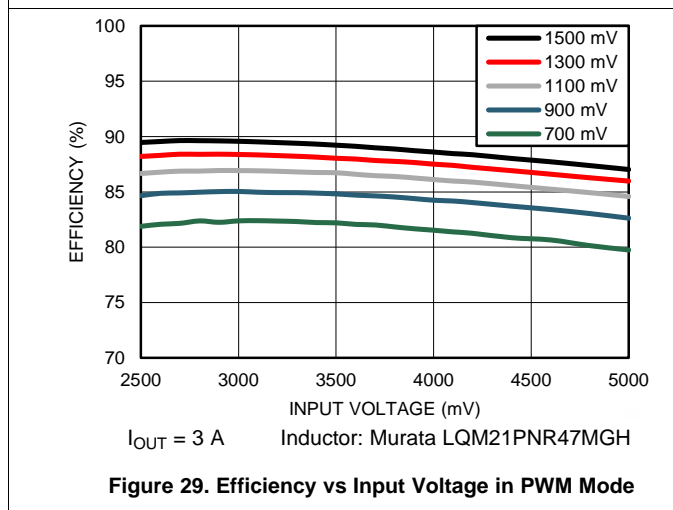
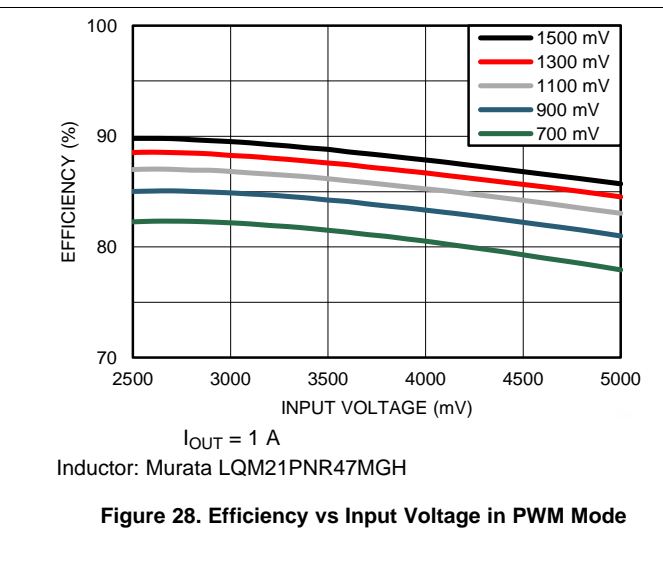
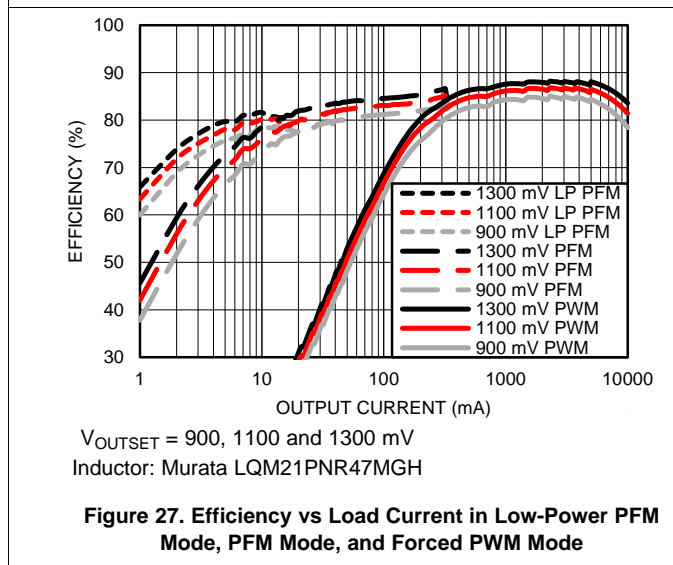
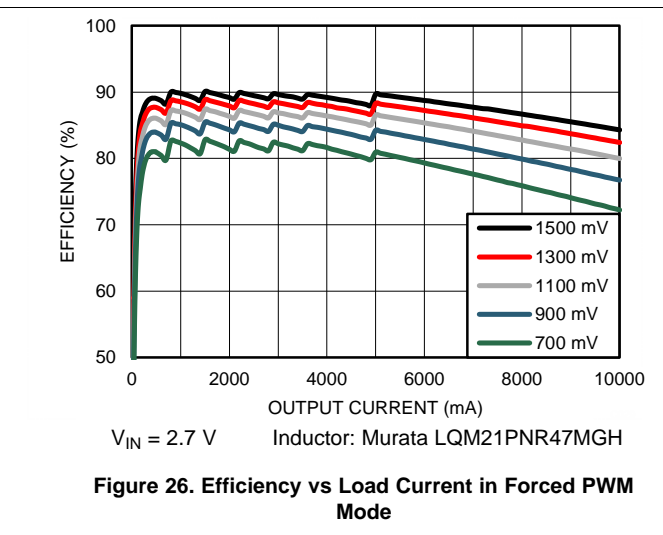
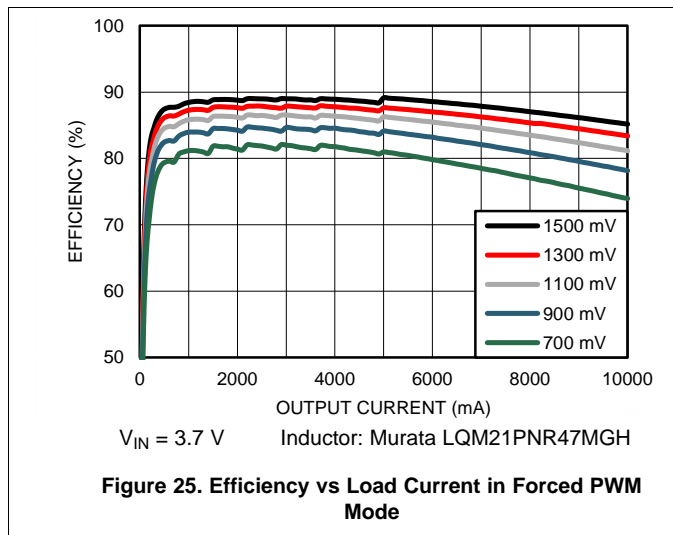
### 8.2.2.5 VIOSYS Capacitor Selection

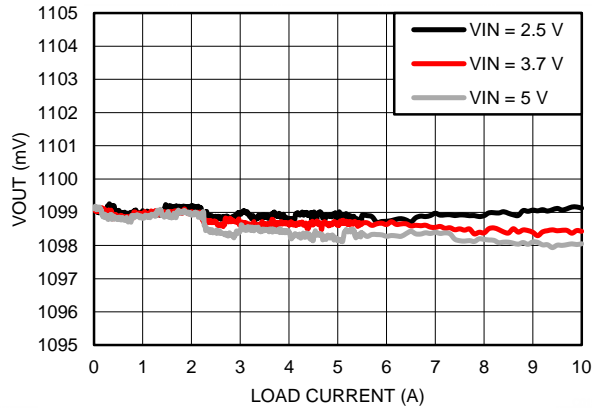
Adding a ceramic low ESR 1- $\mu$ F capacitor between the VIOSYS pin and GND is recommended. If  $V_{VIOSYS}$  signal is low noisy the capacitor is not required.



### 8.2.3 Application Curves

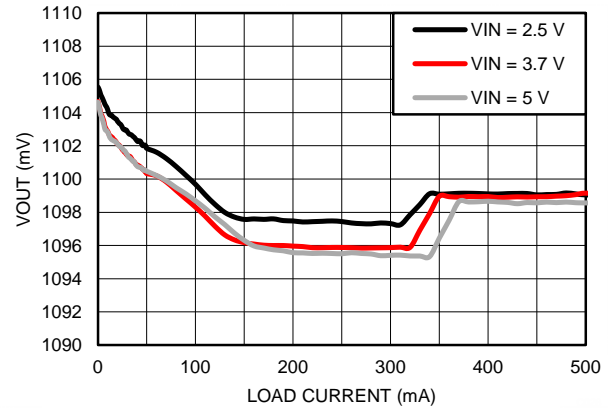
Unless otherwise specified:  $V_{VDDA5V} = V_{VINBXX} = 3.7\text{ V}$ ,  $V_{OUT} = 1.1\text{ V}$ ,  $T_A = 25^\circ\text{C}$





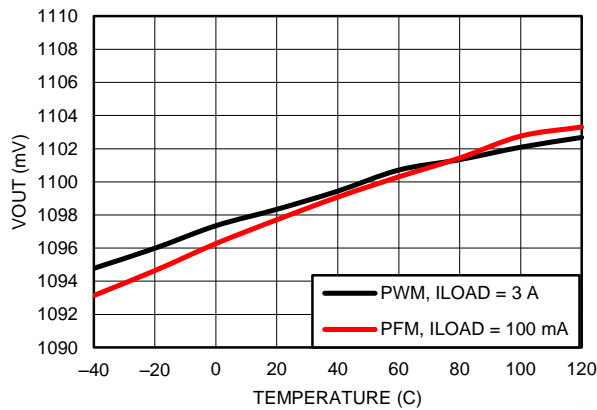
$V_{OUTSET} = 1.1\text{ V}$

Figure 31. Output Voltage vs Load Current in Forced PWM Mode



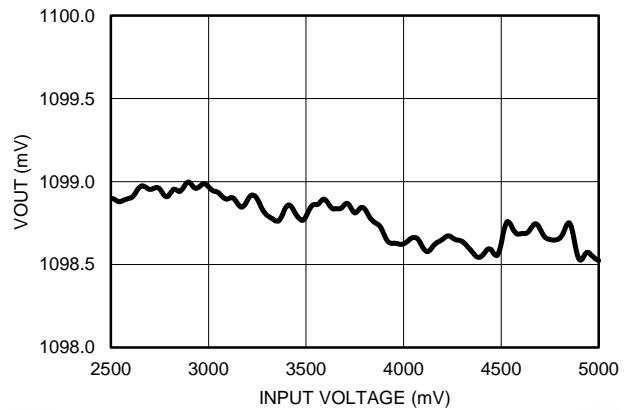
$V_{OUTSET} = 1.1\text{ V}$

Figure 32. Output Voltage vs Load Current in PFM/PWM Mode



$V_{OUTSET} = 1.1\text{ V}$

Figure 33. Output Voltage vs Temperature



$I_{LOAD} = 1.0\text{ A}$       $V_{OUTSET} = 1.1\text{ V}$

Figure 34. Line Regulation

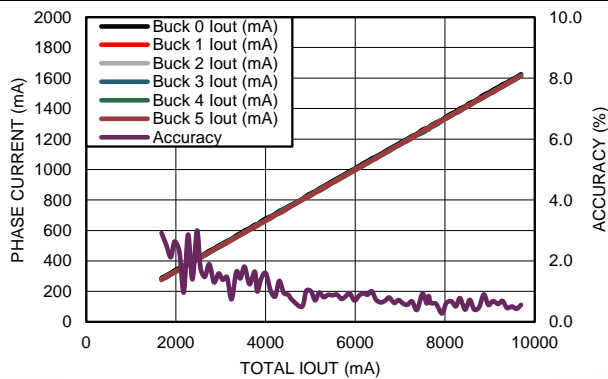


Figure 35. Phase Currents and Current Balancing Accuracy, 6 Phases Active (Currents measured by LP8754)

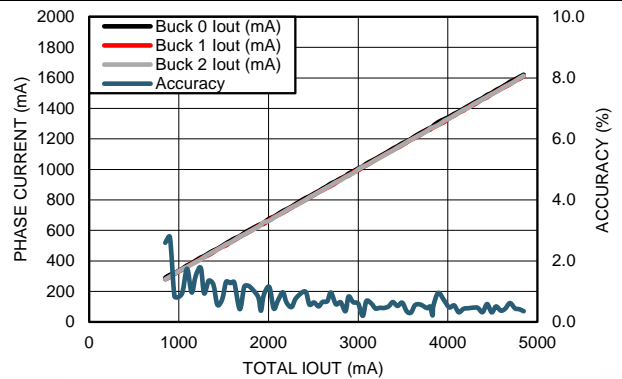


Figure 36. Phase Currents and Current Balancing Accuracy, 3 Phases Active (Currents measured by LP8754)

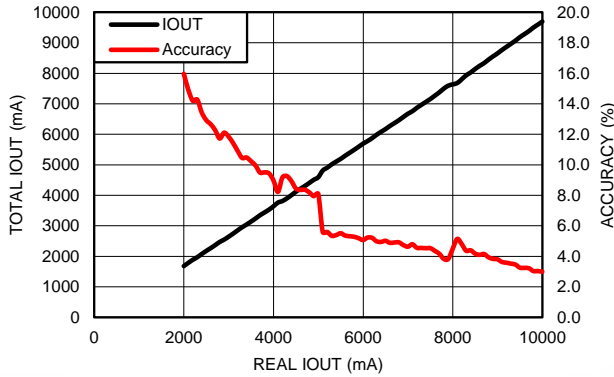


Figure 37. Load Current Measured by LP8754 vs Real Load Current, 6 Phases Active

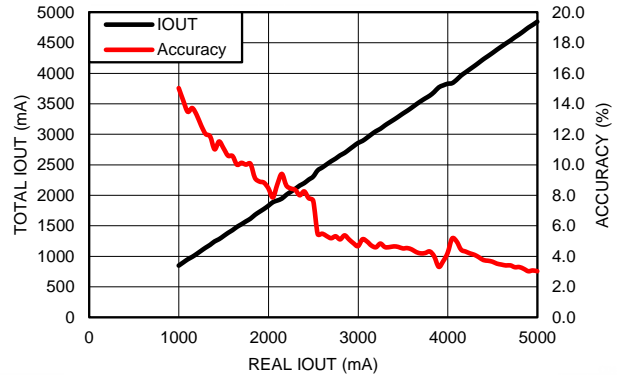


Figure 38. Load Current Measured by LP8754 vs Real Load Current, 3 Phases Active

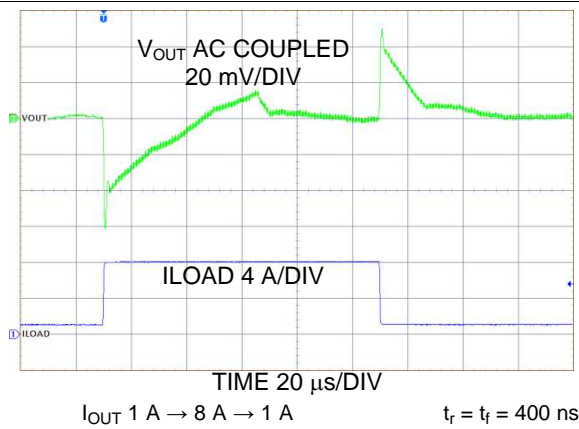


Figure 39. Transient Load Step Response, PWM Mode

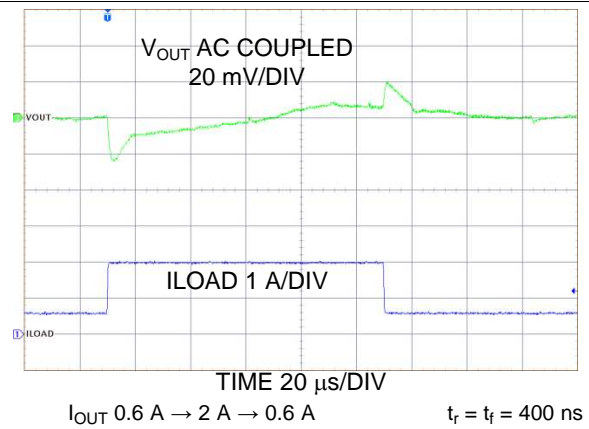


Figure 40. Transient Load Step Response, PWM Mode

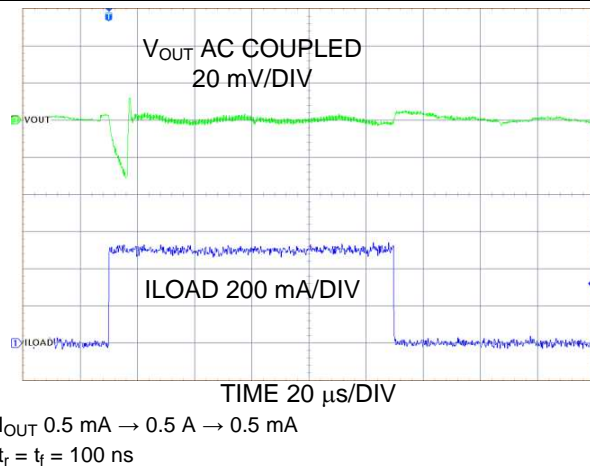


Figure 41. Transient Load Step Response, AUTO Mode

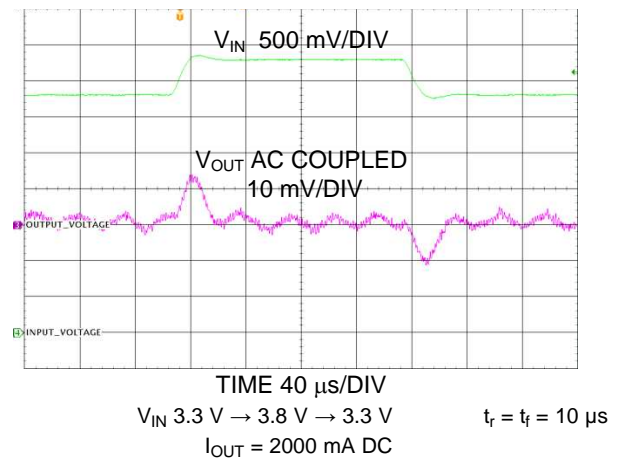


Figure 42. Transient Line Response

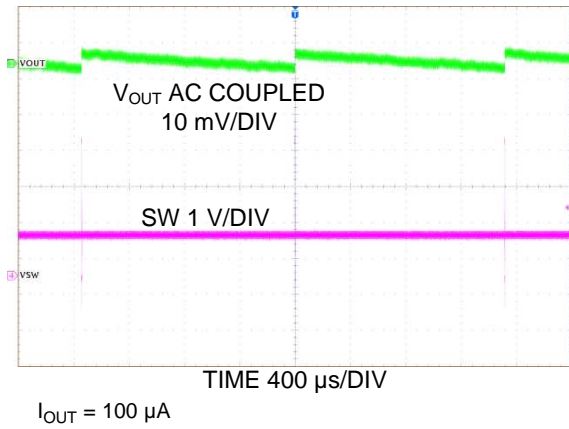


Figure 43. Output Voltage Ripple, PFM Mode

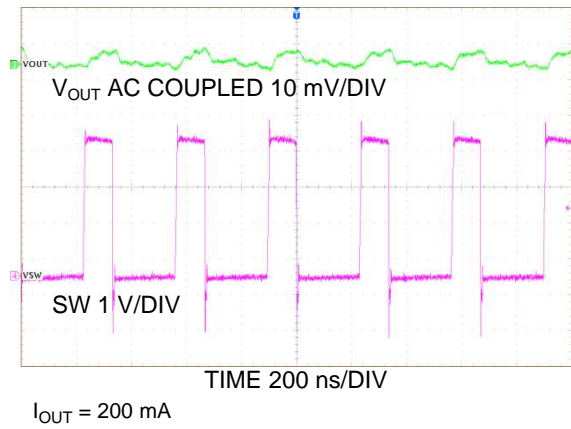


Figure 44. Output Voltage Ripple, PWM Mode, One Phase Active

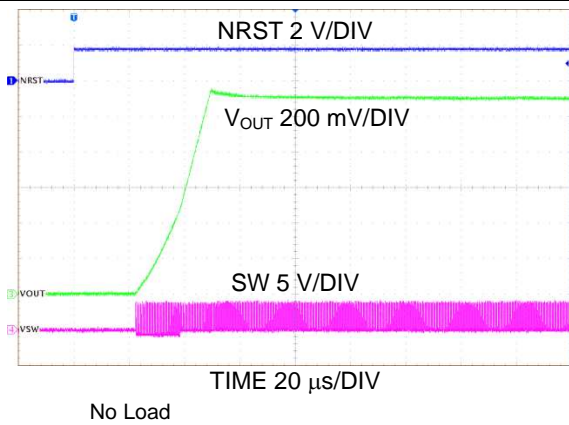


Figure 45. Start-up with NRST, Forced PWM

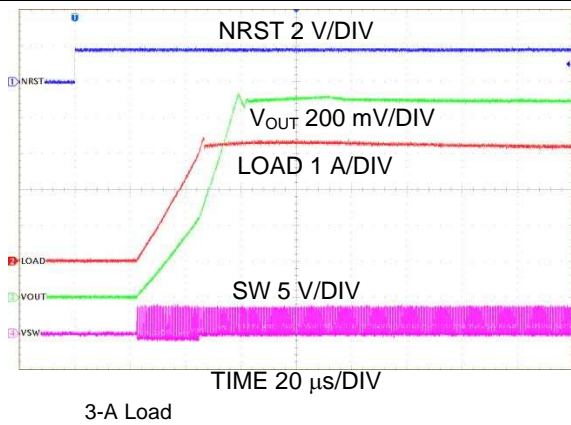


Figure 46. Start-up with NRST, Forced PWM

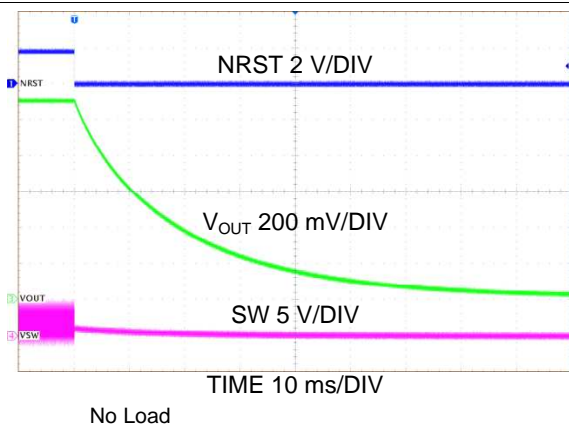


Figure 47. Shutdown with NRST, Forced PWM

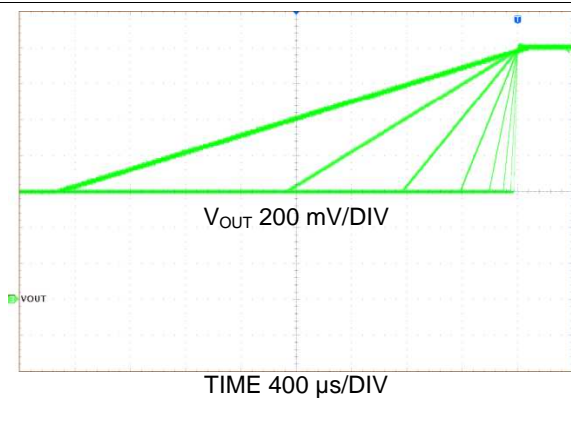


Figure 48.  $V_{OUT}$  Transition from 0.6 V to 1.4 V with Different Ramp Settings

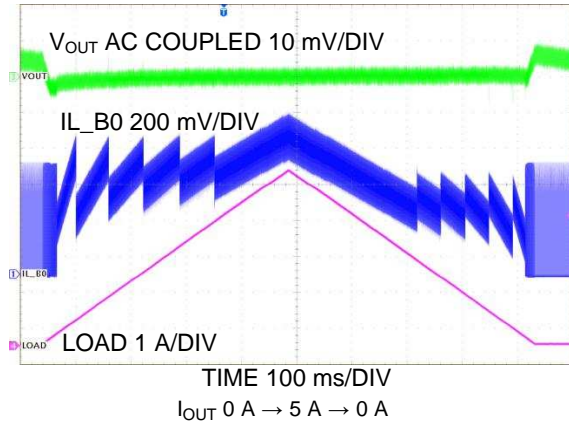


Figure 49. Load Ramp

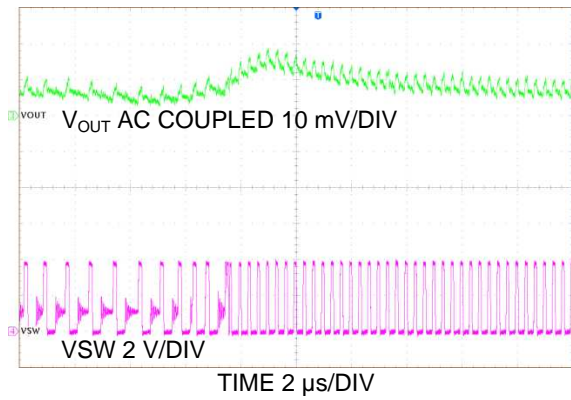


Figure 50. Transient from PFM to PWM Mode

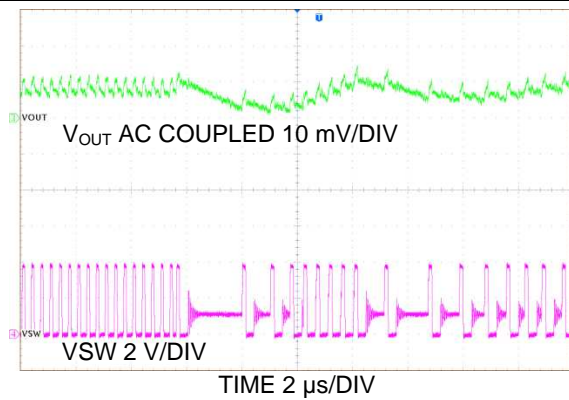


Figure 51. Transient from PWM to PFM Mode

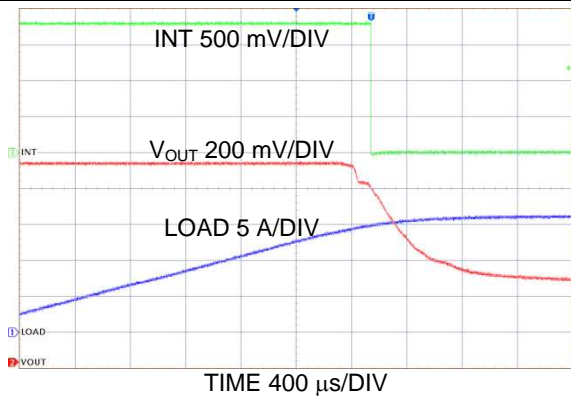


Figure 52. Interrupt Line Going Low with Not Power Good Activation

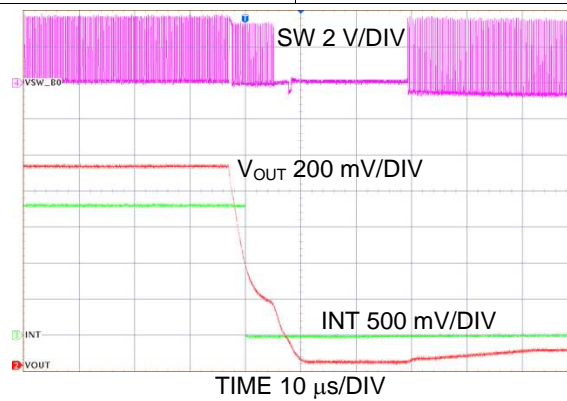


Figure 53. Metallic Short Applied at V<sub>OUT</sub>

## 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 5 V. This input supply should be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail should be low enough that the input current transient does not cause too high drop in the LP8754 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP8754 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

## 10 Layout

### 10.1 Layout Guidelines

The high frequency and large switching currents of the LP8754 make the choice of layout important. Good power supply results will only occur when care is given to proper design and layout. Bad layout will affect noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to 10 A, good power-supply layout is more challenging than for most general PCB design. The following steps should be used as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range:

1. Place  $C_{IN}$  as close as possible to the VINBXX pin and the GND pin. Route the  $V_{IN}$  trace wide and thick to avoid IR drops. The trace between the input capacitor's positive node and LP8754's VINBXX pin(s) as well as the trace between the input capacitor's negative node and power GND pin(s) must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The parasitic inductance on these traces must be kept as tiny as possible for proper device operation.
2. The output filter for each buck, consisting of  $C_{OUT}$  and L, converts the switching signal at SW to the noiseless output voltage. For optimal EMI behavior, it should be placed as close as possible to the device, keeping the switch node small. Route the traces between the LP8754's output capacitors and the load's input capacitors direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VDDA5V and GNDA) should be isolated from noisy signals. Connect VDDA5V directly to a quiet system voltage node and GNDA to a quiet ground point where no IR drop occurs. For additional noise immunity, adding a high-frequency decoupling capacitor of 100 nF to 1  $\mu$ F is recommended. Place the decoupling capacitor as close to the VDDA5V pin as possible. VDDA5V trace is low current, so the trace width does not need to be optimized.
4. If the processor load supports voltage remote sensing, connect the LP8754 feedback pins FBBXX to the respective sense pins on the processor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as GNDBXX,  $V_{IN}$ , and SW, as well as high bandwidth signals such as the I<sup>2</sup>C. Avoid both capacitive as well as inductive coupling by keeping the sense lines short, direct, and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. Running the signal as a differential pair is recommended.
5. GNDBXX,  $V_{IN}$ , and SW should be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy GNDBXX,  $V_{IN}$ , and SW. This can create noise coupling to inner signal layers.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ( $R_{\theta JA}$ ) and junction-to-board ( $R_{\theta JB}$ ) thermal resistances, thereby reducing the device junction temperature,  $T_J$ . It's strongly recommended to perform a careful system-level 2D or full 3D dynamic thermal analysis at the beginning of the product design process, using a thermal modeling analysis software.

### 10.2 Layout Example

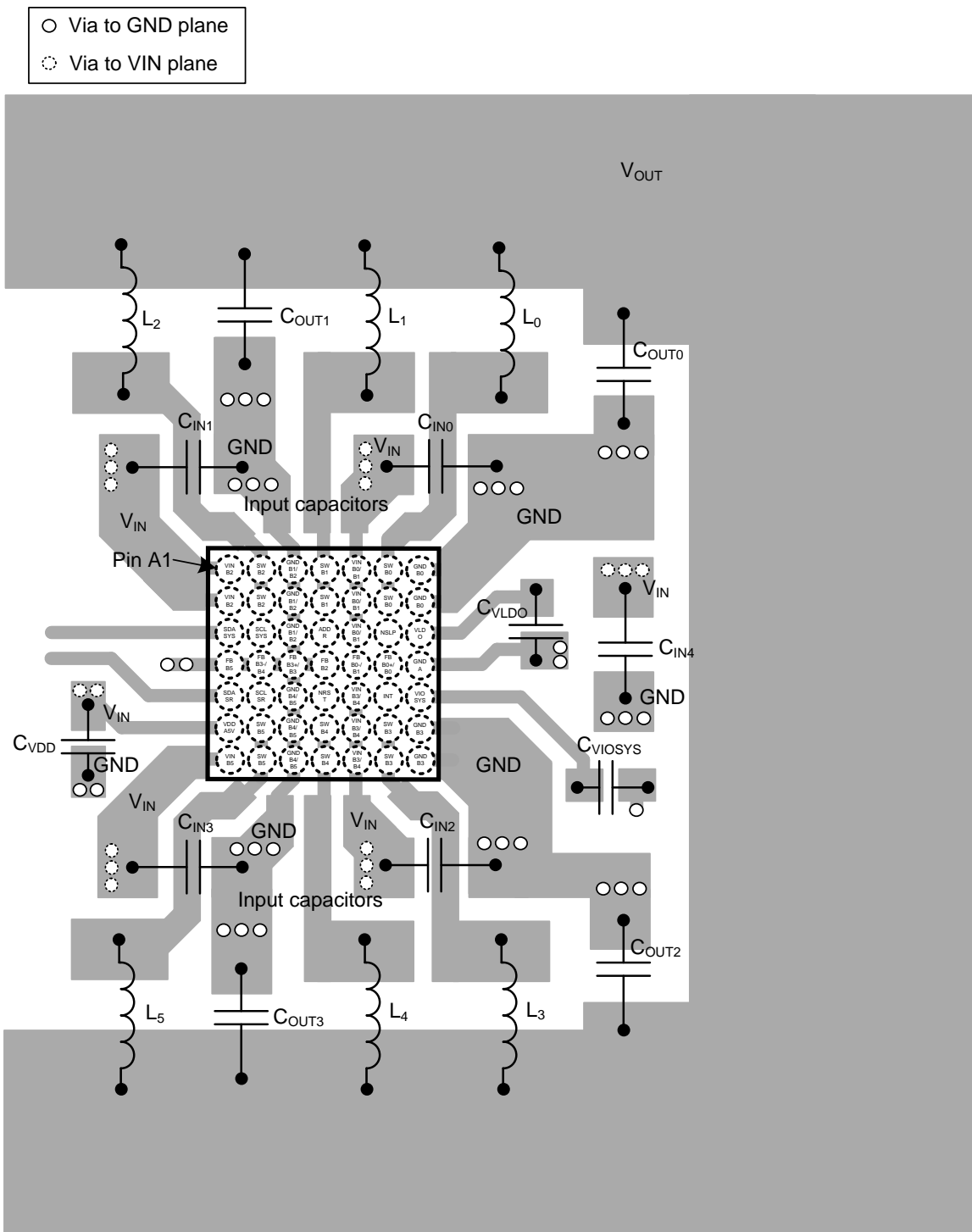


Figure 54. LP8754 Board Layout



## 11 器件和文档支持

### 11.1 器件支持

#### 11.1.1 第三方产品免责声明

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### 11.2 文档支持

#### 11.2.1 相关文档

相关文档如下：

德州仪器 (TI) 应用手册《*DSBGA 晶圆级芯片规模封装*》（文献编号：[SNVA009](#)）。

### 11.3 商标

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.5 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

## 12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP875484YFQR	ACTIVE	DSBGA	YFQ	49	1000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	754A	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

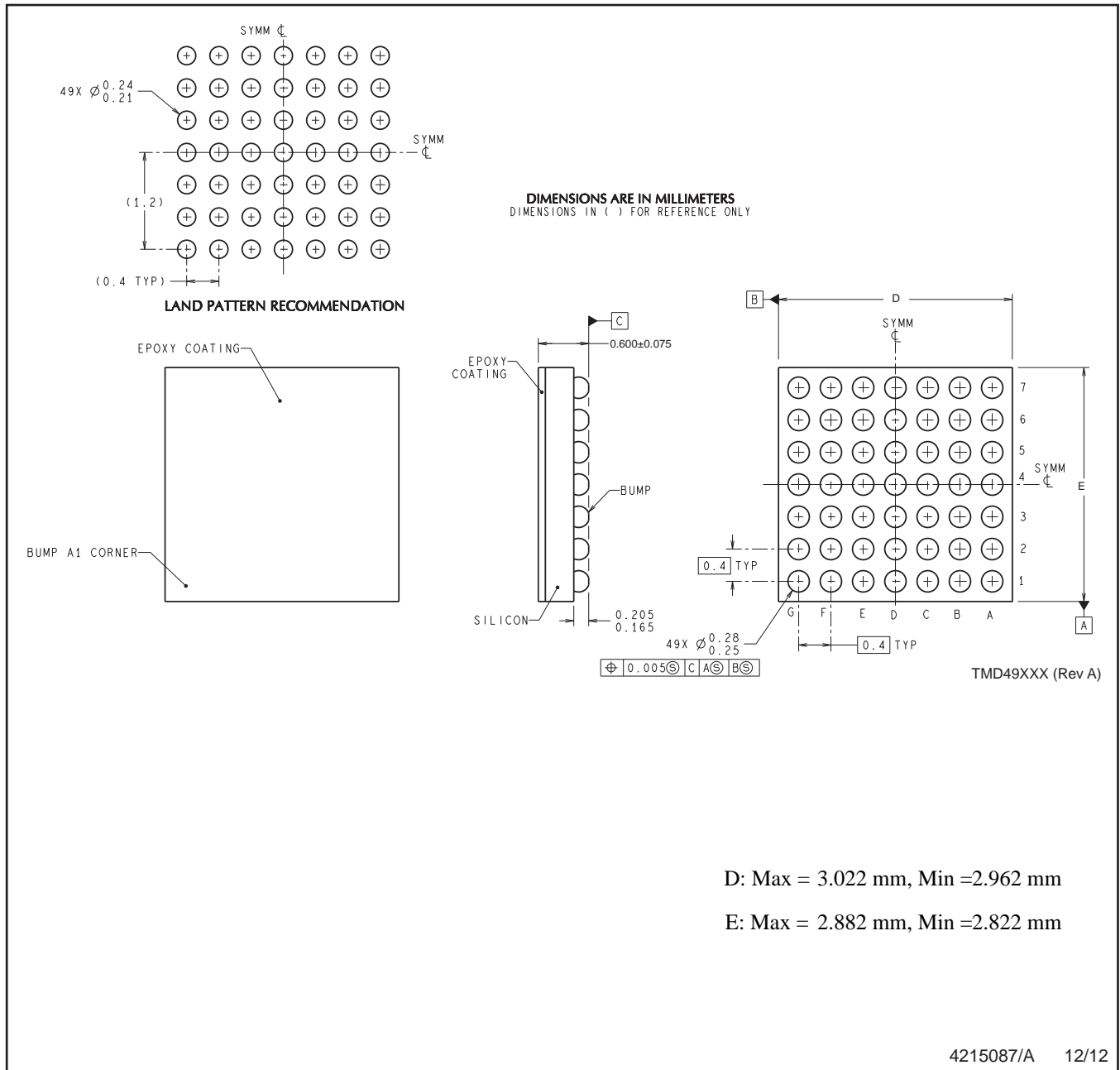
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP875484YFQR	DSBGA	YFQ	49	1000	178.0	12.4	3.06	3.2	0.9	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP875484YFQR	DSBGA	YFQ	49	1000	208.0	191.0	35.0

YFQ0049



D: Max = 3.022 mm, Min = 2.962 mm

E: Max = 2.882 mm, Min = 2.822 mm

4215087/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.

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