具有集成型 FET 的 4.5-V 至 16-V 输入、高电流、3 个同步降压 DC-DC转换器和 2 个USB开关

查询样品: TPS65258

特性

- 高跨度输入供电电压范围: **4.5 V - 16 V**
- **0.8-V, 1%** 准确度参考
- 连续载荷: **3 A (**降压转换器 **1), 2 A (**降压转换器 **2** 和 **3)**
- 最大电流: **3.5 A (**降压转换器 **1), 2.5 A (**降压转换器 **2** 和 **3)**
- 同步运行**,** 外部电阻器设定的**300-kHz – 2.2-MH**开关频率
- 具有内置电流源的外部使能引脚，用于简单排序
- 外部软启动引脚
- 外部电阻器设定的可调逐周期电流限值
- 具有简单补偿电路的电流模式控制
- 自动低脉冲跳跃 **(PSM)** 功率模式**,** 允许一个小于**2%**的输出电流脉动
- 强制**PWM**模式
- 支持预偏置输出
- 电源正常监视器和复位发生器
- **2** 个具有过载和过热保护功能的 **1-A USB** 电源开关
- 小型**,** 高热效**40-**针 **6-mm x 6-mm RHA (QFN)**封装
- **-40°C** 到 **125°C** 结点温度范围

说明/订购信息

TPS65258 是一个具有3个降压变换器的电源管理集成电路（IC）. 由于具有集成的高侧和低侧MOSFET，它能够提供更高效的完全同步转换。 此类转换器设计用于简化应用，同时可以使设计人员根据目标应用对它们的使用进行优化。

此转换器可运行在 5-, 9-, 12- 或者 15-V 系统。 可使用电阻分压器从外部对输出电压值进行设置，此电压值可以是0.8 V至输入电压减去转换器通路上的电阻性压降后所得电压值间的任意数值。 每个转换器特有一个使能引脚，它允许针对排序用途的延迟启动，软启动引脚可通过选择软启动电容对软启动时间进行调节，而一个限流（RLIM）引脚使得设计人员能够通过选择一个外部电阻器来调节电流限值并优化电感器的选择。 所用的转换器都运行在 “断续模式”: 一旦任何一个转换器感应到超过 10ms 的过载电流, 它们将关闭 10ms，然后将会重试启动序列。 如果过载已被排除，则转换器将逐步启动并正常运转。 如果情况不是这样的话，转换器将之视为另外的过载事件并再次关闭，此过程（断续）将一直重复直到故障被清除。 如果过载持续时间少于 10ms，则只有受到影响的转换器会关闭、然后重启动，这不会引起全局的断续模式。

转换器的开关频率由一个连接至 ROSC引脚的外部电阻器设定。 开关式稳压器设计工作频率为300 kHz 至 1.2 MHz。 转换器彼此 180° 异相操作以将输入滤波器要求降到最低。 所有转换器具有峰值电流模式控制以简化外部频率补偿。

此设备有一个内置斜率特性补偿斜波来防止在峰值电流模式控制中的次谐波振荡。 一个传统II类补偿网络能够稳定系统并实现快速瞬态反映。 而且，一个与反馈分频器上层电阻并行的可选电容提供10倍的交叉频率并使得交叉频率超过100kHz。

所有转换器特有一个自动低功耗脉冲PFM模式，此模式可在轻负载和待机运行时提升效能，同时保证一个非常低的输出脉动，允许的值比低输出电压时少 2%。

这个设备包含一个过载电压瞬时保护电路以将电压过冲降到最低。 通过一个能比较FB引脚电压与OVP阀值电压（内部电压参考的109%）的电路，OVP可将输出过冲最小化。 如果FB引脚电压大于OVTP阀值时，高侧MOSFET被置成无效以防止电流流向输出并将输出过冲降到最低. 当FB电压下降至低于OVP较低阀值（内部参考电压的 107%）时，高侧MOSFET可启动下一个时钟周期。

English Data Sheet: SLVSB31

TPS65258 特有一个监视电路，用于监视每个降压输出并且一旦排序完成，PGOOD引脚就被启用。 PGOOD引脚具备漏极开路输出功能。 当任何一个降压转换器被拉低至额定输出电压的85%的时候，PGOOD引脚被置成低输入电平。 当所有转换器的输出超过它额定输出电压的90%的时候，PGOOD引脚被置成高输入电平。 默认重置时间为100ms。 PGOOD的极性是高电平有效。

这 2 个USB 开关为下游USB设备提供所需的高达 1-A 电流。 当输出负载超出电流限制阈值或短路出现时，通过切换到恒定电流模式，上拉过载逻辑输出低电平，PMU将输出电流限制在安全水平上。 当开关中的持续高过载和短路使功率耗散增加进而引起结点温度上升时，则一个过热警告保护电路会关闭此USB开关并允许降压转换器开始运行。

如果结点温度超过 160°C时，此设备执行一个内部热关断以对自身进行保护。 当结点温度超过热敏断路阀值的时候，热关断强制设备停止运行。 一旦温度减至低于 140°C, 此设备重新启动加电序列。 热关断滞后保护温度为 20°C。

订购信息(1)

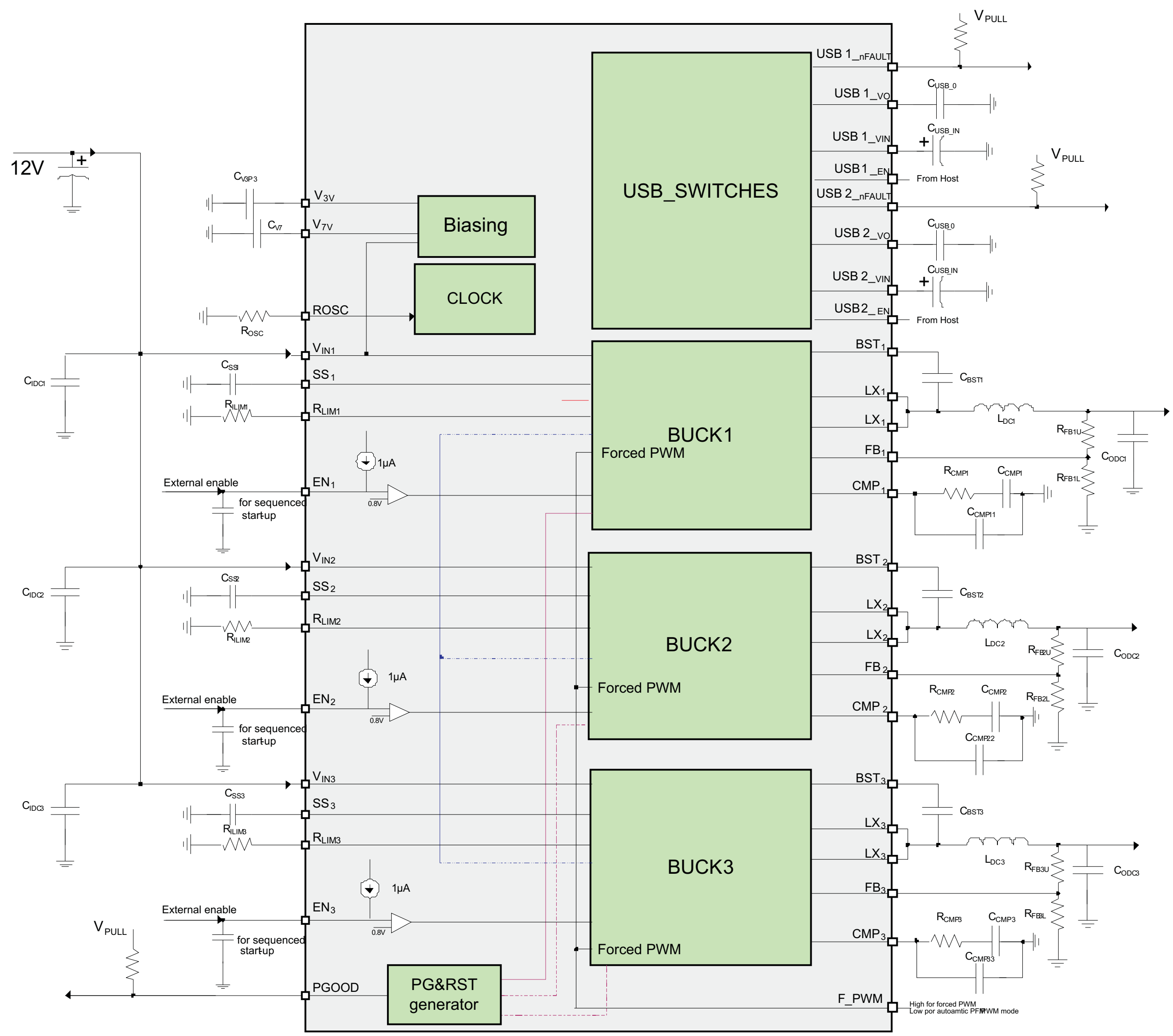
T_A	封装(2)		器件型号	正面标记
-40°C 至 125°C	40-引脚 (QFN) - RHA	卷盘 （ 2500 片 ）	TPS65258RHAR	TPS65258

(1) 如需了解最新的封装及订购信息，敬请查看本文档末的 “封装选项附录”，或查看 TI 网站 www.ti.com.cn。
(2) 封装图样、热数据和符号可登录 www.ti.com/packaging 获取。

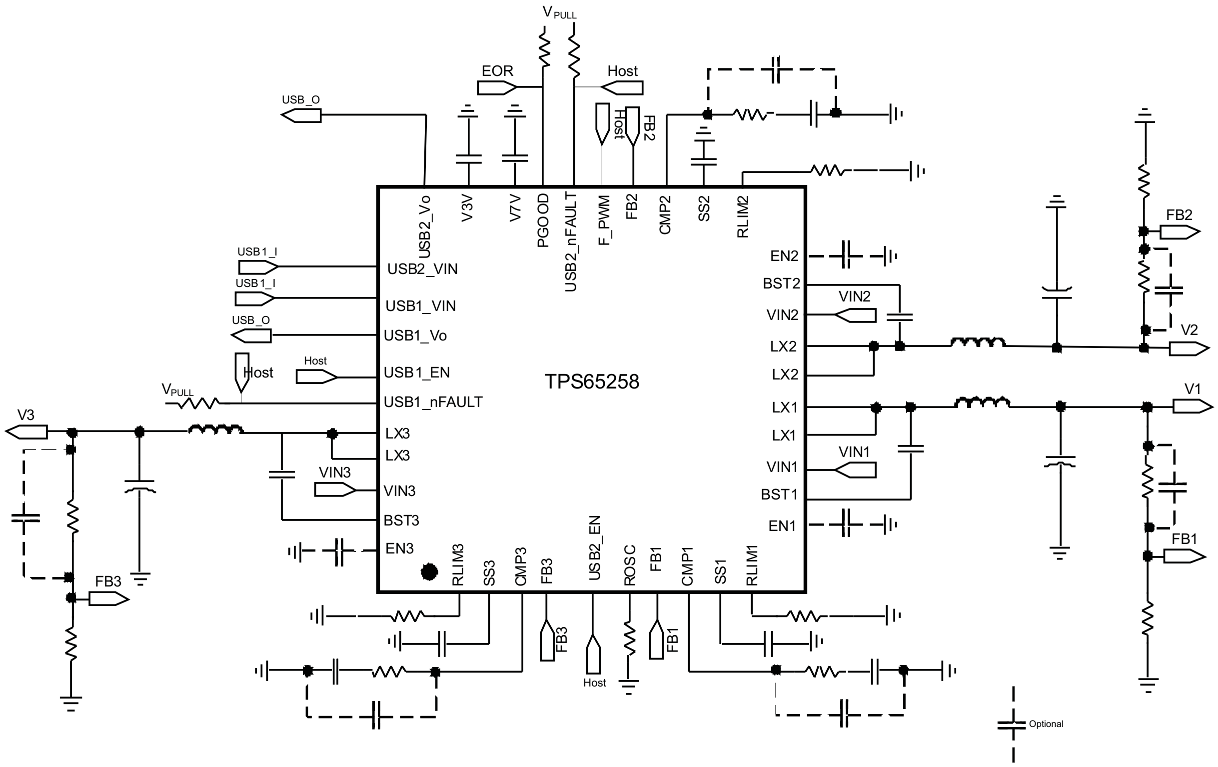
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

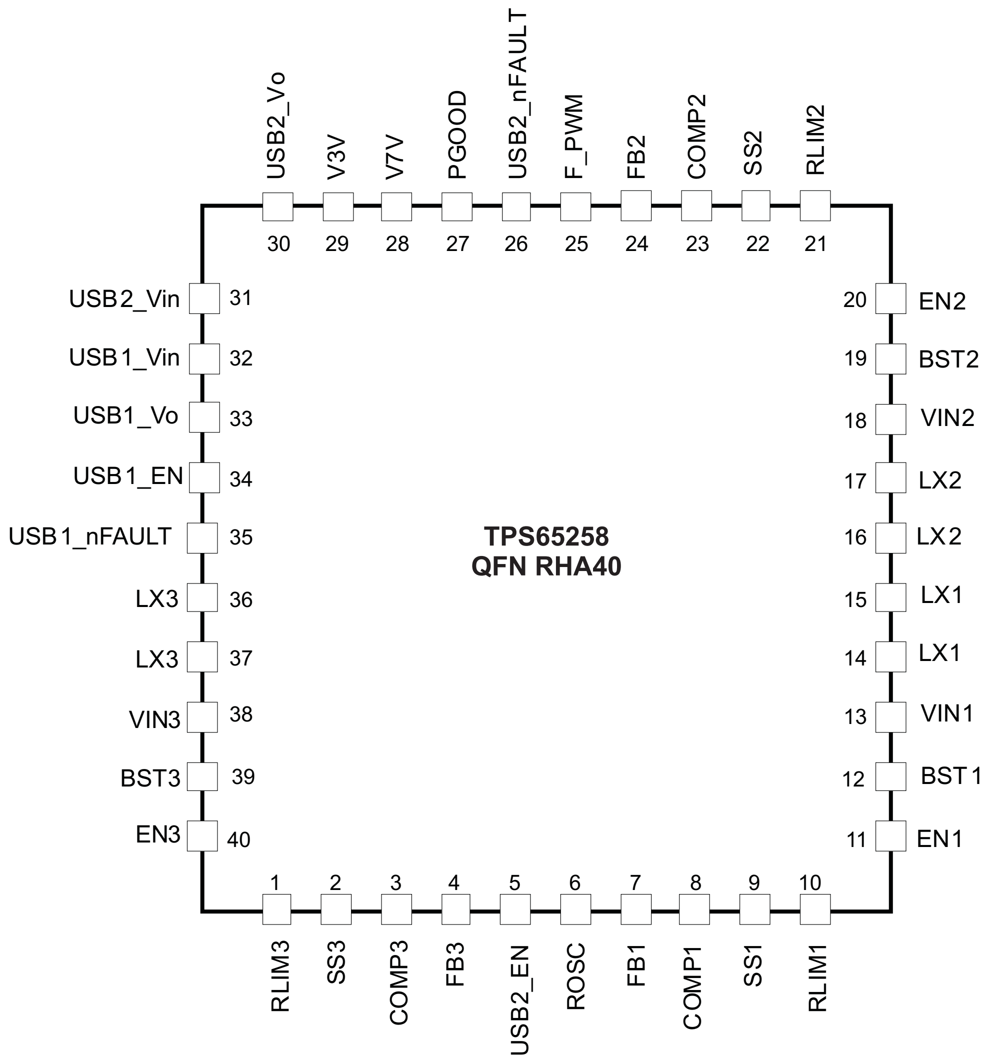
FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION



PIN OUT


USB2_Vo
V3V
V7V
PGOOD
USB2_nFAULT
F_PWM
FB2
COMP2
SS2
RLIM2
30
29
28
27
26
25
24
23
22
21
USB2_Vin 31
USB1_Vin 32
USB1_Vo 33
USB1_EN 34
USB1_nFAULT 35
LX3 36
LX3 37
VIN3 38
BST3 39
EN3 40
20 EN2
19 BST2
18 VIN2
17 LX2
16 LX2
15 LX1
14 LX1
13 VIN1
12 BST1
11 EN1
TPS65258
QFN RHA40
1
2
3
4
5
6
7
8
9
10
RLIM3
SS3
COMP3
FB3
USB2_EN
ROSC
FB1
COMP1
SS1
RLIM1

TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
RLIM3	1	I	Current limit setting for Buck3. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS3	2	I	Soft start pin for Buck3. Fit a small ceramic capacitor to this pin to set the converter soft start time.
COMP3	3	O	Compensation for Buck3. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB3	4	I	Feedback pin for Buck3. Connect a divider set to 0.8 V from the output of the converter to ground.
USB2_EN	5	I	Enable input, high turns on the switch
ROSC	6	I	Oscillator set. This resistor sets the frequency of internal autonomous clock.
FB1	7	I	Feedback pin for Buck1. Connect a divider set to 0.8 V from the output of the converter to ground.
COMP1	8	O	Compensation pin for Buck1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
SS1	9	I	Soft-start pin for Buck1. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
RLIM1	10	I	Current limit setting pin for Buck1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
EN1	11	I	Enable pin for Buck1. A high signal on this pin enables the regulator Buck. For a delayed start-up add a small ceramic capacitor from this pin to ground.
BST1	12		Bootstrap capacitor for Buck1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
VIN1	13	I	Input supply for Buck1. Fit a 10-µF ceramic capacitor close to this pin.
LX1	14, 15	O	Switching node for Buck1
LX2	16, 17	O	Switching node for Buck2
VIN2	18	I	Input supply for Buck2. Fit a 10-µF ceramic capacitor close to this pin.
BST2	19		Bootstrap capacitor for Buck2. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN2	20	I	Enable pin for Buck2. A high signal on this pin enables the regulator. For a delayed start-up add a small ceramic capacitor from this pin to ground.
RLIM2	21	I	Current limit setting pin for Buck2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS2	22	I	Soft-start pin for Buck2. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
COMP2	23	O	Compensation pin for Buck2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB2	24	I	Feedback input for Buck2. Connect a divider set to 0.8 V from the output of the converter to ground.
F_PWM	25		Forces PWM operation in all converters when set high. If low converters will operate in automatic PFM/PWM mode.
USB2_nFAULT	26	I	USB2 fault flag output, open drain, active low. Asserted when overcurrent or over temperature condition is detected in the switch.
PGOOD	27	O	Power good. Open drain output asserted low after all converters and sequenced and within regulation. Polarity is factory selectable (active high default).
V7V	28	O	Internal supply. Connect a 10-µF ceramic capacitor from this pin to ground.
V3V	29	O	Internal supply. Connect a 10-µF ceramic capacitor from this pin to ground.
USB2_Vo	30	O	USB switch output
USB2_VIN	31	I	USB switch input supply
USB1_VIN	32	I	USB switch input supply
USB1_Vo	33	O	USB switch output

TERMINAL FUNCTIONS (continued)

NAME	NO.	I/O	DESCRIPTION
USB1_EN	34	I	Enable input, high turns on the switch
USB1_nFAULT	35	I	USB1 fault flag output, open drain, active low. Asserted when overcurrent or overtemperature condition is detected in the switch.
LX3	36, 37	O	Switching node for Buck3
VIN3	38	I	Input supply for Buck3. Fit a 10-μF ceramic capacitor close to this pin.
BST3	39	I	Bootstrap capacitor for Buck3. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN3	40	I	Enable pin for Buck3. A high signal on this pin enables the converter. For a delayed start-up add a small ceramic capacitor from this pin to ground.
PowerPAD			PowerPAD. Connect to system ground for electrical and thermal connection.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted, all voltages are with respect to GND)

	Voltage range at VIN1,VIN2, VIN3, LX1, LX2, LX3	–0.3 to 18	V
	Voltage range at LX1, LX2, LX3 (maximum withstand voltage transient < 10 ns)	–3 to 18	V
	Voltage at BST1, BST2, BST3 referenced to LX pin	–0.3 to 7	V
	Voltage at V7V, COMP1, COMP2, COMP3, USB1_Vin, USB1_Vo, USB2_Vin, USB2_Vo	–0.3 to 7	V
	Voltage at V3V, RLIM1, RLIM2, RLIM3, EN1,EN2, EN3, SS1, SS2, SS3, FB1, FB2,FB3 , PGOOD, ROSC, USB1_EN, USB1_nLIMx, USB2_EN, USB2_nLIMx,	–0.3 to 3.6	V
T_J	Operating junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		16	V
T_A	Junction temperature	–40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} (°C/W)	T_A = 25°C POWER RATING (W)	T_A = 55°C POWER RATING (W)	T_A = 85°C POWER RATING (W)
RHA	30	3.33	2.3	1.3

(1) Based on JEDEC 51.5 HIGH K environment measured on a 76.2 x 114 x 0.6-mm board with the following layer arrangement:
(a) Top layer: 2 Oz Cu, 6.7% coverage
(b) Layer 2: 1 Oz Cu, 90% coverage
(c) Layer 3: 1 Oz Cu, 90% coverage
(d) Bottom layer: 2 Oz Cu, 20% coverage

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4.5		16	V
IDD_{SDN}	Shutdown	EN pin = low for all converters		170		µA
IDD_Q	Quiescent (push-button pull-up current not included)	Converters enabled, no load Buck1 = 1.2 V Buck2 = 1.8 V Buck3 = 3.3 V T_A = 25°C, F_PWM = Low		600		µA
	Quiescent, forced PWM	Converters enabled, no load F_PWM = High		18		mA
UVLO	V_{IN} under voltage lockout	Rising V_{IN}		4.22		V
		Falling V_{IN}		4.1		
$UVLO_{DEGLITCH}$		Both edges		110		µs
V3p3	Internal biasing supply			3.3		V
V7V	Internal biasing supply			6.25		V
$V7V_{UVLO}$	UVLO for internal V7V rail	Rising V7V		3.8		V
		Falling V7V		3.6		
$V7V_{UVLO\_DEGLITCH}$		Falling edge		110		µs
BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT-START AND SWITCHING FREQUENCY)						
V_{IH_ENx}	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENx} rising	0.66 x V3p3			V
V_{IL_ENx}	Enable treshold low	V3p3 = 3.2 V - 3.4 V, V_{ENx} falling			0.33 x V3p3	V
$V_{IH\_F\_PWM}$	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENx} rising	0.66 x V3p3			V
$V_{IL\_F\_PWM}$	Enable treshold low	V3p3 = 3.2 V - 3.4 V, V_{ENx} falling			0.33 x V3p3	V
ICH_{EN}	Pull up current enable pin			1		µA
t_D	Discharge time enable pins	Power-up		10		ms
I_{SS}	Soft-start pin current source			5		µA
F_{SW_BK}	Converter switching frequency range	Set externally with resistor	0.3		2.2	MHz
R_{FSW}	Frequency setting resistor		50		600	kΩ
f_{SW_TOL}	Internal oscillator accuracy	f_{SW} = 800 kHz	-10		10	%
FEEDBACK, REGULATION, OUTPUT STAGE						
V_{FB}	Feedback voltage	V_{IN} = 12 V , T_A = 25°C	-1%	0.8	1%	V
		V_{IN} = 4.5 V to 16 V	-2%	0.8	2%	
t_{ON_MIN}	Minimum on time (current sense blanking)				135	ns
I_{LIMIT1}	Peak inductor current limit range		0.75		4	A
I_{LIMIT2}	Peak inductor current limit range		0.75		3	A
I_{LIMIT3}	Peak inductor current limit range		0.75		3	A
MOSFET (BUCK 1)						
H.S. Switch	On resistance of high side FET on CH1	25°C, BOOT = 6.5 V		95		mΩ
L.S. Switch	On resistance of low side FET on CH1	25°C, VIN = 12 V		50		mΩ
MOSFET (BUCK 2)						
H.S. Switch	On resistance of high side FET on CH2	25°C, BOOT = 6.5 V		120		mΩ
L.S. Switch	On resistance of low side FET on CH2	25°C, VIN = 12 V		80		mΩ

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET (BUCK 3)						
H.S. Switch	On resistance of high side FET on CH3	25°C, BOOT = 6.5 V		120		mΩ
L.S. Switch	On resistance of low side FET on CH3	25°C, VIN = 12 V		80		mΩ
ERROR AMPLIFIER						
g_M	Error amplifier transconductance	-2 μA < ICOMP < 2 μA		130		μ℧
gm_{PS}	COMP to ILX gm	I_{LX} = 0.5 A		10		A/V
POWER GOOD RESET GENERATOR						
VUV_{BUCKX}	Threshold voltage for buck under voltage	Output falling		85		%
		Output rising (PG will be asserted)		90		
$t_{UV\_deglitch}$	Deglitch time (both edges)			11		ms
t_{ON_HICCUP}	Hiccup mode ON time	VUV_{BUCKX} asserted		12		ms
t_{OFF_HICCUP}	Hiccup mode OFF time	All converters disabled. Once t_{OFF_HICCUP} elapses, all converters will go through sequencing again.		20		ms
VOV_{BUCKX}	Threshold voltage for buck over voltage	Output rising (high side FET will be forced off)		109		%
		Output falling (high side FET will be allowed to switch)		107		
t_{RP}	minimum reset period	Measured after the later of Buck1 or Buck3 power-up successfully		100		ms
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shut down trip point	Rising temperature		160		°C
T_{HYST}	Thermal shut down hysteresis	Device re-starts		20		°C
$T_{TRIP\_DEGLITCH}$	Thermal shut down deglitch			110		μs
USB SWITCHES						
VIN_{USB}	USB input voltage range		3		6	V
$V_{IH\_USB\_EN}$	USB_EN high level input voltage	V3p3 = 3.2-3.4 V, V_{USB_EN} rising	0.66 x V3p3			V
$V_{IL\_USB\_EN}$	USB_EN low level input voltage	V3p3 = 3.2-3.4 V, V_{USB_EN} falling			0.33 x V3p3	V
R_{DS_USB}	Static drain-source on-state resistance	USB_VIN = 5 V and Io_USB = 0.5 A, T_J = 25°C		120		mΩ
I_{CS_USB}	USB current limit	Increasing USB_Vo current di/dt<1 A/s		1.2		A
$K_{OVERCURRENT}$	Overcurrent detection factor Ratio of I_{LIM_START}/I_{CS_USB}	Increasing USB_Vo current di/dt< 1A/s VIN_{USB} = 5 V		1.5		
V_{USBx_nFAULT}	USBx_nFAULT output voltage low	I_{USB_ILIM} = 3 mA			0.4	V
T_{CS_USB}	USB over current fault deglitch	Fault assertion due to Over current protection		5		ms
T_{USB_TRIP}	USB thermal trip point	Rising temperature		130		°C
T_{USB_HYST}	USB thermal trip hysteresis	Falling temperature		20		°C

TYPICAL CHARACTERISTICS

Load Regulation: Buck1 @ 1.2V, 1% Resistor Feedback

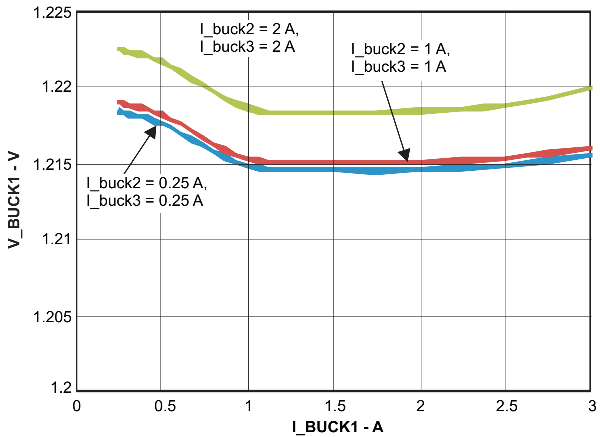


Figure 1.

Load Regulation: Buck2 @ 1.8V, 1% Resistor Feedback

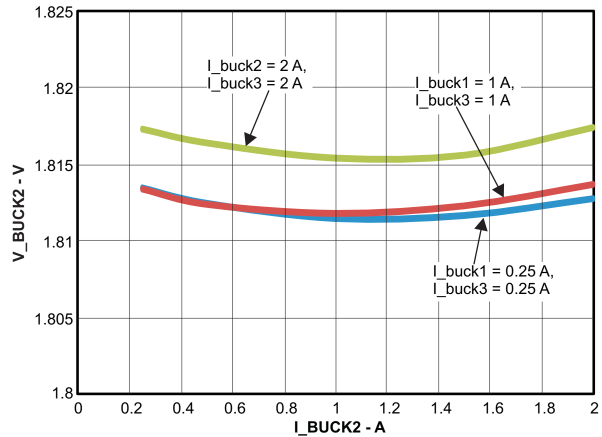


Figure 2.

Load Regulation: Buck3 @ 3.3V, 1% Resistor Feedback

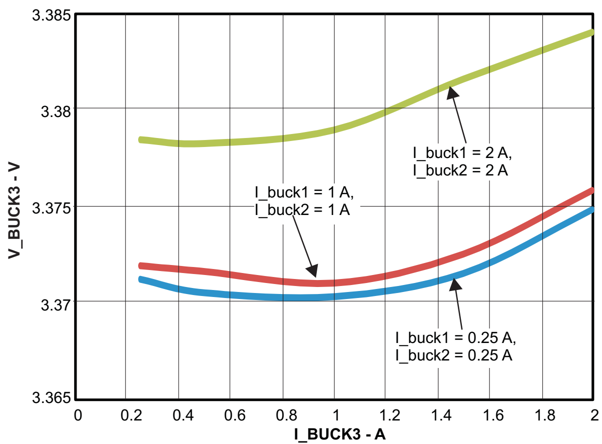


Figure 3.

Buck1 Temp Variation @ 1.2V, 1%Resistor
-40°C to 75°C, Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

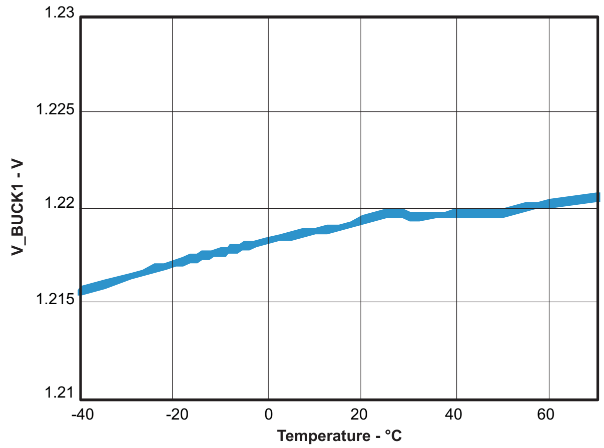


Figure 4.

Current Limit Variation 25°C,
RLIM1 = 100kΩ, RLIM2&3 = 120kΩ

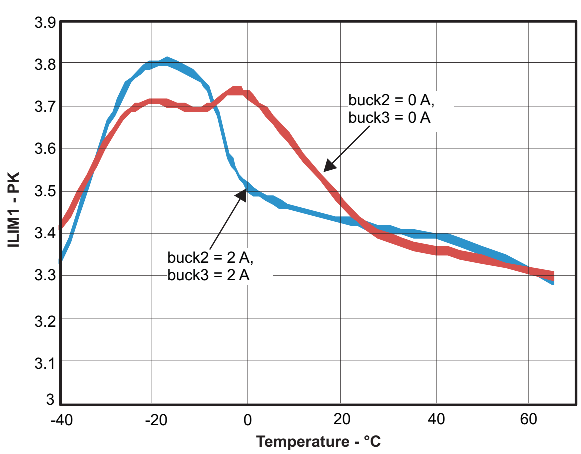


Figure 5.

Buck1 1.2V Efficiency, Forced PWM
L = 4.7μH, 20mΩ, f_{SW} = 500KHz

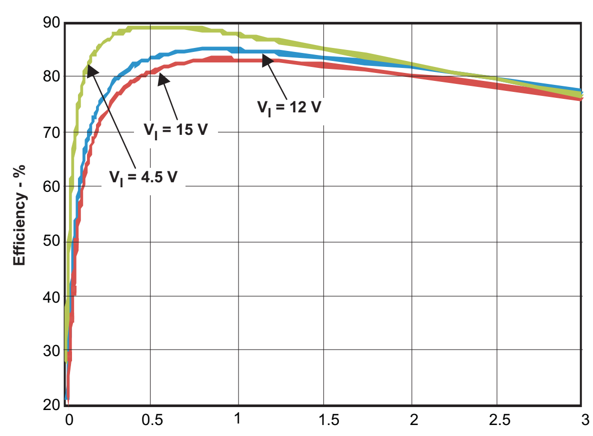


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Buck1 1.2V Efficiency, Forced PWM and PFM
L = 4.7μH, 20mΩ, f_{SW} = 500KHz

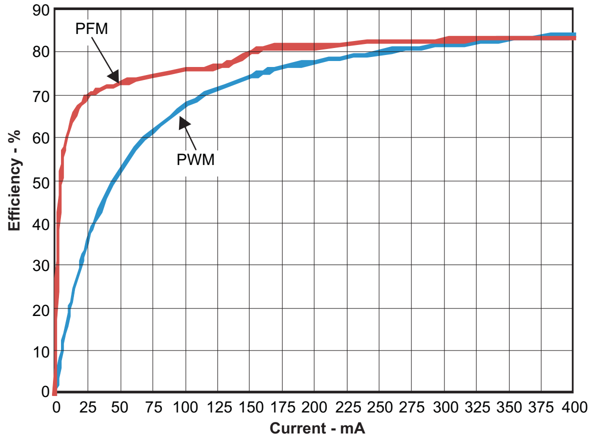


Figure 7.

Buck2 1.8V Efficiency, Forced PWM
L = 4.7μH, 20mΩ, f_{SW} = 500KHz

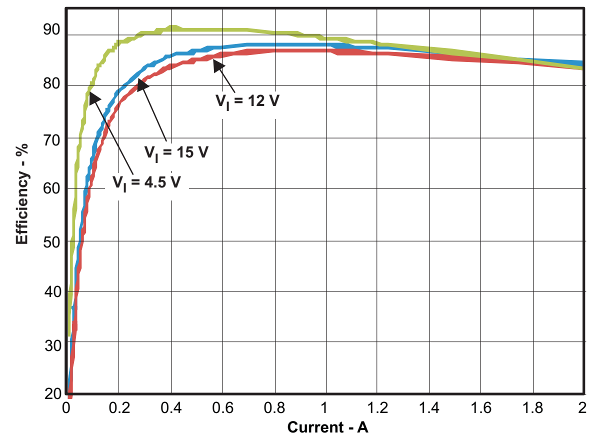


Figure 8.

Buck2 1.8V Efficiency, Forced PWM and PFM
L = 4.7μH, 20mΩ, f_{SW} = 500KHz

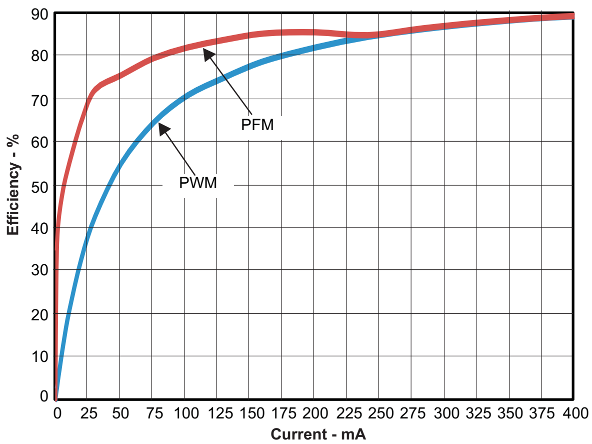


Figure 9.

Buck3 3.3V Efficiency, Forced PWM
L = 4.7μH, 20mΩ, f_{SW} = 500KHz

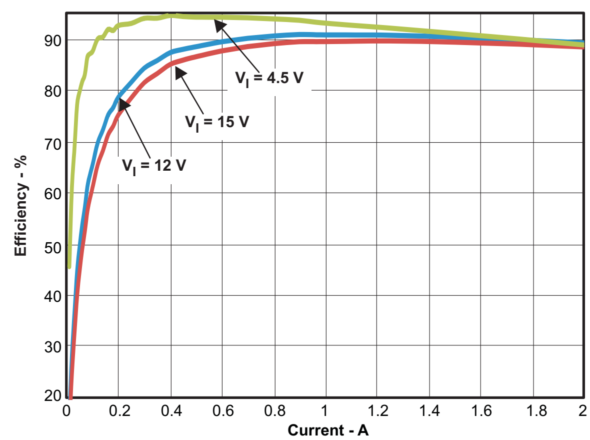


Figure 10.

Buck3 3.3V Efficiency, Forced PWM and PFM
L = 4.7μH, 20mΩ, f_{SW} = 500KHz

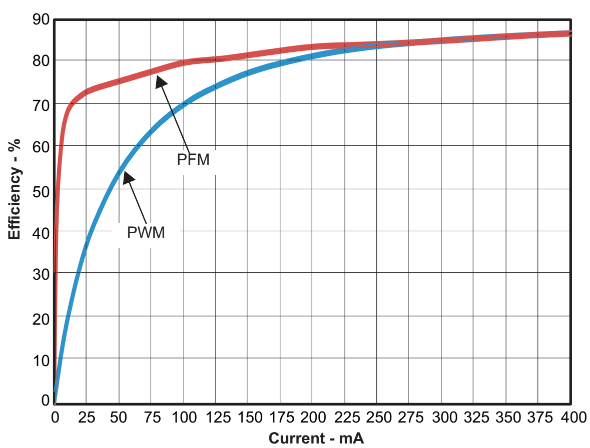


Figure 11.

Power-Up All Converters, No Load V_{IN} = 12V (Green)

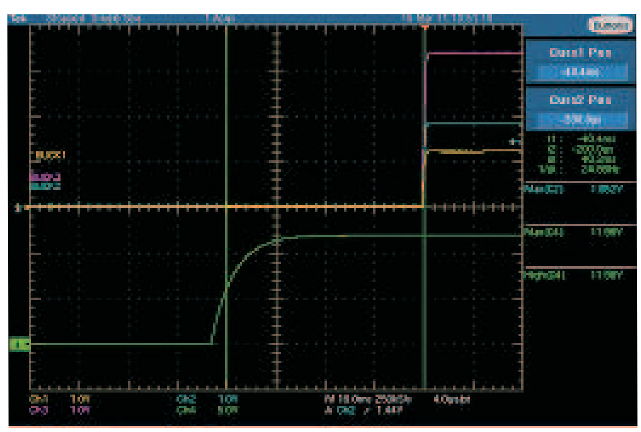


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Power-Up All Converters and PGOOD (Green), No Load

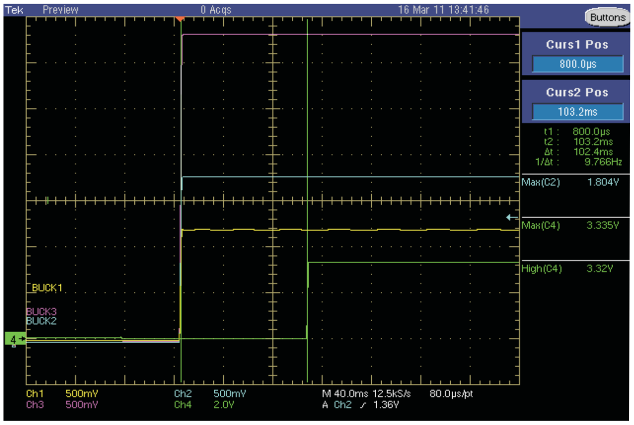


Figure 13.

Detail of Start-Up 4.7nF Fitted to All Enable Pins

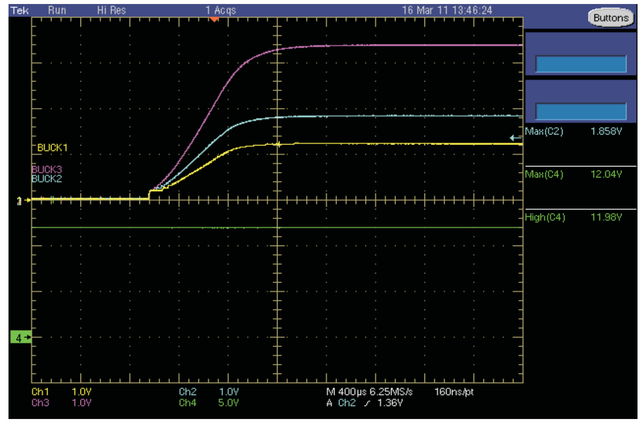


Figure 14.

Ripple T_A = 25°C, Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

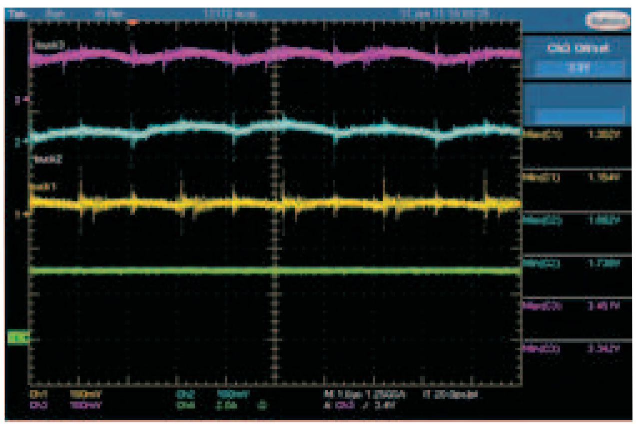


Figure 15.

Ripple T_A = 70°C, Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

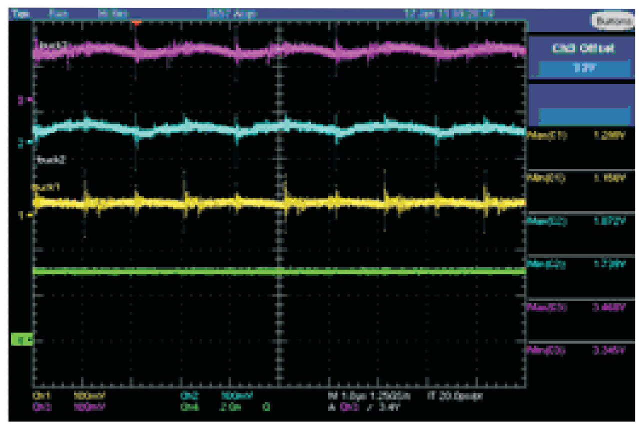


Figure 16.

Ripple T_A = 10°C, Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

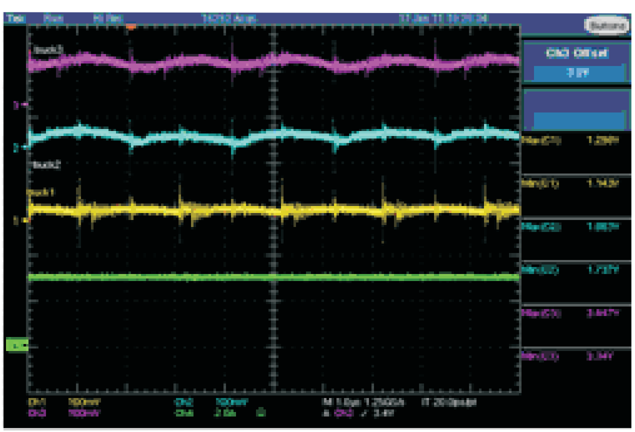


Figure 17.

Ripple T_A = 40°C, Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

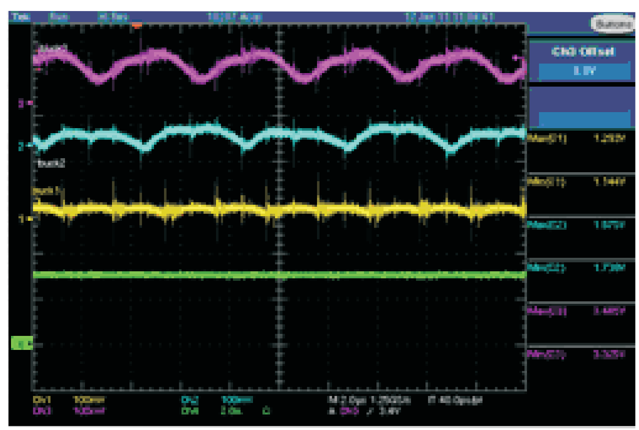


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Transient Response Buck1
1.2V, 1-3A Step, Co = 22μF,L = 4.7μH, f_{SW} = 500KHz

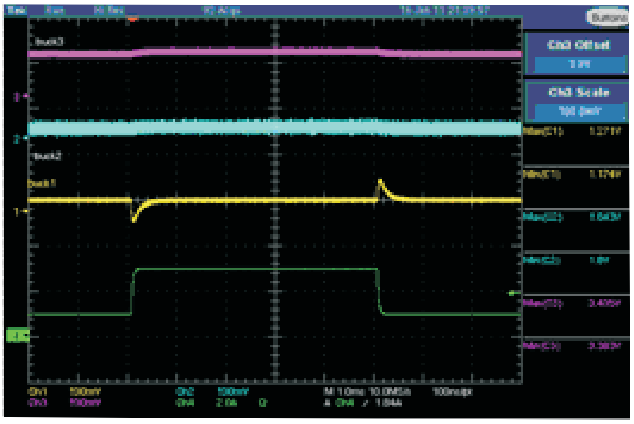


Figure 19.

Transient Response Buck2
1.8V, 1-2A Step, Co = 22μF,L = 4.7μH, f_{SW} = 500KHz

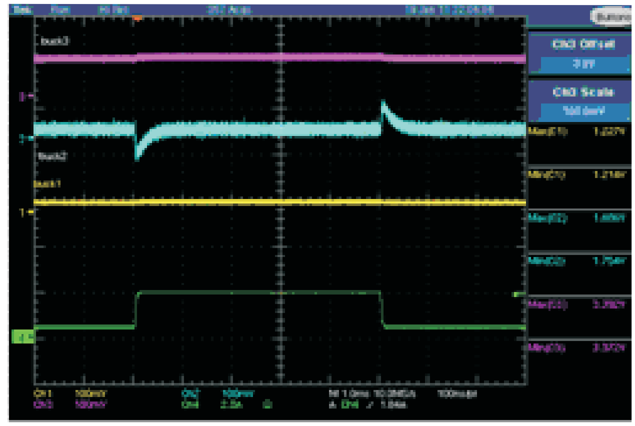


Figure 20.

Buck3 3.3V Efficiency Measured With L = 4.7μH, 20mΩ, f_{SW} = 500kHz

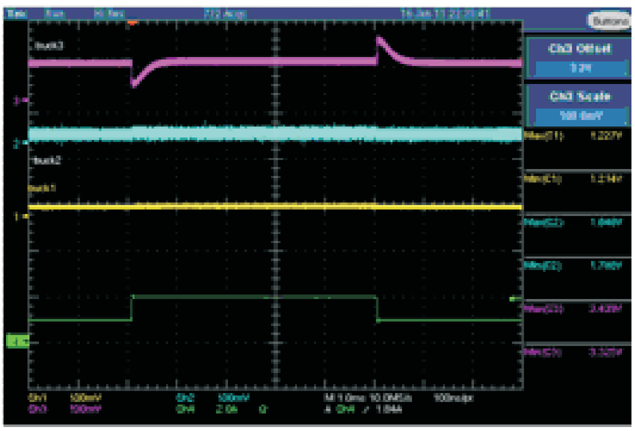


Figure 21.

PFM Operation 1.2V, 1.8V, 3.3V

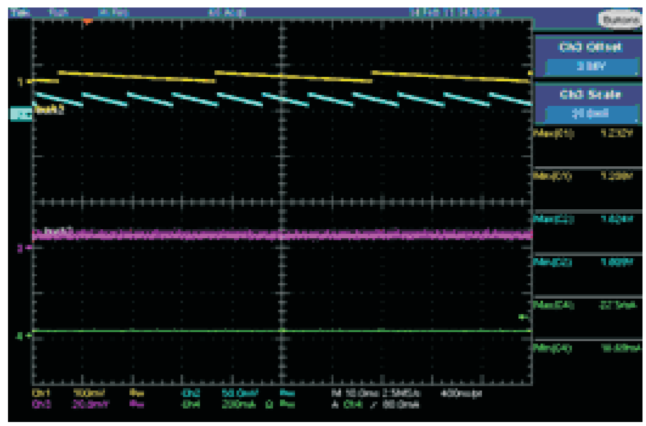


Figure 22.

PFM/PWM Transition (Pin 25 Pulled High)

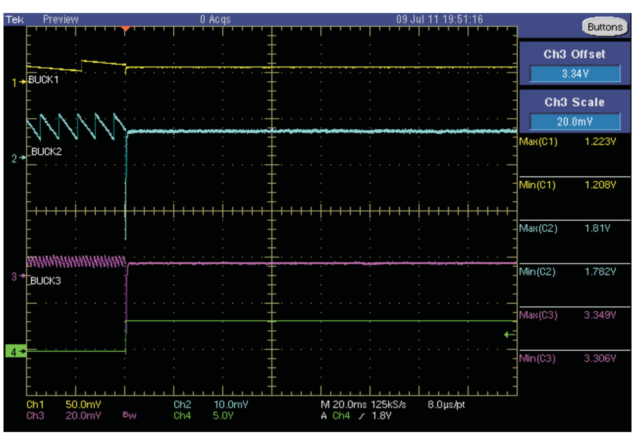


Figure 23.

PFM/PWM Transition (Pin 25 Pulled Low)

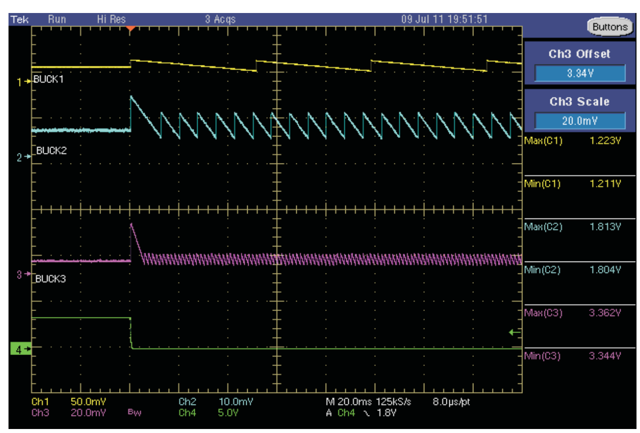


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Buck1 Dynamic Transition from PFM to PWM
4.7μH, 44μF, 500 kHz

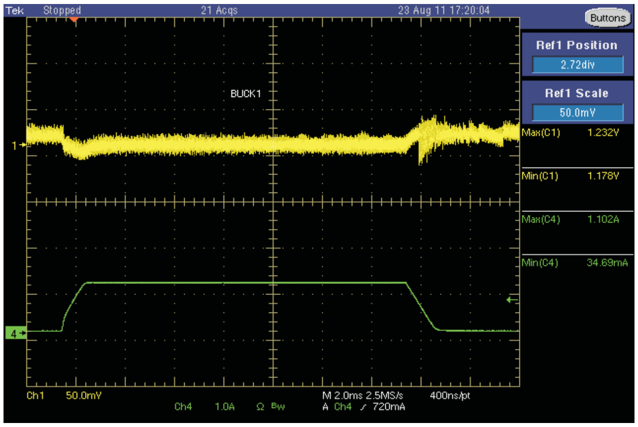


Figure 25.

Buck2 Dynamic Transition from PFM to PWM
4.7μH, 44μF, 500 kHz

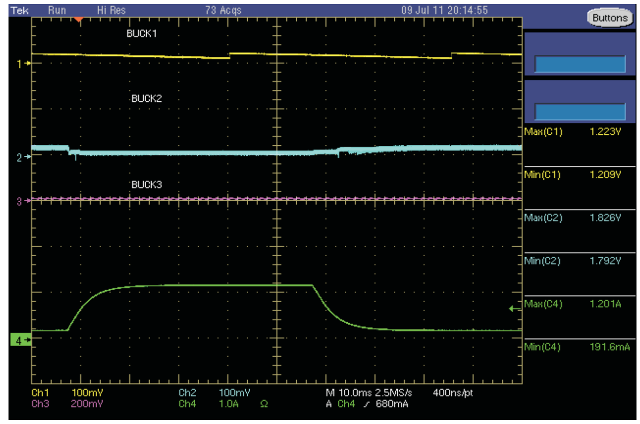


Figure 26.

Buck3 Dynamic Transition from PFM to PWM
4.7μH, 22μF, 500 kHz

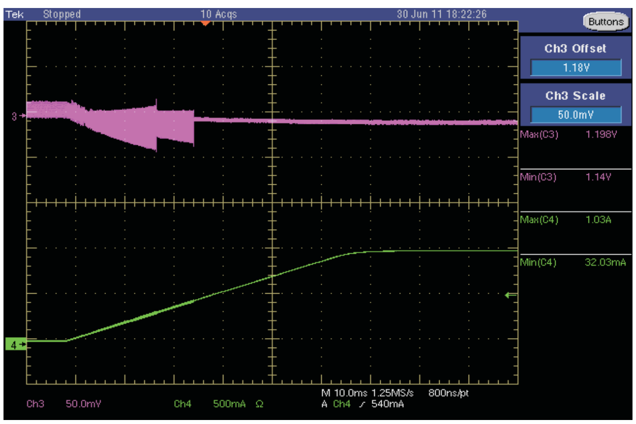


Figure 27.

USB Switch Start-Up No Load

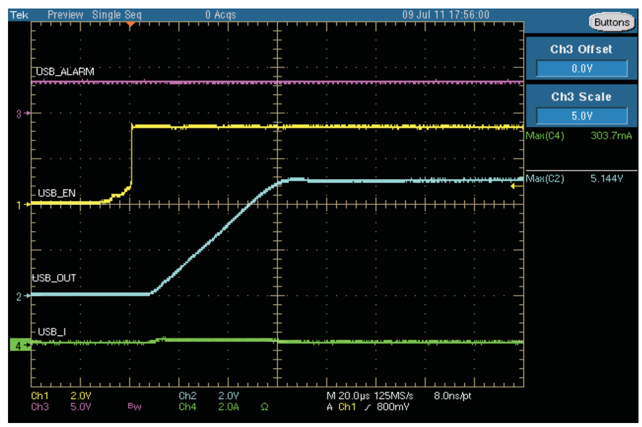


Figure 28.

USB Switch Start-Up No Load

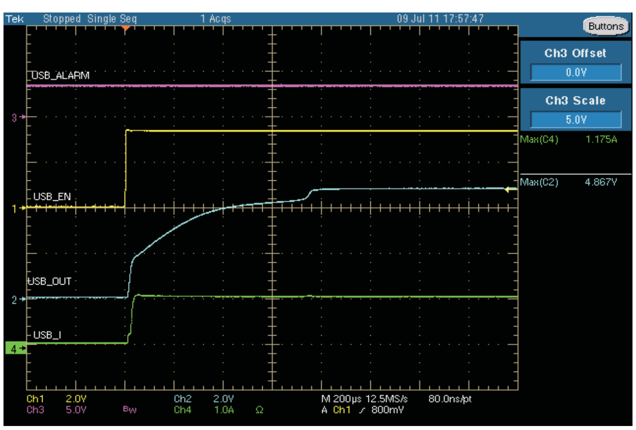


Figure 29.

USB Current Limit Operation (3.3 V)

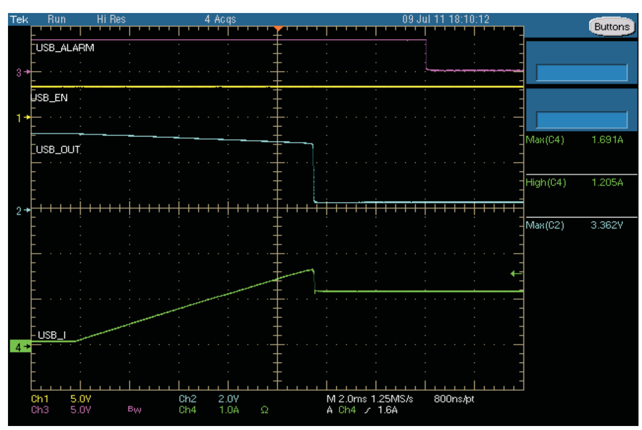


Figure 30.

TYPICAL CHARACTERISTICS (continued)

USB Current Limit Recovery (3.3 V)

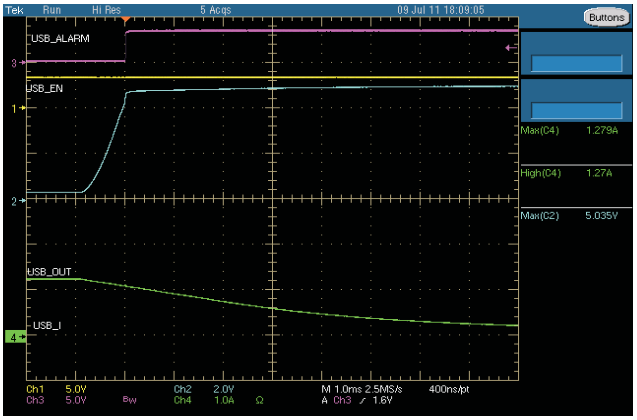


Figure 31.

USB Current Limit Operation (5 V)

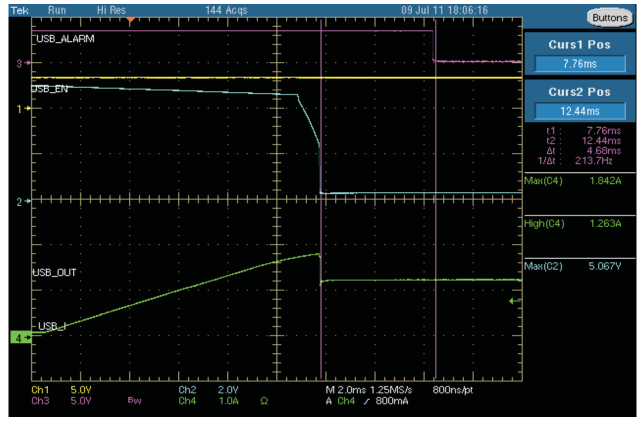


Figure 32.

USB Current Limit Recovery (5 V)

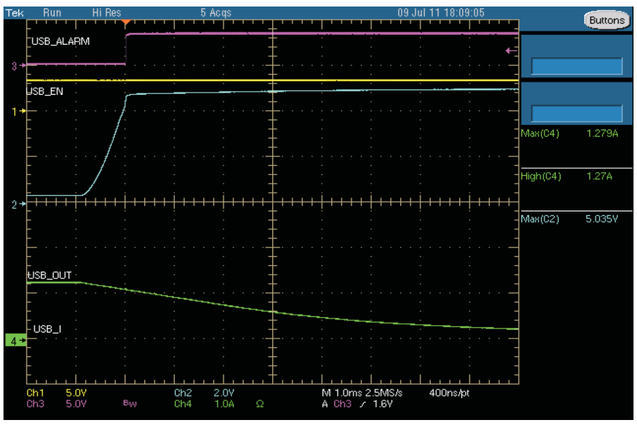


Figure 33.

Bucks Operation (Top 3 Traces) and USB Alarm Operation

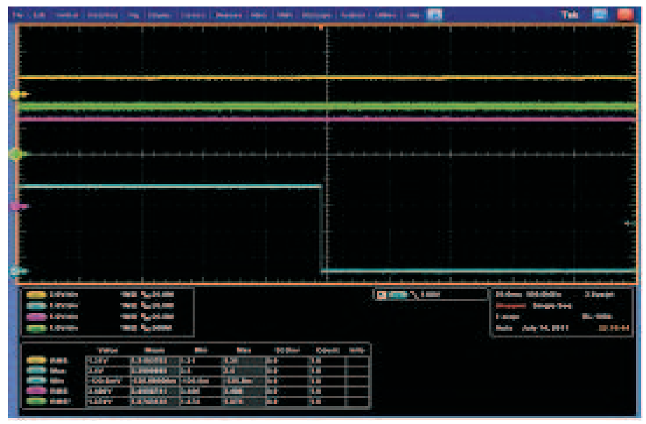


Figure 34.

EVM Layout

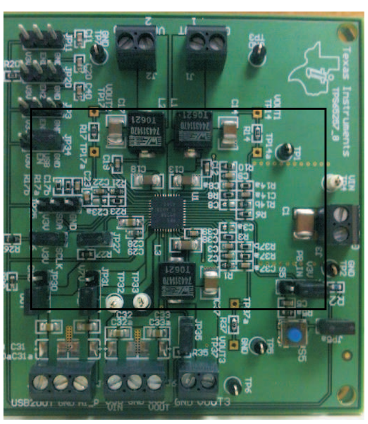


Figure 35.

T_A = 25°, V_{IN} = 12V, f_{SW} = 500kHz
B1 = 3A, B2 = 2A, B3 = 2A

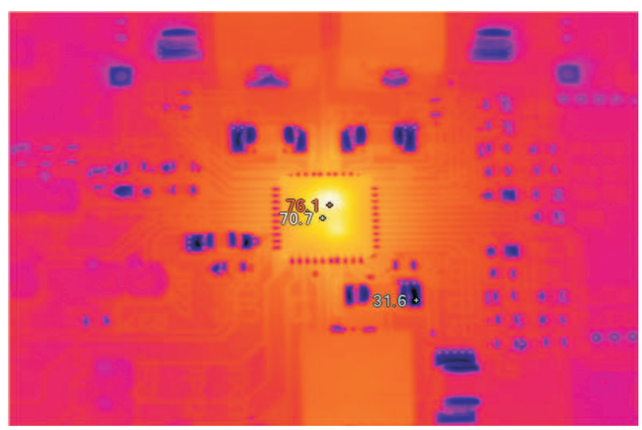


Figure 36.

TYPICAL CHARACTERISTICS (continued)

**T_A = 25°, V_{IN} = 5V, f_{SW} = 500kHz
B1 = 3A, B2 = 2A, B3 = 2A**

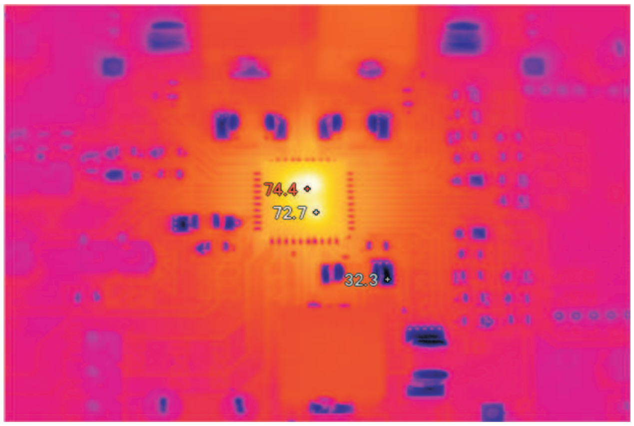


Figure 37.

**T_A = 25°, V_{IN} = 5V, f_{SW} = 1000kHz
B1 = 3A, B2 = 2A, B3 = 2A**

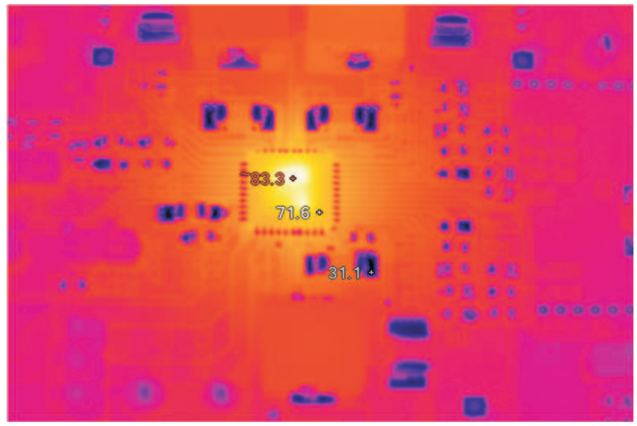


Figure 38.

DETAILED DESCRIPTION

Adjustable Switching Frequency

To select the internal switching frequency, connect a resistor from ROSC to ground. Figure 39 shows the required resistance for a given switching frequency.

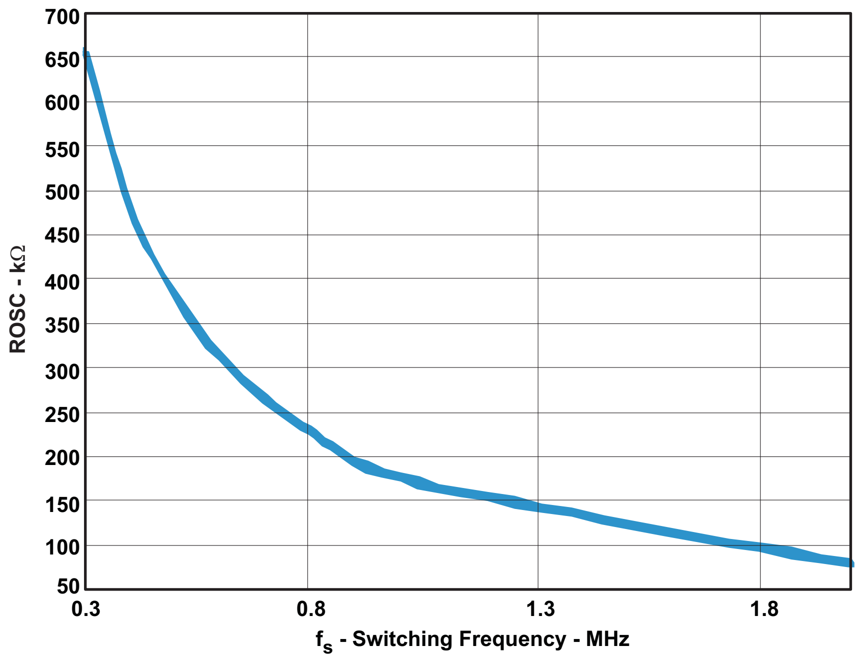


Figure 39. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 174 \bullet f_{SW}^{-1.122} \quad (1)$$

Output Inductor Selection

To calculate the value of the output inductor, use Equation 2.

$$Lo = \frac{Vin - Vout}{Io \cdot K_{ind}} \cdot \frac{Vout}{Vin \cdot fsw} \tag{2}$$

K_{ind} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, K_{ind} is normally from 0.1 to 0.3 for the majority of applications. A value of 0.1 will improve the efficiency at light load, while a value of 0.3 will provide the lowest possible cost solution. The ripple current is:

$$Iripple = \frac{Vin - Vout}{Lo} \cdot \frac{Vout}{Vin \cdot fsw} \tag{3}$$

Output Capacitor

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements. If a minimum transient specification is required use the following equation:

$$Co > \frac{\Delta I_{OUT}{}^{2} \cdot L_o}{V_{out} \cdot \Delta Vout} \tag{4}$$

The following equation calculates the minimum output capacitance needed to meet the output voltage ripple specification.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{V_{RIPPLE}}{V_{RIPPLE}}} \tag{5}$$

Where f_{SW} is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and V_{RIPPLE} is the inductor ripple current.

Input Capacitor

A minimum 10-μF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND of each converter. The input capacitor must handle the RMS ripple current shown in the following equation.

$$Icirms = Iout \cdot \sqrt{\frac{Vout}{Vin\min} \cdot \frac{(Vin\min - Vout)}{Vin\min}} \tag{6}$$

Bootstrap Capacitor

The device has two integrated boot regulators and requires a small ceramic capacitor between the BST and LX pins to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.047 μF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

Soft-Start Time

The device has an internal pull-up current source of 5 μA that charges an external soft-start capacitor to implement a slow start time. Equation 7 shows how to select a soft-start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8 V and the soft-start charge current (I_{SS}) is 5 μA. The soft-start circuit requires 1 nF per around 167 μs to be connected at the SS pin. A 0.8-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant SS pin.

$$T_{ss}(ms) = V_{REF}(V) \bullet \left(\frac{C_{ss}(nF)}{I_{ss}(\mu A)} \right) \tag{7}$$

The Power Good circuit for the bucks has a 10-ms watchdog. Therefore the soft-start time should be lower than this value. It is recommended not to exceed 5 ms.

Delayed Start-Up

If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is ~1.67 ms per nF connected to the pin. Note that the EN pins have a weak 1-MΩ pull-up to the 3V3 rail.

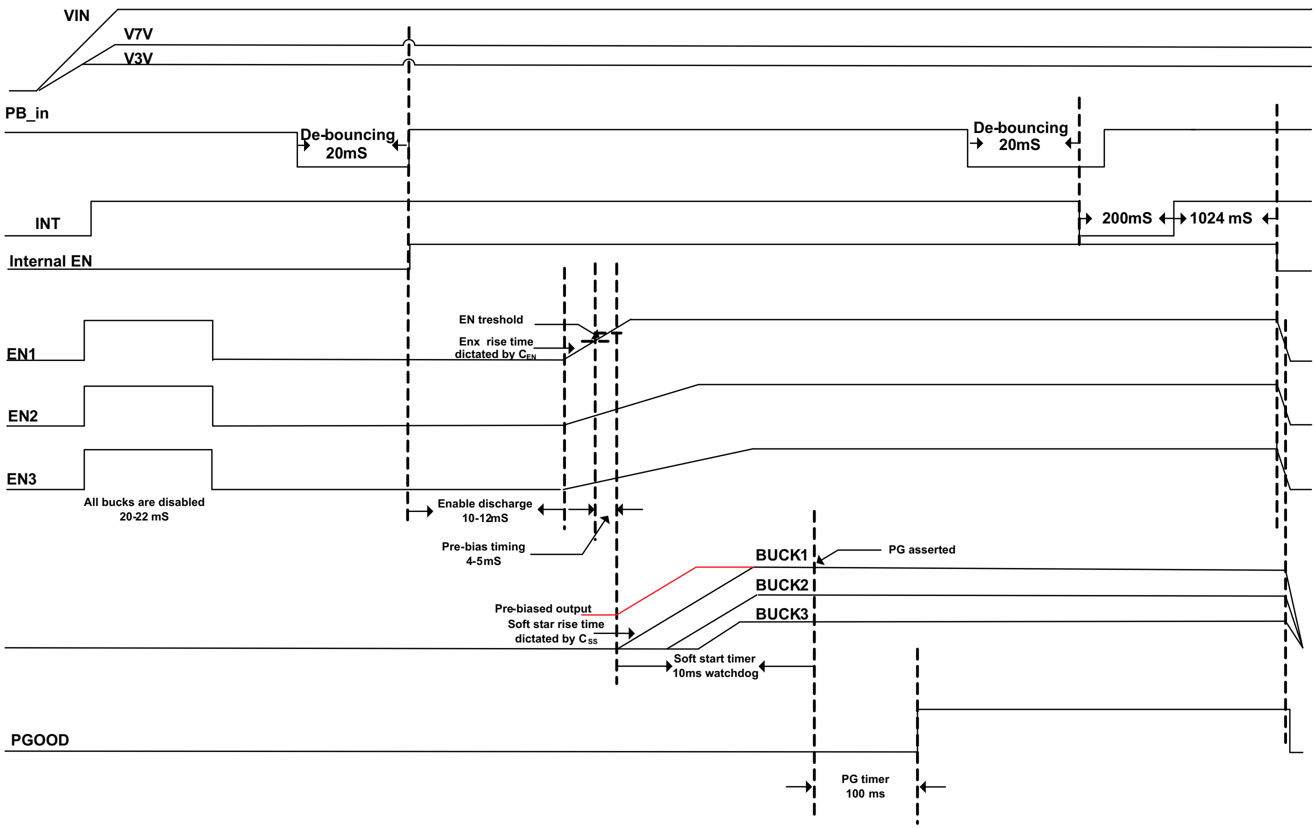


Figure 40. Delayed Start-Up

Out-of-Phase Operation

In order to reduce input ripple current, Buck1 and Buck2 operate 180° out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with a value close to 40 kΩ for the R1 resistor and use Equation 8 to calculate R2.

$$R2 = R1 \cdot \left(\frac{0.8V}{V_O - 0.8V} \right) \tag{8}$$

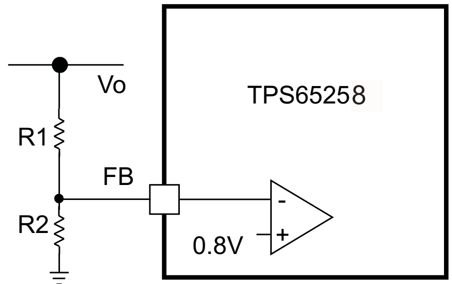


Figure 41. Voltage Divider Circuit

Loop Compensation

TPS65258 is a current mode control DC/DC converter. The error amplifier is a transconductance amplifier with a g_M of 130 μA/V. A typical compensation circuit could be type II (R_c and C_c) to have a phase margin between 60° and 90°, or type III (R_c and C_c and C_{ff} to improve the converter transient response. C_{Roll} adds a high frequency pole to attenuate high-frequency noise when needed. It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

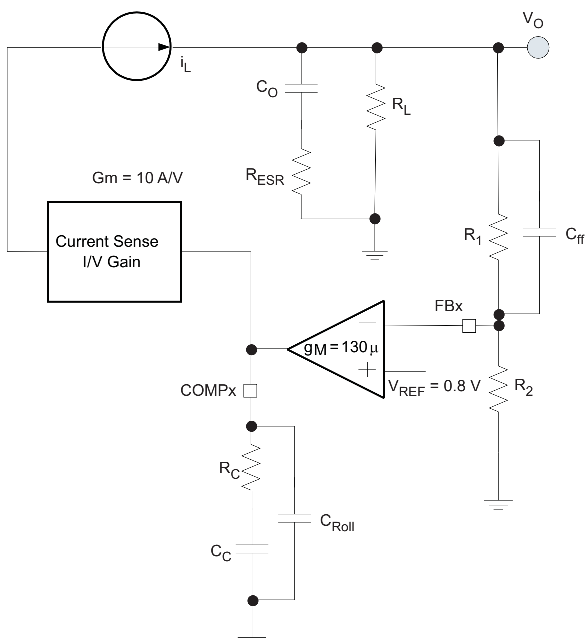


Figure 42. Loop Compensation Scheme

To calculate the external compensation components follow the following steps:

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies around 500 kHz yield best trade off between performance and cost. When using smaller L and C, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Use type III circuit for switching frequencies higher than 500 kHz.
Select cross over frequency (f_c) to be at least 1/5 to 1/10 of switching frequency (f_s).	Suggested $f_c = f_s/10$	Suggested $f_c = f_s/10$
Set and calculate R_c.	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$
Calculate C_c by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}$	$C_c = \frac{R_L \cdot Co}{R_c}$	$C_c = \frac{R_L \cdot Co}{R_c}$
Add C_{Roll} if needed to remove large signal coupling to high impedance CMP node. Make sure that $fp_{Roll} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_{Roll}}$ is at least twice the cross over frequency.	$C_{Roll} = \frac{\mathrm{Re}\,sr \cdot Co}{R_C}$	$C_{Roll} = \frac{\mathrm{Re}\,sr \cdot Co}{R_C}$
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff}) is smaller than equivalent soft-start frequency ($1/T_{ss}$).	NA	$C_{ff} = \frac{1}{2 \cdot \pi \cdot fz_{ff} \cdot R_1}$

Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control.

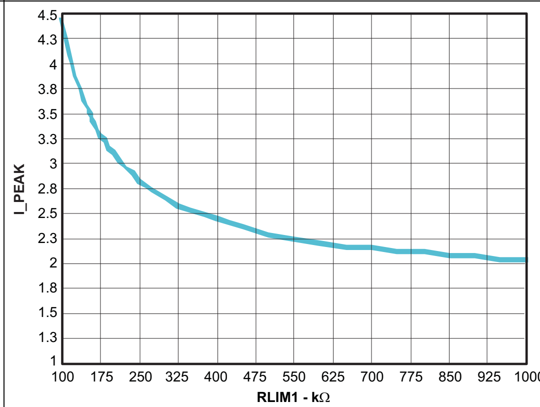
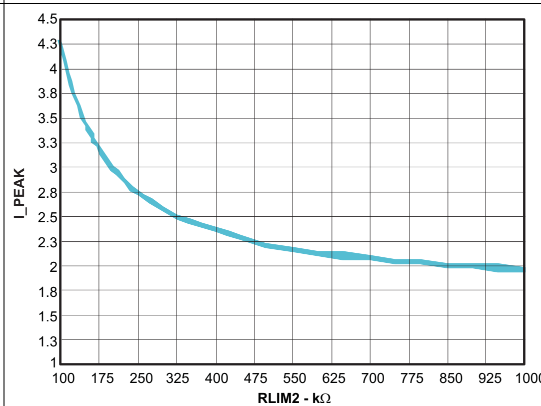
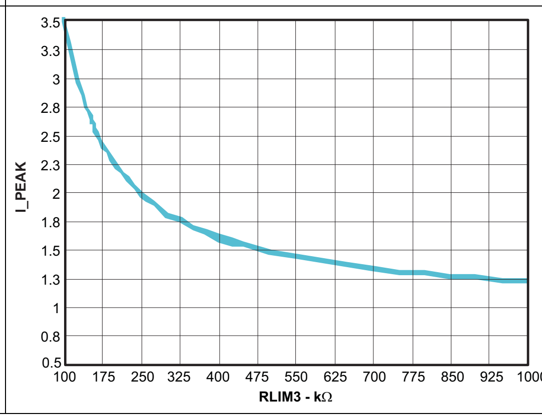
Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when both buck converters’ outputs are more than 90% of its nominal output voltage.

The default reset time is 100 ms. The polarity of the PGOOD is active high.

Current Limit Protection

The TPS65258 current limit trip is set by the following formulae:

	TYPE II CIRCUIT
$$I_{LIM1}(A) = \frac{267}{RLIM1(k\Omega)} + 1.77 \quad (9)$$	
$$I_{LIM2}(A) = \frac{256}{RLIM1(k\Omega)} + 1.72 \quad (10)$$	
$$I_{LIM3}(A) = \frac{253}{RLIM2(k\Omega)} + 0.97 \quad (11)$$	

All converters operate in hiccup mode: Once an over-current lasting more than 10 ms is sensed in any of the converters, they will shut down for 10 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

If an overload condition lasts for less than 10 ms, only the relevant converter affected will shut-down and re-start and no global hiccup mode will occur.

Overvoltage Transient Protection

The device incorporates an overvoltage transient protection (OVP) circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold which is 107%, the high side MOSFET is allowed to turn on the next clock cycle.

Low Power/Pulse Skipping Operation

When a buck synchronous converter operates at light load or standby conditions, the switching losses are the dominant source of power losses. Under these load conditions, TPS65258 uses a pulse skipping modulation technique to reduce the switching losses by keeping the power transistors in the off-state for several switching cycles, while maintaining a regulated output voltage. Figure 43 shows the output voltage and load plus the inductor current.

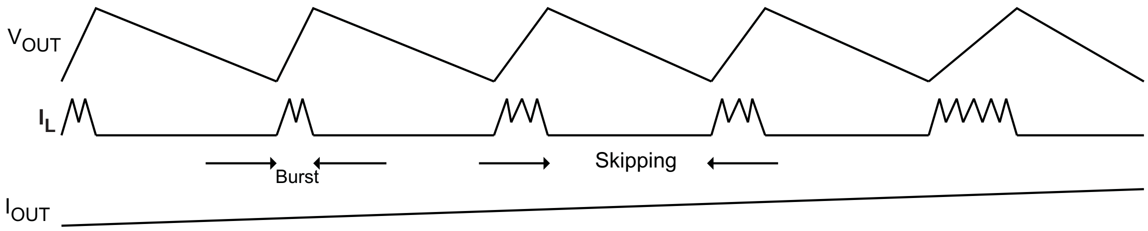


Figure 43. Low Power/Pulse Skipping

During the burst mode, the converter continuously charges up the output capacitor until the output voltage reaches a certain limit threshold. The operation of the converter in this interval is equivalent to the peak inductor current mode control. In each switch period, the main switch is turned on until the inductor current reaches the peak current limit threshold. As the load increases the number of pulses increases to make sure that the output voltage stays within regulation limits. When the load is very light the low power controller has a zero crossing detector to allow the low side mosfet to operate even in light load conditions. The transistor is not disabled at light loads. A zero crossing detection circuit will disable it when inductor current reverses. During the whole process the body diode does not conduct but is used as blocking diode only.

During the skipping interval, the upper and lower transistors are turned off and the converter stays in idle mode. The output capacitors are discharged by the load current until the moment when the output voltage drops to a low threshold.

The choice of output filter will influence the performance of the low power circuit. The maximum ripple during low power mode can be calculated as:

$$V_{OUT\_RIPPLE} = \frac{K_{RIP} T_S}{C_{OUT}} \tag{12}$$

Where K_{RIP} is 1.4 for Buck1 and 0.7 for Buck2 and Buck3. TS can be calculated as:

$$T_S = \frac{0.35}{\left[\left(\frac{V_{IN} - V_{OUT}}{L}\right)\frac{V_{OUT}}{V_{IN}}\right]} \tag{13}$$

USB Switches

The USB switches are enabled (active high) with the USB_ENx pin. The switches have a typical resistance of 120 mΩ and has a fold-back current limit that is typically 25% lower than the overcurrent detection point. If a continuous short-circuit condition is applied to one USB switch output, the USB switches will shut-down once its temperature reaches 130°C, allowing for the buck converters to operate unaffected. Once the USB switch cools down it will restart automatically.

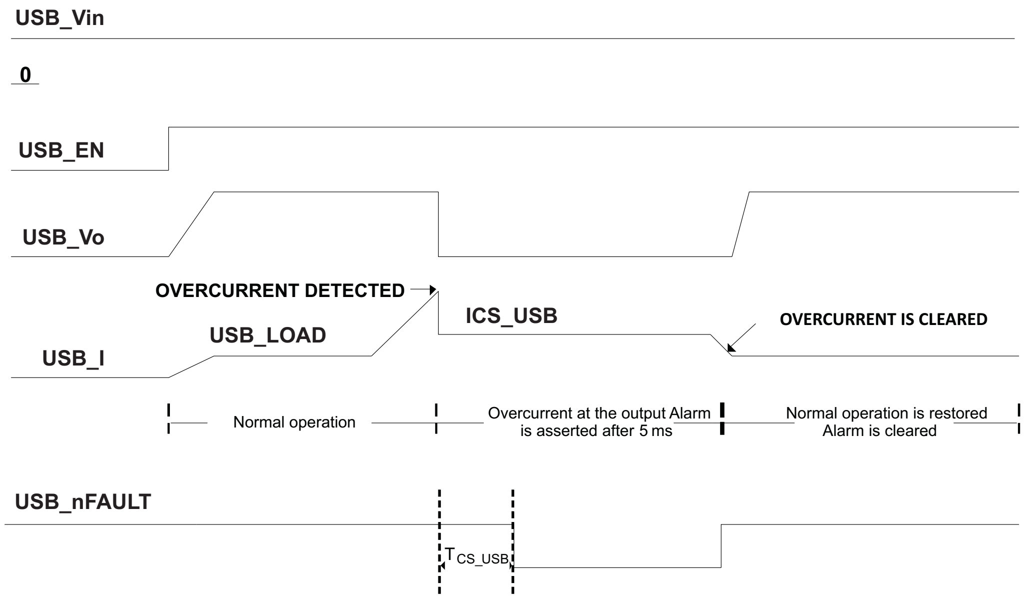


Figure 44. USB Switches

The USB switches are single sided without back-fed protection but the 2 USB switches of TPS65258 can be configured as a back to back switch.

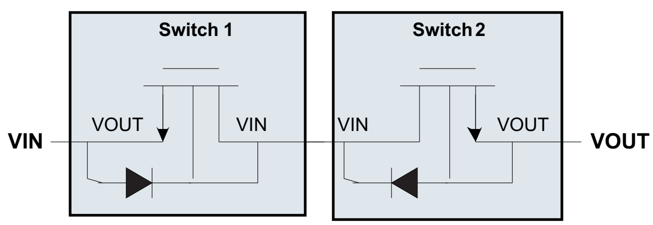
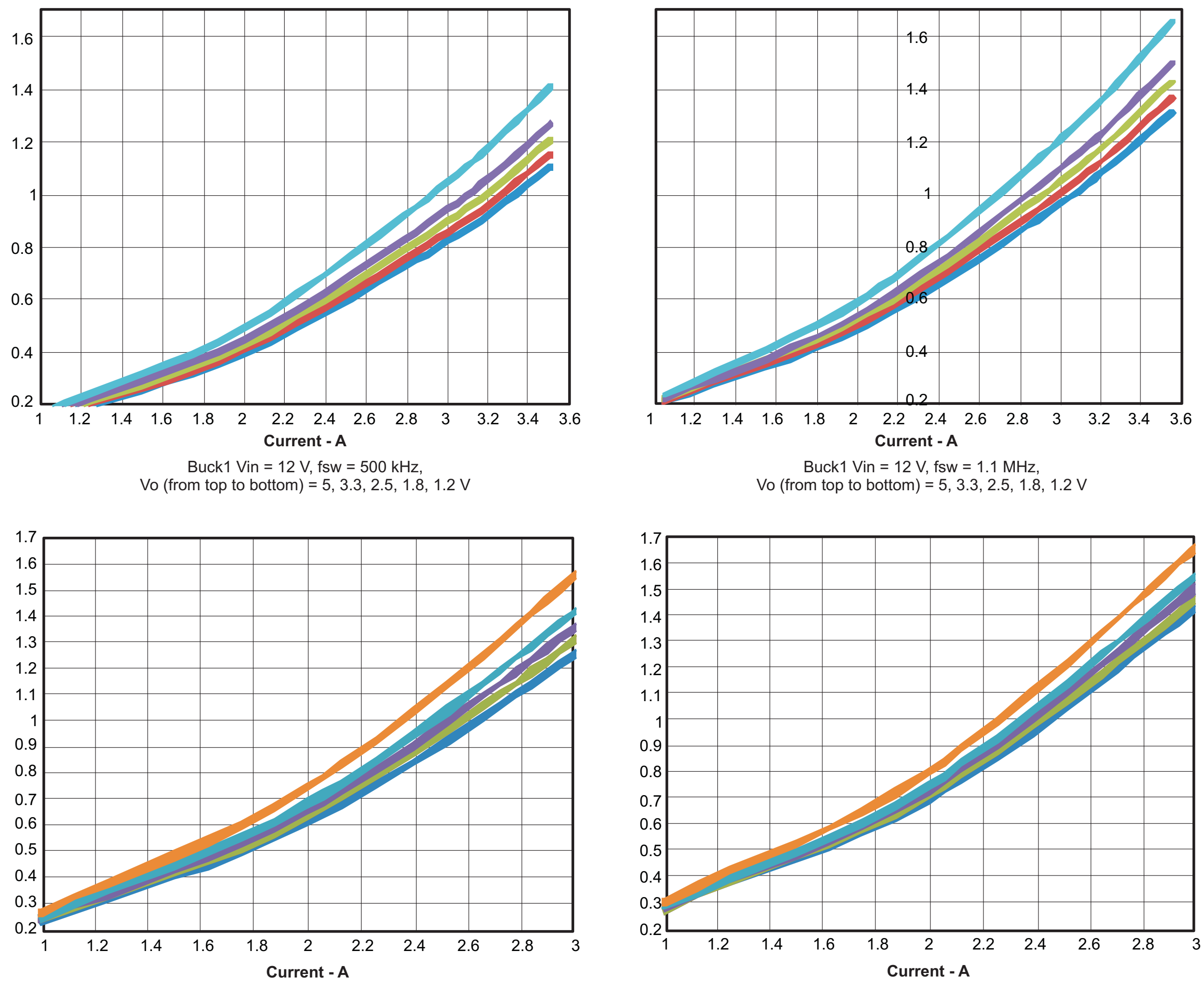


Figure 45. Back to Back Switch

Power Dissipation

The total power dissipation inside TPS65258 should not to exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package (R_{JA}) and ambient temperature. To calculate the temperature inside the device under continuous loading use the following procedure:

1. Define the set voltage for each converter.
2. Define the continuous loading on each converter. Make sure do not exceed the converter maximum loading..
3. Determine from the graphs below the expected losses in watts per converter inside the device. The losses depend on the input supply, the selected switching frequency, the output voltage and the converter chosen.



Buck1 Vin = 12 V, fsw = 500 kHz, Vo (from top to bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

Buck1 Vin = 12 V, fsw = 1.1 MHz, Vo (from top to bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

Buck2&3 Vin = 12 V, fsw = 500 kHz, Vo (from top to bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

Buck2&3 Vin = 12 V, fsw = 1.1 MHz, Vo (from top to bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

Figure 46. Power Dissipation Curves

4. Add additional losses due to the operation of the USB switches.
5. To calculate the maximum temperature inside the IC use the following formula:

$$T_{HOT\_SPOT} = T_A + P_{DIS} \times \Theta_{JA} \quad (14)$$

Where:

T_A is the ambient temperature

P_{DIS} is the sum of losses in all converters

Θ_{JA} is the junction to ambient thermal impedance of the device and it is heavily dependant on board layout

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

3.3-V and 6.5 LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 4.7 µF to 10 µF for V7V pin 28
- 3.3 µF or larger for V3V pin 29

Layout Recommendation

Layout is a critical portion of PMIC designs.

- Place tracing for output voltage and LX on the top layer and an inner power plane for VIN.
- Fit also on the top layer connections for the remaining pins of the PMIC and a large top side area filled with ground.
- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65258 device to provide a thermal path from the PowerPad land to ground.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the CMPx pins. The CMPx and ROSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65258RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65258	Samples
TPS65258RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65258	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

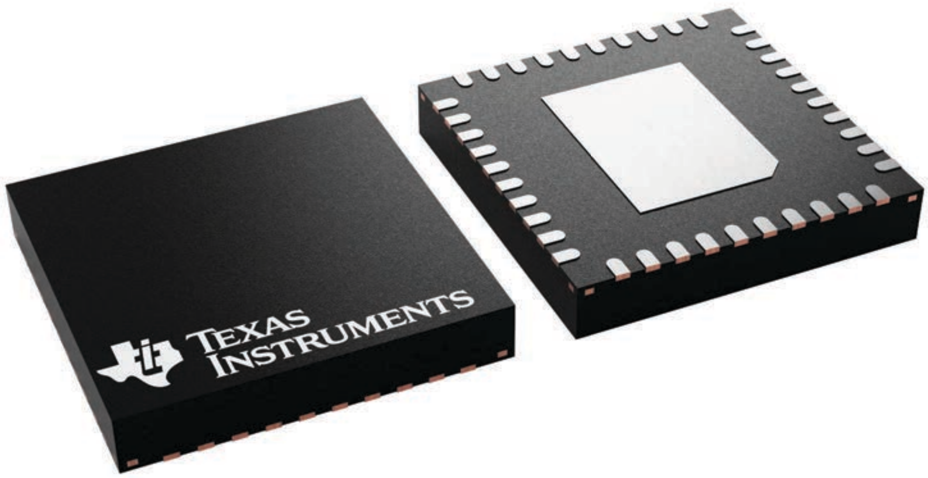
RHA 40

VQFN - 1 mm max height

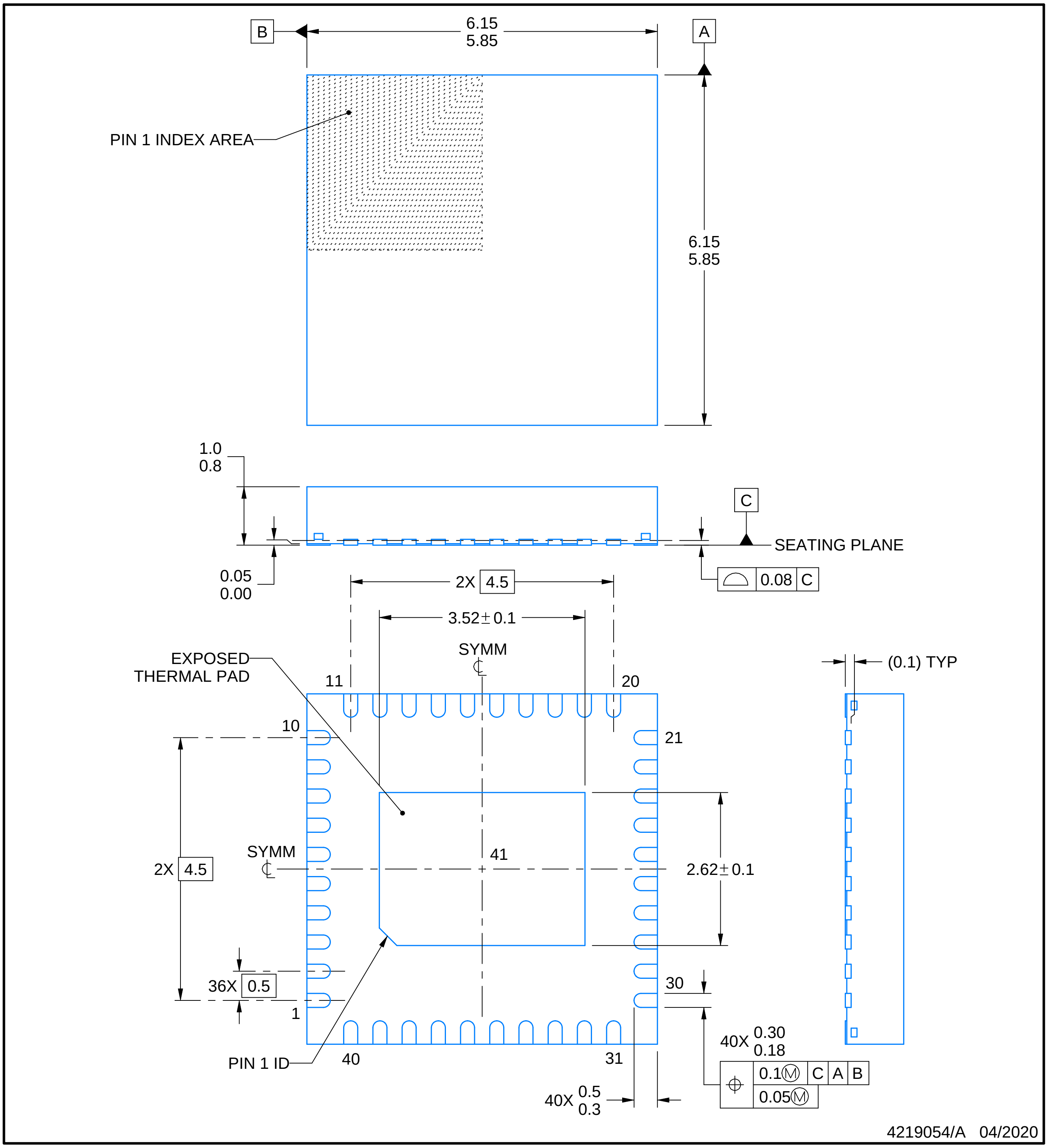
6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

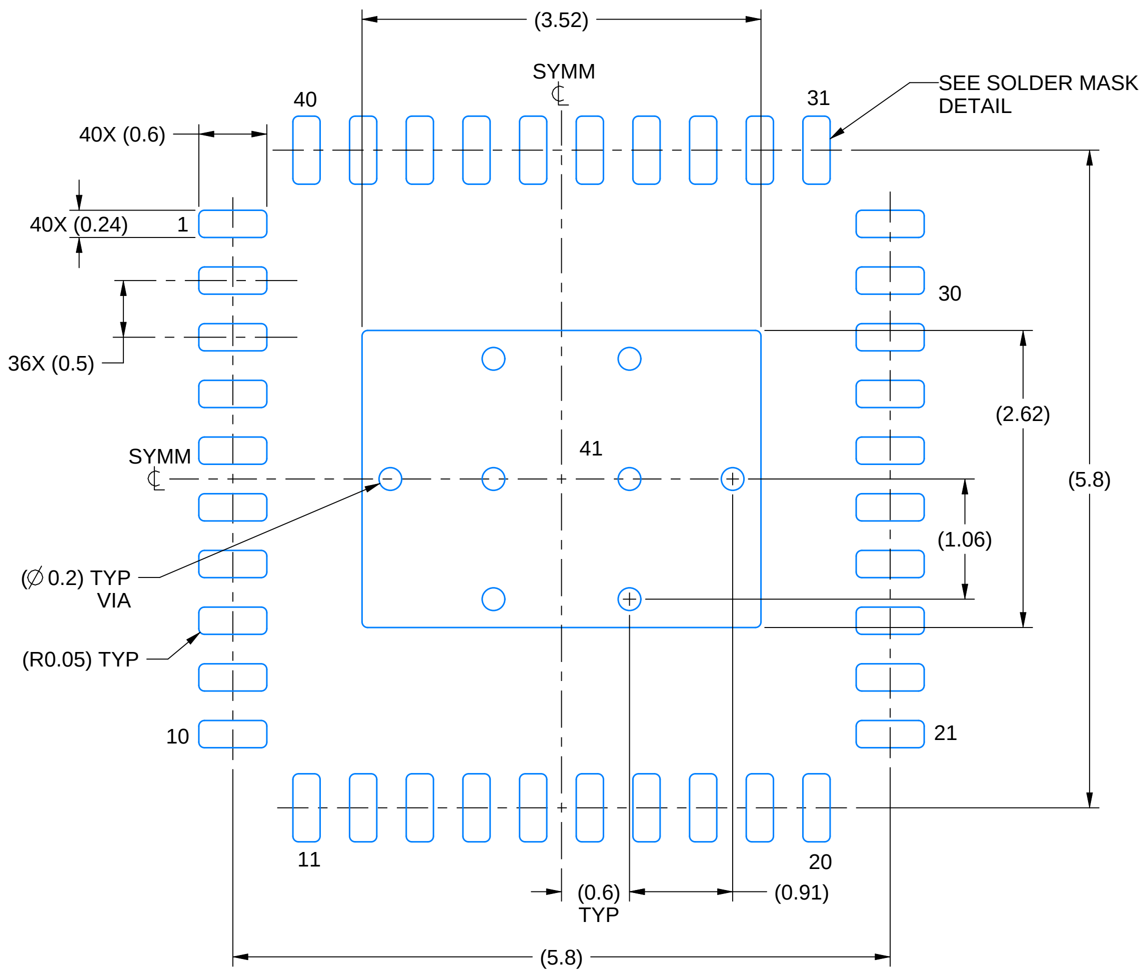


4225870/A

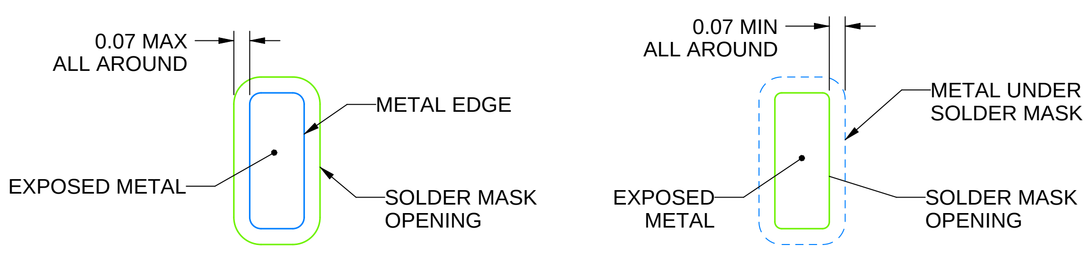


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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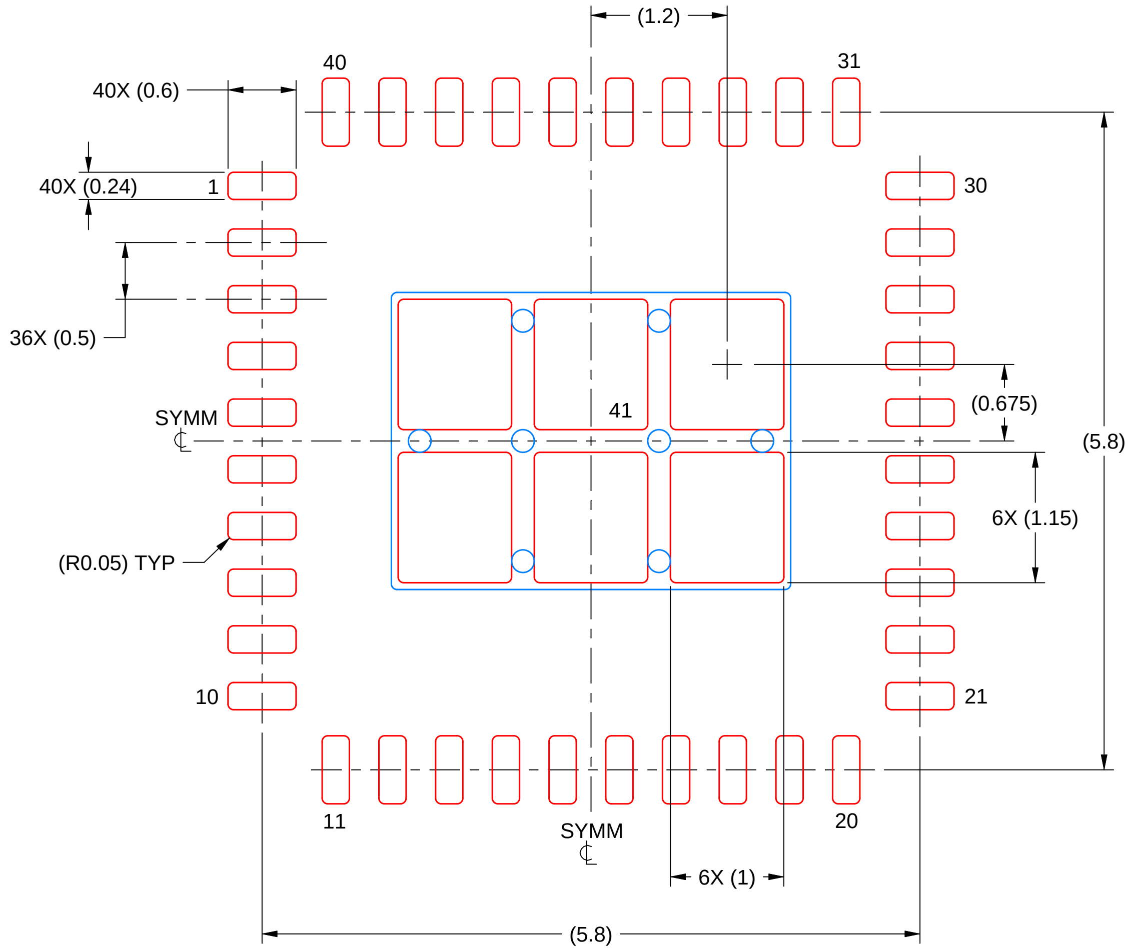
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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