

TPS22924x 3.6V、2A、导通电阻为 18.3mΩ 的负载开关

1 特性

- 集成单负载开关
- 输入电压: 0.75V 至 3.6V
- 导通电阻
 - $V_{IN} = 3.6V$ 时, $R_{ON} = 18.3m\Omega$
 - $V_{IN} = 1.8V$ 时, $R_{ON} = 19.6m\Omega$
 - $V_{IN} = 1.2V$ 时, $R_{ON} = 19.4m\Omega$
 - $V_{IN} = 0.75V$ 时, $R_{ON} = 22.7m\Omega$
- 小型芯片比例 (CSP)-6 封装
0.9mm x 1.4mm、0.5mm 间距
- 2A 最大持续开关电流
- 低关断电流
- 低阈值控制输入
- 受控转换率以避免涌入电流
- 快速输出放电晶体管
- 静电放电 (ESD) 性能测试符合 JESD 22 标准
 - 5000V 人体放电模式 (A114-B, II 类)
 - 1000V 组件充电模式 (C101)

2 应用

- 电池供电类设备
- 便携式工业设备
- 便携式医疗设备
- 便携式媒体播放器
- 销售点终端
- 全球卫星定位 (GPS) 设备
- 数码摄像机
- 笔记本/平板电脑/电子阅读器
- 智能手机

3 说明

TPS22924x 是一款具有受控接通功能的小型、低 R_{ON} 的负载开关。此器件包含一个 N 通道 MOSFET，此 MOSFET 可运行在 0.75V 至 3.6V 的输入电压范围内。一个集成的电荷泵把 NMOS 开关偏置，以实现一个最小的开关导通电阻。此开关可由一个打开/关闭输入 (ON) 控制，此输入可与低压控制信号直接对接。

为能够在开关关闭时快速进行输出放电，添加了一个 1250Ω 的片上负载电阻。此器件的上升时间受到内部控制以避免出现浪涌电流。TPS22924B 在 $V_{IN} = 3.6V$ 时的上升时间为 100μs，而 TPS22924C 在 $V_{IN} = 3.6V$ 时的上升时间为 800μs。

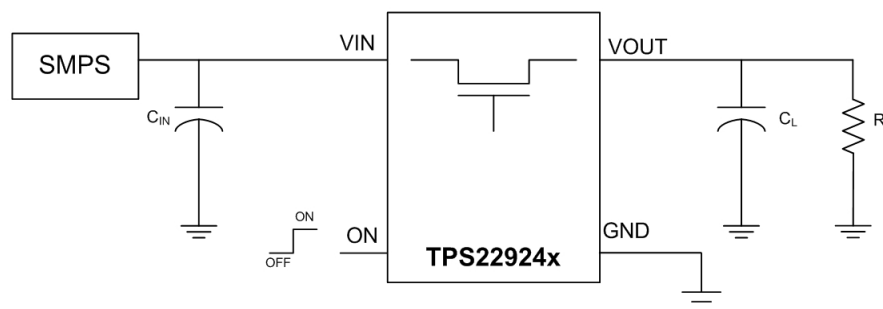
TPS22924x 采用超小型、节省空间的 6 引脚 CSP 封装，并可在 -40°C 至 85°C 温度范围内的自然通风条件下运行。

器件信息 (1)

部件号	封装	封装尺寸 (标称值)
TPS22924B	DSBGA (6)	1.40mm x 0.90mm
TPS22924C	DSBGA (6)	1.40mm x 0.90mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



NOTE: SMPS = 开关模式电源



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (August 2014) to Revision E	Page
• 已添加器件 TPS22924C	1
• 已删除特性: $V_{IN} = 2.5\text{ V}$ 时, $r_{ON} = 18.5\text{ m}\Omega$	1
• 已删除特性: $V_{IN} = 1.0\text{ V}$ 时, $r_{ON} = 20.3\text{ m}\Omega$	1
• 已添加文本至说明“而 TPS22924C 在 $V_{IN} = 3.6\text{ V}$ 时的上升时间为 $800\mu\text{s}$ 。”	1
• Added: TPS22924CYZPR and TPS22924CYZPRB information to Device Comparison Table	3
• Added "Storage temperature" to the Absolute Maximum Ratings ⁽¹⁾ table	4
• Changed Handling Ratings to ESD Ratings	4
• Added section AC Characteristics (TPS22924C)	10
• Changed the Application Curve section	17

Changes from Revision C (July 2014) to Revision D	Page
• 已添加 引脚配置和功能部分 , 概述部分 , 特性描述部分 , 电源相关建议部分	1

Changes from Revision B (June 2013) to Revision C	Page
• 已添加 器件信息表	1
• Added Handling Ratings table	4
• Added Detailed Description section	14

5 Device Comparison Table

T _A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾	BACKSIDE COATING ⁽³⁾	RISE TIME AT VIN = 3.3V (TYP.)
–40°C to 85°C	YZ (0.4mm height)	TPS22924BYZR	___ 5N _	No	96µs
–40°C to 85°C	YZP (0.5mm height)	TPS22924BYZPRB	___ 5N _	Yes	96µs
–40°C to 85°C	YZZ (0.35mm height)	TPS22924BYZZR	___ 7A _	No	96µs
–40°C to 85°C	YZP (0.5mm height)	TPS22924CZPZR	___ 5L _	No	800µs
–40°C to 85°C	YZP (0.4mm height)	TPS22924CZPRB	___ 5L _	Yes	800µs

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).
- (3) CSP (DSBGA) devices manufactured with backside coating have an increased resistance to cracking due to the increased physical strength of the package. Devices with backside coating are highly encouraged for new designs.

6 Pin Configuration and Functions

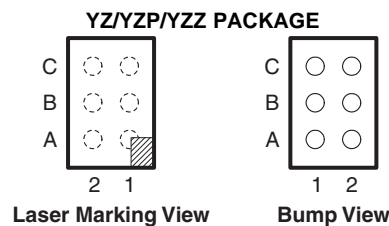


Table 1. Pin Assignments (YZ/YZP/YZZ Package)

C	GND	ON
B	VOUT	VIN
A	VOUT	VIN
	1	2

Pin Functions

NO.	NAME	DESCRIPTION
C1	GND	Ground
C2	ON	Switch control input, active high. Do not leave floating
A1, B1	VOUT	Switch output
A2, B2	VIN	Switch input, bypass this input with a ceramic capacitor to ground

7 Specifications

7.1 Absolute Maximum Ratings ⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage range	-0.3	4	V
V _{OUT}	Output voltage range		V _{IN} + 0.3	V
V _{ON}	Input voltage range	-0.3	4	V
I _{MAX}	Maximum continuous switch current, T _A = -40°C to 85°C		2	A
I _{PLS}	Maximum pulsed switch current, 100-μs pulse, 2% duty cycle, T _A = -40°C to 85°C		4	A
T _A	Operating free-air temperature range	-40	85	°C
T _{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±5000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{IN}	Input voltage		0.75	3.6	V
V _{OUT}	Output voltage			V _{IN}	V
V _{IH}	High-level input voltage, ON	V _{IN} = 2.5 V to 3.6 V	1.2	3.6	V
		V _{IN} = 0.75 V to 2.5 V	0.9	3.6	
V _{IL}	Low-level input voltage, ON	V _{IN} = 2.5 V to 3.6 V		0.6	V
		V _{IN} = 0.75 V to 2.49 V		0.4	
C _{IN}	Input capacitance		1 ⁽¹⁾		μF

(1) See the [Input Capacitor](#) section in Application Information.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22924x	UNIT
		YZ/YZZ/YZP	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	123	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	17.6	
R _{θJB}	Junction-to-board thermal resistance	22.8	
Ψ _{JT}	Junction-to-top characterization parameter	5.7	
Ψ _{JB}	Junction-to-board characterization parameter	22.6	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report, [SPRA953](#).

7.5 Electrical Characteristics

 $V_{IN} = 0.75\text{ V to }3.6\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP (1)	MAX	UNIT
I_{IN}	Quiescent current	$I_{OUT} = 0, V_{IN} = V_{ON}$	Full		75	160	μA
					42	70	
					50	350	
					95	200	
					65	110	
					35	70	
$I_{IN(LEAK)}$	OFF-state supply current	$V_{ON} = \text{GND}, \text{OUT} = 0\text{V}$	Full			3.5	μA
R_{ON}	ON-state resistance	$I_{OUT} = -200\text{ mA}$	25°C	Full	18.3	19.7	$\text{m}\Omega$
					26.0		
			25°C	Full	18.5	19.5	
					25.8		
			25°C	Full	19.6	21.8	
					27.4		
			25°C	Full	19.4	21.8	
					28.0		
25°C	Full	20.3	21.2				
		28.6					
25°C	Full	22.7	25.3				
		34.8					
R_{PD}	Output pulldown resistance (2)	$V_{IN} = 3.3\text{ V}, V_{ON} = 0, I_{OUT} = 3\text{ mA}$	25°C		1250	1500	Ω
I_{ON}	ON-state input leakage current	$V_{ON} = 0.9\text{ V to }3.6\text{ V or GND}$	Full			0.1	μA

(1) Typical values are at $V_{IN} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) See [Output Pulldown](#) in the Application and Implementation section.

7.6 Switching Characteristics, $V_{IN} = 3.6\text{ V}$

 $V_{IN} = 3.6\text{ V}, T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPS22924B (TYP)	TPS22924C (TYP)	UNIT
t_{ON}	Turn-ON time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 3.6\text{V}$	111	800	μs
t_{OFF}	Turn-OFF time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 3.6\text{V}$	3	3	μs
t_r	V_{OUT} rise time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 3.6\text{V}$	96	800	μs
t_f	V_{OUT} fall time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 3.6\text{V}$	2.5	2.5	μs

7.7 Switching Characteristics, $V_{IN} = 0.9\text{ V}$

 $V_{IN} = 0.9\text{ V}, T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPS22924B (TYP)	TPS22924C (TYP)	UNIT
t_{ON}	Turn-ON time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 0.9\text{V}$	160	865	μs
t_{OFF}	Turn-OFF time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 0.9\text{V}$	20	20	μs
t_r	V_{OUT} rise time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 0.9\text{V}$	81	500	μs
t_f	V_{OUT} fall time	$R_L = 10\ \Omega, C_L = 0.1\ \mu\text{F}, V_{IN} = 0.9\text{V}$	5	5	μs

7.8 Typical Characteristics

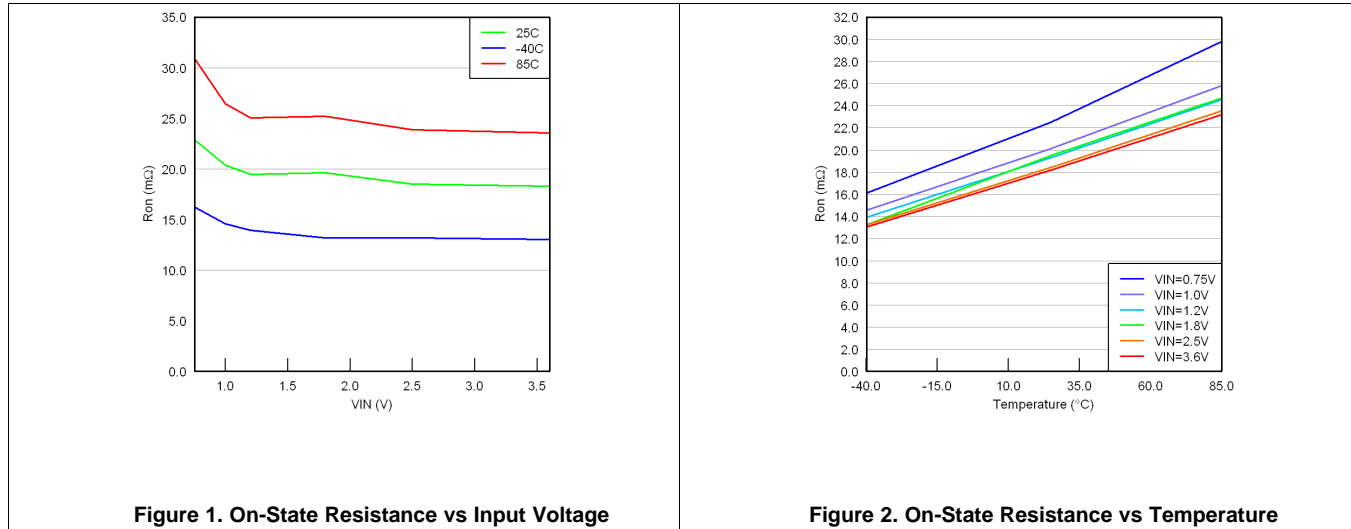


Figure 1. On-State Resistance vs Input Voltage

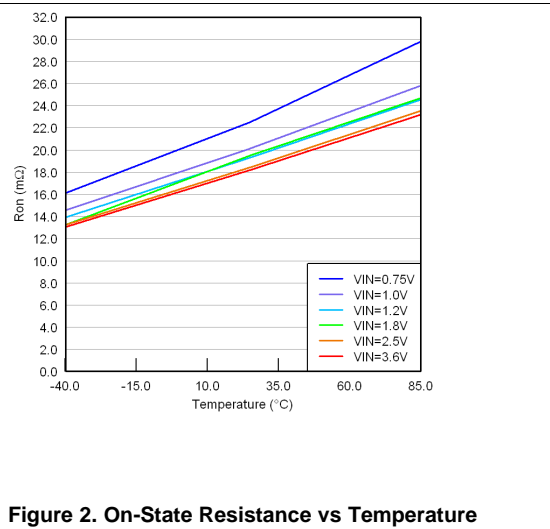


Figure 2. On-State Resistance vs Temperature

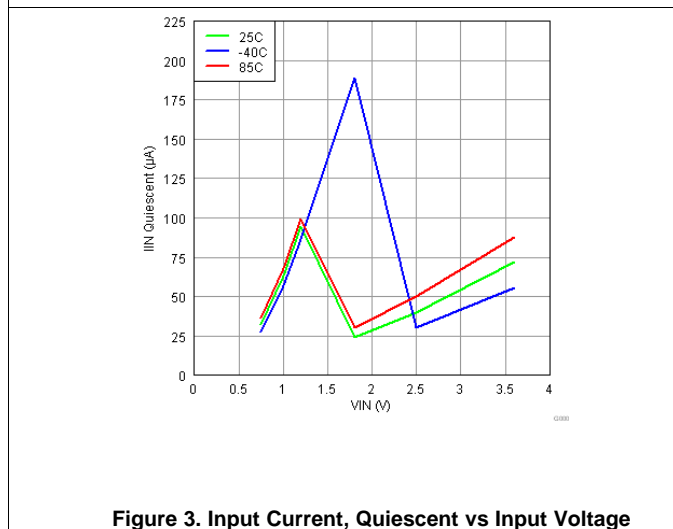


Figure 3. Input Current, Quiescent vs Input Voltage

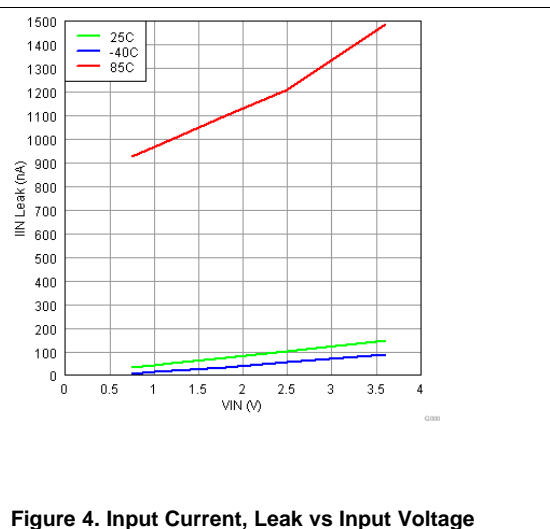


Figure 4. Input Current, Leak vs Input Voltage

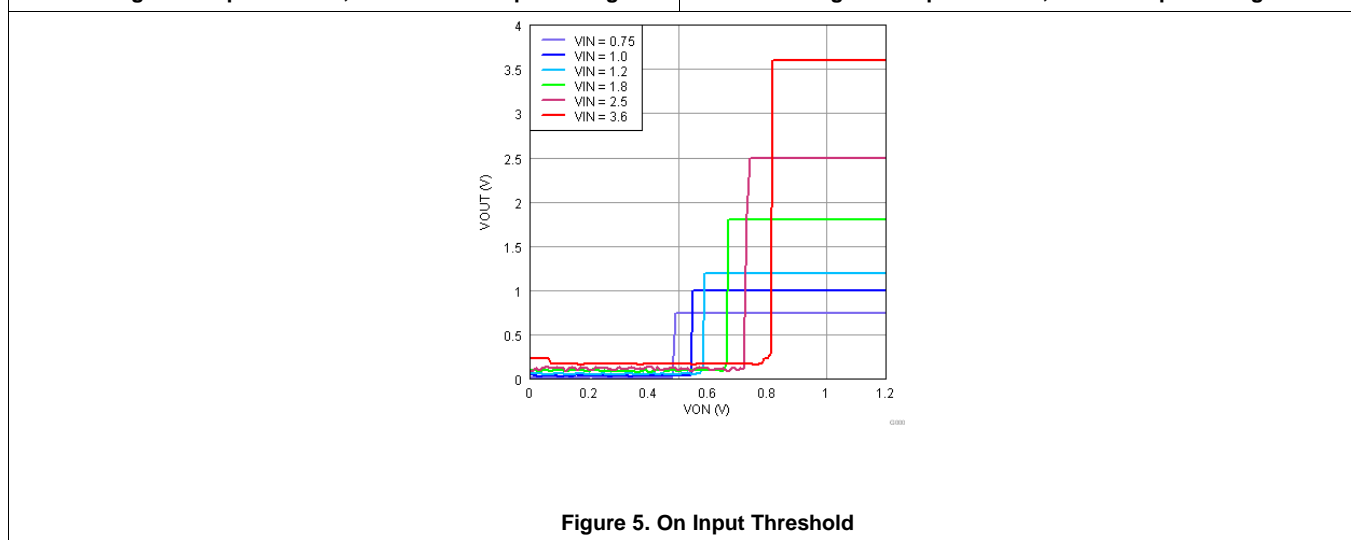
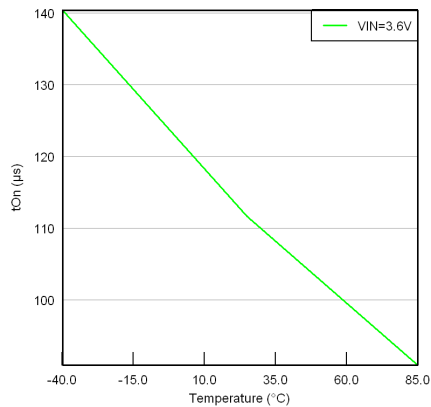


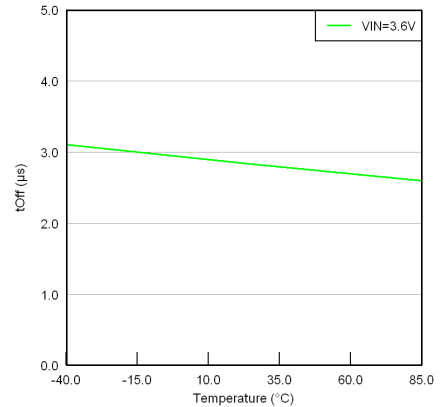
Figure 5. On Input Threshold

7.9 AC Characteristics (TPS22924B)



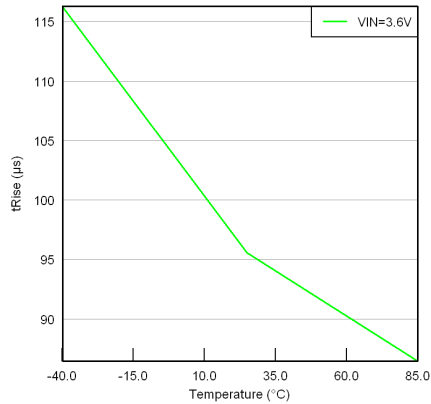
$V_{IN} = 3.6\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 6. Turn-On Time vs Temperature



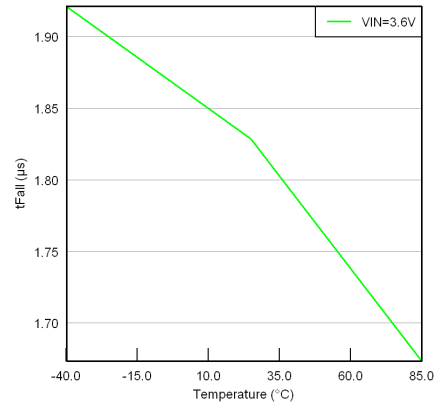
$V_{IN} = 3.6\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 7. Turn-Off Time vs Temperature



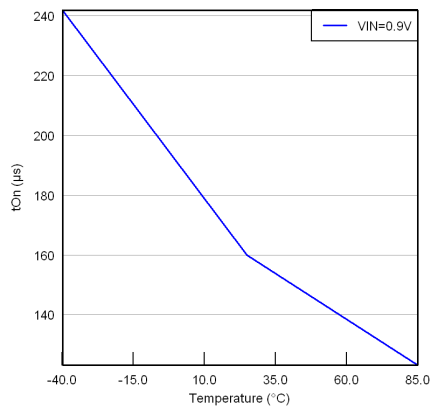
$V_{IN} = 3.6\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 8. Rise Time vs Temperature



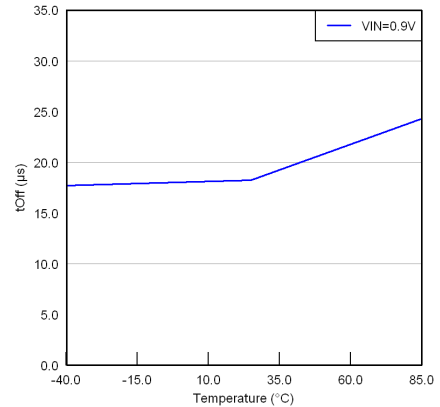
$V_{IN} = 3.6\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 9. Fall Time vs Temperature



$V_{IN} = 0.9\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

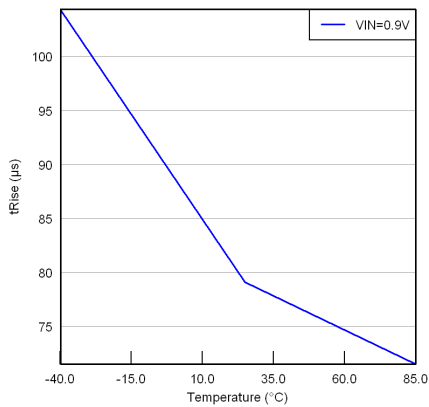
Figure 10. Turn-On Time vs Temperature



$V_{IN} = 0.9\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

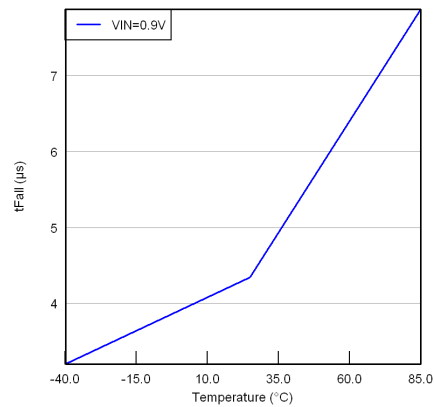
Figure 11. Turn-Off Time vs Temperature

AC Characteristics (TPS22924B) (continued)



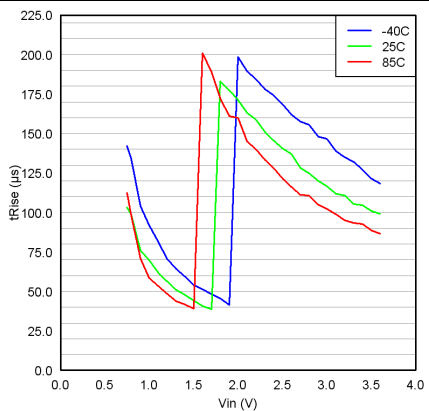
$V_{IN} = 0.9\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 12. Rise Time vs Temperature



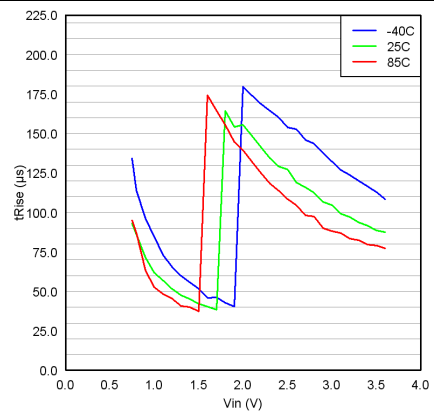
$V_{IN} = 0.9\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 13. Fall Time vs Temperature



$V_{ON} = 1.8\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 14. Rise Time vs Input Voltage



$V_{ON} = 1.8\text{ V}$, $C_L = 20\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 15. Rise Time vs Input Voltage

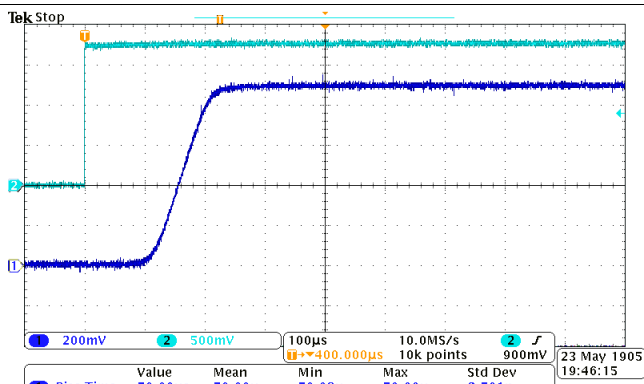


Figure 16. Turn-On Response

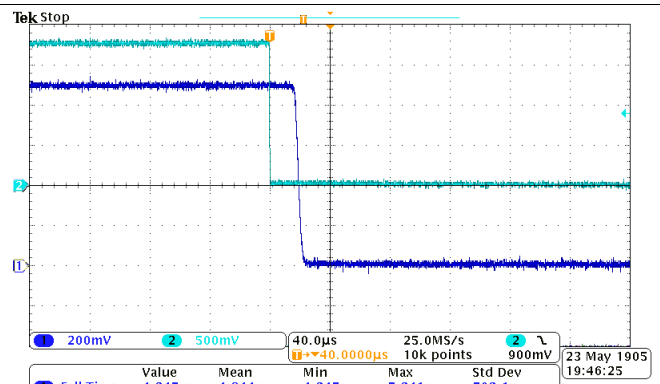


Figure 17. Turn-Off Response

AC Characteristics (TPS22924B) (continued)

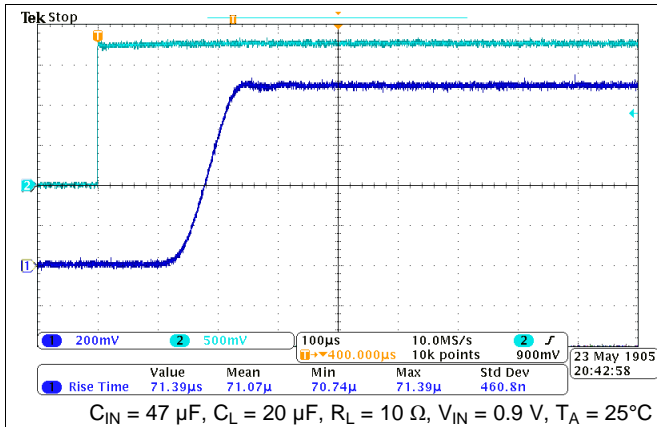


Figure 18. Turn-On Response

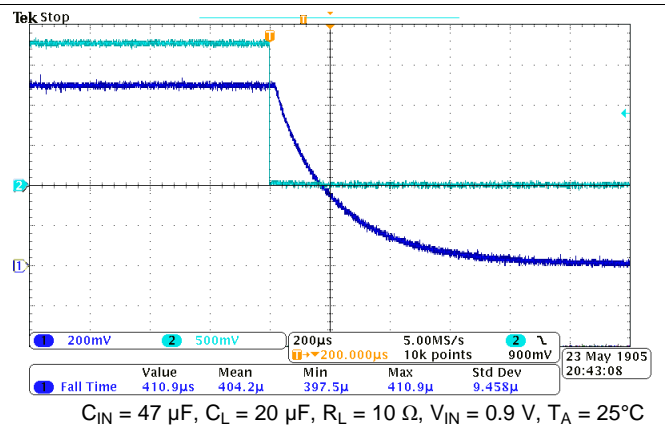


Figure 19. Turn-Off Response

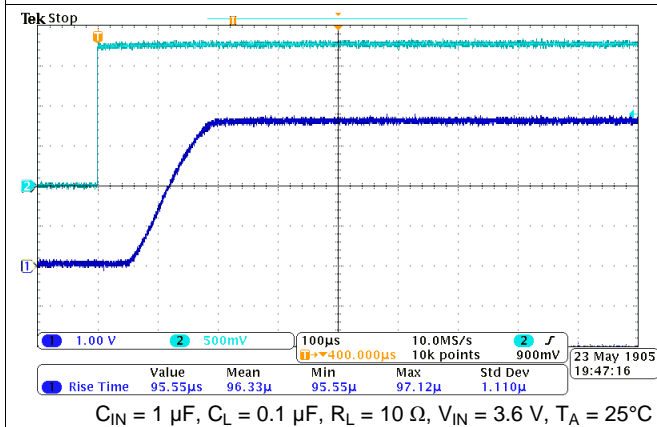


Figure 20. Turn-On Response

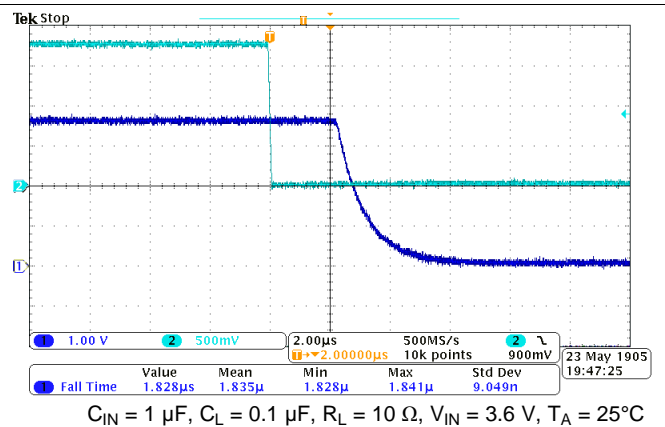


Figure 21. Turn-Off Response

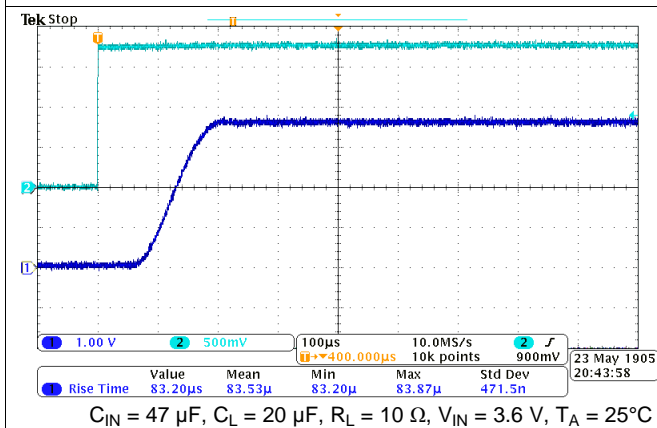


Figure 22. Turn-On Response

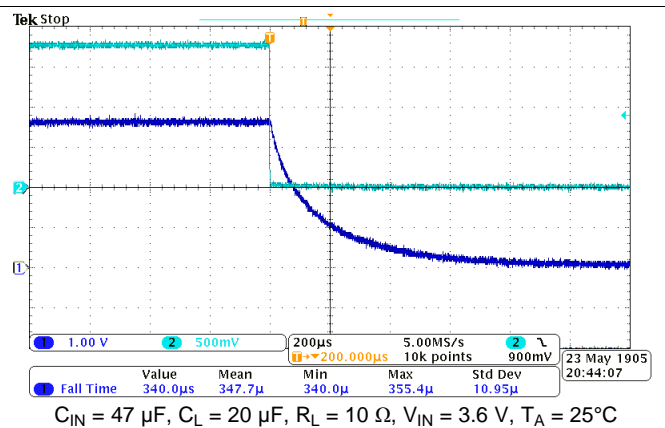
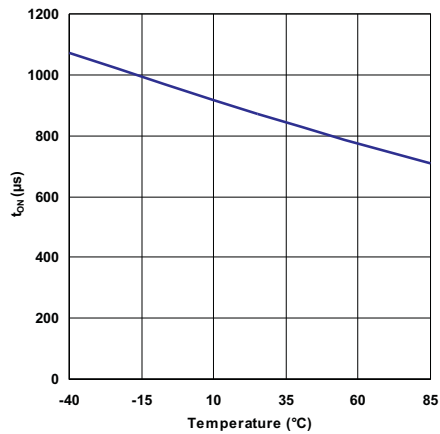
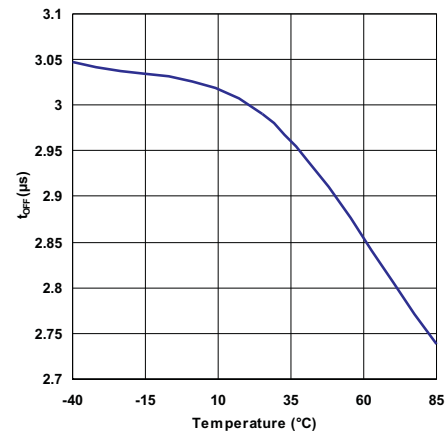
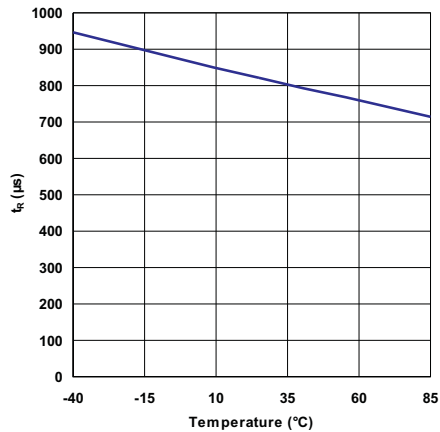
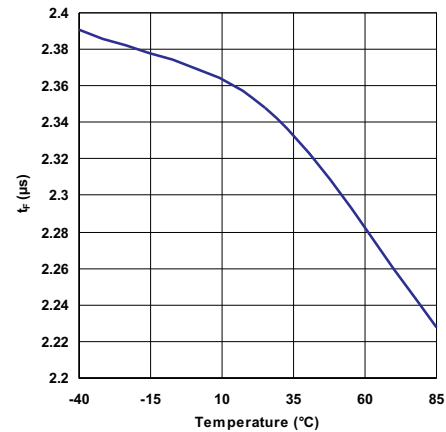
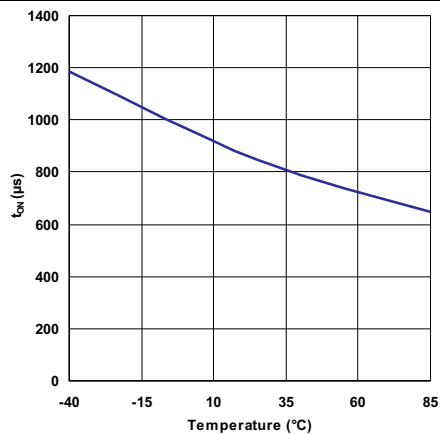
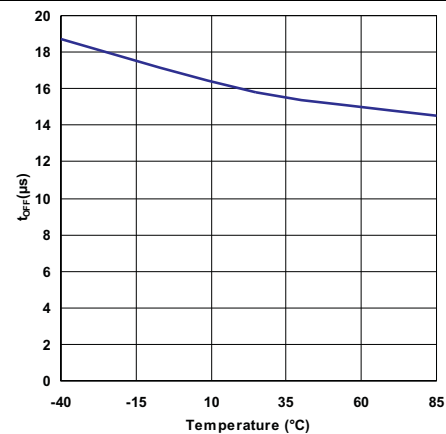
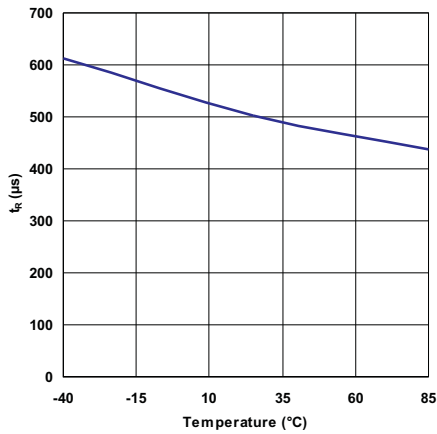


Figure 23. Turn-Off Response

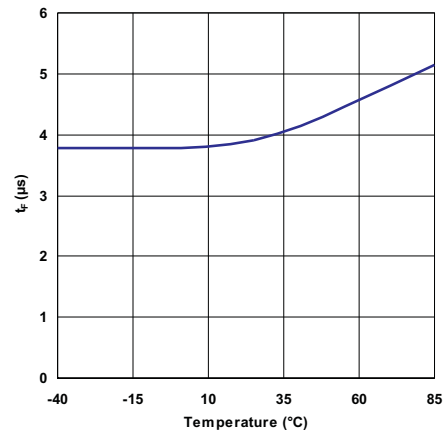
7.10 AC Characteristics (TPS22924C)

 $V_{IN} = 3.6\text{ V}, C_L = 0.1\ \mu\text{F}, R_L = 10\ \Omega$
Figure 24. Turn-On Time vs Temperature

 $V_{IN} = 3.6\text{ V}, C_L = 0.1\ \mu\text{F}, R_L = 10\ \Omega$
Figure 25. Turn-Off Time vs Temperature

 $V_{IN} = 3.6\text{ V}, C_L = 0.1\ \mu\text{F}, R_L = 10\ \Omega$
Figure 26. Rise Time vs Temperature

 $V_{IN} = 3.6\text{ V}, C_L = 0.1\ \mu\text{F}, R_L = 10\ \Omega$
Figure 27. Fall Time vs Temperature

 $V_{IN} = 0.9\text{ V}, C_L = 0.1\ \mu\text{F}, R_L = 10\ \Omega$
Figure 28. Turn-On Time vs Temperature

 $V_{IN} = 0.9\text{ V}, C_L = 0.1\ \mu\text{F}, R_L = 10\ \Omega$
Figure 29. Turn-Off Time vs Temperature

AC Characteristics (TPS22924C) (continued)



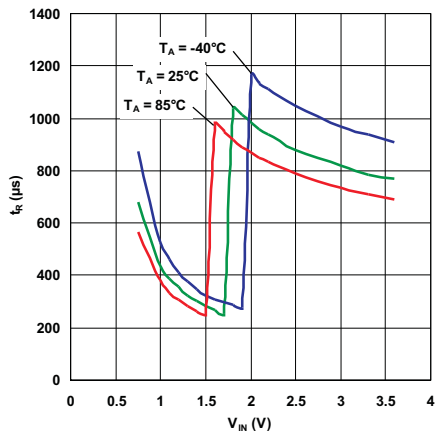
$V_{IN} = 0.9\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 30. Rise Time vs Temperature



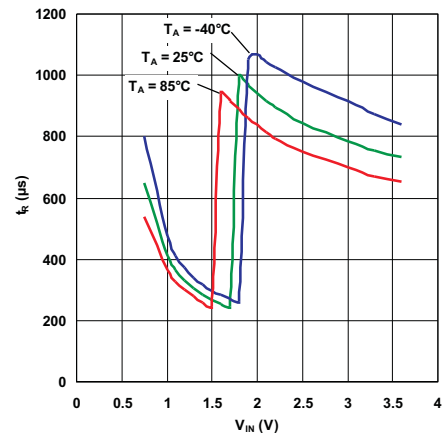
$V_{IN} = 0.9\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 31. Fall Time vs Temperature



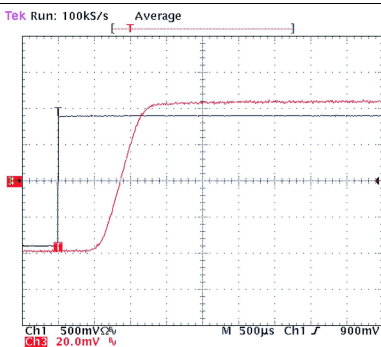
$V_{ON} = 1.8\text{ V}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 32. Rise Time vs Input Voltage



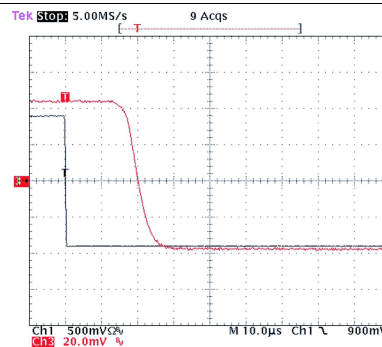
$V_{ON} = 1.8\text{ V}$, $C_L = 20\ \mu\text{F}$, $R_L = 10\ \Omega$

Figure 33. Rise Time vs Input Voltage



$C_{IN} = 1\ \mu\text{F}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$, $V_{IN} = 0.9\text{ V}$, $T_A = 25^\circ\text{C}$

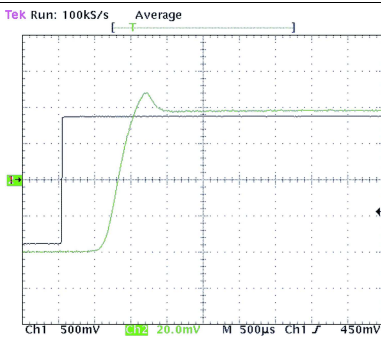
Figure 34. Turn-On Response



$C_{IN} = 1\ \mu\text{F}$, $C_L = 0.1\ \mu\text{F}$, $R_L = 10\ \Omega$, $V_{IN} = 0.9\text{ V}$, $T_A = 25^\circ\text{C}$

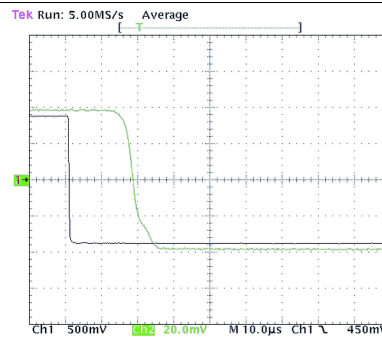
Figure 35. Turn-Off Response

AC Characteristics (TPS22924C) (continued)



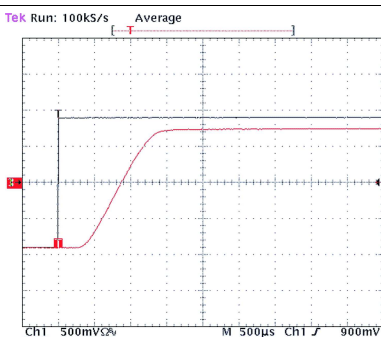
$C_{IN} = 47 \mu\text{F}$, $C_L = 20 \mu\text{F}$, $R_L = 10 \Omega$, $V_{IN} = 0.9 \text{ V}$, $T_A = 25^\circ\text{C}$

Figure 36. Turn-On Response



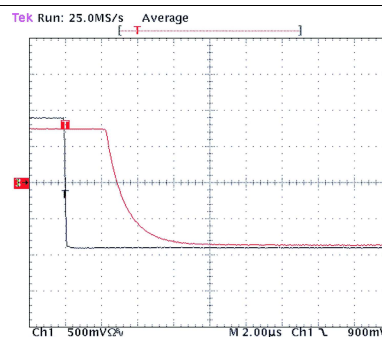
$C_{IN} = 47 \mu\text{F}$, $C_L = 20 \mu\text{F}$, $R_L = 10 \Omega$, $V_{IN} = 0.9 \text{ V}$, $T_A = 25^\circ\text{C}$

Figure 37. Turn-Off Response



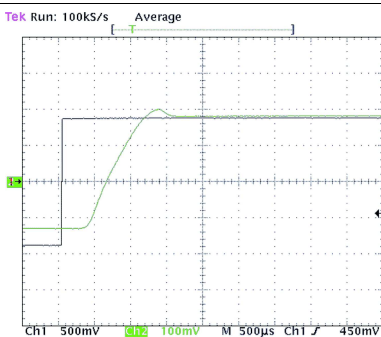
$C_{IN} = 1 \mu\text{F}$, $C_L = 0.1 \mu\text{F}$, $R_L = 10 \Omega$, $V_{IN} = 3.6 \text{ V}$, $T_A = 25^\circ\text{C}$

Figure 38. Turn-On Response



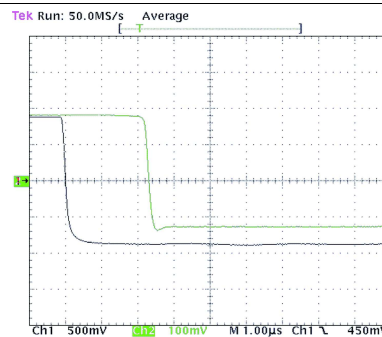
$C_{IN} = 1 \mu\text{F}$, $C_L = 0.1 \mu\text{F}$, $R_L = 10 \Omega$, $V_{IN} = 3.6 \text{ V}$, $T_A = 25^\circ\text{C}$

Figure 39. Turn-Off Response



$C_{IN} = 47 \mu\text{F}$, $C_L = 20 \mu\text{F}$, $R_L = 10 \Omega$, $V_{IN} = 3.6 \text{ V}$, $T_A = 25^\circ\text{C}$

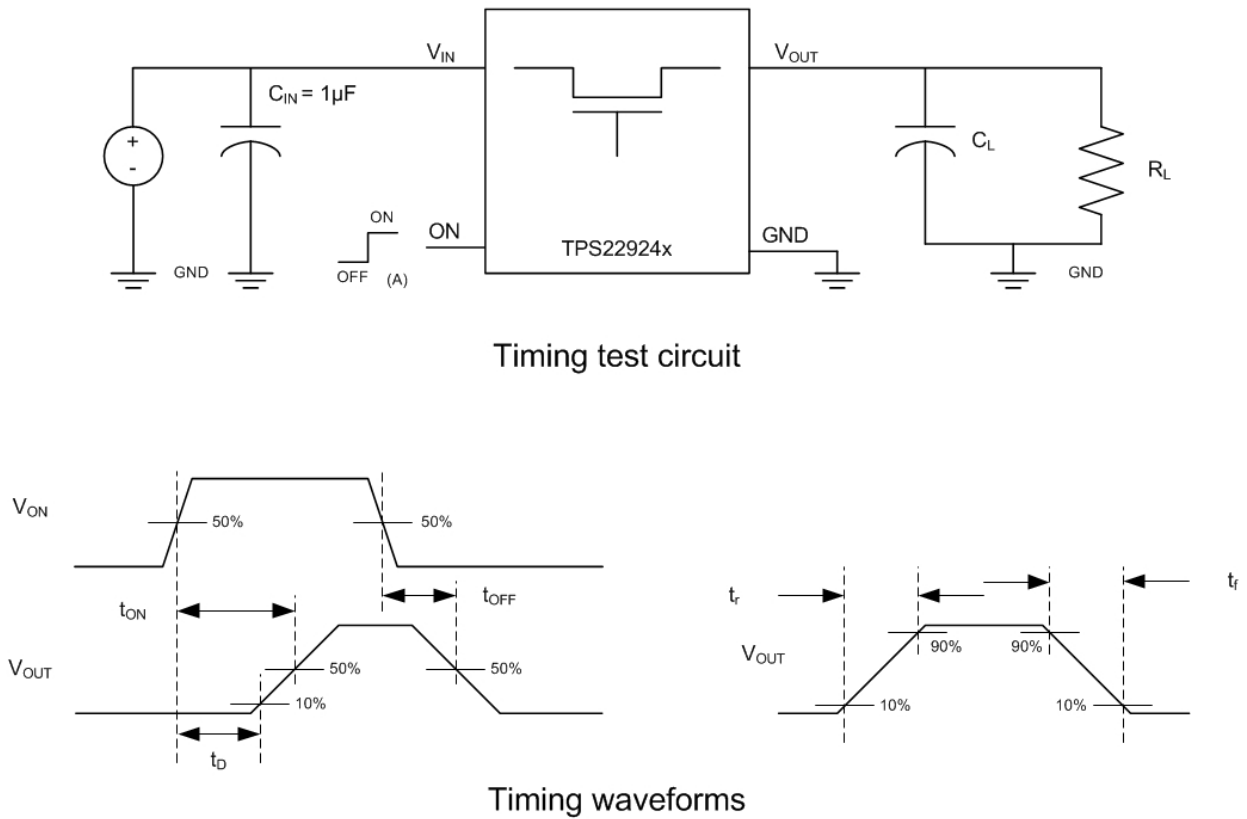
Figure 40. Turn-On Response



$C_{IN} = 47 \mu\text{F}$, $C_L = 20 \mu\text{F}$, $R_L = 10 \Omega$, $V_{IN} = 3.6 \text{ V}$, $T_A = 25^\circ\text{C}$

Figure 41. Turn-Off Response

8 Parameter Measurement Information



(A) Rise and fall times of the control signal is 100ns.

Figure 42. Test Circuit and t_{ON}/t_{OFF} Waveforms

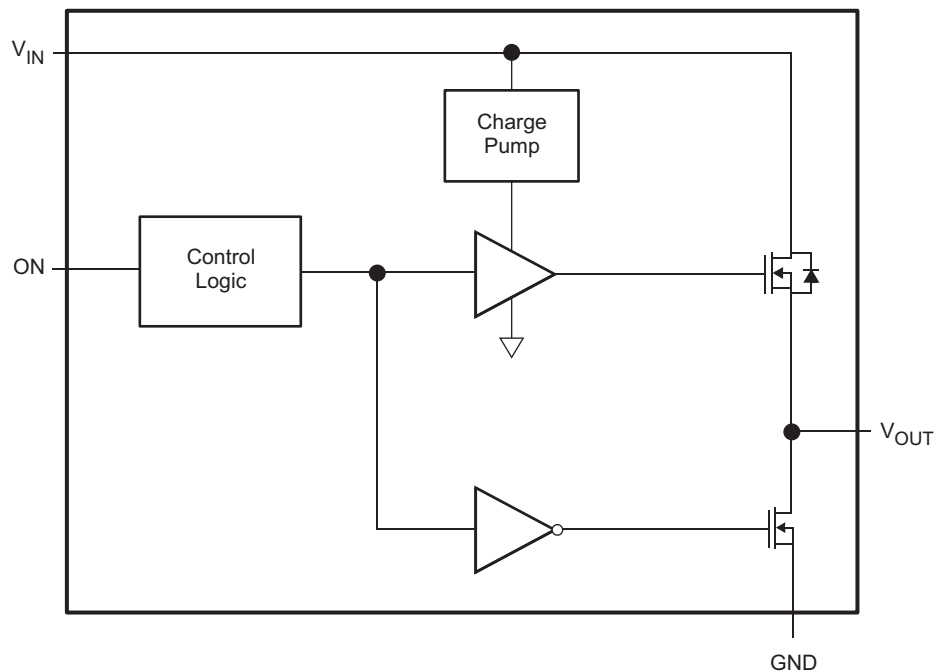
9 Detailed Description

9.1 Overview

The TPS22924x is a single channel, 2-A load switch in a small, space-saving CSP-6 package. This device implements a low resistance N-channel MOSFET with a controlled rise time for applications that need to limit the inrush current.

This device is also designed to have very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 ON/OFF Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

9.3.2 Output Capacitor

Due to the integral body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

9.3.3 Output Pulldown

The output pulldown is active when the user is turning off the main pass FET. The pulldown discharges the output rail to approximately 10% of the rail, then the output pulldown is automatically disconnected to optimize the shutdown current.

9.4 Device Functional Modes

ON (CONTROL SIGNAL)	VIN to VOUT	VOUT to GND ⁽¹⁾
L	OFF	ON
H	ON	OFF

(1) See application section [Output Pulldown](#) .

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN condition of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use [Equation 1](#) to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- ΔV = Voltage drop from VIN to VOUT
- I_{LOAD} = Load current
- R_{ON} = On-resistance of the device for a specific VIN
- An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated. (1)

10.1.2 Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents, when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

10.1.3 Output Capacitor

A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup.

10.2 Typical Application

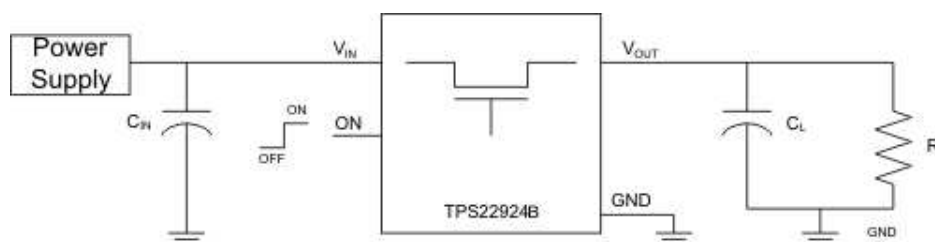


Figure 43. Typical Application

10.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
VIN	3.6 V
CL	1 μ F
Maximum Acceptable Inrush Current	40 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0-V to V_{IN} . This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$\text{Inrush Current} = C \times \frac{dv}{dt}$$

where

- C = Output capacitance
- $\frac{dv}{dt}$ = Output slew rate

The TPS22924B offers a very slow controlled rise time for minimizing inrush current. This device can be selected based upon the maximum acceptable slew rate which can be calculated using the design requirements and the inrush current equation. An output capacitance of 1.0 μF will be used since the amount of inrush increases with output capacitance:

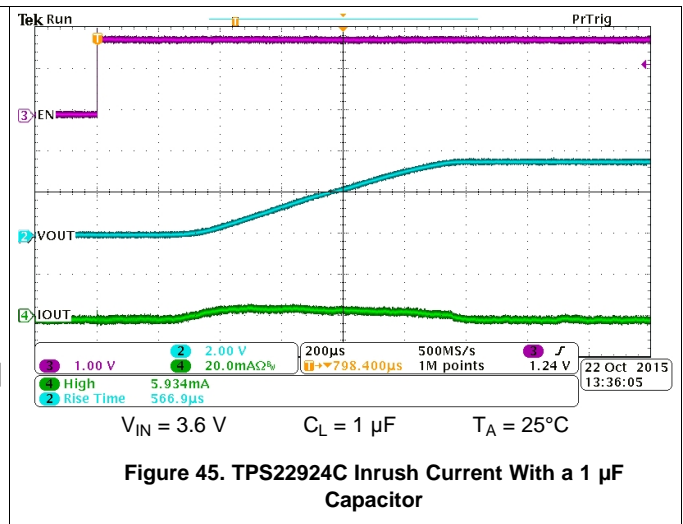
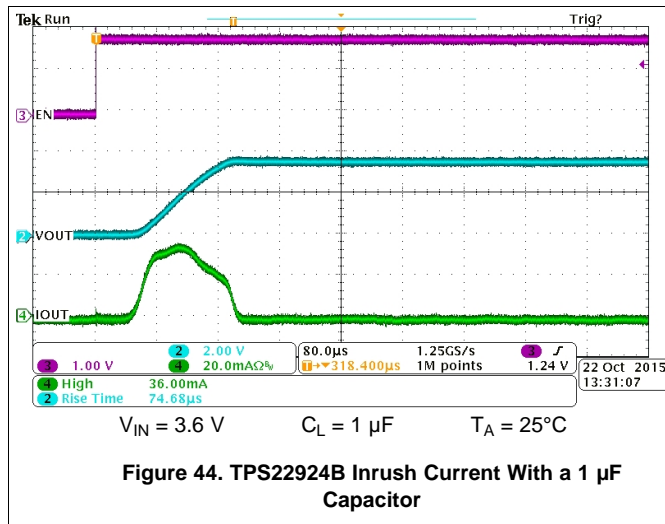
$$40 \text{ mA} = 1.0 \mu\text{F} \times \frac{dv}{dt} \tag{3}$$

$$\frac{dv}{dt} = 40 \text{ V/ms} \tag{4}$$

To ensure an inrush current of less than 40 mA, a device with a slew rate less than 40 V/ms must be used.

The TPS22924B has a typical rise time of 96 μs at 3.6 V. This results in a slew rate of 37.5 V/ms which meets the above design requirements. For an even lower inrush current requirement, the TPS22924C can be used. The slower rise time of 800 μs at 3.6V results in a slew rate of 4.5 V/ms, well below the design requirements.

10.2.3 Application Curve



11 Power Supply Recommendations

The device is designed to operate with a V_{IN} range of 0.75 V to 3.6 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1 μF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 μF may be sufficient.

12 Layout

12.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN} , V_{OUT} , and GND helps minimize the parasitic electrical effects.

12.2 Layout Example

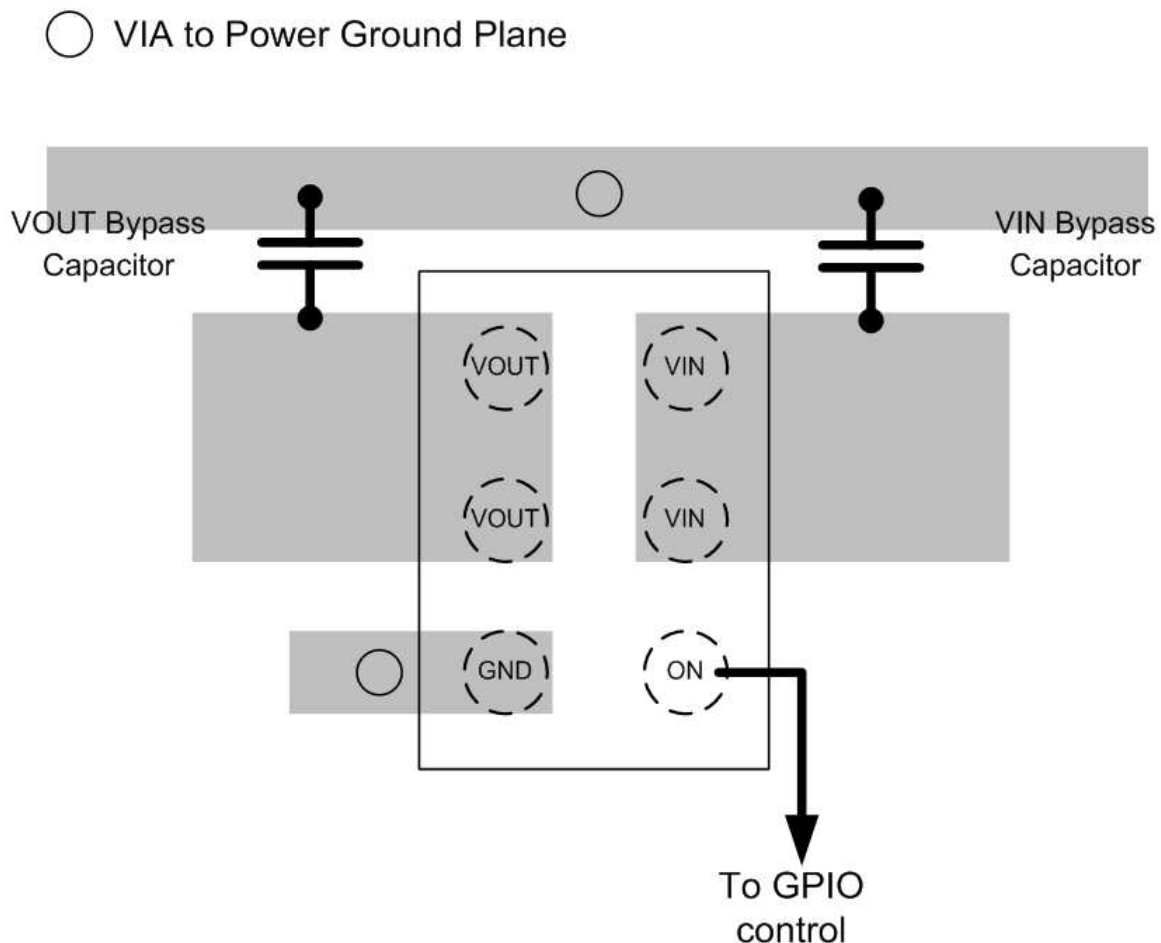


Figure 46. TPS22924x Layout Example

13 器件和文档支持

13.1 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

表 2. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS22924B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS22924C	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 商标

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13.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22924BYZPRB	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5N	Samples
TPS22924BYZR	ACTIVE	DSBGA	YZ	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5N	Samples
TPS22924BYZT	ACTIVE	DSBGA	YZ	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5N	Samples
TPS22924BYZZR	ACTIVE	DSBGA	YZZ	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7A	Samples
TPS22924BYZZT	ACTIVE	DSBGA	YZZ	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7A	Samples
TPS22924CYZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(5L, 5LG)	Samples
TPS22924CYZPRB	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5L	Samples
TPS22924CYZPT	ACTIVE	DSBGA	YZP	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(5LF, 5LG)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22924BYZPRB	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924BYZR	DSBGA	YZ	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924BYZT	DSBGA	YZ	6	250	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924BYZZR	DSBGA	YZZ	6	3000	178.0	9.2	1.02	1.52	0.5	4.0	8.0	Q1
TPS22924BYZZT	DSBGA	YZZ	6	250	178.0	9.2	1.02	1.52	0.5	4.0	8.0	Q1
TPS22924CYZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924CYZPRB	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924CYZPT	DSBGA	YZP	6	250	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

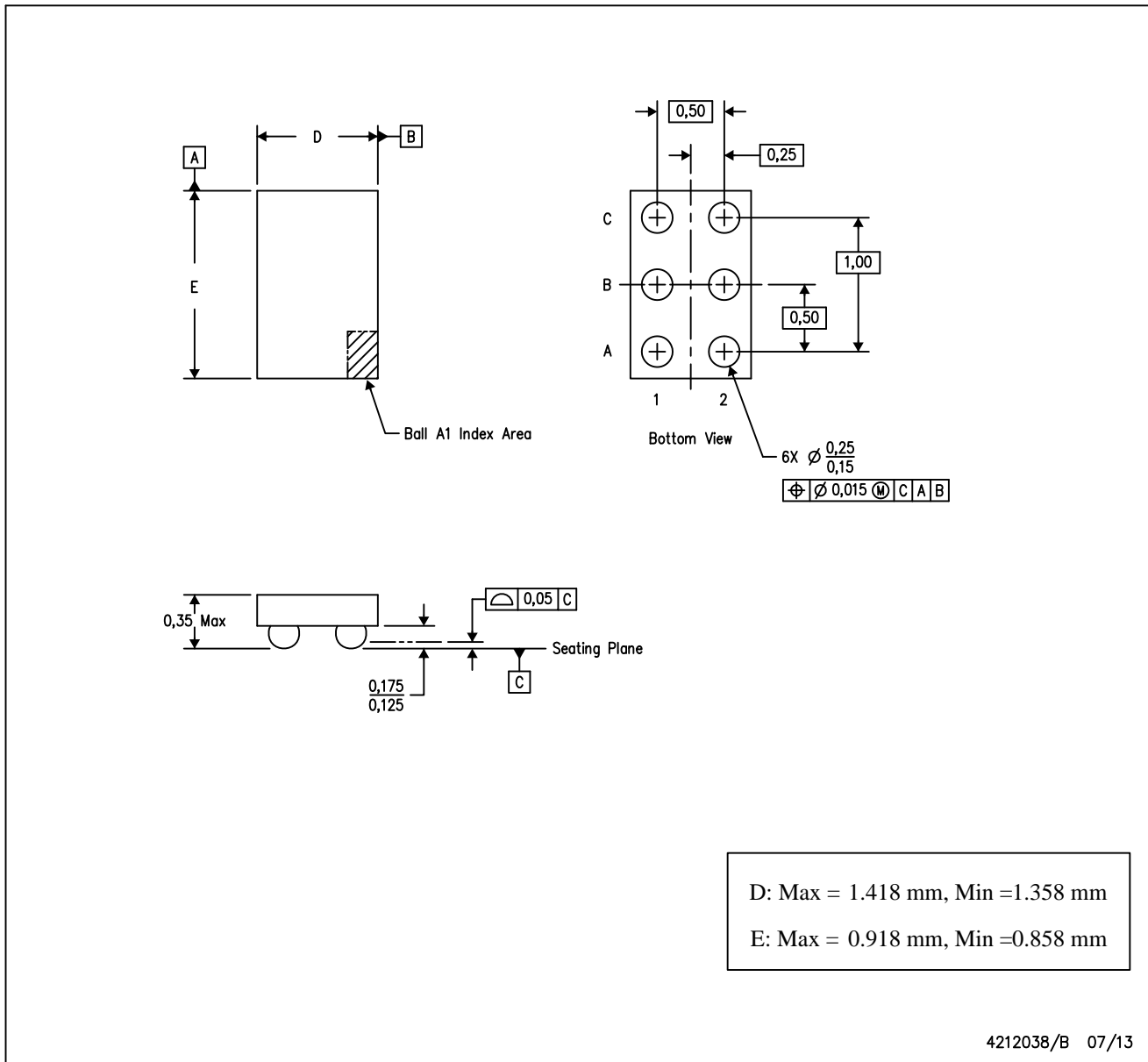
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22924BYZPRB	DSBGA	YZP	6	3000	220.0	220.0	35.0
TPS22924BYZR	DSBGA	YZ	6	3000	220.0	220.0	35.0
TPS22924BYZT	DSBGA	YZ	6	250	220.0	220.0	35.0
TPS22924BYZZR	DSBGA	YZZ	6	3000	220.0	220.0	35.0
TPS22924BYZZT	DSBGA	YZZ	6	250	220.0	220.0	35.0
TPS22924CYZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0
TPS22924CYZPRB	DSBGA	YZP	6	3000	220.0	220.0	35.0
TPS22924CYZPT	DSBGA	YZP	6	250	220.0	220.0	35.0

YZZ (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

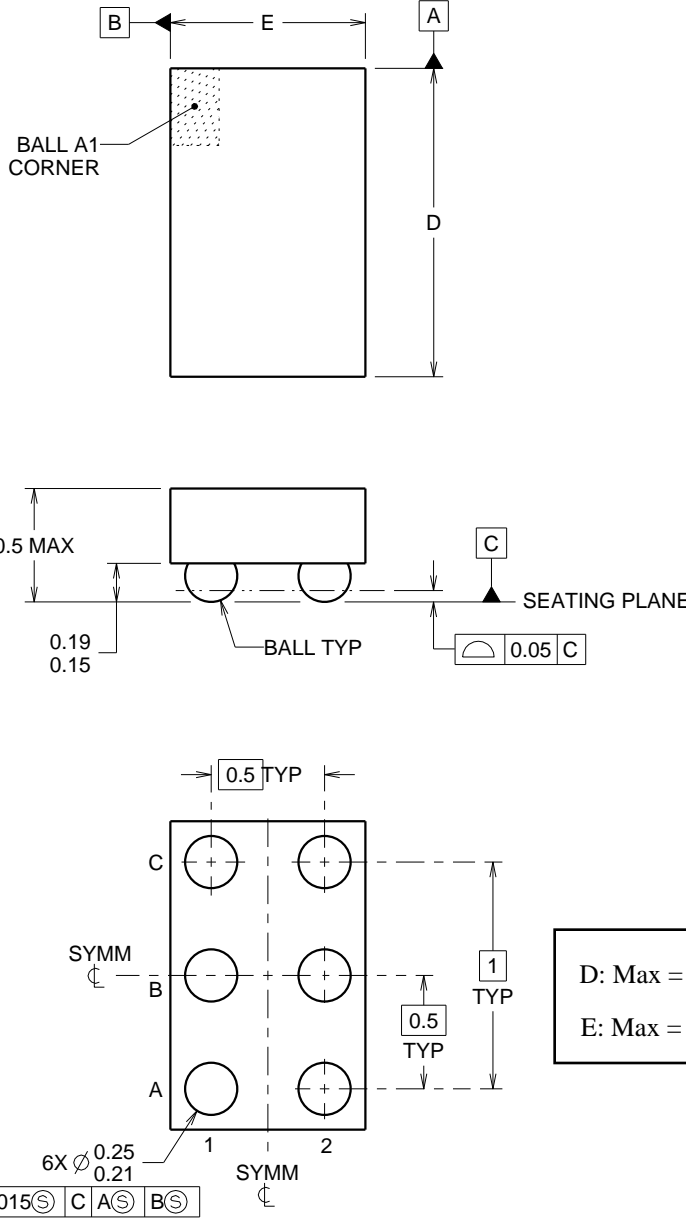
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm
 E: Max = 0.918 mm, Min = 0.858 mm

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NOTES:

NanoFree Is a trademark of Texas Instruments.

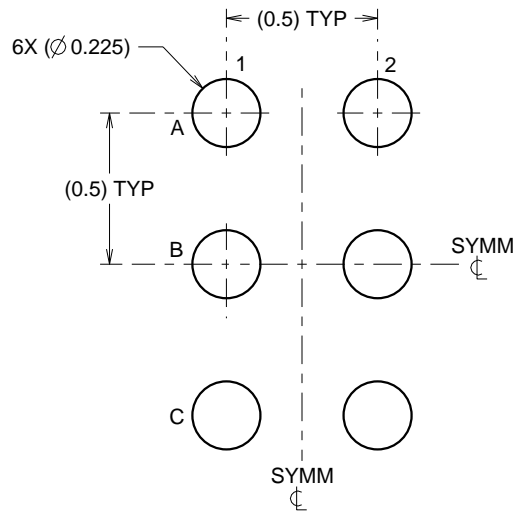
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

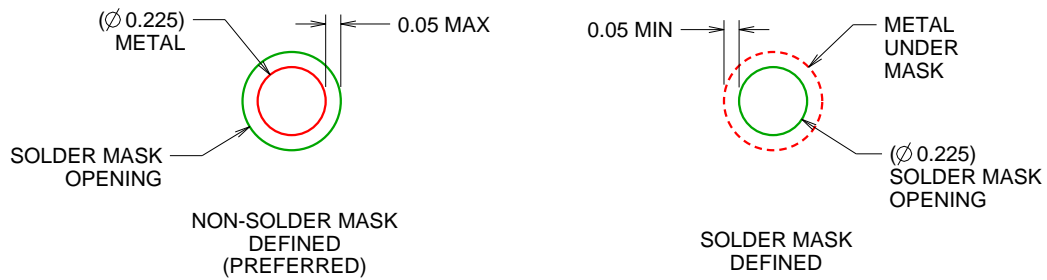
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

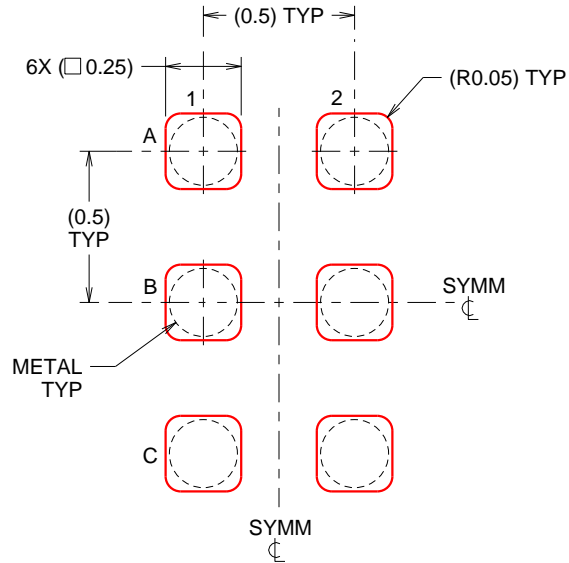
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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